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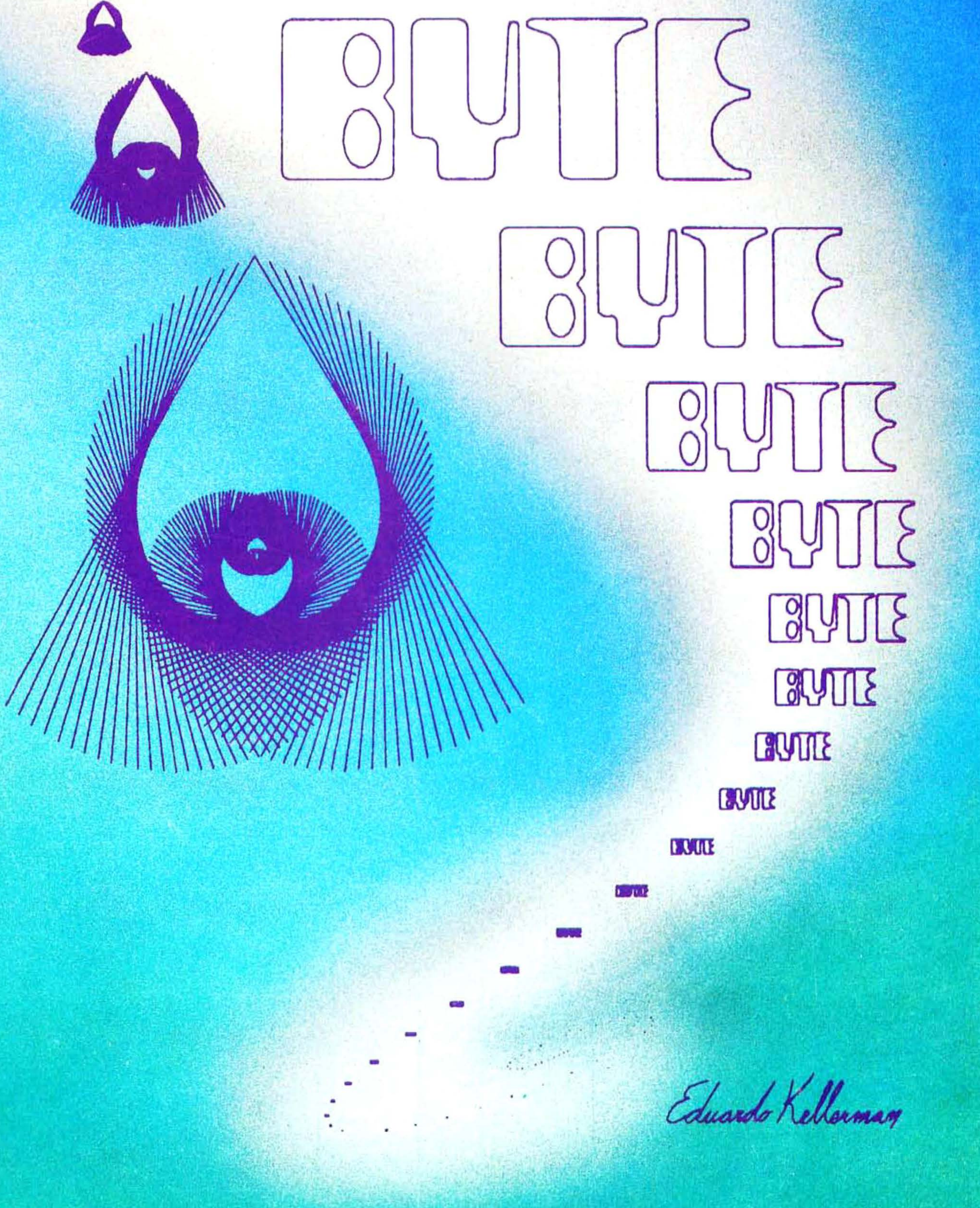

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BYTE September 1978
Volume 3 Number 9

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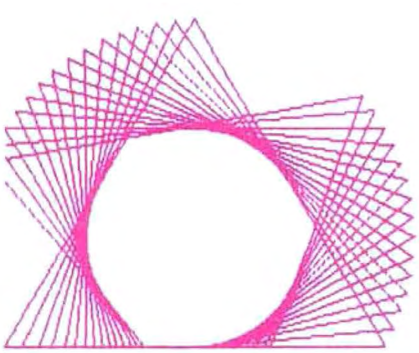
In This BYTE

About the Cover...

The computer artwork for the cover of this issue of BYTE is the work of Ed Kellerman, whose article appears on page 40. It was done using the facilities of IBM in Endicott NY, with the APL language as the major tool and a Tektronix plotter for producing the black images for the various colors of the line drawing component of the cover.

But we looked at the resulting artwork, and then asked Ed if he would allow us to provide some additional hand coloration by Ellen Shamonsky of our art department. (Ellen is the person responsible for the airbrush work on July 1978's cover, which we forgot to credit in that issue.) Ellen provided the multicolored airbrush background for the present cover, using the artwork supplied by Ed as the guide for positioning the various zones.

A background in vectors and matrices can give you a set of powerful tools for manipulating shapes on a graphics display. Read Jeffrey L Posdamer's **The Mathematics of Computer Graphics**. You may find that the mathematics is not as difficult as you think. *page 22*



As other articles in this issue demonstrate, matrix operations are one method of manipulating graphics. The manipulations become simpler when the implementation language is designed to work with matrices. APL is such a language. Eduardo Kellerman gives us a taste of what happens when you mix **APL and Graphics**. *page 40*

In this issue Kin-Man Chung and Herbert Yuen start a series of articles detailing the design and construction of **A "Tiny" Pascal**. Part 1 contains an overall view of the project along with a detailed look at an interpreter for pseudocode which is what the Pascal source program will be compiled into. The Pascal project emphasizes the portability of the language by compiling from Pascal to pseudocode which will then have an individual interpreter for every different machine. *page 58*

What constitutes a program, and what is the proper way to write one? Proper is a loaded word, but if ease of thought and unambiguity are goals of the effort, **Some Words About Program Structure** by Albert D Hearn will be a good starting point for the novice. *page 68*

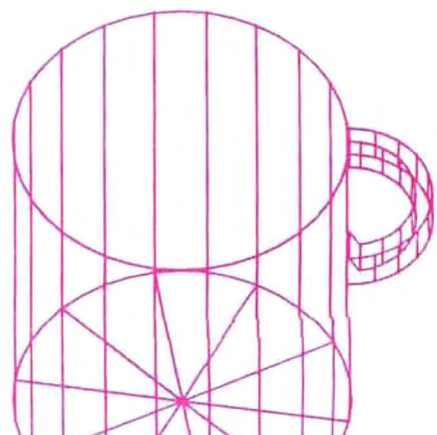
This month we conclude Dr James Williams's three part series on **Antique Mechanical Computers** with **Part 3: The Torres Chess Automaton**. Incredible as it may seem, Leonardo Torres built a working chess automaton in 1911. After a discussion about early concepts in the first "thinking" machines, the chess automaton is described in detail in this article. Dr Williams concludes the series with some philosophical speculations about automata. *page 82*

Steve Ciarcia completes his description of a non-contact scanner by describing the software that will **Let Your Fingers Do the Talking.** *page 94*

In an extended Technical Forum discussion, Jonathan Bondy presents a preliminary design for **S2L: An Altair (S-100) to LSI-11 Bus Adapter.** Here is a starting point for those interested in taking advantage of numerous personal computing peripherals in combination with the 16 bit Digital Equipment Corporation LSI-11 computer. *page 102*

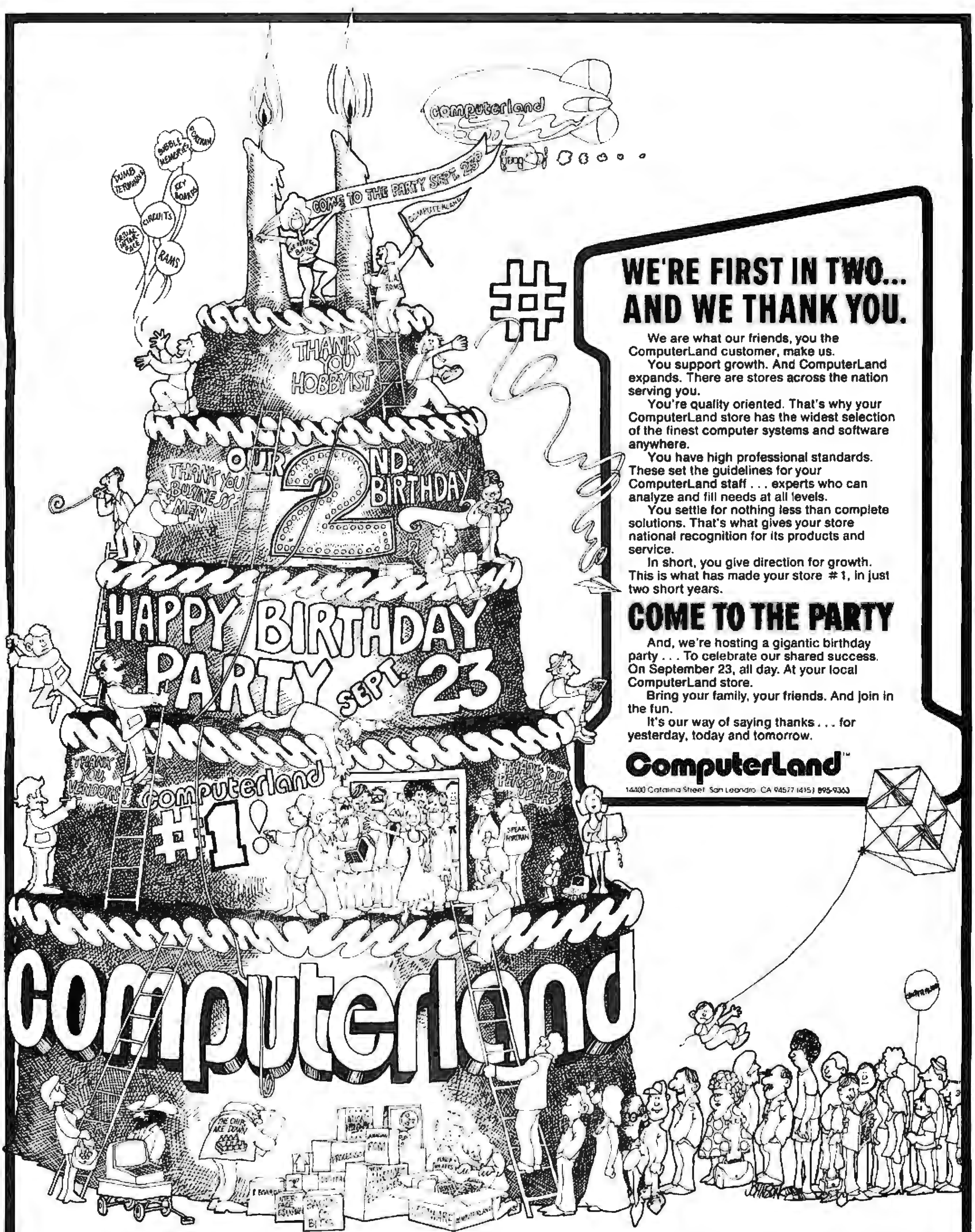
If you intend to use your computer for arithmetic operations it is necessary to have a floating point arithmetic package. Joel Boney's article on implementing a binary floating point package will help you implement **Math in the Real World** if you don't have an appropriate package at your fingertips in a high level language or program library. *page 114*

A displayed object can be defined within a matrix in a program. Once the object has been so defined it is a simple matter to perform **Graphic Manipulations Using Matrices** as described by Joel Hungerford.



page 156

Are you faced with the prospect of owning a just built computer system bare of all niceties such as BASIC or even assembler? Somehow, it is difficult to impress noncomputer people by adding 1 to 1 to get 10. Larry Kheriaty has an interesting language to solve this problem. For Larry's solution read **WADUZITDO: How to Write a Language in 256 Words or Less.** *page 166*



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Editorial

On Entering Our Fourth Year

By Carl Helmers

With this issue, we begin our fourth year of publication of BYTE magazine. The project remains as exciting, if not more so, than when we first put together an issue of the magazine in the summer of 1975. A lot has changed as the people involved with this publication have grown and learned about the process of magazine production. Yet a lot remains similar.

The basic goal of this magazine is not likely to change: to provide readers with a continuing stream of novel ideas and information about computers and related fields. The assumption made about the BYTE reader is that he or she possesses curiosity combined with a willingness to experiment with and learn about topics related to computers and computing. To this end we provide a wealth of tutorials on hardware *and* software aspects of computer science — as well as specific "do it yourself" items on neat projects which can be done by the reader. And all this is tied together with an emphasis on the fun which can be had through the use of computing technology in various ways.

We started out with this idea about the goals of the magazine, and no real knowledge about how far we could take it. After all, the skeptics (on occasion including myself) would ask, can there be that many people interested enough in computers to buy your magazine? But, reflecting the growth of personal computing manufacturing, we went from a 96 page black and white first issue to a 208 page typical current issue, from essentially 0 circulation as of the decision to start the magazine to a present circulation in excess of 140,000 paid copies per month. Perhaps we even played a small part in promoting that growth by providing our advertising and editorial content as a service to the industry.■

Articles Policy

BYTE Publications Inc is continually seeking quality manuscripts written by individuals who are applying personal computer systems, designing such systems, or who have knowledge which will prove useful to our readers. For a more informal description of procedures and requirements, potential authors should send a self-addressed, stamped envelope to BYTE Authors' Guide, 70 Main St, Peterborough NH 03458.

Articles which are accepted are purchased with a rate of $45 per published page, based on technical quality and suitability for the intended readership. As to articles appearing in BYTE magazine, each month, the authors of the two leading articles in the reader poll (BYTE's Ongoing Monitor Box or "BOMB") are presented with bonus checks of $100 and $50. Unsolicited materials should be accompanied by full name and address, as well as return postage.■

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Well, the games part is true. The rest of the claims should be taken with a grain of salt. All of the personal computers will help you learn about computers and how they work in general and the kinds of things they can do for you. Only a few have the capacity to grow and handle meaningful work in a very real sense. And they don't come for peanuts.

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In sum, all small computers are not created equal and Sol users know it to their everlasting satisfaction.

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Processor

The NCC '78 Personal Computer Show

Chris Morgan, Senior Editor

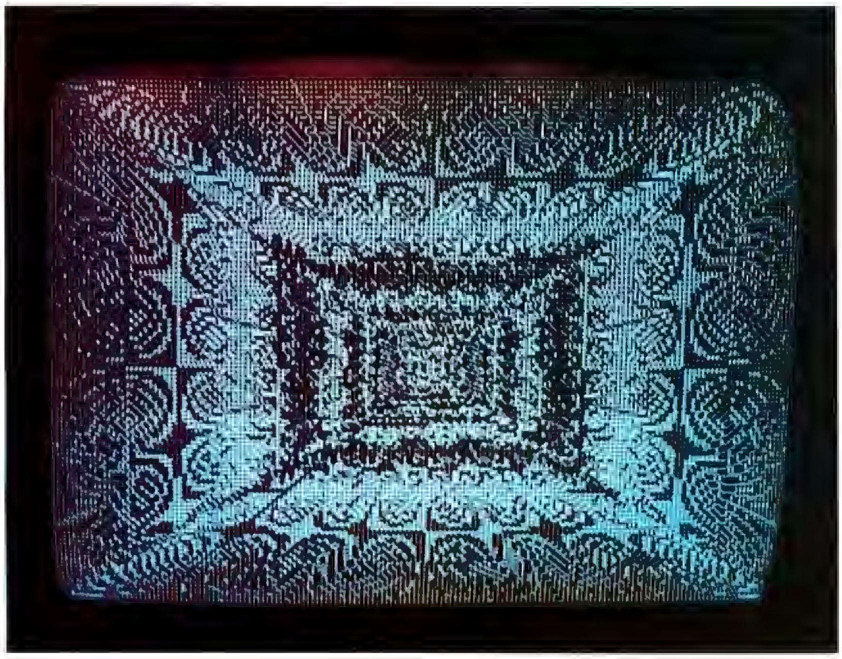

Photo 1: *Complex high resolution graphics created with UCSD Pascal.*

Photo 2: *Color graphics being generated by Exidy's new Sorcerer personal computer.*

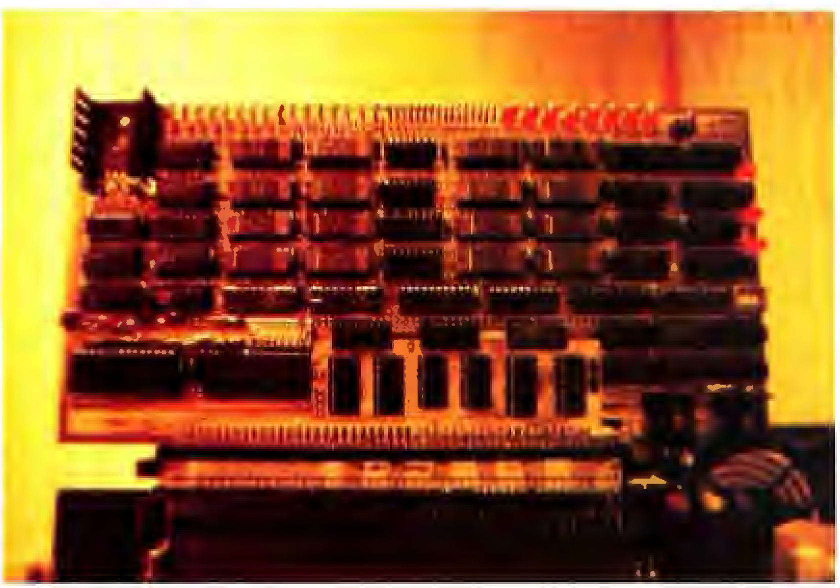

Photo 3: *8 K content addressable memory board from Semionics. The $525 price tag is the lowest we've seen for this type of memory.*

The official attendance was 57,240—that's how many people came to the National Computer Conference in Anaheim CA June 5 thru 8.

Easily the biggest computer show in history, the NCC overflowed the huge Anaheim convention center into a neighboring garage annex converted to handle the extra booths. The personal computing section of the show has grown into a major show of its own in just two years: the crowds there were no less impressive than at the main show.

A diversity of products greeted visitors to the show: everything from digitizers to compilers; Pascal to peripherals; color video systems to surplus parts; and so on. One of the most significant hardware devices on view was an 8 K content addressable memory board for the S-100 bus from Semionics in Berkeley CA. In a normal memory, the address of data is input, and the memory reads from (or writes to) its

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□ **12" CRT, 24x80 Field, Memory-Mapped, EPROM Controlled Font.** Character and line insert/delete allows fast program correction and text editing. Inverse video and programmable field allows highlighting or enlarging graphic information display. Titled fields protect information blocks from being written over accidentally. EPROM controlled font (up to 256 different characters) allows foreign language and special purpose character forms. Video board includes 4K memory-mapped refresh RAM.

□ **Alphanumeric Intelligent Keyboard.** 62-pad main keyboard. Programmable 12-pad control keyboard. Standard typewriter and calculator keyboard layouts. N-key rollover reduces operator error during high-speed data entry.

□ **Commercial BASIC, FORTRAN IV, IMDOS Software.** Built-in ROM monitor allows extensive debugging and diagnostics. BASIC, interactive or compiler version. FORTRAN IV, Level 2 Ansi compiler. IMDOS - IMSAI's multi-disk operating system.

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*Base price VDP-80/1000 $6,995, with 32K RAM memory and dual double density floppy disk drive. U.S. Domestic Price Only.
Features and prices subject to change without notice.

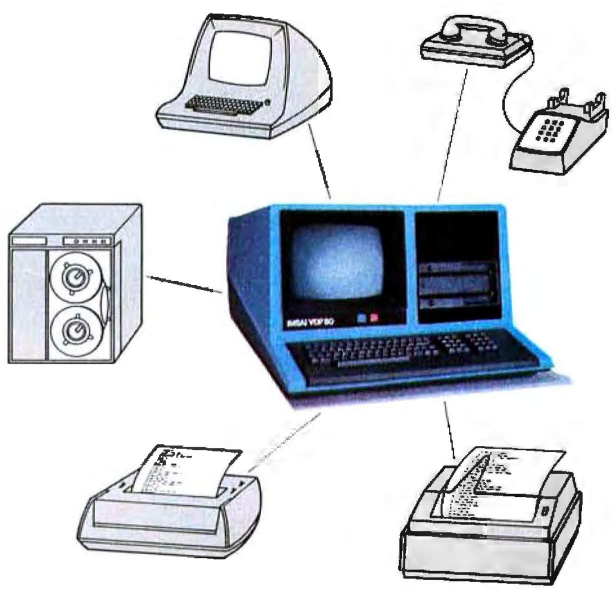

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Photo 4: A throng of people attends the Micro Mouse Maze heat being run by James Hamblen's large economy size "mouse," shown, which traversed the maze in 4:32:28 minutes – the second best time for the show.

Photo 5: Compucolor Model 3 with optional keyboard displaying some unseasonal color graphics. The unit is undoubtedly one of the most cost effective full color graphics systems on the consumer market. Only 117 more shopping days left.

Photo 6: Color expansion board for the RCA Cosmac VIP computer. The board costs $89 and generates eight colors as well as musical tones.

Photo 7: Homebrew 3 voice computer controlled music synthesizer built by John Pratt and Don Shertz of Monterey CA.

contents at that address. In a content addressable memory, the data being sought is presented to the memory, and the memory returns the address of that data (or a suitable code if the data cannot be found.)

The UCSD Pascal Project people were on hand with some impressive graphics displays generated using the Pascal language, and John Pratt and Don Shertz of Monterey CA displayed their homebrew computer music synthesizer which sounded very good.

Mary Ann Duganne and Hal Glicksman displayed a program designed to help Mary's 7 year old son John who has cerebral palsy. Two widely spaced keys on the keyboard are activated by John's fists to move a cursor on a screen and spell out words. For more information, write Hal Glicksman, 76 Market St, Venice CA 90291.

The first entries competed in the amazing Micro Mouse Maze contest, cosponsored by *IEEE Computer* and *Spectrum* magazines. The object was to design a self-powered electronic "mouse" that could solve a maze in the fastest possible time. The sponsors of the contest were amazed (pun intended) at the response to the contest call: over 6000 people wrote for contest kits. Maze trials will be conducted at various computer shows over the next two years before a winner is declared.

These are just some of the highlights of a tremendous show. Next year the NCC will be in New York City. If attendance figures continue to climb at this rate, they'll have to hold the show in Madison Square Garden.■

Why Apple II is the world's best selling personal computer.

Which personal computer will be most enjoyable and rewarding for you? Since we delivered our first Apple® II in April, 1977, more people have chosen our computer than all other personal computers combined. Here are the reasons Apple has become such an overwhelming favorite.

Apple is a fully tested and assembled mainframe computer. You won't need to spend weeks and months in assembly. Just take an Apple home, plug it in, hook up your color TV* and any cassette tape deck—and the fun begins.

To ensure that the fun never stops, and to keep Apple working hard, we've spent the last year expanding the Apple system. There are new peripherals, new software, and the Apple II Basic Programming Manual. And wait till you see the Apple magazine to keep owners on top of what's new.

Apple is so powerful and easy to use that you'll find dozens of applications. There are Apples in major universities, helping teach computer skills. There are Apples in the office, where they're being programmed to control inventories, chart stocks and balance the books. And there are Apples at home, where they can help manage the family budget, control your home's environment, teach arithmetic and foreign languages and, of course, enable you to create hundreds of sound and action video games.

When you buy an Apple II you're investing in the leading edge of technology. Apple was the first computer to come with BASIC in ROM, for example. And the first computer with up to 48K bytes RAM on one board, using advanced, high density 16K devices. We're working to keep Apple the most up-to-date personal computer money can buy. Apple II delivers the features you need to enjoy the real satisfaction a personal computer can bring, today and in the future.

15 colors & hi-resolution graphics, too.

Don't settle for a black and white display! Connect your Apple to a color TV and BASIC gives you instant command of three display modes: Text, 40h x 48v Color-graphics in 15 colors, and a 280h x 192v High Resolution array that lets you plot graphs and compose 3-D images. Apple gives you the added capability of combining text and graphics, too.

Back to basics, and assembly language too.

Apple speaks three languages: fast integer BASIC, floating point BASIC for scientific and financial applications, and 6502 assembly language. That's maximum programming flexibility. And, to preserve user's space, both integer BASIC and monitor are permanently stored in 8K bytes of ROM, so you have an easy-to-use, universal language instantly available. BASIC gives you graphic commands: COLOR=, VLIN, HLIN, PLOT and SCRN. And direct memory access, with PEEK, POKE and CALL commands.

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There's a growing selection of preprogrammed software from the Apple Software Bank—Basic Finance, Checkbook, High Resolution Graphics and more. Now there's a User Section in our bank, to make it easy for you to obtain programs developed

by other Apple owners. Our Software Bank is your link to Apple owners all over the world.

Alive with the sound of music.

Apple's exclusive built-in speaker delivers the added dimension of sound to your programs. Sound to compose electronic music. Sound to liven up games and educational programs. Sound, so that any program can "talk" back to you. That's an example of Apple's "people compatible" design. Another is its light, durable injection-molded case, so you can take Apple with you. And the professional quality, typewriter-style keyboard has n-key rollover, for fast, error-free operator interaction.

Apple is the proven computer.

Apple is a state-of-the-art single board computer, with advanced LSI design to keep component count to a minimum. That makes it more reliable. If glitches do occur, the fully socketed board and built-in diagnostics simplify troubleshooting. In fact, on our assembly line, we use Apples to test new Apples.

*Apple II plugs into any standard TV using an inexpensive modulator (not included).

**In California, call 408/996-1010.

Apple peripherals are smart peripherals.

Watch the far right column of this ad each month for the latest in our growing family of peripherals. We call them "intelligent interfaces." They're smart peripherals, so you can plug them in and run them from BASIC without having to develop custom software. No other personal computer comes close to Apple's expandability. In addition to the built-in video interface, cassette I/O, and four A/D inputs with two continuously variable game paddles, Apple has eight peripheral slots, three TTL inputs and four TTL outputs. Plus a powerful, state-of-the-art switching power supply that can drive all your Apple peripherals.

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Apple is in stock and ready for delivery at a store near you. Call us for the dealer nearest you. Or, for more details and a copy of our "Consumer's Guide to Personal Computers," call 800/538-9696** or write Apple Computer, Inc., 10260 Bandley Drive, Cupertino, CA 95014.

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New from Apple.

Introducing Disk II™: instant access to your files.

Our newest peripheral is Disk II, a high-density 5¼" floppy disk drive for fast, lowcost data retrieval. It's perfect for storing large bodies of data such as household finances, address files and inventories; you can find any record in just half a second. No more searching through stacks of cassettes; with a few keystrokes, your system will load, store and run any file by name.

Disk II consists of an intelligent interface card, a powerful Disk Operating System (DOS), and one or two mini floppy drives. Your Apple will handle up to seven interface cards and fourteen drives, for control of nearly 1.6 megabytes of data, with no expansion chassis. The combination of ROM-based bootstrap loader and an operating system in RAM provides complete disk handling capability, including these special features:
• Soft sectored • Random or sequential file access • Program chaining capability • Universal DOS command processor works with existing languages and monitor • Full disk capability in systems with as little as 16K RAM • Storage capacity: 113 kilobytes/diskette.

See Disk II now at your Apple dealer. Sold complete with controller and DOS at $495.[1]

Peripherals in stock

Hobby Board (A2B0001X), Parallel Printer Interface (A2B0002X), Communication Interface (A2B0003X), Disk II (A2M0004X).

Coming soon

High speed Serial Interface, Printer II, Printer IIA, Monitor II, Modem IIA.

[1] Price subject to change without notice.

Circle 15 on inquiry card.

Apple's smart peripherals make expansion easy. Just plug 'em in and they're ready to run. I've already added two disks, a printer and the communications card.

Programming is a snap! I'm halfway through Apple's BASIC manual and already I've programmed my own space wars game.

Those math programs I wrote last week–I just rewrote them using Apple's mini-assembler and got them to run a hundred times faster.

A Solid State Keyboard as Modern as Your Computer

Solid state electronics has moved the computer quickly from the business world into personal uses. Meanwhile, computer keyboards have hardly moved at all.

Now TASA introduces a keyboard as modern as your computer. Don't confuse it with ordinary flex switches. It is fully solid state and self-contained, ready to plug in and use. Since it has no mechanical moving parts, it responds quickly to your touch. And it provides full ASCII coding in TASA's exclusive color-keyed layout that makes it easier to say what you want to say to your computer.

This is the TASA Micro Proximity Keyboard, and it sells for only $49.95. Despite the price, CMOS/LSI integrated circuits make it totally reliable inside. With the sensors behind a shield of polycarbonate—the most rugged plastic ever developed—it is also durable and reliable outside.

The TASA Keyboard contains all the features you would expect in a professional keyboard—shift, shift lock, control functions, and a normal typewriter format.

If you're tired of costly mechanical keyboards and kits you have to assemble, bring your computer up to date the easy way. Plug in a TASA Keyboard. It will never come between you and your computer.

---

the tasa

Micro Proximity Keyboard

$49.95

Letters

WANTED: A RANDOM NUMBER CIRCUIT

Writing a really good pseudorandom number generator is not an easy thing to do; Knuth devoted half a volume to the process. Also, if you base a computer game on a pseudorandom number generator, you have the awkward problem of supplying a seed for each game. For these reasons, I would like a way of getting truly random numbers into a microprocessor. One way to do this is to have the computer increment a counter while waiting for the user to enter something. If the computer is fast enough, the low order bits of the counter will be random. However, this method is not good for generating large numbers of random numbers, since the user must be consulted for each one. What I really want is a circuit which generates random bits. I've heard that such circuits exist, based on something called "noisy" diodes. Where can I get details?

Scott D Johnson
241 Linden Av
Ithaca NY 14850

Certain processors, like the Zilog Z-80, have methods of apparently forming a random seed number. Since the hidden refresh counter for dynamic memory is always in operation it can be paged whenever a seed for a pseudorandom number generator is required. Within certain constraints it may also be possible to use a series of these numbers as pseudorandom numbers.

WHAT A SMALL COMPUTER CAN DO FOR THE MULTIPLY HANDICAPPED

Being extremely green at this computer game and having no hardware experience (come to think of it no experience whatever) I have only had my Apple about three weeks, but I have a glimpse of the tremendous possibilities now open to me.

Since breaking my neck whilst on National Service in Germany, I've been able to move my head, left, right and slightly backwards and forwards and that's my lot. If anyone tries lying on the floor on his back, using the above movements and tries writing his name with a pen in his mouth (holding a pad above) they will quickly realise there's not a big variety of things someone in my position can do.

Now imagine the same person with the keyboard of a computer in front of him you find the limits go up tenfold.

I know there are machines like "Possom" issued in certain cases by the UK government. It will connect the disabled to TV telephone, it will open doors and curtains, and work a typewriter, about a dozen functions and it costs between £1,400 and £1,600 depending on the number of functions.

The processor I have is an "Apple II" 16 K and because I have to work with a stick in my mouth, the shift and control keys have had to be modified so that they work like a typewriter and use two movements to lock and release.

The Apple has opened up a new world I didn't know existed. It now makes jobs possible, the design and colour graphics and all the games (and don't knock the games, remember your capabilities while lying on the floor) and all this at a touch with a stick, and at costs comparable with "Possom."

All I have to do now is buckle down and do a lot of studying and practicing.

I hope this gives some of your readers a glimpse of what a computer could do for the disabled and severely disabled. Also wonder if they have the same problem I have of doing a bit more, and a bit more to find it's 3 AM, or later, and that you have to force yourself to turn that switch off.

Charles Smith
222 West Ct
The Thistle Foundation
Edinburgh EH16 4EB
SCOTLAND

SOME NOTES FROM JAPAN

You may be interested in details of two recent Tokyo shows. At the Business Machines Show Sharp featured a new programmable calculator, the PC1300. This features magnetic card program storage, alphanumeric printer and display. It has 26 memories (A thru Z), program size is up to "256 steps," two levels of subroutine nesting are allowed, size is 44 by 123 by 220.5 mm (1.7 by 4.8 by 8.7 inches), weight is 680 grams (8 ounces). Numeric format is 10 digit mantissa, 2 digit exponent. Display scrolling (programmed?) was demonstrated at the show. Display and printer are both 16 characters wide.

Continued on page 66

Considering a Microcomputer?

Be Sure to Check Out the Product Offerings of the World's Largest Full Line Microcomputer Company.

All Ohio Scientific machines come with microcomputing's fastest full feature BASIC-in-ROM or on-Disk for instant use.

	Minimum Configuration	Base Price
Challenger I Series		
Economical computer systems that talk in BASIC. Ideal for hobbyists, students, education and the home.		
Superboard II — World's first complete system on a board including keyboard, video display, audio cassette, BASIC-in-ROM and up to 8K RAM	4K RAM	$ 279
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Challenger IP Disk — Complete mini-floppy system expandable to 32K RAM	16K RAM	$1190
Challenger IIP Series		
Ultra high performance BUS oriented microcomputers for personal, educational, research and small business use.		
C2-4P — The professional portable	4K RAM	$ 598
C2-8P — The world's most expandable personal machine for business or research applications	4K RAM	$ 799
C2-4P Disk — The ultimate portable	16K RAM	$1464
C2-8P Single Disk — Ideal for education, advanced personal users, etc.	16K RAM	$1738
C2-8P Dual Disk — Most cost effective small business system	32K RAM	$2597
Challenger II Serial Interface Series		
Same great features as Challenger IIP Series for those who have serial terminals: small business, education, industry.		
C2-0—Great starter for users with a terminal	4K RAM	$ 298
C2-1 — Great timeshare user accessory; cuts costs by running simple BASIC programs locally	4K RAM	$ 498
C2-8S — Highly expandable serial machine, can add disks, etc.	4K RAM	$ 545
Challenger III The Ultimate in Small Computers		
The unique three processor system for demanding business, education, research and industrial development applications.		
C3-S1 — World's most popular 8″ floppy based microcomputer	32K RAM dual floppys	$3590
C3-OEM — Single package high volume user version of C3-S1	32K RAM dual floppys	$3590
C3-A — Rack mounted multi-user business system directly expandabe to C3-B	48K RAM dual floppys	$5090
C3-B — 74 million byte Winchester disk based system. World's most powerful microcomputer	48K RAM dual floppys	$11,090

OHIO SCIENTIFIC also offers you the broadest line of expansion accessories and the largest selection of affordable software!

Compare the closest Ohio Scientific Model to any other unit you are considering. Compare the performance, real expansion ability, software and price, and you will see why we have become the world's largest full line microcomputer company.

I'm interested in OSI Computers. Send me information on:

- ☐ Personal Computers
- ☐ Small Business Computers
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- ☐ I'm enclosing $1.00 for your 64-page small computer buyer's guide.

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Name ______________________

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The C2-8P

An exceptional value in personal computing

If you are interested in an ultra high performance personal computer which can be fully expanded to a mainframe class microcomputer system, consider the C2-8P.

Features:

- Minimally equipped with 8K BASIC-in-ROM, 4K RAM, machine code monitor, video display interface, cassette interface and keyboard with upper and lower case characters. (Video monitor and cassette recorder optional extras.)
- The fastest full feature BASIC in the microcomputer industry.
- Boasts the most sophisticated video display in personal computing with 32 rows by 64 columns of upper case, lower case, graphics and gaming elements for an effective screen resolution of 256 by 512 elements.
- The CPU's direct screen access, coupled with its ultra fast BASIC and high resolution, makes the C2-8P capable of spectacular video animation directly in BASIC.
- Fully assembled and tested: 8 slot mainframe class microcomputer, six open slots for expansion. Supports Ohio Scientific's ultra low cost dynamic RAM boards or ultra high reliability static RAMs.
- The C2-8P can support more in-case expansion than its four nearest competitors combined.
- The C2-8P is the only BASIC-in-ROM computer that can be directly expanded today to a complete business system with line printer and 8" floppy disk drives.
- It is the only personal class computer that can be expanded to support a Hard Disk! (CD-74)

The C2-8P is the fastest in BASIC, has the most sophisticated video display and is the most internally expandable personal computer. Therefore, it should be the highest priced?

Wrong: The C2-8P is priced considerably below several models advertised in this magazine. The C2-8P is just one of several models of personal computers by Ohio Scientific, the company that first offered full feature BASIC-in-ROM personal computers.

For more information, contact your local Ohio Scientific dealer or the factory at (216) 562-3101.

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The OSI 48 Line BUS

OHIO SCIENTIFIC offers the broadest line of BUS compatible microcomputer boards. This line includes several new and exciting products which are not available anywhere else, such as a three processor CPU board, dual port memories and a multiprocessing CPU expander.

OHIO SCIENTIFIC has delivered approximately 100,000 boards based on our 48 line BUS and is now delivering thousands per week in 17 models of computers and dozens of accessories.

OHIO SCIENTIFIC'S BUS design incorporates high band width, high density and mass production technology to achieve a truly remarkable performance to cost ratio.

Here is just a sampling of the many OSI 48 BUS compatible boards available for the systems user, prototyper, OEM user and experimenter.

Product Description	Special Features	Power Supply Voltages Req'd	Board & Doc. Part #	Board & Doc. Price	Assembled Product Part #	Assembled Product Price
CPU						
• Challenger II CPU BASIC-in-ROM 6502 based CPU with serial I/O 4K RAM, machine code monitor	• Can use four 2716 EPROMS instead of BASIC or can be configured for disk	+5/−9	500	39.00	C2-0	298.00
• Challenger III CPU has 6502A, 6800 and Z80 micros, RS-232 serial port, machine code monitor	• 1 megabyte memory manager, software programmable vectors	+5/−9	510	NA	C3-0	490.00
• 560Z multi-processing CPU expander runs PDP-8, Z80 and 8080 code	• Runs concurrently with another OSI CPU	+5/−9	560Z	125.00	NA	NA
RAM						
• 16K static RAM (Ultra low power)	• 215NS access time automatic power down standby mode	+5/+12/−9	520	35.00	CM-3	498.00
• 8K static RAM (low cost)	• Expandable to 16K	+5	—	—	CM-7	198.00
• 16K static RAM (low cost)	• Can be expanded to dual port operation	+5	525	35.00	CM-8	339.00
• 24K static RAM (high density)	• 20 address bits	+5	527	35.00	CM-9	NA
• 4K static RAM (2102 based)	• Can be populated for 4K by 12 bits	+5	420	35.00	CM-2	125.00
• 16K dynamic (ultra low cost)	• Uses 4027 RAMS	+5/+12/−9	530	NA	CM-4	249.00
• 32K dynamic	• 20 address bits	+5/+12/−9	530	NA	CM-5	698.00
• 48K dynamic (high density)	• 20 address bits	+5/+12/−9	530	NA	CM-6	990.00
EPROM Boards						
• 8K 6834 EPROM board	• 16 line parallel port and on board programmer	+5/−9	450	35.00	NA	NA
• 4K 1702A EPROM board	• 16 line parallel port	+5/−9	455	35.00	NA	NA
I/O Boards						
• Audio Cassette interface Kansas City standard 300 baud	• Expandable to CA-7C	+5/−9	430	35.00	CA-6C	99.00
• RS-232 port board	• Expandable to CA-7S	+5/−9	430	35.00	CA-6S	99.00
• Combination audio cassette two 8 bit DACs, one fast A/D and 8 channel input mux	• Also Features 8 parallel I/O lines	+5/−9	430	35.00	CA-7C	399.00
• Combination RS-232 two 8 bit DACs, one fast A/D and 8 channel input mux	• Also features 8 parallel I/O lines	+5/−9	430	35.00	CA-7S	399.00
• 32 by 32 character video display interface	• Keyboard input port	+5/−9	440	35.00	NA	NA
• 32 by 64 character video display interface	• Upper/lower case graphics and keyboard port	+5	540	NA	CA-11	249.00
• 16 port serial board RS-232 and/or high speed synchronous	• 75 to 19,200 baud and 250K and 500K bit rates individually strappable	+5/−9	550	35.00	CA-10X	200.00 to 900.00
• Parallel (Centronics) Line Printer Interface	• With cable	+5/−9	470	NA	CA-9	249.00
• 96 Line Remote Parallel Interface	• Interface "Front End" remotable via 16 pin ribbon cable	+5	—	—	CA-12	249.00
• Voice I/O board with Votrax* module	• Fully assembled voice output, experimental voice input	+5/−9	—	—	CA-14	525.00
DISKS						
• Single 8" floppy disk, 250 Kbytes storage	• Complete with operating system software and disk BASIC	+5/−9	470	NA	CD-1P	790.00
• Dual 8" floppy disk, 500 Kbytes storage	• Complete with operating system software and disk BASIC	+5/−9	470	NA	CD-2P	1390.00
• 74 Million byte Winchester disk and interface	• Complete with OS-65U operating system	+5/−9	—	—	CD-74	6000.00
OTHER						
• 8 slot backplane board with connectors	• Can be daisy-chained to n-slots	—	580	39.00	NA	NA
• Prototyping board	• Handles over 40 16 pin IC's	—	495	29.00	—	—
• Card Extender	• With connectors	—	498	29.00	—	—

For more information, contact your local OHIO SCIENTIFIC Dealer or the factory at (216) 562-3101

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The C3-B
by Ohio Scientific

The world's most powerful microcomputer system is far more affordable than you may think.*

STANDARD FEATURES:

- 74 million byte Winchester technology disk drive yields mainframe class file access speeds and capacity.
- High level data file software makes high performance file structures like multikey ISAM easy to use.
- Triple processor CPU with 6502A, 6800 and Z-80 gives the programmer the best of all worlds in performance and versatility.
- The included 6502A based extended disk BASIC by Microsoft out-benchmarks every micro available, including 4 MHz Z-80 and LSI-11 with extended arithmetic.
- 48K of high reliability static RAM is standard.
- High density 8" floppys provide program and data mobility from machine to machine.
- Completely integrated mechanical system with UL-recognized power supplies; continuous duty cycle cooling; modular construction and rack slide mounted subassemblies.
- Based on a 16 slot Bus-oriented architecture with only 7 slots used in the base machine.
- Directly expandable to 300 megabytes of disk, 768K of RAM in 16 partitions, 16 communication ports, plus console and three printers.
- C3-B's have been in production since February, 1978, and are available now on very reasonable delivery schedules.

The C3-B was designed by Ohio Scientific as the state of art in small business computing. The system places its power where it's needed in the small business environment; in the data files. The C3-B's advanced Winchester technology disk, coupled with its smart controller and dedicated high speed memory channel, gives the C3-B data file performance comparable with today's most powerful maxi-computers.

Yet, the C3-B costs only slightly more than many floppy only computers but offers at least a thousand times performance improvement over such machines (50 times storage capacity multiplied by 20 times access speed improvement).

But what if your business client cannot justify starting with a C3-B? Then start with Ohio Scientific's inexpensive C3-S1 floppy disk based system running OS-65U. When he is ready, add the CD-74 big disk and directly transfer programs and files from floppy to big disk with *NO* modifications.

That's upward expandability!

*Rack as shown above complete with 74 megabyte disk, dual floppys, 48K of static RAM, OS-65U operating system and one CRT terminal under $13,000.

Multiple terminal systems with printers and applications software are priced in the mid-20's.

Circle 290 on inquiry card.

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Jeffrey L Posdamer
Dept of Computer Science
SUNY at Buffalo
Ridge Lea Rd
Amherst NY 14226

The Mathematics of Computer Graphics

Computer graphics by Joel Hungerford

Graphic assistance by Vivian Day

The personal computing literature is filled with material describing the hardware of microprocessors using video graphics. A great deal has also been written about specific graphic applications including video games, computer art, etc. Computer graphics is, however, a powerful tool that requires for its use an understanding of a set of underlying computing and mathematical principles. The purpose of this article is to present some of these principles in the context of personal computing.

The screen of a video display is essentially a space with two dimensions. While a number of schemes exist for dealing with two-dimensional spaces, the most common is Cartesian coordinates. Each point in the space is represented by a pair of numbers corresponding to its distance from two axes at right angles to each other. On a video display this pair of numbers corresponds to the scan line number and picture element within the scan line. The notation [x y] will be used here to denote the element number and scan line number. Due to the nature of displays, the values for x and y are integers of limited range. Each pair of values corresponds to a unique point in the *display space*.

For many problems in which computer graphics is useful, a second space is used. This is the *problem space* (see figure 1). This corresponds to the description of the problem geometry as opposed to the screen. The representation [u v] will be used here for problem spaces. For Space War its dimensions may be measured in parsecs, for a tennis simulation it may be measured in inches, etc. Problem spaces may be integer or real,

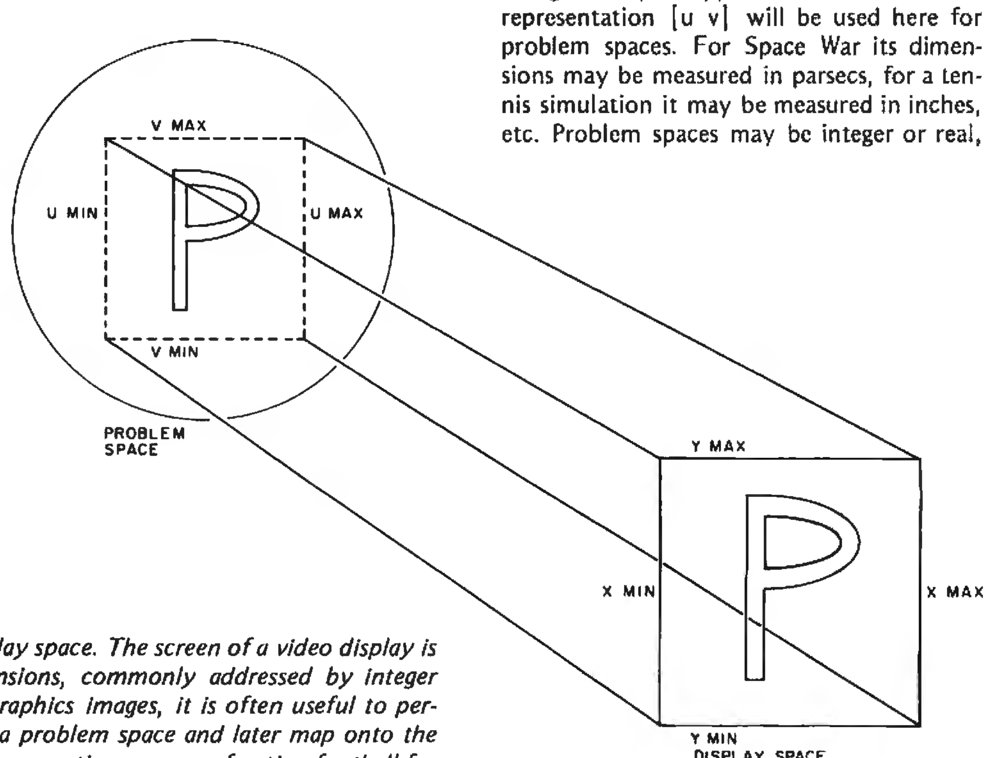

Figure 1: Problem space versus display space. The screen of a video display is essentially a space with two dimensions, commonly addressed by integer Cartesian coordinates. In creating graphics images, it is often useful to perform calculations in what is called a problem space and later map onto the display space. For instance, if you are creating a game of action football for your graphics display, it may be more useful to perform the calculations with u and v coordinates measured in yards (your problem space) and later convert to the display space with its integer coordinates.

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bounded or unbounded and are defined by the nature of the problem, not the use of computer graphics as a tool.

Naturally, there must be a way to convert from one space to the other when both are used. If

xsmin = left screen value
xsmax = right screen value
ysmin = bottom screen value
ysmax = top screen value

and

upmin = minimum problem space u coordinate value
upmax = maximum problem space u coordinate value
vpmin = minimum problem space v coordinate value
vpmax = maximum problem space v coordinate value

then the point [u v] in problem space maps into a point [x y] in screen space as follows:

$$x = \left(\frac{u\text{-}upmin}{upmax\text{-}upmin}\right) \times (xsmax\text{-}xsmin) + (xsmin)$$

$$y = \left(\frac{v\text{-}vpmin}{vpmax\text{-}vpmin}\right) \times (ysmax\text{-}ysmin) + (ysmin)$$

In most cases, operating on individual points is only a beginning. Generally, techniques are needed to deal with line segments that connect points to define figures and regions.

If two points $P_0 = [x_0\ y_0]$ and $P_1 = [x_1\ y_1]$ are to be connected by a line segment, it is often necessary to compute every point on the connecting line (see figure 2). A traditional representation of the straight line is of the form:

$$y = mx + b$$

where

$$m = \frac{y_1 - y_0}{x_1 - x_0} \text{ and } b = y_0 - (x_0 \times m).$$

To compute the series of points that would represent the line segment connecting P_0 and P_1, a program would start with the point at (x_0, y_0) add $m \times \Delta x$ to y_0 and Δx to x_0 enough times to reach x_1 and y_1 (Δx means a small increment of x). It is important to realize that m, b and the intermediate values of x and y may take on noninteger values. For each intermediate point, the rounded values of x and y are used to designate a picture element to be displayed as part of the line's representation.

An alternative to this scheme is the "parametric" line representation. Here, the mathematical representation of the infinite line that passes through P_0 and P_1 is not used.

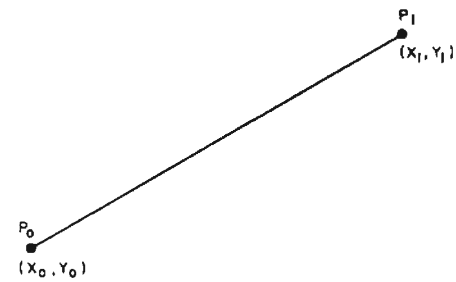

Figure 2: The straight line, a basic element in many displays. If two points are to be connected by a line segment, in a raster graphic display it is necessary to calculate every point on the connecting line. In the case of a vector display, only the endpoints of the vector need be computed.

Instead, we represent only the points between P_0 and P_1:

$$x = (1-t)x_0 + tx_1 = x_0 + t(x_1 - x_0)$$

$$y = (1-t)y_0 + ty_1 = y_0 + t(y_1 - y_0)$$

where t varies from 0 to 1

$$(x,y) = (x_0, y_0) \text{ at } t = 0$$

$$(x,y) = (x_1, y_1) \text{ at } t = 1$$

A line similar to the above line is generated, but with simpler, more direct computations.

For more advanced systems, a number of hardware schemes for line generation exist. Since hardware is not the topic of discussion in this article, refer to reference 1 for a discussion of binary rate multipliers, digital differential analyzers and multiplying digital to analog converters.

Another basic graphics element is the polygon. The polygon is a plane figure consisting of all points inside and on the boundary of a simply connected series of straight lines. For our purposes it is more convenient to represent a polygon by a list of its vertices than by a list of the entire set of displayed points. Polygons raise the issue of the differences between video or *raster* displays and line drawing *vector* or *calligraphic* displays.

The line drawing display has been a standard graphics device. It contains hardware to draw lines between points in the screen space. The image is drawn by tracing over each line in the image in the order the lines were specified. Thus, only points on displayed lines are scanned.

The raster display uses a fixed scanning pattern that covers the entire screen. At

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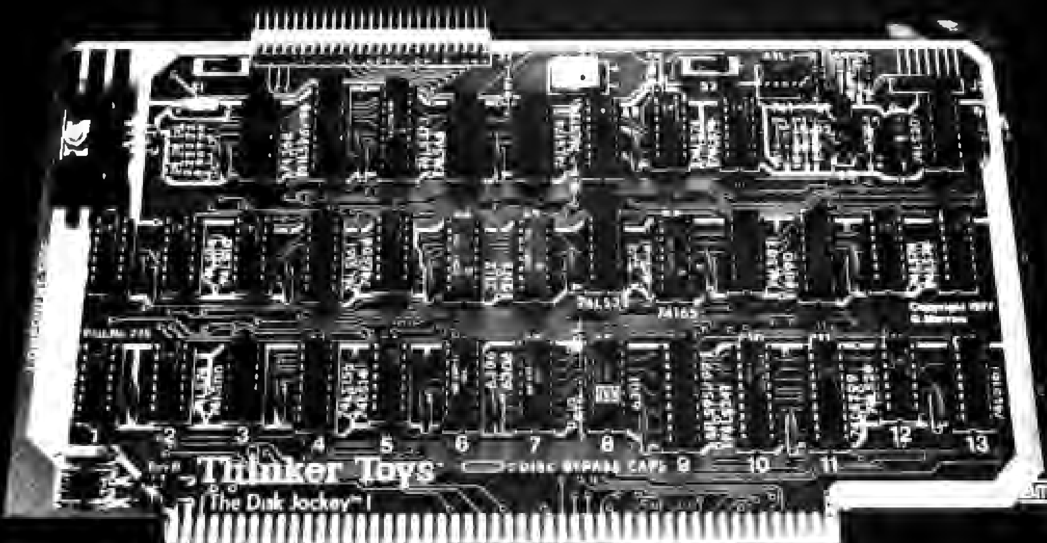

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screen positions which are parts of the displayed image, the scanning beam is intensified, causing images to appear on the screen. On a line drawing display, polygons can be represented by their boundaries; on a raster display they can be "colored in."

Displaying Polygons

A polygon is represented by an ordered set of points: $(x_0,y_0), (x_1,y_1), \ldots (x_n,y_n)$. An alternative notation for this collection is a matrix:

$$M = \begin{bmatrix} x_o & y_o \\ x_1 & y_1 \\ \cdot & \\ \cdot & \\ \cdot & \\ y_1 & y_n \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \\ \cdot & \\ \cdot & \\ \cdot & \\ m_{n1} & m_{n2} \end{bmatrix}$$

Each element of the matrix is a number, specified by its row index and column index. In memory, arrays are typically stored in consecutive locations in either row or column order. It is necessary to calculate an element address from the row and column indices of a particular element in order to access it.

Given the vertices, how can the displayed interior points be calculated? Let us assume (as is usually the case) that the display scans from top to bottom and from left to right. For each line segment in the polygon, determine the vertex with the maximum y value and sort the edges in descending order by the maximum y value. Every vertex in the polygon is now represented in two places: as the beginning and end of two lines. Beginning with the topmost vertex, a line generation algorithm is used on any line that crosses the current y value. Because of the sort that was performed, line segments which begin lower on the screen may be ignored. Since both ends of the line segment are present, a line is dropped from the computation when its "lower" end is passed. For every line passing through the current y value, the x value has been calculated. The points generated are now sorted by x value.

Starting with the minimum x value, fill in picture elements on the scan line until the next value is encountered; leave empty picture elements until another picture element (if any) is encountered. As the program scans from left to right, the x values occupying odd numbered positions (1st, 3rd. . .) in the x-sorted list cause picture element insertion to begin; the even position elements cause picture element insertion to be superseded. Figure 3 shows how this process can be generalized and applied to an arbitrary plane figure in outline form, ie: a letter "P." This procedure is repeated as the y value is stepped down the screen space for each scan line until the "lowest" vertex is encountered, ending the figure.

Transformations

Now that the basic graphic elements have been defined in terms of points and a set of algorithms which generate lines and arbitrary figures from the points, it is necessary to examine the operations needed to manipulate points to perform useful tasks. There are three basic *transformations* in two dimensions: translation, rotation, and scaling or magnification.

Translation is the movement of a point or points by an amount in x and an amount in y. The motion is such that neither the shape, size nor orientation is changed. It may be expressed as:

$$x' = x + changex$$
$$y' = y + changey$$

where the *changex* need not equal *changey*.

If all of the points associated with a line or figure are translated by an equal amount, the graphic element is translated without change in size, shape or orientation. Figure 4

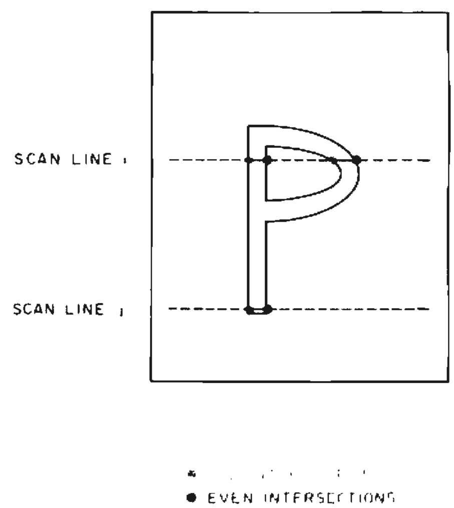

Figure 3: Creating a letter P with a raster scanning video display. During each scan line the program creates blanks until it comes to the first line. After this point it creates solid picture elements until it encounters the next line, whereupon it switches back to blanks. The algorithm states that solid picture elements should follow odd numbered line intersections and that blanks should follow even numbered line intersections.

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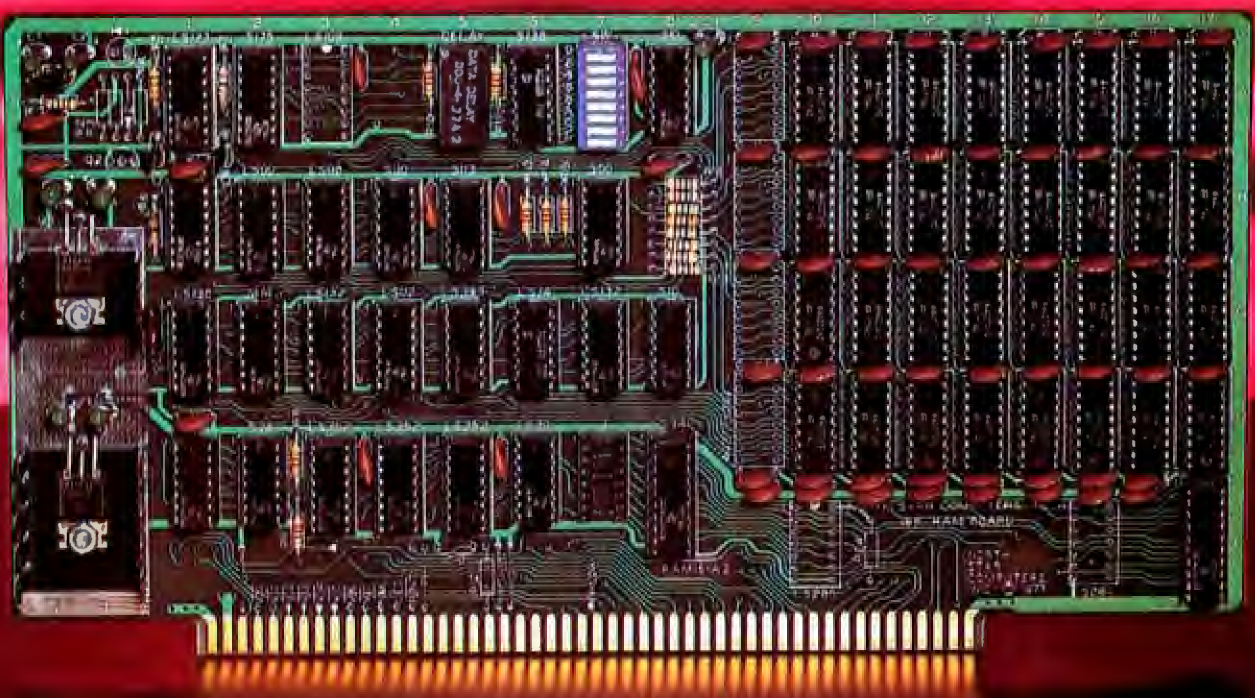

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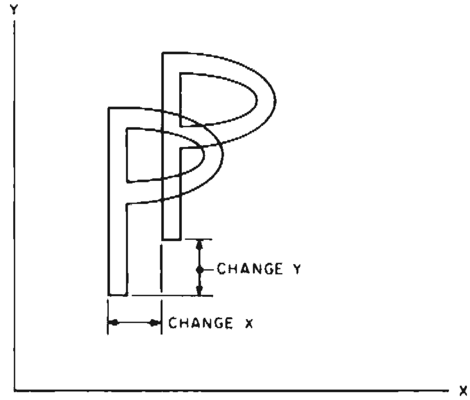

Figure 4: Translation in the xy plane.

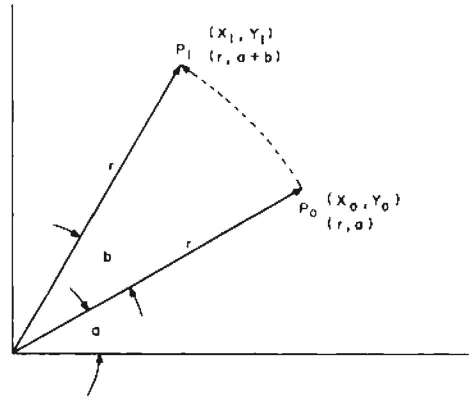

Figure 6: Rotation of vector about the origin.

shows the effect of a translation applied to our arbitrary figure, the letter "P." Rotation is a somewhat different problem. It involves a computation which maintains shape but changes orientation. A rotation will generally leave only one point in the two-dimensional space with its position unchanged: the center of rotation. For the sake of simplicity, the rotation computation is developed with the point (0,0) as the center of rotation. The polar coordinate representation is used (see figure 5). Later it will be shown how to rotate about any arbitrary point. The point to be rotated, P_0, is at position (x_0,y_0) (see figure 6). This is at a distance r from (0,0) and the line from the origin to P makes an angle of a with the x axis. From trigonometry we know that:

$$x_0 = r\cos(a)$$
$$y_0 = r\sin(a)$$

If P_0 is rotated about (0,0) by an angle of b to become P_1 then

$$x_1 = r\cos(a+b)$$
$$y_1 = r\sin(a+b)$$

but from trigonometry we may substitute

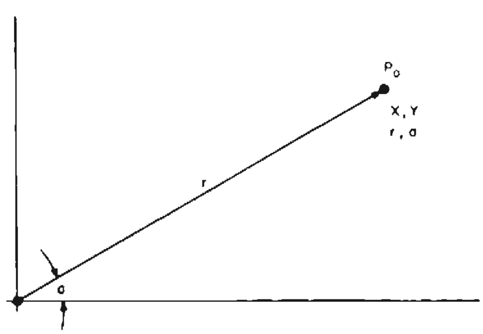

Figure 5: Polar coordinate representation of a point in the xy plane.

for the sum-of-angles form:

$$x_1 = r\cos(a)\cos(b) - r\sin(a)\sin(b)$$
$$y_1 = r\cos(a)\sin(b) + r\sin(a)\cos(b)$$

but from above we get

$$x_1 = x_0\cos(b) - y_0\sin(b)$$
$$y_1 = x_0\sin(b) + y_0\cos(b)$$

The last of the basic transformations is scaling or magnification. This involves a change in size without change in orientation. Depending on the definition of shape, it is either unchanged or changed "without distortion." As in rotation, only a single point in the plane is unchanged by a particular scaling transformation and once again, for convenience, the origin [0 0] is left unchanged. The equations:

$$x_1 = sx_0$$
$$y_1 = sy_0$$

will scale x and y by a factor s. The factor may be greater than or less than 1. If a negative value is used for s, then *reflection* about the origin is performed. If the scale factors for x and y are different, then "stretching" is accomplished. Figure 7 illustrates several scaling transformations applied to the "P" figure seen in several earlier illustrations.

Vectors and Matrices

The use of matrix notation allows simplified extensions and combinations of the basic transformations. A matrix is a rectangular array of numbers identified by row and column numbers. Every row in a particular matrix has the same number of entries, as does every column. The notation A(I,J) refers to the element of matrix A in the Ith row and Jth column. A matrix has a size associated with it, [r c], which defines the

number of rows and number of columns. For matrices A, B and C each having the same number of rows and columns, the following rules are true:

A = B if A(I,J) = B(I,J) for all elements
A = B+C when A(I,J) = B(I,J) + C(I,J) for all elements
A = B−C when A(I,J) = B(I,J) − C(I,J) for all elements

While addition and subtraction of matrices follow in fairly simple fashion from *scalar* (nonmatrix) arithmetic rules, multiplication and operations similar to division are not at all similar. (A scalar is a quantity that is completely specified by a single number, compared with multiple number data constructs, which are vectors and matrices.)

A matrix with only one row is called a *row vector*. Similarly, a matrix with only one column is called a *column vector*. The subject of matrix multiplication is first examined with these simplified forms. While

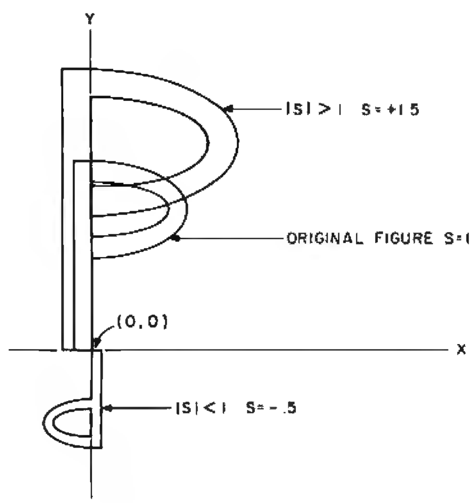

Figure 7: Scaling an arbitrary figure in the xy plane.

there are two forms of vector multiplication, only the *dot product* (also called the *vector-inner-product*) is presented here. Again, using a matrix A (the row vector), B (the column vector) and C (their product) the vector product computation will be described. A vector product can exist only if the number of elements in A and the number of elements in B are equal. If each of these has N elements then

C = A(1,1) X B(1,1) + A(2,1) X B(1,2) . . . + A(N,1) X B(N,1).

This is called the *dot product* of the two vectors. It is the sum of the pairwise products of their elements. C, the dot product of the two vectors, is a single number (a scalar) not a vector or matrix. For example:

let

A = [1 2 3 4] row vector

$$B = \begin{bmatrix} 3 \\ 5 \\ 7 \\ 11 \end{bmatrix}$$ column vector

then

A·B = C = 1X3 + 2X5 + 3X7 + 4X11 = 78

Now suppose that A and B are not restricted to one column and one row, respectively. Instead, we let A have size $[r_A\ c_A]$ and B have size $[r_B\ c_B]$. The matrix product can only be computed if $c_A = r_B$: that is, the number of columns in A is equal to the number of rows of B. Two matrices for which this is true are called *conformable*. C will now have size $[r_A\ c_B]$, inheriting its size from both A and B. Each element in C (which is no longer a scalar) results from the dot product of a row in A with a column in B:

C(I,J) = A(I,1) X B(1,J) + A(I,2) X B(2,J). . . + A(I,N) X B(N,J)

where

$N = c_A = r_B$

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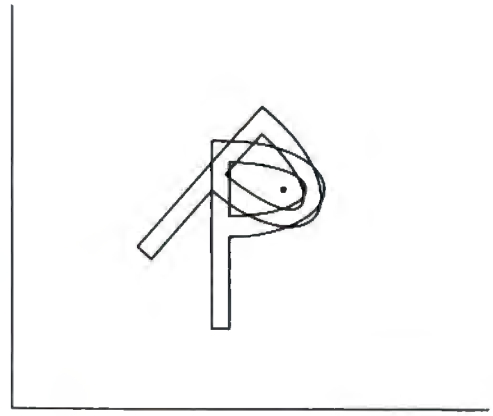


Figure 8: Rotation of an arbitrary figure about an arbitrary point.

and where I takes on all integer values from 1 to r_A and J takes on all integer values from 1 to c_B. For example:

let

$$A = \begin{bmatrix} 1 & 2 \\ 5 & 7 \\ 3 & -1 \end{bmatrix}$$

$$r_A = 3$$
$$c_A = 2$$

$$B = \begin{bmatrix} 3 & 1 & 4 & 1 \\ 5 & 9 & 2 & 6 \end{bmatrix}$$

$$r_B = 2$$
$$c_B = 4$$

The number of columns in matrix A is equal to the number of rows in matrix B. In equation form, this means that:

$$c_A = r_B = 2$$
$$[r_c \ c_c] = [3\ 4]$$

Therefore, we can calculate the matrix result C:

$$C = \begin{bmatrix} 1\times3+ & 1\times1+ & 1\times4+ & 1\times1+ \\ 2\times5 & 2\times9 & 2\times2 & 2\times6 \\ 5\times3+ & 5\times1+ & 5\times4+ & 5\times1+ \\ 7\times5 & 7\times9 & 7\times2 & 7\times6 \\ 3\times3- & 3\times1- & 3\times4- & 3\times1- \\ 1\times5 & 1\times9 & 1\times2 & 1\times6 \end{bmatrix}$$

$$C = \begin{bmatrix} 13 & 19 & 8 & 13 \\ 50 & 68 & 34 & 47 \\ 4 & -6 & 10 & -3 \end{bmatrix}$$

For any matrix M there is a special matrix which, when multiplied by M, yields M. This is called the *identity* matrix (I). It is similar in role to the value 1 in scalar multiplication. Naturally, the identity matrix must be conformable with a particular M. I is a square matrix, with zeros everywhere but on the diagonal, where the value 1 is placed. The diagonal is the set of elements where the row index equals the column index. For example, if I and M are both 3 by 3 matrices, then IM = M:

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} M = M$$

Now let's turn back to rotations, and see how these may be applied to a collection of points describing a figure on the display screen.

Two comments are worth noting at this stage. It is often useful and necessary to apply the same transformation to several points. This occurs when applying a transformation to items such as polygons or more complex collections of points. Additionally, it is useful to combine basic transformations to create more complex transformations.

A collection of points may be represented as a matrix:

$$\begin{bmatrix} x_0 & y_0 \\ x_1 & y_1 \\ \cdot & \\ \cdot & \\ \cdot & \\ x_n & y_n \end{bmatrix}$$

Recall the basic operations of scaling, rotation and translation:

Scaling (about the origin)

$$x_1 = s_x x_0$$
$$y_1 = s_y y_0$$

Rotation (about the origin)

$$x_1 = x_0 \cos(b) - y_0 \sin(b)$$
$$y_1 = x_0 \sin(b) + y_0 \cos(b)$$

Translation

$$x_1 = x_0 + \mathit{changex}$$
$$y_1 = y_0 + \mathit{changey}.$$

If these transformations could be represented as appropriate matrices, they could be applied simultaneously to all points in the collection. Scaling may be represented in matrix form as:

$$[x'\ y'] = [x\ y] \begin{bmatrix} s_x & 0 \\ 0 & s_y \end{bmatrix}$$

or, for a collection of points:

$$\begin{bmatrix} x'_0 & y'_0 \\ \cdot & \\ \cdot & \\ \cdot & \\ x'_n & y'_n \end{bmatrix} = \begin{bmatrix} x_0 & y_0 \\ \cdot & \\ \cdot & \\ \cdot & \\ x_n & y_n \end{bmatrix} \begin{bmatrix} s_x & 0 \\ 0 & s_y \end{bmatrix}$$

Rotation through angle b about the origin may be represented as:

$$\begin{bmatrix} x'_0 & y'_0 \\ \cdot & \\ \cdot & \\ \cdot & \\ x'_n & y'_n \end{bmatrix} = \begin{bmatrix} x_0 & y_0 \\ \cdot & \\ \cdot & \\ \cdot & \\ x_n & y_n \end{bmatrix} \begin{bmatrix} \cos(b) & \sin(b) \\ -\sin(b) & \cos(b) \end{bmatrix}$$

Translation presents a somewhat more difficult problem. No 2 by 2 transformation matrix can be devised that will transform a group of points by a uniform displacement. An alternative representation of the translation is:

$$x' = (x)1 + (y)0 + 1 \cdot \mathit{changex}$$
$$y' = (x)0 + (y)1 + 1 \cdot \mathit{changey}$$

If we now represent all points in two-dimensional space with a 3 element vector of the form [x y 1] for the point at [x y], then the translation operation may be represented in matrix form as

$$\begin{bmatrix} x'_0 & y'_0 & 1 \\ & \cdot & \\ & \cdot & \\ & \cdot & \\ x'_n & y'_n & 1 \end{bmatrix} = \begin{bmatrix} x_0 & y_0 & 1 \\ & \cdot & \\ & \cdot & \\ & \cdot & \\ x_n & y_n & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ \mathit{changex} & \mathit{changey} & 1 \end{bmatrix}$$

Note that a third (unnecessary) column is added to the translation matrix to make the results have the same dimensions as the input points.

The scaling matrix is now rewritten as:

$$\begin{bmatrix} s_x & 0 & 0 \\ 0 & s_y & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The rotation matrix is now:

$$\begin{bmatrix} \cos(b) & \sin(b) & 0 \\ -\sin(b) & \cos(b) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The use of an n+1 element vector to represent a point in n-dimensional space is known as the use of *homogeneous coordinates*.

Now that a uniform representation, the 3 by 3 matrix, is available for transformations, two questions arise: (1) How can more complex transformations be implemented? (2) What effects are obtained from matrices which do not fit into the special structures generated for the basic transformations?

Most complex geometric operations may

Transformed Coordinate Matrix (n by 3)		Coordinate Matrix (n by 3)	Translation to Origin by $(-X_r, -Y_r)$ (3 by 3)	Rotation by Angle b (3 by 3)	Translation by (X_r, Y_r) (3 by 3)

$$\begin{bmatrix} X_o' & Y_o' & 1 \\ & \vdots & \\ X_n' & Y_n' & 1 \end{bmatrix} = \begin{bmatrix} X_o & Y_o & 1 \\ & \vdots & \\ X_n & Y_n & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ -X_r & -Y_r & 1 \end{bmatrix} \begin{bmatrix} \cos(b) & \sin(b) & 0 \\ -\sin(b) & \cos(b) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ X_r & Y_r & 1 \end{bmatrix}$$

Example 1.

be implemented as a sequence of basic operations. A few examples are examined next.

Rotation About an Arbitrary Point $[x_r\ y_r\ 1]$

Since we know how to rotate about the origin, the point R and the object are first moved to the origin. The object is then rotated and the system moved back so that R is at its original location. A matrix representation of this procedure is shown in example 1. The point R will be unchanged by this sequence of transformations. Transformations are *not* generally commutative; ie: the order of application of the transformations *is fixed* to achieve a particular combined result.

A similar statement is true for matrix multiplication:

$$AB \neq BA \quad \text{in general.}$$

But, matrix multiplication is *associative*. That is, if the order of the matrices is fixed, the order in which the individual multiplications is performed does not matter as far as the value of the result is concerned. Thus, in the example shown, we could combine the last three (transformation) matrices by multiplication to yield a single 3 by 3 matrix which represents the combined transformation. If more than three points are represented in the coordinate matrix, this technique will reduce the amount of computation necessary to calculate the result.

As a general comment, it is useful to decompose complex transformations into a series of basic transformations. Any transformation which preserves shape in the sense discussed above can be decomposed into a series of basic transformations represented as matrices. The product of these matrices will be the matrix representation of the complex transformation.

A general 3 by 3 matrix might be represented by:

$$T_3 = \begin{bmatrix} a & b & c \\ d & e & f \\ g & i & j \end{bmatrix}$$

(h intentionally omitted)

Three special cases of this matrix have been presented that represent the basic transformations. While the products of such basic transformations can yield many of the cases of the general T_3 matrix, it is useful to examine some other simple cases. The 3 by 3 identity matrix:

$$I_3 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

yields a result identical to the original set of points. This is a *null* transformation. The effect of setting elements *a* and *e* (referring to the general T_3 matrix elements) equal to other values results in scaling. Setting elements *g* and *i* to nonzero values creates a translation. The process of setting element *b* to a nonzero value is shown in the following equations:

$$x' = x$$
$$y' = bx + y \ .$$

The effect of this change on our figure "P" test pattern is shown in figure 9. This type of transformation is known as a y shear. Note how the "P" has been distorted in the y direction only by this operation.

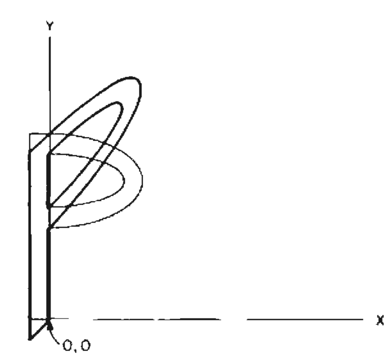


Figure 9: An example of y shear.

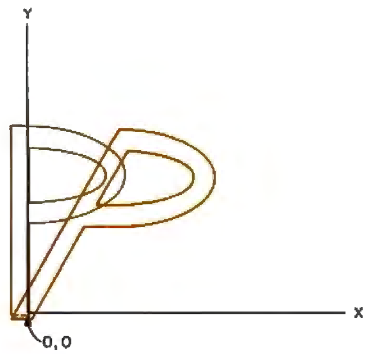


Figure 10: An example of x shear.

Similarly, setting element *d* equal to a nonzero value causes an x shear as shown in figure 10:

$$x' = x + dy$$
$$y' = y$$

If element *c* or element *f* is nonzero, or if element *I* is not one, the result of the transformation is of the form:

$$h \neq 1$$
$$[hx\ hy\ h]$$

Here, *hx* and *hy* are considered to be *biliteral* (2 letter) symbols or variable names, *not* products of *h* and *x* or *y*. In this case, we divide each element of the vector by the last (or homogeneous) element. Thus, the coordinates of the point (x,y) in two-space may be represented by an infinite number of homogeneous representations [*hx hy h*]. The process of dividing through by the homogeneous coordinate is known as homogeneous normalization (see table 1).

A particular problem arises when $h = 0$. In this case, division is undefined. An understanding of this situation is attained by letting *h* go to zero.

The value of the normalized point in table 1 goes out along a line from the origin through the point [*a b*]; as *h* approaches zero, the point goes to infinity. Thus the representation [*a b* 0] defines a point at infinity along the line from the origin through [*a b*]. This representation of points at infinity is completely consistent with all previous discussion and definitions of transformations. The only truly undefined homogeneous value in two-dimensional space is [0 0 0].

Homogeneous Representation			Normalized Representation	
hx	hy	h	x	y
a	b	1	a	b
a	b	.1	10a	10b
a	b	.01	100a	100b
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
a	b	0	undefined	undefined

Table 1: Homogeneous versus normalized representation of coordinates in two-dimensional space. The homogeneous representation of the coordinate pairs is a way of encoding the numbers in a general manner using the extra element h in the matrix row. The values of the coordinates are found by dividing h into each coordinate (expressed here as variable names, ie: "hx"; this does not mean "h times x"). The results are shown in the right side of the table. The extra column in the homogeneous form of the matrix is needed to make the matrix conformable with other matrices used for translation operations.

In transforming graphic elements, a problem may arise regarding the screen space boundaries. Portions of objects may fall outside the screen space after transformation. A similar situation may arise when objects are converted from problem space to screen space. It is therefore necessary to have a procedure for "clipping" the portions of objects outside the screen space so that the on-screen portion is accurately portrayed. The procedure described operates on the typical 4 sided rectangular screen.

The screen may be defined by four inequalities:

$x \geq x_\ell$ x_ℓ = leftmost x value
$x \leq x_r$ x_r = rightmost x value
$y \geq y_b$ y_b = bottom y value
$y \leq y_t$ y_t = top y value

The procedure operates on each line segment in the image and determines what portion, if any, lies in the screen space.

The two endpoints of each line segment are classified as satisfying or not satisfying each of the four inequalities. Three specific

Editor's Note: Analogies Between Hardware and Software

Readers with a hardware background are no doubt familiar with the concept of limiting the range of a signal, or "clipping" it. This is often accomplished using a nonlinear device such as a diode. In this article, we find the same concept used in the software which transforms a list of points making up an image so that it will fit on a display screen. Here, instead of an analog signal, the "signal" being limited is the numerical range of the coordinates being computed. The implementation is different, but the concept is identical. . .CH

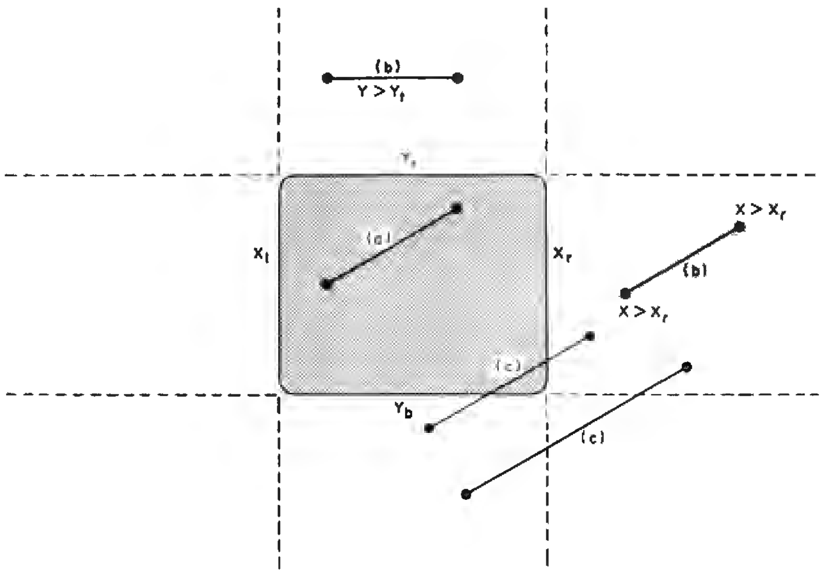


Figure 11: Three different ways a line can appear. Line (a) is completely within the borders of the video screen. The lines labeled (b) are completely outside of the screen area, and the lines labeled (c) are partially within the screen area.

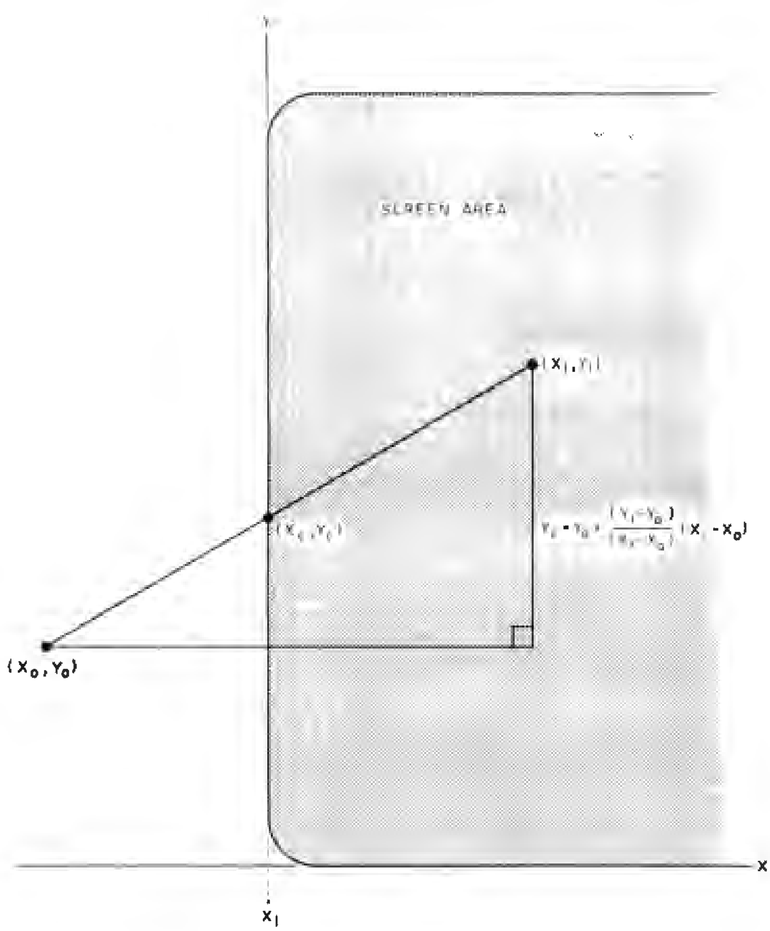


Figure 12a: Clipping. One way of calculating the cutoff point for a line is to use the traditional method of similar triangles. A disadvantage of this method is that it requires multiplication, a relatively time consuming operation on a computer.

cases may result from this endpoint coding:

(a) Both endpoints satisfy all inequalities.
(b) Both endpoints do not satisfy the same inequality.
(c) Neither of the above.

In case (a) the entire line lies within the screen space and is therefore displayed. In case (b) the entire line lies outside the screen space and is therefore not displayed. Case (c) requires further treatment.

The visible portion (if any) of each case (c) line is determined by cutting it with every inequality line (screen boundary) which is violated by either endpoint. Each inequality or clipping boundary not satisfied will cut the line into two portions, visible and invisible. The portion remaining, if any, will be the line segment visible in the screen space.

One approach to determining the point at which a line is cut by a boundary is derived from geometry (see figure 12a). The formulas for the left x boundary can be derived and the x_r, y_b and y_t results follow in similar fashion. By similar triangles:

$$\frac{y_s - y_0}{x_c - x_0} = \frac{y_1 - y_0}{x_1 - x_0}$$

but

$$x_c = x_\ell$$

so

$$y_c = y_0 + \left(\frac{y_1 - y_0}{x_1 - x_0}\right)(x_\ell - x_0)$$

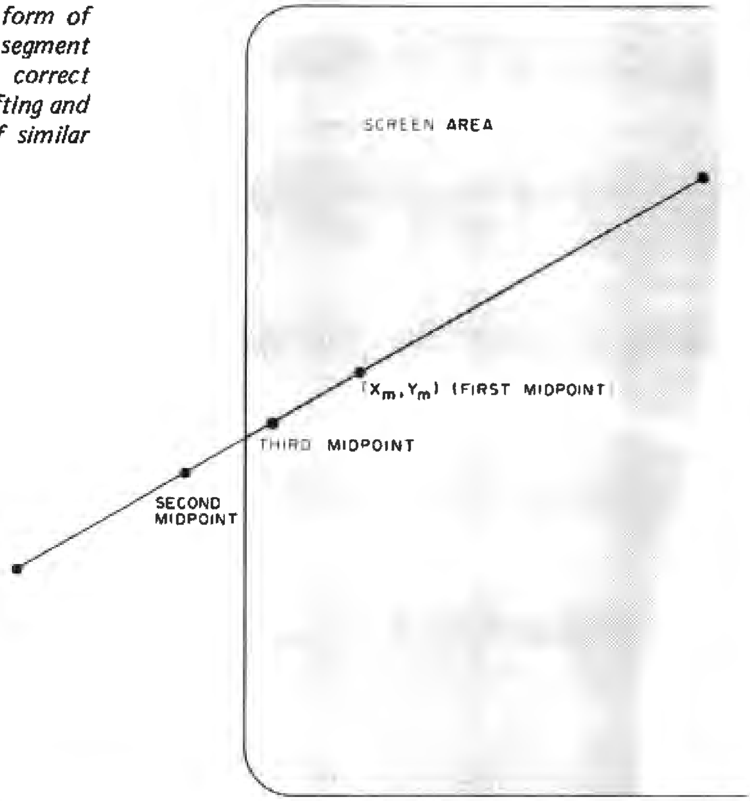
The visible portion of the line is from (x_ℓ, y_s) to (x_1, y_1).

An alternative approach, the clipping divider, is more suitable for microprocessor implementation since it uses neither multiplication nor division. It is actually a type of binary search. Using the example in figure 12b, we define (x_m, y_m) as the midpoint of the line to be clipped. (x_m, y_m) is calculated as follows:

$$x_m = (x_0 + x_1)/2 \quad \text{(add and 1 bit shift)}$$
$$y_m = (y_0 + y_1)/2 \quad \text{(add and 1 bit shift)}$$

If $x_m = x_\ell$, then y_m is the y coordinate of the clipped endpoint and the process is completed. If x_m violates the inequality, then replace (x_0, y_0) with (x_m, y_m). Recalculate (x_m, y_m). If the new x_m satisfies the inequality, then replace (x_1, y_1) with (x_m, y_m). In either of the last two cases, repeat the procedure with the new line, either (x_m, y_m) to (x_1, y_1) or (x_0, y_0) to (x_m, y_m). Because of the shifting used to calculate (x_m, y_m), the process continues no

Figure 12b: Clipping. Another method of calculating the cutoff point of a line on the screen is to use a form of binary search. The method involves halving the line segment successively until the y value converges to the correct answer. This method only requires adding and shifting and is thus quicker to compute than the method of similar triangles.



more times than the number of bits in a word and the y coordinate will converge to the correct value.

This clipping process completes the set of basic operations necessary to operate on two-dimensional information to produce graphic output.

I hope readers will be encouraged to use these practical techniques in their experiments with computer graphics.■

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APL and Graphics

Eduardo Kellerman
V34/0284
IBM Corp
Endicott NY 13760

This article presents an introduction to the use of APL for creating and manipulating graphic images. The paper carries the reader through the steps of interactive graphic design using APL and IBM 5100 APL Graphpak. The last section of this article, giving background information about APL and Graphpak, should be reviewed by the reader not familiar with either of these two topics. August 1977 BYTE is a useful source of APL information. For more detailed information about APL see the references listed at the end of this article.

The initial checkout of the examples was done using an IBM 5100 in stand-alone mode. The results were drawn on an IBM 5103 printer by modifying Graphpak to use output functions from the IBM 5100 Print Plot/APL Problem Solver Library. When the designs grew more complex, the IBM 5100 was connected to an IBM System 370/Model 168 and the code was executed there. The IBM System 370/Model 168 produced its output on a storage scope equipped with a hard copy unit.

Developing Repetitive Patterns

The first example follows a graphic designer through the development of a pleasing design for wrapping paper. Using a triangle as the basis for experimentation, the coordinates for a triangle centered at the origin are derived as shown in figure 1. A matrix, TRI, is then created to describe the triangle to the DRAW function:

```
TRI←4 3⍴1,0,1,0,(COS 30),(-SIN 30),0,(-COS 30),
        (-SIN 30),0,0,1
```

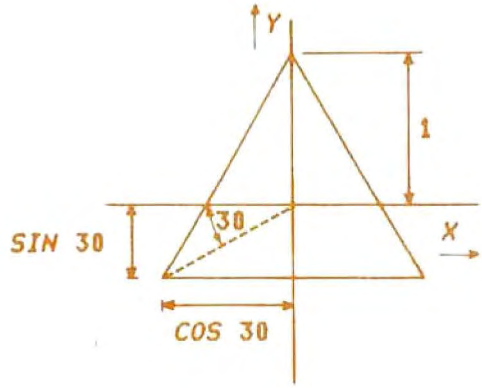


Figure 1: Equilateral triangle centered at the origin, the basic drawing block of our design.

For this example, TRI looks like:

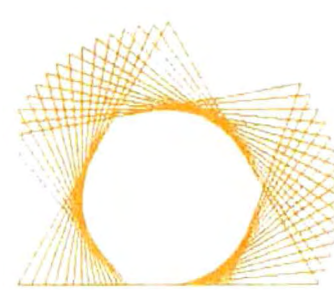
```
   TRI
1      0      1
0      0.87  ¯0.5
0     ¯0.87  ¯0.5
0      0      1
```

To create patterns, translate the TRI matrix into the display window and draw it with the following APL function:

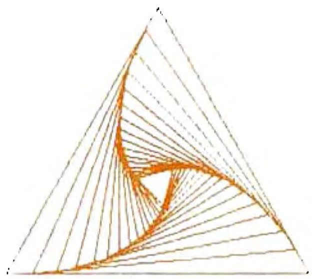
```
      ∇ DESIGN1
[1]     TR←(COS 30),SIN 30
[2]     DRAW TR TRANSLATE TRI
      ∇
```

When executed on the IBM 5100, DESIGN1 gives a very small triangle of the defined dimensions. It will be necessary to increase the size of the triangle since it is presently too small to be used in a design. The function DESIGN2, shown in listing 1, is written to rotate the triangle 15 times and then translate the magnified pattern into the viewing area before drawing it.

Note in line 4 of listing 1 that the initialization of variable OUT is to be a matrix with no rows and three columns. This is done so that OUT has the proper shape when in line 6 it is catenated with TRI2 (which has three columns). When DESIGN2 is executed on the IBM 5100 the result is:



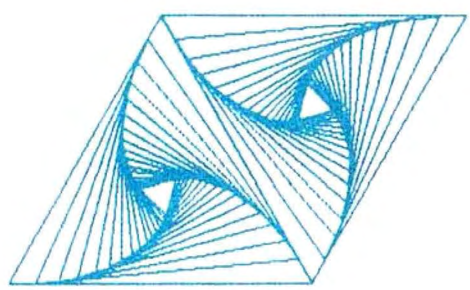
Even though the original (magnified) triangle is within the viewing window, the complete pattern is not. Instead of moving the whole pattern into the display window, the rotating triangles can be *shrunk* so they stay within each other. The result of experimenting with different shrinking factors (actually magnifications of less than 1.0) is the APL function in listing 2. Execution of DESIGN3 results in:



To extend the design over a larger area of the plane, an upside-down version of the nested triangles is used. This upside-down design is obtained by rotating the original design 180° (π radians). The original and new patterns are then drawn side by side. This is accomplished by adding the following two lines at the end of program DESIGN3:

```
[13]  OUT2←180 ROTATE OUT
[14]  DRAW 15 MAGNIFY (2×TR) TRANSLATE OUT2
```

Execution of this program gives:



This pattern is used to cover the plane. To do so, variable OUT is made into a matrix containing the description of both the original set of nested triangles and the upside-down nested triangles by replacing lines 12 thru 14 with:

```
[12]  OUT2←TR TRANSLATE 180 ROTATE OUT
[13]  OUT←OUT,[1] OUT2
```

Then, to draw the N by M tilings, two nested loops are added at the end of the APL function. These loops are incorporated in lines 14 thru 19 of the function DESIGN7, which is shown in its entirety in listing 3.

Note that, in line 16 of listing 3, unnecessary parentheses were used to make the meaning clearer. However, not enough parentheses were added to make the meaning completely unambiguous to readers not familiar with APL. For example, the expression

```
TRX×(1+2×J)
```

could be written

```
TRX×(1+(2×J))
```

```
     ∇ DESIGN2;TR;ROT;REP;OUT;TRI2
[1]    TR←(COS 30),SIN 30
[2]    ROT←0
[3]    REP←15
[4]    OUT← 0 3 ρ0
[5]   LOOP:TRI2←ROT ROTATE TRI
[6]    OUT←OUT,[1] TRI2
[7]    ROT←ROT+5
[8]    →LOOP IF 0<REP←REP-1
[9]    DRAW 15 MAGNIFY TR TRANSLATE OUT
     ∇
```

Listing 1: DESIGN2, an APL routine used to rotate the basic triangle and translate it into the viewing window. This operation is repeated 15 times. Note the use of variables in the header line of the function. This assures only local use of those variables.

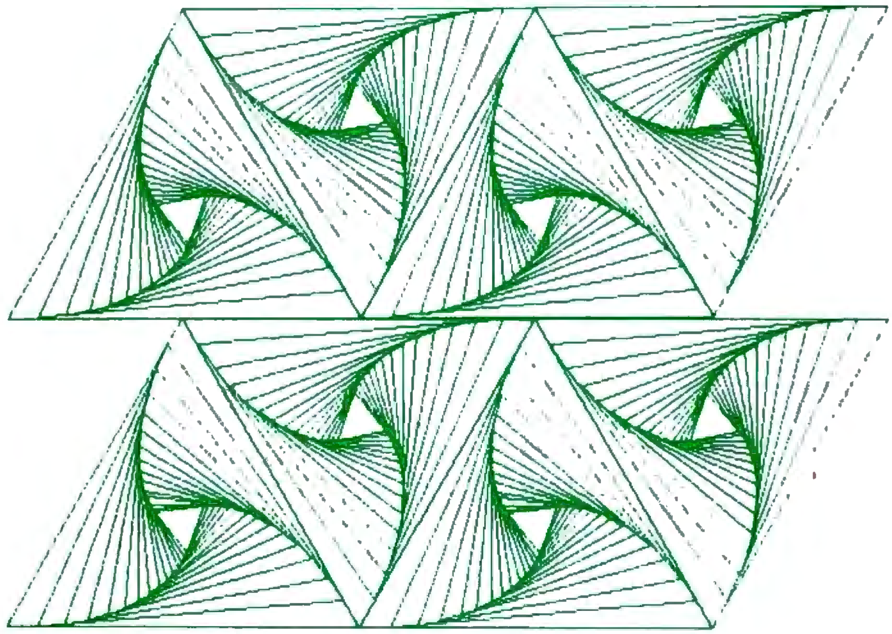
```
     ∇ DESIGN3;TR;MAG;ROT;REP;OUT;TRI2
[1]    TR←(COS 30),SIN 30
[2]    MAG←1
[3]    ROT←0
[4]    REP←15
[5]    OUT← 0 3 ρ0
[6]   LOOP:TRI2←ROT ROTATE TRI
[7]    TRI2←MAG MAGNIFY TRI2
[8]    OUT←OUT,[1] TRI2
[9]    ROT←ROT+5
[10]   MAG←MAG×0.87
[11]   →LOOP IF 0<REP←REP-1
[12]   DRAW 15 MAGNIFY TR TRANSLATE OUT
     ∇
```

Listing 2: DESIGN3, an APL routine which rotates and shrinks the basic triangle shape to keep the rotated triangles inside of the previously drawn triangle. This also keeps the rotated triangles within the viewing window.

```
     ∇ N DESIGN7 M;TR;TRX;TRY;MAG;ROT;REP;OUT;TRI2;OUT2
[1]    TR←(TRX←COS 30),TRY←SIN 30
[2]    MAG←1
[3]    ROT←0
[4]    REP←15
[5]    OUT← 0 3 ρ0
[6]   LOOP:TRI2←ROT ROTATE TRI
[7]    TRI2←MAG MAGNIFY TRI2
[8]    OUT←OUT,[1] TRI2
[9]    ROT←ROT+5
[10]   MAG←MAG×0.87
[11]   →LOOP IF 0<REP←REP-1
[12]   OUT2←TR TRANSLATE 180 ROTATE OUT
[13]   OUT←OUT,[1] OUT2
[14]   I←0
[15]  LPI:J←0
[16]  LPJ:TR←(TRX×(1+2×J)),(I+TRY×(I+1))
[17]   DRAW 15 MAGNIFY TR TRANSLATE OUT
[18]   →LPJ IF M>J←J+1
[19]   →LPI IF N>I←I+1
     ∇
```

Listing 3: APL program for drawing an N by M tiling of a surface. Each of the tiles consists of a right side up, rotated, magnified triangle series and an upside down, rotated, magnified triangle series.

Figure 2: Repetitive pattern resulting from the execution of DESIGN1. The prerequisite for accepting this design is aesthetic. The author felt that this was a pleasing arrangement of triangles.



Listing 4: A modification to listing 3, incorporated in line 16, shifts every other row of the pattern half a triangle to produce a more pleasing effect.

```
    ∇ N DESIGN8 M;TR;TRX;TRY;MAG;ROT;REP;OUT;TRI2;OUT2
[1]   TR←(TRX←COS 30),TRY←SIN 30
[2]   MAG←1
[3]   ROT←0
[4]   REP←15
[5]   OUT← 0 3 ρ0
[6]  LOOP:TRI2←ROT ROTATE TRI
[7]   TRI2←MAG MAGNIFY TRI2
[8]   OUT←OUT,[1] TRI2
[9]   ROT←ROT+5
[10]  MAG←MAG×0.87
[11]  →LOOP IF 0<REP←REP-1
[12]  OUT2←TR TRANSLATE 180 ROTATE OUT
[13]  OUT←OUT,[1] OUT2
[14]  I←0
[15] LPI:J←0
[16] LPJ:TR←(TRX×¯1+(2|I)+2×J),I+TRY×(I+1)
[17]  DRAW 15 MAGNIFY TR TRANSLATE OUT
[18]  →LPJ IF M>J←J+1
[19]  →LPI IF N>I←I+1
    ∇
```

Listing 5: DESIGN9, an APL program that produces pictures such as the one shown in figure 4. The basic pattern has been shifted from row to row to produce a more pleasing design.

```
    ∇ N DESIGN9 M;TR;TRX;TRY;MAG;ROT;REP;OUT;TRI2;OUT2
[1]   TR←(TRX←COS 30),TRY←SIN 30
[2]   MAG←1
[3]   ROT←0
[4]   REP←15
[5]   OUT← 0 3 ρ0
[6]  LOOP:TRI2←ROT ROTATE TRI
[7]   TRI2←MAG MAGNIFY TRI2
[8]   OUT←OUT,[1] TRI2
[9]   ROT←ROT+5
[10]  MAG←MAG×0.87
[11]  →LOOP IF 0<REP←REP-1
[12]  OUT2←OUT
[13]  OUT[;3]←-OUT[;3]
[14]  OUT←OUT2,[1] TR TRANSLATE OUT
[15]  I←0
[16] LPI:J←0
[17] LPJ:TR←(TRX×¯1+(2|I)+2×J),I+TRY×(I+1)
[18]  DRAW 15 MAGNIFY TR TRANSLATE OUT
[19]  →LPJ IF M>J←J+1
[20]  →LPI IF N>I←I+1
    ∇
```

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Figure 3: Full size design created by shifting the pattern of figure 2. The rows have been shifted in relation to each other for appearance.

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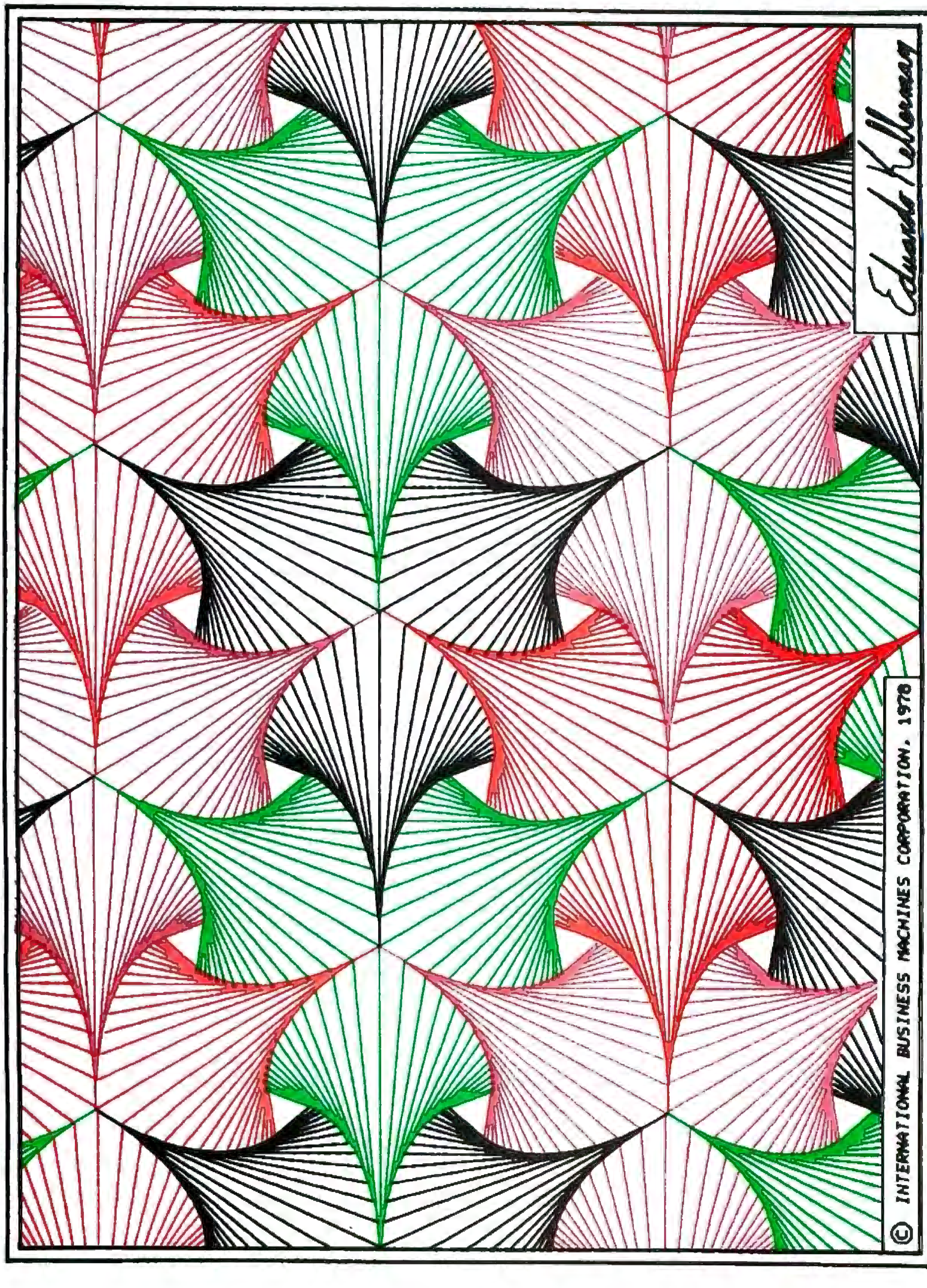

Figure 4: Pattern produced by flipping *the triangles over, an example of how easy it is to produce a wide variety of patterns with only small modifications to a basic design program.*

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The I/O section of this software has been modified to operate with the TARBELL Floppy Disk Interface in 24K bytes of memory. Five commands permit listing of directory, typing contents of an ASCII file, renaming a file, erasing a file from disk, and saving memory on disk. Fourteen programs are included which are invoked like commands. Six source files are included for transferring between TARBELL Cassette and disk, cold-start loading, Basic I/O system with drivers, and reformatting crashed diskettes. Documentation includes a listing of BIOS and instructions to patch CBIOS for your system. Price is $100 on CP/M diskette with documentation. (CP/M is a product of Digital Research).

CP/M 1.4 Update Package

A TARBELL Update Package for those now using CP/M 1.3 is now available on diskette. The Update Package adds new commands and the ability to access four disk drives, as well as 2 new CP/M manuals, TARBELL CP/M User's Guide and a new BIOS listing. Price: $50.00.

SPOOLER

This 8080 program will save many hours of computing time. It intercepts all output to the list device, spools the output to a high-speed disk file, and directs the spooled data to a low-speed printer during unused cycle time while the CPU waits for transfer of data to and from the console. System throughput is greatly increased with the aid of SPOOLER. Output is never lost due to insufficient memory allocation. Fully compatible with the CP/M file system, SPOOLER permits parallel processing without hardware interrupt, and with minimal impact on other processes. Price: $50.00 (Copyright KLH Systems.)

BASIC-E Compiler

Designed to work with CP/M Disk Operating System this software requires a total of 20K bytes of memory. Included are 26 compiler error messages and 23 run-time error messages. Disk files may be read, written or updated by using both sequential and random access. Included are blocked and unblocked files. Price for compiler and run-time monitor on diskette is $10.00. Manual is available separately for $5.00. (Public domain software by Gordon E. Eubanks, Jr.).

CBASIC Programming System

Upward compatible from BASIC-E, CBASIC is similar but expanded to include several business oriented facilities, allowing decimal computations to 14 digits of precision, data formatting and PRINT USING statements. Statements allow access to disk files and disk file maintenance. Strings of characters may be read from the console to permit correct input line format to be checked before reading data. General programming features include variable names up to 31 characters, optional line numbers, dynamic debugging tracers, and optional data output to printer. CBASIC on diskette and manual priced at $100. (Copyright Software Systems.)

EMPL-an 8080 APL

Especially suited to educational applications, EMPL is an adaptation of APL, using the ASCII character set. This 8K version occupies the first 5376 bytes of memory and operates in two modes. The Execution Mode permits all instructions to be executed immediately. The Definition Mode permits the user to enter functions. EMPL on Tarbell Cassette with manual is $15.00. (Copyright 1977 Erik Mueller).

*ALTAIR is a trademark/tradename of MITS, Inc.
**CP/M is a trademark/tradename of Digital Research.

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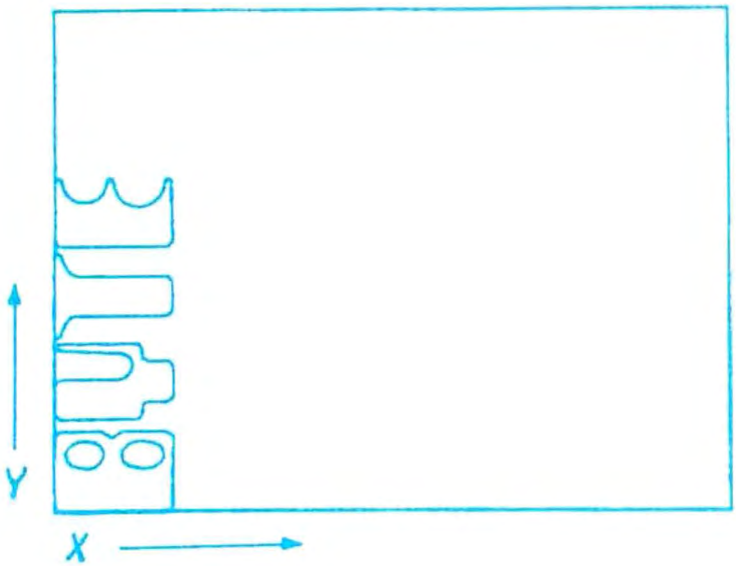


Figure 5: Basic design for example 2 in the text. The drawing window is shown for clarity.

Figure 6: Series of logos shrinking into infinity, created by experimenting with size. A magnification process is all that is required to reduce the size of the logo and converge into the origin which is at the corner.

```
      ∇ LOGOS1 ;LOGO;I;MAG
[1]     LOGO←180 ROTATE BYTE
[2]     LOGO← 100 76 TRANSLATE LOGO
[3]     I←0
[4]     MAG←1
[5]    LOOP:
[6]     DRAW MAG MAGNIFY LOGO
[7]     MAG←MAG×0.74
[8]     →LOOP IF 15>I←I+1
      ∇
```

Listing 6: LOGOS1, APL program that translates and shrinks the logo into infinity.

but in reality it needs no parentheses at all. Similarly, all the parentheses in

```
(I+TRY×(I+1))
```

are unnecessary. The values for TRX and TRY are computed in line 1 of listing 3.

Variables N and M have been placed in the header line of the new APL function, and now become part of the calling syntax for it. Trying out the new function by entering:

```
2 DESIGN7 2
```

results in figure 2.

It appears that a better design can be obtained by shifting every other row by half a triangle. This is accomplished by making use of the residue primitive function,

```
|
```

where

```
2|I
```

results in 1 if I is odd, and 0 if I is even. This change is incorporated in line 16 of DESIGN8:

```
[16] LPJ:TR←(TRX×¯1+(2|I)+2×J),I+TRY×(I+1)
```

Also incorporated in line 16 is a shift of TRX units to the left for the entire drawing. The purpose of this shift is to avoid uncovered areas in the display window.

When DESIGN8 was tested, it was clear that an appropriate selection of colors would add significantly to the design. Without going into details, DESIGN8 was modified so that it would create three different, overlapped pictures. Each could then be printed in a different color. The resulting design is shown in figure 3.

Several other interesting designs can be obtained by slight modification of program DESIGN8. For example, instead of rotating the nested triangles to obtain an upside-down pattern, the sign of the values for the Y axis of the original set of embedded triangles can be reversed. This is equivalent to flipping the pattern over. The result is shown in figure 4. The APL function used to produce the design for figure 4 is shown in listing 5. Additional designs can be created by overlapping patterns.

Designing the Cover

The areas involving graphics in which APL and Graphpak can be used are virtually unlimited. This second example follows a graphic designer who would like to create a design using a customer's trademark. He is told that the design should portray the virtues of the product. For the example consider the logo which appears on the cover of BYTE magazine.

The designer first creates a matrix called BYTE which contains the data required to draw the basic logo. This matrix was created by manually digitizing the logo. The logo can then be drawn, as in figure 5, by entering the command:

```
DRAW BYTE
```

The intention is to create the design at a 90° angle. This way the logo can be moved along the X side of the display window (which is longer than the Y side). By reducing the size of the logo as it is moved, the customer's request for creating a feeling of "never-endingness" can be met. (Note: in figure 5, and in some of the figures that follow, the outline of the display window has been added to aid in understanding the discussion.)

One way to move an object while simultaneously shrinking it is to displace it from the origin while using the MAGNIFY function to reduce the values for the X and Y axes. To move the logo diagonally across

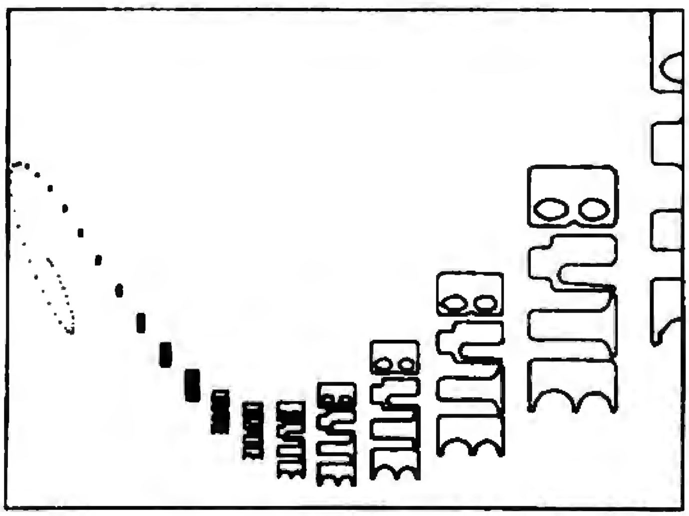


Figure 7: Spiraling design produced by incorporating a sine function into the shift process.

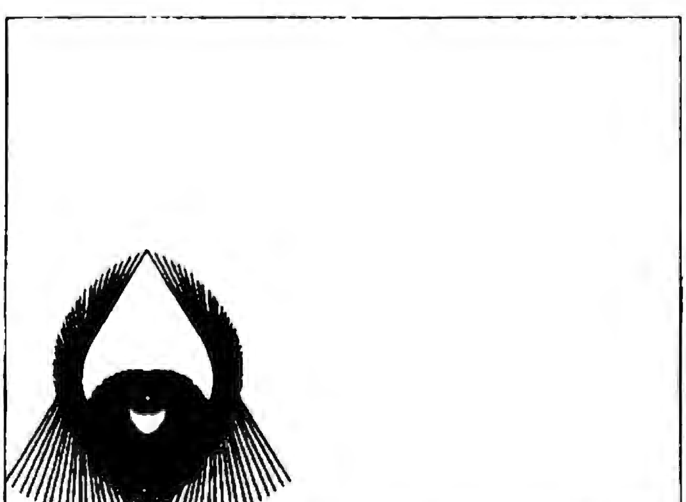


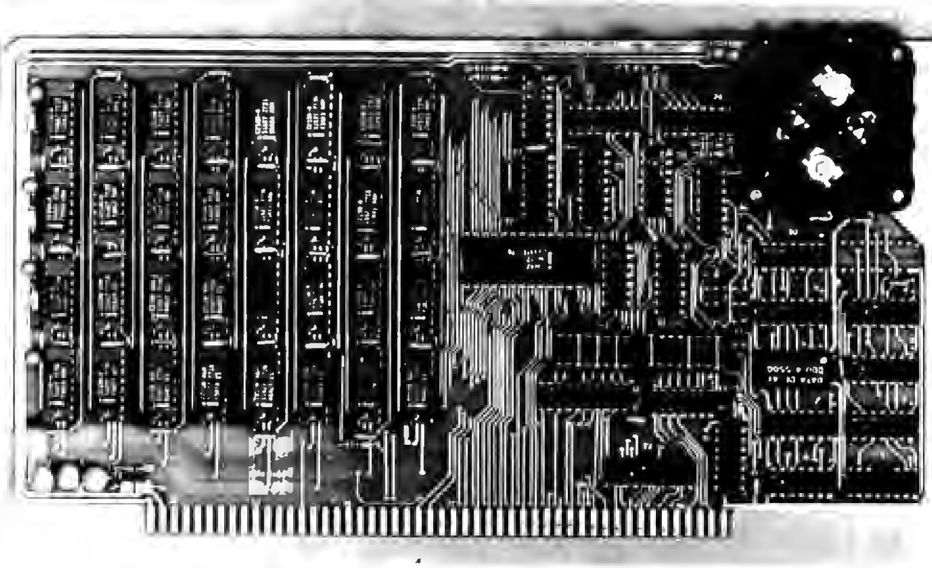
Figure 8: Pattern composed of a series of shrinking and rotating lines reflected about the Y axis to produce the symmetrical shape shown. The drawing window is displayed for clarity.

```
    ∇ LOGOS2;LOGO;I;MAG;TR;MAGSIN;MODULATE
[1]   LOGO←180 ROTATE BYTE
[2]   LOGO← 100 76 TRANSLATE LOGO
[3]   I←0
[4]   MAG←1
[5]   TR← 13 0
[6]   MAGSIN← 4.2 10
[7]  LOOP:FIG←MAG MAGNIFY LOGO
[8]   DRAW TR TRANSLATE FIG
[9]   MAG←MAG×0.74
[10]  MAGSIN←0.95×MAGSIN
[11]  MODULATE←1○((4.5-I),(I-2))÷5
[12]  MODULATE←MODULATE×MAGSIN
[13]  TR←TR+MODULATE
[14]  →LOOP IF 50>I←I+1
    ∇
```

Listing 7: Modification to the program. The addition of a sine function to the program changes the shrinking line of logos into a shrinking spiral.

```
    ∇ PICTURE1;I;M;LINE;MAG;ROT;M;Z;TR
[1]   I←0
[2]   M← 0 3 ⍴0
[3]   LINE← 2 3 ⍴ 1 0 24 0 21 ¯12
[4]   MAG←1
[5]   ROT←0
[6]  LP:M←M,[1] ROT ROTATE MAG MAGNIFY LINE
[7]   MAG←MAG×0.98
[8]   ROT←ROT-3
[9]   →LP IF 200≥I←I+1
[10]  Z←M
[11]  M[;2]←-M[;2]
[12]  Z←Z,[1] M
[13]  TR←(-⌊/Z[;2]),(-⌊/Z[;3])
[14]  DRAW TR TRANSLATE Z
    ∇
```

Listing 8: PICTURE1, an APL routine for producing a design using a series of shrinking and rotating straight lines. This design, when added to the pattern already created, results in the front cover of this month's BYTE.



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Description of Graphpak

This section covers common APL terminology, some Graphpak conventions, and a description of APL functions which are used in the paper. The discussion is, by necessity, oversimplified. It provides only enough information to understand the paper. For more complete information on APL and Graphpak, consult the references.

In APL, programs are called *functions*. *Primitive* functions are those which are part of the APL system, and are generally written as just one symbol or two overstruck symbols. One of the exceptions is the sine function which is written:

```
1○
```

For example:

```
⍳ , ⍴ , ⍉
```

A *scalar* is a single number, for example: 3.1415. In general, a *vector* consists of several numbers, for example: 3 5 2.54. This definition of scalar and vector suffices as far as this paper is concerned. However, the exact definition of a scalar is "an object with 0 dimensions," and for a vector, "an object of 1 dimension." In fact, a vector can contain one or more elements or be empty.

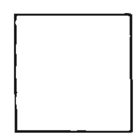
This paper is limited to the "Drawing Component" and parts of the "Descriptive Geometry Component" of Graphpak. For a description of the other components of Graphpak refer to the *IBM 5100 APL Graphpak, Program Description/Operations Manual.*

The descriptive geometry functions of Graphpak are designed to perform geometric transformations on descriptions of three-dimensional objects, and to display projections of the transformed objects on the display window. The Graphpak display window is normally a rectangle in the XY plane with the coordinate origin at the left bottom corner. In this paper the width (X direction) of the window is 100 units and the height (Y direction) is 76 units. Even though only two-dimensional objects are used here, the transformations take place in three-dimensional space. The Z dimension is assumed to come perpendicularly out of the page.

To describe a series of lines to be drawn by Graphpak, a matrix with three columns is used. The first column is a binary vector. A 1 tells the program to go to the (X,Y) position indicated by columns 2 and 3 without drawing a line. A 0 means go to the indicated (X,Y) position while drawing a straight line. The function *DRAW* takes as its argument a matrix that describes a series of lines and draws them. For example, if the variable *BOX* contains:

```
1  0  0
0 10  0
0 10 10
0  0 10
0  0  0
```

then *DRAW BOX* gives:



The desired values can be placed in *BOX* by entering

```
BOX←5 3⍴1 0 0 0 10 0 0 10 10 0 0 10 0 0 0
```

where

```
⍴
```

(rho) is the reshape (primitive) function. The

Table 1: Geometric transformation functions used in this article.

Z←D TRANSLATE X	Yields *Z*, a matrix which describes the object *X* having been translated *D[1]*, and *D[2]* in the X and Y directions, respectively. If *D* is a scalar (a single number), it is assumed to be a translation in the X direction.
Z←A ROTATE X	Yields *Z*, a matrix which describes the object *X* having been rotated *A[1]*, *A[2]*, and *A[3]* degrees counter clockwise (looking in) about the X, Y, and Z axes, respectively, in that order. If *A* contains only one or two values, enough zeros are assumed to precede it to make its length equal to three.
Z←P MAGNIFY X	Yields *Z*, a matrix which describes the object *Z* having been magnified *P[1]* and *P[2]* times in the X and Y directions, respectively. If *P* is a scalar, the function extends that number to all coordinates.

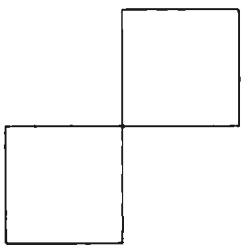
left argument of rho specifies the shape to be given to the right argument. If two matrices describing two objects are to be put together, they can be *catenated* in the first dimension using

```
,[1]
```

For example, using the *TRANSLATE* function (whose description follows):

```
BOX2←10 10 TRANSLATE BOX
DRAW BOX,[1]BOX2
```

gives:



The geometric transformation functions used in this article are summarized in table 1. In the descriptions given in table 1, *TRANSLATE* and *MAGNIFY* are described as operating only in the X and Y directions. This is a simplification for the purpose of the paper. They are capable of performing three-dimensional manipulations.

In addition to the Graphpak functions, the following APL functions are used here:

```
    ∇ Z←A IF B
[1]   Z←B/A
    ∇

    ∇ Z←SIN X
[1]   Z←1○X×(○2)÷360
    ∇

    ∇ Z←COS X
[1]   Z←2○X×(○2)÷360
    ∇
```

The *IF* function is used to make the APL code used in the paper clearer to readers not familiar with APL. The *SIN* and *COS* functions are also used to make the code clearer to readers not familiar with APL; but in addition, they take an argument expressed in degrees (the APL primitive trigonometric functions assume their arguments to be expressed in radians).

the display window after rotating it 180° requires:

```
DRAW 100 76 TRANSLATE 180 ROTATE BYTE
```

Incorporating the above into the APL function LOGOS1 (listing 6) to test the hypothesis produces figure 6.

Next the designer tries to make a spiral by adding an X and Y translation to the shrinking logo using a sine function (in APL, sine is designated by:

```
1○
```

followed by an argument in radians) which decreases in magnitude. After some experimentation the function in listing 7 was found.

Note the shift by 13 units in statement 5 of listing 6. This was necessary because the translation using sines (statements 10 thru 15) carried the design into negative X values. Execution of LOGOS2 results in the pattern of figure 7.

There is still some empty space which could be filled with some type of interesting design. After experimenting with rotating a shrinking line, the function in listing 7 was developed.

Lines 10, 11, and 12 of PICTURE1 create a symmetrical picture by reflecting the figure generated about the Y axis. Line 13 determines the minimum translation required to get the figure within the display window. Execution of PICTURE1 results in figure 8. After rotating and making smaller drawings of the design created by PICTURE2, they are placed in the design created with logos. The finished product can be seen on the cover of this issue of BYTE.

In summary, we have followed a graphic designer using APL and Graphpak through two problems and have seen the ease with which these software tools can be used for creating and manipulating graphic images.■

REFERENCES

1. *APL Language,* IBM form GC26-3847.
2. *IBM 5100 APL Graphpak, Program Description/Operations Manual,* IBM form SB30-0850.
3. *IBM 5100 APL Graphpak Application Brochure,* IBM form GB30-0850.
4. *IBM 5100 Print Plot/APL Problem Solver Library, User's Manual,* IBM form SA21-9264.
5. Iverson, K E, *An Introduction to APL for Scientists and Engineers,* APL Press, Pleasantville NY, 1976.
6. Iverson, K E, *APL in Exposition,* APL Press, Pleasantville NY, 1976.
7. Iverson, K E, *Introducing APL to Teachers,* APL Press, Pleasantville NY, 1976.

A good practice in APL is to localize variables needed only within a function by placing them in the header line of the function. In this way all the local variables will disappear from the workspace when the function completes execution . . . **RGAC**

BYTE's Bits

UCLA Computer Club 20th Anniversary Party

The UCLA Computer Club will be holding a 20th anniversary party and reunion in October 1978. The *tentative* date is October 14. The intent is to have club members from every era (WDPC, Computing Facility, ARPA, CCN) present so that everybody has old friends to talk to. "Resistors" are also welcome.

If you are a former UCLA Computer Club member, or you knew old members and would like to see them again, please send your name, address, and phone number to Joe Katz, Computer Club, 3514 Boelter Hall, UCLA, Los Angeles CA 90024. A complete list will be sent to everyone who responds whether they decide to attend or not.■

A Worm Invades an Apple. . . (or, Computer versus Computer)

Rumor has it that the underground technology of defrauding the telephone monopoly took a dubious step forward with the notorious "Capt Crunch's" latest escapade. Word is that the Federal prosecutors in the trial will introduce an Apple II computer in evidence as the instrument of the crime.■

More Notes from the Rumor Mill: Heath Software

According to highly reliable sources, Heath is offering a slightly scaled down version of the DEC RT11 operating system (version 2C) as part of their H27 dual full-size floppy disk kit. The software package, called the HT11, is being bundled with the floppy kit for a total price of approximately $1700, and will be available in October 1978. The RT11 operating system (well-known in minicomputer circles) plus the RX01 dual floppy disk system would cost about $7000 if purchased from Digital Equipment Corporation (DEC).

The only difference between the RT11 and HT11 packages is that the latter does not have the super macroassembler or the foreground-background monitor (plus some additional utilities). It does have DEC's standard BASIC, however. Heath will also be offering DEC's standard FORTRAN package for $100.

Finally, there is a possibility that Heath will be offering a UCSD Pascal package for $200 in the near future.■

Computerland's Second Birthday

Computerland, currently the largest *computer store* chain, reports to us that they will be celebrating their second birthday on Saturday, September 23. Customers and friends are invited to local outlets of the chain. In our opinion, as patrons of the Nashua NH store, Computerland has to be one of the best planned and managed retail operations in this business. We trust that the Nashua store is typical of the other stores in this chain, which number over 40. . . .CH■

BYTE's Bugs

Capacitor Value

In Robin Moseley's article "A Low Cost Light Wand Amplifier" (May 1978 BYTE, page 92), the value of capacitor C1 should be approximately 47 mF.

Anyone using the optional peak detector to measure the amplifier output should allow for the forward drop of the two detector diodes and adjust the circuit for a DC output voltage from the detector of approximately 0.5 V.■

Meetings in Bedford MA

In July 1978 BYTE, we mentioned in the Clubs and Newsletters section that the New England Computer Society meets monthly at the Mitre Corp Cafeteria, Bedford MA. However, we neglected to mention that they meet the first Wednesday of each month at 7 PM. (Members of the BYTE editorial staff are usually in attendance at these meetings.)■

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ROM Magazine, January 1978, writes, "THE PET comes out of the box, plugs into the wall, and is ready to use." It is equipped with a CRT video display with reverse and blink features, an alpha-numeric keyboard with complete graphics and a built-in standard cassette tape deck.

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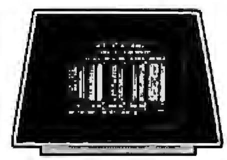
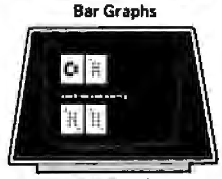
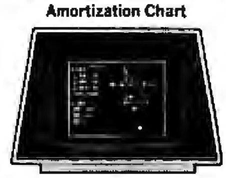
Bar Graphs



Amortization Chart



Black Jack



Teaching Trigonometry

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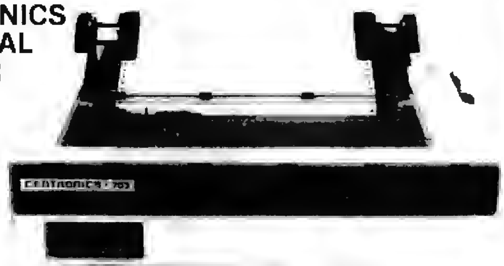

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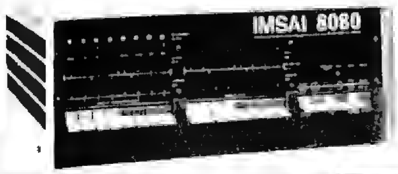

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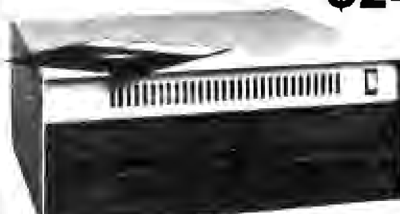

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A "Tiny" Pascal Compiler

Part 1: The P-Code Interpreter

Kin-Man Chung
124 Scottswood Dr
Urbana IL 61801

Herbert Yuen
POB 2591, Station A
Champaign IL 61820

Roughly speaking, a compiler is a program that translates the statements of a high level language (such as Pascal or FORTRAN) into a semantically equivalent program in some machine recognizable form (such as machine or assembly code). The former is usually referred to as the source program while the latter is called the object program. An interpreter, on the other hand, reads in the source program and starts exection directly, without producing an object program.

There is little doubt that compilers and interpreters are a necessary part of any computer system. The reason most personal computer systems do not have high level language compilers is not that there is no need for them. Compilers, being inherently more complex than interpreters, require more effort to write and more computer memory to run. The main advantage of a compiler over an interpreter is the relative speed. A compiled program typically runs an order of magnitude faster than an equivalent program executed interpretively. In fairness, it must be also pointed out that interpreters are usually easier to use, and more suitable for an interactive environment.

This series of articles is an attempt to describe how a compiler for a subset of Pascal was implemented on an 8080 computer system. It is not our intention to go into details for the reasons for the choice of the language. Pascal is widely recognized as superior to many other languages. For an overview of the language, readers are referred to August 1978 BYTE. The publication, *Pascal: User Manual and Report*, by Kathleen Jensen and Niklaus Wirth (Springer-Verlag, 1974) should also be consulted as the authoritative source book on the language in its original form.

This is not, of course, the first Pascal compiler ever written for microcomputers. However, instead of waiting for a Pascal compiler to be written for our particular processor, we decided to undertake the project ourselves. In this way, we can add or subtract features from the original Pascal to suit our needs and system capabilities, so that it can be easily integrated with other system software developed so far.

2 Stage Compiler

The compiler is divided into two stages: a p-compiler and a translator. Instead of having the compiler generate machine code directly, it generates code for a hypothetical machine, called the p-machine. These codes, called p-codes, are then converted into the target machine codes by the translator. Dividing the task of a compiler into two stages offers several advantages. The compiler can be written abstractly, without committing oneself to a particular machine and worrying about details of code generation and optimization. Such a compiler is said to be portable, meaning that it can be used on other computer systems with minimal start up effort. It is only at the last stage of code translation from the p-codes to actual machine codes that we have to commit ourselves to a particular machine.

Another advantage this method offers is greater flexibility when writing the compiler. The compiler and the translator can be coded and debugged separately. The flexibility of such a compiler was apparent to us as we started to introduce more and more Pascal features into our original minimal subset. Seldom was it necessary for us to introduce new p-codes other than those originally specified.

There is also one more reason for breaking

About the Authors

Kin-man Chung is currently a graduate student at the University of Illinois at Urbana-Champaign. Presently his equipment includes an Altair 8800 with 44 K bytes of memory, a North Star disk system, a 100 cps impact matrix printer, and a Selectric terminal. His current interest in microcomputers is the development of an interactive Pascal compiler for microcomputers, and a high resolution graphics system capable of animation.

Herbert Yuen received a master of science degree in computer science from the University of Illinois at Urbana-Champaign. He is presently working full-time as a research assistant at the university. His primary interest in microcomputers is software systems development. One of his future plans is to implement a small information retrieval system for a microcomputer.

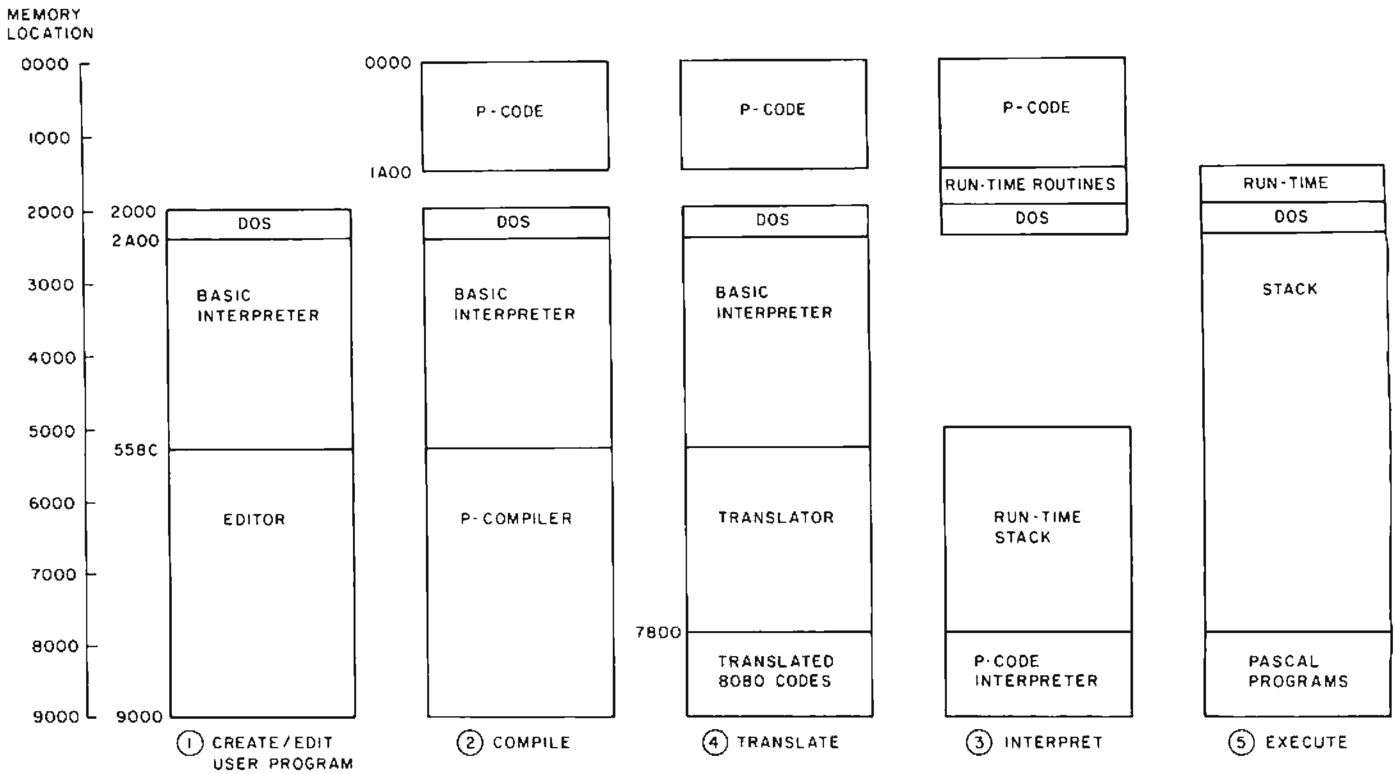

Figure 1: Memory overlay structure of the modules of the compiler. The North Star DOS and BASIC start at hexadecimal 2000 and take up approximately 14 K bytes of memory. The p-compiler is the largest BASIC program of the system; in its compressed form (void of all comments and blanks) it occupies 14 K bytes. It reads Pascal source programs created by the editor from disk files, and generates relocatable p-codes directly in memory. We use hexadecimal 0000 to 19FF for p-codes and find it adequate for Pascal source programs under about 300 lines in length. The smaller translator (9 K bytes) produces 8080 codes directly filled into memory. The origin of the codes can be specified. The run time routines (which total 1 K bytes of memory) are needed only when the translated 8080 codes are being executed. The interpreter is written in Pascal, compiled and translated. The BASIC interpreter is no longer needed when it or any other Pascal program is being run.

the compiler into two stages: most small computers do not have enough memory space to store the complete compiler. After the p-codes are generated, the p-compiler is no longer needed, and can be overlaid with the translator. Therefore the compiler and the translator can share the same memory locations.

Actually we also use two other utility programs: a text editor and a p-code interpreter. The editor is used to prepare the Pascal source programs. The interpreter is used to interpret the p-codes produced by the p-compiler. This provides another alternative for running the Pascal programs. Because it is equipped with various debugging aids, such as setting up breakpoints in p-codes and outputting values for variables, debugging can be easily done. Only after a program is verified to be correct is the translator loaded, and 8080 code produced. This allows easy development of the Pascal programs without sacrifying efficiency at run time. Figure 1 shows the overlay structure for the various modules of the compiler. Figure 2 shows the logical flow during a program development.

In this part of the series on our project, we will describe the general plan. The Pascal subset is defined using syntax diagrams. A description of the p-machine and its codes are also given. We will discuss the p-compiler, translator and runtime routines in the following parts.

Bootstrap Compiler

How does one introduce a new language into a computer system with limited computer resources? By computer resources we mean not only the computer hardware like memory and peripherals, but also software tools. We have learned from experience not to attempt programs with the complexity of a compiler in machine or assembly language. This left us with BASIC. Although it is not the most desirable language to write a compiler with, it turned out to be adequate. Some careful thought is needed, of course, to handle recursive subroutine calls from BASIC, a feature central to our compiler writing.

The alternative to BASIC is to go to a commercial computer and write the whole or part of the compiler in an appropriate

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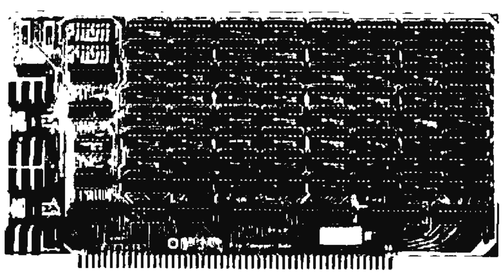

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language. The finished product (or part of it) can then be transferred to the smaller computer. This is, however, a luxury most of us cannot afford.

Of course, the compiler written in BASIC

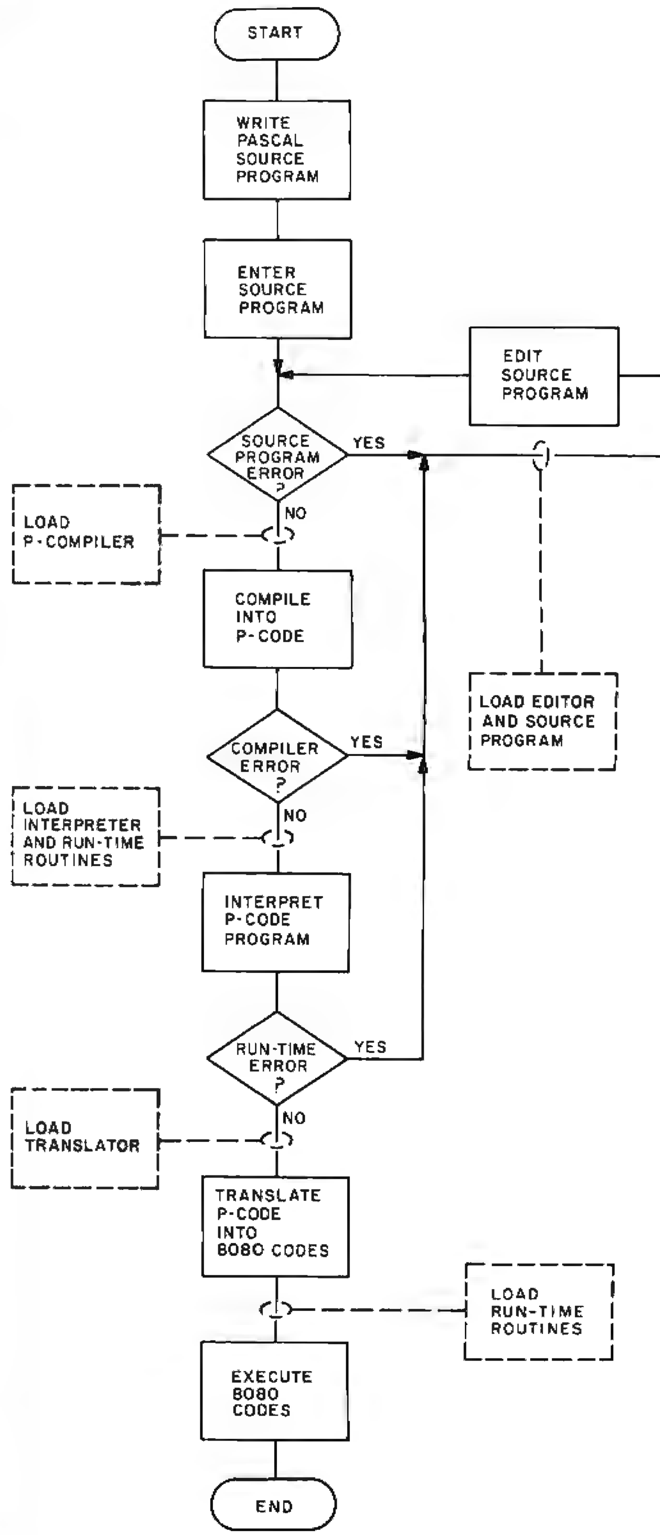

Figure 2: Flowchart showing development of a Pascal program.

would be very inefficient and slow. But this actually would not matter, since it would only be used as a *bootstrap* compiler. The concept of bootstrapping should be familiar to most personal computer owners. We usually use it when initially starting up our computers. After turning on the power, a bootstrap loader is first loaded into the computer (either manually or through the use of read only memory). This bootstrap loader is then used to load the loader, which in turn loads the monitor into memory. The bootstrap loader is a smaller version of the loader; it is just big enough to load the main loader and not adequate to be a general purpose loader.

The same idea can be applied to compiler writing. A compiler for a small subset of a language is first written. This subset should be big enough so that a compiler for a bigger subset of the same language can be written in it. The larger compiler is then written and compiled, using the first compiler. Next, a compiler for a still bigger subset of the same language can then be written and compiled, using the second compiler, and so on until a compiler for the complete language is produced. In actual practice, no more than three stages are used. It does not matter if the first compiler is very inefficient. The idea is to get a working, albeit primitive and inefficient, compiler with minimum starting effort.

Pascal Subset Syntax

The syntax of Pascal can be described precisely by using a notation usually called Backus-Naur form (BNF). This is a collection of rules for the grammar of the language. Instead of dealing with Backus-Naur form directly, we use an equivalent but more understandable notation: the syntax diagrams. Figure 3 describes the syntax of the Pascal subset we are interested in.

In the syntax diagram, the square boxes are called nonterminal symbols, while the ovals are called terminal symbols. Terminal symbols are the basic building units of the language and require no further expansion. In our case, the names that represent the terminals are also their textual representations in the language. The nonterminal symbols in the syntax diagrams can be expanded using rules specified in another syntax diagram, and there is a syntax diagram for each nonterminal symbol in the syntax diagram. A branch in the diagram represents options allowable by the grammar. When all nonterminal symbols are eliminated by expansion in this fashion, we would have a valid program. We start off a compilation with the nonterminal program. Looking at

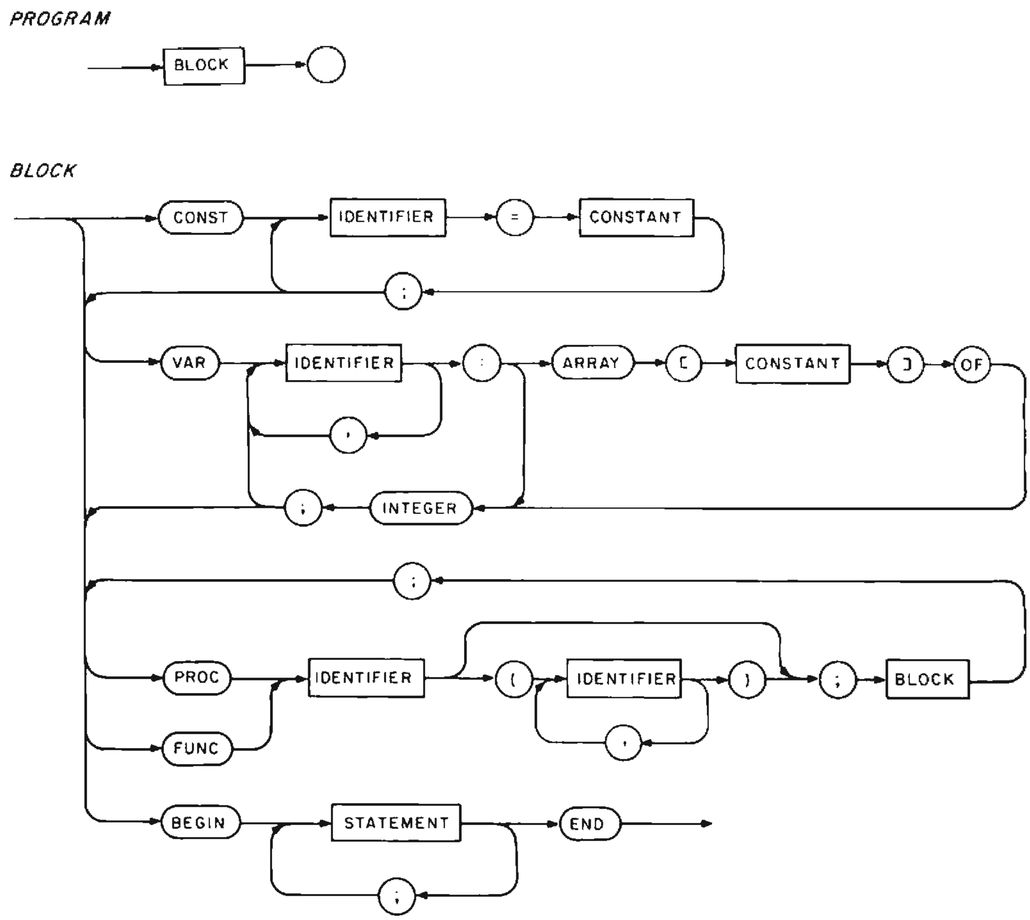

Figure 3: Syntax diagrams of the Pascal subset. For the syntax diagrams of the full Pascal set refer to the book by Kathleen Jensen and Niklaus Wirth, entitled Pascal: User Manual and Report. *These diagrams totally define the subset of the language that we are using.*

the syntax diagram we see that a program is a block followed by a period (.). Looking at the syntax diagram for block, we notice that it can have an optional declaration part followed by the main body which begins with the string **begin**, followed by any number of the nonterminal symbols, statement, separated by semicolons (;), and then the string **end**. The statement block can be further expanded by the syntax diagram for statement, and so on.

The reason we go through the details here is because it is important to precisely describe the features we want to include in our language before starting to write the compiler. It is the first step towards writing the compiler. These syntax diagrams will later become flowcharts for the syntax analyzer of the compiler.

Readers familiar with Pascal will no doubt notice several important features missing from our subset. There is no GOTO statement. The only data type we have is integer and integer array of one dimension. Also missing from the subset is the structured data type, pointer type, user defined type, and file type. A less obvious omission is passing the parameter of a procedure by address; the parameters are passed by value only. Aside from the fact that these features are difficult to implement, they are not indispensable in our bootstrap process. Of course, features like user defined type and structured type are some of the unique features of Pascal, and should not be omitted in the long run. But we feel that they can be added later.

We have also included some trivial but nevertheless useful enhancements to the language, which we hope do not deviate from the standard too much. One is the addition of the optional clause **else** to the case statement which provides an exit path if the value of the variable does not fall into any of the **case** labels. Another is the inclusion of format controls in the read and write statements. Following an expression in a *write* statement, a pound sign, #, indicates numeric form and a percent sign, %, indicates hexadecimal format. If there is no format control, a character whose ASCII code equals the expression is output. Also a hexadecimal constant is prefixed by %. This allows processing of hexadecimal numbers without conversion by the user.

To allow interfacing Pascal programs with assembly programs, a facility is provided to read or write a byte from or to absolute memory locations. The array *mem* is a reserved array name that is used to do this.

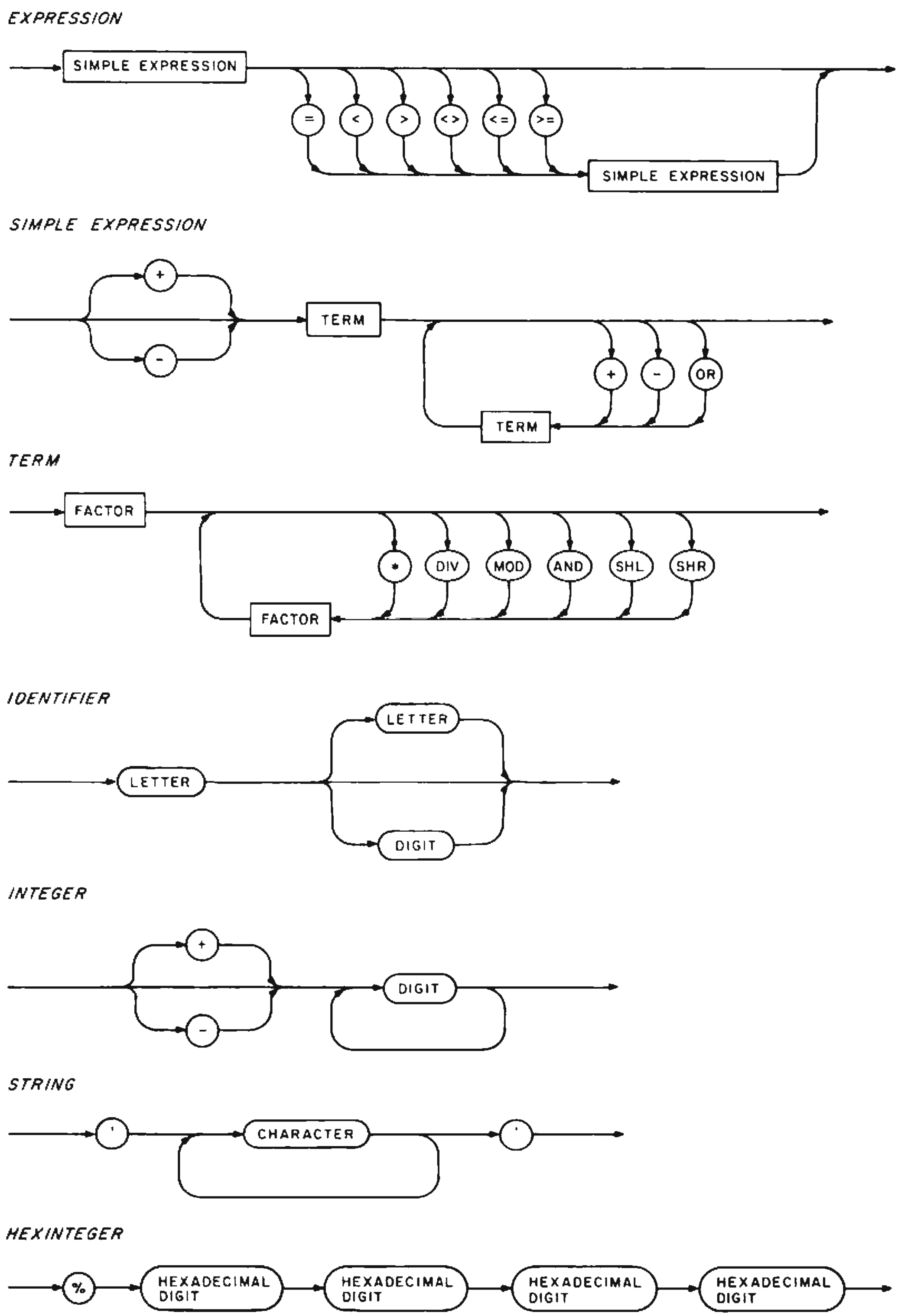

Figure 3, continued: Elementary constructs for Pascal subset. Hexinteger is usually not defined in Pascal but is used here so that actual memory locations can be easily manipulated.

Continued on page 149

Continued from page 17

List price was about 100,000 Yen, which means it will sell discount for about 80,000+ Yen. Like the PC1200 (already on sale in the US) the PC1300 seems to use Sharp's own 4 bit 1 chip 64 pin flatpack microprocessor, with 2 K bytes of read only memory on chip. Sharp earlier released the EL-6000, a child's arithmetic practice calculator.

Mitsubishi had a 4 bit microprocessor (M58840) with on-chip 8 bit analog to digital converter (5% accuracy claimed).

Panafacom had the C15, a BASIC language 16 bit machine with touch keyboard, video display, 15 ips Philips cassette, but no printer (it will be an option). Its BASIC includes graphics, matrices (option) and strings, cassette tape utilities and commands for its IEC bus option. (The 16 bit chip is not new.) 700,000 Yen with 16 K memory, 16 K expansion will be option. They also have a do it yourself kit, the "L-kit," with color graphics.

NEC's BASIC station, a do it yourself 8080 board with hexadecimal keyboard, plus separate alphanumeric keyboard, video (TV) and cassette interfaces, runs a 4 K Tiny BASIC with peek, poke and graphic commands. It costs about 200,000 Yen. Their Level 2 BASIC, with strings, subscripts and arrays, and standard (sin, log, etc) math routines plus up to 18 character alphanumeric names, is due in July. (Level 1 and Level 2 are not compatible, maybe they plan to use their new 16 bit chip μPD768B).

A small company, INPEX, has an 8085 kit with large keyboard for machine language programming; the keys correspond to opcodes Cost is about 80,000 Yen.

KS Wilkinson
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JAPAN

RARE CHASSIS?

I want to thank Dan Fylstra for his article in the May 1978 BYTE, page 22, "Convert Your TV Set to a Video Monitor." It was clearly written and well illustrated. I was about to purchase a TRS-80 from Radio Shack and his article convinced me that I should buy a Hitachi TV and a Pickles and Trout converter. Thus I would have both a computer display and a portable TV.

But alas! I live in Dallas TX. And in Dallas TX not one store that I called that handles Hitachi TVs has the models with the SX chassis! What's more, the Hitachi district offices listed in the yellow pages have closed and I was given a phone number in Atlanta GA! Now I could have called long distance to Atlanta, but I wasn't interested in ordering a TV from Atlanta or Tokyo. Chances are the model has been discontinued anyway.

Pickles and Trout had a good idea, but does a 12 inch TV exist that is not AC/DC? A TV chassis with a transformer type power supply does allow an easier hookup than does a "hot" chassis. But if one is not generally available, there is a market for an AC/DC converter that is as specific as the Pickles and Trout unit.

As for me, I ordered the TRS-80 complete with display cathode ray tube (CRT). After all, they toss in the cassette recorder if you buy the whole thing! But I do hope the SX chassis does exist elsewhere so others can use Mr Fylstra's article.

Clarence J Stinson
9138 Chimney Corner
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Thank you for any help you can provide.

Brad Slocum
236-D E Red Oak Dr
Sunnyvale CA 94806

*We've not published such an article to date, but it would make an excellent topic for the homebrewer. For output one could use one of the new electrostatic printers with graphic capability which retail for about $800 – or simply display the images on your video outputs with bit map graphics, possibly using colors where available. . . .*CH

DREAMING . . .

I am 12½ years old, and plan to get a computer system up and running in the near future. The mainframe I have selected is the Heathkit H11, incorporating the DEC LSI-11 processor. I chose this mainframe because of the processor employed and the low price, only $1295. This price is offset by a few disadvantages, such as its bus, with only six slots, and the fact that its price is only relatively low (at this time I have only $724.08). But, like any other problems in this world, these can be solved. I can fix the bus problem by simply buying an expansion interface from DEC, but this makes the second problem worse yet. And, unlike other problems, buying more of what you need (money) simply defeats itself in its purpose. So I just have to save. (And save, and save. . . .)

However, by the time I finally do

have the money for it, something bigger and better (and slightly more expensive) will have appeared on the horizon. I will probably continue at this pace until I am a millionaire at 21. At this point, of course, I will buy a large computer from DEC or some other company and charge people to timeshare on it. Only problem is, I don't know where I am going to get the million dollars in the first place. It's nice dreaming, though, and my dreaming is going to get me somewhere in this world. (I hope so, anyway!)

Norman Aleks
659 Driftwood Ln
San Dimas CA 91773

A sound philosophy. . . .

GOTCHA!

On page 154 of the May 1978 BYTE you described the new products by Lucas-Adams Labs Unltd. The address of this manufacturer was not printed. Could you please let me know the address so that I can enquire about the products?

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*Unfortunately, Lucas-Adams Labs Unltd did not supply us with their address. However, we thought that our readers would be interested in their (totally fictional) product line so we published the press release. I am sure that with perseverance, their address may be found in the combined annals of April fools jokes for this year. . .*RGAC

KUDOS FOR KENT

It seems E W Kent ("The Brains of Men and Machines," January through April 1978 BYTE) has violated Higher Education Law #1: Never explain complex issues in understandable terms. Kent must be aware of the ramifications of violating this most basic principle of higher education, the most significant being the release of usable information to lay people who might understand it and use it.

Kent has produced a classic, and has given the computer scientist a game plan for the creation of the first real cybernetic system. He has also given the electrical engineering community a new direction: if you are an engineer, think neuron and cortex instead of bus and processor. While you are doing this (in conjunction with people like E W Kent), the computer scientist will be developing algorithms and operating systems to support your hardware. We have a long road ahead, but thanks to Kent we're on our way.

David R Fashenpour
5411 Cerro Vista
San Antonio TX 78233■

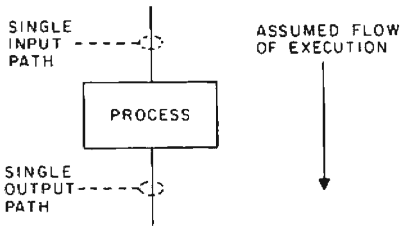


Figure 1: The process block is the "black box" of programming: it is entered by a single input path, does some arbitrary operations upon data, and is exited by a single output path. The "arbitrary operations" can be as simple as one step in an arithmetic calculation, or as complex as a compilation of a program — it all depends on the point of view taken.

Some Words About Program Structure

Albert D Hearn
98 SW 13th Av
Boca Raton FL 33432

Microprocessor programming, at this point in time, is a black art. Once you have learned the basic instruction set, you're on your own. Some people get the knack of this mysterious task fairly quickly, and some do not. Those who do well seem to have developed some sort of system for going about it. The point is that an organized, systematic approach is required if there is any hope for continued programming success. The purpose of this article is to describe to you one such method which has become very popular with programmers of all types, using all kinds of computers from micros to the giants.

Concept

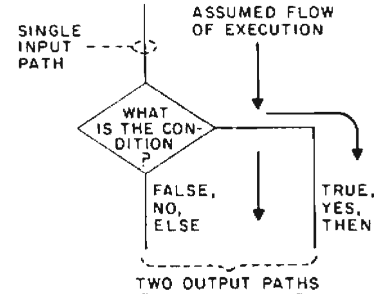
What we're looking for is simplicity in the writing of programs. This is usually achieved if the program can be reduced to a collection of basic components which fit together in very well-defined ways. This is the concept behind structured programming.

Any program can be considered to have only two basic building blocks. One is the process block shown in figure 1. It simply performs some defined function, or process. It might represent a simple function requiring only a few, maybe only one, instructions in the program, or a much larger function requiring many instructions. Whatever it does, it has one input and one output.

The second basic block is the decision block shown in figure 2. This elementary capability of any computer is that which gives it all its power and flexibility. It is the ability to alter the path taken by the program based upon the value of some parameter or condition which can be tested by certain instruction types. For example, two numbers can be compared and a test for equality used to decide which of two program paths will be taken as a result.

These two fundamental building blocks will now be used in the construction of a set of basic program structures with which any other program can be built. The three general structures are called *sequence*, *if-then-else* and *loop*. Variations of these will be examined, as well as combinations which can be used to build more complex functions.

Figure 2: The decision block is a simpler concept than the process block, in the sense that the amount of computation required rarely approaches the generality of an "arbitrary process." A decision block has one input and, depending upon a binary condition, takes one of two output paths. In this figure, the names "true," "then" and "yes" denote one possible path; the names "false," "else" and "no" describe the other possible path. In programming languages, the "then" or "else" terminology for the two paths is frequently built into the language design; the other terms are frequently seen in flowchart representations of programs.

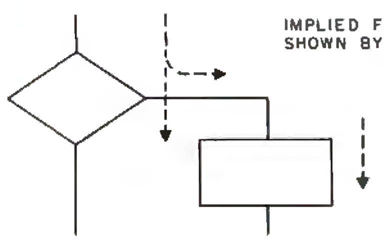


Remember: In structured programming, everything is a process block, with one input path and one output path.

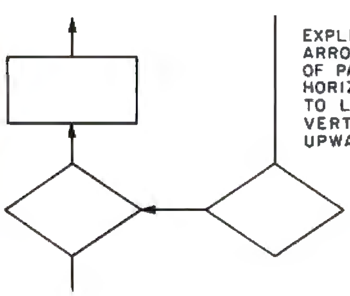
Editor's Note:
BYTE Flowchart Flow Conventions

As an "ideal" standard, flowcharts in BYTE use a direction of flow convention as follows:

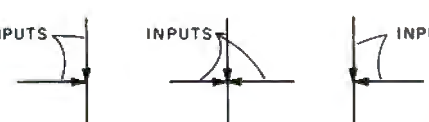
Default flow: *Vertical flow is from the top of a diagram toward the bottom, and horizontal flow is from the left of a diagram towards the right, unless explicit flow is used. Thus:*



Explicit flow: *Vertical flow upward or horizontal flow leftward in a drawing is shown with an explicit arrow at the end of the flow path, thus:*



Merged flow: *When two or three paths of flow merge, the two or three inputs to the joint path have arrows noted:*



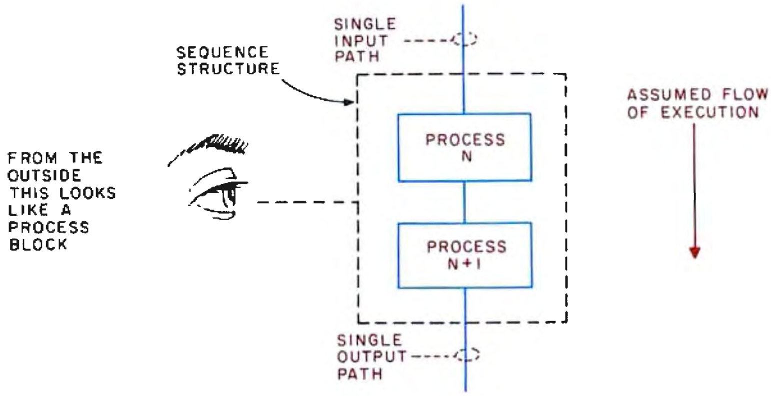


Figure 3: The sequence *structure is the simplest programming structure. It can be viewed from the outside as the equivalent of a process block, but upon close examination it is found to contain one or more process blocks.*

Basic Structures

The simplest of the program structures, shown in figure 3, is the *sequence* structure, which is composed of one or more process blocks strung together serially. Like the process block from which it is built, the *sequence* structure has only one input path and one output path. In fact, you will soon see that one of the rules that we want all structures to conform to is that they have a single input path and output path. Furthermore, an entire program, which can be represented by one large process block, should also conform to this rule.

The next structure is the *if-then-else* structure, shown in figure 4. It consists of a decision block and two process blocks. Only one of the process blocks is executed for any single pass through the structure. The result of the test or comparison represented by the decision block determines which process block is chosen. Notice that

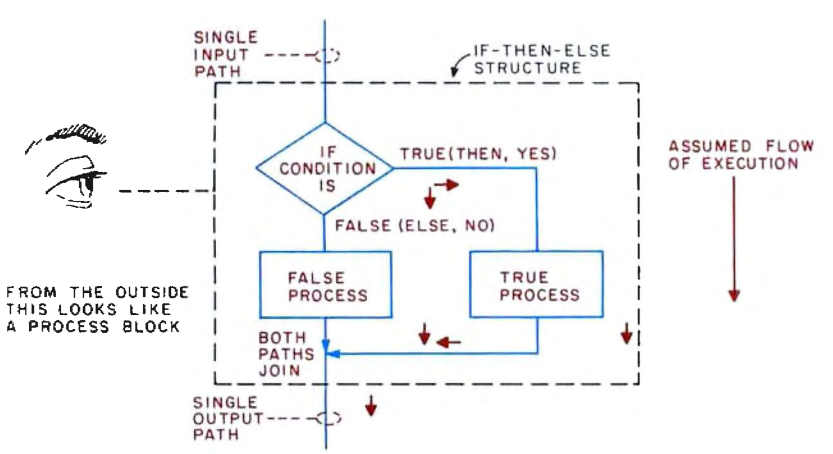


Figure 4: The if-then-else *structure is composed of a decision block and two process blocks. The process blocks may themselves be viewed as any form of structure with a single input and a single output path, and thus might in fact be* sequence *structures,* if-then-else *structures, etc.*

regardless of which path is taken there is one common exit path from the *if-then-else* structure. This is required to maintain our single exit philosophy.

An *if-then-else* structure does exactly what it says: *if* a condition is true, *then* take a specified action, *else* take a specified alternate action. However, there are times when only one action is required in only one of the paths. No action is necessary in the other path. In an actual flow diagram, this is of course shown by drawing a flow line in place of one or the other process block of the *if-then-else* structure since the most trivial process is simply going to the next process without doing anything. Note however that only one of the process blocks can be made up of this simplest case of "do nothing" since if both process blocks were eliminated from the *if-then-else* structure, the net effect would be to "do nothing" all the time whether or not the condition was true or false.

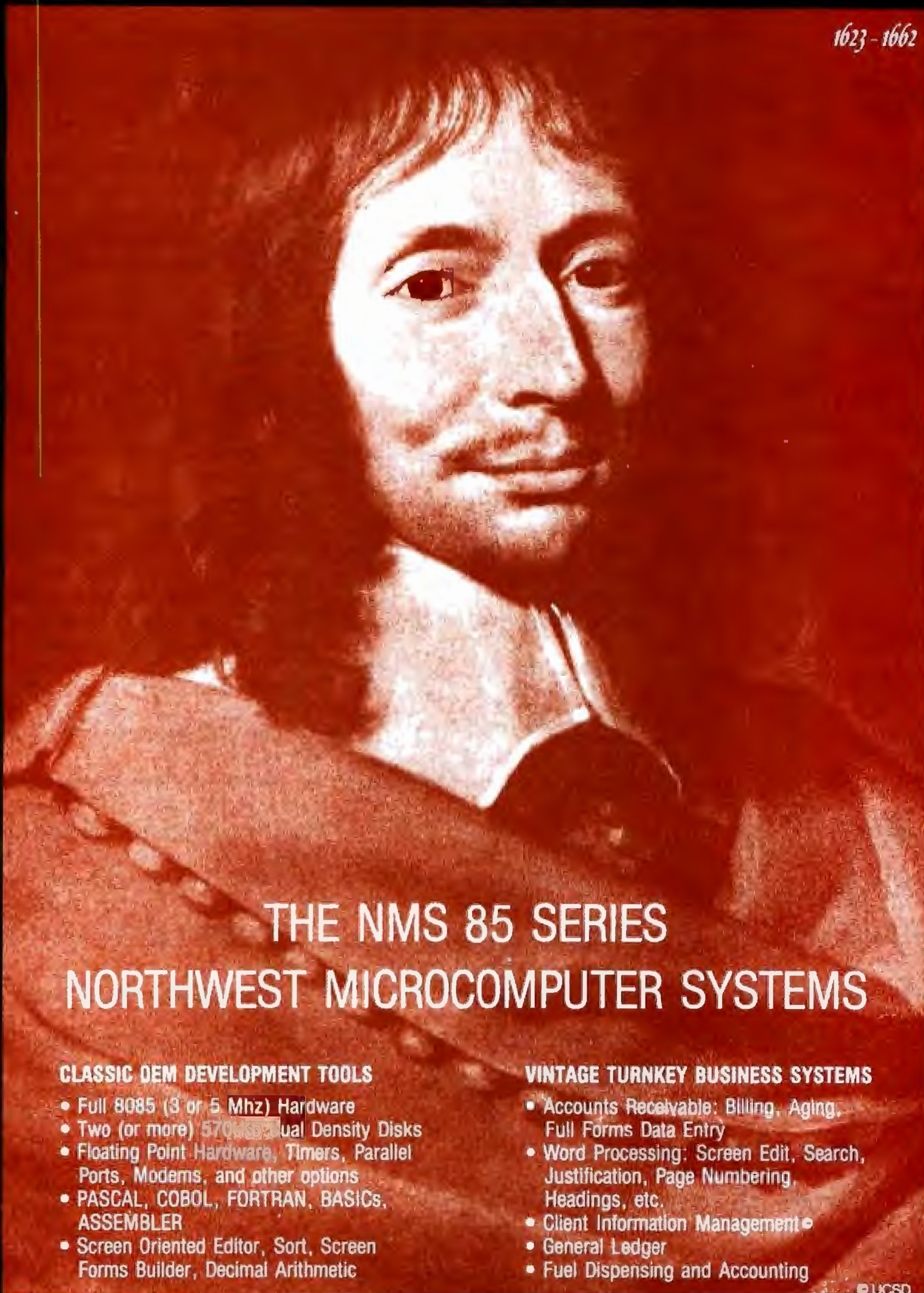
The *If* part of an *if-then-else* structure is simply any program instruction which can perform a test and take one of two paths depending upon the outcome. In an assembly language, this is usually a conditional jump or a branch instruction based upon the outcome of some comparison, arithmetic operation or other operation which affects processor status flags used in such branches and jumps. The branching instruction specifies the destination address of the beginning of one path. Whether it is the *then* or the *else* leg is arbitrarily defined, and the next sequential instruction is assumed to begin the opposite path.

Some higher level languages like BASIC have ready-made *if-then-else* instructions. BASIC has IF and THEN; ELSE is implied. The following shows how an *if-then-else* would look in BASIC:

```
1   IF X=Y THEN 10
.   .......
.   .......   } FALSE PART
.   .......
.   GOTO 15
10  .......
.   .......   } TRUE PART
.   .......
15 END
```

In this example, the *else* code immediately follows the IF instruction. The GOTO 15 ends the *else* path and causes the program to branch to the common exit point at line 15. The *then* path starts at line 10 and ends at line 15. [*BASIC is considered to be an "unstructured" language because of the need for an explicit GOTO following*

Blaise Pascal



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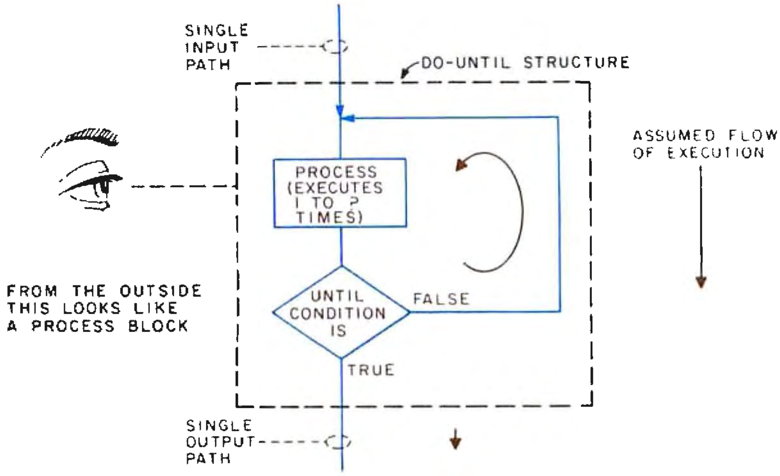

Figure 5: The do-until *structure is a looping form whose purpose is to execute a given process block at least once. After executing the process block, the "until condition" is tested and if found to be false, execution loops back to repeat the process block before testing the condition again.*

the "false part" of an IF-THEN-ELSE construction.]

If you use assembly language in your programming, and your assembler has a macroinstruction capability, then you can write your own *if-then-else* macros. It is beyond the scope of this article to describe how this is done, but it isn't very difficult.

If you use assembly language and don't have facilities for writing macros, then you can simulate the function of the macroassembler in order to gain the advantages of structured programming. Simply sit down and write yourself a set of standard *if-then-else* structures. Take the five or six most common decision types (equal, not equal, zero, greater than, etc) and write skeleton programs for each. Leave blanks for the actual condition to be tested, and leave space for the actual code which will perform the *then* and *else* functions. Later, when you need an *if-then-else* while writing a program, you can draw upon your set of prewritten structures. Not only does this eliminate your having to invent similar program sequences over and over again, but it also prevents many bugs and greatly eases the effort you have to put into program writing.

The last basic structure is the *loop*, which provides a means of repeating a sequence of instructions until some stop condition is found to exist. There are two kinds of loop structures: *do-until* and *do-while*.

A *do-until* structure, shown in figure 5, performs the function in the process block at least once. After that, a test is done to determine if the condition for stopping the process looping has been found true. As long as the condition is not true, the looping continues. When it becomes true the looping ends and the exit path is taken. This type of structure can be used, for example, when you need to search a table of values, looking for a particular value. If you know that the table will always contain a matching entry, the program routine need not be more complicated by logic to detect end-of-table before a matching value is found. Notice that the first table entry is always examined before the decision is made to continue (this is because the ending condition decision is based upon the value of that entry).

The second type of loop is the *do-while*, shown in figure 6. The difference between this and the *do-until* structure is that the test is done before the process block is executed. In many cases there is not a lot of significance to this difference because both types of structures can do the same jobs.

In specific situations you will find that one form will usually be better suited or more convenient than the other. The primary difference to remember is that the *do-until* form always executes the process block at least once whether or not the *until* condition is true, and that the *do-while* may not execute the process at all if the *while* condition is false at the time of the first test. Experience will best teach you which to use in the various situations.

A variation of the loop structures of either form might be considered, the endless loop or *do-forever*. This form of loop occurs when the *while* or *until* condition is never changed to allow execution of the output

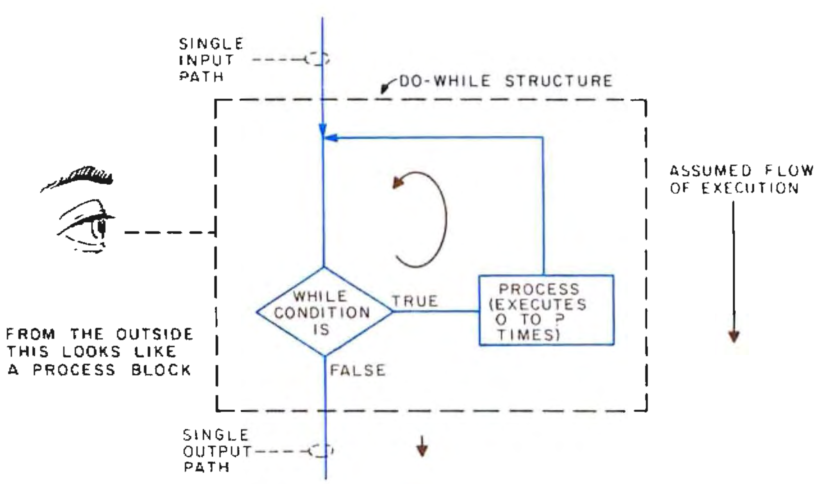

Figure 6: The do-while *structure is a looping form whose purpose is to execute a given process block only if the "while condition" is true. Thus it can execute the process block zero times if the condition is false initially, or an arbitrary number of times so long as the condition remains true during repeated execution of the process block.*

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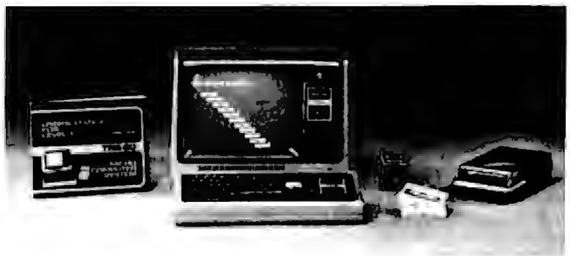

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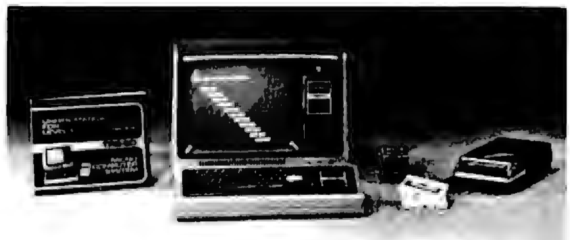

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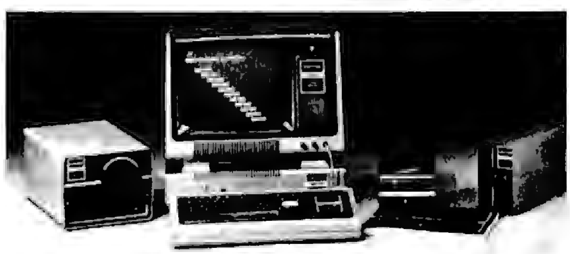

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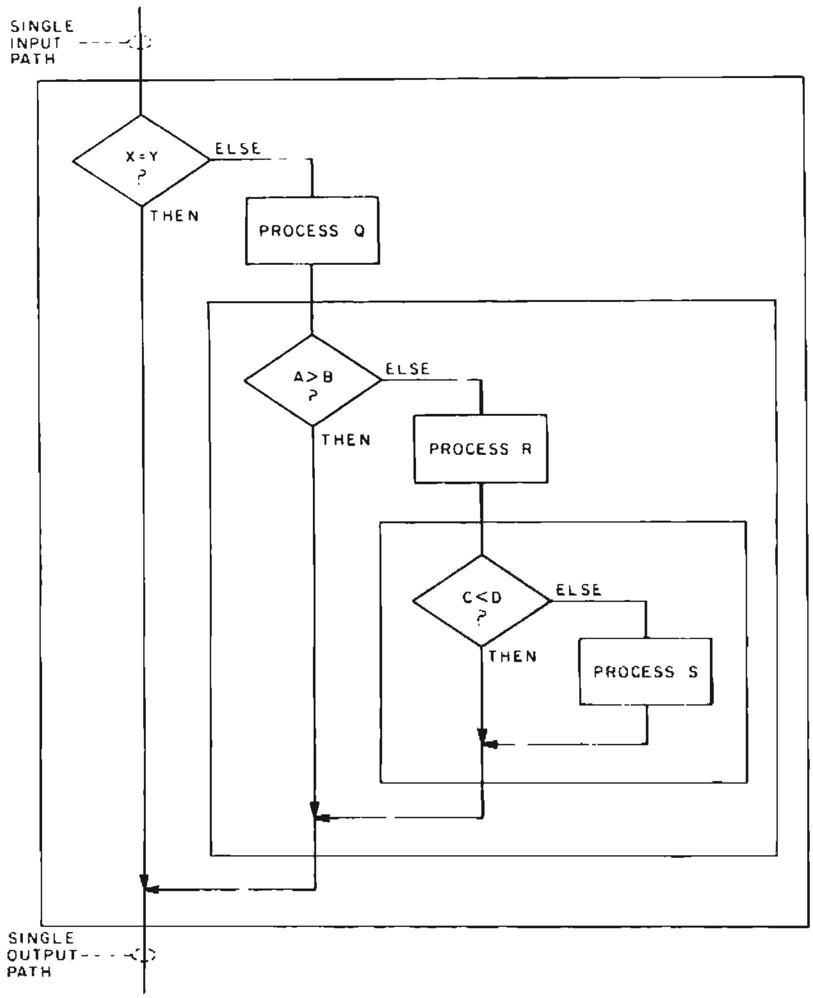

Figure 7: The various types of structures can be nested by noting that any place where a process block is indicated, a more complex structure can be used since it, too, only has one input path and one output path of execution. Thus, for example, this flowchart shows nesting of a process Q block and an if-then-else *structure as the else part of the* if-then-else *structure with condition* X=Y?. *This second* if-then-else *in turn has a third* if-then-else *as part of its else part. The colored outlines show the nesting of one structure within another.*

path of the structure. Intentional endless loops are occasionally used, as in the low level programming trick of hanging up execution in a tight loop to flag errors, or the quite legitimate endless loops which form the outer level of control of a typical executive or monitor program. But for most programming purposes, an endless loop is a bug or error in the program.

An Example

Now using the basic structures, we can construct a program of any size and complexity by combining and nesting in any manner as long as some fundamental rules are adhered to:

- The program as a process should have only one input path and one output path.
- Structures within the program can be nested but each structure must be totally contained within the structure in which it is being nested (this will be illustrated later).
- There should be no branching unless it is part of a structure (for example, the GOTOs required in languages like BASIC).
- Refrain from attempting to optimize the program by violating the above rules. There is a right time for this later.

Before we look at an example of structuring a program, let's first look at how nesting of basic structures works. Figure 7 shows a flowchart of a program which,

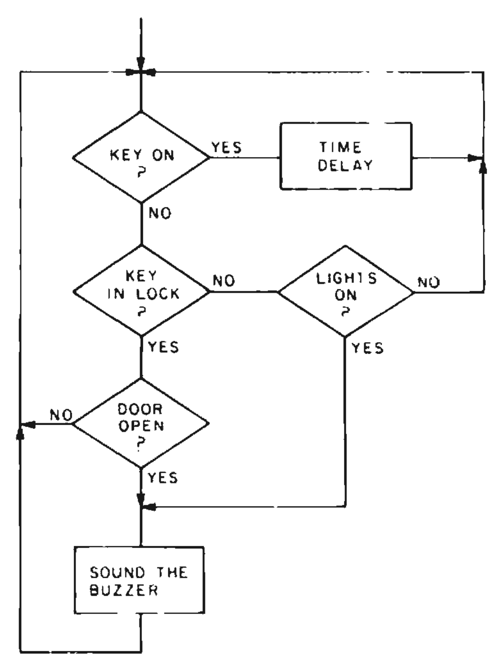

Figure 8: An unstructured flowchart performs an endless process as might be implemented in an automobile interlock. This is a complete and viable solution of the problem, but it involves numerous branching operations performed in an uncontrolled (GOTO) fashion.

overall, could be represented by a single *if-then-else*. But when it is looked at in more detail, the *else* leg contains another *if-then-else* as part of the instruction sequence there; the *else* leg of that structure contains yet another *if-then-else*. The heavy outlines show that each of the nested structures are totally enclosed by their parent structures; there is no overlap. A BASIC-like program to perform the function shown in figure 9 appears as listing 1. Again, I use outlines to illustrate that each structure is embedded in its entirety within another higher level structure. Notice that I have used indentation of lines to increase the readability of the program. Each separate structure should be at a different level of indentation than its parent.

```
1   IF X=Y THEN 32
      process Q
.
.
10    IF A>B THEN 31
        process R
.
.
20      IF C<D THEN 30
          process S
.
30      CONTINUE
31    CONTINUE
32  END
```

Listing 1: A BASIC-like program equivalent for the flowchart of figure 7. The lines in the picture emphasize the structured programming formalism.

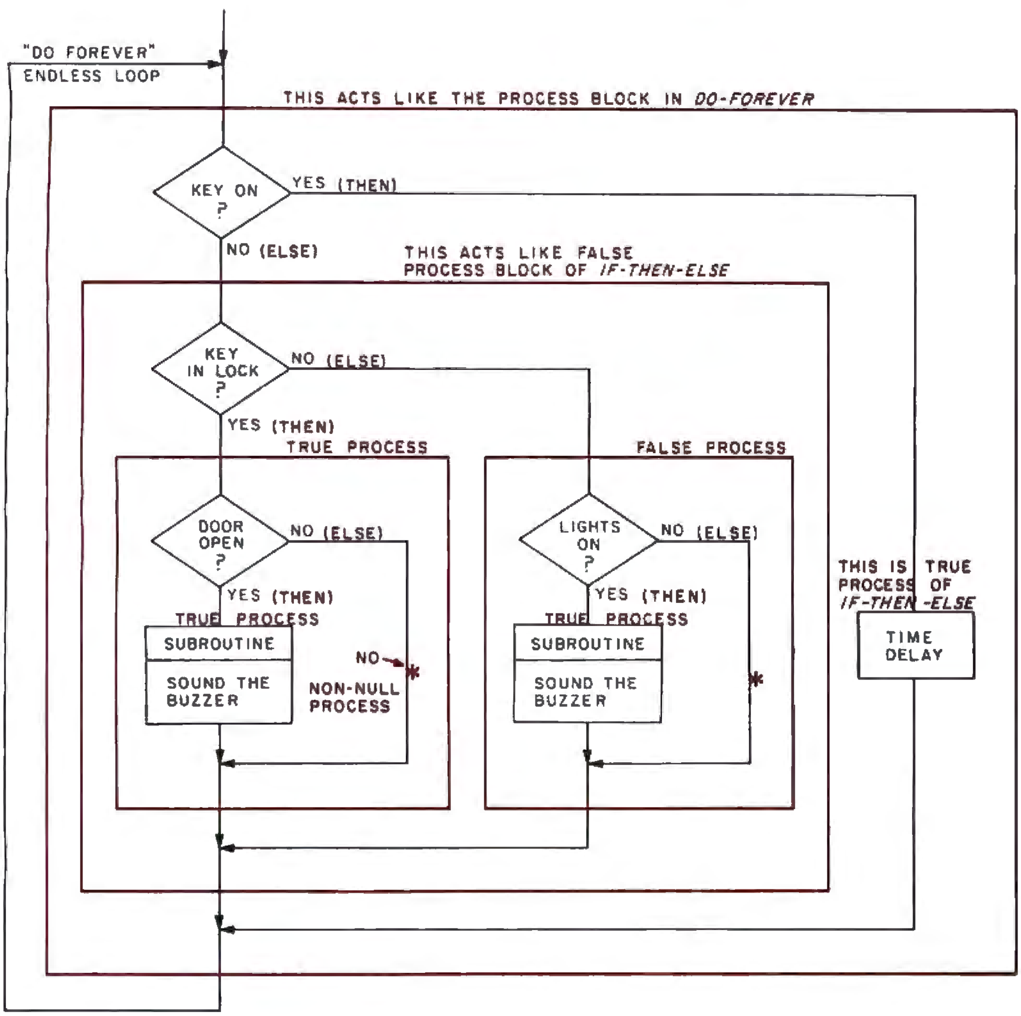

Figure 9: Taking the algorithm of figure 8 and casting it into a standardized, structured programming form eliminates all GOTO operations in languages with a complete if-then-else *structure, and in languages like BASIC, reduces use of GOTO operations to standardized structures. In this flowchart, we've positioned all the blocks to emphasize the nesting of structure. One of the primary reasons for the emphasis on structured programming is one of communications of ideas to other programmers (or the originating programmer at a later date). The claim is made that a flowchart like this one, and its equivalent representation in listing 2, provide a standardized way of communicating algorithms which makes the listing or chart easier to understand and read.*

Let's look now at an example of a simple program and show how a structured version might differ from an unstructured version.

The program is one which might be part of a future automobile computer control system using a microprocessor. Its purpose is to trigger a buzzer if the ignition key is left in the lock when the left front door is opened, or if the headlights are left on when the key is not in the lock. A delay is performed before conditions are checked again.

The flowchart in figure 8 shows how we might have drawn it without attempting to apply any of the principles of structured programming. Now, look at figure 9 which shows the structured version. Both forms of the program do the same function, but the structured form is clearly more straightforward and easier to write code from.

Basically, a number of things happened to the flowchart when it was structured. First, all the branches (or GOTOs) became forward branches except those in loop structures. This allows for reading the chart from top to bottom in an orderly way. Secondly, each decision block and process block has been put into a proper structure and nested totally within its parent structure. Thirdly, every structure regardless of its place in the overall program has only one input and one output.

One thing has happened that might appear to be a little strange to you. The sequence structure which performs the buzzer function appears twice now, where it only appeared once before. This is necessary in order to keep the structure clean. Remember, you cannot simply branch into the other buzzer block because those two structures would then overlap. The inefficiency implied by the double appearance of that block might bother you, but it will probably turn out that the block will be written as a subroutine and the only inefficiency will be an extra call instruction.

Listing 2 is a BASIC-like program for the structured flowchart. (Here "BASIC-like" means using the syntax of BASIC but allowing variable names to be many characters in length for purposes of illustrating their meaning.) I have not attempted to make the program complete and have taken some liberties in order to illustrate my points.

A few words of explanation are in order. First, the instructions at lines 3, 4 and 5 represent a *do-until* structure which is used to implement a delay by simply incrementing a counter (X) until it reaches a large value. The name BUZZ represents the line number of a subroutine (not shown) which activates an electronic buzzer in the car's dash.

Now is the time to go back and look at the program to make it more efficient in its operation or in the amount of memory required. This should be done only if it is absolutely necessary. If it is necessary, try to maintain the structuring to the extent that it doesn't destroy the clarity of the program or increase its complexity. In our example program, notice that there are three CONTINUE instructions at lines 13, 14 and 15 leading to a GOTO at line 16. The speed of the routine can be improved and the memory requirements can be reduced by eliminating the CONTINUEs and changing any instruction which references any of them to go to line 16. Alternatively, you could change each of those references to go directly to line 1 although you would be seriously interfering with the intent of structuring.

In conclusion, I invite you to try the techniques described in this article when you write your next program. If you have done it any other way before, it takes a little getting used to, but I think you will ultimately agree that it has a lot to offer. Hopefully, you will see the benefits in the form of less time spent getting your program designed, written and debugged. In short, I believe that it can help make programming even more enjoyable.■

```
1   LET X=0
2   IF KEY ≠ON THEN 7
3      LET X=X+1
4      IF X=5000 THEN 6
5         GOTO 3
6      GOTO 13
7   IF KEY=INLOCK THEN 11
8      IF LIGHT ≠ON THEN 10
9         GOSUB BUZZ
10     GOTO 13
11  IF DOOR ≠OPEN THEN 13
12     GOSUB BUZZ
13  CONTINUE
14     GOTO 1
```

Listing 2: A BASIC-like application program for activating a buzzer of an automobile given several conditions. A subroutine BUZZ is indicated (by a call with the keyword GOSUB) to actually sound a noise during the loop. In this BASIC-like representation, several liberties with syntax have been taken.

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Antique Mechanical Computers

Part 3: The Torres Chess Automaton

Dr James M Williams
58 Trumbull St
New Haven CT 06510

But now these men were suggesting that a machine could assist in or substitute for a human mental activity.

19th Century Developments

The automata of the 18th century were in fact sequence controllers possessing both digital and analog stored programs whose readouts were mechanisms that imitated human and animal actions (computers of a sort). During the next century they inspired a flood of automata, the best of which von Helmholtz described in his 1847 book, *Uber die Erhaltung der Kraft,* as being equal in achievement to the best in any other branch of science. Derek Price's book, *Automata in History,* includes material from von Helmholtz (see bibliographical notes).

In the 19th century men were starting to contemplate how mechanisms might be able to improve the human state. Charles Babbage had this notion in mind when in December 1837, precisely 99 years after Vaucanson's marvelous demonstration (see July 1978 BYTE "Antique Mechanical Computers, Part 1") he wrote the first sentence of *On the Mathematical Powers of the Calculating Engine:* "The object of the present volume is to show the degree of assistance which mathematical science is capable of receiving from mechanism." An obscure accountant of Manchester, Percy Ludgate, working without knowledge of Babbage, expressed the same thought when he wrote in 1909 the first sentence of *On a Proposed Analytical Engine:* "I propose to give in this paper a short account of the result of about six years work, undertaken by me with the object of designing machinery capable of performing calculations, however intricate or laborious, without the immediate guidance of the human intellect."

I think we may be too near to our machines to see the revolution residing in what these men said. Before Babbage and Ludgate, machines amplified or assisted or enabled the *physical* actions of humans. But now these men were suggesting that a machine could assist in or substitute for a *mental* activity of a human. Machines would enter into the realm of the human brain. It was a breathtaking idea, but not an easy one to put into effect. Babbage's two machines were never fairly begun, nor was Ludgate's. (In Babbage's case the reason was not that nineteenth century machine technology was unequal to the task, but rather because he kept changing his concepts and never produced any completed working drawings as he continuously visualized bigger and bigger machines. For him, the end was never in sight, and he left off working at a point where the machine would have been the size of a basketball court and some yards high. His son completed the "Mill" (ALU) with its printhead long after Babbage's death, in 1906. See Randell in the bibliographical notes for a photo of the Mill and a reproduction of the printout of multiples from 1 to 23 of π in 28 significant figures.)

Torres and the Incredible Chess Playing Automaton

Gifted chess players have been known to play several concurrent games, making moves without hesitation from board 1 to board *n*, then back to board 1. The best chess playing programs of today can't do that with any degree of success against most skilled players. But the remarkable fact is that in 1911 a machine was invented that automatically played a particular endgame of chess (King and Rook versus King) against a human opponent, and detected any false moves!

Leonardo Torres was the inventor, and his machine was displayed in the Mechanical Laboratory at the Sorbonne early in 1914. Photo 1, taken from a 1915 issue of the *Scientific American Supplement,* shows the

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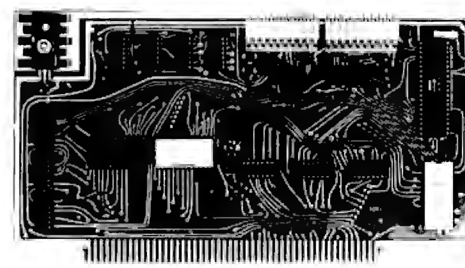

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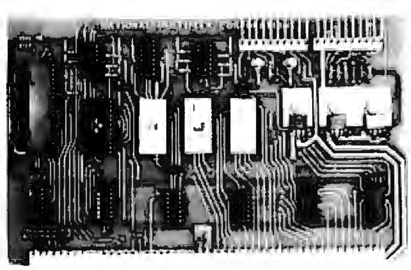

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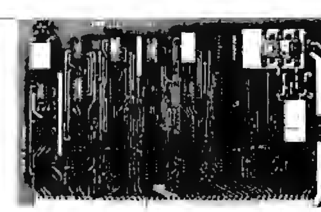

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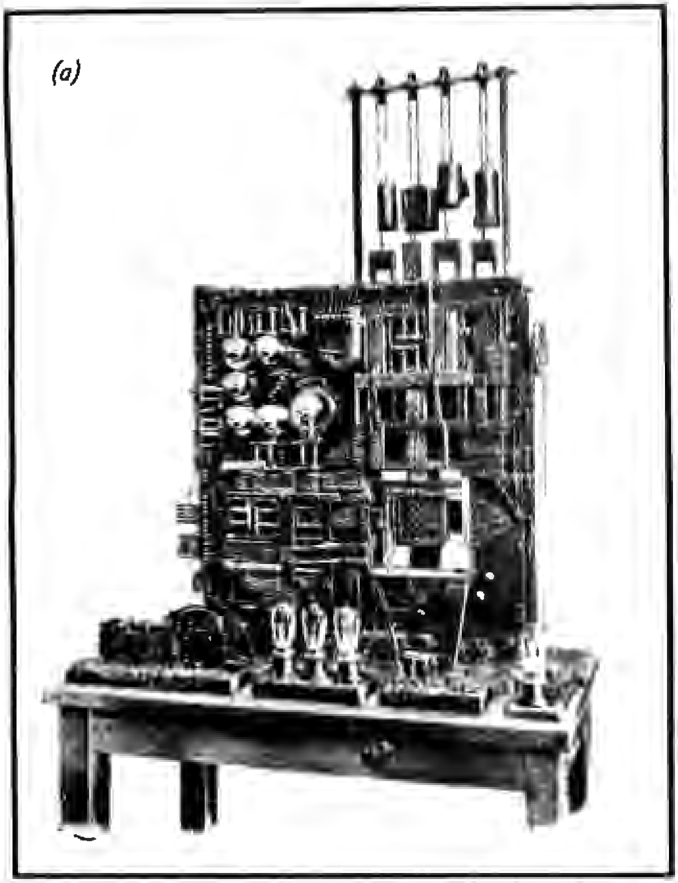

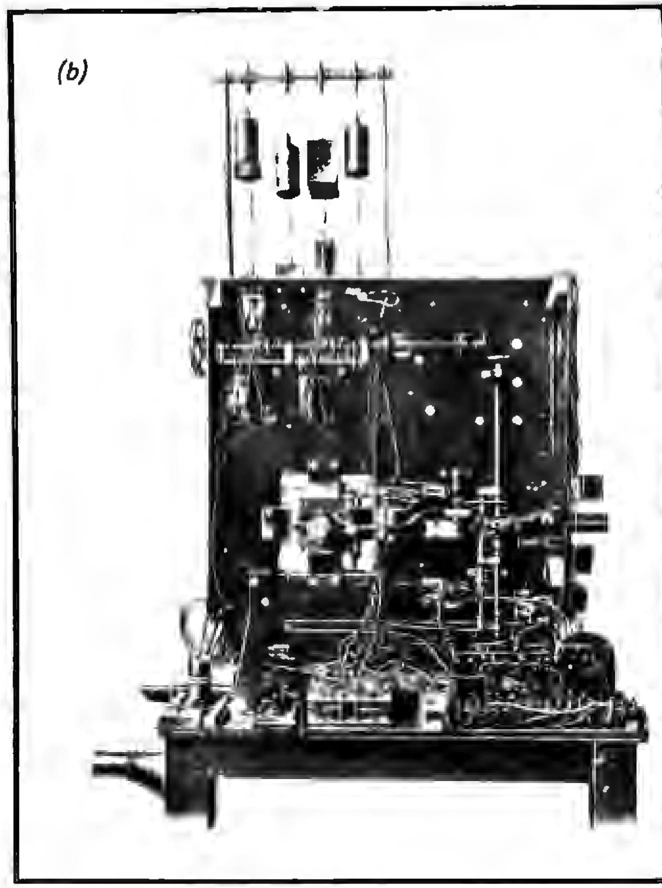

Photo 1: Front (a) and back (b) views of the 1911 chess playing automaton invented by Leonardo Torres. The unit played a particular chess endgame (King and Rook versus King) only and could force a win. The chessboard is shown in the lower right of center in photo 1a. Horizontal and vertical arms moved the pieces (which were actually electrical jacks) from square to square, and the logic circuitry consisted of battery driven relays arranged in a logical tree structure (see figure 3). Photos courtesy of Scientific American *(Supplement 80, Number 2079, November 1915).*

Torres was a true amateur who did his work because he loved it.

machine. It seems to have been powered by the array of weights atop the console, but it used electricity (almost surely from a battery) in its logic system, which consisted of commutators and intricate switchgear. Indeed, most of the face of the console is covered with relays and switches with their linkages and wiring, but one can make out the vertical chessboard, sans chess pieces, in the lower right quadrant of the face. It is about 8 to 10 inches (20 to 25 cm) wide and has holes in the center of each of the 64 squares that are really plug holes into which fitted the carved chess pieces (actually jacks on their lower ends used to make electrical contact). Sequential switches of two sorts are visible on the apron in the foreground, and the signalling lamps consist of a 3 lamp cluster in the middle with another single lamp on the right.

The machine in operation must have been an amazing sight, for its visible action was automatic. The sliding arms (poorly shown in the photo; located both above and to the left of the board) would grasp the chosen White piece, unplug it, transfer it to a new computed location, and reinsert the piece into the board. Then it waited for Black's next move. This is a degree of automation I don't recall seeing since I last gazed at a Linotype, and in 1914 it must have been an awesome spectacle. To be sure, Black always was checkmated, even with the first move, since White (the machine) had too much strength. If Black made a false move, the machine would sense it and light a signal lamp, then wait until the piece was moved to a legitimate square. Three false moves in the course of a game would "jam" the machine, which would not continue play until a reset switch was closed and pieces were properly placed. Possibly the pieces could be placed anywhere on the chessboard upon initiating a game; accounts do not make this clear. At any rate, the algorithm is quite general and directs the White King a square at a time, and the White Rook a row or column at a time inexorably toward the Black King until he is hemmed in.

In 1922 an improved version was displayed. Photographs and a description may be found in Chapuis (see bibliographical notes). This more modern machine had a horizontal chessboard grooved to accom-

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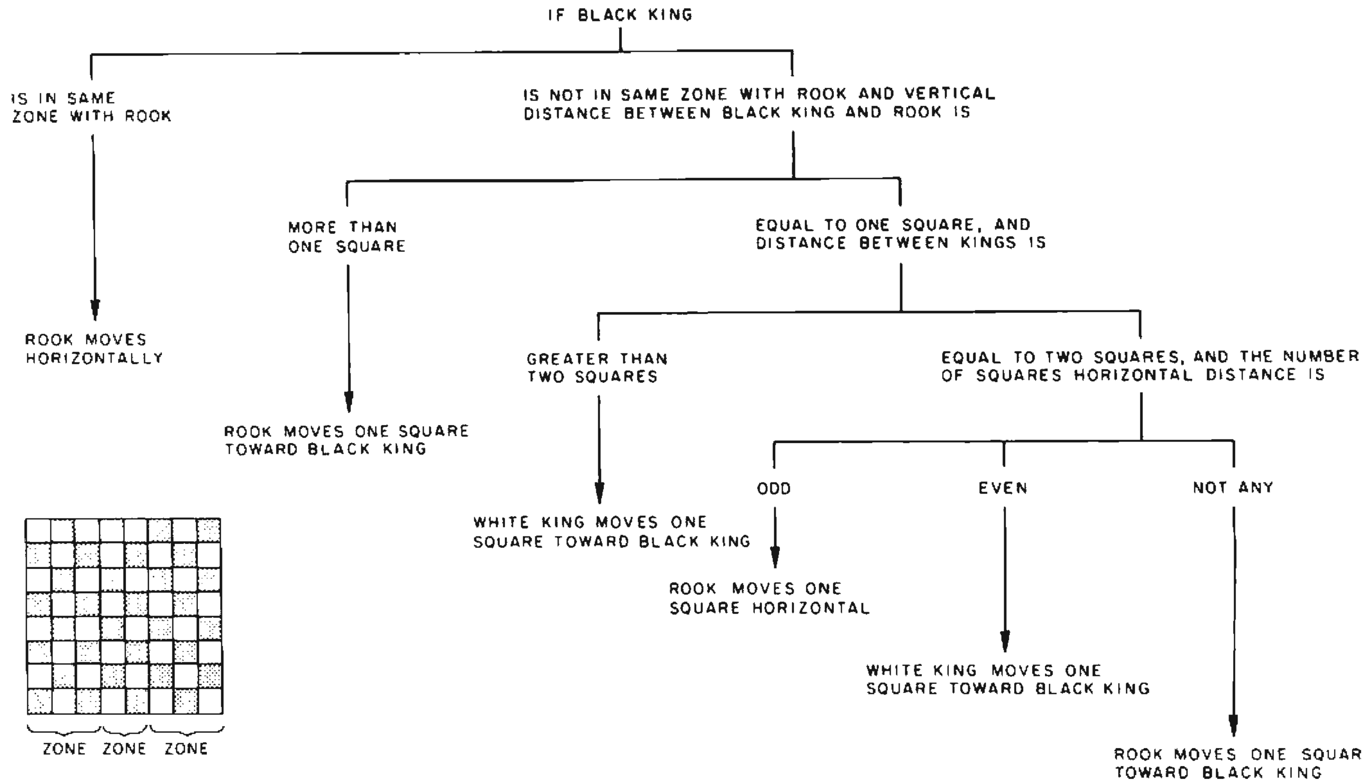

Figure 1: A chart of the algorithm used by Torres' 1911 chess endgame playing automaton.

"It is necessary that the automata imitate living actions according to their inputs, and adapt their conduct to changing circumstances."

modate wires that sensed the location of a piece, and a complex clutch and gear system within the tabletop accomplished White's moves, via magnets. It was all powered by a few small electric motors, and a phonograph record pronounced the words "echec et mat" when Black was checkmated. Figure 1 shows a chart of the action, drawn from the *Scientific American* article. *[According to David Levy in* Chess and Computers, *the Torres machine is still in good working order and can be seen in the museum at the Polytechnic Institute in Madrid SPAIN. . . .*CM*]*

Torres was one of those vital persons who ornaments the history of science: a person of intense curiosity and independent means who devotes time and energy to the exploration of arcane subjects many decades before the professionals find their way into the original excavations and mine the uncovered veins of ore left behind. He was a true amateur who did his work because he loved it; history is studded with these men: Schliemann, Humboldt, Lavoisier, Rumford, Kelvin, Babbage, Bohr, etc.

Leonardo Torres was born in 1852 in Santander on the north coast of Spain, and was trained as a civil engineer. Unfortunately I could learn only very little about his life since the biography by his son is in French and is not available to me, but a few facts emerge: he was a patriot, and a capable politician as well, who arranged for the Spanish government to liberally subsidize his "large and well-equipped mechanical laboratory at Madrid." Perhaps this is related to the fact that in 1906 in Bilbao harbor he displayed before the King a small scale radio controlled boat which "could select between various rudder positions and speeds, and cause a flag to be run up and down a mast." A lifelong Francophile, during World War I he designed a plane called the Astra-Torres for the French Air Corps. He also pursued quite mundane things: designs for aerial cablecars, apparatus to test lubricating powers of oil, a "universal pantograph" that automatically corrected any unwanted jiggles by a special linkage.

One of his first interests was mechanical analog computing devices, perhaps before 1900. He was familiar with Babbage's publications. In a paper dated 1920 he outlined an electromechanical calculating machine he exhibited in France. The machine consisted of a modified typewriter and several boxes of apparatus, connected only by a bundle of wires, all mounted on a table for display. (A picture of the machine is in Randell's book; see the bibliography.) The operator types in the numbers desired to be manipulated together with the sign of the operation to be performed, and after a few moments an = followed by the result is typed out. This is a 4 function machine that can deal with perhaps six or seven digits. This was in 1920, mind you! He revealed the

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theoretical underpinning for his calculating apparatus in general terms in 1914, in the *Essais sur l'automatique.* (In 1914, *automatique* was a new word, translatable as automation or as automatics.)

Torres' essay is so lucid and fresh that today, 64 years after publication, it still casts much illumination on the human and machine interface. After describing a first type of automaton, a machine designed to mimic the movements of a living creature, he describes a second type of automaton (Torres' own italics), "... those that imitate, not the simple gestures, but the thoughtful actions of a man, and which can sometimes replace him." He gives examples: "... the self-propelled torpedo, which *knows* how to maneuver in order to arrive at its target, the balance which weighs coins so as to *choose* the ones which are of legal weight." He speaks of the need for a "... special chapter of the theory of machines which would be called *Automatics*" and of the need to investigate "means for constructing automata endowed with a *pattern of behavior* of greater or lesser complexity." "These automata will have *sense organs*, ie: thermometers, magnetic compass, manometers, etc" together with "limbs, ie: machines or mechanisms capable of executing the operations which they are instructed to do." And they will need power sources. "Moreover, it is essential, being the chief objective of *Automatics*, that the automata be capable of *discernment*; that they can at each moment take account of the information they receive, *or even information they have received beforehand*, in controlling the required operation." *"It is necessary that the automata imitate living beings in regulating their actions according to their inputs, and adapt their conduct to changing circumstances."*

"Construction of mechanisms which play the role of sense organs is not difficult in theory."

After noting that construction of mechanisms which play the role of sense organs is not difficult in theory, and that new apparatus to achieve this measuring (sensing) function is invented every day (what cannot be measured today will be measured tomorrow or shortly), he adds that the same may be said of devices to effect the automaton's work. No one can point to a limit in the inventing of machines to perform functions. But, "It is not the same when one asks whether it is possible to construct an automaton which, in order to decide on its manner of working, *ponders* on the circumstances which surround it. The estimate is, I believe, that this may be done only in some very simple cases ... it is thought possible to automate the mechanical operations performed without thinking by a workman, but that those requiring the exercise of mental faculties will never be executed mechanically." "I shall try to show in this article, from a purely theoretical point of view, *that it is always possible to build an automaton whose actions depend on a greater or lesser number of circumstances, according to rules which one can impose arbitrarily during its construction.*" In reference to this quote, Torres described a simple digital device, but with the novelty that it displays a worked out form of conditional branching: ahead of its time, like so much of Torres' writings and work.

In his writings, Torres selected his words so carefully that it is possible to argue his distinction between "to discern," a process of input which he welcomes and illustrates as measurements; and "to ponder," a verb he seems to reserve for human thought, where more has to be taken into account than just the information of the moment or information previously received. And what is that "more"? I suggest that only people who know mechanics very well can appreciate fully the chasm between their creations and those of life (ie: between organic information and mechanical information). Randell observes, and I heartily agree, that "In all this work [Torres] was deliberately exploit-

ing the new facilities that electromechanical techniques offered and challenging accepted ideas as to the limitations of machines." But he not only exploited, he revelled; he did more than challenge: he expressed his disbelief and undertook to amaze his skeptics.

Torres worked on what he enjoyed, and a spirit of breathless, childlike fun is visible in all his activities. Imagine in 1906 a radio controlled boat that coasts up to a dock where stands the King of Spain, cuts its engine, heels sharply to starboard, and runs the royal flag smartly up and down the mast! The King salutes, the crowd cheers *¡ Viva la España!* What ecstasy it must have been for Torres. This is something beyond a demonstration of Hertzian waves as applied to potential weapons of war. It is something human: a radio controlled triumph. But such moments do not recur frequently. Torres the inventor-scientist is almost surely speaking in this quotation from the *Scientific American* article (see bibliography) about his 1911 chess player: "There is no claim that it will think or accomplish things where thought is necessary, but its inventor claims that the limits within which thought is really necessary need to be better defined, and that the automaton can do many things that are popularly classed with thought." You can hear the muted sadness, the resignation mingled with pride. Well, it still can play a flawless endgame of chess. If only it could be made to live. The next one I make will, at least, talk.

BIBLIOGRAPHICAL NOTES

1. The information in these articles has been synthesized from various sources I have encountered in reading about the history of computers, several histories of which make mention of Vaucanson in the sentence that directly precedes the one about Babbage. I found no literature explaining Vaucanson's creations until I came across:

Chapuis, Alfred E, and Droz, Edmond, *Automata: Historical and Technological Study*, Editions du Griffon, Neuchatel SWITZERLAND, 1958.

Here an astonishing and catholic variety of automated devices are described and illustrated, most of them trivial, such as pictures with clockwork-driven, moving figures. It is maddening that Chapuis' *Automata* treats the great mechanical computers of the past with little care. Chapuis and Droz were in a unique position because they read French, the language of most of the original docu-

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ments. They had pursued the field of automata so long (Chapuis & Edouard Gelis published *Le Monde des Automates* in 1928, as well as making a film about automata in 1945) that their fame on the continent would have enabled them to study the machines minutely. They meticulously reconstructed the dates of inception, untangled the inventors of automata, and deduced the fate of the machines. Their myriad illustrations are unsurpassable.

2. You can read a translation of Vaucanson's own description of his automata in:

   Ord-Home, Arthur W J G, *Clockwork Music*, Crown Publishers, New York, 1973.

   which is currently in print. This book mentions and illustrates the Eureka poetry composing machine, a violin playing device, and quotes a newspaper account of one or two astonishing automatons (unless they are fabricated) such as a life-size mannequin that plays violin sonatas under keyboard control. There is little else of interest regarding stored programs. Lots of fun, though.

3. A most valuable survey which speaks of a great many mechanisms and machines from the historical viewpoint, but describes them hardly at all is:

   Price, Derek J deSolla, *Automata in History: Origins of Mechanism and the Mechanistic Philosophy, Technology and Culture,* volume 5, number 1, 1964.

   which is worthwhile for the long perspective it offers on mechanics, and for the sense of continuity it conveys regarding human endeavor. You begin to learn that the world has always been filled with restless, thoughtful, imaginative and inventive people.

4. It is fun to read a splendidly researched volume like:

   Carroll, Charles Michael, *The Great Chess Automaton,* Dover Publications, New York, 1965.

   which is still in print and describes a nearly century long hoax (for which Vaucanson had unwittingly cleared the path), as well as Maelzel's actual mechanical achievements that blossomed into an industry by 1900.

5. For me the doyen of computer historians is:

   Randell, Brian, *The Origins of Digital Computers: Selected Papers,* Springer Verlag, Heidelberg, New York, 1973.

   where the developments that preceded and led up to the digital computer are spelled out event by event. As if Randell's crystalline commentary were not enough, he includes original papers (some in lucid translation) by Babbage, an incredibly clever man, and just about everybody who did anything useful in the development of computers, such as Aiken, Hopper (the only woman in the book), Eckert, Von Neumann, Goldstine, and Mauchly. They are included here, along with Leonardo Torres. Many machines are also included, such as the Zuse relay computer of wartime Germany, the Bell Labs relay computer, Altanasoff's Iowa State computer with its novel capacitor storage system, and of course, ENIAC and EDSAC, those feeble giants.

6. The following article makes fascinating reading:

   Anonymous, "Torres and His Remarkable Automatic Devices (He Would Substitute Machinery for the Human Mind.)", *Scientific American Supplement 80,* number 2079, 6 November 1915.

7. Torres' machine is also described in:

   Levy, David, *Chess and Computers,* Computer Sciences Press, Potomac MD, 1976.■

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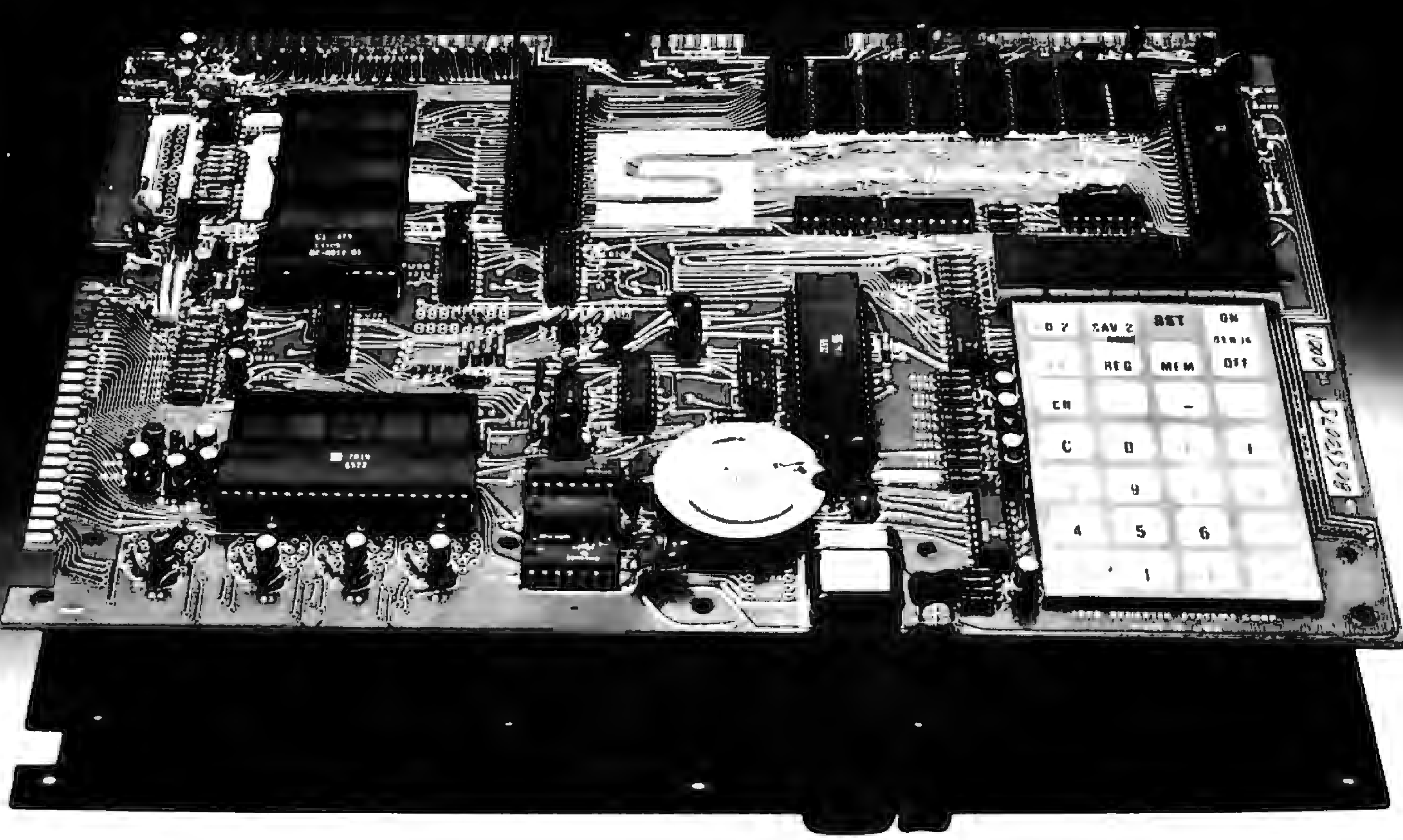

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I would like to thank Dr Russell Reiss for contributing ideas which have led to this and other articles. . . .SC

In "Let Your Fingers Do the Talking – Add a Noncontact Touch Scanner to Your Video Display" (August 1978 BYTE, page 156), I detailed the hardware design of a noncontact touch scanner which sits over a conventional video screen. This system, though lower in resolution, allows a fingertip to simulate the function of a light pen and with proper programming can become as important a peripheral as the common ASCII keyboard.

Quick Hardware Review

The scanner consists of 32 pairs of infrared light emitting diode transmitters and photo transistor receivers arranged around the perimeter of a picture frame. There are 16 pairs on the X axis and 16 pairs on the Y axis. The hardware logic sequentially activates the 32 pairs, first in the X direction (horizontal) then in the Y direction (vertical). If a physical obstruction is placed in the plane of the scan, one X and one Y beam are interrupted. The corresponding X and Y beam addresses are stored when this happens. Since there are 16 pairs per axis, each coordinate can be represented by a 4 bit code and both the X and Y addresses can be packed into one data byte.

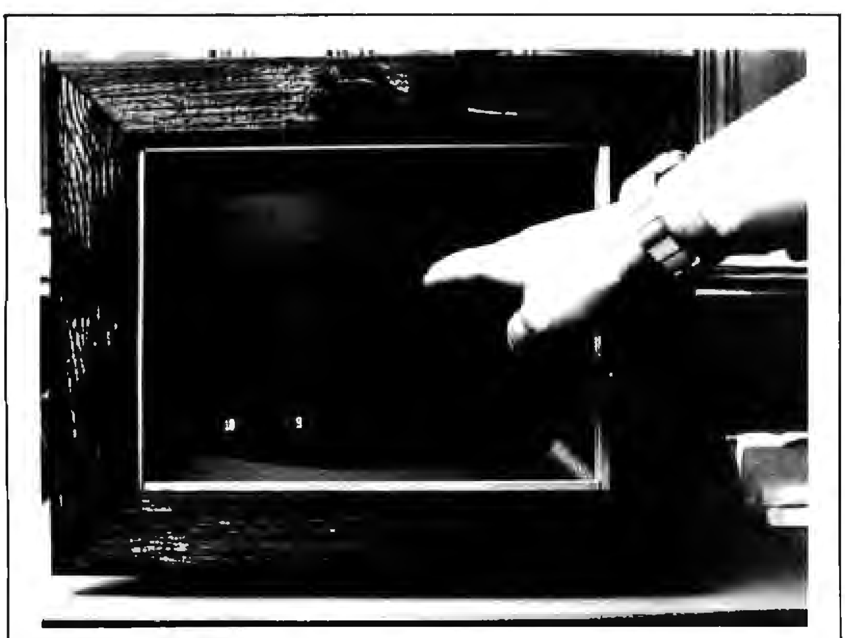

Photo 1: The basic information returned from the touch panel is a coordinate pair for one of 256 possible finger sized locations on the video display's face. Here, using the program in listing 3, the displayed coordinates 10 and 9 correspond to the point just touched on the screen.

The end result of the hardware logic is a very simple scanner to computer interface. The scanner output is one 8 bit byte containing the 4 bit X and 4 bit Y addresses. The only other signals are a little something often referred to as hand shaking. A data ready line is set to a high level output when the scanner has sensed an obstruction.

This data ready signal can be tied to a parallel input port and scanned as I have done, used as a control line on a peripheral interface circuit, or used directly to generate a processor interrupt. If the touch panel is to be exercised in BASIC, the first method will prove to be easiest. The latter method, normally used with a machine language program rather than BASIC, will be the most efficient from a memory utilization standpoint.

I continue to use BASIC wherever the interface data processing speed allows it. In this way I can write illustrative program examples which are not tied to a particular processor. Of course, the speed advantages of machine language may be useful if your programs using the touch panel have a lot to do; so feel free to strike out on your own using these BASIC programs as a model.

Whatever the software method utilized to recognize the data ready bit, the program action must be the same. After the data ready bit goes high, the data byte is stored and the data ready is reset by momentarily pulsing the ready reset line low. In BASIC, the easiest way to do this is to tie the ready reset line to one bit on a parallel output port (it need only be a strobe rather than a latched output) and then sequentially execute two OUT instructions. The 10 ms pulsewidth I get on my machine is the result of the time it takes for BASIC to respond. The program examples presented in the listings use the following port allocations (in decimal):

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Data Ready	–	Input Port 2 (least significant bit)
Ready Reset	–	Output Port 16 (least significant bit)
X, Y Coordinate		Input Port 16 (b_7-b_4 is X address) (b_3-b_0 is Y address).

```
100 REM THIS IS THE ONLY SOFTWARE NECESSARY TO EXERCISE THE
    SCANNER
110 REM *** RESET SCANNER ***
120 OUT 16,0 : OUT 16,255 : REM THIS WILL GIVE A SHORT RESET PULSE TO
    PORT 16
130 REM *** TEST DATA READY ***
140 T=INP(2) : REM THE DATA READY SIGNAL IS BIT 0 OF PORT 2
150 T=T AND 1 :REM MASK ALL BUT BIT 0
160 IF T<>1 THEN GOTO 140 :REM TEST TO SEE IF DATA READY IS SET
170 REM *** READ DATA ***
180 D=INP (16) :REM SCANNER IS ATTACHED TO PORT 16
190 D1=(D AND 240)/16 :REM MASK AND SHIFT RIGHT 4 BITS
195 REM D1 IS THE X COORDINATE
200 D2=D AND 15
205 REM D2 IS THE Y COORDINATE
210 RETURN :REM RETURN IS ONLY NECESSARY IF CALLED AS A
    SUBROUTINE
```

Listing 1: Subroutine used to determine activated coordinates on the scanner.

```
10  PRINT "MY SCREEN ITCHES!! PLEASE SCRATCH IT!"
20  GOSUB 100 :REM ACTIVATE SCANNER
30  PRINT "OH!! THAT FEELS SO GOOOOOOOD!!!"
40  END
```

Listing 2: Example of using the entire video screen as a push button.

```
100 S=USR(255) :REM THIS IS A SCREEN CLEAR FOR DG Z-80
110 PRINT"THIS IS A TEST OF TOUCH INPUT"
120 PRINT"THE SCREEN IS CURRENTLY BEING SCANNED BY AN ARRAY"
130 PRINT"     INFRARED LEDS AND OPTICAL SENSORS"
140 PRINT
150 PRINT"POINT AT THE SCREEN SOMEPLACE "
160 GOSUB 1000 :REM GOTO THE SCANNER SUBROUTINE AND RETURN WITH COORDINATES
170 PRINT"                    THANKYOU"
180 PRINT
190 PRINT
200 PRINT"THE SCANNER HARDWARE SAYS THAT YOU TOUCHED LOCATION"
210 PRINT"          X=";D1;"AND  Y=";D2;"      ON A 16X16 GRID"
220 GOSUB 2500 :REM CALL SLIGHT DELAY TIMER
250 S=USR(255) :REM CLEAR SCREEN
260 PRINT"LET ME DEMONSTRATE THE COORDINATE SYSTEM"
270 PRINT"POINT YOUR FINGER AT THE SCREEN AND I'LL PRINT OUT (X,Y)"
280 PRINT"TO EXIT JUST POINT TO LOCATION (15,15) ---UPPER RIGHT"
290 GOSUB 1000 :REM CALL SCANNER
300 S=USR(255) :REM CLEAR SCREEN
310 IF D1=15 THEN 320 ELSE 330
320 IF D2=15 THEN END
330 PRINT
340 PRINT D1,D2; :REM PRINT COORDINATES
350 GOTO 290
1000 REM *** RESET SCANNER ***
1010 OUT 16,0 :OUT 16,255
1050 REM *** TEST DATA READY ***
1060 T=INP(2)
1070 T=T AND 1
1080 IF T<>1 THEN GOTO 1060
1090 REM *** READ DATA ***
1100 D=INP(16)
1110 D1=(D AND 240)/16 :REM THIS IS THE X VALUE
1120 D2=D AND 15 :REM THIS IS THE Y VALUE
1130 RETURN
2500 FOR W=1 TO 2000
2510 NEXT W
2520 RETURN
```

Listing 3: This program outputs the coordinates of the point you are touching on the screen. The output of the program can be used at a higher level to indicate some object that is printed on the screen.

Using the Touch Panel

Using the touch panel in any BASIC program, whether it be game or instructional, will necessitate having a subroutine to read and reset the scanner placed somewhere within the BASIC program. The total software necessary to exercise the touch panel is shown in listing 1.

If a GOSUB 100 command is encountered, BASIC vectors to this subroutine and begins execution. This subroutine will not return until someone touches the screen. Variable D1 would contain the X coordinate and D2 would contain the Y value. Each call to this subroutine results in returning to the main program with the X, Y address of a single touched point. To obtain ten touch inputs would require calling this routine ten times.

The simplest program utilizing the scanner would be one which sensitizes the entire screen to act as one giant push button. Such a program is similar to a press any key option on a keyboard.

The program in listing 2 prints "MY SCREEN ITCHES!! PLEASE SCRATCH IT!" on the video screen, waits for someone to touch any place on the screen and then responds with the message in line 30. Notice that we did not use the coordinate information from the scanner because we only needed to take advantage of the fact that the subroutine returns only if data is *ready*.

Test the Coordinate System

If one builds the touch panel, the first program written should be one that illustrates the coordinate system dynamically, such as the program in listing 3. (All BASIC programs in this article are written in Micro Com 8 K Zapple BASIC.)

After printing an opening comment on the video screen, the program calls the scanner subroutine as before. This time when it returns, it prints out the X and Y coordinate which was touched as shown in photo 1. The rest of the program is a repeat of this basic cycle with one exception. The values of D1 and D2 are both compared to 15 after each scan. Should you point at coordinate position (15,15) the program ends.

Converting Position to Function

So far we have displayed only the raw output of the scanner and have not used it in its true application. Telling you that you are pointing to location (4,2) illustrates that the touch panel functions, but does no use-

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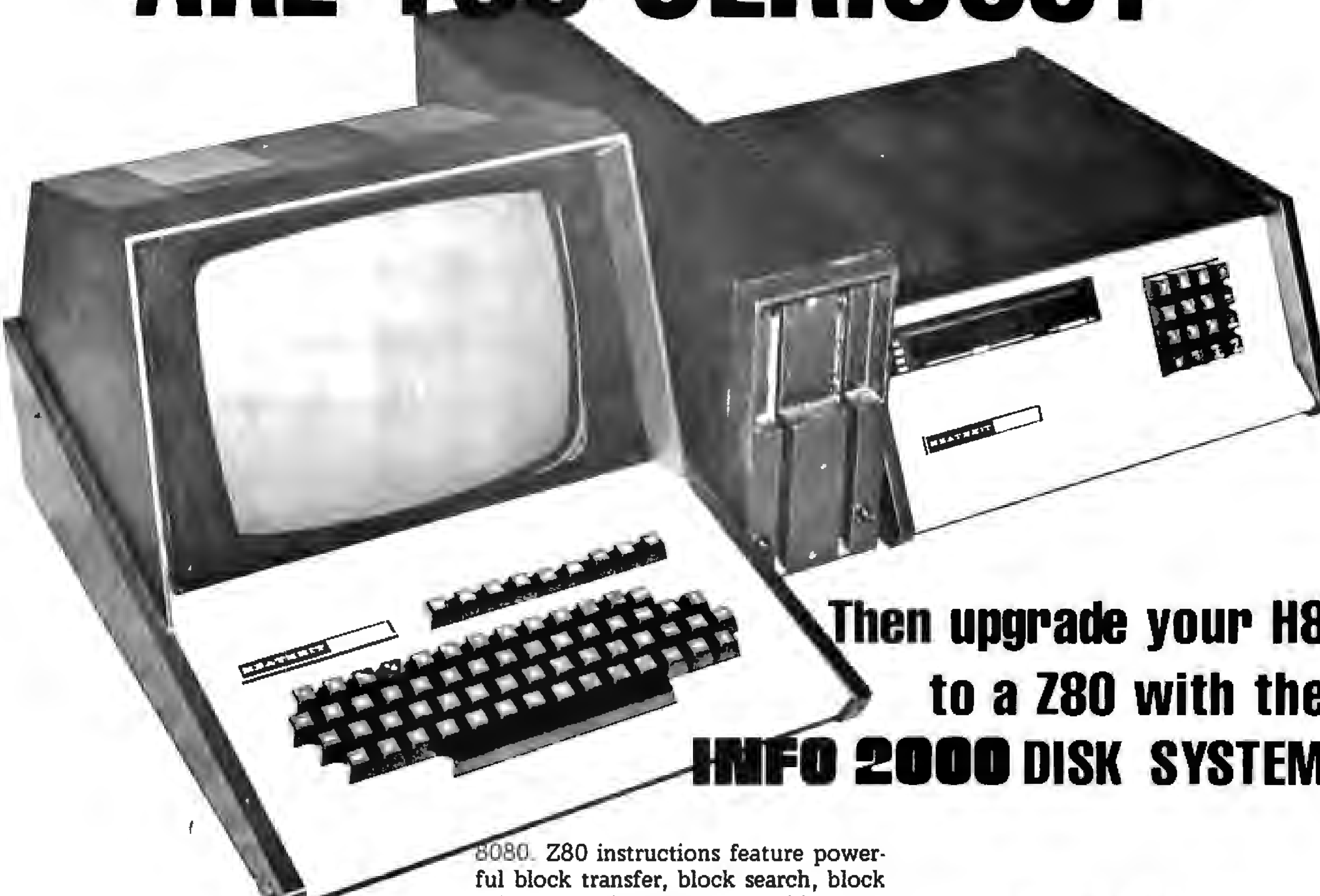

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Photo 2: Here is a picture of an experiment which was backed up by a fairly long BASIC program: using the screen as the input device for a simulation of an ordinary 4 function calculator. The imagination of the user, to use a well-worn cliche, is the only limitation upon trying experiments with special purpose keyboards and interactive sequences on the screen. Use of the video display behind the touch panel area makes easily altered software the determining factor — rather than physical tools in the workshop.

```
100 S=USR(255)
110 PRINT'NAME                                     ADDRESS'
120 FOR L=1 TO 12
130 PRINT
140 NEXT L
150 PRINT'PHONE                             VITAL CHARACTERISTIC'
160 GOSUB 1000
170 IF D1 7 THEN GOTO 300 ELSE GOTO 200
200 REM THIS ROUTINE DECIDES IF YOU ARE POINTING TO
202 REM SECTOR 1 OR 2
210 IF D2.7 THEN PRINT'UNLISTED NUMBER' :GOTO 2000
220 PRINT'BRENDA (THE LITTLE WOOFER) CIARCIA'
230 GOTO 2000
300 REM THIS ROUTINE DECIDES IF YOU ARE POINTING TO
302 REM SECTOR 3 OR 4
310 IF D2 7 THEN PRINT'SCOTTISH TERRIER -- FOUR LEGGED BURGLAR ALARM' :GOTO 2000
320 PRINT'BOX 582   GLASTONBURY,CONN. 06033'
330 GOTO 2000
990 REM
992 REM SCANNER SUBROUTINE
1000 OUT 16,0 :OUT 16,255
1010 T=INP(2)
1020 T=T AND 1
1030 IF T<>1 THEN GOTO 1010
1040 D=INP(16)
1050 D1=(D AND 240)/16
1060 D2=D AND 15
1070 RETURN
2000 FOR N=1 TO 2000
2010 NEXT N
2020 GOTO 100
```

Listing 4: Illustration of a BASIC program which divides the screen into four sectors and performs a function dependent on which sector is touched by the user.

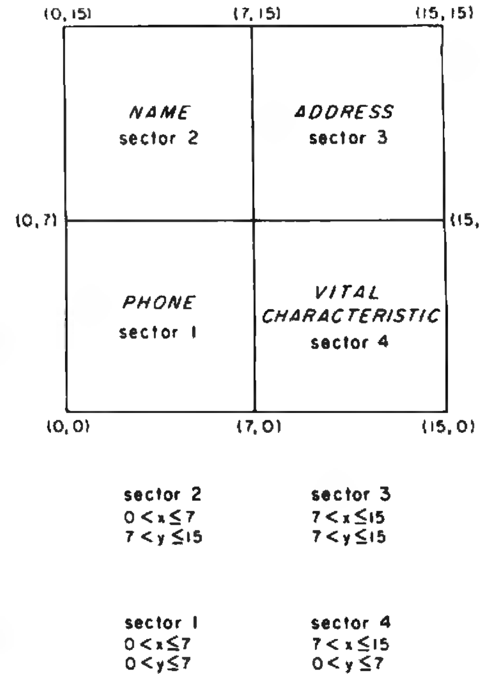

Figure 1: Physical arrangement of sectors on the screen as used by program in listing 4.

ful work. If instead some letter or word were at (4,2) and the program used this higher function output rather than just the numerical coordinate, we'd have something.

Fortunately it isn't all that difficult. By dividing the scanner system into fields and having each field represent a function, we can do useful work. A 2 level program must be written. First, it should have the capability of formatting the screen so that the printing is beneath the proper touch coordinate. Then, after returning from the scanner subroutine, it must translate this position value into the function designated by the printing on the screen.

A simple program which divides the screen into four fields or sectors and performs a function dependent on which sector is touched is shown in listing 4. Figure 1 describes the mathematical relationship between the coordinate system and the BASIC program of listing 4.

After printing the opening lines on the screen the program calls for the data from the scanner. The X coordinate (D1) is first tested to see if it is greater than 7. If it is, then either sector 3 or 4 must have been chosen. If D1 is less than 7 then it must be sector 1 or 2. After choosing whether it is the right or left half of the screen the test is repeated with the Y coordinate. In theory, this binary search method would require no more than eight such tests if all 256 points were designated as separate fields.

A further extension of this binary search

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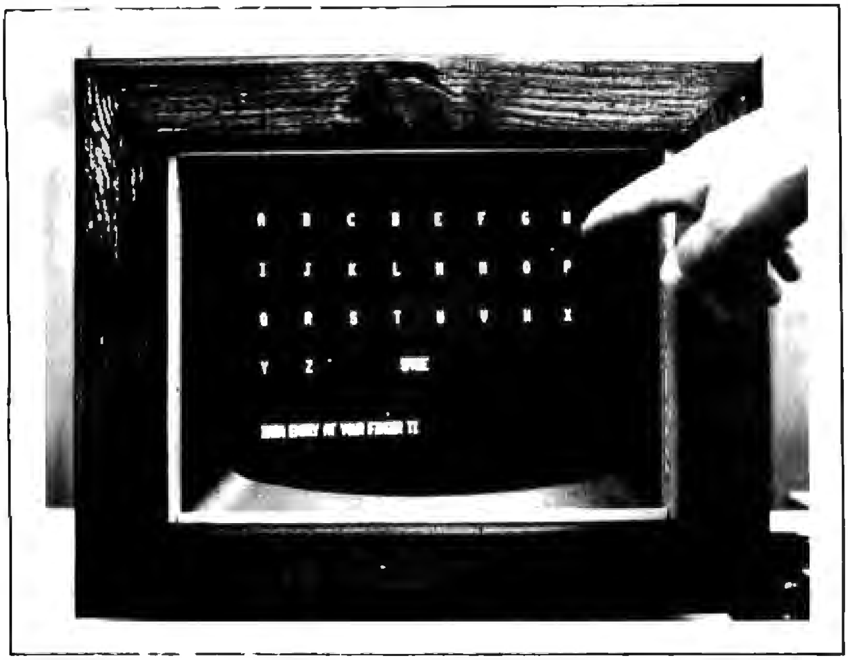


Photo 3: Touch panel input using the program of listing 5. The line of text at the bottom of the display was entered by touching the index finger to each letter in turn. The photo is shown with the letter P about to be pressed.

```
100 REM THIS PROGRAM DISPLAYS A KEYBOARD ON THE CRT SCREEN
110 REM AND ILLUSTRATES DATA ENTRY WITHOUT A PHYSICAL KEYBOARD
120 REM JUST POINT AT THE LETTERS AND IT WILL 'TYPE' YOUR MESSAGE
200 PRINT"A        B        C        D        E        F        G        H"
210 PRINT
215 PRINT
220 PRINT"I        J        K        L        M        N        O        P"
230 PRINT
235 PRINT
240 PRINT"Q        R        S        T        U        V        W        X"
250 PRINT
255 PRINT
260 PRINT"Y        Z                 SPACE"
261 PRINT
262 PRINT
263 PRINT
264 PRINT
265 GOSUB 2500
268 GOSUB 1000
270 IF D2>=12 THEN PRINT CHR$(D1/2+65);:GOTO 265
280 IF D2>=10 THEN PRINT CHR$(D1/2+73);:GOTO 265
290 IF D2>=8  THEN PRINT CHR$(D1/2+81);:GOTO 265
300 IF D2>=5  THEN 302 ELSE 310
302 IF (D1/2+89)>91 THEN PRINT CHR$(32);:GOTO 265
303 PRINT CHR$(D1/2+89);:GOTO 265
310 IF D2=0 THEN GOTO 320 ELSE 330
320 IF D1=15 THEN 330 ELSE GOTO 265
330 S=USR(255) :REM CLEAR SCREEN
340 PRINT"TO RETRY EXERCISE----TOUCH SCREEN"
350 GOSUB 1000
360 GOTO 200
1000 OUT 16,0 :OUT 16,255 :REM LINES 1000-1070 READ THE SCANNER DATA
1010 T=INP(2)
1020 T=T AND 1
1030 IF T<>1 THEN GOTO 1010
1040 D=INP(16)
1050 D1=(D AND 240)/16
1060 D2=D AND 15
1070 RETURN
2500 FOR A=0 TO 500 :REM THIS IS A SHORT DELAY
2510 NEXT A
2520 RETURN
```

Listing 5: Keyboard simulation program.

```
100 REM THIS IS A SIMPLE PROGRAM TO ILLUSTRATE SIMULTANEOUS
110 REM DATA INPUT FROM EITHER THE TOUCH PANEL OR THE KEYBOARD
120 Q=INP(0) :REM KEYBOARD IS ATTACHED TO PORT 0
130 REM MSB IS KEYBOARD STROBE  --- BITS 0 TO 6 ARE 7 BIT ASCII
140 IF Q>0 THEN GOTO 220 :REM CHECK KEYBOARD STROBE
150 T=INP(2) :REM SCANNER DATA READY IS PORT 2 LSB
160 T=T AND 1
170 IF T<>1 THEN GOTO 120
180 D=INP(16) :D1=(D AND 240)/16 :D2=D AND 15 :REM READ SCANNER COORDINATE
190 PRINT"PANEL TOUCHED AT LOCATION ("D1;D2")"
200 GOSUB 240
210 GOTO 120
220 PRINT"KEYBOARD KEY ";CHR$(INP(0));" PRESSED"
230 GOTO 120
240 OUT 16,0 :OUT 16,255 :REM RESET SCANNER HARDWARE
250 RETURN
```

Listing 6: Method for scanning two input devices simultaneously on a Digital Group Z-80 system.

concept is used in the calculator of photo 2. While never meant to replace the hand held calculator it uses a routine similar to the previous example to determine the action of each of the 16 possible entries. The picture is included to present the reader with one of the many possible applications of the scanner. The program, however, is quite long and difficult to explain in an introductory article such as this.

Simulated Keyboard

One use of the touch panel would be the simulation of direct keyboard entry. Obviously this technique is valuable only where limited data entry is required. Large menu selection programs with numerous choices displayed may not always have the particular item of interest. By having one of the available selections be a keyboard display and entry routine such as photo 3 and listing 5, the miscellaneous entry could be accommodated. The program of listing 5 displays a keyboard on the video screen and allows one to *type* by pointing to the individual characters. The example does not include punctuation and a carriage return, but they could be easily accommodated.

One final note. Using the touch panel need not eliminate the standard ASCII keyboard as an input device. By using the BASIC INPUT command, keyboard entry is still available to the user as is the scanner through a callable subroutine. A program could be written where some entries come from the touch panel and others from the keyboard. A more versatile program would allow input from either device at any time.

Listing 6 is a simple program which demonstrates how BASIC can scan two input devices simultaneously and provide appropriate response.

I hope that this touch panel design will spark the creative interests of other computer enthusiasts. In a field where technology advances by leaps and bounds and product obsolescence can be described in months, innovative ideas are necessary to extend the concept of creative home computing. By adding advanced peripherals and high level languages, system obsolescence is delayed considerably.

Next month: build a 5 W dual voltage DC to DC converter for your interfaces.■

Technical Forum

About the Author

Jon Bondy has been involved with computers for over ten years, and is currently employed by General Electric's Space Division as a computer systems engineer. He has had experience with a wide variety of computer systems and languages. His chief interests are instruction set design and computer architecture in general, including an enthusiasm for that class of high level language oriented stack machines inspired by the Burroughs "D" machine. He gives lectures occasionally for and is vice president of the Philadelphia Area Computer Society.

S2L: An Altair (S-100) to LSI-11 Bus Adaptor

Jonathan Bondy
Box 148
Ardmore PA 19003

For many months, those of us who admire the architecture of the PDP-11 computers have been looking for a way to adapt the wealth of Altair (S-100) bus products to this processor. The introduction of the Heath H11 (LSI-11 based) processor has further emphasized the need to solve the problems which have thus far made the LSI-11 incompatible with the Altair (S-100) bus peripherals. This article describes the problems which exist, and one solution which I see for them. It has been written in advance of actually implementing the solution, but it should prove valuable to all those experimenters who wish to take up the challenge of an LSI-11 to Altair bus adapter.

For years, the only problem with the LSI-11 as a personal computer has been price. The processor board (KD11-F) itself is a rather good deal at a discount level of 20 to 30 percent, but the accessories are somewhat expensive compared with typical personal computing products as seen in table 1.

Most of the extra expense of the LSI-11 systems can be attributed to three factors:

1. The DEC prices are generally higher. The memory prices demonstrate this.
2. The use of highly regulated power supplies with the DEC products results in a more costly power supply. In addition, few experimenters are likely to homebrew such a power supply due to its complexity and its being the single element which could cause major destruction should it fail.
3. The LSI-11 has no front panel switches, and instead requires the user to examine and modify the state of the machine via a serial console device. While most industrial customers of DEC are able to afford the high cost of a serial terminal, many

Table 1: Price comparisons of Industrial quality Digital Equipment Corporation LSI-11 modules and systems with functionally similar modules for the Altair (S-100) bus.

Component	Typical Hobby Price (S-100 Products)	Typical DEC/MDB/ RDA Price	Comments
Memory	$500 for 16 K bytes	$900 for 16 K bytes	
Serial IO	$100	$230	Required
Parallel	$100	$200	
Video display memory	$200	$600	
Power supply	$100	$400 to $1000	
Backplane	$150	$350	
Chassis	$200	$350	
Prototyping card	$25	$75 to $150	Two sizes

These prices were effective at the time of the article's writing. Current prices differ markedly. . .CH hobbyists have discovered that memory mapped video is both cheaper and faster than a serial device. Because of this, DEC's decision to use the serial interface in this fashion forces a user to either support two terminals (one serial and one memory mapped) or make do with the serial device. It is unfortunate that a serial device, at any reasonable data rate, is simply unacceptable for some of the applications which an experimenter might wish to pursue, one example of which is state of the art word processing applications.

The three conflicting forces of the high prices of the LSI-11 systems, the desire for that processor's architecture, and the problems with the serial terminal requirement have kept me from going ahead with an LSI-11 system for well over a year. I have finally started on a project of my own which is to adapt an LSI-11 to Altair (S-100) bus peripherals and memory.

My idea was that, since the widest variety of reasonably priced peripherals are available on the Altair (S-100) bus, I should build an Altair (S-100) to LSI-11 bus adaptor (S2L). In order to start the design of an Altair bus adaptor, a number of decisions had to be made. Initially, I decided that splitting the 16 bit LSI-11 bus (also known as the "Q" bus) into two 8 bit Altair (S-100) buses, one for the even bytes and one for the odd bytes, would create too much havoc. Certainly one could purchase pairs of memory boards and allocate them in the memory address space appropriately, but when dealing with devices such as memory mapped video displays, adjacent bytes on the screen would be every other byte in the address space of the LSI-11. Additionally, two of every card would be needed in most cases, and adjacent memory mapped IO ports (the only type being considered in the case of the PDP-11 architecture) would be on alternate cards. For this reason, I felt that only one Altair (S-100) bus should be connected to the bus adaptor. This implied that multiple byte reads and writes would have to be performed by the bus adaptor and some sort of state machine would have to be built to do this.

The project was made more difficult by the fact that the LSI-11 allows both 16 bit word width reads and writes, as well as single byte writes. (Single byte reads are *not* required, since the processor can ignore whatever data it wishes.). Additionally, a read modify write cycle is provided, and that had to be supported by the bus adaptor.

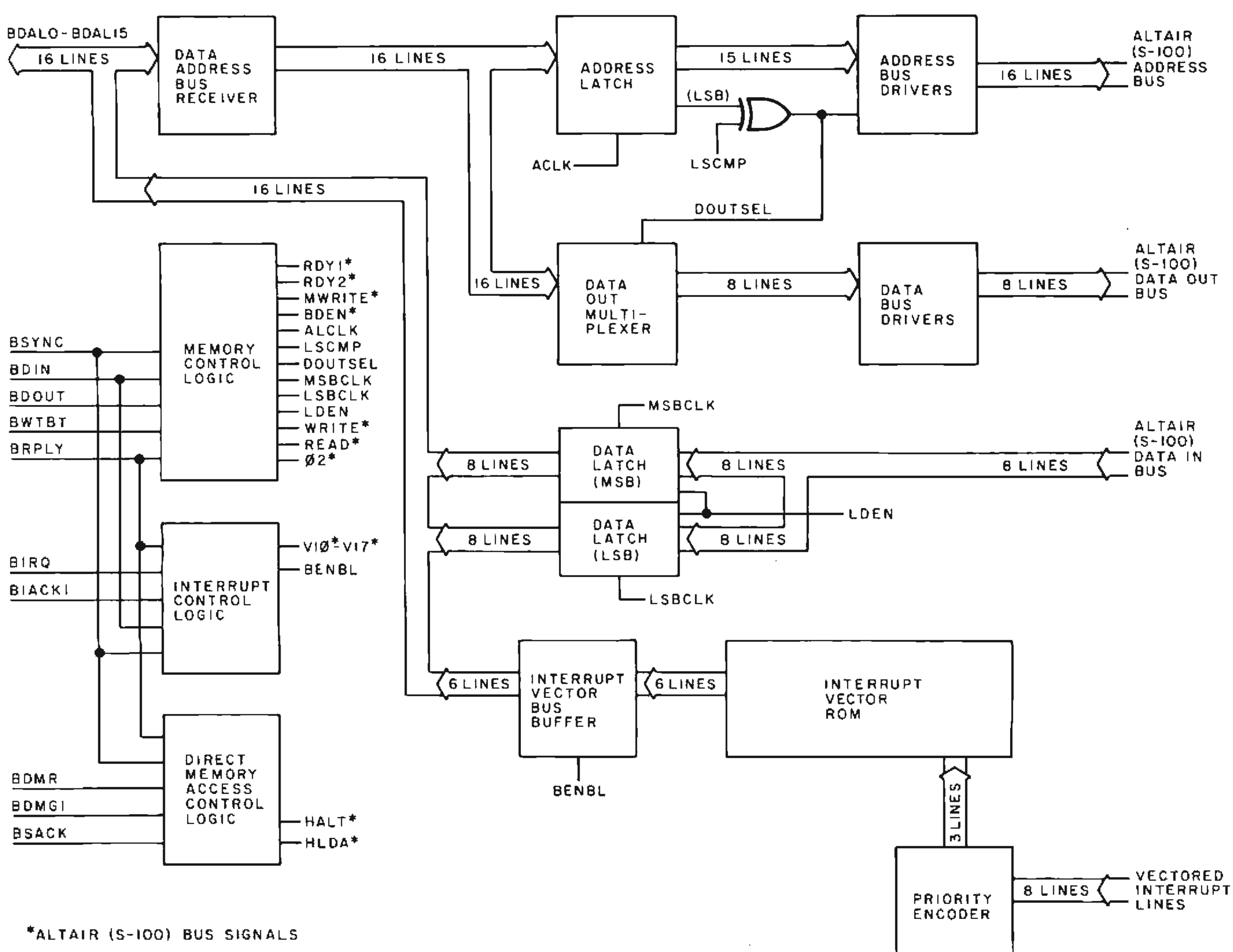
Finally, both direct memory access and vectored interrupts had to be supported if there was to be any hope of running LSI-11 software on the beast which would result. It should be noted that just because a memory address responds from the Altair (S-100) bus, that doesn't mean that it couldn't be built to look to the LSI-11 as if it were a "normal" LSI-11 device interface. I wouldn't be giving up the facility to use standard PDP-11 software by building this bus adaptor, but merely making it a bit more difficult.

I should note here that what follows is an untested design based on the references given at the end of the article and some conversations with friends who have Altair (S-100) systems. A variety of Altair (S-100) schematics from Processor Technology, IMSAI, Technical Design Labs and Cromemco, to name a few, were scanned to try to insure some approximation of compatibility, but the design is neither built nor tested. I welcome any comments from readers who are interested in this project.

The block diagram of the S2L bus interface box is shown in figure 1. It consists of three main sections devoted to memory signals, direct memory access signals and interrupt signals. The schematics for the control logic blocks may be found in figures 7 thru 9, but for the time being, I will discuss their function rather than their detailed implementation in order to simplify the discussion.

Let us first consider a memory read operation as diagrammed in figure 2. Note that all times in the timing diagrams are sequenced correctly, but, many times they are not to scale. Also, note that the clock (Φ2) may be shown as being synchronous with some signals, but this is not necessarily so since the LSI-11 bus is an asynchronous bus. The LSI-11 indicates the start of a bus cycle by asserting the BSYNC L signal. ("Asserted" means going into a logical 1 state, not becoming +4.5 V;

Figure 1: Block diagram of the S2L interface which allows Altair (S-100) bus peripherals and memory to be used with the LSI-11 "Q" bus. Details of memory control, interrupt control and DMA control logic blocks are found in figures 7, 8 and 9 respectively.



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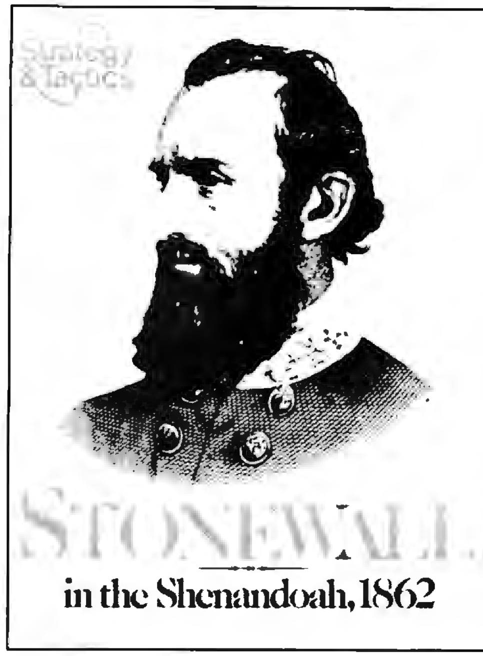

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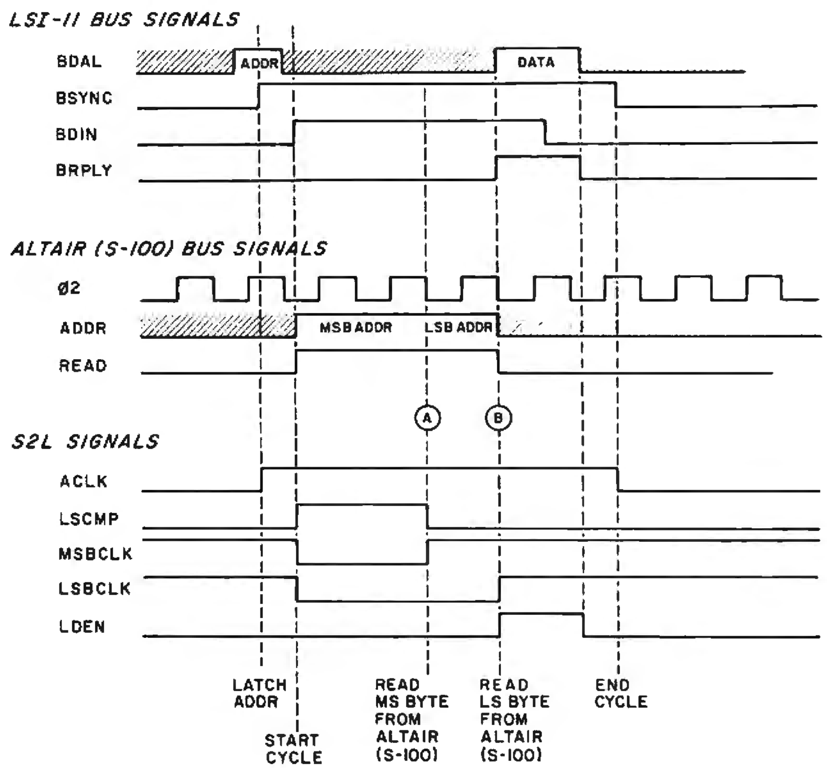

Figure 2: Timing diagram of an LSI-11 memory read cycle as it is interpreted by the S2L interface and passed on to the Altair (S-100) bus.

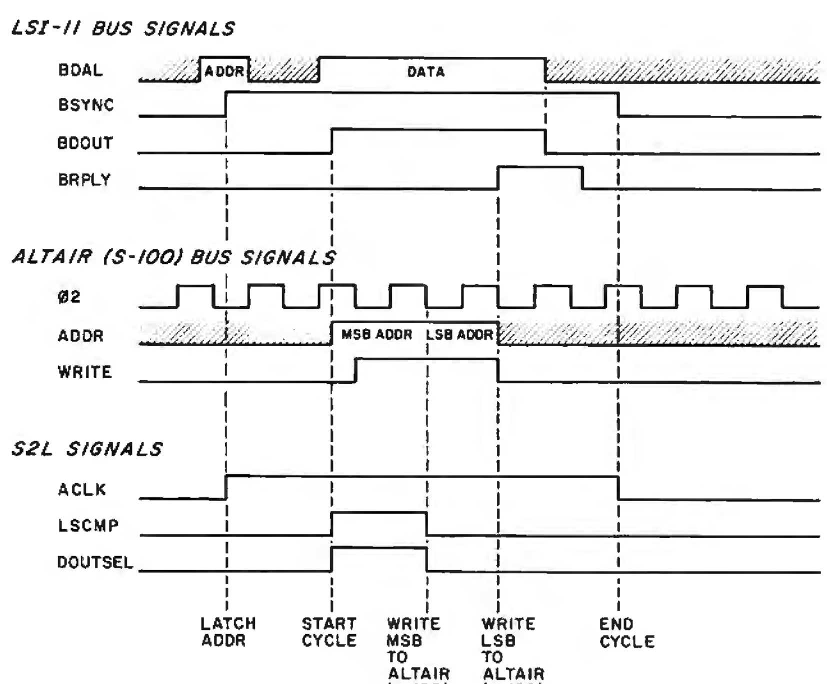

Figure 3: Timing diagram of an LSI-11 memory write (16 bit word) cycle as it is interpreted by the S2L interface and passed on to the Altair (S-100) bus.

I am using the trailing "L" to denote negative logic, so in this case assertion means going to 0.4 V.) The negative logic used by all LSI-11 bus signals is due to the bus being implemented with open collector logic, rather than the three state logic which is common in most hobby computers. The rising edge of BSYNC should be used to latch the data and address bus lines (BDAL0 L to BDAL15 L), since at this time they contain the address for the bus cycle. When BDIN L is asserted, the first of the two Altair (S-100) bus cycles occurs. This cycle occurs during the first complete cycle of the S2L clock that occurs after BDIN L is asserted. The first byte read is the most significant byte of the word (ie: the byte with the odd address), and the LSCMP signal is asserted during this time in order to provide the correct address on the Altair (S-100) bus. I am assuming that since only 16 bit word reads may be made, all addresses on the bus during read cycles will be even addresses.

The falling edge of the S2L clock (Φ_2) latches the most significant byte of data enabled by the low state of the MSBCLK signal (Ⓐ in figure 2). Then the second read cycle is initiated, this time for the least significant byte (even address). When the cycle completes, the least significant byte is latched with the next S2L clock enabled by a low state on the LSBCLK signal (Ⓑ in figure 2). After this, LDEN is asserted to drive the latched data onto the LSI-11's "Q" bus, and BRPLY L is sent back to the LSI-11 to tell it that the data on the bus is valid. The termination of the BDIN signal indicates to the S2L that the data has been accepted by the LSI-11, and the S2L then terminates BRPLY L.

For this interface to work with a reasonable variety of Altair (S-100) bus memory boards, phase 2 clock, RDY1, RDY2 and WAIT signals are provided. Any S2L clock pulse may be inhibited by one or both of the RDY lines until a slow peripheral has data ready, or has accepted data, in a manner similar to that of the 8080 and 6502 processors.

The write cycle, diagrammed in figure 3, is almost identical to the read cycle. The differentiation between read and write is made by the LSI-11 by asserting the BDOUT L signal rather than BDIN L. During a write, rather than having to provide two clocks to latch the bytes read, the S2L must provide

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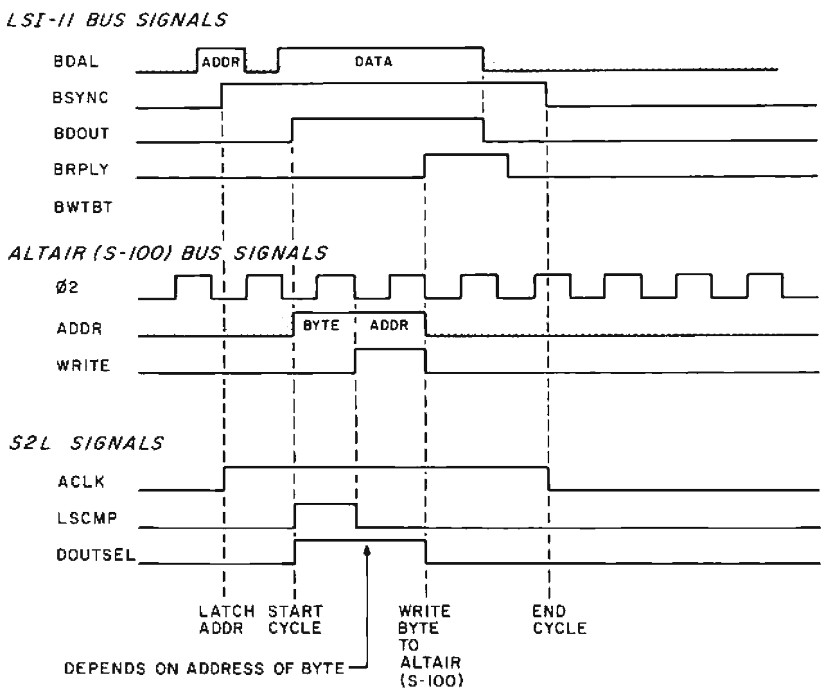

Figure 4: Timing diagram of an LSI-11 memory write (8 bit byte) cycle as it is interpreted by the S2L and passed on to the Altair (S-100) bus.

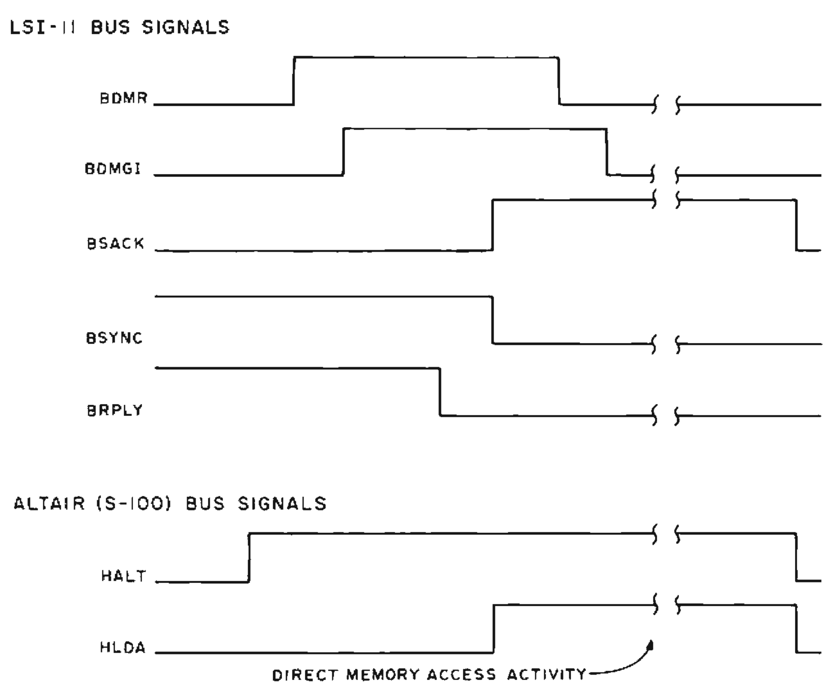

Figure 5: Timing diagram for the initiation of DMA activity on the Altair (S-100) bus between memory segments on that bus and peripherals on that bus. (DMA from an Altair (S-100) bus peripheral to peripherals or memory on the LSI-11 "Q" bus is not supported in this design.)

a byte selection signal (DOUTSEL) to a multiplexer which will determine which half of the word will be written at any time. The timing is as in the figure. As in the case of the read, I assume that only word width writes will occur with a word (even) address.

In order to perform a single byte write cycle, the S2L performs a normal write cycle, except that it skips the first of the two Altair (S-100) bus writes. Since it is the write to the address with the inverted lowest bit which is skipped, the correct byte is written in half of the time, and the cycle terminates normally. The diagram for this is shown in figure 4.

The LSI-11 bus supplies signals with which the memory and device interfaces reply to the LSI-11 when IO transactions take place (BRPLY L). The S2L adaptor will respond with a BRPLY L signal whether the address requested is implemented or not. This will cause problems with some LSI-11 software and firmware, especially the firmware ODT LOAD command which sizes memory automatically by sensing when memory addresses fail to set a BRPLY L response. Also, the system of reply signals has another advantage which will be lost when using the S2L adaptor: when attempting to write to ROMs on the LSI-11 system, no BRPLY L is generated and a bus timeout error occurs, which is a good error detection system. The S2L will effectively eliminate this facility.

The procedure for dealing with direct memory access (DMA) is much easier on the Altair (S-100) bus than on the LSI-11 bus, and the S2L interface enables the Altair (S-100) devices to take advantage of the simpler protocol. Looking at figure 5, the device starts the DMA cycle by asserting the HALT L signal to request use of the bus. The assertion of BDMR L by the S2L requests the use of the bus by a peripheral of the LSI-11. The simultaneous assertion of BDMGI L and the termination of BSYNC L and BRPLY L indicates that the DMA privilege has been granted by the LSI-11. The S2L then responds by terminating the BDMR signal, and by asserting both the BSACK L signal to tell the LSI-11 that the bus is in use, and the HLDA L signal to tell the Altair bus peripheral that it may now use the bus. Note that if more than one peripheral wishes to perform direct memory

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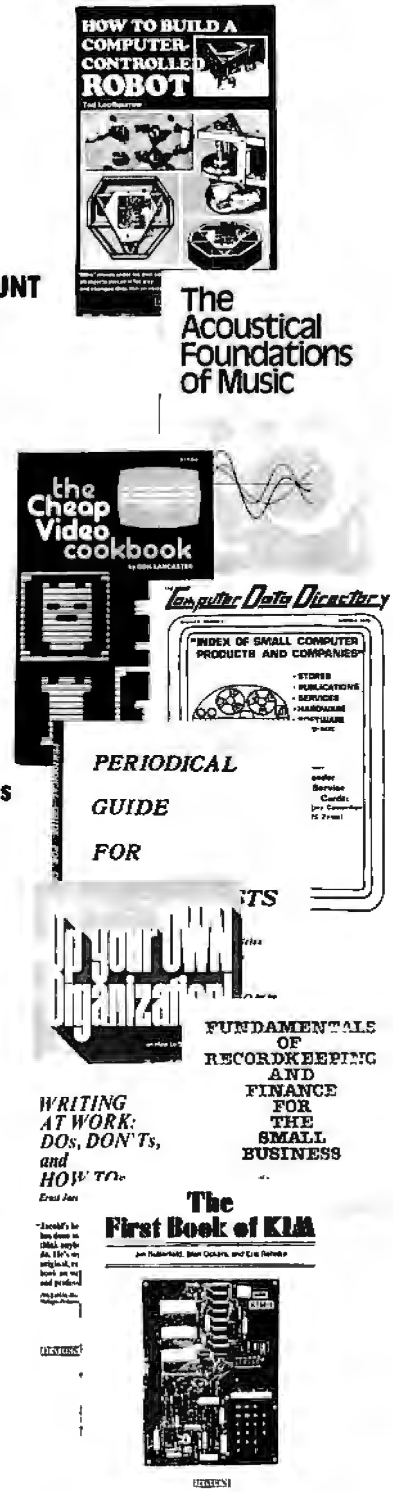

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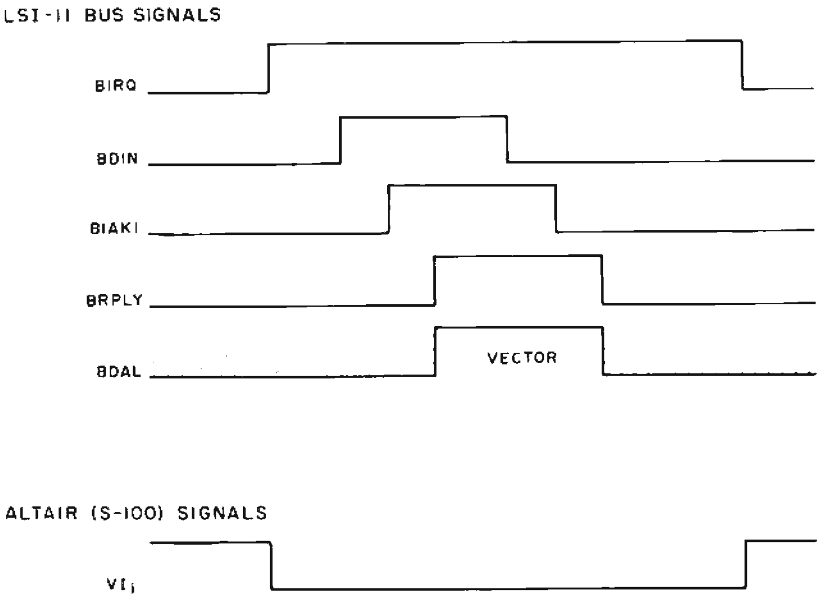

Figure 6: Timing diagram of the S2L interface's response to an Altair (S-100) bus vectored interrupt signal. When one of the eight possible vectored interrupt signals is asserted (low), the S2L interface responds by creating a vectored interrupt sequence for the LSI-11 "Q" bus.

access, neither will be able to determine easily which device is being selected. Whenever the Altair (S-100) bus peripheral is finished with the bus, it terminates the HALT L signal, causing the S2L to terminate the BSACK L signal, releasing the bus for the LSI-11 to use.

Note that this interface will not allow Altair (S-100) bus devices to perform DMA to any memory which is on the LSI-11 side of the S2L; I felt that the simplicity of the interface as shown, combined with the complexity of the extended function interface, was justification for leaving things as shown. In any event, one justification for the development of this adaptor was that Altair bus memory was cheaper than DEC memory, so one can expect most of the system memory to be Altair (S-100) bus memory.

One other point to make is that the LSI-11 on board memory is dynamic and requires refreshing, which the LSI-11 does by microcoded routines. This microcoded refresh creates bursts of bus activity every 2 ms, lasting about 130 μs. These bus activations can cause problems in a real time environment, and can cause data overruns in DMA devices if these devices do not allow enough internal buffering to last the 130 μs. Although nonburst-mode refresh is possible, the prices which DEC asks for the module are pretty high for the facility. For this reason, use of Altair (S-100) bus static memory and disabling of the KD11-F's dynamic memory and refresh microcode might be useful to some people.

The eight vectored interrupt lines on the Altair (S-100) bus lend themselves directly to interfacing with DEC's vectored interrupt scheme. Looking at figure 6, the timing for the S2L's interrupt sequence is given. Whenever one of the vectored interrupt inputs from the Altair (S-100) bus (VI0 thru VI7) is asserted, BIRQ L is sent back to the LSI-11 to request interrupt service. The

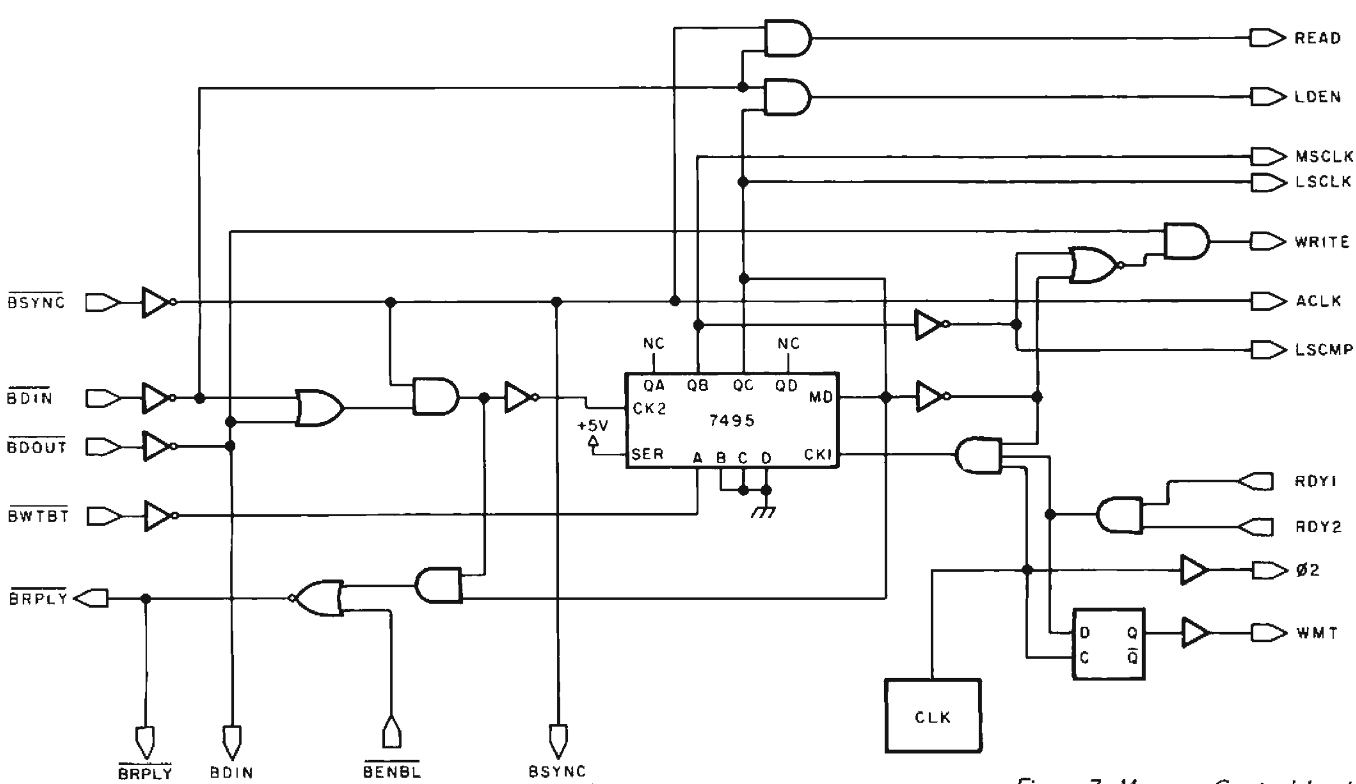

Figure 7: Memory Control Logic.

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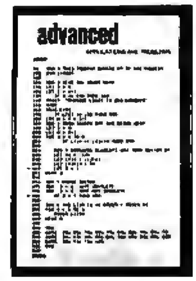

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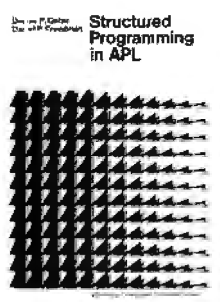

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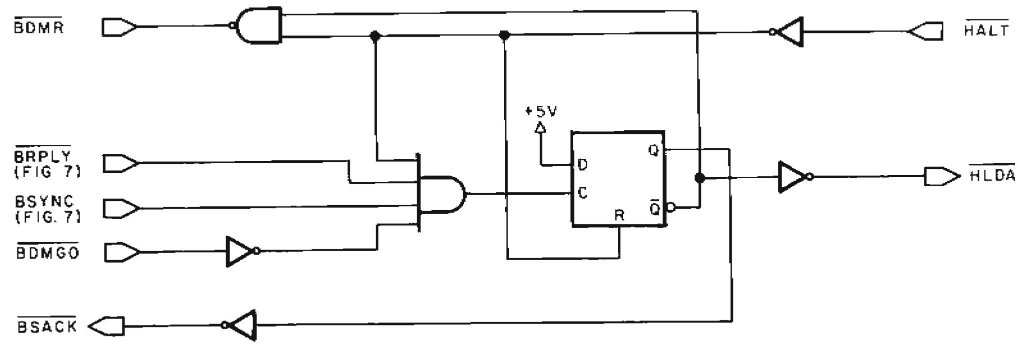

Figure 8: Direct memory access control logic.

LSI-11 will respond by asserting BIAKI L and BDIN L, the former to request that an interrupt vector be placed on the bus, and the latter to indicate that data is coming in on the bus. The S2L responds to this by placing the vector on the bus, and by asserting BRPLY L, to inform the LSI-11 that the bus value is now valid data. The termination of BDIN L and BIAKI by the LSI-11 results in the S2L's termination of BRPLY L and the release of the bus for other uses. At this point, an interrupt should occur. Each of the eight interrupt lines is prioritized and will cause an LSI-11 interrupt when asserted. The LSI-11 vector address for each Altair (S-100) bus vectored interrupt line will be the value programmed in the read only memory.

I am not going to go through the schematics in figures 7 thru 9 in detail, since their function is fairly well-defined by the timing diagrams and the above discussions. However, a few notes are in order. The use of the 7495 is a bit subtle since the load, which occurs via CLK2 whenever a BDIN or BDOUT signal is asserted, changes the mode of the shift register from LOAD to SHIFT. This allows the first write to be skipped conditionally upon the state of the BWTBT L signal at the start of the write cycle, and allows the shifting to stop when the one bits coming in from the serial input reach the third flip flop. The latches used for most significant byte and least significant byte storage are 8551s since they have three state buffers, which allow their output to be placed on the LSI-11 bus conditionally.■

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LSI-11, PDP-11/03 User's Manual (EK-LSI11-TM-002), DEC, 1975.

Microcomputer Handbook, DEC, 1976.

Also: numerous Altair (S-100) bus peripherals schematics borrowed from friends served as background information for this discussion.

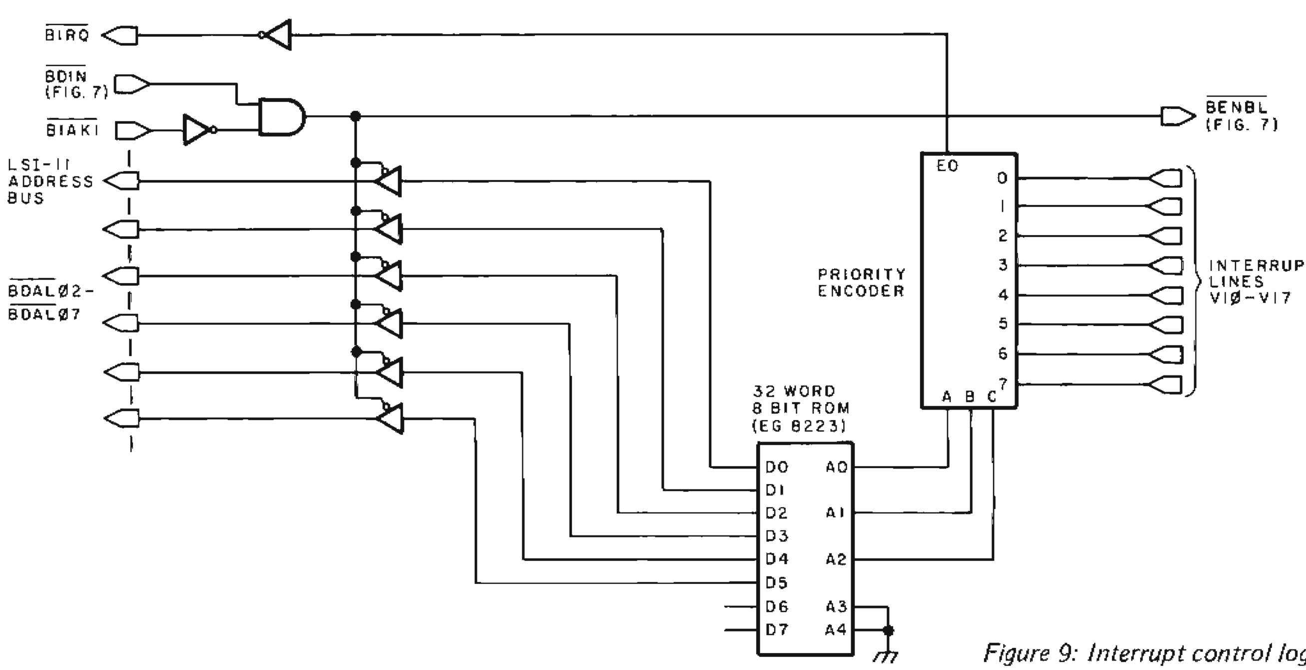


Figure 9: Interrupt control logic.

Math in the Real World

Joel Boney
Motorola Inc
6707 LaSalle
Austin TX 78723

Your system is completed. You bought a kit with lots of memory and spent many hours assembling it. The manufacturer's manuals are dog eared. You've read various works on computer programming which inspired you to write integer multiply and divide routines and create your own mathematical statement processor. The routines are thoroughly debugged and now you are ready to enter your first mathematical statement: 5 ÷ 2 =. The computer promptly responds with '2'. Well, that's not really wrong in integer arithmetic where remainders are often dropped, but most of us learned in the third grade that 5 ÷ 2 really equals 2.5. How do you get your computer to answer 2.5 instead of 2? Read on. The answer lies in floating point or real representation and manipulation of numbers.

Floating Point

A floating point number is a number that can be represented by an integer portion and a fractional portion. The number 2.5 is a floating point or real number; so are 3.3, 0.9 and 2.0. All can be represented by an integer part and a fractional part. The numbers: 1, 8 and 17 are not real since they have no fractional portion. Numbers in scientific notation such as 2.37×10^8 are real.

Before jumping head first into how to represent floating point numbers in the computer, an understanding of how floating point numbers are represented in base ten is instructive. For example, in the number 125.76, the digit positions correspond to:

$$\begin{aligned} 1 \times 10^2 &= 100.00 \\ 2 \times 10^1 &= 20.00 \\ 5 \times 10^0 &= 5.00 \\ 7 \times 10^{-1} &= 0.70 \\ 6 \times 10^{-2} &= 0.06 \end{aligned}$$

The decimal point merely tells where the boundary exists between the positive powers of ten and the negative powers of ten. Numbers to the left of the decimal point are positive powers of ten and those to the right are negative powers of ten. In binary (base 2) numbers the same rule applies. The base 10 equivalent of the binary number 101.11 is:

$$\begin{aligned} 1 \times 2^2 &= 1 \times 4 &= 4.00 \\ 0 \times 2^1 &= 0 \times 2 &= 0.00 \\ 1 \times 2^0 &= 1 \times 1 &= 1.00 \\ 1 \times 2^{-1} &= 1 \times .5 &= 0.50 \\ 1 \times 2^{-2} &= 1 \times .25 &= 0.25 \\ & & \overline{5.75} \end{aligned}$$

The '.', which is now called a binary point, denotes the division between positive and negative powers of two. This concept can be expanded to any base, but here we will only consider base 10 and base 2. In general the '.' might be called the "base point."

Quite often it is more convenient to represent real decimal numbers in scientific notation. This allows both very small and very large numbers to be written with the fewest number of digits (eg: 3.75×10^{-10}, rather than 0.000000000375). Numbers in scientific notation are represented by three parts: integer portion, fractional portion and exponent. In order to conserve memory within the computer and to make calculations have fewer steps, it is more convenient to represent all real numbers with only a fraction and an exponent. This is accomplished by moving all digits to the right of the base point while adjusting the exponent appropriately. Thus all numbers are of the form: $.FFF \times 10^{EE}$ in base 10 (where "*FFF*" are the fractional digits and "*EE*" is an expression for the power of ten exponent). This change of form does not in any way alter the value of the number or change the accuracy of the subsequent calculations. For example: 3.75×10^2

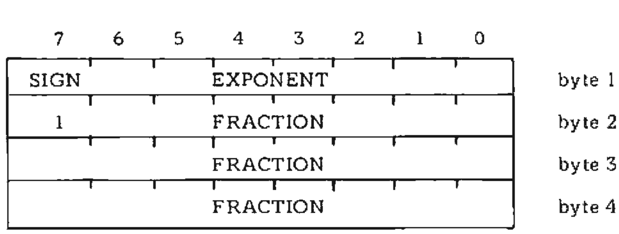


Figure 1: Format for the arrangement of data in the computer's memory for the binary floating point representation described here. The high order bit of byte 2 will usually be '1' because of normalization. The only time that this will not happen is when the number being represented is zero.

About the Author

Joel Boney is currently employed by Motorola in its Integrated Circuits Division plant in Austin TX. He is responsible for the software input in the system and architectural design for future Motorola processors and peripheral chips. He is currently involved in the MC6809 and MC6805 projects.

Binary					Decimal				
00000000	.10000000	00000000	00000000	=	0.5	x	2^0	=	0.5
00000001	.10000000	00000000	00000000	=	0.5	x	2^1	=	1.0
00000001	.11000000	00000000	00000000	=	0.75	x	2^1	=	1.5
10000001	.11000000	00000000	00000000	=	−0.75	x	2^1	=	−1.5
01111111	.10000000	00000000	00000000	=	0.5	x	2^{-1}	=	0.25
11111111	.10000000	00000000	00000000	=	−0.5	x	2^{-1}	=	−0.25
00000000	.10000000	00000000	00000001	=	0.50000006	x	2^0	=	0.50000006

Table 1: An example of binary floating point numbers and their decimal equivalents.

becomes 0.375×10^3 thus eliminating the integer portion of the number.

If the fractional portion of a number has a fixed number of digits as is the case within a computer, then the greatest accuracy is achieved if the digit following the base point is nonzero. Using a 5 digit fraction, the number 0.37868×10^5 is more accurate than 0.03787×10^6. We now have formulated two rules that will make calculations easier and maintain maximum accuracy:

- Floating point numbers will consist of only a fraction and an exponent.
- Floating point numbers will be adjusted so that no zeros immediately follow the base point.

The only exception to these rules is the number zero which is allowed to violate rule two. Manipulating numbers so that they conform with the above rules is called normalization.

All of the above examples were in base ten, but as might be expected the concepts are just as valid in base two except the exponent is now a power of two instead of ten. Therefore, numbers are of the form: $.FFF \times 2^{EE}$ (where *FFF* and *EE* are now hexadecimal representations of binary numbers). At this point we must decide upon a specific format to use within the computer that will give sufficient accuracy without wasting memory. A fraction containing 24 bits gives an accuracy of $1/2^{24}$ or about seven decimal places. A two's complement exponent of base 2 containing seven bits gives an exponent range of approximately $\pm 10^{\pm 19}$. This format has sufficient magnitude range for many applications and can represent numbers over 38 decimal orders of magnitude.

There are several common formats for floating point numbers. In some, the exponent is a power of 16 and a fraction is considered normalized if any of the four most significant bits are set. Exponents are often represented in "excess" form

Listing 1: Algorithm for inputting real numbers. This algorithm will result in a floating point number in the four byte form described in this article.

```
Begin
    Clear exponent and integer of answer
    Clear fraction of answer (4 bytes)
    Do while input character ≠ '.'
        If input character = '−' then set fraction sign = 1
        If input character is a number then
            Convert input character from ASCII to binary
            Integer: = integer * 10 + input number
        Endif
    Enddo
    N: = 1
    Do while input character = number and N < 8
        Convert input character from ASCII to binary
        Fraction: = fraction + (Table(N) * input number)
        N: = N + 1
    Enddo
    Do while integer ≠ 0
        Shift integer and fraction one bit right
        Increment exponent
    Enddo
    Normalize answer
    Roundup answer
    Delete integer portion and fraction byte 4
End
```

instead of two's complement form. In this form some appropriate number is added to all exponents so they are all positive. The specific format I chose consists of four 8 bit bytes for each number and is shown in figure 1. The high order bit (bit 7 typically) of byte one is the algebraic sign of the number (1 = −). The low order seven bits of the first byte (bit 6 to bit 0) are the signed two's complement value of the exponent. Bytes two, three and four contain the normalized unsigned fraction with the understood binary point preceding byte two. Note that bit seven of byte two is 1 for all normalized numbers except zero because of normalizing rule two.

Some sample numbers and their decimal equivalents are given in table 1.

Ins and Outs

Now that we've defined a format for real numbers, how can we put it to use? Several subroutines will be required. We need to be able to read real numbers from a terminal and convert them to our defined format and vice versa. Also, we need to outline how we can operate on real numbers once they are converted. First, the ins and outs.

The conversion to and from the terminal is the most difficult part of handling floating point numbers. An attempt is made here to outline a procedure that is well adapted to microprocessors. Several other algorithms are outlined in *The Art of Computer Programming, volume 2* by Donald Knuth (see references following this article) including information on converting to and from scientific notation.

Suppose the input string 13.05 is typed at a terminal. Since the computer will see the characters as they are typed left to right, the program in listing 1 can easily convert any number preceding the decimal point into a binary integer. In this example the 13 becomes 00001101, assuming an 8 bit integer. Once the decimal point is read the fraction can be calculated if a table of unnormalized fractions corresponding to the binary equivalent of 10^{-n} is stored in memory. Since there is no need for n to be larger than the accuracy of the final format, table 2 was calculated with n equal to seven. Table 2 was calculated using a BASIC program to determine which bits in the fraction should be set. Note that the fractions in this table are 32 bits wide instead of the 24 bits required in the final answer. This is done to insure the accuracy of the conversion. Using this table and starting with a zero exponent byte and zero in a 4 byte fractional portion in the answer, when the first number following the decimal point is typed on the terminal it is multiplied by the table value of the fraction for 0.1 and added to the fraction of the answer. Subsequent inputs are multiplied by 0.01, 0.001, etc, and added to the answer until the bottom of the table is reached after seven inputs or the input string is exhausted. Since the input numbers are 0 thru 9, it is easier and takes less time in a microprocessor to do the multiplication by successive additions. For the example input, 13.15, the fraction is calculated by example 1. Including the integer portion and the exponent the input becomes the representation in example 2. Normalizing this by shifting the integer and fraction four bits to the right and adding 4 to the exponent it becomes example 3.

Now the integer portion and the low order byte of the fraction can be deleted after incrementing the next to low order byte if bit seven of the low order byte was set (rounding up). See example 4 for the final value in the correct 4 byte format. Had the input number been −13.05 instead of +13.05, the only difference in the number generated would be bit seven of the exponent (fraction sign bit) would be set. Note that if the input had been something like 0.005 the normalizing process described above would require left shifts of the frac-

Table 2: Decimal fraction to binary equivalent conversions. The table covers only the first seven digits since the accuracy of the routines we are considering is only seven places. This conversion assumes that the exponent is set to zero.

Decimal		Binary					
0.1	=	00011001	10011001	10011001	10011001	=	10^{-1}
0.01	=	00000010	10001111	01011100	00101000	=	10^{-2}
0.001	=	00000000	01000001	10001001	00110111	=	10^{-3}
0.0001	=	00000000	00000110	10001101	10111000	=	10^{-4}
0.00001	=	00000000	00000000	10100111	11000101	=	10^{-5}
0.000001	=	00000000	00000000	00010000	11000110	=	10^{-6}
0.0000001	=	00000000	00000000	00000001	10101101	=	10^{-7}

Example 1.

	1	x	0.10	=	1	x	00011001	10011001	10011001	10011001
+	5	x	0.01	=	5	x	00000010	10001111	01011100	00101000
							00100110	01100110	01100110	01100001

Example 2.

Integer	Fraction				Exponent
00001101	00100110	01100110	01100110	01100001	00000000

Example 3.

Integer	Fraction				Exponent
00000000	11010010	01100110	01100110	01100110	00000100

Example 4.

Exponent	Fraction		
00000100	11010010	01100110	01100110

Table 3: Portion of table used to convert the exponent of 2^e into decimal notation of the form F x 10^{Exp}.

e (index)	Exp (1 byte)	F (3 bytes)		
.	.		.	
.	.		.	
.	.		.	
4	00000010 (2)	00101000	11110101	11000001 (0.16)
3	00000001 (1)	11001100	11001100	11001100 (0.80)
2	00000001 (1)	01100110	01100110	01100110 (0.4)
1	00000001 (1)	00110011	00110011	00110011 (0.2)
0	00000000 (0)	00000000	00000000	00000000 (0)
1	00000000 (0)	10000000	00000000	00000000 (0.5)
2	00000000 (0)	01000000	00000000	00000000 (0.25)
3	00000000 (0)	00100000	00000000	00000000 (0.125)
.	.		.	
.	.		.	
.	.		.	

tion while decrementing thus creating a negative exponent.

Outputting real numbers is slightly more difficult. The fraction and exponent part must be dealt with simultaneously since conversion of the exponent from base 2 to 10 will affect the fraction. Due to this complexity, it is preferable to output real numbers in scientific notation. The output form that is used is 1305 E + 2 instead of $0.1305 \times 10^{+2}$.

To accomplish the conversion we will need a rather large (4 by 128 byte) table to convert 2^e (where e is the exponent of the real number to be output) to $F \times 10^{Exp}$ (where F is an unnormalized fraction in our 3 byte notation and Exp is the power of 10 of the number we wish to print. A portion of the middle of the table is given in table 3.

The base 2 exponent e is not a member of the table, but is used as the index into the table to retrieve values of Exp and F. Using e we access the table and multiply the fraction F times the fraction of the number we wish to output using a multiply fraction subroutine described later. The resultant fraction of this multiplication will be the fraction that must be converted and printed followed by the letter E and the decimal value of Exp, including its sign, from the table to obtain the desired scientific notation.

Printing of the fraction uses the same table as used for converting to real format. In the first iteration the binary fraction for 0.1 is subtracted from the fraction until the fraction goes negative. For each subtraction except the last a counter is incremented and becomes the number to print. After the number is printed, the fractional value of 0.1 is added back into the fraction. This whole process is effectively a binary divide by 0.1. After 0.1 is added back, the procedure is repeated for 0.01, 0.001, etc, until all seven output digits are printed. This process is summarized in listing 2.

It should be noted that the above algorithms pose particular problems on various implementations and the programmer should be cautious of such things as overflow and carry flags as well as round off errors while doing the multiprecision operations.

The Arithmetic

Now we have a format for floating point or real numbers and we know how to input and output them. All that remains is the internal manipulation subroutines. All these subroutines require two normalized real arguments, which in the following text and listings will be referred to as argument 1 (ARG1) and argument 2 (ARG2). They all create a normalized real answer (ANS). We will use the predefined format except that during the internal manipulation some extra bits are occasionally needed at the right of the fraction to retain accuracy. Only a couple of bits are necessary, but since most microprocessors have 8 bit words, it is easier to add a whole byte to each fraction thus creating a 4 byte fraction instead of the prescribed three bytes. This fraction will be rounded to a 3 byte fraction in the defined format before returning to the caller of the manipulation subroutines.

Addition is defined as ARG1 + ARG2 = ANS. Once again the base 10 analogy will be useful in understanding how to implement an algorithm. If we desire the sum of the two normalized real numbers 0.375×10^5 and 0.22×10^4, we must first make the exponents equal before we can add the fractions. Once the exponents are equal, the fractions can be added and the answer given the common exponent. Thus, the example becomes:

$$\begin{array}{r} 0.375 \times 10^5 \\ +\,\underline{0.022 \times 10^5} \\ 0.397 \times 10^5 \end{array}$$

To make the exponents equal in this example, the number with the smaller exponent was shifted right n decimal digits and its exponent incremented by n. It is desirable to adjust the smaller number since shifting the larger number would require left shifts that might result in numbers being shifted into the integer portion which

Listing 2: Algorithm for outputting real numbers. This algorithm uses table 2 to convert the fraction. The output algorithm shifts the fraction and integer part left until the exponent equals zero or bit 7 of the integer word is set to 1. If bit 7 of the integer word is set, any further shifts will destroy the number.

```
Type entry = record of
        Exp: 8 bit binary
        F: 24 bit fraction
Var conv-table: array [-64..63] of entry
    table: array [1..7] of 24 bit fraction
(* e is the base 2 exponent of the number to be output*)
Begin
    Fraction: = conv-table[e].F * fraction of number to be output
    If Fraction sign = 1 then print '-'; endif
    Print decimal point
    N: = 1
    Do while N <8
        CTR: = -1
        Do while fraction is positive
            Fraction: = fraction-table(N)
            CTR: = CTR + 1
        Enddo
        Fraction: = fraction + table (N)
        Convert CTR to ASCII and print it
    Enddo
    Print 'E'
    If conv-table[e].Exp is negative then print '-'; Endif
    Convert conv-table[e].Exp to decimal ASCII and print it
End
```

would violate the defined format. Any shifting, however, can create accuracy problems in a fixed digit (or bit) computer, since if the magnitude of two numbers differs by a large amount, their sum will be equal to the larger number. For example, if we had a calculator with six digits for a fraction and we added 0.300×10^8 and 0.20×10^0, the answer would be 0.300000×10^8 since shifting 0.20 seven digits to the right would cause it to become zero.

Listing 3: Algorithm for real addition and subtraction. Before additions or subtractions can take place the numbers must be manipulated so that their exponents are equal.

```
Begin
    Do while exponent ARG1 ≠ exponent ARG2
        If exponent ARG1 > exponent ARG2 then
            Shift fraction ARG2 right one bit
            Increment exponent ARG2
        Else
            Shift fraction ARG1 right one bit
            Increment exponent ARG1
        Endif
    Enddo
    If fraction ARG1 is negative then 2's complement fraction ARG1;Endif
    If fraction ARG2 is negative then 2's complement fraction ARG2;Endif
    If operation is addition then
        Fraction ANS: = fraction ARG1 + fraction ARG2
    Else
        Fraction ANS: = fraction ARG1 – fraction ARG2
    Endif
    Exponent ANS: = exponent ARG1 or ARG2
    Normalize ANS
    Roundup ANS
End
```

Listing 4: Real multiplication algorithm. When multiplying real numbers it is not necessary to worry about the exponents being equal. Multiplication can take place under any conditions.

```
Begin
    Fraction ANS: = fraction ARG1 * fraction ARG2
    Exponent ANS: = exponent ARG1 + exponent ARG2
    Set overflow flag if exponent overflowed or underflowed
    Normalize ANS
    Roundup ANS
End
```

Listing 5: The real division routine must check to see if the dividing number is zero. If it is, the overflow flag is set and the routine is ended. The fractional part of the number to be divided should always be smaller than the dividing number. This is assured by shifting the number to be divided one place left and incrementing the exponent.

```
Begin
    If fraction ARG2 = 0 then
        Set overflow flag
    Else
        Shift fraction ARG1 one bit right
        Increment exponent ARG1
        Fraction ANS: = fraction ARG1/fraction ARG2
        Exponent ANS: = exponent ARG1 – exponent ARG2
        Set overflow if exponent overflowed or underflowed
        Normalize ANS
        Roundup ANS
    Endif
End
```

Binary real addition is identical to the above decimal example except the shifts are by *n* binary bits and the exponent is a power of 2. The algorithm in listing 3 first checks to see if the exponents are equal. If not equal, the fraction of the smaller argument is shifted one place right and its exponent incremented. This continues until the exponents are equal. Since our format stores the fractions as absolute unsigned values, all the fractional portions of negative fractions must be two's complemented before addition can proceed. Once the negation of any negative fractions is completed, the fractions can be added by a multiprecision addition. The fractional portion of the answer is then composed of the sum of the adjusted fractions and the exponent becomes the common exponent. This answer may need to be normalized. In fact, all the manipulation subroutines will require a check for normalization before exit, and therefore a subroutine to normalize arguments is desirable.

Subtraction is defined as ARG1 – ARG2 = ANS. The subtraction routine is identical to the addition routine except a multiple precision subtract is substituted for the addition. In most implementations the addition and subtraction routines are the same routine with a flag to indicate whether a subtraction or addition of the fraction should occur.

Multiplication of real numbers is easier than addition since the fractions can be multiplied regardless of the exponents. The multiplication algorithm in listing 4 is defined as: ARG1 * ARG2 = ANS. The multiplication of the fractions involves a 32 bit by 32 bit multiplication, but only the most significant 32 bits of the result are necessary which reduces the complexity of the multiplication somewhat.

For details on writing a multiplication subroutine check the references, or better yet check the user group library for your microprocessor to see if one already exists. The biggest problem with real multiplication is that overflow or underflow of the exponent can occur during the addition of the exponents. Therefore, the subroutine must take precautions to check for overflow or underflow and flag the result as erroneous if either occurred. The answer obtained by the above algorithm may need to be normalized before returning it to the caller.

Division is similar to multiplication and is defined as ARG1/ARG2 = ANS. Since most division algorithms will not terminate if ARG2 is equal to zero, the division algorithm in listing 5 first checks the fraction of ARG2 to see if it is zero. If it is zero, the algorithm should return with an overflow indication. Also, many division algorithms require that the fraction of ARG1 be smaller than the fraction for ARG2. The division routine could check to see if this condition exists, or better yet, since we know both numbers are normalized (ie: the most significant bit is set) and since we have added an extra byte for accuracy, we can always shift ARG1 one bit to the right and insure that it is less than ARG2. Of course, we must add one to ARG1's exponent to compensate for the right shift. Now we can proceed with a normal 32 by 32 bit divide of the fractions. Once the fractional portion of the answer is complete, the exponent of the answer is equal to the exponent of ARG1 minus the exponent of ARG2. Again precautions must be taken to insure (or at least flag) that no underflow or overflow of exponents has occurred. The answer may need to be normalized.

Conclusion

This article has attempted to give an overview of what is necessary to create a package of floating point subroutines that can be used for many applications. Floating point manipulation is not trivial and some microprocessors will be better adapted to the task than others. Instructions that can handle multiple precision arguments such as "add with carry," "subtract with carry" in conjunction with shifts and rotates on memory make the implementation simpler. Be cautioned that the procedures outlined are general and any particular microprocessor will require special procedures to adjust for processor peculiarities. In any case, it seems the majority of the code is dedicated to shifting fractions right or left to insure accuracy or in checking for various error conditions.

On the positive side, a good debugged binary floating point package takes less memory and runs faster than the decimal floating point implemented in many BASIC packages. The add, subtract, multiply and divide routines lay the framework for the programmer to create more exotic subroutines such as sine, cosine, etc. Best of all, when we ask our computer to divide 5 by 2, it responds with 2.5.■

REFERENCES

1. Knuth, Donald E, *The Art of Computer Programming, volume 2,* Addison-Wesley, 1969.
2. *Digital Computer Design Fundamentals,* McGraw-Hill, 1962, pages 70 thru 73.
3. Boney, Joel, *Floating Point Package,* Motorola User Group Library, 1976.

Event Queue

September 6-8, COMPCON Fall '78, Capitol Hilton Hotel, Washington DC. Sponsored by the IEEE Computer Society, this conference will cover computers and communications, interfaces and interactions. Such topics as microprocessors in communications, multiple computer systems, advances in communications technology and many others will be discussed at this conference. Contact Kenneth H Crandall Jr, COMPCON Fall '78, POB 639, Silver Spring MD 20901.

September 11-12, Microprocessors: Hardware, Software and Application, Worcester Polytechnic Institute, Worcester MA. This intensive, highly focused program is geared specifically for technical professionals who need comprehensive knowledge of the latest microprocessor technology. It will give the attendee a better understanding of current and future microprocessor based systems, likely trends and relevant technologies and a firm foundation in critical areas of microprocessor system design and project management. Contact Continuing Professional Education, Worcester Polytechnic Institute, Worcester MA 01609.

September 11-15, Coding and Information Theory, Georgia Institute of Technology. This course will present the fundamentals of representation, storage and transmission of data. Protection against storage and transmission errors using error detection and error correcting (including Hamming) codes will be developed. Efficiency enhancement through information compressing codes, predictive run encoding and Markov chains (probabilistic finite state machines) will be discussed. Contact Short Course Program Office, 6266 Boelter Hall, UCLA Extension, Los Angeles CA 90024, (213) 825-3344 or 825-1295.

September 12-14, Computers in Cardiology, Stanford University. This conference will include contributed presentations on the application of computers to cardiovascular research, diagnosis and treatment. Contact Mrs Droni Moo, conference coordinator, Cardiology Division, Stanford University School of Medicine, 701 Welch Rd, Suite 3303, Palo Alto CA 94304, (415) 497-7507.

September 12-14, WESCON/78 Show and Convention, Los Angeles Convention Center and Los Angeles Bonaventure Hotel. Contact Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo CA 90245, (213) 772-2965.

September 15-17, 2nd Annual Personal and Business Small Computer Show, New York Coliseum, New York NY. Exhibitors will include major manufacturers, distributors and publications in the computer field. A lecture series will include topics of interest to business and professional people, hobbyists and the general public. Contact D R McGlynn, 71 N Moger Av, Mt Kisco NY 10549.

September 18-20, Computer Cryptography, The George Washington University. This course is designed to aid managers and users of computer systems in the protection of computer data. Commercial products will be discussed generically and relative capabilities discussed in general. Emphasis will be placed on the implementation, use, cost and impact of cryptographic systems in computers and in evolving computer networks. Contact Continuing Engineering Education Program, George Washington University, Washington DC 20052, (202) 676-6106 or the toll free number (800) 424-9773.

September 18-22, Digital Filters, Georgia Institute of Technology. This course will provide a practical introduction to the subject of digital filters. Topics will include the frequency approach, Fourier series and integrals, nonrecursive filter design, theory of recursive filter design, discrete Fourier transforms, fast Fourier transform implementation, estimation of power spectra and nonlinear phenomena due to quantizing signals. This course will be of interest to those who use linear combinations of data. The emphasis is on its basic nature and practicability. Contact Nonie Watanabe, Short Courses, 6266 Boelter Hall, UCLA Extension, Los Angeles CA 90024.

September 29-October 1, International Microcomputer Exposition, Dallas Convention Center, Dallas TX. This exposition will be directed toward all levels of technology from the professional engineer to the beginning computer hobbyist. In addition to the seminars, a panel of experts will be available to answer questions. Contact Beverly Tanner at (214) 271-9311.

October 5-8, Midwest Personal Computing Show, Apparel Center's Expocenter, Chicago IL. More than 200 displays featuring the full spectrum of the latest personal computing developments are expected to be presented by manufacturers and distributors. A comprehensive program of seminars, forums and practical application clinics will parallel the four days of exhibits. Contact Midwest Personal Computing Exposition, ISCM, 222 W Adams St, Chicago IL 60606, (312) 263-4866.

October 16-19, Information Management Exposition and Conference, McCormick Place, Chicago IL. The theme, strategic planning in the information age, was selected to convey the need for a corporate strategy for the gathering, storage, retrieval, dissemination and management's use of information. Computer equipment to be demonstrated will include large, medium and small systems, mini and micro systems, small business systems, terminals, peripherals, data communication systems, data collection and preparation handling systems, magnetic media and accessories. Contact Clapp & Poliak Inc, 245 Park Av, New York NY 10017.

October 24-26, Project Management for Computer Systems, New York NY. This 3 day seminar will illustrate techniques for planning, implementing, installing and controlling projects. Specific examples and case studies will be discussed. This seminar is intended for computer project managers, data processing managers, VPs of administration, financial managers and others involved in EDP systems development and implementation. Contact the University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

October 27-29, BizComp '78, Marriott Motor Hotel, Atlanta GA. BizComp '78 will highlight the small budget necessary for the independent business operator to be able to purchase an in-house computer system. All facets of the small business computer industry will be on display from the latest innovations in computers to business software and word processing, supplies and services. Contact Felsburg Associates Inc, 12203 Raritan Ln, POB 735, Bowie MD 20715, (301) 262-0305.

October 30-November 1, 2nd Annual Data Entry Management Association Conference, Sheraton Harbor Island Hotel, San Diego CA. The conference theme is data entry today and tomorrow and will concentrate on the human side of data entry and distributed data entry. There will be a full schedule of seminars, panel discussions, and workshops, including hands-on workshops with various vendors' equipment. Contact Marilyn Bodek, DEMA, 16E Weavers Hill, Greenwich CT 06830.

October 31-November 3, Tulsa Computer Conference, Skyline Sheraton East, Tulsa OK. Contact Tulsa Chapter Association for Systems Management, 4110 S 100 E Av, Suite 128, Tulsa OK 74145.

November 5-8, Computer Applications in Medical Care, Washington DC. This IEEE sponsored symposium on computer applications in medical care is designed to inform physicians and health care professionals about current and potential applications of computer technology to patient care; and to identify areas of future research and development that need to be addressed. Contact Abund O Wist, PhD, general chairman, Medical College of Virginia, (804) 770-4957.

November 6-8, Asilomar Conference on Circuits, Systems and Computers, Asilomar Hotel and Conference Grounds, Pacific Grove CA. This conference, sponsored by the IEEE Computer Society, will delve into areas such as circuit theory and design, communication and control systems, computer systems, computer aided design, etc. Contact Donald E Kirk, Electrical Engineering Dept, Naval Postgraduate School, Monterey CA 93940.

November 8-11, Asian Business Expo/Hong Kong, Kowloon-Canton Railway Convention Complex, Hung Hom, Hong Kong. This exposition will feature displays of over 100 business services and equipment with the opportunity to participate in seminars. Contact Industrial & Scientific Conference Management Inc, 222 W Adams St, Chicago IL 60606, (312) 263-4866.

November 13-16, COMPSAC, The Palmer House, Chicago IL. The IEEE Computer Society's second international computer software and application conference. This conference will bring together computer practitioners, users and researchers to share their ideas, experiences and requirements for applications software, management techniques, and software development support, including automated techniques. Contact Wallace A Depp, executive director, Processor and Computer Software System Division, Bell Laboratories, Naperville IL 60540, (312) 690-2111.

November 19-22, The 11th Annual Microprogramming Workshop, Asilomar Conference Ground, Pacific Grove CA. This worksop will provide a forum for the discussion and comparison of design techniques for firmware and for the supporting hardware. Informal interaction between groups working in similar research and application environments will highlight the topical session. For more information contact Dr Alice G Parker, Micro-11 program chairman, Dept Electrical Engineering, Carnegie-Mellon University, Pittsburgh PA 15213, (412) 578-2472.

November 28-30, 9th Annual Canadian Computer Show, International Centre, Toronto CANADA. Products displayed at this show will include: computer and data processing equipment, supplies and services, including minicomputers, peripheral hardware and software, keypunch services, consulting and contract programming and timesharing. Contact Industrial Trade Shows of Canada, 36 Butterick Rd, Toronto Ontario M8W 3Z8, (416) 252-7791.■

Plugging the KIM-2 Gap

Power Wiring Table

Number	Type	+5 V	Gnd
IC1	7404	14	7
IC2	7400	14	7
IC3	7486	14	7

M Garth Notley
RFD 1 Route 129
Yorktown Heights NY 10598

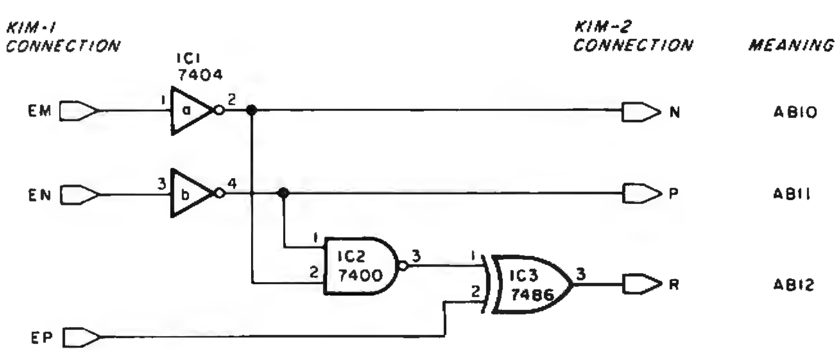
One of my uses of the KIM-1 computer is to create programs that will execute on a smaller dedicated 4 K byte 6500 processor such as the 6505. However, the user manual for the KIM-2 4 K byte memory expansion says the following:

> *Note. . .It is* not *possible to put your expansion memory in the memory block 0400-1400 hex already decoded on KIM-1.*

I want to use the addresses hexadecimal 0000 to 0FFF to hold all the programs and simulated IO routines that will eventually go in the 6505, then use addresses hexadecimal 1000 to 13FF for the programs that test the 6505 programs. Readers with the same problem may care to use my solution which I have been using successfully for some months.

Use address switch setting 0001 for an address range of hexadecimal 1000 to 1FFF. Then modify the connections for address lines AB10, AB11 and AB12 as in figure 1. This modification will map the KIM-1 address range of 0400 to 13FF into a KIM-2 address range of 1000 to 1FFF.■

Figure 1: Modification to allow the address of the KIM-1 from hexadecimal 0400 to 13FF to be mapped into a KIM-2 address range of 1000 to 1FFF.



See ad on pages 8 & 9.

Clubs and Newsletters DIRECTORY

The following is the second BYTE Clubs and Newsletters Directory (the first was published in January 1977 BYTE). The directory was compiled from information supplied by the various clubs listed. A form was sent to all clubs and newsletters listed in the first directory requesting up-to-date information. If the form was not returned, we deleted the club from the second directory. In addition, the listing was correlated with back issues of the magazine and materials on file in the BYTE offices. If information is missing in one or more categories, it means the data was not provided. We will be keeping the file available and updating it for the next directory; so, if there are errors or if you have a new club which has just been formed, send the information to: Laura Hanson, Clubs and Newsletters Editor, BYTE Publications Inc, 70 Main St, Peterborough NH 03458.

The listings follow this form:

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

Zips 00000 - 10000

1. New England Computer Society
2. POB 198
   Bedford MA 01730
3. Mitre Corp Cafeteria, Rt 62, East of Rt 3, Bedford MA
4. First Wednesday of month
5. *NECS Newsletter* (monthly)
6. Dave Day, president; Dave Mitton, secretary
7. (603) 434-4239, (617) 493-3154, respectively
8. $6 per year
9. Current users groups are PC Net (personal computing network), TRS-80, 6800, Digital Group, PET, RCA-1802.

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1. The Alcove Computer Club
2. 230 Main St
   North Reading MA 01864
3. Same
4. Special events
5. None
6. J P Vullo
7. (617) 664-4271
8. None
9. Hardware and software; systems such as MITS, TRS-80.

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1. The Boston Computer Society
2. 17 Chestnut St
   Boston MA 02108
3. Commonwealth School
   151 Commonwealth Av (corner Dartmouth St)
   Boston MA
4. Fourth Wednesday of every month at 7 PM
5. Being developed
6. Jonathan Rotenberg
7. (617) 227-1399
8. $5 per year; includes admission to all meetings and events plus mailing list
9. An information exchange and resource center based upon members' needs. The BCS sponsors: sub-groups, advanced and beginner hard-

ware and software sessions, software exchange, various types of guest speakers, etc, when needed and feasible.

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1. TRS Club
2. 96 Dothan St
   Arlington MA 02174
5. Yes
6. Poi K Pow
9. TRS user group; TRS cassette or diskette media. A software library is available at low or copying cost. Library includes inventory, security, games, data base, sort, etc.

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1. Rhode Island Computer Hobbyists (RICH)
2. c/o E D Iannuccillo
   POB 599
   Bristol RI 02809
3. Jabbour Electronic City
4. Third Tuesday of September, October, November, March, April, May
5. Yes
6. E D Iannuccillo
7. (401) 253-5450
8. $2 per year
9. Construction projects
10. Our club is small and friendly. Members come from many vocations and many are students; most are not experts in computers. We demonstrate equipment and help each other with problems.

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1. The Southern New England Computer Society
2. 267 Willow St
   New Haven CT 06511
3. Varies
5. *Yankee Bits*
6. Arthur Downes
7. (203) 562-8034
8. $3 covers dues and newsletters
9. Micros, minis and macros from the ELF to IBM 360 and software at all levels
10. Sometimes we will send a sample copy of *Yankee Bits*. Anybody is welcome no matter what level of interest or knowledge.

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1. Bridgeport Area Society for Involved Computerists (BASIC)
2. 12 Wildwood Dr
   Trumbull CT 06611
3. Trumbull Town Library
4. Second Wednesday each month
5. *MICROFLASH* published monthly
6. Al Song
7. (203) 268-9807 (nights), (203) 576-6556 (days)
8. $8 per year
9. Hardware, software, anything whatsoever to do with computers
10. Established August 1977 with 40 paid members and 150 on the mailing list.

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1. Amateur Computer Group of New Jersey
2. 1776 Raritan Rd
   Scotch Plains NJ 07076
4. Main meeting third Friday of month; 8080/Z-80 user group first Friday of month; 6800/6502 user group fourth Friday of month
5. Yes
6. Sol Libes
7. (201) 277-2063
8. $5 per year
9. User groups: CPM, Radio Shack, PET, 8080/Z-80, 6800/6502, 1802 and 9900. Classes: BASIC, 8080 programming, 6800 programming, 6502 programming and "Getting Started."
10. Software libraries, annual member directory, annual festival, and annual contest. There are 800 members. Starting PC network.

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1. New Jersey Apple Users Group
3. Computer Lab of NJ
   141 Route 46
   Budd Lake NJ 07828
4. First Friday of month, 7:30 PM
6. Dan Fischler

Zips 10000 - 20000

1. New York Amateur Computer Club
2. POB 106, Church St Station
   New York NY 10007
3. Varies
5. Untitled, monthly 5 to 10 page newsletter

Circle 4 on inquiry card.

DIRECTORY, continued

6. Bob Schwartz or John Frederick
7. (212) 663-5549, 866-4298, respectively
8. $10 per year
9. Mostly S100, word processing, some music types.

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1. **Long Island Computer User Society (LICUS)**
2. POB 322
East Northport NY 11731
3. Commack High School South
Commack NY
4. Second Tuesday of each month
5. *Queue* (monthly)
6. John Vollers or Jim Zukowski
7. (516) 493-3612, 586-3555/757-9329, respectively
8. $3 per year
9. Software development and applications dealing mainly with DEC equipment
10. Informal group meetings; we try to have a guest speaker discuss a relevant subject of interest.

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1. **Long Island Computer Association**
2. 36 Irene Ln E
Plainview NY 11803
3. New York Institute of Technology
4. Second Friday of month — 8080 group; third Friday of month — regular meeting and 6800 group
5. *The Stack*
6. Aileen Harrison
7. (516) 938-6769
8. $10 per year, $5 students
9. 6800 group, 8080 group, Pascal, BASIC, kit building, and troubleshooting.

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1. **AEC Transfer**
2. 8 Gedney Way
or 147 Fostertown Rd
Newburgh NY 12550
5. *AEC Newsletter*
6. William Callahan Jr
7. (914) 565-4621
8. 25 cent entry fee; $5 subscription fee (subject to change)
9. Correspondence club; newsletter with emphasis on science and science fiction articles.
10. Readership supported for articles and stories, nonprofit; glad to hear from anyone interested in receiving or contributing to newsletter.

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1. **Computer Hobbyists in Processing (CHIPS)**
2. POB 4840
General Electric Co, CSP3-16
Syracuse NY 13221
3. Baker Hall, Electronics Park
Syracuse
4. Usually third Thursday each month except July and August
5. *CHIPS Newsletter*
6. Dave Flagg or Jerry Green
7. (315) 456-1903, 456-7357, respectively
8. $4 per year
9. Hobby systems of all kinds and all applications.
10. Approximately 50 members and average meetings attended by 38 to 45 members. Membership not restricted to GE and is drawn from 60 mile radius around Syracuse.

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1. **Rome Area Computer Enthusiasts (RACE)**
2. RD 1, W Carter Rd
Rome NY 13440
3. Patty's Stagecoach Inn
4. Second Tuesday at 7:30 PM
5. *Micros Along the Mohawk*
6. Michael Troutman
7. (315) 336-0986
9. Special interest groups around the 6800 and 8080/Z-80 microprocessors as well as one for beginners.

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1. **Students Cybernetic Laboratory (SCYL)**
2. c/o A E Adams
RFD Box 260
Chaffee NY 14030
3. Yorkshire NY
4. Irregular
5. Irregular, at present
6. A E Adams or Karl Grampp
7. (716) 849-1433
8. None
9. Intel 8080, Business applications
10. Club just now becoming reactivated and reorganized.

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1. **Rochester Area Microcomputer Society**
2. POB D
Rochester NY 14609
5. *Memory Pages*
6. Glenn Alexander, president
7. (716) 377-0697

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1. **Ithaca Computer Group**
2. POB 91
Ithaca NY 14850
5. None
6. S Edelman
7. (607) 273-3271
8. None
9. All

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1. **Electronotes**
2. 1 Pheasant Ln
Ithaca NY 14850
3. None
4. None
5. *Electronotes — Newsletter of the Musical Engineering Group*
6. Bernie Hutchins

7. (607) 273-8030
8. Newsletter, monthly 22 page issues, $20 per year
9. Electronic music, including digital control of analog synthesizers, and special music synthesis techniques
10. Back issues and other publications are available; write for order forms, descriptions and sample issue.

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1. Pittsburgh Area Computer Club
2. 400 Smithfield St
   Pittsburgh PA 15222
3. Northway Mall Community Room
4. Third Sunday, 11 AM
5. Yes
6. Fred Kitman
7. (412) 391-3800
8. $12 per year
9. Robots and the MACC
10. Meetings consist of a general talk, formal meeting and speaker.

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1. The Central Pennsylvania Computer Club
2. 1979 Crooked Oak Dr
   Lancaster PA 17601
3. Elizabethtown Public Library — alternate locations occasionally
4. Third Friday on even numbered months, fourth Wednesday on odd numbered months; 7 PM to 9 PM both nights
5. *Data Dump*
6. Joseph Pallas
7. (717) 569-3137
8. $3 students, $7 adults per year (includes subscription to *Data Dump)*
9. We are a small group (30+ members) which provides help to newcomers and fosters interaction among system owners.

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1. PET User Group
2. POB 371
   Montgomeryville PA 18936
5. *PET User Notes*
6. Gene Beals
7. (215) 257-8195
8. $5
9. Commodore PET information and program exchange.

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1. Philadelphia Area Computer Society
2. POB 1954
   Philadelphia PA 19105
3. Science Building, LaSalle College
   20th Olney Av
   Philadelphia PA

The listings follow this form:

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4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

4. Third Saturday of the month, 2 PM
5. *The Data Bus*
6. Dick Moberg or Jon Bondy
7. (215) 923-3299, 642-1057, respectively
8. $10 ($5 student)
9. Subgroups on most major processors/computers; starship subgroup (for space travel simulation with microcomputers), computer network and Pascal
10. PACS currently has over 250 members and is growing fast. Emphasis is placed on education and monthly courses are offered on A/D design, Pascal, 6502 BASICs, operating systems, and many other topics. For meeting information and other local computer news, dial the PACS hotline: (215) 925-5264.

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1. Delaware Users of Microprocessor Systems (DUMPS)
2. 2405 Maxwellton Rd
   Stanton DE 19804
5. None
6. Jodie S Hobson
7. (302) 998-5594
8. None
9. Currently hardware oriented
10. Meetings consist of general business, technical talk or demonstration, and rap session.

Zips 20000 - 30000

1. Washington Amateur Computer Society
2. 4201 Massachusetts Av, #168
   Washington DC 20016
4. Last Friday of each month, 7:30 PM
5. *JWACS* ($5 per year)
6. Bob Jones, editor
10. For more information, send a SASE to the above address.

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1. Microcomputer Investors Association
2. 2415 Ansdel Ct
   Reston VA 22091
3. As called
5. *The Microcomputer Investor*
6. Jack Williams
7. (703) 620-2591
8. Nonprofit, professional association, $30/member
9. The fundamental purpose of the association is to facilitate the exchange of data and information relating to investments and microcomputers with the express purpose of such interchange being directed toward maximizing profits in stocks, bonds, warrants, stock options and commodities, including commodity options and futures straddles.

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1. Chesapeake Microcomputer Club Inc
2. POB 87
3. White Oak Library
   11701 New Hampshire Av
   Silver Spring MD
4. Fourth Monday at 7:30 PM
   7:30 PM
5. *The Analytical Engine*
6. Rich Kuzmack
7. (703) 821-2873 (home)
8. $12 per year
9. Processor-oriented special interest groups, investors group, store and forward system with Bell 103 access for message and software interchange, PC networking.
10. Geographically-oriented chapters and affiliates in the greater Washington DC/Baltimore area.

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1. Amateur Radio Research and Development Corp (AMRAD)
2. 1524 Springvale Av
   McLean VA 22101
3. Patrick Henry Branch Library
   101 Maple St E, Vienna VA 22180
4. First Monday of each month at 8 PM
5. *AMRAD Newsletter*
6. Paul L Rinaldo
7. (703) 356-8918
8. Regular $10, second in household $5, student $2. Life: regular $100, second in household $50.
9. Computers, amateur radio and radioteleprinter operation.

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1. Crystal City Computer Club
2. 3008 Mosby St
   Alexandria VA 22305
3. Commissioner's Conference Room, Bldg 3, 11th Floor, Crystal Plaza
   Arlington VA
4. First nonholiday Monday, 11:30 to 12:30
5. *IO*
6. Russell E Adams
7. (703) 548-8261
8. $4 per year and $5 with newsletter
9. Assist newcomers and interchange of programs and ideas
10. Have small library, occasional classes, 48 members; affiliated with Chesapeake Computer Club.

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1. Charlottesville Computer Hobbyists Club
2. 1928 Arlington Blvd, #209
   Charlottesville VA 22903
3. Math-Astronomy Building
   University of Virginia
4. Second Monday of each month
5. No name, monthly if possible
6. Richard A Stanley
7. (804) 296-5583 or 293-7976
8. $2 per year (supports newsletter)
9. Software, systems and hardware.

1. IBM 5110/5100 Users Group
2. 5541 Parliament Dr
   Suite 104
   Virginia Beach VA 23462
5. Not yet, but probably every other month
6. Richard E Easton
7. (804) 490-0154
9. Specifically oriented toward IBM 5110 or IBM 5100 installed users
10. Especially interested in 5110-5100 applications in the health care field.

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1. Tidewater Computer Club
2. 677 Lord Dunmore Dr
   Virginia Beach VA 23462
3. Electronic Computer Programming Institute, Janaf Office Bldg, Janaf Shopping Center, Military Hwy and Virginia Beach Blvd in Norfolk VA
4. 7:30 PM first and third Tuesdays each month
5. None as of yet
6. C Dawson Yeomans, publicity chairman
8. $6 for six months
9. Discussions cover hardware and software, system demonstrations.
10. New members are always welcome.

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1. Dyna-Micro Users Group
2. POB 1053
   Lexington VA 24450
5. *Digital Directions*
6. Dr Frank A Settle Jr
7. (703) 463-6244
8. $15 initial fee
9. Items of interest to users of Mini-Micro and Dyna-Micro designers marketed by E&L Instruments Inc.

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1. West Virginia Computer Society
2. 167 Iroquois Trail
   Ona WV 25545
3. Dunbar City Park, Dunbar WV
5. *"Oscillations" of the West Virginia Computer Society*
6. Bill England, president
7. (304) 736-9794
8. $12 per year, also family and student dues; newsletter subscription $6 per year
9. Any and all phases of computers and associated equipment; digital electronics
10. Everyone is welcome to attend meetings. Member MACC.

The listings follow this form:

1. Name of organization
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6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

1. Triangle Amateur Computer Club
2. POB 17523
   Raleigh NC 27609
3. Dreyfus Auditorium
   Research Triangle Park
4. Last Sunday of each month at 2 PM
5. Newsletter
6. Russell O Lyday Jr
7. (919) 787-4137, 541-6957
8. Subscription fee $6 per year
9. Introductory as well as advanced topics discussed at each meeting.

Zips 30000 - 40000

1. Atlanta Area Microcomputer Hobbyist Club
2. POB 7602
   Atlanta GA 30357
3. Decatur Federal Savings
   Dunwoody Village
4. Last Wednesday of each month
5. *AAMHC Newsletter*
6. Jim Straligos
7. (404) 894-3505 (days), 457-8030 (nights)
8. $10 per year
9. Personal computing; 6800 and 8080
10. Club participates in the Atlanta ham fest/computer fest which is held annually first weekend in June.

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1. Okaloosa Computer Hobbyist Club
2. 32 Denton Blvd, NW #72
   Fort Walton Beach FL 32548
4. Every second and fourth Tuesday
6. Loretta R Guske, secretary
7. (904) 242-5938

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1. Central Florida Computer Club
2. 2821 Sunset Rd
   Apopka FL 32703
3. Basement of Orlando Utilities Bldg, 500 S Orange Av, Orlando FL
4. Third Sunday of each month, 2 PM
5. Notes on last meeting and points of interest for next meeting
6. John W Neel
7. (305) 862-1329
8. $10 per year
9. Helping newcomers to the world of computers; programming classes; keeping up to date on the latest innovations in the computer world.
10. In progress: complete list of members showing type of equipment by CPUs; type of occupation; telephone numbers (work and home); use of computers.

1. Indian River Computer Society
2. FIT Elect Eng Dept
   Country Club Rd
   Melbourne FL 32901
3. Florida Institute of Technology
   Room 112
4. First and third Thursdays of each month at 7 PM
5. *THE μBUS* (monthly)
6. Frank Canova, president
7. Messages at: (305) 723-3701 ext 330
8. $3 initiation fee, $2 per quarter
9. Wide interest range from how to get started to large system applications. Many members are involved in homebrew 8080, 6502, 6800, Z-80 and F8 systems, although other systems are used by members as well.

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1. Birmingham Microprocessor Group
2. 774 Twin Branch Dr
   Birmingham AL 35226
3. "The Computer Center" (temporary)
4. Fourth Sunday each month at 2 PM
5. Newsletter
6. Joe Callaway
7. (205) 933-7806
8. $6 per year
9. None

Zips 40000 - 50000

1. Amateur Computer Society of Columbus OH (ACSCO)
2. Computer Data Systems
   1372 Grandview Av
   Columbus OH 43212
3. Center of Science and Industry
4. First Wednesday every month, 7:30 PM
5. *I/O*
6. Fred Hatfield K8VDU, president
7. (614) 486-0677
8. $10 per year
9. Personal computer networking, implementation of SAM 76 language versions and amateur radio applications.

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1. The Cleveland Digital Group
2. 8650 Harvard Av
   Cleveland OH 44105
3. Same
4. Third Sunday of the month, 2 PM
5. *The Shift Register*
6. David A Rolnicki, chairman: programs committee
7. (216) 524-2434
8. $10 per year
10. Informal meetings held every Tuesday night 7:30 on. Speakers come on a regular monthly basis (Sunday meetings).

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1. Goodyear Computer Club
2. c/o J F Derry, D-109E PIT 1
   Goodyear T&R Co
   Akron OH 44316
3. Goodyear Hall, 8 PM fourth Tuesday each month
4. IAG meets 7 PM before club meeting; club meets at 8 PM, business, speaker, demos; HG meets at 9 PM
5. *The Late Edition*

Circle 378 on inquiry card.

6. R Messner, Goodyear Aerospace Corp, D-47063, Akron OH 44315
7. (216) 794-7265
8. $10 per year
9. Investment analysis group (IAG), hardware group (HG), software group — under discussion (SG), setting up club library reference service for magazine exchange.
10. Have club Xerox CF-16 (Goodyear surplus) and Burroughs accounting machine. Looking for space to set up. Goodyear employees can telephone into GAC Sigma 9, 5 PM to midnight seven days a week using HG modem or equivalent. Membership not limited to Goodyear employees.

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5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

Circle 287 on inquiry card.

1. Compute, Evalute, Trade
2. POB 104
   Tipp City OH 45371
3. IUPUI, Indianapolis IN
4. Last Wednesday in month
5. *Byte Back*
6. Charles Tyzzer
8. None
9. Business systems.

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1. Dayton Microcomputer Association
2. Dayton Museum of Natural History
   2629 Ridge Av
   Dayton OH 45414
3. Same as above
4. Last Tuesday of month, 7:30 PM
5. *Dayton Microcomputer Association Data Bus*
6. Dean Lampman, president
   Marilyn Mix, vice-president
   Jack Steele, secretary
7. (513) 984-2084, 253-9468, 256-8005, respectively
8. $10 per year includes *Data Bus*
9. The 6800, 8080, 6502 special interest groups meet individually at least once a month
10. For the past two years we have held a 1 day show of computers for the public. This year we demonstrated at the Dayton Amateur Radio Convention and at the National Airborne Electronics Conference.

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1. Apple I Library
2. 51625 Chestnut Rd
   Granger IN 46530
3. Mail
6. Joe Torzewski
7. (219) 272-4670
8. Stamp appreciated for reply
9. Promote Apple I computer

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1. Floyd County Computer Enthusiasts
2. RR#2, POB 466A
   New Albany IN 47150
3. Varies
4. Set meetings are uncommon
5. None
6. Nathan Engle
8. None
9. Software, robots, artifical intelligence
10. Most of our members are high school level and we are making an effort to get a computer center in the local school system. Any help we can get would be much appreciated.

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1. Purdue University Computer Hobbyist Club (PUNCH)
2. Room 67, Electrical Engineering Bldg
   Purdue University
   West Lafayette IN 47907
3. Matthews Hall, Purdue University
4. Monday nights, 7 PM
5. *PUNCH* newsletter, published irregularly
6. Don Gillc, president
7. (317) 463-2340
8. $2 annual dues
9. General hardware and software design, hobbyist activities, sponsoring the annual IEEE computer show at Purdue (March 24 1979).

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1. Southeastern Michigan Computer Organization (SEMCO)
2. POB 9578
   Detroit MI 48202
3. Ford Automotive Safety Center Auditorium, Dearborn MI
4. Second Sunday of every month at 7 PM
5. *Data Bus*
6. Jim Rarus, president
7. (313) 775-5320 (24 hour club news line)
8. $10 per year or $6 per year 50 miles from Detroit
9. We have a number of special interest groups (SIGs). The following are some of our interests: Radio Shack, S-100 bus, KIM, 6800, Digital Group, RCA 1802, Heathkit, medical applications, SIG-BIG large machines and microinterfaces. A number of our members are also employed and interested in automotive applications.
10. Charter member of the Midwest Affiliation of Computer Clubs (MACC); host 1978 Computerfest; active in giving talks to educational institutions; access to club computer message service; free time to club members on HP 2000 BASIC system.

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1. Mid Michigan Computer Club
2. 15151 Ripple Dr
   Linden MI 48451
3. Various places (members' homes)
4. Irregular
5. None
6. Tony Preston
7. (313) 735-5279
8. None
9. Helping beginners select equipment; program library.

Zips 50000 - 60000

1. Eastern Iowa Computer Club
2. POB 164
   Hiawatha IA 52233
3. REC Bldg, basement
   999 35th St
   Marion IA
4. Last Sunday of month
5. Yes

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1. Quad City Computer Club
2. 2155 W 30 St
   Davenport IA 52804
3. Rock Island Arsenal
   Rock Island IL 61201
5. Monthly newsletter
6. Cecil Fretwell
7. (319) 386-3723
8. $6 per year

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1. Durant Computer Club
2. 901 S 12th St

Watertown WI 53094
3. Meets at above address
4. Fourth Monday at 7 PM
6. Bill Shier, president
9. System building
10. 15 members.

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1. **Small Computer Engineering Association of Minnesota**
2. POB 4244
St Paul MN 55104
3. University of Minnesota, Mechanical Engineering Bldg, Room 4
4. Last Thursday of month at 7:30 PM
5. *Twin City Technical Hobbyist*
6. Mike Young
7. (612) 884-2841
9. Hardware of different systems. 8080, 6800, 6502, MP-12, 1802 user groups.
10. 685 members.

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1. **Resource Access Center**
2. 3010 4th Av S
Minneapolis MN 55408
4. We sponsor SCEAM (Small Computer Engineering Association of Minnesota)
5. We publish *Twin Cities Technical Hobbyist* as a service to several local computer clubs, whose newsletters are contained therein.
6. R Koplow
7. (612) 781-7608
8. None
9. We are a special educational and research program in EDP and general technical aid to inner city, nonprofit community services. We sponsor microhobbyist clubs and newsletters.

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1. **Minnesota Computer Society**
2. POB 35317
Minneapolis MN 55435
3. Brown Institute, 3123 E Lake St
Minneapolis MN
5. *Tid BITS*
6. Jean Rice
7. 941-1051
8. $7 per year includes subscription to the newsletter
9. 8080, 6800, Z-80, 6502, 2650, 1802, 8085, TRS-80
10. Board meeting, film, show and tell, main speaker, business meeting, and random access session.

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1. **XXX-11**
2. 514 S 9th St
Moorhead MN 56560
3. By mail
4. Monthly
6. C R Corner
7. (218) 233-6682
9. Computer control; machine-independent software

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1. **RCA 301 Users Group**
2. RR 2, POB 585
Rapid City SD 57701
5. Yes
6. Jay Roman
7. (605) 341-5030
9. Communication via newsletter information about RCA 301/ UNIVAC Series 70 users, equipment, and software.

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1. **Fargo-Moorhead Computer Club (FMCC)**
2. POB 2017
Fargo ND 58102
3. First Thursday: NDSU Fargo
Third Thursday: MSU Moorhead
4. First and third Thursdays at 7:30 PM
6. Dan Kary
7. (218) 233-6682
8. $5 per year
9. Circuit design, promoting small computer interest; general programming.
10. About 80 members on list.

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1. **Missoula Amateur Computer Club**
2. 2203 E Crescent
Missoula MT 59801
4. First Monday of month
6. David Eggebraaten
7. (406) 728-5657
8. No dues
9. All aspects of microcomputers for persons in western Montana.

Zips 60000 - 70000

1. **CACHE (Chicago Area Computer Hobbyist's Exchange)**
2. POB 52
South Holland IL 60473
3. Northern Illinois Gas Bldg, Golf and Shermer Roads, Glenview IL
4. 1 PM, third Sunday of month, July excluded.
5. *MicroSCOPE* and meeting announcements
7. Hotline (recorded announcement), (312) 849-1132
8. $10 per year
9. More general than special – CP/M local users group; SOL/Cuts and 8080-Tarbell cassette software libraries; computer aided instruction group getting started; North Star users; Digital Group Users, etc.
10. Regular presentations by manufacturers, stores and fellow hobbyists.

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1. **ICE 9ine Inc**
2. POB 291
Western Springs IL 60558
3. Various dinner meeting locations
5. *Ice 9ine Journal*
6. R A Hoekstra
7. (312) 530-0067
8. Newsletter subscription is $10 per year

The listings follow this form:

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

9. Timesharing system for members. Very informative newsletter with over 500 subscriptions.

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1. SPC-12 Users Group
2. 7706 W Gregory
   Chicago IL 60656
3. 2704 W North Av, Chicago IL 60647
5. Soon to be announced
6. Manuel C Martinez
7. (312) 631-6623
8. None at present

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1. St Louis Area Computer Club Inc
2. POB 28924
   St Louis MO 63132
3. Thornhill Branch, St Louis County Library, FeeFee Rd and Willowyck
4. First Thursday of every month, 7 PM
5. *SLACC STACK*
6. Frank Curtis, president
7. (314) 993-0589
8. $5 per year
9. Every third meeting is "show and tell nite." Special groups include: 8080 homebrew group; modem design group; Dura terminal group
10. The club is a Missouri not-for-profit corporation for educational and scientific purposes related to microcomputers and personal computing. We have a technical and software library for members' use.

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1. Computer Network of Kansas City
2. 1251 Kansas Av
   Kansas City KS 66105
3. Midwest Research Institute, 425 Volker Blvd, Kansas City MO
4. Second Sunday of each month, 6:45 PM
5. *Thru-Put*, Earl Day, editor
6. Harold J Schwartz, president
7. (913) 371-2616 (work), 648-5410 (home)
8. $12 per year
9. Completing modem designed by members; hardware schooling and design and trading; software schooling; network priorities and software.
10. We are in the very interesting position since our start (two years ago) to shortly begin a local network. We hope to be tying into a nationwide network late next year.

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1. Mid-America Computer Hobbyists
2. POB 13303
   Omaha NE 68113
3. Commercial Federal Savings and Loan, Bellevue NE
4. Second Thursday of each month
5. *MACH*
6. Thomas F Smith, president
7. (402) 294-4479 (work), 292-6031 (home)
8. $5 per year
9. 1802 SIG and Poly 88 SIG
10. Most club members are military stationed at Offutt AFB, NE, SAC Headquarters where a great many computers are used for command and control application.

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1. SCAMPUS
2. 2215-A Walker Dr
   Omaha NE 68123
5. *SC/MP Users Group Newsletter*
6. Tom Bohon, coordinator

Zips 70000 - 80000

1. CENtral Oklahoma Amateur Computing Association (CENOACA)
2. POB 2213
   Norman OK 73070
3. Oklahoma State Univ Tech, 900 N Portland, Oklahoma City OK
4. Second Saturday, 10 AM
5. *CENOACA Newsbits* (monthly)
6. Lee Lilly or Don Holyoke
7. (415) 737-6121, 329-3209, respectively
8. $5 per year
9. 6800 Users Group meets third Saturday at 333 NW 5th, #2308, Oklahoma City OK. Dr James Petty is the contact person. Demonstrations and special programs planned for each CENOACA meeting.
10. *Newsbits* accepts free nonbusiness classified advertising (space available) and very low cost business advertising. CENOACA was organized in January 1976 and incorporated as a nonprofit organization under the laws of the state of Oklahoma in June 1976 to "provide a forum for the exchange and dissemination of information among members concerning the computer arts and sciences."

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1. The Tulsa Computer Society
2. POB 1133
   Tulsa OK 74101
3. Tulsa Vocational Technical School Seminar Room 3420
   E Memorial Dr
4. Last Tuesday of month at 7:30 PM
5. *The I/O Port*
6. Jerry Henshaw
7. (918) 836-7364
8. $6 per year

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1. The Computer Hobbyist Group of North Texas
2. POB 1344
   Grand Prairie TX 75051
3. UTA, University Hall, Room 108 and UTA, Green Center, Room 21530
4. 1 PM, third Saturday; 1 PM, first Saturday, respectively
5. *Printed Circuit*
6. Bill Fuller
8. $7 per year
9. TRS-80, 6502, PET, 9900, Digital Group.

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1. Houston Amateur Microcomputer Club

2. POB 37102
Houston TX 77036
3. Various
4. Second Friday and fourth Tuesday
5. *NYBBLE*
6. Troxel Ballou
7. (713) 661-6806
8. $12 per year

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1. JSC Computer Hobbyist Club
2. c/o EP4/L W Jenkins, president
NASA LBJ Space Center
Houston TX 77058
3. Gilruth Research Center, LBJ Space Center
4. First Thursday, third Monday 5 to 7 PM
5. Meeting announcement flyer
6. EP4/L W Jenkins, president
8. $7 per year first class mail
$4 per year JSC interoffice mail
10. Our *BYTE* subscription is mailed to JM6/Technical Library where it is available to club members and others in the periodical area.

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1. Texas A&M Microcomputer Club
2. POB M9, Aggieland Station
College Station TX 77844
3. Room 203, Zachry Engineering Center, Texas A&M University
4. Alternate Wednesdays, tutorials on other Wednesdays
5. In process of publishing first issue
6. Larry Wayne Brown, president
7. (713) 693-5748
8. $5 per semester or $10 per year
9. APL committee (8080); BASIC committee (6800); hardware and software tutorials; Micro Expo '79.
10. Micro Expo '79 to be held March 2, 3, and 4 1979 in the Memorial Student Center of Texas A&M University.

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1. Alamo Computer Enthusiasts
2. 7517 Jonquill
San Antonio TX 78233
3. Room 104, Chapman Graduate Center, Trinity University
4. Fourth Friday of every month
5. *Alamo Computer Enthusiast*
6. John R Stanton
7. (512) 657-3069
8. $2 per year subscription
9. All areas.

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1. Northside Computer Group
2. 5819 Brenda
San Antonio TX 78240
6. John McClenny Jr
8. No dues
9. 6800, 6809, 6502 microprocessors, bipolar bit slices. Projects include 256 by 256 motion graphics; super cheap voice synthesis, making all our software ROMable; flight simulator program.

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1. Permian Basin Computer Group
2. Data Processing Dept
c/o Ector County Schools
POB 3912
Odessa TX 79760
3. Midland chapter: Student Center, Midland College
Odessa chapter: Elect Tech Bldg, Rm 203, Odessa College
4. Midland chapter: Second Monday each month at 7:30 PM
Odessa chapter: Second Saturday each month at 1 PM
5. None
6. John Rabenaldt
7. Midland: (915) 697-4607 after 6 PM
Odessa: (915) 332-9151 ext 43 weekdays
8. None
9. Comsumer (home) computers; home-built computers; color graphics; floppy disk systems; Selectric typewriter interfaces.

Zips 80000 - 90000

1. Southern Nevada Personal Computing Society (SNPCS)
2. 1405 Lucilee St
Las Vegas NV 89101
3. Clark County Community College Cheyenne Campus, Room 1062
4. 12 noon, second Saturday each month
5. *HARD COPY* (monthly)
6. Edna H Wells, secretary
7. (702) 642-0212
8. Individual, $12 per year; family $18 per year; student $3 per year
9. Our primary purpose is to assist each other in making informed decisions when buying computers, accessories and software.
10. We have (May 78) 54 members with widely varied technical backgrounds.

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1. Northern Nevada Computer Club
2. c/o UNSCC
POB 9068
Reno NV 89507
3. University of Nevada Computing Center
4. 8 PM, second Wednesday, September thru May
5. None
6. Al Brady
7. (702) 784-4008
8. None
9. Information exchange for small computers.

The listings follow this form:

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

Clubs and Newsletters

Zips 90000 - 99999

1. Glendale College Computer Club
2. 1500 N Verdugo Rd
   Glendale CA 91208
3. Glendale College
6. R Unterman
7. (212) 240-1000 ext 200
8. $2 per year

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1. Compucolor-Intecolor Users Group
2. 5250 Van Nuys Blvd
   Van Nuys CA 91401
3. Same as above
5. Bimonthly
6. Stan Pro
7. (213) 788-8850
8. $15 first year
9. Business programs; game programs; interfacing to other systems; special uses and interfaces to machines.
10. Program interchange.

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1. San Diego Computer Society
2. POB 9988
   San Diego CA 92109
5. Yes
8. $4 membership donation; $6 newsletter subscription
9. The San Diego Computer Society is a nonprofit, tax exempt corporation whose purpose is to provide its members and the general public with a useful source of computer related information.
10. Write to above address for membership application.

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1. Homebrew Computer Club
2. POB 626
   Mountain View CA 94042
3. Stanford Linear Accelerator Center and Sherman Fairchild Medical Center
4. Printed in newsletter
5. *Homebrew Computer Club Newsletter*
6. Robert Reiling
7. (415) 967-6754 after 7 PM
8. Donation of $10 to $12 per year requested to pay meeting and newsletter costs.
10. A sample *Homebrew Computer Club Newsletter*, listing meeting dates and location, may be obtained by sending an SASE to the *Homebrew Computer Club Newsletter* at the above address.

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1. The Apple Core
2. POB 4816
   Main Post Office
   San Francisco CA 94101
5. Yes
6. Scot Kamins
8. To be determined
10. To qualify as a member, you must own or regularly use an Apple in any memory configuration.

DIRECTORY, continued

1. Bay Area Microprocessor Users Group (BAMUG)
2. 1211 Santa Clara Av
   Alameda CA 94501
3. 1450 53rd St, Emeryville CA
4. First Thursday of each month
5. *Bay Area Microprocessor Users Group Newsletter*
6. Timothy O'Hare
7. (415) 523-7396
8. Donations; no dues or fees required.
9. The club is open to all interested persons. It has an education forum every month with guest speakers to enlarge computer knowledge.
10. The club also has a software library, group buys on equipment and a swap meet at every meeting.

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1. Diablo Professional Users Group
2. c/o R J Hendrickson
   321 Golf Club Rd
   Pleasant Hill CA 94523
3. Library conference room, Diablo Valley College
4. Fourth Wednesday of each month
5. Meeting minutes constitute the newsletter
6. R J Hendrickson
7. (415) 687-8373
8. None
9. Professional applications of personal computer systems. Meetings are comprised of speakers, demonstrations and random access sessions.

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1. 6800 Computer Club
2. POB 18081
   San Jose CA 95158
3. University of Santa Clara
4. First Tuesday of each month
5. None
6. Ray Boaz
7. (408) 269-9522
8. None
9. Everything on hardware and software for all 6800 systems.
10. For 6800 users we provide the place to exchange software, discuss problems, find solutions to problems, evaluate vendors, use limited

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>
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> 7. Contact phone number
> 8. Dues or subscription fees
> 9. Special interests
> 10. Other comments

group buying power and exchange information on home computer news and events. We have a software library with programs on tape (KCS) at cost of reproduction and tape. All inquiries are answered when time permits.

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1. Sacramento Microcomputer Users Group (SMUG)
2. POB 161513
   Sacramento CA 95816
3. SMUD Training Facilities, 59th St
4. Fourth Tuesday of each month, 7:30 PM
5. *Push & POP*
8. $6 per year
9. PET and SOL workshops
10. Please write SMUG at the address above with all meeting, membership and other questions.

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1. Aloha Computer Club Inc
2. POB 4470
   Honolulu HI 96813
3. Leeward Community College
4. First Wednesday of each month, groups at 6:30 PM, and meeting at 8 PM
5. *De Buggo*
6. Bob Holz
(808) 455-0271 or 455-4854
8. er year
9. (/M, Heath, 6800, and PCNET.

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1. Portland Computer Society
'. 4032 SE Grant C
   Portland OR 97214
Varies
Social: First Thursday of each month; Business: Third Wednesday and Saturday of each month.
5. *PCS1976*
6. Percy G Wood
7. (503) 235-9641
8. $10 per year
9. Language Theory SIG.

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1. Northwest Computer Society
2. POB 4193
   Seattle WA 98104
3. Pacific Science Center
4. First and third Thursday of each month
5. *Northwest Computer News*
7. (206) 284-6109 (message)
8. $7 per year
9. Timeshare at 50 cents per hour, annual computer fair in April and software contests
10. First meeting of each month we have guest speaker of demonstration; second meeting of each month is an open forum. News circulation is 1000.

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1. Apple Core Computer Club
2. 220 N 2nd St #17
   Yakima WA 98901
3. J M Perry Institute
   2011 W Washington Av
5. None: monthly notification of meeting to members.
6. Jerry P Starzinski, president or Russell Miller, secretary
7. (509) 452-2540 (after 6 PM), 453-7169 (8 AM to 5 PM), respectively
8. $5 per year
9. Many members have SwTPC 6800 systems. Lively trade of information and programs. Presently have eight working systems, three being build. Some members going into 8080s and others.
10. Club celebrated first anniversary May 25 1978 and has grown from eight founding members to a present membership of thirty. Lots of new and exciting projects in the planning stages.

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1. Anchorage Computer Group
2. 364 H 6th St
   Ft Richardson AK 99505
3. Time and place to be determined
4. Monthly date to be determined.
6. Constantine T Papas
7. (907) 862-1238
9. Assistance to the novice home computerist.

FOREIGN and INTERNATIONAL CLUBS and NEWLETTERS

1. Microcomputers in Psychiatry
2. 26 Trumbull St
   New Haven CT 06511
3. none
5. *Microcomputers in Psychiatry*
6. Marc D Schwarz MD
7. (203) 562-9872
8. $6 per year
9. A bimonthly newsletter for mental health professionals interested in sharing experiences and ideas about the use of computers in the field. Includes information on subscribers' uses of computers for psychiatric testing, history testing, therapy, research and simulations. Also includes reviews and notices of commercially available hardware and software for use in a mental health setting.

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1. Transaction
2. POB 461
   Philipsburg PA 16866
5. *Transaction*
8. $3 per year
9. Users group and newsletter for PET owners.

1. KIM-1/6502 User Group
2. 109 Centre Av
   Norristown PA 19401
5. *KIM-1/6502 User Notes*
6. Eric C Rehnke
7. (215) 631-9335
8. $5 for six issues
9. A communication medium for KIM users
10. Around 2000 members worldwide.

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1. Buss
2. 325 Pennsylvania Av SE
   Washington DC 20003
3. none
5. *Buss: The Independent Newsletter of Heath Company Computers*
6. Charles Floto, editor
8. $7 for 12 issues
9. Software and hardware compatible with H8, H11, or ET-3400.
10. Sample issue available upon request mentioning BYTE.

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1. TRS-80 Users Group
2. 7554 Southgate Rd
   Fayetteville NC 28304
3. Our group is international so we do not have meetings.
5. *TRS-80 Users Group Newsletter*
6. R Gordon Lloyd
7. (919) 867-5822
8. $10 per year (ten newsletters, 20 pages per issue)
9. Radio Shack TRS-80 computer, programs for the TRS-80, and interfacing the TRS-80 to the outside world.

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1. SR-52 Users Club
2. 9459 Taylorsville Rd
   Dayton OH 45424
3. None
5. *52-Notes*
6. Richard C Vanderburgh
8. $1 per issue of *52-Notes*; back issues start June 1976.
10. *52-Notes*: style and technical level are aimed at individuals with above average intelligence and attention span, but whose formal education may have ended with high school. Scope is all of the Texas Instruments personal programmable calculators. Coverage of the TI-58/59 machines began June 1977. The SR-52 Users Club is a national/international group.

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1. Personal Computing Society
2. c/o James White

The listings follow this form:

1. Name of organization
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6. Contact person
7. Contact phone number
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9. Special interests
10. Other comments

Clubs and Newsletters

1202 Riverview Ln
Watertown WI 53094
5. Soon to be announced
6. Richard A Kuzmack
7. (703) 821-2873 (evenings)
9. The Society's communications objectives will include publication of a newsletter for computer clubs and a club directory. Surveys will be conducted and published to share information on matters of interest to computer enthusiasts. PCS will foster the development of standards such as those necessary to the operation of a personal computer communications network.
10. This national organization was recently formed to facilitate noncommercial applications of computer technology. It will foster communication and coordination among the numerous computer clubs and individuals in the personal computing community. The board of directors of PCS are: Charles Floto, Washington DC; Richard Kuzmack, McLean VA; Sol Libes, Scotch Plains NJ; Larry Press, Santa Monica CA; Jim Rarus, E Detroit MI; Robert Reiling, Mountain View CA; Gifford Toole, Mississauga, Ontario CANADA; M D Turner, Austin TX; and James White, Watertown WI.

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1. Theater Computer Users Group
2. 104 N St Mary
Dallas TX 75214
3. Assorted conventions of other groups (USITT, ATA)
4. Random
5. *TCUG Newsletter*
6. Mike Firth
7. (214) 827-7734
8. $4 per year
9. Uses of computers of any size, but particularly small ones, in any aspect of producing live drama, including lighting control, ticket management, bookkeeping, inventory, costing, research.
10. A national organization created to share data in a specific area.

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1. Association of Small Computer Users
2. 75 Manhattan Dr
Boulder CO 80303
5. *Interactive Computing, Minicomputer News* and *Datapro Feature Reports*
8. $25 per year
9. The Association of Small Computer Users is a nationwide professional organization devoted to providing an unbiased source of user oriented information on mini and microcomputers for business and scientific applications. It is organized as a nonprofit association to represent and serve small computer users and to provide a forum for the ex-

DIRECTORY, continued

change of information among small computer users.

1. Robot Builder
2. 208 Via Colorin
   Palos Verdes Estates CA 90274
3. none
5. *Robot Builder*
6. Michael Westvig
7. (213) 378-0580
8. $6 per year (bimonthly), $12 overseas, beginning with volume 2, number 1, January 1979.

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1. Computer Information Organization Inc
2. POB 158
   San Luis Rey CA 92068
3. Publishing only
5. *Radio Shack Computing, Low-Cost Word Processing* and *S-100 Bus Computer User Notes*
6. Bill McLaughlin, editor
7. (714) 757-4849
8. *Radio Shack* $10 for 12 issues, *S-100* $5 for six issues and *Word Processing* $12.95 for 12 issues
9. Real uses of computers: either business, home, education, small or large organization
10. *Word Processing* newsletter is developing interfaces to ordinary electric typewriters, to Selectric, Olivetti and other single element typewriters, to Friden and other special machines.

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1. PPC
2. 2541 W Camden Pl
   Santa Ana CA 92704
5. *PPC Journal*
6. Richard J Nelson, publisher
8. $15 per year
9. To share programs, techniques, news, etc, for HP PPCs.
10. Six chapters at present: Cincinnati/Dayton, Chicago, Washington DC, Albuquerque, Orange County and NE Iowa Chapters. Nearly 2000 members in 35 countries. Started June 1974. For more information send 9 by 12 inch SASE (2 oz postage attached) to above address.

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10. Other comments

1. Calculator Lib: The Liberated Calculator Users Club
2. POB 2151
Oxnard CA 93034
3. Ventura County (we do not have a permanent meeting address yet)
5. Quarterly club activity report and the irregularly published newsletter *Calculator Lib*
6. Gene Hegedus
7. (805) 486-7191
8. Yearly membership dues of the non-profit club is $6 which includes the quarterly reports. The irregularly published newsletter *Calculator Lib* is $2.75 per issue postpaid.
9. This global club (with members on three continents) is the first to serve the interests of all calculator users, regardless of the make of their machines. It is dedicated to exploring the limits of the state of the art of calculator mathematical techniques.
10. The club presently is in a formative stage, having been organized on requests of *Calculator Lib* readers and therefore presently we need members who will volunteer as officers of the club, working on the editorial committee (for the quarterly report) as correspondents, reporters, etc (all this with the understanding that no salaries will be paid). The operation and future action of the club depends upon the interest, ability and resources of the individual members. More information on The Liberated Calculator User's Club is available for a (#10) SASE from Gene Hegedus, Calculator Lib, POB 2151, Oxnard CA 93034.

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1. Computer Faire
2. POB 1579
Palo Alto CA 94302
3. Varies
4. Varies
5. *Silicon Gulch Gazette* (a randomly published 4 to 20 page newspaper)
6. Jim Warren
7. (415) 851-7075
8. None
9. Intelligent machines for home, business and industry

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1. SOLUS, The Sol User's Society
2. POB 23471
San Jose CA 95153
3. Local chapters in various cities across the country
5. *SOLUS News*
8. $10 (US dollars only) in USA, Canada and Mexico; $15 (US dollars only) elsewhere
9. To facilitate exchange of information and software among owners of Processor Technology Sol Computer Systems (or other computers with VDM and CUTS or HELIOS), to review hardware and software products tested for Sol compatibility and consumer advocate.
10. We maintain a cooperative but independent relationship with the manufacturer. Send $1 for sample issue of newsletter.

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1. HEX Users Group
2. 36012 Military Rd S
Auburn WA 98002
3. None: correspondence only
5. *HEX Newsletter*
6. Charles C Worstell
7. (206) 927-6038 (Tacoma WA)
8. First time send SASE; $4 for next seven issues of newsletter which is irregular.
9. Low cost, effective system without ASCII keyboard; Motorola 6800 EVK/II kit is most popular.
10. Have monitor system to use BASIC on original 24 key keyboard of Motorola 6800 EVK/II.

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1. Société d'Informatique Amateur du Québec
2. C P 9242
Sainte-Foy, PQ
CANADA G1V 4B1
3. Pav Vachon, Salle 3870, Univ Laval
4. Second Monday of each month at 7:30 PM
5. *La Routine*
6. Gilles Paillard, secretary
7. (418) 871-1960
8. Nonstudent $20, student $15 or journal only $10
10. Activities for current year cease in June with election of new officers, and resume in September.

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1. Ottawa Computer Group
2. POB 13218
Kanata Ontario
CANADA K2K 1X4
3. National Research Council Auditorium, 100 Sussex Dr, Ottawa Ontario CANADA
4. First Monday of each month, 8 PM
5. *OCG Newsletter*
6. W Mitchell, secretary
7. (613) 596-2287
8. $5 per year and $5 initiation fee.

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1. Association of Computer Experimenters (ACE)
2. c/o Ken Bevis, 220 Cherry Post Dr
Mississaliga, Ontario
CANADA L5A 1H9
3. Hamilton, Ontario CANADA
5. *Ipso Facto*
6. Bernie Murphy, editor, 102 McCraney St, Oakville Ontario, CANADA L6H 1H6
7. Tentatively $10
8. Microcomputers, peripherals and software in general, with RCA-1802

microprocessor and software in particular.
9. The ACE club started in September 1977 and has about 450 members from across the US and Canada.

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1. Toronto Region Association of Computer Enthusiasts (TRACE)
2. POB 545, Streetsville, Ontario CANADA L5M 2C1
3. North Campus, Humber College, room J209 and Ontario Science Centre, lecture hall C
4. Fourth Friday of each month, 8 PM and second Sunday of each month, 2 PM, respectively
5. *TRACE Newsletter*
6. Ross Cooling, president
7. (416) 488-3314
8. $15 per year or $7 per year newsletter only.

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1. Kitchener-Waterloo Microcomputer Club
2. E2-3354 Electrical Engineering Dept, University of Waterloo Waterloo, Ontario CANADA N2L 3G1
3. Engineering 4, room 3388, University of Waterloo
4. First Wednesday of each month, 7:30 PM
5. None
6. Roger K Sanderson
7. (519) 579-6445 (home) or 885-1211 ext 3815 (work)
8. None
9. We hold very informal meetings for the purpose of getting people with similar interests together. We also have a small dedicated group of regulars who are doing interesting hardware and software development.

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1. West Coast Computer Society
2. POB 4476 Vancouver BC CANADA
3. British Columbia Institute of Technology, room D412
4. First Wednesday of each month at 8 PM (no meetings July and August)
5. *Print Out*
6. Peter Luckham
7. (604) 522-3484
8. $15 per year
9. Personal computing.

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7. Contact phone number
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10. Other comments

Clubs and Newsletters

1. Microcomputer Encounter Group
2. 207-885 Old Esquimalt Rd
   Victoria BC
   CANADA V9A 4W9
6. Varghese Cherian, secretary
9. Exchanging information and ideas.

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1. Amateur Computer Club
2. 7 Dordells
   Basildon, Essex
   ENGLAND
5. Six times a year
6. Mike Lord
7. (0268) 4 11125
8. £2 PA or $4 (US currency)

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1. Hobby Computer Club
2. Delftsekade 12
   2266 A J Leidschendam
   NETHERLANDS
3. Several towns in Belgium and the Netherlands.
4. Usually once each month
5. *Hobby Computer Club Nieuwsbrief* (Dutch), bimonthly
6. Dick Barnhoorn
7. Netherlands 070-273537
8. Netherlands: 15 Guilder; Belgium: 225 Franc
9. No bias to any system or microprocessor
10. Membership passed 800 in May 1978. Hardware service (cheap parts and reductions) and software library started in January 1978. HCC Computer Day in October. We're taking part in several large scale exhibitions to promote the concept of personal computing.

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1. Japan Microcomputer Club
2. Kikaishinko-kaikan, JEIDA
   5-5-8, Shiba-koen, Minato-ku
   Tokyo JAPAN
3. Same as above
4. Twice a month
5. *Micom* (Japanese version), *Micom Circular* (Japanese version), *Micro Computer News* (English version)
6. Koji Yada, editor
7. 03-438-1869
8. Y6,000 per year
9. All aspects of hobbyist computers for persons in Japan.■

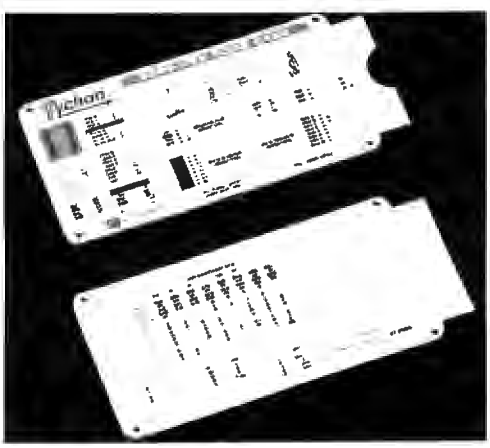
The listings follow this form:

1. Name of organization
2. Mailing address
3. Meeting location
4. Meeting algorithm
5. Newsletter or publication
6. Contact person
7. Contact phone number
8. Dues or subscription fees
9. Special interests
10. Other comments

Book Reviews

The 8080 Programmer's Pocket Guide
Scelbi Computer Consulting Co
Milford CT 06460
$2.95

Tychon 8080 Hex Code Card
by Tychon Inc
POB 242, Blacksburg VA 24060
$2.95



At first it might seem odd to review the *8080 Programmer's Pocket Guide* and the 8080 Hex Code Card at the same time, but they both serve as quick references for 8080 assembler programming and hand assembly of the resulting programs. Either one alone is a great improvement over thumbing through the appendices of larger books; ideally you should have both.

The 8080 Programmer's Pocket Guide is a small booklet (4.5 by 3.5 inches, 11.5 by 9 cm) intended as a quick reference to the 8080 instruction set. It has three sections. The first is a discussion of each instruction in the set describing what it does, what flags it affects, and the octal and hexadecimal values for it. The second part is a discussion of a program for loading Intel hexadecimal format paper tapes. The third section is a summary of the instruction set ordered by function. This gives the instruction, its octal and hexadecimal values, the number of cycle states, and the page on which the instruction is discussed.

I find this booklet very useful. There is, however, one minor blemish that may confuse some users. Parts of the booklet are adapted from Scelbi's *8080 Software Gourmet Guide and Cookbook*. This cookbook, like previous Scelbi publications, uses a set of mnemonics which were based on those for the 8008. Scelbi has since changed over to the standard Intel 8080 mnemonics, and they use the standard ones throughout the pocket guide. However, some of the discussions taken from the previous book still use the old mnemonics (eg: LBA rather than MOV B, A). Also, the text occasionally refers to appendices from the cookbook. But these are minor problems; the booklet is well worth having.

Tychon's 8080 Hex Code Card (15 by 8 cm) is a slide rule type summary of the 8080 instruction set. Also available is a card for those who prefer octal. The front of the card gives all the instructions and their hexadecimal values, and tells how each instruction affects the flags. The back of the card gives an ASCII chart, a hexadecimal to binary conversion chart, a chart of the register pairs, and one of the flag byte. The card itself is made of fairly heavyweight cardboard. If Tychon ever puts a plastic card out I'll be among the first to buy it, since the present card is used so much that I may wear it out. If you ever hand assemble programs for the 8080, I highly recommend this card.

John A Lehman
716 Hutchins #2
Ann Arbor MI 48103 ■

Languages Forum

Making an H9 Understand Lower Case

George J Frye
Frye Electronics Inc
POB 23391
9826 SW Tigard St
Tigard OR 97223

We have been using the Heathkit LSI-11 computer as supplied with their model H9 CRT terminal and recently ran into an interesting problem. Source programs that included lower case alphabetical ASCII characters would not read out on the terminal in an intelligible way; the 64 character generator just went bananas and interpreted these lower case characters as slashes, percent signs, etc.

I have also noted that some other devices, such as the Practical Automation DMTP-6-uP Printer, also use 64 character sets, and may be faced with the same problem.

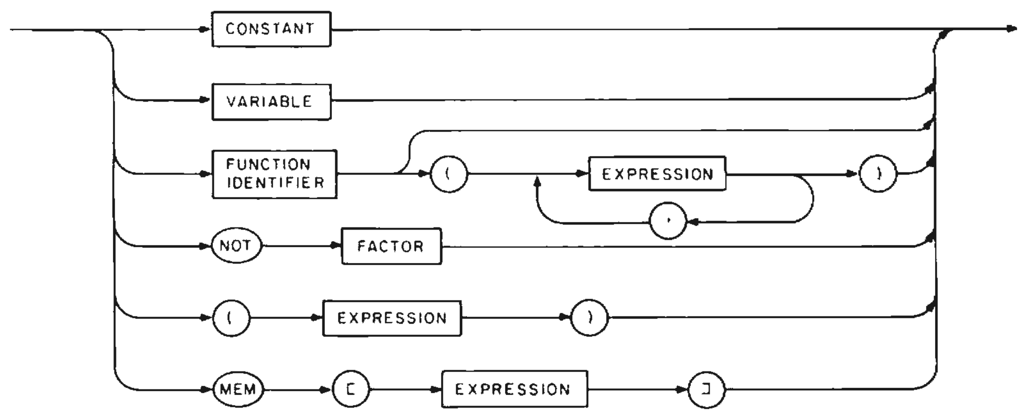
The Heath terminal is easily modified so that both upper and lower case alphabetical characters read out as upper case. (Some form of this modification may also work with the above printer.)

Heath feeds the character generator chip, IC205, with a 6 bit signal latched through from the ASCII bus. The most significant data line is latched onto the character generator board but not run to IC205. A bit of study will show that changing the drive to the most significant bit of IC205 from ASCII bus line 6 to an inverted ASCII bus line 7 will cause the character generator to recognize lower case and upper case alpha characters as upper case (Tektronix uses this trick in their display terminals).

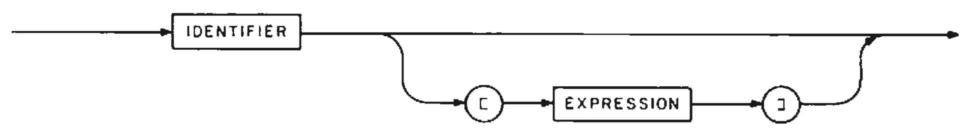
The modification is easily done by cutting the run from pin 15 of IC203 (bit 6) to pin 1 of IC206, soldering in a wire from pin 10 of IC203 (bit 7) to pin 11 of IC219, and soldering in another wire from pin 10 of IC219 to pin 1 of IC206. IC219 is a hexadecimal inverter, and the pins 10 and 11 are the output and input of an unused section of this IC.■

Continued from page 65

FACTOR



VARIABLE



CONSTANT

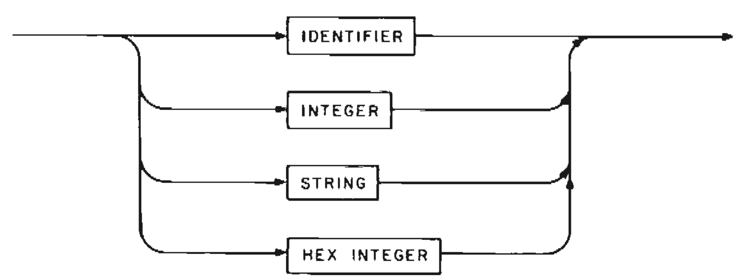


Figure 3, continued: Notice that some of the diagrams, for example FACTOR, contain themselves in their own definitions. This is known as a recursive definition.

For instance:

mem [i]:=mem[j];

reads the byte from the memory location *j* and writes it back to memory location *i*. Machine language subroutines can be called from Pascal programs. The statement:

Call (i);

can be used to make a call to memory address *i*.

The P-Machine

The p-machine is a stack oriented machine consisting of four registers and two memory storage areas. Memory is separated into program storage and data storage areas. The program storage area contains the program codes (p-codes), and remains unchanged during program execution. The data storage area contains the values of variables. It is also used to store temporary values during arithmetical and logical operations.

Though the variables can be fetched and stored in a random fashion, the data storage area operates as a stack with respect to arithmetical and logical operations and runtime storage allocation. Arithmetical and logical operations are done on the top elements of the stack, and the results of the operations are pushed back on the stack. In this respect, one might call it a zero address machine, since operations (except store and load instructions, which must specify an address) are done without reference to any address. Later we will discuss the use of the stack during runtime storage allocation.

STATEMENT

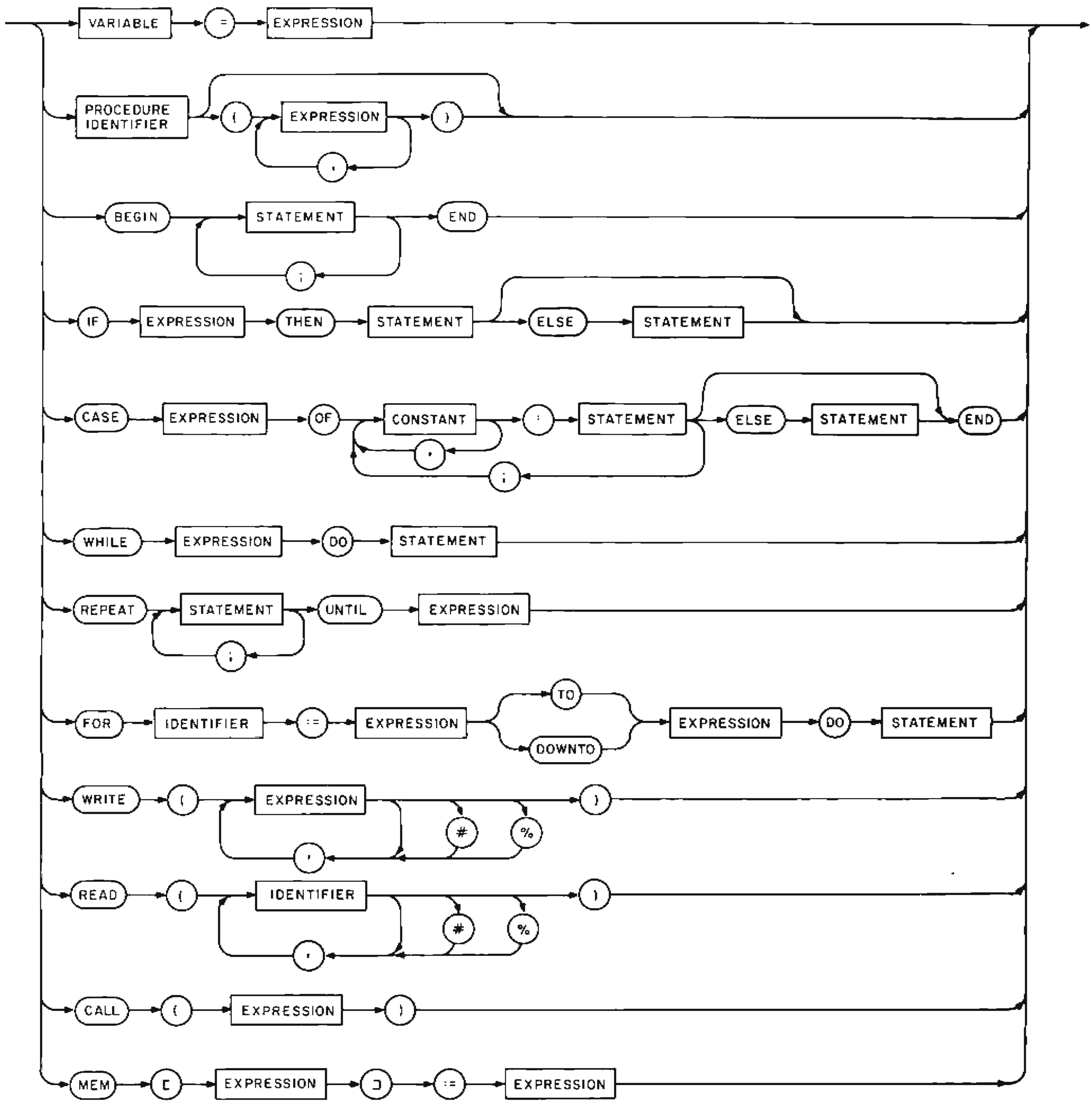


Figure 3, continued.

The four registers in the p-machine are the program counter, P, which points to the next executable instruction in the program storage; the instruction register, I, which contains the current execution instruction; the stack pointer, T, which points to the top of the stack, and the base address register, B, which contains the current base address. The functions of the first three registers should be quite clear from the above discussion. The function of register B will become clear after we discuss storage allocation.

Each variable in a Pascal procedure has a scope and lifetime. The scope of a variable is the range within which it can be referenced. The scope of a Pascal variable is simply the procedure block to which it belongs. The lifetime of a variable is from the time storage is allocated for it to the time storage is disallocated. In Pascal, this is the time the procedure defining the variable is activated to the time a return is executed by the procedure. This is different from the way variables are treated in BASIC, where the scope of a variable is the entire program and its lifetime the entire execution time.

Since procedure activation is strictly a first in, last out process, the use of stack is an appropriate strategy. When a procedure is activated, storage for its local variables is allocated on the top of the stack, and is disallocated when the procedure is terminated. Thus the stack contains all the variables of the currently active procedures. The variables of the last activated procedure are on the top of the stack, those of the second to last activated procedure next to it, and so on.

Since storage allocation is not static, addresses cannot be assigned at compile time, but must be calculated at runtime. The base register, B, always points to the starting location of the segment of the data block in the stack. The addresses generated by the compiler are not absolute addresses, but displacements from some base addresses. If the variable is local, then its address is the displacement from the current base register B; but if the variable is from an outer procedure, then the base address for that procedure should be calculated, and added to the displacement.

To do this, and to ensure proper procedure or function linkage, extra storage is allocated on the stack when a procedure is activated. Figure 4 shows the various quantities present in each of the procedure blocks. The function return value is used only for function calls, and storage is allocated for any parameters needed by the procedure or function. The base address contains the value of the current base register B, and the return address contains the program return address at the place of the call. The functions of the dynamic linkage and the static linkage need further explanation.

The dynamic linkage forms a chain that reflects the procedure activation history. It points back to the base address of the procedure that was activated immediately before this one. For instance, if procedure A calls procedure B, which calls procedure C, then the dynamic link chain points from C to B, and then to A. It is used to ensure that the program returns to its previous state when exiting a procedure. In particular, the base register B must be loaded with the correct base address of the calling procedure. This would be easy to do if we follow a step through the dynamic link chain.

The static link, on the other hand, reflects the static hierarchical structure of the procedures. Each active procedure has a link that points to the procedure (also active) that immediately contains it. The static links actually form a tree, with the

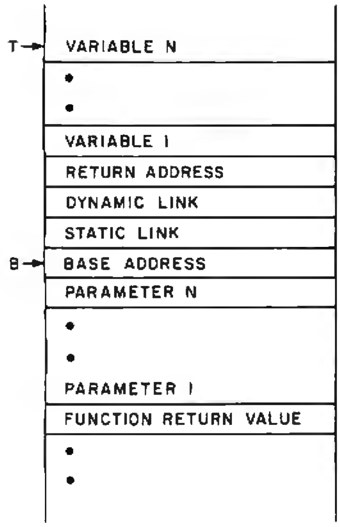


Figure 4: A typical activation record for a function. For a procedure, the function return value is omitted. Note that the procedure and function parameters, as well as the function return value, are below the base register B, and thus would have negative displacements.

main program block as the root. These links, which in general are different from the dynamic links, are used to let programs have access to the correct base address of the variables in an outer procedure, since at compiler time, only the static relationship among the procedures are known. The compiler therefore generates the pair (static level difference, relative displacement from the base address) as addresses for variables. The calculation of the addresses from these pairs would presumably slow down the process, but it is a small price to pay for nice features like recursive procedure calls.

Op Code (Hexadecimal)	Mnemonic		Operation
00	LIT	0,n	load literal constant
01	OPR	0,n	arithmetic or logical operation
02	LOD	v,d	load variable
12	LODX	v,d	load indexed variable
03	STO	v,d	store variable
13	STOX	v,d	store indexed variable
04	CAL	v,a	call procedure or function
05	INT	0,n	increment stack pointer
06	JMP	0,a	jump unconditional
07	JPC	c,a	jump conditional
08	CSP	0,n	call standard procedure

Table 1: Basic p-codes. The v in call, load and store instructions is the difference in static level between the current procedure and the one being called or the one which contains the variable from the base address. An address in a p-code program is shown by a. The condition code, c, can either be 0 or 1.

The P-Codes

The p-machine has only 11 basic instructions, which are listed in table 1. For the sake of simplicity and easy handling in this version of the implementation, all instructions are four bytes long. The contents of the four bytes are as follows:

byte 1: op — the operation code.
byte 2: can be (i) v — static level difference.
or (ii) c - condition code in a jump instruction.
or (iii) 255 — denotes absolute addressing.
or (iv) not used for some instructions.
bytes 3,4: can be (i) d - displacement from the base address.
or (ii) n - numeric constant.
or (iii) a — address in the p-code program.

The OPR (arithmetic and logical operations) and CSP (call standard procedure) are further subdivided into more instructions. The complete set of instruction mnemonics and operations is listed in table 2. The LODX and STOX instructions are used to load and store array elements with the value of the array subscript on top of the stack. The call standard procedure (CSP) instruction is primarily used for input and output (IO) operations. Besides the basic function of inputting and outputting single characters, additional procedures have been implemented to relieve the user from writing IO conversion routines in Pascal for numeric and hexadecimal numbers. In the future, more procedures can be added to handle the input and output of other data types such as floating point numbers and file records for tape or disk. Meanwhile these seven instructions are sufficient for convenient use in writing the bootstrap compiler and its related software.

Readers are urged to read the p-code interpreter listing which simulates the operations of the p-machine. The program statements are straightforward and self-explanatory. Familiarity with the p-machine instruction set is essential in understanding the code generation part of the p-compiler.

The P-Code Interpreter

Since the p-machine is a hypothetical computer, there has to be some method of executing the p-codes generated by the compiler. There are two simple solutions to this problem. One is to write an interpreter which can decode and execute the p-codes. The other solution is to write a translator which can decode the p-codes and output equivalent executable machine codes for an existing computer. Both methods have been used in our compiler system. The first method, although it runs slower, is good for developing programs because many debugging facilities can be implemented in the interpreter. The second method is good for production programs which may need faster execution speed. A p-code to 8080 machine code translator will be described in part 3 of this series.

The p-code interpreter is made up of two major modules:

- Main program.
- Procedure which simulates the p-machine.

Every call to the simulator will execute one p-machine instruction. Each p-machine instruction cycle can be divided into four stages:

- Fetch a p-code from memory.
- Increment the program counter.
- Decode the instruction.
- Execute the instruction.

Several global variables are used to hold the values of the p-machine registers such as program counter, stack pointer, current instruction, etc. A one-dimensional array represents the data stack. Functional operations of the various p-machine instructions are coded directly from the instruction set defined in table 2. The main program simply initializes the program counter to zero and then calls the simulator repeatedly to simulate machine execution. This sounds simple but not useful, because the user has no control of the program during execution until it terminates.

In order to enable user control of an executing p-code program, the main program must accept commands from the user which instruct it to call the simulator a specified

G: *go* — Set program counter to zero; initialize other counters; start execution.
S: *single-step* — Execute one p-code; display the mnemonics of the next p-code pointed by the updated program counter.
R: *run/restart* — Start execution from current program counter until the program ends or a breakpoint is reached. This command is used to continue execution at a breakpoint.
B: *set breakpoint* — A p-code address is entered as a breakpoint after the interpreter prompts with a ?. Up to five breakpoints may be set.
C: *clear* — All breakpoints previously set are cleared.
Y: *display breakpoint* — Display the breakpoints already set.
X: *examine status* — Display the values of: current program counter, base address, stack pointer, the top two elements of the stack.
K: *stack content* — A value is entered as the stack pointer after the interpreter prompts with a ?. It will then display the values of six stack elements starting from this stack pointer.
T: *trace* — Display the address and mnemonics of the 16 p-codes last executed. This command is usually applied at a breakpoint. It is used for tracing the logic flow of the program.
E: *examine program* — A p-code address is entered as a display pointer (DP) after the interpreter prompts with a ?. It will then display the mnemonics of the p-code at this address. This command and the U and N commands are used for examining the p-codes anywhere in the program without altering the current program counter.
U: *up* — Decrement the display pointer by one and display the mnemonics of the p-code pointed by it.
N: *next* — Increment the display pointer by one and display the mnemonics of the p-code pointed by it.
Q: *quit* Terminate the interpreter program and return to operating system.

Table 3: Interpreter commands. All commands for the p-code interpreter are single characters. A command is entered after the interpreter prompts the user with a > on the video display. Additional information is needed for some commands such as breakpoint and stack addresses. On entry to the interpreter it will ask for the starting memory address of p-codes and initialize the program counter to zero. On exit it will display the number of p-codes executed.

Mnemonic	Description	Mnemonic	Description
LIT 0, n	load literal constant	OPR 0,20	decrement (sp) by 1
OPR 0, 0	procedure return	OPR 0,21	copy (sp) to (sp+1)
OPR 0, 1	negate (sp)	LOD v,d	load a word
OPR 0, 2	add (sp) to (sp−1)	LOD 255,0	load a byte from absolute address (sp)
OPR 0, 3	subtract (sp) from (sp−1)	LODX v,d	load a word with index address (sp)
OPR 0, 4	multiply (sp−1) by (sp)	STO v,d	store a word
OPR 0, 5	divide (sp−1) by (sp)	STO 255,0	store a byte to absolute address (sp−1)
OPR 0, 6	low order bit of (sp)	STOX v,d	store a word with index address (sp)
OPR 0, 7	(sp−1) modulo (sp)	CAL v,a	procedure call
OPR 0, 8	test for (sp−1)=(sp)	CAL 255,0	call procedure at absolute address (sp)
OPR 0, 9	test for (sp−1)<>(sp)	INT 0,n	increment sp by n
OPR 0,10	test for (sp−1)<(sp)	JMP 0,a	jump to location a
OPR 0,11	test for (sp−1)>=(sp)	JPC 0,a	jump to location a if low order bit (sp)=0
OPR 0,12	test for (sp−1)>(sp)	JPC 1,a	jump to location a if low order bit (sp)=1
OPR 0,13	test for (sp−1)<=(sp)	CSP 0,0	input 1 character
OPR 0,14	logical (sp−1) OR (sp)	CSP 0,1	output 1 character
OPR 0,15	logical (sp−1) and (sp)	CSP 0,2	input an integer
OPR 0,16	logical NOT of (sp)	CSP 0,3	output an integer
OPR 0,17	shift left (sp) logical	CSP 0,4	input a hexadecimal number
OPR 0,18	shift right (sp) logical	CSP 0,5	output a hexadecimal number
OPR 0,19	increment (sp) by 1	CSP 0,8	output a string

Table 2: The p-machine instruction set. The stack pointer, sp, points to the top element of the stack. The content of the stack element is represented by (sp). The operands of the OPR instructions are replaced by their results on the stack. The result of the six relational operations is 1 if the test is true and 0 if false. With the exception of single operand OPR instructions, all instructions adjust the stack pointer, sp, after execution.

North Star BASIC

A brief summary of North Star BASIC (version 6, release 3) is given for readers not familiar with its particular features.

Variable names are one or two characters long: an alphabetical character followed optionally by a decimal digit. There are four types of variables: numeric, string, array of numeric, and function. The string variables are names postfixed by a dollar sign $, while function names are prefixed by FN. Functions (and the parameters) are defined by the declaration DEF, and ended by FNEND (for multiline function). The parameters in the function definition are local to the function, and would not affect variables in the calling program.

Strings cannot be dimensioned. The DIM declarations for strings declare the maximum length of the string variables, not their dimensions. The notation A$ (3, 5) denotes the substring of A$ from position 3 to 5. Thus if A$=ABCDEFG, A$ (3, 5) is the string CDE. This substring expression can be used both on the left or righthand side of an assignment statement.

Multiple statement lines are allowed. Statements within a line are separated by either colons, :, or back slashes, \.

Absolute memory locations can be accessed from BASIC programs. The function EXAM(I) returns the content of memory at address I; and the instruction FILL I, J writes a value of J into memory address I.

Another feature of North Star BASIC is its ability to read from or write to disk files. The statement OPEN #0, "FNAME" assigns disk file "FNAME" to file unit #0. A subsequent READ #0,A$ reads A$ from the disk file, and a WRITE #0,A$ writes A$ to the disk file. A built-in function TYP can be used to check the type of data to be read. It has a value of 0 when the end of file is reached.

number of times or to display register and stack contents. This is the simple idea of a debugging interpreter. The debugging aids commonly known include single step execution, set and reset of breakpoints, and display of register and stack contents. A number of these debugging facilities have been incorporated in the p-code interpreter. Table 3 shows the 13 interpreter commands and their functions. Note that the trace command is particularly useful in analyzing mysterious logic flow of a program, such as discovering the path along which a breakpoint is reached. This command is more convenient to use and much faster than single step execution. The limits on the number of breakpoints and the number of instructions traced can be changed easily in the program.

The first version of the p-code interpreter was written in BASIC. While developing the p-compiler, different constructs of Pascal statements were tested one at a time using the interpreter to verify the correctness of the p-codes generated. After the compiler was debugged, the interpreter was rewritten in Pascal. The program logic is very similar to the BASIC version. Since the program

Listing 1: Pascal source code for the p-code interpreter as output by the authors' system. This version implements all of the commands in table 3.

```
P-CODES STARTS AT 0000
WANT CODE PRINTED?N
   0 ?$P INTS
   0 ( P-CODE INTERPRETER   HY 1  3/31/78   BY  H YUEN :
   0     ( LAST MOD 4/12/78 )
   0 CONST U=15;BPLIM=5,SIZE=500,SIZE1=480.
   1 VAR Z,P,B,T,BP,P0,TP,CMD,I,L,K,STOP INTEGER.
   1       S ARRAY[SIZE] OF INTEGER.
   1       TRACE ARRAY[U] OF INTEGER.
   1       MN ARRAY[26] OF INTEGER.
   1       BREAK ARRAY[BPLIM] OF INTEGER.
   1
   1    ( IMPORTANT GLOBAL VARIABLES
   1     P PROGRAM COUNTER       B BASE POINTER
   1     T STACK POINTER        BP BREAK POINT INDEX
   1    TP TRACE STACK PTR       K INSTRUCTION COUNTER
   1     S DATA STACK            Z STARTING ADDR OF P-CODE :
   1
   1 FUNC BASE(LEV).
   1  VAR B1:INTEGER.
   2  BEGIN B1 =B;
   5   WHILE LEV>0 DO BEGIN
   9    B1:=S[B1];LEV =LEV-1 END,
  17   BASE =B1
  18  END (BASE).
  20
  20 PROC INIT,
  20  VAR I:INTEGER,
  21  BEGIN T =0,B =1,P =0;STOP =0.
  30   S[1]:=0,S[2] =0,S[3] =-1.
  40   P0:=0;TP:=U,K =0;
  46   FOR I =0 TO U DO TRACE[I] =-1
  55  END (INIT);,
  63
  63 PROC CRLF,
  63  BEGIN WRITE(13,10) END.
  70
  70 PROC EXEC;
  70  VAR X,A,L,F,IDX INTEGER,
  71  BEGIN X =P SHL 2 + Z;
  78   A =MEM[X+3] SHL 8 +MEM[X+2].
  90   TP:=TP+1,IF TP>U THEN TP =0.
 100   TRACE[TP] =P;
 103   P:=P+1;P0 =P,K =K+1.
 113   F:=MEM[X],
 116   IF F<=8 THEN IDX =0
 121    ELSE BEGIN IDX =1,F =F-16 END.
 129   CASE F OF
 130 0:BEGIN T =T+1,S[T] =A END.
 142 1: CASE A OF
 147   0 :BEGIN (RETURN)
 151         T =B-1;B =S[T+2];P =S[T+3] END,
 166   1 :S[T]:=-S[T].
 176   2 :BEGIN T:=T-1:S[T]:=S[T]+S[T+1] END,
 194   3 :BEGIN T:=T-1;S[T]:=S[T]-S[T+1] END;
 212   4 :BEGIN T =T-1:S[T] =S[T]*S[T+1] END;
 230   5 :BEGIN T:=T-1;S[T] =S[T] DIV S[T+1] END.
 248   6 :S[T] =S[T] AND 1, (TEST FOR ODD)
 259   7 :BEGIN T:=T-1.S[T] =S[T] MOD S[T+1] END.
 277   8 :BEGIN T =T-1;S[T]:=S[T]=S[T+1] END,
 295   9  BEGIN T =T-1,S[T] =S[T]<>S[T+1] END.
 313   10 BEGIN T =T-1.S[T] =S[T]<S[T+1] END.
 331   11 BEGIN T =T-1.S[T] =S[T]>=S[T+1] END.
 349   12 BEGIN T =T-1.S[T] =S[T]>S[T+1] END.
 367   13 BEGIN T =T-1,S[T] =S[T]<=S[T+1] END.
 385   14 BEGIN T =T-1,S[T] =S[T] OR S[T+1] END.
 403   15 BEGIN T =T-1.S[T] =S[T] AND S[T+1] END.
 421   16 S[T] =NOT S[T].
 431   17 BEGIN T =T-1,S[T] =S[T] SHL S[T+1] END.
 449   18 BEGIN T =T-1,S[T] =S[T] SHR S[T+1] END.
 467   19 S[T] =S[T]+1,
 478   20 S[T] =S[T]-1,
 489   21 BEGIN (COPY:
 493        T =T+1.S[T] =S[T-1] END
 503     ELSE BEGIN WRITE(' ILLEGAL OPR').CRLF.STOP =1 END
 521   END (CASE OF A).
 523 2 BEGIN (LOAD:
 527     L =MEM[X+1].
 532    IF L=255 THEN S[T] =MEM[S[T]]
 539    ELSE BEGIN IF IDX THEN A =A+S[T].
 549          T =T+1-IDX,S[T] =S[BASE(L)+A] END
 564   END,
 565 3 BEGIN (STORE;
 569    L =MEM[X+1].
 574    IF L=255 THEN BEGIN
 578     MEM[S[T-1]] =S[T];T:=T-2 END
 589    ELSE BEGIN
 590     IF IDX THEN A =S[T-1]+A;
 599     S[BASE(L)+A] =S[T];T:=T-1-IDX END
 614   END,
 615 4 BEGIN (CALL)
 619    L =MEM[X+1].
 624    IF L=255 THEN BEGIN CALL(S[T]).T =T-1 END
 635    ELSE BEGIN
 636     S[T+1] =BASE(L);S[T+2]:=B;
 649     S[T+3] =P;B =T+1;P =A END
 660   END,
 661 5 IF T>(SIZE1-A) THEN BEGIN
 671    WRITE(' STACK OVFL').CRLF,STOP =1 END
 687   ELSE T =T+A.
 693 6:P:=A; (JMP)
 700 7 BEGIN IF S[T]=MEM[X+1] THEN P:=A.   (JPC)
```

```
714     T:=T-1 END;
719  8:CASE A OF (CSP)
724    0:BEGIN T:=T+1;READ(S[T]) END;   (IN CHAR)
736    1:BEGIN WRITE(S[T]);T:=T-1 END;  (OUT CHAR)
748    2:BEGIN T:=T+1;READ(S[T]#) END;  (IN NUMBER)
760    3:BEGIN WRITE(S[T]#);T:=T-1 END;(OUT NUMBER)
772    4:BEGIN T:=T+1;READ(S[T]%) END;  (IN HEX)
784    5:BEGIN WRITE(S[T]%);T:=T-1 END;(OUT HEX)
796    8:BEGIN (OUT STRING)
800       FOR IDX:=T-S[T] TO T-1 DO WRITE(S[IDX]);
820       T:=T-S[T]-1 END
827    ELSE BEGIN WRITE(' ILLEGAL CSP');CRLF;STOP:=1 END
845    END (CASE OF A)
846  ELSE BEGIN WRITE(' ILLEGAL OPCODE');CRLF;STOP:=1 END
867   END (CASE OF F)
868  END (EXEC);
869
869  PROC CODE(PC); (PRINT CODE)
869   VAR X,N,IDX:INTEGER;
870   BEGIN X:=PC SHL 2 +Z;N:=MEM[X]*3;
882    IF N<=24 THEN IDX:=' '
887    ELSE BEGIN N:=N-48;IDX:='X' END;
895    WRITE('  ',PC#,'  ',MN[N],MN[N+1],MN[N+2],IDX,'
924     MEM[X+1]#,',',MEM[X+3] SHL 8 +MEM[X+2]#);CRLF
944   END (CODE),
945
945  PROC CKBP; (CHECK BREAK POINT)
945   VAR I INTEGER,
946   BEGIN IF P<0 THEN STOP =1
952    ELSE BEGIN
954    FOR I =1 TO BP DO
961     IF BREAK[I]=P THEN BEGIN
966       WRITE(' BREAK '),CODE(P),
978        STOP =1 END END
985   END (CKBP),
986
986  BEGIN (MAIN)
986   FOR I:=0 TO 26 DO
994    MN[I]:=MEM[I+%1E80]; (MNEMONICS ARE IN MEMORY)
1005  WRITE('ADDR?'),READ(Z%),CRLF,
1015  INIT; CODE(P),BP =0,
1021  REPEAT WRITE('>');READ(CMD);
1025   CASE CMD OF
1026 'R':BEGIN STOP =0;REPEAT EXEC;CKBP UNTIL STOP END;
1037 'S':BEGIN EXEC, CODE(P) END,
1046 'X':BEGIN
1050       WRITE('  P=',P#,' B=',B#,' T=',T#,
1072            ' S[T]=',S[T]#,' S[T-1]=',S[T-1]#);CRLF
1099      END;
1100 'G':BEGIN INIT;REPEAT EXEC;CKBP UNTIL STOP END;
1110 'T':BEGIN WRITE(' *TRACE*');CRLF;
1125       FOR I:=0 TO U DO BEGIN
1132        TP:=TP+1;IF TP>U THEN TP =0;
1142        IF TRACE[TP]>=0 THEN CODE(TRACE[TP]) END
1151      END;
1157 'K':BEGIN READ(I#);
1163       FOR J:=I TO I+6 DO
1172        WRITE('  ',S[J]#),CRLF
1185      END,
1186 'B':IF BP<BPLIM THEN BEGIN
1194       BP:=BP+1;WRITE(BP#,' ');
1202       READ(BREAK[BP]#);CRLF END;
1207 'C':BEGIN (CLEAR BP)
1211       BP:=0;CRLF END;
1215 'Y':BEGIN FOR I:=1 TO BP DO
1226       WRITE('  ',BREAK[I]#);CRLF END;
1240 'E':BEGIN READ(P0#);CODE(P0) END;
1250 'U':IF P0>0 THEN BEGIN
1258       P0:=P0-1;CODE(P0) END;
1266 'N':BEGIN P0:=P0+1;CODE(P0) END;
1278 'Q':P:=-1
1283      ELSE BEGIN WRITE('??');CRLF END
1291  END (CASE OF CMD)
1292  UNTIL P<0;
1296  CRLF; WRITE(K#,' INSTR  EXECUTED.');CRLF
1319 END (MAIN),
INTERPRET(I), OR TRANSLATE(T)?
```

structure of the Pascal version is neat and highly readable, the debugging time is minimal. The Pascal source program is shown in listing 1. The program design is rather straightforward. Readers with some programming experience in any high level language should be able to read and understand it without the help of a flowchart or further explanation on program logic. Note that in the main program and procedure *exec*, the case...of statement is put to good use. In the BASIC version the interpreter commands have to be tested within a FOR loop by comparing the input character with a string array, and then an ON...GOTO statement is used to branch to various parts of the program.

It must be emphasized again that the interpreter executes p-codes and not Pascal statements. Therefore the user is required to have some knowledge of the p-machine and p-codes. In addition to this, the p-compiler should be instructed to list p-codes together with Pascal program statements during compilation. They will be cross-referenced when running the interpreter. Obviously this procedure is not as convenient and easy to use as an ordinary BASIC interpreter, but still it provides the only way for debugging Pascal programs in our present version. A new debugging scheme is being planned for the future which will enable the user to debug programs at the Pascal statement level. This means the user may refer to variables and arrays and statements rather than stack contents and p-code addresses. Part 2 will go into details of the design and implementation of the p-compiler.■

Graphic Manipulations Using Matrices

Joel C Hungerford
Stearns Rd
Amherst NH 03031

$$P = \begin{vmatrix} X \\ Y \\ Z \end{vmatrix}$$

$$C = \begin{vmatrix} a & b & c \\ d & e & f \\ g & h & i \end{vmatrix}$$

Figure 1: Two types of matrices used in graphics applications. P represents a point in space. The matrix C contains equations to relate the transformed values of X, Y, and Z to the original values.

One definition of graphics might be "a means to convert data into information." Our computers create printed data at a great rate, but all this data is not information until it conveys to a person some trend or fact about the world we live in. A small part of graphics is the conversion of data representing the position in space of the surface of an object into a three-dimensional picture of that object. The picture may be useful for itself as computer art, or it may help understand something about the object.

Imagine looking down the length of a pencil, using only one eye. With the eraser held away from the viewer, the pencil appears as a polygon with a dark place in the center where the lead is. The length of the pencil and the eraser are invisible. Now imagine the pencil rotated about its point until it is pointed toward the viewer's shoulder. The length of the pencil and the eraser are now visible, and appear in the form of translations to the side and up of the surface of the pencil. The relation between the position of a point on the pencil, specified in three dimensions X, Y and Z, and the apparent translation of that point as the pencil is rotated is expressed by standard equations. These can be written in an organized fashion using matrices. These matrices are called *coordinate transform matrices*. They are powerful tools because they separate the mathematics associated with the angle of observation from the data describing the surface of an object. The small computers available today make it easy to convert surface data to pictorial information using matrices. This article will show how.

Definitions

The Cartesian coordinate system will be used in this discussion. On a computer graphic screen, X is the horizontal dimension, Y is defined as the vertical dimension, and Z is depth into the screen. Positive values are to the right, up, and away from the viewer. The origin will usually be in the center of the screen. A plane is described by any two axes. Thus, the X,Y plane is the surface of the computer screen, the Y,Z plane is seen edge on as the Y axis, and the X,Z plane is seen edge on as the X axis.

An equation which does not specifically include a particular coordinate direction will be interpreted to mean that the described line or point may exist anywhere along the unmentioned axis. Thus, X=1 represents the entire Y,Z plane located at 1 along the X axis. The line defined by Y=X may exist anywhere along the Z axis; therefore this equation defines a plane tilted 45 degrees from the horizontal, seen edge on at Z equal to zero on the computer screen. A surface may be made parallel to an axis by omitting that axis, as above, or may be specified at all values of X, Y and Z. Thus, Y=X+Z is a surface defined for all space.

Two kinds of matrices will be used here. The first kind is a matrix which represents the coordinates of a point in space, described by X, Y and Z. This matrix, P, is a column matrix, with one column and three rows as shown in figure 1. It will be used to hold the values for a point on the surface, both before and after transformation. All drawing commands will use the X and Y from this matrix.

The second kind of matrix contains the standard equations which relate the transformed values for X, Y and Z to the original values. This matrix, C, has three rows and three columns. The numbers at each position in this matrix are derived from the standard equations for some specific coordinate transformation type, such as a rotation. If the angle of observation of the object is arrived at by two successive operations, such as a rotation in each of two planes, then the matrix, C, which controls this view may have numbers in it that are derived from two matrix equations. The procedure which produces a single matrix combining several operations is called matrix multiplication. Matrix multiplication is used both to produce the particular numbers in the 3 by 3 matrix, C, which describe a point of observation, and then to apply those numbers to derive a transformed 3 by 1 matrix, P, which gives the apparent position of some part of the object's surface.

Computing Procedure

Given the ability to do matrix multiplication (the details will be presented below), the sequence of operations to produce a three-dimensional picture of an object is short and easily stated:

1. Generate an array of data consisting of the X, Y and Z coordinates of the object to be drawn. This may be either computed as the drawing progresses, or done all at once and stored. The latter way is faster if the viewpoint is to be adjusted to find the most pleasing picture.
2. Define the viewpoint. For this part, a matrix is generated for each motion required to arrive at the desired point of view. The matrices are then multiplied together to produce a single 3 by 3 matrix to be used in the main routine. The order of multiplication may be important.
3. Write a program to draw the object in its untransformed state. This will be a sequence of commands which move the graphic cursor to a spot on the object at the beginning of an edge or other feature, then draw (move leaving a line behind) to another spot on the object. Specify the move and draw coordinates in terms of a column matrix element rather than X, Y and Z. Define the elements at each spot by using each of the points in the array.
4. When the untransformed picture is accurate and understood, then the picture is reoriented by simply inserting a matrix multiplication between the specification of each column matrix and the associated graphic command. The original X, Y, Z coordinates of the spot on the object are thereby transformed into a new set of X, Y, Z numbers representing the spot seen from the new viewpoint. Each set of coordinates from step 1 is multiplied by the matrix generated in step 2.

4a. An alternate method is to do all the transformations at once, changing all the X, Y and Z points in the array formed in step 1 into transformed X, Y and Z numbers in the same array.

Since the computer screen is really only two-dimensional, only the X and Y elements are used in step 3. After transformation, these numbers are shifted about and contain depth information. The drawing made in this fashion is a projected view rather than a three-dimensional drawing. The difference is that in the projected view sides which are parallel on the object remain parallel in the projected view, but in the three-dimensional view all lines converge at infinity along the Z axis. The difference is minor. The observer perceives a three-dimensional picture in most cases; the projected view in some figures is perceived either as having relief or depth without the visual clue of lines meeting at infinity. This leads to some interesting optical illusions using projected views.

The rest of this article discusses some of the transformations available and shows the pictorial results of each.

Matrix Multiplication

What information is necessary to write a subroutine to perform the matrix transformations described in this article? The general theory of matrix algebra and its interpretation is beyond the scope of this discussion. For more information and a very clear description of many other uses for matrices, the reader is referred to The Mathematics of Matrices *by Philip J Davis. Here are some brief notes on the subject:*

Two aspects of matrices are important in matrix multiplication. These are the order of the matrices being multiplied (which one comes first), and the shape of each matrix. The elements in the output matrix resulting from a multiplication of two matrices are each formed by combining numbers in the columns of the first matrix and rows of the second matrix, done in a standard order. All the necessary rows and columns have to exist for the output to exist. Thus, some matrices may be multiplied in one order, but not in the opposite order. The rule is: the number of columns of the first matrix must equal the number of rows of the second matrix.

In table 1, the two matrices may be multiplied in the order (C) (P) but not in the order (P) (C). The result of multiplying (C) (P) is a new column matrix P'. A mathematician would say that two matrices are "conformable for multiplication" when the order and shape requirements are met. He would also say "(C) is multiplied by (P)" here. The requirement for conformability leaves one dimension of the shape of each matrix unrestricted. The unrestricted dimensions establish the shape of the output matrix. Tables 1 and 2 summarize the necessary arithmetic. The elements in (C) are numbers, which are each computed in various ways depending upon the desired transformation.

$$\begin{vmatrix} A & B & C \\ D & E & F \\ G & H & I \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X'= (X*A+Y*B+Z*C)
Y'= (X*D+Y*E+Z*F)
Z'= (X*G+Y*H+Z*I)

Table 1: Matrix multiplication format.

$$\begin{vmatrix} A & B & C \\ D & E & F \\ G & H & I \end{vmatrix} \begin{vmatrix} J & K & L \\ M & N & O \\ P & Q & R \end{vmatrix} = \begin{vmatrix} A' & B' & C' \\ D' & E' & F' \\ G' & H' & I' \end{vmatrix}$$

A'= (A*J+B*M+C*P)	B'= (A*K+B*N+C*Q)	C'= (A*L+B*O+C*R)
D'= (D*J+E*M+F*P)	E'= (D*K+E*N+F*Q)	F'= (D*L+E*O+F*R)
G'= (G*J+H*M+I*P)	H'= (G*K+H*N+I*Q)	I'= (G*L+H*O+I*R)

Table 2: 3 by 3 matrix multiplication format.

Types of Transformations

The operations possible using coordinate transform matrices are not limited to shifting and rotating the picture. A number of more drastic changes may be made to the picture. Some of these changes are: magnification, shear, stretching in one direction, and mapping onto a surface.

The following figures and tables show examples of several coordinate transform operations. Each operation is represented by the matrix, the equations for the output matrix elements, and a figure to show how a picture of a well-known object is changed by the operation.

Unit Matrix

Table 3 shows the unit matrix. This transformation reproduces the picture of the object in its original view as defined above. Figure 2 shows a side view of a coffee cup.

$$\begin{vmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{vmatrix} \begin{Vmatrix} X \\ Y \\ Z \end{Vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

```
X'= (X*1+Y*0+Z*0)
Y'= (X*0+Y*1+Z*0)
Z'= (X*0+Y*0+Z*1)
```

Table 3: The unit matrix.

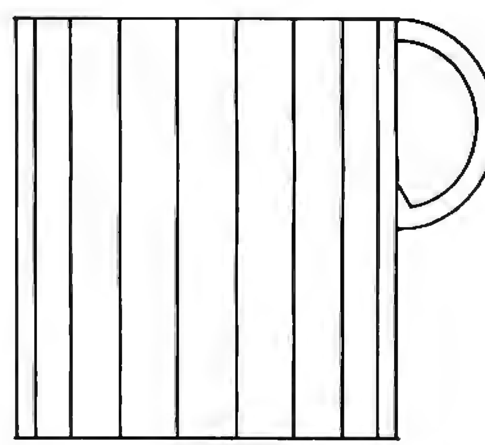


Figure 2: The standard view (untransformed).

$$\begin{vmatrix} 1 & 0 & 0 \\ 0 & K & 0 \\ 0 & 0 & 1 \end{vmatrix} \begin{Vmatrix} X \\ Y \\ Z \end{Vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

```
X'= (X*1+Y*0+Z*0)
Y'= (X*0+Y*K+Z*0)
Z'= (X*0+Y*0+Z*1)
```

Table 4: Expansion along the Y axis by a factor K.

Scaling

The object may be defined with some shape which is not quite the final version, but which uses easily verified dimensions. Thus, in our example, the height is equal to the diameter, and the square outline in figure 2 quickly shows that the array of data defining the cup is correct in the X and Y dimensions.

Selective magnification along any axis may be used to alter the proportions of the object to a shape that may be nearer that required by the user. Thus, table 4 and figure 3 are appropriate for users with large capacities; table 5 and figure 4 produce a cup for those with wide mouths, while table 6 and figure 6 produce a cup which could be used for filling a pie plate with whipped cream.

If the proportions are correct but the user wants to create several different sizes, table 7 will allow the same magnification to take place along all the axes. One such magnified cup is shown in figure 5.

$$\begin{vmatrix} K & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X'= (X*K+Y*0+Z*0)
Y'= (X*0+Y*1+Z*0)
Z'= (X*0+Y*0+Z*1)

Table 5: Expansion along the X axis by a factor K.

$$\begin{vmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & K \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X'= (X*1+Y*0+Z*0)
Y'= (X*0+Y*1+Z*0)
Z'= (X*0+Y*0+Z*K)

Table 6: Expansion along the Z axis by a factor K.

$$\begin{vmatrix} K & 0 & 0 \\ 0 & K & 0 \\ 0 & 0 & K \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X'= (X*K+Y*0+Z*0)
Y'= (X*0+Y*K+Z*0)
Z'= (X*0+Y*0+Z*K)

Table 7: Magnification by a factor K.

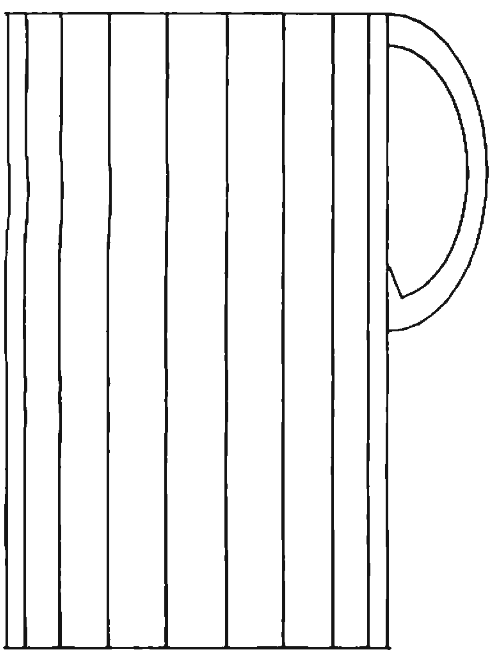


Figure 3: Expanded along the Y axis by a factor of 1.5.

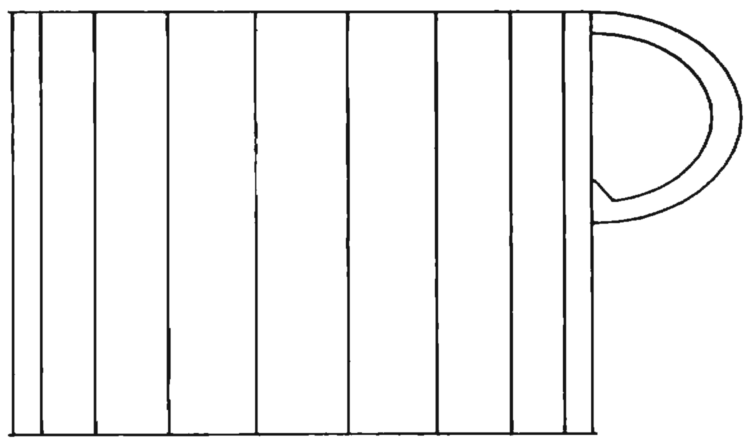


Figure 4: Expanded along the X axis by a factor of 1.5.

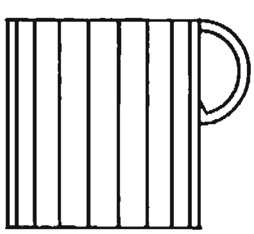


Figure 5: Magnified by a factor of 0.5.

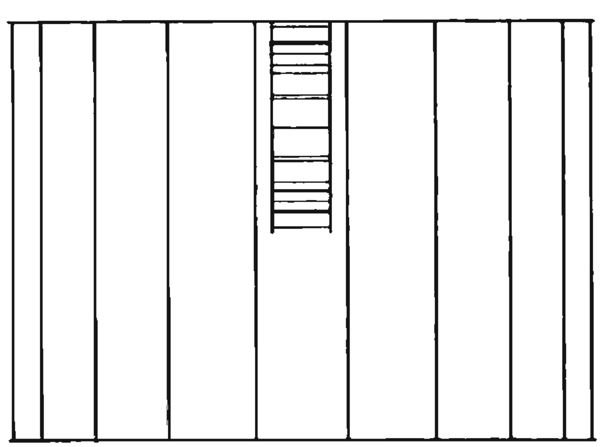


Figure 6: Rotated 90 degrees and expanded along Z axis by a factor of 1.5.

Shear

The object in its original shape may be boring and conventional in shape and lack individuality. This failing may be rectified as in table 8 and figure 7. To shear the object, the position of a point on the object is displaced from its original position by a function of the point's position along an orthogonal axis. These figures displace the points upward by a value equal to half the horizontal distance to each point.

Table 9 and figures 8 and 9 show shear along the horizontal axis. Figure 9 shows the same object as figure 8 rotated 90° to illustrate that the third axis is unchanged by this operation. As in the other operations, shears along all axes may be combined.

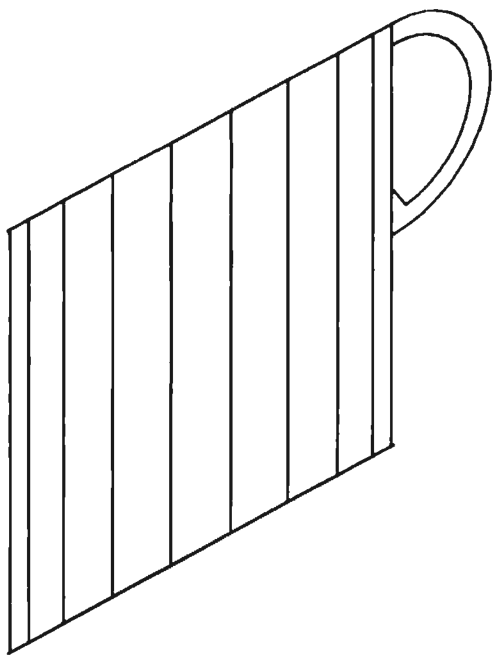


*Figure 7: Sheared along Y by X*0.5.*

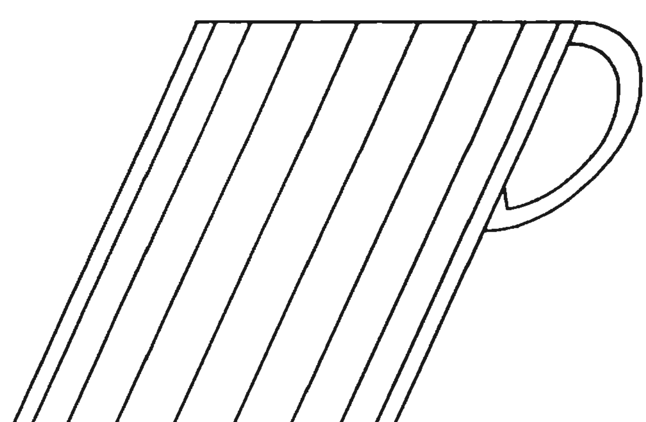


*Figure 8: Sheared along X by Y*0.5.*

$$\begin{vmatrix} 1 & 0 & 0 \\ K & 1 & 0 \\ 0 & 0 & 1 \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X' = (X*1+Y*0+Z*0)
Y' = (X*K+Y*1+Z*0)
Z' = (X*0+Y*0+Z*1)

Table 8: Shear along the Y axis in the X, Y plane by a factor K.

$$\begin{vmatrix} 1 & K & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X' = (X*1+Y*K+Z*0)
Y' = (X*0+Y*1+Z*0)
Z' = (X*0+Y*0+Z*1)

Table 9: Shear along the X axis in the X,Y plane by a factor K.

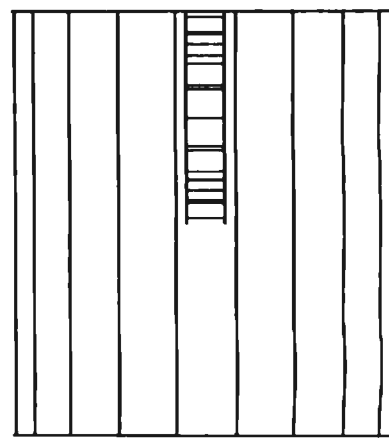


Figure 9: Rotated 90 degrees, sheared along X.

Rotations

The object may be reoriented in space by rotating it about any axis. A particular angle of view may be arrived at by some sequence of rotations about each axis. This is easily accomplished using the matrices in the following tables.

A point of confusion occurs when using rotations. The order of multiplication of the matrices (or the order of applying the operations to the object) is important. The axes remain associated with the object, not the screen. This means, for instance, that if the rotation in the X, Y plane shown in table 10 is applied first to the object, then subsequent rotations in the other planes happen in the slanted planes (X,Z and Y,Z) shown in figure 10.

It required some care to accurately predict the final picture after several rotations, especially since projected views lack the visual clue due to lines converging at infinity. Tables 11 and 12 along with figures 11 and 12 show the effects of rotation in the other two planes.

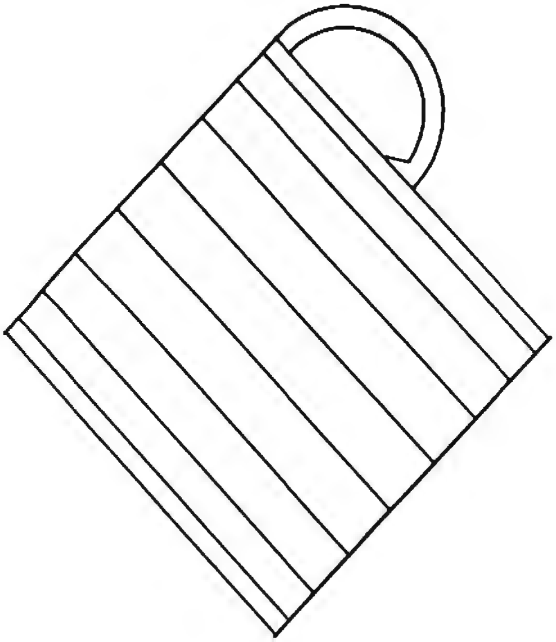


Figure 10: Rotated 45 degrees in the X, Y plane.

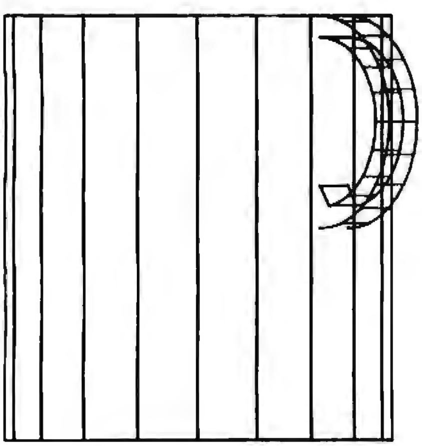


Figure 11: Rotated 45 degrees in the X, Z plane.

$$\begin{vmatrix} COS(T) & -SIN(T) & 0 \\ SIN(T) & COS(T) & 0 \\ 0 & 0 & 1 \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

```
X '= (X*COS(T)+Y*-SIN(T)+Z*0)
Y '= (X*SIN(T)+Y*COS(T)+Z*0)
Z '= (X*0+Y*0+Z*1)
```

Table 10: Rotation in the X,Y plane.

$$\begin{vmatrix} COS(T) & 0 & -SIN(T) \\ 0 & 1 & 0 \\ SIN(T) & 0 & COS(T) \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

```
X '= (X*COS(T)+Y*0+Z*-SIN(T))
Y '= (X*0+Y*1+Z*0)
Z '= (X*SIN(T)+Y*0+Z*COS(T))
```

Table 11: Rotation in the X,Z plane.

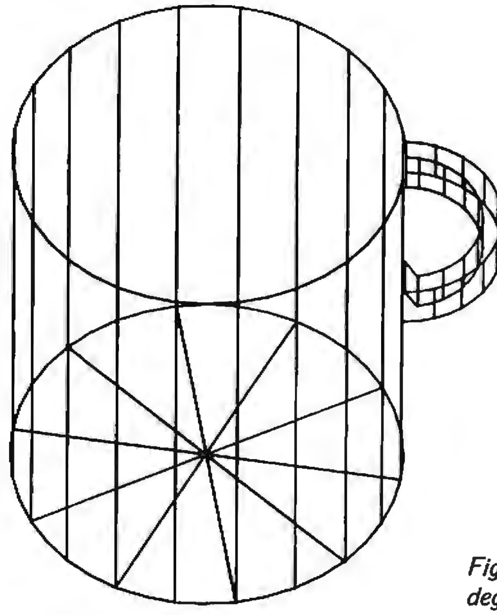


Figure 12: Rotated 45 degrees in the Y,Z plane.

$$\begin{vmatrix} 1 & 0 & 0 \\ 0 & COS(T) & -SIN(T) \\ 0 & SIN(T) & COS(T) \end{vmatrix} \begin{vmatrix} X \\ Y \\ Z \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

```
X '= (X*1+Y*0+Z*0)
Y '= (X*0+Y*COS(T)+Z*-SIN(T))
Z '= (X*0+Y*SIN(T)+Z*COS(T))
```

Table 12: Rotation in the Y,Z plane.

Combinations

Table 13 shows an example of the sequential application of two rotations using the procedure shown in table 2 to define the elements. Figure 13 combines the three rotations, a magnification and two scale changes along individual axes. Figure 14 applies shear and rotation. Figure 15 shows just the rotation for comparison purposes.

$$\begin{vmatrix} 1 & 0 & 0 \\ 0 & COS(T) & -SIN(T) \\ 0 & SIN(T) & COS(T) \end{vmatrix} \begin{vmatrix} COS(S) & -SIN(S) & 0 \\ SIN(S) & COS(S) & 0 \\ 0 & 0 & 1 \end{vmatrix} = \begin{vmatrix} A' & B' & C' \\ D' & E' & F' \\ G' & H' & I' \end{vmatrix}$$

A'= (1*COS(S)+0*SIN(S)+0*0)
B'= (1*-SIN(S)+0*COS(S)+0*0)
C'= (1*0+0*0+0*1)
D'= (0*COS(S)+COS(T)*SIN(S)-SIN(T)*0)
E'= (0*-SIN(S)+COS(T)*COS(S) -SIN(T)*0)
F'= (0*0+COS(T)*0-SIN(T)*1)
G'= (0*COS(S)+SIN(T)*SIN(S)+COS(T)*0)
H'= (0*-SIN(S)+SIN(T)*COS(S)+COS(T)*0)
I'= (0*0+SIN(T)*0+COS(T)*1)

Table 13: Rotation in the X,Y and Y,Z planes sequentially.

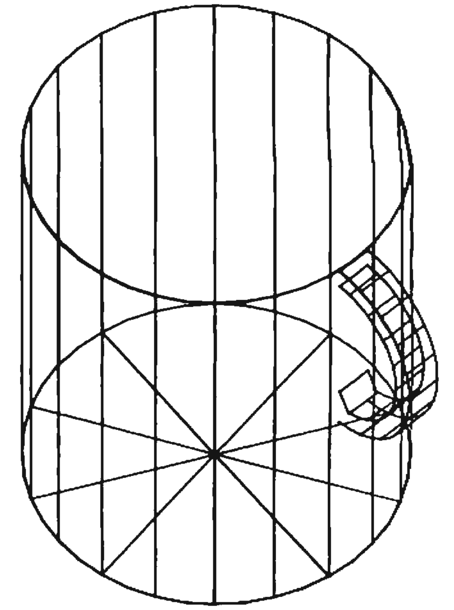


Figure 15: Rotated but not sheared.

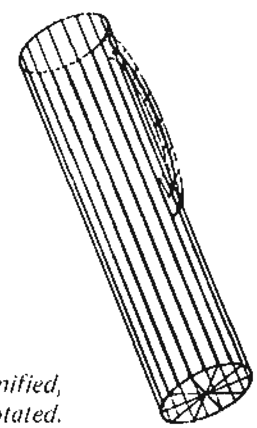


Figure 13: Magnified, expanded, and rotated.

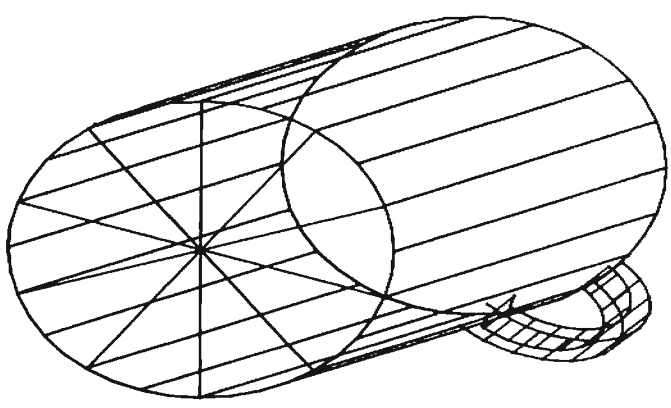


Figure 14: Rotated and sheared.

$$\begin{vmatrix} X+k \\ Y+m \\ Z+n \end{vmatrix} = \begin{vmatrix} X' \\ Y' \\ Z' \end{vmatrix}$$

X'= X+k
Y'= Y+m
Z'= Z+n

Table 14: Translation matrix.

Translation

Moving the object sideways is not shown but is accomplished by adding the translation value to the original value for each axis as shown in table 14.

Mapping

All of the examples shown so far have applied the same operation to every point on the surface of the object. The coordinate transform matrix contains the same numbers for all parts of the object. A more complicated operation results when the value (X,Y, Z) associated with a point on the surface of the object is replaced by a function of X, Y, and Z at each point. The result maps the object onto some surface. Thus, if X is replaced by sin(X), for instance, the object will experience a change in scale which changes with X, and the output position of a point on the object which has a value of X equal to zero, and an arbitrary Y and Z is the same as a point with a value of X equal to 180 or 360 if the computer interprets the value of X as degrees.

The result of replacing X by sin(X) pictorially is identical to the projected view of a cylinder, parallel to the Y axis, which has the original view (such as figure 2) painted onto its surface. If the dimensions of the object for this example are such that the width is equal to 360 units, then the cylinder is completely circumscribed by the original view of the object.

In order to make a three-dimensional picture of the mapped figure, the other two dimensions must also be specified. For the example here, the depth must also be mapped by setting Z equal to cos(X). Since the new surface is a cylinder, Y is unchanged.

Mapping Example

Figure 16 shows a label to be pasted on the coffee cup. This label, like the cup itself, is defined by an array of data giving the X, Y and Z coordinates of each point. The standard view is in the Z equal to zero plane. A subroutine then replaces the X and Z values with the mapped values in all the points of the array. Since the standard view of the cup is a side view, and the label is to be pasted opposite the handle, 180° is added to X before computing the mapped functions. The lower left corner of figure 16 is coordinate (0,0).

The mapped array of data is now subjected to whatever coordinate transforms are applied to the cup. Figure 17 shows the result as applied to the label alone. Figure 18 shows the completed picture.

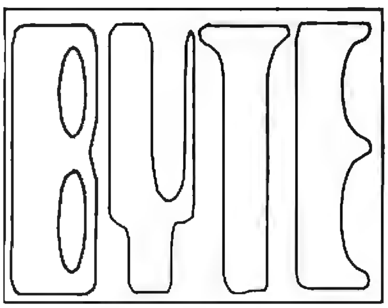


Figure 16.

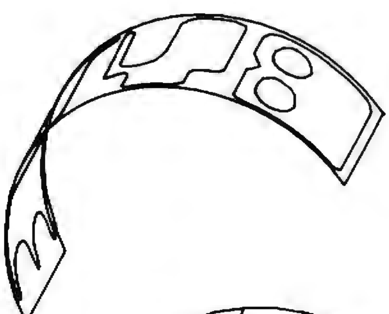


Figure 17.

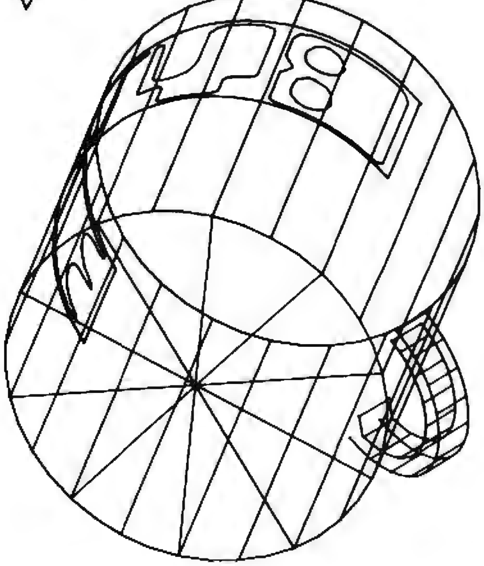
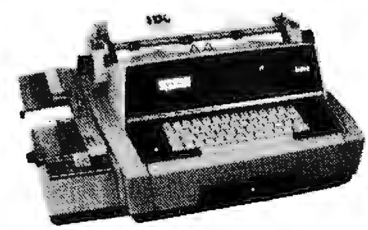


Figure 18.



Illusions

Figure 19 shows the same object as figure 18, rotated 180°. While most viewers see the cup with the handle toward them, "looking down into it" in figure 18, many find that figure 19 alternates between looking *down* into it with the handle away from the viewer, and looking *up* at it from the bottom, with the handle at the top. This example shows that a relatively minor change in viewpoint may produce a great change in terms of the clarity of the information presented.

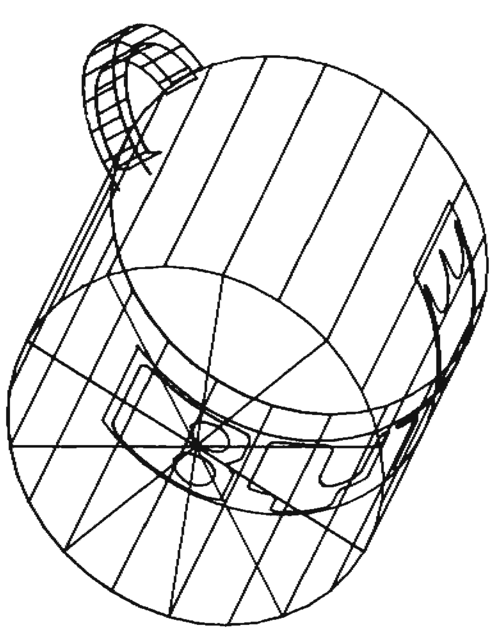


Figure 19.

Mapping Uses

Mapping may be used to compress the picture of an object to fit it into a particular space, to selectively emphasize some part while compressing the rest, such as the region near X equal to zero or 180° in this example. Or it may be used to picture some complicated configuration which is more easily defined in a rectangular coordinate system. Thus, a simple rectangular electrode configuration expressed in Cartesian coordinates may be used to compute the electric field lines at each point in the configuration. Mapping processes plus the coordinate transforms may then be used to change the known field picture into one for a complicated electron gun in a cathode ray tube.

Excerpts from the BASIC program which produced the pictures in this article are shown in listing 1. The machine used is a Tektronix 4051 graphic computer with a 4662 plotter, with matrix read only memory. The matrix command A MPY B is specific to this equipment. The rest of the program is in a fairly standard BASIC.

Lines 2000 to 2490 comprise the main program which draws the coffee cup. The purpose of each subroutine is noted. The program defining the various matrices in terms of viewpoint parameters is shown in lines 2535 to 3010. The program to combine the matrices into a single 3 by 3 matrix, C4, which is applied to the drawing is listed in lines 3120 to 3200. The A MPY B format does the matrix multiplication. In a machine without this extension, a subroutine using the equation listed in the various figures would do the same job, but take much more space.

Lines 4000 to 4300 show part of the much longer listing which defines the cup: A1 (N,1) = X, A1 (N,2) = Y, A1 (N,3) = Z. The variable A1 (N,4) is a secondary address used with a form of the print command to make it move (21) or draw (20). This is a faster way to draw on the Tektronix machine. Lines 4050 to 4140 draw the top and bottom circle.

Lines 5240 to 5270 convert the cup dimensions to graphics display units (GDUs) which are required to use this style of drawing commands. This program, with all arrays, filled, uses about 28,500 bytes of memory. Incidentally, lacking a printer, I printed the program using the plotter.

Listing 1.

```
2000 DELETE A1,A2,B1,B2,B3,B4,B5,B6,B7,B8,B9,C1,C2,C3,V1,C4,V2
2002 DIM A1(262,4),A2(262,4),B1(3,3),B2(3,3),B3(3,3),B4(3,3),B5(3,3)
2003 DIM B6(3,3),B7(3,3),B8(3,3),B9(3,3),C1(3,3),C2(3,3),C3(3,3),C4(3,3)
2004 DIM V1(3,1),V2(3,1)
2005 REM THIS SUBROUTINE DEFINES THE CUP
2010 GOSUB 2500
2090 REM THIS SUBROUTINE DEFINES THE TRANSFORM MATRICES
2100 GOSUB 2540
2140 REM THIS SUBROUTINE MULTIPLIES ALL THE MATRICES TOGETHER
2150 GOSUB 3120
2160 REM THIS SUBROUTINE CHANGES A1 TO A NEW VIEW,A2
2170 GOSUB 5500
2180 REM THIS SUBROUTINE CHANGES THE CUP FROM USER DATA UNITS TO GDU'S
2190 GOSUB 5240
2195 REM THIS SUBROUTINE DRAWS THE FIGURE
2200 GOSUB 5200
2490 END

2535 REM B1 ROTATES IN THE X,Y PLANE BY T1 DEGREES
2540 B1=0
2550 B1(1,1)=COS(T1)
2560 B1(1,2)=-SIN(T1)
2570 B1(2,1)=SIN(T1)
2580 B1(2,2)=COS(T1)
2590 B1(3,3)=1
2600 REM B2 ROTATES IN THE X,Z PLANE BY T2 DEGREES
2610 B2=0
2620 B2(1,1)=COS(T2)
2630 B2(1,3)=-SIN(T2)
2640 B2(2,2)=1
2650 B2(3,1)=SIN(T2)
2660 B2(3,3)=COS(T2)
2670 REM B3 ROTATES IN THE Y,Z PLANE BY T3 DEGREES
2680 B3=0
2690 B3(1,1)=1
```

```
2700 B3(2,2)=COS(T3)
2710 B3(2,3)=-SIN(T3)
2720 B3(3,2)=SIN(T3)
2730 B3(3,3)=COS(T3)
2740 REM B4 IS THE UNIT MATRIX
2750 B4=0
2760 B4(1,1)=1
2770 B4(2,2)=1
2780 B4(3,3)=1
2790 REM B5 EXPANDS ALONG THE X AXIS BY K1
2800 B5=B4
2810 B5(1,1)=K1
2820 REM B6 EXPANDS ALONG THE Y AXIS BY K2
2830 B6=B4
2840 B6(2,2)=K2
2850 REM B7 EXPANDS ALONG THE Z AXIS BY K3
2860 B7=B4
2870 B7(3,3)=K3
2880 REM B8 MAGNIFIES BY K4
2890 B8=K4*B4
2900 REM B9 REFLECTS IN THE Y=X PLANE
2910 B9=0
2920 B9(1,2)=1
2930 B9(2,1)=1
2940 B9(3,3)=1
2950 REM C1 SHEARS ALONG THE X AXIS BY K5 X/Y RATIO
2960 C1=B4
2970 C1(1,2)=K5
2980 REM C2 SHEARS ALONG THE Y AXIS BY K6 X/Y RATIO
2990 C2=B4
3000 C2(2,1)=K6
3010 RETURN

3120 C3=B6 MPY B5
3130 C4=B7 MPY C3
3140 C3=B8 MPY C4
3150 C4=C1 MPY C3
3160 C3=C2 MPY C4
3170 C4=B2 MPY C3
3180 C3=B3 MPY C4
3190 C4=B1 MPY C3
3200 RETURN

4000 REM THIS PART FORMS THE TOP AND BOTTOM EDGE OF THE CUP
4010 A1(1,1)=10
4020 A1(1,2)=10
4030 A1(1,3)=0
4040 A1(1,4)=21
4050 FOR N=0 TO 360 STEP 9
4060 A1(N/9+2,1)=10*COS(N)
4070 A1(N/9+2,3)=10*SIN(N)
4080 A1(N/9+2,2)=10
4090 A1(N/9+2,4)=20
4100 A1(N/9+44,1)=A1(N/9+2,1)
4110 A1(N/9+44,3)=A1(N/9+2,3)
4120 A1(N/9+44,2)=-10
4130 A1(N/9+44,4)=20
4140 NEXT N
4142 A1(43,1)=A1(44,1)
4144 A1(43,2)=A1(44,2)
4146 A1(43,3)=A1(44,3)
4148 A1(43,4)=21
4150 REM A1 IS FILLED TO #84 AT THIS POINT
4160 A1(85,1)=10
4170 A1(85,2)=0
4180 A1(85,3)=1
4190 A1(85,4)=21
4200 REM THIS PART DRAWS THE OUTSIDE OF THE HANDLE
4210 FOR N=0 TO 180 STEP 9
4220 A1(N/9+86,1)=5*SIN(N)+10
4230 A1(N/9+86,2)=5-5*COS(N)
4240 A1(N/9+86,3)=1
4250 A1(N/9+86,4)=20
4260 A1(N/9+107,1)=A1(N/9+86,1)
4270 A1(N/9+107,2)=A1(N/9+86,2)
4280 A1(N/9+107,3)=-1
4290 A1(N/9+107,4)=20
4300 NEXT N

5200 FOR N=1 TO 262
5210 PRINT #1,A2(N,4);A2(N,1),A2(N,2)
5220 NEXT N
5230 RETURN
5240 FOR N=1 TO 262
5250 A2(N,1)=A2(N,1)/15*40+50
5260 A2(N,2)=A2(N,2)/15*40+50
5270 A2(N,3)=A2(N,3)/15*40
5280 NEXT N
5290 RETURN
5500 FOR N=1 TO 262
5510 V1(1,1)=A1(N,1)
5520 V1(2,1)=A1(N,2)
5530 V1(3,1)=A1(N,3)
5540 V2=C4 MPY V1
5550 A2(N,1)=V2(1,1)
5560 A2(N,2)=V2(2,1)
5570 A2(N,3)=V2(3,1)
5580 A2(N,4)=A1(N,4)
5600 NEXT N
5610 RETURN ■
```

WADUZITDO:

How To Write a Language in 256 Words or Less

Larry Kheriaty
Computer Center
Western Washington University
Bellingham WA 98225

Every computer owner likes to show his or her microcomputer to friends. The first question the friends usually ask is, "What does it do?" The software system presented here demonstrates what a computer can do in a manner simple enough for almost anyone to understand. Even if you have a larger, more capable system, it is often worthwhile to be able to demonstrate something that can be accomplished on a smaller scale. WADUZITDO is small enough to run on almost any microcomputer yet it allows even the novice user to make the computer "do something."

WADUZITDO is a complete high level language processor that fits in less than 256 bytes on either a 6800 or 8080 based system. The only other requirement is some kind of terminal. The system includes a text editor to allow a program to be entered and modified, and an interpreter to execute the program. The only external routines needed are single character input and single character output such as those provided by most system monitors.

The object of WADUZITDO is to run simple conversational programs. There are just five statement types, roughly derived from the PILOT language. To keep it small only the most essential capabilities are available. This also makes programming very easy. In fact, only a few minutes after my unsuspecting spouse had asked, "What does it do?", she had written the interactive dialogue program in listing 1 to help me make out a list of acceptable birthday gifts!

Programming in WADUZITDO is straightforward and uncomplicated. For example, to direct the computer to display a line of text on the terminal you use the *type* statement. The following example shows the format of the *type* statement.

```
T:WHAT COULD BE EASIER
THAN THIS?
```

The T is the operation code for *type*. A colon always follows the operation code. The text after the colon is displayed exactly as shown.

The *accept* statement allows the program to receive one input character from the terminal keyboard. Normally it is used after a *type* that asks for a response. For example:

```
T:CAN YOU TELL ME WHAT 2 + 3
EQUALS?

A:
```

The *accept* statement is just the A operation code followed by a colon. When it is encountered execution pauses until the user keys in any single character. Then the input character is saved internally for use in subsequent *match* statements.

The *match* statement is used to test the character entered by the user on the previous *accept*. *Match* is coded as an M (the operation code), followed by a colon and one character. The character in the statement is compared to the last character entered by the user. The result of the comparison is recorded internally in the match flag: Y if the match is equal, N if it is not equal.

Once set the match flag can be used to conditionally execute or skip any subsequent statement. This is done by placing either a Y (yes) or N (no) immediately before any operation code. If the Y or N is the same as the match flag the statement is executed, otherwise it is skipped. An elaboration of the previous example illustrates the use of *match*.

```
T:WHAT IS 2 + 3?

A:

M:5

YT:FIVE, RIGHT.

NT:NO, THE ANSWER IS 5.
```

Normally statements are executed sequentially. The *jump* statement is used to alter the normal sequence. The format of the *jump* statement is J, followed by a colon, and a number from zero to nine. The statement J:0 causes a branch back to the last *accept* statement executed. Execution resumes from that statement. The J:0 statement can be used to allow the user to reanswer a previous question. For example:

```
T:HOW MANY FEET IN A YARD?
A:
M:3
YT:RIGHT.
NT:WRONG STUPID, TRY AGAIN.
NJ:0
```

The second form of the jump makes use of program markers. A program marker is an asterisk, *, preceding any statement. The statement J:n, where n is a number from 1 to 9, causes a branch to the nth program marker forward from the *jump*. This form of the *jump* is shown in the sample program in listing 2 which plays NIM.

The last type of statement is *stop*. This statement merely terminates execution of the program and returns control to the program editor. The format of the *stop* statement is S:

To increase the versatility of the language the S: statement can, at the user's option, be made to call a user written machine language subroutine from within the WADUZITDO program. To do this requires a one statement modification to the system which is detailed below. If you choose to make this modification you can consider S: to be the operation code for *subroutine* rather than *stop*. The format of the *subroutine* statement is S:x where x is any single character which serves as a parameter to the user written program. The value x will be stored in register A in both the 6800 and 8080 version. It can be used to select different functions to be performed by the program.

During execution any statement which does not fit the syntax of one of the five statement types is printed in its entirety, then execution resumes normally with the next statement. Table 1 summarizes the WADUZITDO instruction set.

When WADUZITDO is first entered con-

```
T:IT IS BIRTHDAY LIST TIME.
T:THE PURPOSE OF THIS PROGRAM IS TO
T:DETERMINE WHAT GIFTS ARE ACCEPTABLE.
T:TYPE THE CODE LETTER ASSOCIATED WITH
T:THE POTENTIAL GIFT IDEA...
T:  A  HOME APPLIANCE
T:  B  SOMETHING BORING
T:  C  ITEM OF CLOTHING
T:  D  SOMETHING DECORATIVE FOR THE HOUSE
T:  G  GARBAGE DISPOSAL
T:  M  MY OWN COMPUTER
A:
M:A
YT:UNACCEPTABLE.
M:B
YT:NO WAY.
M:C
YT:ACCEPTABLE IF NOT UGLY.
M:D
YT:OKAY IF CHOSEN WITH GOOD TASTE
YT:SO AS NOT TO BE TACKY.
M:G
YT:YEAH !
M:M
YT:THE LAST THING IN THE WORLD
YT:I WOULD EVER WANT.
NM:A
NM:B
NM:C
NM:D
NM:G
NT:CANT YOU READ FOOL, THAT IS NOT
NT:ONE OF THE CHOICES.
NT:TRY A,B,C,D,G OR M
J:Ø
```

Listing 1: WADUZITDO program written by a noncomputer person. Notice the last line of the program, the J:0 command. This instruction will make the program execution jump back to the accept statement to try another input.

```
T:LETS PLAY NIM WITH 7 PEBBLES.
T:WE TAKE TURNS TAKING 1,2 OR 3.
T:THE LAST ONE TO TAKE ONE LOSES.
T:THERE ARE 7, HOW MANY ?
A:
M:1
YJ:1
M:2
YJ:2
M:3
YJ:6
T:YOU CAN TAKE ONLY 1,2, OR 3.
J:Ø
*T:THAT LEAVES 6, I TAKE 1 LEAVING 5.
T:HOW MANY ?
A:
M:1
YJ:5
M:2
YJ:4
M:3
YJ:3
T:YOU MUST TAKE 1,2 OR 3.
J:Ø
*T:THAT LEAVES 5, I TAKE 1 LEAVING 4.
T:HOW MANY ?
A:
M:1
YJ:3
M:2
YJ:2
M:3
YJ:1
T:YOU MUST TAKE 1,2 OR 3 ONLY .
J:Ø
*T:THAT LEAVES THE LAST ONE.
T:I TAKE IT ... YOU WIN.
J:5
*T:THAT LEAVES 2, I TAKE 1 LEAVING 1.
J:3
*T:THAT LEAVES 3, I TAKE 2 LEAVING 1.
J:2
*T:THAT LEAVES 4, I TAKE 3 LEAVING 1.
*T:HOW MANY ?
A:
M:1
NT:YOU HAVE NO CHOICE BUT TO TAKE 1.
NT:HOW MANY ?
NJ:Ø
T:YOU JUST TOOK THE LAST ONE ... I WIN.
*T:TO PLAY AGAIN PUSH THE DOLLAR SIGN.
S:
```

Listing 2: A NIM playing program. This program demonstrates the jumping capability of the language.

STATEMENT	FORMAT	WHAT IT DOES
type	T:text	Display text on the terminal.
accept	A:	Input one character from the terminal keyboard.
match	M:x	Compare x to last input character and set match flag to Y if equal, N if not equal.
jump	J:n	If n=0 jump to last *accept*. If n=1 thru 9 jump to nth program marker forward from the J.
stop	S:	Terminate program and return to text editor.
subroutine	S:x	Call user machine language program (requires modification).
conditionals	Y N	May precede any operation code. Execute only if match flag is Y. Execute only if match flag is N.
program marker	*	May precede any statement, serves as a *jump* destination.

Table 1: Program instructions for the WADUZITDO language.

EDIT CHARACTER	HEX	MEANING
$	24	Start execution.
\	5C	Move edit pointer to program start.
/	2F	Display next line of program.
%	25	Pad inserted line with nulls.
bs or -	08 or 5F	Backspace to correct typing error.
cr	0D	End of statement.
any other		Character stored in program and edit pointer advances.

Table 2: Editing characters used by the built-in text editor.

trol is passed to the program editor which is used to enter or alter source programs. Also an internal program pointer, called LOC, is automatically set to the beginning of the source area. As each statement is entered on the keyboard the characters are stored and the internal pointer advances. Typing errors may be corrected by entering a backspace and the correct character. To reset the pointer to the start of the program enter a backslash, \. To display the next line of the program enter the mirror image of the reset slash, /. To replace a line, display each line up to but not including the one to be replaced, then enter the new line. The new line should be no longer than the line it replaces. If it is longer, the next line of text is also overwritten. End the replacement line with a percent key rather than a carriage return. The % causes null characters to be stored as filler up to the start of the next line. To begin execution of the program enter a dollar sign, $. (The editing commands are summarized in table 2.)

If you already have a good text editor in your system it may be used instead of the one included. Each statement is variable length, terminated by a carriage return character. All other control characters between statements are ignored.

Complete 6800 and 8080 assembly listings containing source and object code are included to simplify implementation on your system. The 6800 version in listing 3 uses the MIKBUG monitor; the 8080 version in listing 4 uses the SOLOS/CUTER monitor. If you have one of these two system monitors you need not modify the program at all.

The entry point to the system is at location zero. Upon entry the stack pointer is assumed set to address some scratchpad memory area large enough to accommodate a few levels of call. In MIKBUG or SOLOS/CUTER, as with most system monitors, this is handled automatically by the GO or EXEC command. The 2 byte value stored in LOC (hexadecimal 100) must point to the place where the user program is to be stored. In the assembly listings note that this value is shown as hexadecimal 0106, the first location not occupied by the system.

If you don't have one of the above monitors you must supply character input and character output routines and change the references to IN and OUT to address these routines. In the listings you will find one reference to IN and one to OUT which needs to be changed. If your terminal requires a delay after each carriage return you can set the number of null padding characters by a one byte modification to the statement labeled PLF.

Any of the special characters used by the text editor ($, %, \, /, bs) can be easily changed to another more convenient character on your keyboard.

As shown in the assembly listings the S: statement halts execution by branching to the text editor. If you don't modify this you can treat it as a *stop* statement. To use it as a subroutine call you must modify the JMP SUB instruction to be a JSR or CALL (depending on the system) to the appropriate address. Upon entry to the subroutine

Text continued after listings on page 173

Circle 288 on inquiry card.

Circle 395 on inquiry card.

Circle 153 on inquiry card.

Circle 17 on inquiry card.

Circle 72 on inquiry card.

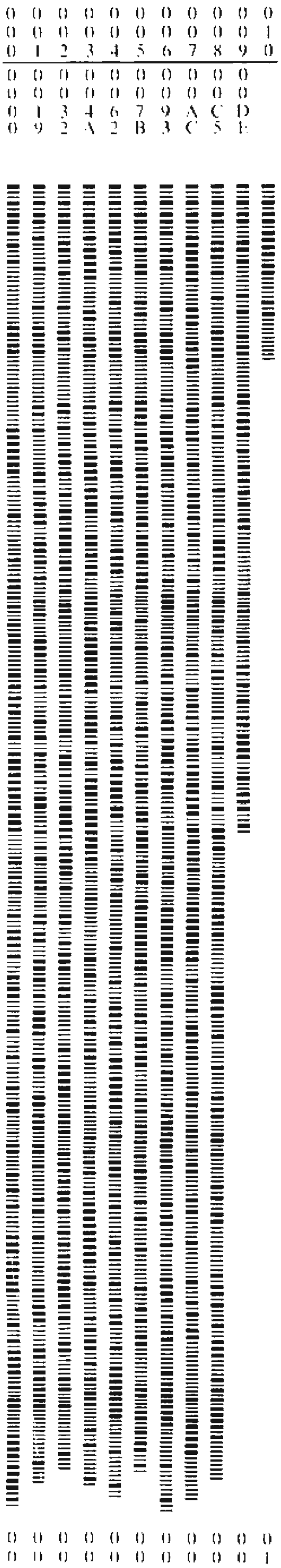
Circle 105 on inquiry card.

Circle 386 on inquiry card.

Circle 65 on inquiry card.

Circle 77 on inquiry card.

Figure 1: Absolute loader format representation of the 6800 WADUZITDO program of listing 3.




```
                   *                WADUZITDO
                   *         6800 VERSION BY LARRY KHERIATY
                   *
                   *     MIKBUG SUBROUTINES USED
                   IN        EQU   $E1AC      INPUT FROM KEYBOARD TO ACCA
                   OUT       EQU   $E1D1      OUTPUT FROM ACCA TO TERMINAL
                             ORG   $0000
                   SUB       EQU   $0000      USER SUBR START (CAN BE MODIFIED)
                   *    ENTER SYSTEM AT LOCATION 0 WITH STACK POINTER PRESET
                   *    TO SCRATCH PAD RAM ENOUGH FOR A FEW LEVELS OF CALL
0000 FE 0100       START     LDX   LOC        SOURCE PROGRAM AREA START
0003 8D 45         EGET      BSR   JIN        ACCEPT SOURCE CHAR
0005 81 5C                   CMP A #$5C       \  ?
0007 27 F7                   BEQ   START      YES, BACK UP TO PROGRAM START
                   *
0009 81 24                   CMP A #$24       $  ?
000B 27 45                   BEQ   EXEC       YES, GO EXECUTE THE PROGRAM
                   *
000D 81 08                   CMP A #$08       BS  ?
000F 26 03                   BNE   DIS        NO
0011 09                      DEX              YES, BACK UP ONE IN SOURCE
0012 20 EF                   BRA   EGET       LOOP BACK
                   *    PROCESS DISPLAY OF NEXT LINE
0014 81 2F         DIS       CMP A #$2F       /  ?
0016 26 07                   BNE   PAD        NO
0018 BD 00D5                 JSR   PRT        GO PRINT TO CR
001B 8D 21         EPLF      BSR   PLF        PRINT LINE FEED AND NULLS
001D 20 E4                   BRA   EGET       LOOP
                   *    DO LINE REPLACEMENT- PAD TO END OF STMT WITH NULLS
001F 81 25         PAD       CMP A #$25       %  ?
0021 26 12                   BNE   CHAR       NO
0023 86 0D                   LDA A #$0D       CR
0025 8D 27                   BSR   JOUT       PRINT IT
0027 86 0D                   LDA A #$0D       CR
0029 C6 40                   LDA B #$40       COUNT OF 64
002B A1 00         PADL      CMP A 0,X        AT CR YET ?
002D 27 06                   BEQ   CHAR       YES QUIT PADDING
002F 6F 00                   CLR   0,X        PAD WITH NULL
0031 08                      INX              INCR LOC PTR
0032 5A                      DEC B            DECREMENT SAFETY COUNTER
0033 26 F6                   BNE   PADL       LOOP TILL CR OR 64 NULLS
                   *    STORE ENTERED SOURCE CHAR IN PROGRAM
0035 A7 00         CHAR      STA A 0,X        CHAR TO SOURCE LOC
0037 08                      INX              MOVE LOC PTR UP ONE
0038 81 0D                   CMP A #$0D       IS IT A CR ?
003A 27 DF                   BEQ   EPLF       YES, ECHO A LINE FEED
003C 20 C5                   BRA   EGET       NO, GET ANOTHER CHAR
                   *    SUBROUTINE TO PRINT LINE FEED TO TERMINAL
003E C6 00         PLF       LDA B #$00       NUMBER OF NULLS TO PRINT
0040 4F            PLFL      CLR A            NULL
0041 8D 0B                   BSR   JOUT       WRITE A NULL
0043 5A                      DEC B            DECREMENT COUNTER
0044 2A FA                   BPL   PLFL       LOOP TILL ENOUGH NULLS
0046 86 0A                   LDA A #$0A       LINEFEED
0048 20 04                   BRA   JOUT
                   *    NEXT FEW LINES MUST BE ALTERED IF YOU DONT USE MIKBUG
004A BD E1AC       JIN       JSR   IN         CALL CHAR INPUT ROUTINE
004D 39                      RTS              RETURN TO CALLER
004E BD E1D1       JOUT      JSR   OUT        CALL CHARACTER OUTPUT ROUTINE
0051 39                      RTS              RETURN TO CALLER
                   *
                   *    COME HERE TO BEGIN EXECUTION OF THE SOURCE PROGRAM
                   *
0052 FE 0100       EXEC      LDX   LOC        STARTING LOC OF PROGRAM
0055 09                      DEX              LESS ONE
0056 08            LOOPI     INX              ADR OF NEXT PGM BYTE
0057 A6 00         LOOP      LDA A 0,X        NEXT PGM BYTE
0059 81 2A                   CMP A #$2A       *  CHAR ?
005B 2F F9                   BLE   LOOPI      YES(OR IGNOREABLE CONT CHAR)
                   *
                   *    PROCESS Y OR N FLAG TESTS
005D 81 59                   CMP A #$59       Y  ?
005F 27 04                   BEQ   TFLG       YES
0061 81 4E                   CMP A #$4E       N  ?
0063 26 0F                   BNE   XA         BRANCH IF NOT A FLAG TEST
                   *
0065 08            TFLG      INX              STEP LOC OVER Y OR N
0066 B1 0105                 CMP A FLG        COMPARE TO CURRENT MATCH FLAG
0069 27 EC                   BEQ   LOOP       ITS EQUAL SO EXECUTE THE STMT
                   *
                   *    ITS A FLAG FAILURE, SKIP OVER THE STMT
006B 08            SKIP      INX              STEP LOC PTR
006C A6 00                   LDA A 0,X        NEXT CHAR IN PGM
```

Listing 3: 6800 version of the WADUZITDO language. A dump of the MIKBUG format of WADUZITDO (shown in listing 3a, page 172) can be used for manual entry of the program. This version was run locally at BYTE using a SwTPC 6800.

Figure 2: Absolute loader format representation of the 8080 WADUZITDO program of listing 4.

000	001	002	003	004	005	006	007	008	009	010	011
0000	0019	0032	004B	0063	007B	0094	00AC	00C4	00DD	00F6	

```
006E 81 0D            CMP A #$0D     TO END OF STMT ?
0070 26 F9            BNE   SKIP     NOT YET, SO LOOP
0072 20 E2            BRA   LOOP1    AT NEXT STMT, GO DO IT
                *
                *  PROCESS ACCEPT STATEMENT
0074 81 41      XA    CMP A #$41     A  ?
0076 26 11            BNE   XM       NO
0078 FF 0102          STX   LST      YES, SAVE LOC OF LAST ACCEPT
007B 8D CD            BSR   JIN      ACCEPT ONE CHAR FROM KYBD
007D B7 0104          STA A CHR      SAVE IT
0080 08               INX            MOVE OVER A
0081 86 0D      PCR   LDA A #$0D     CR
0083 8D C9            BSR   JOUT     PRINT IT
0085 8D B7            BSR   PLF      PRINT LINE FEED
0087 20 CD            BRA   LOOP1    STEP OVER : AND GO ON
                *
                *  PROCESS MATCH STMT
0089 81 4D      XM    CMP A #$4D     M  ?
008B 26 12            BNE   XJ       NO
008D 08               INX            STEP OVER M
008E 08               INX            STEP OVER :
008F A6 00            LDA A 0,X      GET MATCH CHAR
0091 C6 59            LDA B #$59     ASSUME Y
0093 B1 0104          CMP A CHR      COMP MATCH CHAR TO INPUT CHAR
0096 27 02            BEQ   MX       BRANCH IF IT MATCHES,FLG=Y
0098 C6 4E            LDA B #$4E     RESULT IS N
009A F7 0105    MX    STA B FLG      SET MATCH FLAG TO Y OR N
009D 20 B7            BRA   LOOP1    STEP OVER MATCH CHAR AND GO ON
                *
                *  PROCESS JUMP STATEMENT
009F 81 4A      XJ    CMP A #$4A     J  ?
00A1 26 17            BNE   XS       NO
00A3 E6 02            LDA B 2,X      DESTINATION


00A5 C4 0F            AND B #$0F     CLEAR ZONE
00A7 26 05            BNE   JF       ITS A JUMP FORWARD
00A9 FE 0102          LDX   LST      ZERO.. JUMP BACK TO LAST ACCEPT
00AC 20 A9            BRA   LOOP     CONTINUE FROM THERE
                *
                *  SKIP FORWARD UNTIL PASS N *-MARKERS ( N IS IN ACCB )
00AE 08         JF    INX            STEP PGM LOC
00AF A6 00            LDA A 0,X      NEXT CHAR
00B1 81 2A            CMP A #$2A     *-MARKER ?
00B3 26 F9            BNE   JF       NO, KEEP LOOPING
00B5 5A               DEC B          FOUND ONE, COUNT IT
00B6 26 F6            BNE   JF       LOOP IF NEED TO FIND MORE
00B8 20 9C            BRA   LOOP1    DESTINATION FOUND, GO EXECUTE
                *
                *  PROCESS STOP OR SUBROUTINE STATEMENT
00BA 81 53      XS    CMP A #$53     S  ?
00BC 26 0A            BNE   XT       NO
00BE 08               INX            STEP OVER S
00BF 08               INX            STEP OVER :
00C0 A6 00            LDA A 0,X      PARAMETER TO REG A
00C2 08               INX            STEP OVER PARAMETER
                *  NEXT STMT MAY BE MADE TO BE A  JSR TO USER SUBR
00C3 7E 0000          JMP   SUB      GO TO USER SUBR (OR TO EDITOR)
00C6 20 8F            BRA   LOOP     GO ON UPON RETURN FROM USER SUBR
                *
                *  PROCESS TYPE STATMENT AND SYNTAX ERRORS
00C8 81 54      XT    CMP A #$54     T  ?
00CA 26 02            BNE   TE       NO, ITS AN ERROR
00CC 08               INX            YES, STEP OVER T
00CD 08               INX            STEP OVER :
00CE 8D 05      TE    BSR   PRT      PRINT UP TO CR
00D0 BD 003E          JSR   PLF      PRINT LNE FEED
00D3 20 82            BRA   LOOP     DONE WITH T
                *
                *  SUBR TO PRINT UP TO NEXT CR
00D5 C6 40      PRT   LDA B #$40     COUNT OF 64
00D7 A6 00      PRTA  LDA A 0,X      NEXT CHAR
00D9 5A               DEC B          DECREMENT SAFETY COUNTER
00DA 27 0A            BEQ   PRTB     EXIT IF OVER 64 TILL CR
00DC BD 004E          JSR   JOUT     PRINT IT
00DF A6 00            LDA A 0,X      RELOAD CHAR TO ACCA
00E1 08               INX            STEP LOC PTR
00E2 81 0D            CMP A #$0D     CR ?
00E4 26 F1            BNE   PRTA     NOT CR, LOOP
00E6 39         PRTB  RTS            DONE, RETURN
                *
                *  ABOVE IS END OF READ ONLY PORTION OF THE PROGRAM
                *
                *  THE FOLLOWING IS CHANGEABLE DATA
                *
                      ORG   $100     MOVE TO START OF DATA AREA
0100      0106  LOC   FDB   $0106    ADDR OF SOURCE PROGRAM AREA
0102      0000  LST   FDB   0        PLACE TO SAVE LOC OF LAST A:
0104      00    CHR   FCB   0        PLACE TO SAVE LAST INPUT CHAR
0105      00    FLG   FCB   0        PLACE TO SAVE MATCH FLAG
                *
                      END
```

Listing 4: 8080 version of the WADUZITDO language. A hexadecimal dump (shown in listing 4a) is provided for manual entry. This version was run locally at BYTE using a SOL-20.

```
                 *                  WADUZITDO
                 *        8080 VERSION BY LARRY KHERIATY
                 *
                 *     SOLOS/CUTER SUBROUTINES USED
                 IN         EQU     0C01FH      INPUT FROM KEYBOARD TO A-REG
                 OUT        EQU     0C019H      OUTPUT FROM B-REG TO TERMINAL
                 *
                            ORG     0000H
                 SUB        EQU     0000H       USER SUBR START (CAN BE MODIFIED)
                 *    ENTER SYSTEM AT LOCATION 0 WITH STACK POINTER PRESET
                 *    TO SCRATCH PAD RAM ENOUGH FOR A FEW LEVELS OF CALL
                 *
0000 2A 0001     START      LHLD    LOC         SOURCE PROGRAM AREA START
0003 CD 4600     EGET       CALL    JIN         ACCEPT SOURCE CHAR
0006 FE 5C                  CPI     5CH         \  ?
0008 CA 0000                JZ      START       YES, BACK UP TO PROGRAM START
                 *
000B FE 24                  CPI     24H         $  ?
000D CA 5200                JZ      EXEC        YES, GO EXECUTE THE PROGRAM
                 *
0010 FE 5F                  CPI     5FH         BS   ?
0012 C2 1900                JNZ     DIS         NO
0015 2B                     DCX     H           YES, BACK UP ONE IN SOURCE
0016 C3 0300                JMP     EGET        LOOP BACK
                 *
                 *    PROCESS DISPLAY OF NEXT LINE
0019 FE 2F       DIS        CPI     2FH         /  ?
001B C2 2400                JNZ     PAD         NO
001E CD DF00                CALL    PRT         GO PRINT TO CR
0021 C3 0300                JMP     EGET        LOOP
                 *
                 *    DO LINE REPLACEMENT- PAD TO END OF STMT WITH NULLS
0024 FE 25       PAD        CPI     25H         %  ?
0026 C2 3C00                JNZ     CHAR        NO
0029 06 0D                  MVI     B,0DH       CR
002B 78                     MOV     A,B         CR TO A ALSO
002C CD 4D00                CALL    JOUT        PRINT IT
002F 0E 40                  MVI     C,40H       COUNT OF 64
0031 BE          PADL       CMP     M           AT CR YET ?
0032 CA 3C00                JZ      CHAR        YES QUIT PADDING
0035 36 00                  MVI     M,00H       PAD WITH NULL
0037 23                     INX     H           INCR LOC PTR
0038 0D                     DCR     C           DECREMENT SAFETY COUNTER
0039 C2 3100                JNZ     PADL        LOOP TILL CR OR 64 NULLS
                 *
                 *    STORE ENTERED SOURCE CHAR IN PROGRAM
003C 77          CHAR       MOV     M,A         CHAR TO SOURCE LOC
003D 23                     INX     H           MOVE LOC PTR UP ONE
003E FE 0D                  CPI     0DH         IS IT A CR ?
0040 CC F000                CZ      PLF         YES, ECHO A LINE FEED
0043 C3 0300                JMP     EGET        NO, GET ANOTHER CHAR
                 *
                 *    CHANGE NEXT FEW LINES IF YOU DONT USE SOLOS/CUTER
0046 CD 1FC0     JIN        CALL    IN          CALL CHAR INPUT ROUTINE
0049 CA 4600                JZ      JIN         TRY AGAIN IF NO CHAR YET THERE
004C 47                     MOV     B,A         PREPARE TO ECHO THE CHAR
004D CD 19C0     JOUT       CALL    OUT         CALL CHARACTER OUTPUT ROUTINE
0050 78                     MOV     A,B         RESTORE JIN CHAR TO A
0051 C9                     RET                 RETURN TO CALLER
                 *
                 *    COME HERE TO BEGIN EXECUTION OF THE SOURCE PROGRAM
                 *
0052 2A 0001     EXEC       LHLD    LOC         STARTING LOC OF PROGRAM
0055 2B                     DCX     H           LESS ONE
0056 23          LOOPI      INX     H           ADR OF NEXT PGM BYTE
0057 7E          LOOP       MOV     A,M         NEXT PGM BYTE
0058 FE 2B                  CPI     2BH         *  CHAR ? (NOTE 2BH IS '*'+1)
005A FA 5600                JM      LOOPI       YES(OR IGNOREABLE CONT CHAR)
                 *
                 *    PROCESS Y OR N FLAG TESTS
005D FE 59                  CPI     59H         Y  ?
005F CA 6700                JZ      TFLG        YES
0062 FE 4E                  CPI     4EH         N  ?
0064 C2 7600                JNZ     XA          BRANCH IF NOT A FLAG TEST
                 *
0067 23          TFLG       INX     H           STEP LOC OVER Y OR N
0068 BA                     CMP     D           COMPARE TO CURRENT MATCH FLAG
0069 CA 5700                JZ      LOOP        ITS EQUAL SO EXECUTE THE STMT
                 *
                 *    ITS A FLAG FAILURE, SKIP OVER THE STMT
006C 23          SKIP       INX     H           STEP LOC PTR
006D 7E                     MOV     A,M         NEXT CHAR IN PGM
006E FE 0D                  CPI     0DH         TO END OF STMT ?
0070 C2 6C00                JNZ     SKIP        NOT YET, SO LOOP
0073 C3 5600                JMP     LOOPI       AT NEXT STMT, GO DO IT
                 *
                 *    PROCESS ACCEPT STATEMENT
0076 FE 41       XA         CPI     41H         A  ?
0078 C2 8E00                JNZ     XM          NO
```

```
S1130000FE0100BD45815C27F78124274581092660
S1130010030920EF812F2607BD00D58D2120E4811F
S1130020252612860D8D27863DC640A100270A6F52
S1130030000085A26F6A70009810D27DF20C5C60950
S11300404F8D035A2AFA860A20049DE1AC398DE179
S1130050D139FE01000908A600812A2FF98159927 08
S113006004814E260F08B1010527EC08A600810D76
S113007026F920E281412611FF01028DCD8701044A
S113008008860D8DC98DB720CD814D26120808A69E
S113009000C659B101042702C64EF7010520B781F5
S11300A04A2617E602C40F2605FE010220A90BA667
S11300B000812A26F95A26F6209C8153260A08082C
S11300C0A600087E0000208F8154260208089D05B2
S11300D08D003E2092C640A60054270ABD004EA697
S10A00E00008810D26F1392F
```

Listing 3a: MIKBUG format for the 6800 version of WADUZITDO.

```
00002A0001CD4600FE5CCA0000FE24CA5200
0010FE5FC219002BC30300FE2FC22400CDDF
002000C30300FE25C23C00060D78CD4D000E
003040BECA3C003600230DC231007723FE0D
0040CCF000C30300CD1FC0CA460047CD19C0
005078C92A00012B237EFE2BFA5600FE59CA
00606700FE4EC27600238ACA5700237EFE0D
0070C26C00C35600FE41C28E00220201CD46
0080005F23060DCD4D00CDF000C35600FE4D
0090C2A10023237E1659BBCA9E00164EC356
00A000FE4AC2C30023237EE60F47C295002A
00B00201C35700237EFE2AC2B50005C2B500
00C0C35600FE53C2D20023237E23C30000C3
00D05700FE54C2D9002323CDDF00C357000E
00E040460DCAF000CD4D007E23FE0DC2E100
00F00E000600CD4D000DF2F200060AC34D00
0100060100000000
```

Listing 4a: Dump of the 8080 version of WADUZITDO. The format consists of 4 character hexadecimal address and 16 hexadecimally coded bytes of information. There is no checksum computed for any of the information.

PAPERBYTE^{tm} Bar Codes for WADUZITDO

In figure 1 and figure 2, we provide a PAPERBYTE^{tm} bar code representation for the WADUZITDO programs of listing 3 and listing 4. These bar code representations were created in the absolute loader format documented in detail in the PAPERBYTE book, Bar Code Loader, *written by Ken Budnick of Micro-Scan Associates, and available for $2 at local computer stores or by mail (add $.75 postage and handling) from BITS Inc, 25 Route 101 W, Peterborough NH 03458.*

Text continued from page 168

the index register (6800) or HL register pair (8080) contains the location of the next program statement and should be saved and restored before returning from the subroutine. In the 8080 version the DE register pair should also be saved. Register A will contain the one character parameter, x, of the S:x. Its use is totally up to the subroutine.

The system has been organized so that the six bytes of changeable data are isolated from the read only portion. This means the rest of the 256 byte system could be placed in read only memory. It would fit in a single 1702A EROM chip.

It is easy to see how this language could be used to write a question and answer conversation using multiple choice or true, false answers. It may not be so obvious that more complex logic is possible. The example in listing 2 is a computer versus user NIM game which demonstrates a way this can be done.

Although WADUZITDO is not the ultimate answer to personal computing, it is something that almost anyone can have some fun with, and it definitely squeezes the most out of 256 bytes of memory.

A Pascal WADUZITDO

Notes by Ray Cote
Program by Larry Kheriaty

Along with the assembly language versions of WADUZITDO, Larry Kheriaty sent us the Pascal version shown in listing 5. The program is basically self-documenting and very easy to translate into assembly level programs for any particular processor. The program is indented to show logical relationships between related areas of text. This is sometimes known as prettyprinting.

The first four lines of the program are definition lines for the main program. In Pascal, all variables must be defined completely at the start of the section in which they are used. "Completely" means name and data type. This is a great help since all variables must be explicitly defined. You can easily check to see what type of variable is being used.

WADUZITDO uses two types of var-

Listing 4, continued:

```
007B 22 0201             SHLD  LST      YES, SAVE LOC OF LAST ACCEPT
007E CD 4600             CALL  JIN      ACCEPT ONE CHAR FROM KYBD
0081 5F                  MOV   E,A      SAVE IT
0082 23                  INX   H        MOVE OVER A
0083 06 0D               MVI   B,0DH    CR
0085 CD 4D00             CALL  JOUT     PRINT IT
0088 CD F000             CALL  PLF      PRINT LINE FEED
008B C3 5600             JMP   LOOPI    STEP OVER : AND GO ON
               *
               *   PROCESS MATCH STMT
008E FE 4D     XM        CPI   4DH      M  ?
0090 C2 A100             JNZ   XJ       NO
0093 23                  INX   H        STEP OVER M
0094 23                  INX   H        STEP OVER :
0095 7E                  MOV   A,M      GET MATCH CHAR
0096 16 59               MVI   D,59H    ASSUME Y
0098 BB                  CMP   E        COMP MATCH CHAR TO INPUT CHAR
0099 CA 9E00             JZ    MX       BRANCH IF IT MATCHES,FLG=Y
009C 16 4E               MVI   D,4EH    RESULT IS N
009E C3 5600 MX          JMP   LOOPI    SET MATCH FLAG TO Y OR N
               *
               *   PROCESS JUMP STATEMENT
00A1 FE 4A     XJ        CPI   4AH      J  ?
00A3 C2 C300             JNZ   XS       NO
00A6 23                  INX   H        STEP OVER J
00A7 23                  INX   H        STEP OVER :
00A8 7E                  MOV   A,M      DESTINATION
00A9 E6 0F               ANI   0FH      CLEAR ZONE
00AB 47                  MOV   B,A      NUMBER OF *S TO SKIP
00AC C2 B500             JNZ   JF       ITS A JUMP FORWARD
00AF 2A 0201             LHLD  LST      ZERO.. JUMP BACK TO LAST ACCEPT
00B2 C3 5700             JMP   LOOP     CONTINUE FROM THERE
               *
               *   SKIP FORWARD UNTIL PASS N *-MARKERS ( N IS IN BREG )
00B5 23        JF        INX   H        STEP PGM LOC
00B6 7E                  MOV   A,M      NEXT CHAR
00B7 FE 2A               CPI   2AH      *-MARKER ?
00B9 C2 B500             JNZ   JF       NO, KEEP LOOPING
00BC 05                  DCR   B        FOUND ONE, COUNT IT
00BD C2 B500             JNZ   JF       LOOP IF NEED TO FIND MORE
00C0 C3 5600             JMP   LOOPI    DESTINATION FOUND, GO EXECUTE
               *
               *   PROCESS STOP OR SUBROUTINE STATEMENT
00C3 FE 53     XS        CPI   53H      S  ?
00C5 C2 D200             JNZ   XT       NO
00C8 23                  INX   H        STEP OVER S
00C9 23                  INX   H        STEP OVER :
00CA 7E                  MOV   A,M      PARAMETER TO REG A
00CB 23                  INX   H        STEP OVER PARAMETER
               *   NEXT STMT MAY BE MADE TO BE A CALL TO USER SUBR
00CC C3 0000             JMP   SUB      GO TO USER SUBR (OR TO EDITOR)
00CF C3 5700             JMP   LOOP     GO ON UPON RETURN FROM USER SUBR
               *
               *   PROCESS TYPE STATMENT AND SYNTAX ERRORS
00D2 FE 54     XT        CPI   54H      T  ?
00D4 C2 D900             JNZ   TE       NO, ITS AN ERROR
00D7 23                  INX   H        YES, STEP OVER T
00D8 23                  INX   H        STEP OVER :
00D9 CD DF00 TE          CALL  PRT      PRINT UP TO CR
00DC C3 5700             JMP   LOOP     DONE WITH T
               *
               *   SUBR TO PRINT UP TO NEXT CR
00DF 0E 40     PRT       MVI   C,40H    COUNT OF 64
00E1 46        PRTA      MOV   B,M      NEXT CHAR
00E2 0D                  DCR   C        DECREMENT SAFETY COUNTER
00E3 CA F000             JZ    PLF      EXIT IF OVER 64 BEFORE CR
00E6 CD 4D00             CALL  JOUT     PRINT IT
00E9 7E                  MOV   A,M      RELOAD CHAR TO ACCA
00EA 23                  INX   H        STEP LOC PTR
00EB FE 0D               CPI   0DH      CR ?
00ED C2 E100             JNZ   PRTA     NOT CR, LOOP
               *
               *   SUBROUTINE TO PRINT LINE FEED AND PAD
00F0 0E 00     PLF       MVI   C,00H    NUMBER OF NULLS TO PRINT
00F2 06 00     PLFL      MVI   B,00H    NULL
00F4 CD 4D00             CALL  JOUT     WRITE A NULL
00F7 0D                  DCR   C        DECREMENT COUNTER
00F8 F2 F200             JP    PLFL     LOOP TILL ENOUGH NULLS
00FB 06 0A               MVI   B,0AH    LINE FEED
00FD C3 4D00             JMP   JOUT     PRINT THEN RETURN
               *
               *   ABOVE IS END OF READ ONLY PORTION OF THE PROGRAM
               *
               *   THE FOLLOWING IS CHANGEABLE DATA
               *
                         ORG   0100H    MOVE TO START OF DATA AREA
0100 0601      LOC       DW    0106H    ADDR OF SOURCE PROGRAM AREA
0102 0000      LST       DW    0000H    PLACE TO SAVE LOC OF LAST A:
               *   THE NEXT TWO BYTES ARE ONLY FOR 6800 COMPATIBILITY
0104 00        CHR       DB    00H      UNUSED, LAST INPUT CHAR IN EREG
0105 00        FLG       DB    00H      UNUSED,MATCH-FLAG IN DREG
               *
                         END
```

iables: integer and character. There is also a definition for constants (CONST). CONST informs the compiler that the value being assigned to this variable will not change. Integer variables will only take on whole number values.

The type character (CHAR) means that the variables will take on the values of ASCII characters, including all letters, numbers and special symbols.

The last line of the definition section defines a variable PROG as an array of characters. This definition also states that the relative base address of the array will be unity and the variable PZ will be used to specify locations within the array.

After defining our variables we are ready to start the first executable part of the program. In Pascal, the logical parts of the program are broken into procedures, equivalent to subroutines in languages such as FORTRAN. Every procedure is blocked off by BEGIN and END statements. The name of the first procedure is CHIN. After we have determined the name, we are told to begin executing procedure ACCEPT (which will return to us input values in variable CBUF). This is a subroutine which is not shown since it is specific to the processor being used. The next two procedures are also calls to subroutines used to DISPLAY the contents of the buffer and move the output to a new line. These two procedures are also machine dependent. Notice that Pascal allows you to use descriptive names. This is very important when writing a program that you want other people to read or that you want to understand at a later date.

The next procedure, LIST, first defines its own local variables, which it will use only within the LIST routine. As before, the procedure is delimited by BEGIN and END statements. This procedure introduces us to the concept of loops. Here we have a related pair of commands: REPEAT and UNTIL. These two commands cause the one line of three instructions and the call to procedure CHOUT to execute until either the value I is greater than 64 or the variable CBUF is equal to CEOL. Once either of these two conditions occurs, the program logic proceeds to call procedure NEWLINE. At this point the LIST procedure ends and returns to whatever procedure called it.

Procedure EXECUTE looks structurally the same as procedure LIST. There is a definition of variables, the BEGIN and END delimiters, and a REPEAT-UNTIL structure. This time the REPEAT-UNTIL statement is not waiting for a relation to be true, but is rather checking against one variable. Looking at how DONE was defined at the beginning of the procedure, we see that its designation is BOOLEAN. This means that the variable is being used as a logical variable and can take on the value true or false. The REPEAT-UNTIL instruction waits to see if the variable DONE is true. If so, we have finished this procedure and can stop it.

Listing 5: Pascal listing of WADUZITDO. See notes by Ray Cote.

```
PASCAL VERSION OF WADUZITDO, LARRY KHERIATY
PROGRAM WADUZITDO;
  CONST PZ=5000; BS=127; EOL=10;
  VAR LOC,LST,I : INTEGER; LCHR,FLG,CBUF,CBS,CEOL : CHAR;
    PROG : ARRAY[1..PZ] OF CHAR;

  PROCEDURE CHIN; BEGIN ACCEPT (CBUF); END;
  PROCEDURE CHOUT; BEGIN DISPLAY (CBUF); END;
  PROCEDURE NEWLINE; BEGIN DISPLAY (NL) ; END;

  PROCEDURE LIST; VAR I:INTEGER;
    BEGIN I:= 0;
      REPEAT
        CBUF := PROG [LOC]; LOC := LOC+1; I:=I+1;
        CHOUT
      UNTIL (I>64) OR (CBUF=CEOL); NEWLINE
    END;

  PROCEDURE EXECUTE; VAR DONE : BOOLEAN;
    BEGIN LOC := 1; DONE := FALSE;
      REPEAT
        CBUF := PROG[LOC] ; IF CBUF < '*' THEN CBUF := '*';
        IF NOT(CBUF IN ['*','Y','N','A','M','J','T','S'])THEN LIST ELSE
          CASE CBUF OF
            '*': LOC := LOC+1;
            'Y','N' : IF CBUF=FLG THEN LOC := LOC+1
                      ELSE REPEAT CBUF := PROG[LOC]; LOC:=LOC+1
                           UNTIL CBUF=CEOL;
            'A' : BEGIN LST := LOC; CHIN; LCHR :=CBUF;
                    NEWLINE; LOC :=LOC+2 END;
            'M' : BEGIN IF LCHR=PROG[LOC+2] THEN FLG :='Y'
                        ELSE FLG := 'N';
                    LOC := LOC+3 END;
            'J' : IF PROG[LOC+2] = '0' THEN LOC :=LST
                  ELSE BEGIN I:= ORD(PROG[LOC+2])-48;
                         REPEAT LOC:=LOC+1;
                           IF PROG[LOC] = '*' THEN I := I-1
                         UNTIL I=0 END;
            'T' : BEGIN LOC := LOC+2; LIST END;
            'S' : BEGIN DONE := TRUE; LOC := 1 END
          END
      UNTIL DONE
  END;

  BEGIN CBS := CHR(BS); CEOL := CHR(EOL); CBUF :='\';
    WHILE TRUE DO BEGIN
      IF CBUF ='\' THEN LOC :=1
      ELSE IF CBUF=CBS THEN LOC := LOC-1
      ELSE IF CBUF='/' THEN LIST
      ELSE IF CBUF='$' THEN EXECUTE
      ELSE IF CBUF='%' THEN
        BEGIN I:=0;
          WHILE (I<64) AND (PROG[LOC] <> CEOL) DO
            BEGIN PROG[LOC] := CHR(0); LOC := LOC+1 END;
          PROG[LOC] := CEOL; LOC := LOC +1; NEWLINE
        END
      ELSE BEGIN PROG[LOC] := CBUF; LOC := LOC+1;
        IF CBUF=CEOL THEN NEWLINE END;
      CHIN
   END
  END.
```

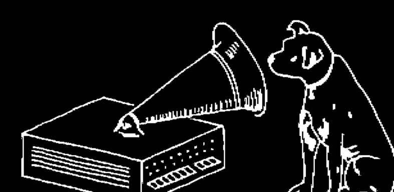
Procedure EXECUTE also contains an IF-THEN-ELSE statement. If the value of CBUF is not contained within the brackets, perform procedure LIST. If the value of CBUF is somewhere within the square brackets, we want to perform an operation related to that value. We now come to another Pascal instruction, the CASE statement.

We are given a set of cases to choose from. The CASE statement tells us that we will be using the value in variable CBUF to determine what is to be done. We scan down each of the cases and find the one labeled with the value in CBUF. Since CBUF is type character we are looking at ASCII characters. Once we find the value of CBUF we execute the statements associated with it that are blocked off by another set of BEGIN and END statements. After we have finished, we move to the end of the CASE statement and then the last line of REPEAT-UNTIL statement.

The next section of the program does not look like the preceding sections. It does not start with a PROCEDURE statement, but has a BEGIN statement. So far we have discussed procedures. Any of the procedures that needed to use variables have defined their own. So why did we define those variables at the very beginning of the program? The reason is not to use them in a procedure, but to use them in the main program. This BEGIN statement is nothing more than the start of the mainline logic for program WADUZITDO. The mainline logic inputs characters and either stores them in an array as program or executes them as commands. This routine will not jump out of the loop and will have to be interrupted to stop. Of course it is possible to create another command that will allow you to exit from this cycle.

Now that we have looked at the Pascal version of WADUZITDO, the reader should refer back to either of the assembly versions. The Pascal version performs the same function as the assembly versions.

The assembly language versions need to be heavily commented for the reader to understand what is happening. Even liberal comments will not help when converting from one assembly language to another. The Pascal version can be easily converted into any machine language. It is also self-documenting. Notice that even without a single comment, the Pascal listing is extremely easy to decipher. . . . RGAC■



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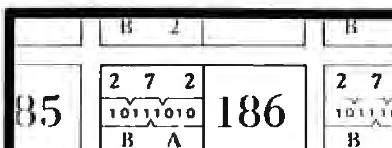

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What's New?

Is It a Plot?

Here is one of the most exciting peripherals available for the personal computer user who is interested in graphic arts applications: a very affordable ($1085) digital plotter from Houston Instrument called the Hi Plot. The statistics on this machine are impressive to say the least. The resolution of the pen tip is either .005 inch or 0.01 inch giving a total of 1400 by 2000 picture elements or 700 by 1000 picture elements respectively in its 7 by 10 inch (17.8 cm by 25.4 cm) plotting area. Standard ink cartridges are available in four colors, allowing the user to switch cartridges to produce mixed color plots. According to Tom Hall of Houston Instrument it is also possible for the individual user to kludge a standard drafting ink pen into the plotter, allowing a much wider selection of colors to be used in the form of personally chosen inks.

Many of the plotting samples seen in this issue should be reproducible by the small system owner who uses this peripheral, a typical personal system with a high level language and floppy disks, and some imagination.

Complete and ready to plot, the Hi Plot costs $1085. Contact Houston Instrument, One Houston Square, Austin TX 78753.■

Circle 569 on inquiry card.

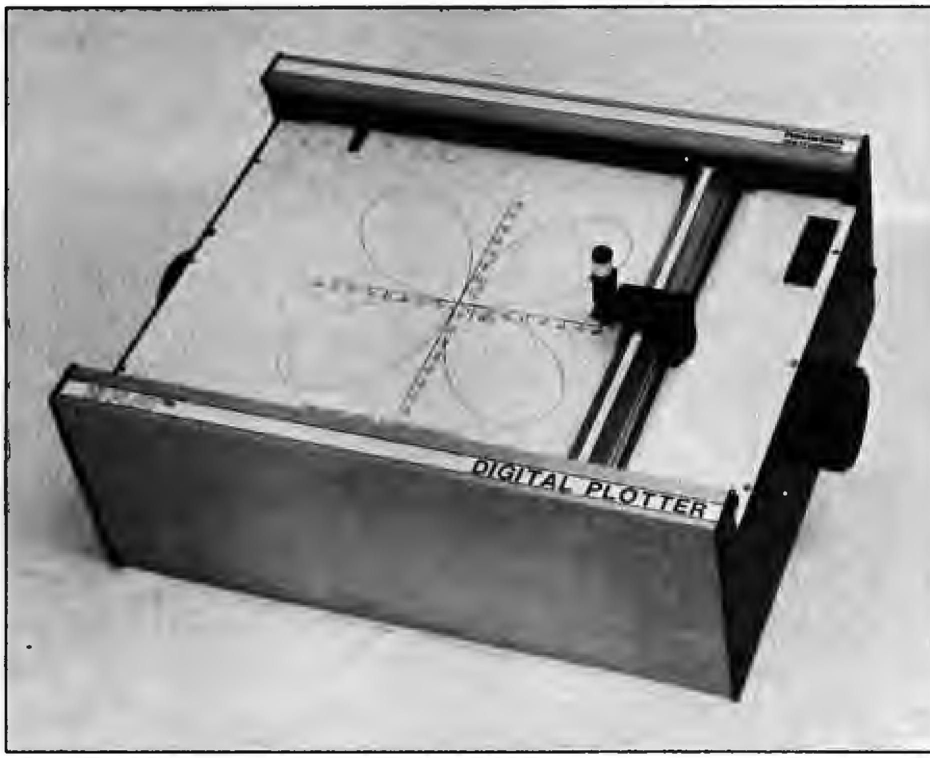


Photo 1: The new Houston Instrument's Hi Plot plotter is shown here in a typical analytical situation: plotting a polar coordinate function in the plane of the paper with Cartesian axes for reference.

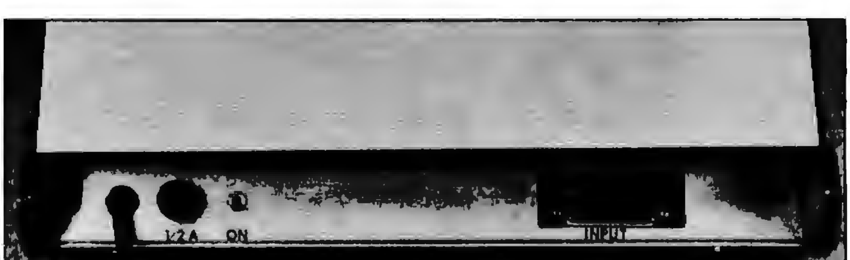


Photo 2: The interface to the user's computer is via a standard DB-25 connector located on the lower edge of the rear panel of the plotter.

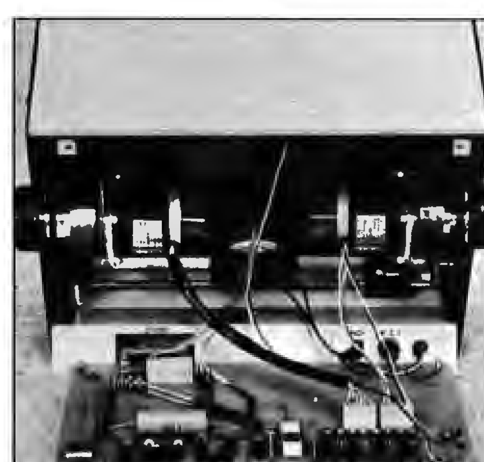


Photo 3: Inside the Hi Plot plotter, we find this pair of stepper motors which drive the mechanism through cable linkages.

Write for Free North Star Newsletter and Catalog

North Star Computers Inc, 2547 Ninth St, Berkeley CA 94710, is offering the latest issue of its newsletter free on request. In this issue North Star announces eight new application software diskettes and lists more than 50 commercially available application programs ready for use on North Star equipment. In addition, North Star's 16 page product catalog is also available free of charge.■

Circle 570 on inquiry card.

Micropolis Announces Double Sided Floppy Disk Drives

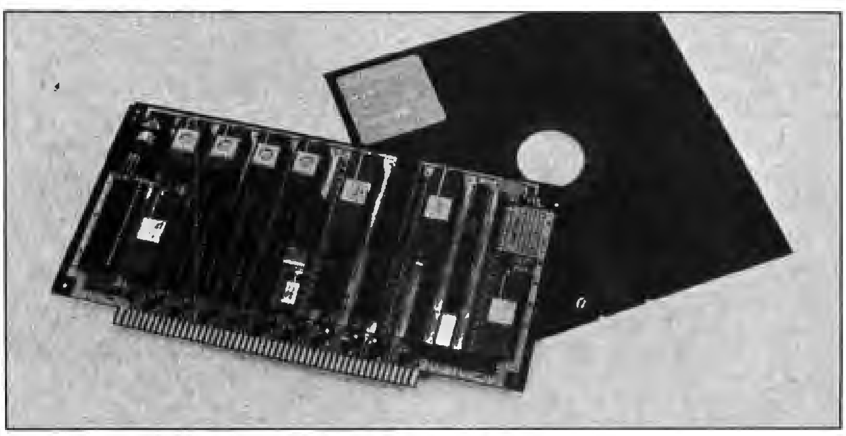
Double sided floppy disk drives are now available on two of Micropolis Corp's OEM series. The company's Mega-Floppy series, Models 1015 and 1055, features an intelligent controller that facilitates interconnection of four subsystems to a common host interface for a total on line storage capacity of more than 15 M bytes.

The 1015 is an unpackaged drive designed to integrate floppy disk storage into a system enclosure. This series is expanded to four products of double sided options. Storage capacity ranges from 143 K bytes to 630 K bytes per drive. The Model 1015's file space may be optionally expanded up to 946 K bytes by using the Micropolis intelligent controller and group code recording (GCR) method. The 5¼ inch floppy offers GCR and a microprocessor based controller as standard features. Model 1055 has four soft sectored formats for each of its 77 tracks, yielding a maximum capacity of 1892 K bytes of useable file space on its double sided version. An optional add on module, comprised of two read and write heads and two drives sharing a common controller, increases the subsystem formatted capacity to 3784 K bytes.

The 35 track configuration single drive, double sided 1015 Model III with 287 K bytes of formatted capacity is priced at $330 in quantities of 500. A quad density version, the 1015 Model IV, which has 77 tracks per surface and a track density of 100 tracks per inch with up to 946 K bytes formatted capacity, is $396. The Micropolis intelligent controller is a $369 option on the quad density version when purchased in quantities of 500. The Model 1055 Model IV, which includes the intelligent controller, power supply, bidirectional interface, enclosure and almost 2 M bytes of on line capacity, is priced at $1796 in quantities of 50. For further information, contact Micropolis Corp, 3959 Deering Av, Canoga Park CA 91304.■

Circle 556 on inquiry card.

Intelligent Double Density Diskette Controller



This new stand alone intelligent controller, the PerSci Model 1170, is capable of managing either single or double density recording on as many as 32 diskette sides for a total system formatted data capacity of 16 M bytes.

The controller is a compact computer for use in diskette subsystem management and microcomputer applications. It uses microprocessor intelligence to communicate by file name and to assume the housekeeping functions usually performed by the processor. File management functions include initialization; allocation and deallocation of diskette space; error detection and retry; creating, deleting, renaming, copying of files; and diagnostic testing.

Designed to operate PerSci's recently introduced Model 299 drive, the 1170 is also capable of handling two PerSci Model 277 dual diskette drives or various combinations of Models 299 and 277.

The price is $800 in large quantities.

Contact PerSci Inc, 12210 Nebraska Av, W Los Angeles CA 90025. ■

Circle 557 on inquiry card.

Improved System Disk for System 88

PolyMorphic Systems has announced a second system software edition for their System 88 microcomputers, making them faster and easier to use. The software includes an enhanced operating system, BASIC, text editor and assembler.

Added to the BASIC language are string arrays and array commands that allow the user to create and manipulate labels for tables and charts, mailing lists, personnel records, inventory, and billing, and so on. For the scientific user, BASIC now has inverse trigonometric, hyperbolic and gamma functions. Also included are new statistical functions that simplify data reduction.

The System 88 text editor now permits the user to move, copy, or delete an entire block of text. Cursor movements are now two-dimensional; the original cursor movements have been retained. For further information, contact PolyMorphic Systems, 460 Ward Dr, Santa Barbara CA 93111.■

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- MARK FREQUENCY: 1200 Hz; SPACE FREQUENCY: 2200 Hz.
- REVERSE CHANNEL COMMUNICATION over 2-wire lines at 5 Baud (387 Hz.)
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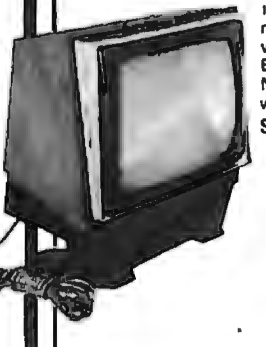

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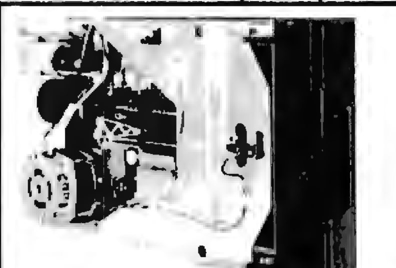

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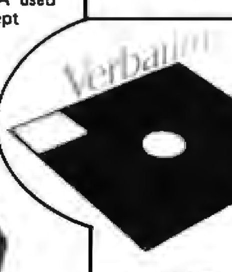

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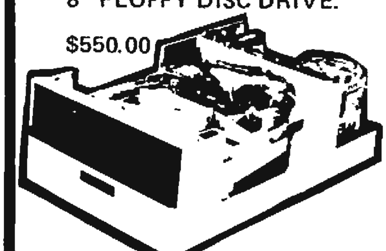

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FLOPPY DISC INTERFACE
JADE Floppy Disc (Tarbell Board) KIT **$175.00 ea.**
S.D. Computer Products Versa Floppy Kit **$149.00 ea.**
Assembled & Tested **$189.00 ea.**

STATIC RAM BOARDS
ASSEMBLED & TESTED
8K

Ram 8 (250ns)	$169.95
Ram 8B (450ns)	$139.95
250ns KIT Mem-1	$169.95
450ns KIT Mem-1	$125.00
BARE BOARD	$25.00

16K Uses 2114 (lo pwr.)

Ram 16 (250ns)	$375.00
Ram 16B (450ns)	$325.00
MEM-2 Kit (250ns)	$285.00

32K Assembled & Tested by SEALS ELECTRONICS

JG-32 (250ns)	$795.00
JG-32B (450ns)	$725.00
250ns KIT	$575.00

6800 Adapter - adapts Mem-1 8K board to Motorola MEK 6800D2 evaluation kit.

16K STATIC BOARD
with memory management can be used with Alpha Micro or Cromenco Systems. ASSEMBLED & TESTED

RAM 65(250ns)	$390.00
RAM 65B (450ns)	$350.00

E-PROM BOARDS

MR-8 (8K uses 2708) KIT with 1K RAM	$99.50
MR-16T (16K uses 2716) KIT with 1K RAM	$99.50
EPM-1 (uses up to 4K of 1702)	$59.95
RAM/N/ROM (16K uses any E-PROM) KIT	$117.00
JG-8/16 (uses 2708 or 2716) KIT	$59.95
BARE BOARD	$30.00

EXPANDABLE E-PROM — S.D. Computer Products
16K or 32K EPROM **$49.95** without EPROM
Allows you to use either 2708's for 16K of Eprom or 2716's for 32K of EPROM.

COMPUTER MAINFRAME
Includes: **$295.00**
Power Supply +8v at 18amps
±16v at 2 amps
Mother Board - 12 slots with connectors Assembled & Tested
Has Whisper Quiet Fan & AC Line Filter
Cabinet size 7"H x 19"W x 22" D

DYNAMIC RAM BOARD
by S. D. Computer Products
On board refresh is provided with no wait states or cycle stealing required. +8VDC 400MA DC, +18VDC 400MA and -18VDC 30MA DC.

EXPANDABLE 32K uses 4115 (2oons)
8K Kit $151.00 24K Kit $325.00
16K Kit $240.00 32K Kit $400.00
EXPANDABLE 64K uses 4116 (200ns)
16K Kit $250.00 48K Kit $675.00
32K Kit $475.00 64K Kit $875.00

JADE 16K DYNAMIC KIT
uses 4096 (300ns) **$200.00**

JADE Z80 KIT
with PROVISIONS for ONBOARD 2708 and POWER ON JUMP

(2MHZ)	$135.00ea.
Assembled & Tested	$170.00ea.
(4MHZ)	$149.95ea.
Assembled & Tested	$184.95ea.
Bare Board	$35.00ea.

JADE VIDEO INTERFACE KIT
KIT **$99.95**
Assembled & Tested **$139.95**

S-100 Bus compatible
32 or 64 Characters per line - 16 lines
Graphics (128 x 48 matrix)
Parallel & compositive video
On board low-power memory
Powerful software included for cursor, home, EOL, Scroll Graphics/Character Upper case, lower case and Greek. Black-on-white & White-on-black.

JADE PARALLEL/SERIAL INTERFACE KIT
KIT **$124.95**
Assembled & Tested **$154.95**

- S-100
- 2 Serial interfaces with RS232 interfaces or 1 Kansas City cassette interface.
- Serial interfaces are crystal controlled
- Selectable baud rates.
- Cassette works up to 1200 baud.
- 1 parallel port.

TV-1
Convert T.V set to Video Monitor
KIT . . . **$8.95**

JADE 8080A KIT
$100.00 kit
BARE BOARD $30.00

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4901 W. Rosecrans-W
Hawthorne, Calif. 90250

Freight Charge $2.00 less than 10-lbs.

NEW CATALOG NOW AVAILABLE

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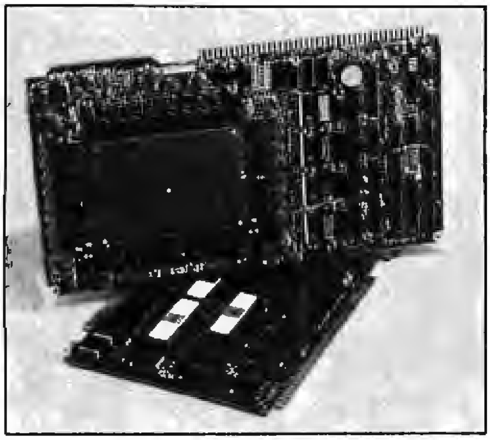
"THE PIGGY IS COMING"

Circle 195 on inquiry card.

Ampex MCM-8080 Core Memory Board



This 16 K byte core memory for 8080 microcomputers is now available from Ampex Corp, 200 N Nash St, El Segundo CA 90245. Fully compatible with SBC 80 single board computers, the MCM-8080 provides nonvolatile storage for 16 K bytes with a data access time within 325 ns. The read and write cycle times are 780 and 1240 ns, respectively.

Each memory board includes electronics to detect input DC power conditions and inhibit operation when out of tolerance. The microcomputer is a pin compatible alternative to the SBC 016, SBC 046, SBC 416 and MDS 016 memory boards used with Intel SBC 80/05, 80/10 and 80/20 or equivalent computers. It can be used to provide up to 64 K bytes of addressable locations for either 8 bit or 16 bit applications.

The board measures 12 by 6.75 by 0.50 inches (30.48 by 17.14 by 1.27 cm) and utilizes the +5 V and +12 V power available. Single unit price is $885.■

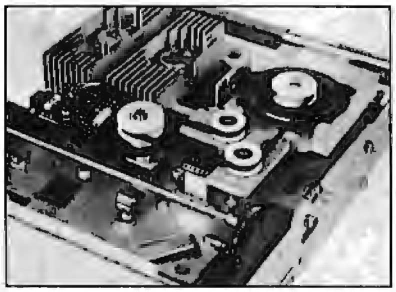
Circle 592 on inquiry card.

C1-6800 Microprocessor Memory

The microprocessor memory C1-6800 is a 16,384 word, 8 bit dynamic random access memory. The memory module plugs directly into the EXORciser and is plug compatible with the Mex-6812, 6815, 6816-1. Through the use of the 16,384 by 1 bit NMOS dynamic memory parts the memory module capacity can be increased up to 64 K bytes on a single board. An access time of 300 ns accompanied with on board hidden refresh permits maximum utilization of processor speed. The memory is addressable as a contiguous block in 4 K word increments thru 64 K. The on board dual in line package switch assigns the addresses for customer configuration. Prices are $390 for 16 K by 8 and $1230 for 64 K by 8. Contact Chrislin Industries Inc, 31312 Via Colinas #102, Westlake Village CA 91361.■

Circle 593 on inquiry card.

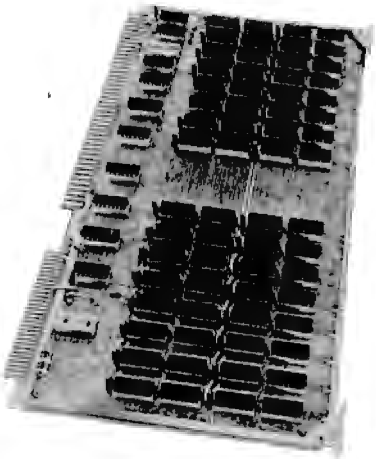
Building Block for Cartridge Memories



The Model 650 cartridge transport from North Atlantic's Qantex Division, 200 Terminal Dr, Plainview NY 11803, is designed as an original equipment manufacturer (OEM) memory building block for instruments, word processors, data processing systems for small businesses and other computer based equipment. The unit lists singly for $475, complete with "intimate electronics," stores up to 23 million bits of unformatted digital data on the four tracks of a DC300A tape cartridge. Optical tachometer holds tape speed at 30 inches per second for read and write operations, giving 48 K bps data transfer rate at 1600 bpi recording density. Tape is accelerated to 90 inches per second for rewind and fast search, permitting any stored data to be accessed in about 20 seconds. The transport can also be supplied with read after write heads for data validation during the actual recording process.■

Circle 594 on inquiry card.

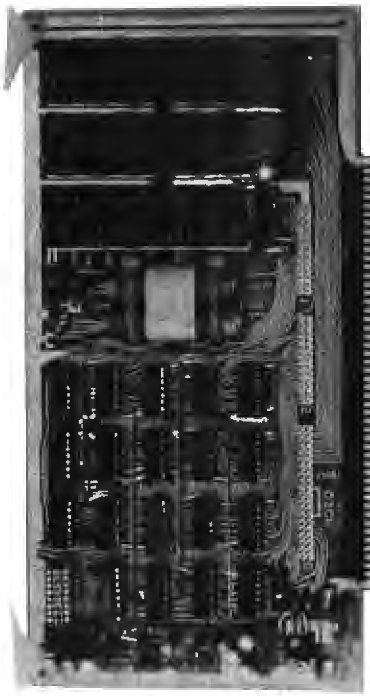
Battery Backup for Memory Board



Two static programmable memory boards capable of battery backup and compatible with Intel's SBC 80/05, SBC 80/10 and SBC 80/20 have been announced by Electronic Solutions Inc, 7969 Engineer Rd, San Diego CA 92111. The two versions are the RAM-4L containing 4 K bytes of memory and the RAM-8L containing 8 K bytes of memory. The RAM-8L uses a single 5 V power supply and draws 1.2 A typical, 1.7 A maximum under operation. During battery backup at 1.7 V, the battery current is 0.5 A typical, 0.8 A maximum. Three alkaline D cell batteries can back up 8 K bytes of memory for 11 hours, according to the company. The RAM-4L is priced at $312 and the RAM-8L is $428.■

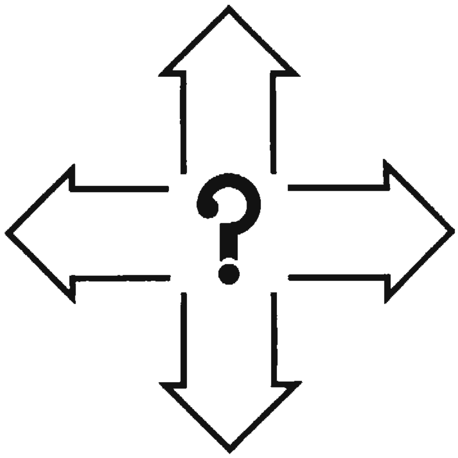
Circle 595 on inquiry card.

Non-Volatile High Speed Semiconductor Programmable Memory



The ElectriCom 4020 is a single card memory designed to meet the requirements for short and long term nonvolatile high speed programmable memory systems. Memory data is maintained for a minimum of 3 months (6 months typical) after the primary board power is removed. The long data retention time allows the 4020 to be used for high speed program and data files that may be removed and stored away from the host processor. On-board nickel-cadmium batteries, battery charger and power state monitors eliminate the need for external support circuitry. The primary input power disturbance level at which the 4020 will no longer respond to read or write commands is user set with an onboard potentiometer and LED indicator. Connection to the card edge connector from the IO headers is made with wire wrap allowing the 4020 to be used with all bus structures including the Altair (S-100). The 4020 is priced at $287 and may be purchased from ElectriCom, 12567 Crenshaw Blvd, Hawthorne CA 90250.■

Circle 596 on inquiry card.



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CPU-1™ 8080A CPU BOARD WITH
8 LEVEL VECTOR INTERRUPT.

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$220. ASSEMBLED AND TESTED

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wmc inc.™ WAMECO INC.
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2708/2716 EPROM MEMORY BOARD

* S-100 BUS
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* MEMORY BANK SELECT OPTION
* SOL™ COMPATIBLE MEMORY DISABLE
* SELECTABLE WAIT STATES
* FULLY BUFFERED INPUTS AND OUTPUTS
* DOUBLE SOLDER MASK
* SILK SCREENED PARTS LAYOUT
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$30. BARE

$100. KIT (LESS EPROMS)

TESTED AND ASSEMBLED $130. (LESS EPROMS)

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wmc inc.™ WAMECO INC. 3107 LANEVIEW DRIVE SAN JOSE CA 95132

ITHACA AUDIO

THE OEM MARKETPLACE

Ithaca Audio Boards

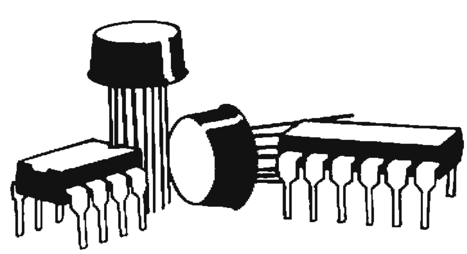
Are fully S-100 compatable, featuring gold edge connectors and plated-through holes. All boards (except the Protoboard) have fully buffered data and address lines, DIP switch addressing, solder mask and parts legend.

Z-80 CPU Board Most powerful 8 bit central processor available. Featuring power-on-jump, provision for on-board 2708. Accepts most 8080 software. **$35.00**

8K Static RAM Board High speed static memory at the lowest cost per bit. Includes memory protect/unprotect and selectable wait states. **$25.00**

2708/2716 EPROM Board Indispensable for storing dedicated programs and often used software. Accepts up to 16K of 2708's or 32K of 2716's. **$25.00**

Protoboard Universal wire-wrap board for developing custom circuitry. Accepts any size DIP socket. **$25.00**



RAM!

32K for $319.00

Ithaca Audio is now stocking the Mostek 4115 for S.D.'s Expandoram. Buy their basic kit, 24K of add-on RAM from us and SAVE.

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Ithaca Audio 24 4115's @ $7.00 ea.	168.00
TOTAL	$319.00
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YOU SAVE	**$156.00**

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FAIRCHILD 2102 LHPC	1.60
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IMSAI 8080 Kit with 22 Slot M.B.
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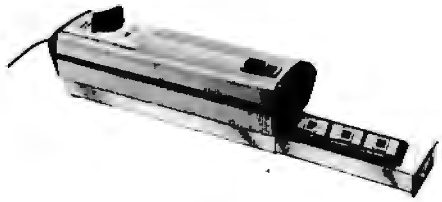
ITHACA AUDIO
P.O. Box 91
Ithaca, New York 14850
Phone: 607/273-3271

What's New?

New EROM Erasing Lamps



Two new EROM erasing ultraviolet lamps have been introduced by Spectronics Corp, 956 Brush Hollow Rd, Westbury NY 11590. The Spectroline PE-14 is a small ultraviolet lamp designed especially for the small systems users and personal computer enthusiasts. The PE-14T is the same as the PE-14, but has a 60 minute timer for automatic shut off. Both lamps will erase up to six programmable read only memory chips at one time in 14 minutes. Both UV erasing lamps feature a high intensity, shortwave UV tube, a specular reflector, and a V shaped holding tray that maintains up to six chips at a constant exposure distance. The high intensity tube is fully protected within the anodized aluminum housing, and a safety interlock prevents the unit from operating when the tray is not fully inserted. The conductive foam pad holds the chip in place during exposure and prevents electrostatic build up, while protecting the chip from possible static charge.■

Circle 650 on inquiry card.

CSC Proto-Clip Integrated Circuit Test Clips Used to Protect MOS Devices from Static

The CSC Proto-Clip integrated circuit test clips clip gently onto DIP integrated circuit packages and bring their pin connections to the top end of the clip. Cabled versions of this tool include a connecting cable preattached to the top or business end of the integrated circuit test clip. By attaching all leads at the far end of the cable to a good working ground, each integrated circuit pin is effectively shorted to ground and the problem of static discharge during handling is eliminated. The clips are available in 14 pin, 16 pin, 24 pin and 40 pin configurations; 18, 24 and 36 inch cables are available in each clip size. Prices for each clip and cable assembly range from $7.75 to $21.75 (unit quantities). For further information contact Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509.■

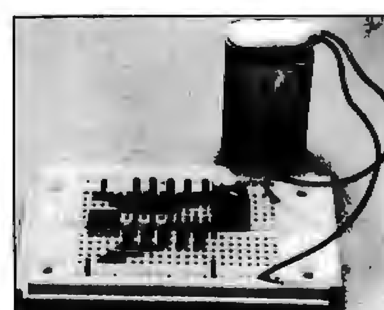
Circle 651 on inquiry card.

Attention Paper Tape Tearers

This advanced splicer punch gauge for all 8, 7-6, and 5 channel perforated tapes is being marketed by Telex Marketing Company, 6464 Sunset Blvd, Los Angeles CA 90028. The Telex Splicer/Puncher is said to make perfect splices and to repair tears up to 8 inches long. Utilizing a precision scissors type cutting shear, it works with all paper and Mylar tapes. Also featured are a data patch storage compartment, precision code hole punch, precision tape gauge, hold down arms, precision registration pins, and a punch position guide. For $169.50 Telex is offering a starter kit which includes the Splicer/Puncher and 300 data patches.■

Circle 652 on inquiry card

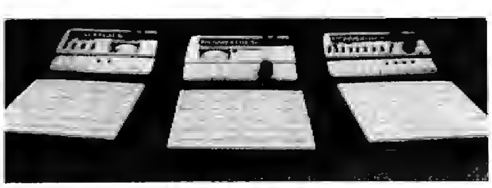
Pocket-Size Solderless Breadboards



The Continental Specialties Corp carries a line of Experimenter socket solderless breadboards. The smallest of these is 3.6 inches by 2.1 inches by .3 inches, about the size of an audio cassette. No soldering, drilling or tooling is required. Parts simply plug right into the breadboard and interconnections are accomplished by pushing short lengths of hookup wire into adjacent holes. Prices range from $4 to $10.95. Contact Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509.■

Circle 655 on inquiry card.

All Circuit Evaluators



These new Powerace all circuit evaluators have been introduced by A P Products Inc, POB 110, 72 Corwin Dr, Painesville OH 44077. The Powerace line includes three power breadboards, Models 101, 102 and 103. All three models offer 256-5 tie point terminals and 16-25 tie point buses, fused power supply and ground plane. All models feature Super-Strip SS-2s and will accept all DIP sizes plus TO-5s and discretes with leads to .032 inch diameter. Prices are $84.95 for the 101, $114.95 for the 102, and $124.95 for the 103. For further information about the different models, contact the company.■

Circle 653 on inquiry card.

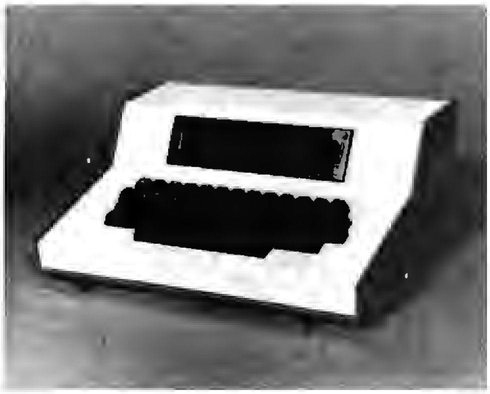
TR 1983 Bus Oriented UART Replacement for 8251 UART

The TR 1983 bus oriented universal asynchronous receiver transmitter (or UART) that is fully compatible with the asynchronous capabilities of the 8251 UART is now available from Western Digital Corp, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663. It has a 28 pin package pinout that allows direct replacement of the 8251. The TR 1983 features full or half duplex operation, and is powered by a single +5 V supply. For further information, write to the company.■

Circle 654 on inquiry card.

Circle 39 on inquiry card.

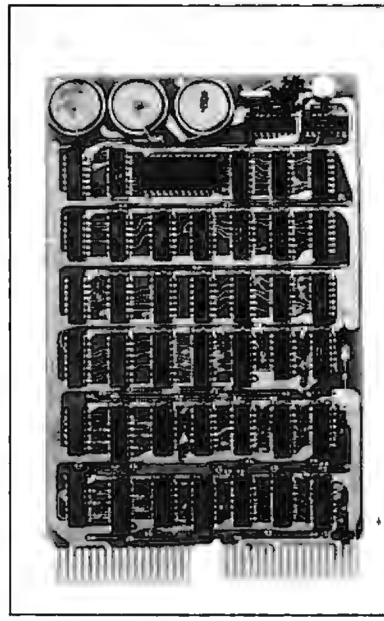
Use This for a Compact Extension Terminal



The Transactor III data terminal utilizes a microprocessor in its design. Features available include synchronous or asynchronous communications line support for both dedicated or polled multidrop environments. The terminal includes a single line 32 character gas discharge display and a 53 key Teletype style keyboard. It can be directly attached to any computer with an RS-232 or 20 mA current loop interface or can be attached to a communications line through a modem. Switches allow the user to select the operating mode including: 110 to 9600 bps transmission speeds, full or half duplex, even, odd or no parity, and the station address. The unit supports ASCII coded data with EBCDIC coded data available as an option. Other options include an expanded 256 byte data buffer and an addressable RS-232 port. The terminal can be provided with any line protocol for direct replacement of IBM 2260, 3275 or other types of terminals. Price is $995 from Computerwise Inc, 4006 E 137th Ter, Grandview MO 64030.■

Circle 571 on inquiry card.

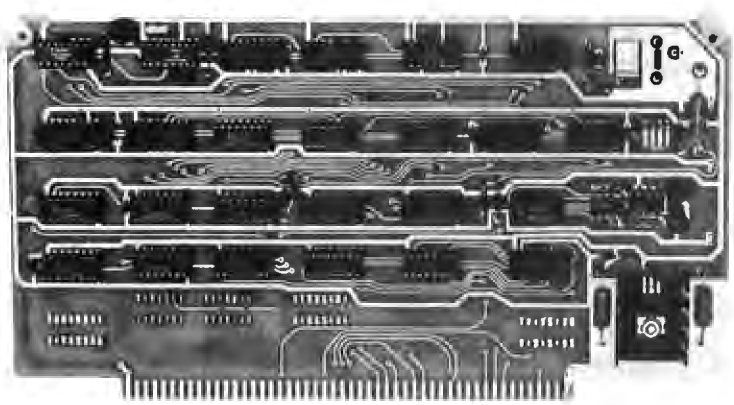
Timing Control Unit Available for LSI-11/2



This dual size peripheral board, designated TCU-50D, provides calendar and real time functions for DEC's LSI-11 and LSI-11/2. The unit, equipped with rechargeable battery back up capability, will keep track of the correct date and time for up to three months after the computer's power is turned off. This feature also enables the user to keep track of system down time during power failures. The board will present the date (month and day) and the time (hours, minutes and seconds) when a read instruction is given by the user. The units are shipped working and preset to the correct date and local time at the customer's location. A simple routine can reset the date and time. The TCU-50D costs $295 and is available from Digital Pathways Inc, 4151 Middlefield Rd, Palo Alto CA 94306.■

Circle 572 on inquiry card.

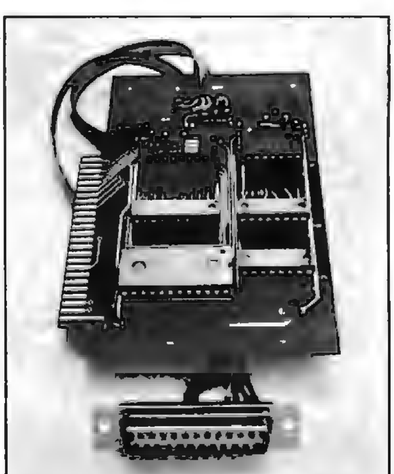
High Resolution Graphics



Although this Vector high resolution graphics board has been designed to operate with all Vector Graphic computers with 8 K bytes of static programmable memory, the manufacturer says it is fully compatible with any S-100 bus computer. The board is designed to operate in one of two modes: digital output or 16 level gray scale. It requires +8 VDC and a minimum of 8 K programmable memory and will produce digital graphic displays of 256 pixels horizontal by 240 pixels vertical in the digital mode or gray scale pictures 128 pixels horizontal by 120 pixels vertical. The video output conforms to RS-170 and will interface to standard raster scan monitors. The board is priced at $235 fully assembled and tested, $195 as a kit, and 8 K bytes of memory must be available in the user's system for a screen buffer. From Vector Graphic Inc, 790 Hampshire Rd, Westlake Village, CA 91361.■

Circle 573 on inquiry card.

Intelligent Communication Interface from Apple



Low cost telephone communication for the deaf; inexpensive high speed message transfer; computers challenging each other at chess; remote system failure diagnosis; access to data banks and program libraries by phone. . .are only a few of the applications made possible by the newly announced intelligent communications interface from Apple Computer Inc, 10260 Bandley Dr, Cupertino CA 95014.

The new card, Model A2B0003X, can be connected to any device which will accept the industry standard RS-232C serial interface, including the 103 A type modems manufactured by various companies. It operates at 110 or 330 bits per second. The price of the card is $180. It is supplied complete, with operating system built in, with cable and operation manual.■

Circle 574 on inquiry card.

16K E-PROM CARD

New!

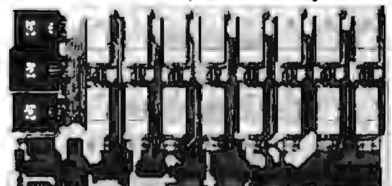
IMAGINE HAVING 16K OF SOFTWARE ON LINE AT ALL TIME!

S-100 (Imsai/Altair) Buss Compatible!

KIT FEATURES:

1. Double sided PC board with solder mask and silk screen and gold plated contact fingers.
2. Selectable wait states.
3. All address lines & data lines buffered!
4. All sockets included.
5. On card regulators.

KIT INCLUDES ALL PARTS AND SOCKETS (except 2708's). Add $25. for assembled and tested.



PRICE CUT!

$57.50 kit

WAS $69.95

SPECIAL OFFER:

Our 2708's (450NS) are $12.95 when purchased with above kit.

8K LOW POWER RAM KIT-$149.00

Fully Static!

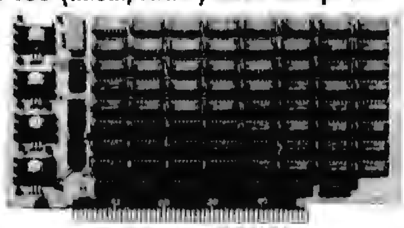
ADD $20 FOR 250NS

S-100 (Imsai/Altair) Buss Compatible!

KIT FEATURES:

1. Doubled sided PC Board with solder mask and silk screen layout. Gold plated contact fingers.
2. All sockets included.
3. Fully buffered on all address and data lines.
4. Phantom is jumper selectable to pin 67.
5. FOUR 7805 regulators are provided on card.

(450NS)



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Same as standard 7805 except 750 MA output. TO—220. 5VDC output.
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Now full speed! Prime new units from a major U.S. Mfg. 450 N.S. Access time. 1K x 8. Equiv. to 4-1702 A's in one package.
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BRAND NEW 2102A-4. FACTORY PRIME!

WE MADE ANOTHER SUPER SURPLUS BUY!

PERFECT FOR USE WITH OUR BLANK 8K PC BOARD SHOWN ABOVE.

THESE PARTS HAVE BEEN SCREENED TO MEET THE LOW POWER SPEC. AND ARE GUARANTEED BY US TO BE 40 MA. MAXIMUM ICC. (28 MA. TYPICAL)

LOW POWER

450 N.S.

"A" VERSION FOR BATTERY BACKUP!

8 FOR $7.95

32 FOR $28

4K STATIC RAM'S
2114. The new industry standard. Arranged as 1K x4. Equivalent to 4-21 L02's in 1 package! 18 pin DIP. 2 chips give 1Kx8.
2/$24. 8/$85.

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SLA-1. Common Anode. .33 inch character size. The original high efficiency LED display. 75c ea.
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(AC XFMR $1.95)

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- FOUR JUMBO ½ INCH LED DISPLAYS
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- 24 HR ALARM SIGNAL OUTPUT
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- POWER FAILURE INDICATOR
- SLEEP & SNOOZE TIMERS
- DIRECT LED DRIVE (LOW RFI)
- COMES WITH FULL DATA

ASSEMBLED! NOT A KIT!

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PERFECT FOR USE WITH A TIMEBASE.

COMPARE AT UP TO TWICE OUR PRICE!

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SALE!
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1000 FOR $17.50

New! REAL TIME Computer Clock Chip
N.S. MM5313. Features BOTH 7 segment and BCD outputs. 28 Pin DIP. $4.95 with Data

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Circle 297 on inquiry card.

★ YOUR BEST BUY IN WIRE WRAP SUPPLIES ★

PRECUT WIRE

WHY BUY WIRE ON ROLLS?

PRECUT & STRIPPED WIRE IS:

- **Fast** - No more cutting & stripping by hand
- **Reliable** - Good, clean, uniform strip
- **Economical** - Cheaper than using bulk wire

Precut Wire		Bulk Wire	
100 pcs of 3" at $.82	3¼¢/ft.	50 ft roll at $1.99	4¢/ft.
100 pcs of 6" at 1.06	2¢/ft.	100 ft roll at 2.95	3¢/ft.
Wire Kit 1 at $6.95	2 1/3¢/ft.		

30 Kynar stripped 1" on each end. Lengths are overall. Colors: Red,Blue,Green,Yellow,Black,Orange,White. Wire packaged in plastic bags. Add 25¢/length for tubes

	100	500	1000	5000
2½ in	.78	2.40	4.30/K	3.89/K
3 in	.82	2.60	4.71/K	4.22/K
3½ in	.86	2.80	5.12/K	4.55/K
4 in	.90	3.00	5.52/K	4.88/K
4½ in	.94	3.21	5.93/K	5.21/K
5 in	.98	3.42	6.34/K	5.52/K
5½ in	1.02	3.65	6.75/K	5.86/K
6 in	1.06	3.85	7.16/K	6.19/K
6½ in	1.15	4.05	7.57/K	6.52/K
7 in	1.20	4.25	7.98/K	6.85/K
7½ in	1.25	4.45	8.39/K	7.18/K
8 in	1.29	4.65	8.80/K	7.53/K
8½ in	1.32	4.85	9.21/K	7.84/K
9 in	1.36	5.05	9.62/K	8.17/K
9½ in	1.40	5.25	10.03/K	8.50/K
10 in	1.45	5.51	10.44/K	8.83/K
Addl. Inches	.10	.41	.82/K	.66/K

WIRE KITS

#1 $6.95

250	3"	100	4½"
250	3¼"	100	5"
100	4"	100	6"

#2 $19.95

250	2½"	250	4"	250	6"
500	3"	250	5"	100	6½"
500	3½"	100	5½"	100	7"
500	4"	1 250 ft Roll Bulk			

Choose One Color or Assortment

SOLDERLESS BREADBOARDS

2.2" x 6.5"

SK 10 $16.50

INCLUDING:
Over 100 pieces of precut wire in assorted lengths — free!
Choose 1 color: Red, Black, Blue, Yellow, Green, White, Orange Or Assortment

INTERCONNECT CABLES

Ribbon cable connectors for connecting boards to front panels or board to board

	SINGLE ENDED			DOUBLE ENDED		
	14 pin	16 pin	24 pin	14 pin	16 pin	24 pin
6"	1.24	1.34	2.05	2.24	2.45	3.37
12"	1.33	1.44	2.24	2.33	2.55	3.92
24"	1.52	1.65	2.63	2.52	2.76	4.31
48"	1.91	2.06	3.40	2.91	3.17	5.08

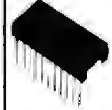
WIRE WRAP TOOLS

$34.95
With Free Wire Kit 1 ($6.95 Value)

HOBBY WRAP
Model BW 630

Batteries & Charger	$11.00
WSU 30 Hand Wrap-Unwrap Strip Tool	6.25
WSU 30M, for Modified Wrap	7.25
BT 30 Extra Bit	2.95

WIRE WRAP SOCKETS



	1-9	10-24	25-99	100-249	250-999	1K-5K
• 8 pin	.35	.33	.31	.29	.25	.23
• 14 pin	.35	.33	.31	.29	.28	.27
• 16 pin	.37	.35	.33	.31	.30	.29
• 18 pin	.60	.55	.45	.43	.40	.37
20 pin	.84	.78	.71	.63	.59	.54
• 22 pin	.90	.85	.82	.78	.70	.60
24 pin	.91	.84	.78	.68	.64	.59
25 pin strip	1.25	1.05	.95	.80	.70	.65
28 pin	.95	.89	.84	.80	.76	.74
40 pin	1.50	1.40	1.30	1.20	1.05	.90

Gold 3-Level Closed Entry Design.
*End & Side Stackable. All prices include Gold
2 Level Sockets Also Available

EDGE CARD CONNECTOR SALE!

44 Pin	Solder Tail	$1.75	$15/10
100 Pin	Solder Tail	3.50	$30/10
100 Pin	Wire Wrap	3.50	$30/10

All connectors include Gold

PAGE DIGITAL ELECTRONICS

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- All others, shipped Ppd in U.S. via UPS
- For Blue Label (Air) or 1st Class, add $1
- We accept Visa & Mastercharge
- Most orders shipped same day

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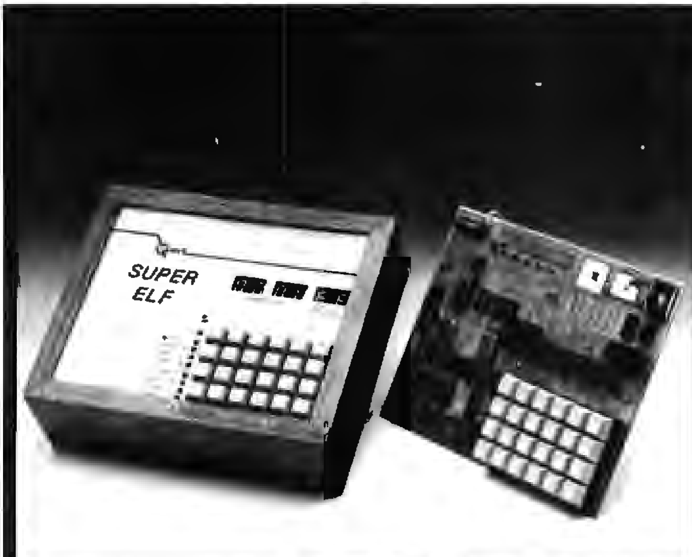
Phone (213) 357-5005

Dealer Inquiries Invited



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For will call only: (408) 988-1640
2322 Walsh Ave.

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Same day shipment. First line parts only. Factory tested. Guaranteed money back. Quality IC's and other components at factory prices.

INTEGRATED CIRCUITS

MICROPROCESSOR

6800	19.50
8080A with data	8.95
Z80	18.95
8212	2.90
8214	8.00
8216	2.90
8224	2.90
8228	5.35
8251	9.25
8253	10.00
8255	9.25
CDP1802CD	19.95
CDP1802D	25.00
CDP1861	12.95
6820	9.95
6850	12.95
6502	18.50

PROM

1702A	[illegible]
N82S23	[illegible]
N82S123	[illegible]
N82S126	[illegible]
N82S129	[illegible]
N82S131	[illegible]
N82S136	[illegible]
N82S137	[illegible]
2708	[illegible]
DM8577	[illegible]
8223	[illegible]
2716TI	[illegible]

IC SOCKETS
Solder Tin Low Profile

PIN	1 UP	PIN	1 UP
8	.15	24	.35
14	.18	28	.42
16	.20	36	.58
18	.27	40	.61
22	.30		

3 level wire wrap gold
14 pin .25 16 pin .27
2 level 14 pin ww .20

CONNECTORS

44 pin edge	2.00
100 pin edge	4.50
100 pin edge WW	5.25

MOS/MEMORY RAM

2101-1	3.95
2102-1	1.28
2102AL-4	1.60
21F02	1.85
2104A-4	4.95
2107B	4.95
2111-1	4.95
2112-2	3.95
2114	8.50
4116	24.95
2513B	6.30
21L02-1	1.49
MM5262	.40
MM5280	3.00

MM5320	9.95
MM5330	5.94
PD411D-3	4.00
PD411D-4	5.00
P5101	13.95
4200A	12.95
82S25	2.90
91L02A	1.75
HD0165-5	6.95
MM57100	4.50
GIAY38500-1	9.95
MCM6571A	9.95
9368	3.50

INTERFACE

8T25	3.20
8T26	1.69
8T28	2.75
8T97	1.69
8T98	1.69
8095	.65
8096	.65
8097	.65
8098	.65

ASCII KEYBOARDS

[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	$14.95

CRYSTALS

1 MHz	4.50	2.0100 MHz	1.95
2 MHz	4.50	2.097152 MHz	4.50
4 MHz	4.25	2.4576 MHz	4.50
5 MHz	4.25	3.2768 MHz	4.50
10 MHz	4.25	5.0688 MHz	4.50
18 MHz	3.90	5.185 MHz	4.50
20 MHz	3.90	5.7143 MHz	4.50
32 MHz	3.90	6.5536 MHz	4.50
32768 Hz	4.00	14.31818 MHz	4.25
1.8432 MHz	4.50	18.432 MHz	4.50
3.5795 MHz	1.20	22.1184 MHz	4.50

30 MHz Frequency Counter Kit	$47.75
Prescaler Kit to 350 MHz	$19.95

COMPUTER BOARD KITS

8K RAM Board Kit	$134.95
4K EPROM Kit	114.95
I/O Board Kit	44.50
Extender Board w/connector	12.50
Video Interface board kit	125.00
16K EPROM board kit w/o PROMS	74.50
16K Static RAM board kit	395.00
North Star Floppy Disk Kit	$665.00
Additional Drive Kit	415.00
Paratronics 100A Logic Analyzer Kit	$199.00
Model 10 Trigger Expander Kit	$229.00
Model 150 Bus Grabber Kit	$369.00

New Cosmac Super "ELF"

RCA CMOS expandable to 64K microcomputer w/HEX keypad input and video output for graphics. Just turn on and start loading your program using the resident monitor on ROM. Pushbutton selection of all four CPU modes. LED indicators of current CPU mode and four CPU states. Single step op. for program debug. Built in pwr. supply, 256 Bytes of RAM, audio amp & spkr. Detailed assy man. w/PC board & all parts fully socketed. Comp. Kit $106.95. High address display option 8.95, Low address display option 9.95. Custom hardwood cab., drilled front panel 19.75. Nicad Battery Backup Kit w/all parts 4.95. Fully wired & tested in cabinet without options 151.70. 1802 software club. 10–12 pg. monthly publication 12.00 per yr.

4K Elf Expansion Board Kit with Cassette I/F $79.95

Available on board options: 1K super ROM monitor $19.95. Parallel I/O port $7.95. RS232 I/F $3.50. TTY 20 ma I/F $1.95. S-100 Memory I/F $4.50. Need 4K Expansion Board Kit for all above options. Power Supply Kit ±5 +12V 5 amp $24.95.

Tiny Basic for ANY 1802 System

Cassette $10.00
on ROM Monitor $38.00
Super Elf owners take 30% off.
Object code listing or paper tape with manual $5.50

Auto Clock Kit $15.95

DC clock with 4-.50" displays. Uses National MA-1012 module with alarm option. Includes light dimmer, crystal timebase PC boards. Fully regulated, comp. instructs. Add $3.95 for beautiful dark gray case. Best value

60 Hz Crystal Time Base Kit

All parts and instructions $4.40.

'78 IC Update Master Manual

1978 IC Update Master Manual $30.00
Complete IC data selector 2175 pg. Master reference guide. Over 42,000 cross references. Free update service through 1978. Domestic postage $3.50. Foreign $6.00.

Video Modulator Kit $8.95

Convert your TV set into a high quality monitor without affecting normal usage. Complete kit with full instructions.

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Video computer with games and graphics.

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Batt. oper. 1mV and .1NA resolution. Resistance to 20 meg. 1% accuracy. Small, portable, completely assem. in case. 1 yr. guarantee.

PROM Eraser

Ultraviolet, assembled $49.95

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FREE: Send for your copy of our NEW 1978 QUEST CATALOG. Include 28¢ stamp.

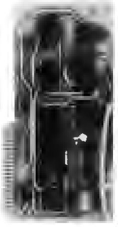
Circle 307 on inquiry card.

COMPUTER INTERFACES & PERIPHERALS

SAVE SAVE

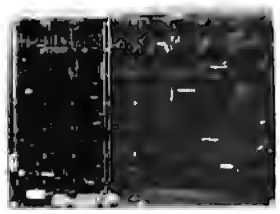
For free catalog including parts lists and schematics, send a self-addressed stamped envelope.

APPLE II SERIAL I/O INTERFACE *



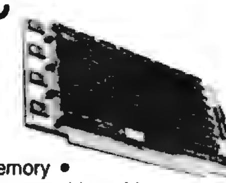
Part no. 2
Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer. • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. Board only — $15.00; with parts — $42.00; assembled and tested — $62.00

T.V. TYPEWRITER



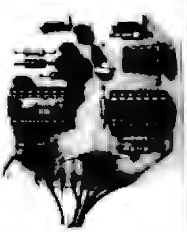
Part no 106
• Stand alone TVT • 32 char/line, 16 lines, modifications for 64 char/line included • Parallel ASCII (TTL) input • Video output • 1K on board memory • Output for computer controlled curser • Auto scroll • Non-destructive curser • Curser inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, and -12 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper case only • Board only $39.00, with parts $145.00

8K STATIC RAM



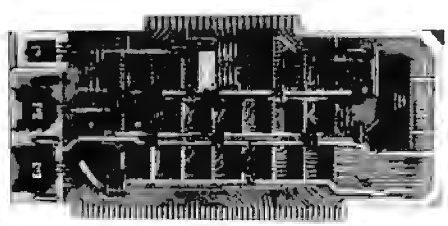
Part no. 300
• 8K Altair bus memory • Uses 2102 Static memory chips • Memory protect • Gold contacts • Wait states • On board regulator • S-100 bus compatible • Vector input option • TRI state buffered • Board only $22.50; with parts $160.00

MODEM *



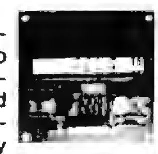
Part no. 109
• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output-serial • Connect 8 ohm speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board $7.60; with parts $27.50

TIDMA *



Part no. 112
• Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate. • S-100 bus compatible • Board only $35.00; with parts $110.00

RF MODULATOR *

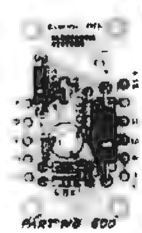


Part no. 107
• Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple. • Power required is 12 volts AC C.T., or +5 volts DC • Board $7.60; with parts $13.50

DC POWER SUPPLY *

Part no. 6085
• Board supplies a regulated +5 volts at 3 amps., +12, -12, and -5 volts at 1 amp. • Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps. • Board only $12.50; with parts excluding transformers $42.50

RS 232/TTY * INTERFACE

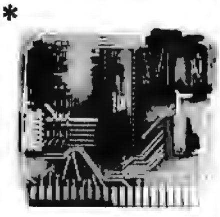


Part no. 600
• Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232 • Two separate circuits • Requires +12 and -12 volts • Board only $4.50, with parts $7.00

TAPE INTERFACE *

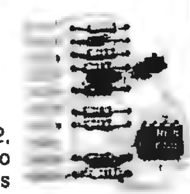
Part no. 111
• Play and record Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board $7.60; with parts $27.50

UART & BAUD RATE GENERATOR *



Part no. 101
• Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. • All connections go to a 44 pin gold plated edge connector • Board only $12.00; with parts $35.00 with connector add $3.00

RS 232/TTL * INTERFACE



Part no. 232
• Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires -12 and +12 volts • All connections go to a 10 pin gold plated edge connector • Board only $4.50; with parts $7.00 with connector add $2.00

ELECTRONIC SYSTEMS

Dept. B, P.O. Box 21638, San Jose, CA. USA 95151

To Order: Mention part number and description. For parts kits add "A" to part number. In USA, shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D orders. California residents add 6.5% for tax. Outside USA add 10% for air mail postage, no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. All items are in stock, and will be shipped the day order is received via first class mail. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts." Dealer inquiries invited.
24 Hour Order Line: (408) 226-4064

✱ Circuits designed by John Bell

Circle 125 on inquiry card.

What's New?

PERIPHERALS

Pocket-Sized Terminal

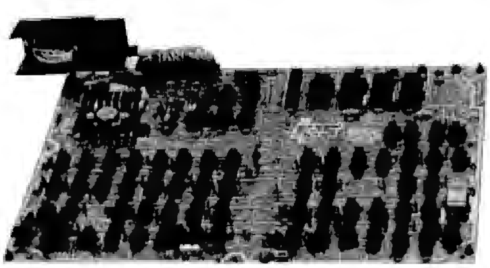
An alternative to the Teletype has been developed by Gleichmann & Co, Wormser Str 9, D 6710 Frankenthal WEST GERMANY. The pocket-sized terminal has the same electrical interface but according to the company costs about one tenth as much as the conventional solution.

The size of a pocket calculator, the device has a built-in microprocessor, works fully electronically, and is noiseless. It has a keyboard for 64 alphanumeric characters, produces serial ASCII code and is compatible with any equipment that operates on a 20 mA current loop. It has a 9 digit display. The IO lines are galvanically separated by optoelectronic couplers. Transmission speed is 110 bps or, optionally, 300 bps. The device measures 3 by 6 by 1 inches (7.5 by 15.5 by 2.5 cm) and has a power consumption of 400 mA from the 5 V supply and 140 mA from the 12 V supply.

The US distributor is Sedillo Company Inc, 225 E Sunnyoaks Av, Campbell CA 95008.■

Circle 633 on inquiry card.

Interface for Teletype Model 40 Printer



The C/D-40 interface board allows the 300 line per minute Teletype Model 40 printer to connect to a host computer or terminal that offers a Centronics or Dataproducts interface. Complete hardware and software transparency is provided so that plug to plug compatibility exists without making system modifications. The C-40 allows for the replacement of any Centronics printer and the D-40 provides for Dataproducts replacement.

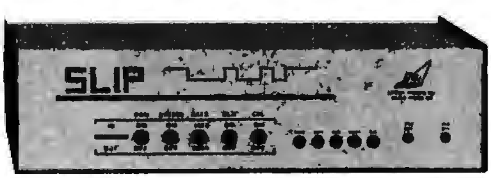
The board is self-contained and does not require external power when mounted within the printer cabinet, since power is derived from the printer. The board may also be mounted inside the host system. This allows for computer and printer separation, via two wire pairs, of up to 2000 feet.

Standard features include field selectable control character code conversion, parity selection, extended ASCII, and variable motor time out after last character received.

The C-40 is priced at $795 and can be obtained from Innovative Electronic Systems Inc, 15200 NW 60 Av, Miami Lakes FL 33014.■

Circle 635 on inquiry card.

Plotter Controller



The Serial Language Independent Plotter Controller (SLIP) is installed between your terminal and a modem on a time shared network or between your terminal and a local computer. With the connection of an XY recorder to SLIP, you have plotting and graphics capability. Any teleprocessing site utilizing standard RS-232 serial communications can become a remote graphics facility.

SLIP contains a microprocessor to provide internal vector and character generation features, allowing a maximum of plotting with a minimum of data exchange. SLIPS capabilities include the support of two way user and computer communications during a plot, and an off line mode which assists in plot layout and design. It also detects and indicates character format errors.

During plot generation SLIP intercepts the plot data from the computer and generates XY signals to the plotter. The X and Y outputs from SLIP are selectable over a wide range of voltages to accommodate input requirements of most XY recorders.

The price is $1465 from Special Systems Inc, 8045 Newell St, Silver Spring MD 20910.■

Circle 636 on inquiry card.

Micrographics Printer Combines Graphics and Alphanumerics

A MicroGraphics printer, the EX-820, which can mix high resolution graphics and full ASCII alphanumerics, is now available from Axiom, 5932 San Fernando Rd, Glendale CA 91202, at the single quantity price of $795.

Under software control, users have flexibility in mixing alphanumeric ASCII fields and graphic fields on any line. The user can define the size of each graphic field and can choose from four preprogrammed horizontal dot resolutions up to 128 dots per inch. Once the fields have been defined, the EX-820 automatically formats graphic and alphanumeric printouts to user specifications. Vertical dot resolution is fixed at 65 dots per inch. There is also provision for automatic histogram generation.

Standard features include: RS-232C serial input as well as parallel ASCII; driven by an Intel 8048; 512 character multiline asynchronous input buffer, optionally expandable to 2 K byte characters; 96 character ASCII standard, optionally expandable to 256 characters with user programmable fonts; software selection of three character sizes to give 80, 40 or 20 column printing; software selection of reverse printing, where light characters are formed on a dark background; 2 K bytes of user programmable read only memory (low cost option) which converts the printer into an intelligent printer.

Dimensions are 11 by 4 1/4 by 12 inches (28 by 10.8 by 30.5 cm). It weighs 12 pounds (5.4 kg), including a 230 foot roll of paper.■

Circle 634 on inquiry card.

Where Do New Product Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the neat new whizbang gizmo or save the world software package is of interest to the personal computing experimenters and homebrewers who read BYTE, we print the information in some form. We openly solicit such information from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications.

NEW ANNOUNCING

The EW-2001 A "Smart" VIDEO BOARD KIT At A "Dumb" Price!

A VIDEO BOARD + A MEMORY BOARD + AN I/O BOARD – ALL IN ONE!

- STATE OF THE ART TECHNOLOGY USING DEDICATED MICROPROCESSOR I.C.
- NUMBER OF I.C.s REDUCED BY 50% FOR HIGHER RELIABILITY
- MASTER PIECE OF ENGINEERING
- FULLY SOFTWARE CONTROLLED

Priced at ONLY **$199.95** Basic Software Included

SPECIAL FEATURES:
- S-100 bus compatible
- Parallel keyboard port
- On board 4K screen memory (optional)* relocatable to main computer memory
- Text editing capabilities (software optional)
- Scrolling: up and down through video memory
- Blinking characters
- Reversed video
- Provision for on board ROM
- CRT and video controls fully programmable (European TV)
- Programmable no. of scan lines
- Underline blinking cursor
- Cursor controls: up, down, left, right, home, carriage return
- Composite video

*Min. 2K required for operation of this board.

DISPLAY FEATURES:
- 128 displayable ASCII characters (upper and lower case alphanumeric, controls)
- 64 or 32 characters per line (jumper selectable)
- 32 or 16 lines (jumper selectable)
- Screen capacity 2048 or 512
- Character generation: 7 x 11 dot matrix

OPTIONS:

Sockets	$10.00
2K Static Memory (with Sockets)	$45.00
4K Static Memory (with Sockets)	$90.00
Complete unit, assembled and tested with 4K Memory	$335.00
Basic software on ROM	$20.00
Text editor on ROM	$75.00

DEALER INQUIRIES WELCOMED

8080 SUPPORT

8212	$3.00
8214	7.95
8216	3.50
8228	5.95
8251	7.95
8555	8.50

8080A CPU $7.75

RAM - 2114 1Kx4 450ns $8.00

1/4W RESISTOR
10 Ohm – 1.5m
$1.75/100
of one value

RIBBON CABLE
32 Conductor
26 AWG – $.60/Foot

1 Pole 10 Pos. ROTARY SWITCH 3 for $1.00

MINIATURE Slide Switch DPDT $.15; 10/$1.00

1 Pole 8 Pos. TO5 Miniature Rotary Switch 3 for $1.00

Push Button Momentary Switch 3 for $1.00

HEXADECIMAL LABEL KEYBOARD
- Matrix coded output
- Interfaces with 74C922 for binary code
- Zero bounce
- Est. life: 100 million
- Remove back to stick on

SHIPPING: Keyboard and Video Board: $3.50; others: $1.25
California residents add 6% sales tax

ELECTRONICS WAREHOUSE Inc.
1603 AVIATION BLVD.
REDONDO BEACH, CA. 90278
TEL. (213) 376-8005
WRITE FOR FREE CATALOG
Minimum Order: $10

ASCII 3rd GENERATION KEYBOARD KIT *ONLY $68.00

- TTL Logic Circuits
- Power: +5V 275mA
- Upper and Lower Case
- Full ASCII Set (Alpha Numeric, Symbols, Control)
- 7 or 8 Bits Parallel Data
- Optional Serial Output
- Selectable Positive or Negative Strobe, and Strobe Pulse Width
- 'N' Key Roll-Over
- Fully Debounced
- Carriage Return Key
- Repeat Function Key
- Shift Lock, 2 Shift Keys
- 4 User Defineable Keys
- P.C. Board Size: 17-3/16" x 5"

OPTIONS:
- Metal Enclosure Painted IBM Blue and White) $25.00
- 18 Pin Edge Con. $2.00
- I.C. Sockets $4.00
- Serial Output (Shift Register) $2.00
- Upper Case Lock Switch for Capital Letters and Numbers $2.00

KIT INCLUDES: Keyboard, P.C. Board, all required components & assembly manual.

NOTE: If you have this 63 Key Teletype Keyboard you can buy the Kit without it for only $44.95.

Circle 130 on inquiry card.

Algorithmics PR-DW1 Precision Printer

The Algorithmics PR-DW1 Daisy Wheel Printer is a printer designed for use with microcomputer systems for high quality printing and plotting applications. This printer operates under control of an internal microprocessor and communicates with the host microprocessor over a high speed asynchronous parallel interface. It prints bidirectionally at rates of 45 characters per second. The carriage can be positioned left and right in increments as fine as 1/48 of an inch (0.53 mm). Hardware options include 55 characters per second version, metal print wheel, cam feed platen and forms tractor. The interface to the host computer consists of both hardware and software. The hardware component is a custom 50 conductor cable that terminates at the host machine in standard 25 pin connectors. The software consists of two applications packages. One package is for text printing and features bidirectional printing, automatic tabbing, and high speed travel over character spaces and blank lines. The second package is a graphics package that utilizes the 1/120 inch horizontal and 1/48 inch vertical precision print head positioning to achieve full graphics capabilities. Price is $2678 from Algorithmics Inc, POB 56, Newton Upper Falls MA 02164.■

Circle 656 on inquiry card.

Circle 30 on inquiry card.

DIODES/ZENERS

1N914	100v	10mA	.05
1N4005	600v	1A	.08
1N4007	1000v	1A	.15
1N4148	75v	10mA	.05
1N4733	5.1v	1 W Zener	.25
1N753A	6.2v	500 mW Zener	.25
1N758A	10v	"	.25
1N759A	12v	"	.25
1N5243	13v	"	.25
1N5244B	14v	"	.25
1N5245B	15v	"	.25

SOCKETS/BRIDGES

8-pin	pcb .20	ww	.35
14-pin	pcb .20	ww	.40
16-pin	pcb .20	ww	.40
18-pin	pcb .25	ww	.75
22-pin	pcb .35	ww	.95
24-pin	pcb .35	ww	.95
28-pin	pcb .45	ww	1.25
40-pin	pcb .50	ww	1.25

Molex pins .01 | To-3 Sockets .25
2 Amp Bridge 100-prv .95
25 Amp Bridge 200-prv 1.95

TRANSISTORS, LEDS, etc.

2N2222	NPN (2N2222 Plastic .10)	.15
2N2907	PNP	.15
2N3906	PNP (Plastic - Unmarked)	.10
2N3904	NPN (Plastic - Unmarked)	.10
2N3054	NPN	.35
2N3055	NPN 15A 60v	.50
T1P125	PNP Darlington	.35
LED Green, Red, Clear, Yellow		.15
D.L.747	7 seg 5/8" High com-anode	1.95
MAN72	7 seg com-anode (Red)	1.25
MAN3610	7 seg com-anode (Orange)	1.25
MAN82A	7 seg com-anode (Yellow)	1.25
MAN74A	7 seg com-cathode (Red)	1.50
FND359	7 seg com-cathode (Red)	1.25

C MOS

4000	.15
4001	.15
4002	.20
4004	3.95
4006	.95
4007	.20
4008	.75
4009	.35
4010	.35
4011	.20
4012	.20
4013	.40
4014	.75
4015	.75
4016	.35
4017	.75
4018	.75
4019	.35
4020	.85
4021	.75
4022	.75
4023	.20
4024	.75
4025	.20
4026	1.95
4027	.35
4028	.75
4030	.35
4033	1.50
4034	2.45
4035	.75
4040	.75
4041	.69
4042	.65
4043	.50
4044	.65
4046	1.25
4049	.45
4050	.45
4066	.55
4069/74C04	.25
4071	.25
4081	.30
4082	.30
MC 14409	14.50
MC 14419	4.85
4511	.95
74C151	1.90

– T T L –

7400	.10
7401	.15
7402	.15
7403	.15
7404	.10
7405	.25
7406	.25
7407	.55
7408	.15
7409	.15
7410	.15
7411	.25
7412	.25
7413	.25
7414	.75
7416	.25
7417	.40
7420	.15
7426	.25
7427	.25
7430	.15
7432	.20
7437	.20
7438	.20
7440	.20
7441	1.15
7442	.45
7443	.45
7444	.45
7445	.65
7446	.70
7447	.70
7448	.50
7450	.25
7451	.25
7453	.20
7454	.25
7460	.40
7470	.45
7472	.40

7473	.25
7474	.30
7475	.35
7476	.40
7480	.55
7481	.75
7483	.75
7485	.55
7486	.25
7489	1.05
7490	.45
7491	.70
7492	.45
7493	.35
7494	.75
7495	.60
7496	.80
74100	1.15
74107	.25
74121	.35
74122	.55
74123	.35
74125	.45
74126	.35
74132	.75
74141	.90
74150	.85
74151	.65
74153	.75
74154	.95
74156	.70
74157	.65
74161	.55
74163	.85
74164	.60
74165	1.10
74166	1.25
74175	.80

74176	.85
74180	.55
74181	2.25
74182	.75
74190	1.25
74191	.95
74192	.75
74193	.85
74194	.95
74195	.95
74196	.95
74197	.95
74198	1.45
74221	1.00
74367	.75
75108A	.35
75491	.50
75492	.50
74H00	.15
74H01	.20
74H04	.20
74H05	.20
74H08	.35
74H10	.35
74H11	.25
74H15	.45
74H20	.25
74H21	.25
74H22	.40
74H30	.20
74H40	.25
74H50	.25
74H51	.25
74H52	.15
74H53J	.25
74H55	.20

74H72	.35
74H101	.75
74H103	.55
74H106	.95
74L00	.25
74L02	.20
74L03	.25
74L04	.30
74L10	.20
74L20	.35
74L30	.45
74L47	1.95
74L51	.45
74L55	.65
74L72	.45
74L73	.40
74L74	.45
74L75	.55
74L93	.55
74L123	.85
74S00	.35
74S02	.35
74S03	.25
74S04	.25
74S05	.35
74S08	.35
74S10	.35
74S11	.35
74S20	.25
74S40	.20
74S50	.20
74S51	.25
74S64	.15
74S74	.35
74S112	.60
74S114	.65

74S133	.40
74S140	.55
74S151	.30
74S153	.35
74S157	.75
74S158	.30
74S194	1.05
74S257 (8123)	1.05
74LS00	.20
74LS01	.20
74LS02	.20
74LS04	.20
74LS05	.25
74LS08	.25
74LS09	.25
74LS10	.25
74LS11	.25
74LS20	.20
74LS21	.25
74LS22	.25
74LS32	.25
74LS37	.25
74LS38	.35
74LS40	.30
74LS42	.65
74LS51	.35
74LS74	.35
74LS86	.35
74LS90	.55
74LS93	.55
74LS107	.40
74LS123	1.00
74LS151	.75
74LS153	.75
74LS157	.75
74LS164	1.00
74LS193	.95
74LS367	.75
74LS368	.65

LINEARS, REGULATORS, etc.

MCT2	.95
8038	3.95
LM201	.75
LM301	.45
LM308 (Mini)	.95
LM309H	.65
LM309K (340K-5)	.85
LM310	.85
LM311D (Mini)	.75
LM318 (Mini)	1.75
LM320K5 (7905)	1.65
LM320K12	1.65

LM320T5	1.65
LM320T12	1.65
LM320T15	1.65
LM324N	1.25
LM339	.75
7805 (340T5)	.95
LM340T12	.95
LM340T15	.95
LM340T18	.95
LM340T24	.95
LM340K12	1.25

LM340K15	1.25
LM340K18	1.25
LM340K24	1.25
78L05	.75
78L12	.75
78L15	.75
78M05	.75
LM373	2.95
LM380 (8-14 PIN)	.95
LM709 (8,14 PIN)	.25
LM711	.45

LM723	.40
LM725N	2.50
LM739	1.50
LM741 (8-14)	.25
LM747	1.10
LM1307	1.25
LM1458	.65
LM3900	.50
LM75451	.65
NE555	.35
NE556	.85
NE565	.95
NE566	1.25
NE567	.95

9000 SERIES

9301	.85	95H03	1.10
9309	.35	9601	.20
9322	.65	9602	.45

MICRO'S, RAMS, CPU'S, E-PROMS

74S188	3.00	8214	8.95
1702A	4.50	8224	3.25
MM5314	3.00	8228	6.00
MM5316	3.50	8251	8.50
2102-1	1.45	8255	10.50
2102L-1	1.75	8T13	1.50
2114	9.50	8T23	1.50
TR1602B	3.95	8T24	2.00
TMS 4044-	9.95	8T97	1.00
		2107B-4	4.95
8080	8.95	2708	9.50
8212	2.95	Z80 PIO	8.50

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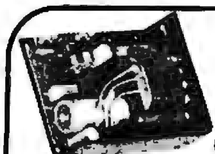
SPECIAL DISCOUNTS

Total Order	Deduct
$35 - $99	10%
$100 - $300	15%
$301 - $1000	20%

Circle 180 on inquiry card.

Circle 200 on inquiry card.



ELPAC POWER SUPPLIES

Completely Assembled

SPECIFICATIONS:
105-125/210-250 Vac, 47-440 Hz Input:

Line Regulation	±0.1%
Load Regulation	±0.1% no-load to rated-load
Output Ripple and Noise	±0.1% p-p, dc to 10 MHz
Input/Output Isolation	100 megohm dc, 900 Vac
Short Circuit Current	35% rated current

PART NO.	RATINGS WATTS	VOLTS	AMPS	PRICE
SOLV15-5*	15	5	3	$36.95
SOLV15-12*	15	12	1.5	36.95
SOLV30-5	30	5	6	59.95
SOLV30-12	30	12	3	59.95
OVP1	over voltage protection for SOLV30-5, -12			9.95

*SOLV15-5, 12 includes OVP installed

NEW! BULB-ENERGY SAVER

BULB-ENERGY SAVERS used for years by major industrial users — now available for home or office use. Bulb Savers can cut electrical bills by as much as 3%. BULB SAVERS lengthens light life by

1. Acting as an electrical "shock absorber" turns the bulb on slowly, eliminating the "thermal shock". Bulb life increases 300 percent.
2. Banishes Current "Surges". Cushions line voltage surges when other loads cut power line.
3. Reduces Energy Consumption.

Bulb lasts 3 or more times longer. Fits Standard Socket. 5 watts to 200 watts

	1-9	10+
BES-1	1.39 ea.	1.20

CRYSTALS
THESE FREQUENCIES ONLY

PART NO.	FREQUENCY	CASE	PRICE
CY1A	1.000MHz	HC33	5.95
CY1.84	1.8432MHz	HC33	5.95
CY2A	2.000MHz	HC33	5.95
CY2.01	2.010MHz	HC33	1.95
CY2.50	2.500MHz	HC33	4.95
CY3.27	3.2768MHz	HC33	4.95
CY3.57	3.579545MHz	HC33	4.95
CY3A	4.000MHz	HC18	4.95
CY4.91	4.916MHz	HC18	4.95
CY7A	5.000MHz	HC18	4.95
CY5.18	5.185MHz	HC18	4.95
CY6.14	6.144MHz	HC18	4.95
CY6.40	6.400MHz	HC18	4.95
CY6.55	6.5536MHz	HC18	4.95
CY12A	10.000MHz	HC18	4.95
CY14A	14.31818MHz	HC18	4.95
CY19A	18.000MHz	HC18	4.95
CY18.43	18.432MHz	HC18	4.95
CY22A	20.000MHz	HC18	4.95
CY30A	32.000MHz	HC18	4.95

TRIMMERS

10MM size trimmers -.394" Dia.

Part No.	1-9	10-24	25-49	100+
TR-11(value)	.35	.30	.25	.20

Resistance values - 100, 500, 1K, 2K, 5K, 10K, 20K, 50K, 100K, 200K, 1 meg

TRIMPOTS

Single-Turn - 1/2 Watt
Square - Top Adjust - 3/8" Size

Part No.	1-9	10-24	25-49	50-99
840P(value)	.99	.89	.80	.70

Resistance Values - 50, 100, 500, 1K, 2K, 5K, 10K, 20K, 50K, 100K, 200K, 500K, 1 meg

15-Turn - 3/4 Watt
Rectangular Side Adjust 3/4" x 1/4" Size

Part No.	1-9	10-24	25-49	50-99
830P(value)	1.35	1.25	1.20	1.15

Resistance Values - 50, 100, 500, 1K, 2K, 5K, 10K, 20K, 50K, 100K, 200K, 500K, 1 meg

1/16 VECTOR BOARD

	0.1" Hole Spacing Part No	P-Pattern L	W	Price 1-9	10 up
PHENOLIC	64P44 062XXXP	4.50	6.50	1.72	1.54
	169P44 062XXXP	4.50	17.00	3.69	3.32
EPOXY	64P44 062WE	4.50	6.50	2.07	1.86
GLASS	84P44 062WE	4.50	8.50	2.56	2.31
	169P44 062WE	4.50	17.00	5.04	4.53
	169P84 062WE	8.50	17.00	9.23	8.26
EPOXY GLASS COPPER CLAD	169P44 062WEC1	4.50	17.00	6.80	6.12

CONNECTORS

25 Pin-D Subminiature

DB25P(as pictured)	PLUG	$3.25
DB25S	SOCKET	4.95
DB51226-1	Cover for DB25 P or S	1.75

MOLEX CONNECTOR PINS

M-530-1 — $1.95/100 pins (minimum order) — $16.00/1000 pins

Pre-packaged in strips

INSTRUMENT/ CLOCK CASE

Injection molded unit. Complete with red bezel. 4½" x 4" x 1-9/16".

$3.49

MICROPROCESSOR COMPONENTS

P8085	CPU	$29.95	CDP 1802	CPU	$19.95
8080A	CPU	10.95	Z80	CPU	24.95
8212	8-Bit Input/Output	4.95	2650	MPU	26.50
8214	Priority Interrupt Control	7.95	MC6800	MPU	19.95
8216	Bi-Directional Bus Driver	4.95	MC6810AP1	128 x 8 Static Ram	5.95
8224	Clock Generator/Driver	5.95	MC6820	Periph. Interface Adapter	7.95
8228	System Controller/Bus Driver	5.95	MC6821	Periph. Interface Adapter	11.50
8251	Prog. Comm. Interface	9.95	MC6830L8	1024 x 8 Bit ROM	14.95
8255	Prog. Periph. Interface	10.95	MC6850	Asychronous Comm. Adapter	14.95

RAM'S

1101	256 x 1	Static	$1.49
1103	1024 x 1	Dynamic	.99
2101	256 x 4	Static	5.95
2102	1024 x 1	Static	1.75
2107/5280	4096 x 1	Dynamic	4.95
2111	256 x 4	Static	6.95
2112	256 x 4	Static	5.95
2114	4K x 1	Static 450ns	9.95
2114L	4K x 1	Static 450ns Low Power	10.95
2114-3	1K x 4	Static 300ns	10.95
2114L-3	1K x 4	Static 300ns Low Power	11.95
7489	16 x 4	Static	1.75
8101	256 x 4	Static	5.95
8111	256 x 4	Static	6.95
8599	16 x 4	Static	3.49
21L02	1024 x 1	Static	1.95
74200	256 x 1	Static	6.95
93421	256 x 1	Static	2.95
MM5262	2K x 1	Dynamic	3/1.00
MK4027 (UPD414)	4K	DYNAMIC 16 PIN	5.95
MK4116 (UPD416)	16K	DYNAMIC 16 PIN	29.95
TMS4044-45NL	4K	STATIC	14.95

ROM'S

2513(2140)	Character Generator (upper case)	$9.95
2513(3021)	Character Generator (lower case)	9.95
2516	Character Generator	10.95
MM5230N	2048 Bit Read Only Memory	1.95

USER MANUALS

1802M	CDP1802 Manual	$7.50
Z80M	Z80 Manual	7.50
2650M	2650 Manual	6.00

PROMS

1702A	2048 x 1	Famous	$5.95
5203	2048 x 1	Famous	14.95
82S23	32 x 8	Open C	5.00
82S115	4096 x 1	Bipolar	19.95
82S123	32 x 8	Tristate	5.00
74S287	1024 x 1	Static	7.95
2708	8K	EPROM	10.95
2716 T.I.	16K	EPROM	29.95
2716 Intel (2516 T.I.)	16K	EPROM	59.95
6301-1	1024 x 1	Tri-State Bipolar	3.49
6330-1	256 x 1	Open C Bipolar	2.95
74186	512 x 1	TTL Open Collector	9.95
74188	256 x 1	TTL Open Collector	3.95

SHIFT REGISTERS

MM5013N	1024 Bit Accumulator Dynamic	2.95
MM5016H	500/512 Bit Dynamic	.89
MM5017H	Dual 500/512 Bit Dynamic	2.95
2504T	1024 Dynamic	3.95
2518	Hex 32 Bit Static	4.95
2519	Hex 40 Bit Static	4.00
2522	Dual 132 Bit Static	2.95
2524	512 Dynamic	.99
2525	1024 Dynamic	2.95
2527	Dual 256 Bit Static	2.95
2528	Dual 250 Static	4.00
2529	Dual 240 Bit Static	4.00
2532	Quad 80 Bit Static	2.95
2533	1024 Static	2.95
3341	Fifo	6.95
74LS670	4 X 4 Register	1.95

UART'S

AY-5-1013	30K BAUD	$5.95

SPECIAL REQUESTED ITEMS

TELEPHONE KEYBOARD CHIPS

AY-5-9100	$14.95
AY-5-9200	14.95
AY-5-9500	4.95
AY-5-2376	14.95
HD0165	7.95
74C922	9.95

ICM CHIPS

ICM7045	$24.95
ICM7205	19.95
ICM7207	7.50
ICM7208	19.95
ICM7209	6.95

NMOS READ ONLY MEMORIES

MCM6571	$13.50
MCM6574	13.50
MCM6575	13.50

TV GAME CHIP SET
AY-3-8500-1 Chip and 2.010 MHz Crystal $7.95

MISCELLANEOUS

11C90	$19.95	MK40240	$17.50
MC3061P	11.95	DS0026CH	3.75
MC1408L7	4.95	TIL308	10.20
MC1408L8	5.75	95H90	11.95
LD110/111	$25.00/set		
MC4016(74416)	7.50		
4N33	3.95		

NEW

The Sinclair PDM35. A personal digital multimeter for only $59.95

Now everyone can afford to own a digital multimeter

Technical specification
DC Volts (4 ranges)
AC Volts
DC Current (5 ranges)
Resistance (5 ranges)
Dimensions
Weight
Power supply
Sockets
Options: AC adapter for 117 V 60 Hz power. De-luxe padded carrying wallet.

PART NO.	DESCRIPTION	PRICE
PDM35	Digital Multimeter (Completely Assembled)	$59.95
PDM-AC	117volt AC Adapter	6.95
PDM-DP	Deluxe padded carrying case	6.95

B&K PRECISION 3½-Digit Portable DMM

- Overload Protected
- 3" high LED Display
- Battery or AC operation
- Auto Zeroing
- 1mv, 1Va, 0.1 ohm resolution
- Overrange reading
- 10 meg input impendence
- DC Accuracy 1% typical

Ranges: DC Voltage - 0-1000V
AC Voltage 0-1000V
Freq. Response 50-400 HZ
DC/AC Current 0-100mA
Resistance 0-10 meg ohm
Size 6.4 x 4.4 x 2

Model 2800 $99.95
Comes with test leads, operating manual and spare fuse

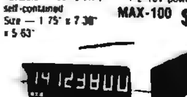
Accessories:

AC Adapter BC-28	$9.00
Rechargeable Batteries BP-26	20.00
Carrying Case LC-28	7.50

CSC 100 MHz 8-Digit Counter

- 20 Hz-100 MHz Range
- .5" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable — completely self-contained
- Size — 1.75" x 7.38" x 5.63"
- Four power souces, i.e. batteries, 110 or 220V with charger, 12V with auto lighter adapter and external 7.2-10V power supply

MAX-100 $134.95



ACCESSORIES FOR MAX 100:
Mobile Charger Eliminator — use power from car battery — Model 100 — CLA $3.95
Charger/Eliminator — use 110 V AC — Model 100 — CAI $9.95

63-Key Unencoded KEYBOARDS Hexadecimal Encoder

This is a 63-key, terminal keyboard newly manufactured by a large computer manufacturer. It is unencoded with SPST keys, unattached to any kind of PC board. A very solid molded plastic 13 x 4" base suits most application. IN STOCK **$29.95/each**

19-key pad includes 1-10 keys, ABCDEF and 2 optional keys and a shift key. **$10.95/each**

$5.00 Minimum Order — U.S. Funds Only
California Residents — Add 6% Sales Tax
Spec Sheets — 25¢
1978 A Catalog Available—Send 41¢ stamp

NEW NAME

Jameco ELECTRONICS

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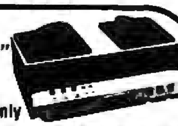
The Incredible "Pennywhistle 103"



$139.95 Kit Only

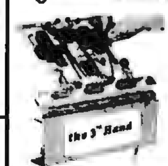
The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications for the deaf. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

Data Transmission Method	Frequency-Shift Keying, full-duplex (half-duplex selectable)
Maximum Data Rate	300 Baud
Data Format	Asynchronous Serial (return to mark level required between each character)
Receive Channel Frequencies	2025 Hz for space, 2225 Hz for mark
Transmit Channel Frequencies	Switch selectable: Low (normal) = 1070 space, 1270 mark; High = 2025 space, 2225 mark
Receive Sensitivity	-46 dbm acoustically coupled
Transmit Level	-15 dbm nominal. Adjustable from -6 dbm to -20 dbm
Receive Frequency Tolerance	Frequency reference automatically adjusts to allow for operation between 1800 Hz and 2400 Hz
Digital Data Interface	EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar)
Power Requirements	120 VAC, single phase, 10 Watts
Physical	All components mount on a single 5" by 9" printed circuit board. All components included.

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align

The Original the 3rd Hand

$9.95 each



- Leaves two hands free for working
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- Position board on angle or flat position for soldering or clipping
- Sturdy, aluminum construction for hobbyist, manufacturer or school rooms

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- Times to 59 minutes 59.59 seconds
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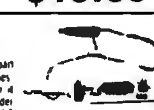
Model KB503 5V Power Kit	$17.50

JE700 CLOCK

The JE700 is a low cost digital clock, but is a very high quality unit. The unit features a simulated walnut case with dimensions of 6 x 2¼ x 4. It utilizes a MAN72 high brightness readout, and the MM5314 clock chip.

115 VAC — *KIT ONLY* **$16.95**

JE803 PROBE



The Logic Probe is a unit which is for the most part indespensible in trouble shooting logic families TTL, DTL, RTL, CMOS. It derives the power it needs to operate directly off of the circuit under test, drawing a scant 10 mA max. It uses a MAN3 readout to indicate any of the following states by these symbols: (H) 1 (LOW) 0 (PULSE) P. The Probe can detect high frequency pulses to 45 MHz. It can't be used at MOS levels or circuit damage will result.

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printed circuit board

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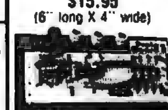

PB100 - 4.5" x 6"	$19.95
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PB102 - 7" x 4.5"	39.95
PB103 - 9" x 6"	59.95
PB104 - 9.5" x 8"	79.95
PB203 - 9.75 x 6½ x 2¾	80.00
PB203A - 9.75 x 6½ x 2¾ (includes power supply)	129.95

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14 PIN	$4.50
16 PIN	4.75
24 PIN	8.50
40 PIN	13.75

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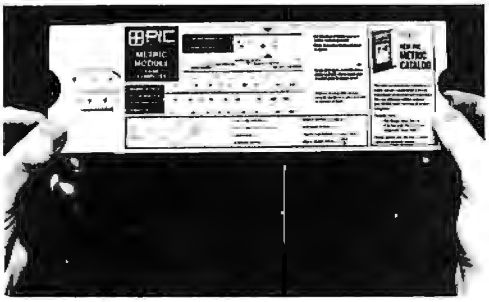
What's New?

PUBLICATIONS

PIC Offers Free Metric and Inch Gear Computer



The PIC Design Division of Benrus Corp now offers a metric and inch gear computer in a convenient, one setting, pocket slide rule. This design tool is capable of indicating 18 different gear functions instantly; inch gear data is on one side of the computer and metric module data on the other. One quick setting of the PIC gear computer gives simultaneous readings of metric modules, diametral pitch, tooth dimensions and circular pitch plus pitch diameter and outside diameter for both metric and inch gears. The PIC gear computer contains 16 basic gear formulas plus drawings which illustrate tooth size and configuration for both metric module and inch gears with 20° pressure angle. To send for your free computer write to PIC Design Div, Benrus Corp, POB 335, Benrus Center, Ridgefield CT 06877.■

Circle 605 on inquiry card.

1978 Smith Catalog Offers Many New Products

More than 20 new product groups representing several electronic component or hardware categories are among approximately 10,000 items featured in the newly published, multicolored, 104 page, 1978 full line catalog from Herman H Smith Inc, 812 Snediker Av, Brooklyn NY 11207. The free catalog includes a number of new binding posts, Mil-Spec-Jacks, fused test leads, the Hook-on Jr Probe with prods and leads, BredBlox and BredStix, BredBord kits, miniature and projection lamps, power terminals, lacing cords, wire nuts, rubber bumpers and many other new items. The catalog can be obtained by writing the company.■

Circle 606 on inquiry card.

New Products for the Commodore PET 2001

Getting Started with Your Pet is a workbook intended for PET users who are anxious to put their PET to work. This beginner's workbook is said to supplement the documentation provided by Commodore. It covers the fundamentals of PET BASIC and explains its characteristics, limitations and useful features. The descriptive text is said to include step by step, detailed exercises including the expected PET responses. In addition to this beginning text, workbooks on advanced topics are said to be available as well as software applications for the PET. No price was given, so for more information write TIS, POB 921, Los Alamos NM 87544.■

Circle 607 on inquiry card.

New Catalog from Alcoswitch

A complete line of miniature (7/8 inch diameter bushing) oil tight pushbuttons, selectors and pilot lights is described in Alcoswitch's new 12 page catalog, publication T278. Over 20 basic models are listed with details concerning control function options and color choices. The contact blocks offered range from logic types to 600 VAC models. This catalog will be sent free of charge to all inquiries. Contact Alco Electronic Products Inc, 1551 Osgood St, North Andover MA 01845.■

Circle 608 on inquiry card.

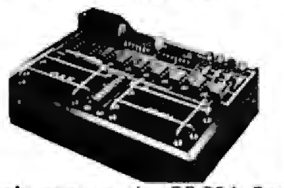
MicroAge Product Information

Literature describing MicroAge's printers, video boards, CRTs, monitors and keyboards is now available from the company. Included with the product descriptions is a complete price list. For this literature write MicroAge, 14250 12th Pl #101, Tempe AZ 85281.■

Circle 609 on inquiry card.

Circle 38 on inquiry card.

OPTICAL PAPER TAPE READER



Simply connect the OP-80A Paper Tape Reader to any 8-bit parallel port and pull the tape thru (0-5,000 cps). **A custom optical sensor array eliminates read errors found in lower cost units.** ***(This is the one that works!)*** **Complete with manual and interface cable. $84.50 Kit and $99.95 A & T.**

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Variations in tape speed between PHIDECK drives is the primary reason tapes recorded on different drives by you and your friends cannot be read.

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Then you need ROTA-STROBE.

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ROTA-STROBE is designed to work on PHIDECK drives manufactured by Triple I and sold by THE DIGITAL GROUP, PERIPHERAL VISION and others.

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Getting Started with Your PET WB-1 $4.00
Covers the fundamentals of PET BASIC: calculator and program mode, data input and output, data representation, program storage on the cassette.

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Covers string and substring search, concatenation, replacement and manipulation.

PET Graphics WB-3 $4.95
Covers use of cursor control and special graphics symbols to draw plots, histograms, and sketches.

PET Cassette I/O WB-4 $4.95
Covers OPEN, CLOSE, string and numeric data files

Miscellaneous PET Features WB-5 $3.95
Covers the clock, random number generator, upper and lowercase alphabetic characters, saving memory space, etc

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Is he sorting and searching his life away?
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Bring out his hidden talents with a sophisticated selection of **BAUDY JOKES AND BYTING WIT!**
Let your computer comic delight your friends with a dazzling display of wit and whimsy! Your computer will have the last laugh!
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Text Processor for the EPA Micro-68b Computer

TEXT is a word processor which executes on the EPA Micro-68b computer with the following equipment: 16 K bytes of programmable memory, one floppy disk unit, one video display terminal and a printer. TEXT accepts lines of source text interspersed with lines of format control information and formats the text into a printable, paginated document having user designated style. Some of the capabilities of TEXT include: left and right justification; automatic word hyphenation; page headings; page footings, including page numbers; indenting; centering; single, double or triple spacing of lines; footnotes and bibliography references.

The most important feature is that the text stream is free format, which means that the typist, with the aid of the EPA TEXT Editor, can type the document text in any convenient format and TEXT will format the output as desired.

For further information contact Chuck Bennett, Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110.■

Circle 575 on inquiry card.

A New DOS for Poly 88 and North Star Disk Systems

The Lazy Man's DOS (disk operating system) for Poly 88 owners with North Star Disk Systems has been announced by Cardinal Products, 1600 Tilden St, Wichita Falls TX 76309. According to the company, control character commands let you quickly and easily load and start BASIC, jump back to DOS, restart BASIC cold (initialized) or warm (retaining some user program data), list directory while in DOS or BASIC and bring up front panel mode at any time. List scrolling can be controlled on a line by line basis. The control Z is released for use in the BASIC editor. Delete key backspaces and erases a character at a time. The Poly 88 real time clock interrupt system may be left connected. Diskette and instructions are $15.95.■

Circle 576 on inquiry card.

Multitasking Executive Added to Microbench Software

MTX-11, a multitasking executive for PDP-11 and LSI-11 computers, is the latest addition to Microbench software. The MTX-11 is said to execute multiple tasks on an interleaved basis with software priorities determining which task to execute if competition exists for processor and system resources.

The MTX-11 is priced at $1395 plus $100 per processor and is available from Virtual Systems Inc, 1500 Newell Av, Suite 406, Walnut Creek CA 94596.■

Circle 577 on inquiry card.

Compiler BASIC Does Business, Control Applications on Microprocessor Systems

Software Dynamics BASIC, a compiler version of the programming language, is now available for 6800 microprocessor systems. Decimal arithmetic, formatted output and file IO is said to make SD BASIC ideal for microprocessor business applications such as payroll and inventory. High speed binary arithmetic, transcendental functions, assembly language interface and the performance resulting from compiling BASIC programs makes SD BASIC a tool for building process control programs. According to the company, the software is currently available on American Microsystems MDC, Smoke Signal Broadcasting BFD-68, SwTPC DOS and Wave Mate microcomputers. The IO Interface Package concept allows you to customize SD BASIC to your DOS system. Further information can be obtained from Software Dynamics, 18914 S Laurelbrook Pl, Cerritos CA 90701.■

Circle 578 on inquiry card.

Software for the H8

Two tapes are available for the Heathkit H8 computer from a newly formed company called Ed-Pro Inc, 6580 Buckhurst Tr, Atlanta GA 30349. According to the company, one of the tapes contains a collection of 11 game programs, while the other contains personal finance programs for checkbook reconciliation, budgeting and calculation of interest for various kinds of loans and investments. Tapes are supplied with complete program listings and user instructions. The tapes sell for $20 each (with a 10% discount if both are purchased).■

Circle 580 on inquiry card.

Assembly Language Development System for 8080 and Z-80

The Program Development System (PDS) is an assembly language development system for 8080 or Z-80 microcomputers with at least one disk drive. PDS is said to include a unified assembler/editor, a macro assembler combining the features of a relocating linking loader, a string oriented text editor, and a trace debugger/disassembler. The assemblers favor the Intel instruction mnemonics treating the Z-80 superset as a logical and syntactical extension. Source modules are available for floating point arithmetic, floating point IO, trigonometric functions, numerical and alphabetic sorting, matrix inversion, fast Fourier transform, and a full function expression evaluator. For further information contact Allen Ashley, 395 Sierra Madre Villa, Pasadena CA 91107.■

Circle 579 on inquiry card.

Data Base and Query System Responds to Pidgin English

It is said that your home or business computer can manage a data base of stored information and respond to your queries in pidgin English, using a new microcomputer software package called WHATSIT. The system runs in BASIC on a modest personal computer yet it brings the power of a data base manager. Data is stored and retrieved by typing pidgin English requests. Indexing and disk space allocation are handled automatically. The file structure is never frozen but develops automatically through normal use to adapt to user requirements. Stored information is automatically cross-indexed under any desired headings, and headings may be added or changed at any time. Available in North Star BASIC, the system runs in 24 K of memory. It is offered with three ready to run programs on a minidisk for $75. A manual written in nontechnical language is $25. It is available from Information Unlimited, 698 W 70 S Private Rd, Hebron IN 46341.■

Circle 583 on inquiry card.

Communications Software for LSI-11 Announced

The RT-11 compatible software driver for the Mighty-Mux 11L, direct memory access (DMA) serial line multiplexer, has been announced by Educational Data Systems, Inc, 1682 Langley Av, Irvine CA 92714.

Providing efficient IO for any RT-11 based LSI-11 system, this new package simultaneously supports full duplex asynchronous IO to as many as 128 ports on the multiplexer. Control requests are provided to determine port status, set port characteristics (bps rates, parity, etc), assign logical and physical port mapping, and abort IO requests.

For stand alone multiplexing operations, modules are provided which may be linked directly to an applications package. This avoids the intervention and overhead of the RT-11 IO subsystem. A second configuration loads the package as a standard RT-11 driver.

The driver will function with any VO2 system and is provided at no charge to users of the Mighty-Mux 11L.■

Circle 582 on inquiry card

Software for Users of North Star BASIC

A series of programs for users of North Star BASIC is available on North Star diskette with user instructions. Word processing, investments, inventory and other business oriented programs are offered. A complete catalog of North Star software is now available, including not only California Software material, but programs available from firms around the world. For further information contact California Software, POB 275, El Cerrito CA 94530.■

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Circle 308 on inquiry card.

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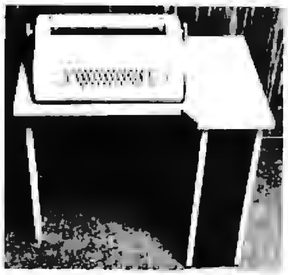
ASCII SELECTRIC



ASCII Selectric with ASCII parallel electronics.
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Weight: 120 lbs. Dimensions: 29"Hx35"Wx33"D.

Print Speed: (14.8 characters per second)

Platen: 15" wide, pin feed or form feed device optional (132 print positions).

Parallel output only—15 characters per second accepts 7 bit ASCII parallel w/strobe & prints on Selectric. The unit still works as a typewriter in off-line mode.

DATEL SELECTRIC (IBM Selectric Mechanism)

Specifications:
- Size: 21"Wx21"Dx8"H.
- Power Input 115 Volt Hz
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- Weight: 54 lbs. (Shipping weight 65 lbs.)
- 15" Carriage
- 15 CPS
- Correspondence code
- Half Duplex
- 132 Print Positions, 10 Pitch

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RS232 Connection
300 Baud

TI 990/4

Single Board 16 Bit Micro Computer

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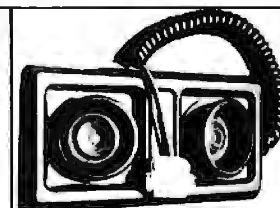

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Useable with most modem chips/kits
Used — $17.50 (w/prints)

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Texas residents add 5% sales tax. Please call if you have a question.
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SHIPPING INFORMATION:
Modems: $2.00 each; 2 for $4.00 UPS.
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40 line discrete display board

40 line switch input board

40 line new data board

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8 SLOT 44 PIN BUS
50 Pin Edge Connector

Mother Board $20.00 ea
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Card guides for above $10.00 per set.

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Discounts available at OEM quantities. For orders less than $25 total, add $1.25 for shipping. California residents add 6% sales tax. Estimated shipping time 2 days ARO with money order. For checks allow 7 days for check to clear.

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Apple BASIC Instructions...

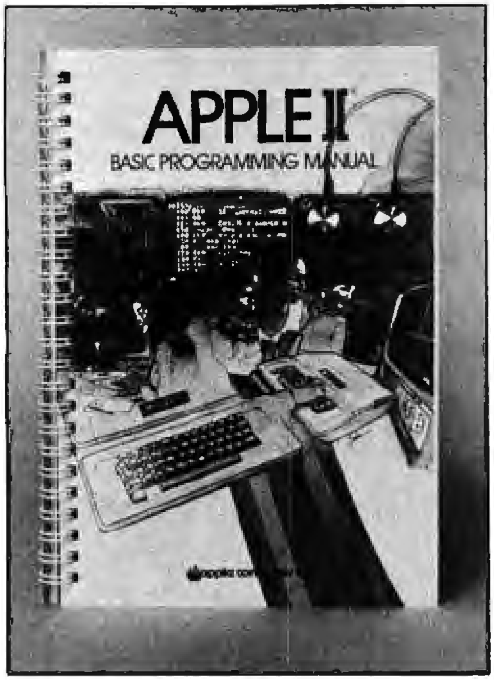


Photo 1.

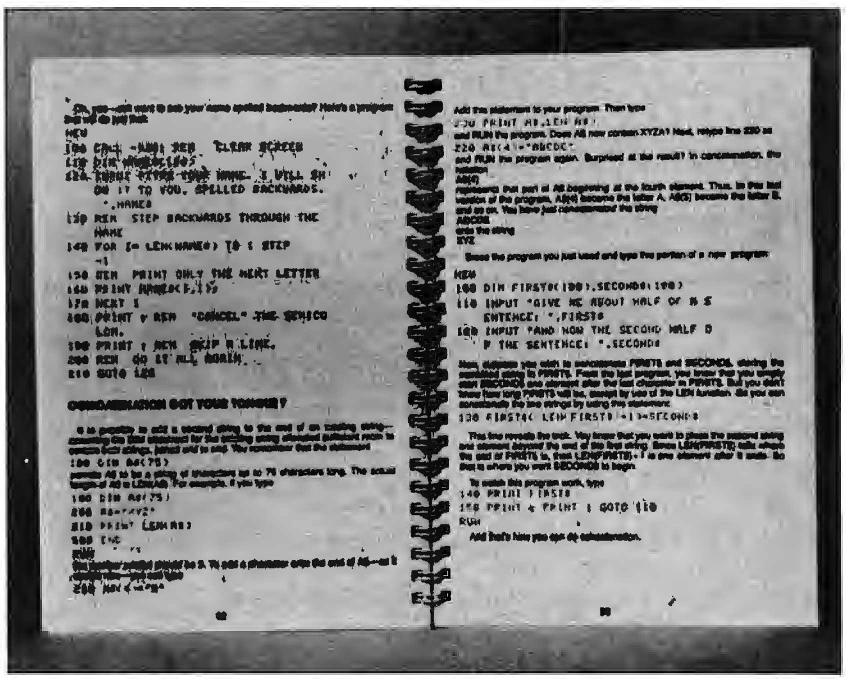
We recently received copies of the new *Apple II BASIC Programming Manual,* written by Jef Raskin of Apple Computer Inc, 20863 Stevens Creek Blvd, Bldg B3-C, Cupertino CA 95014. The manual measures about 6 by 8.5 inches (15 by 22 cm) with 125 pages bound within its covers. The book (see photo 1) is intended to be a working manual for familiarizing its reader with the Apple II computer. Whenever necessary, internal graphics include representations of the machine's keyboard highlighted with a green color to emphasize a point being made. Listings of computer output are often printed in green, as produced by a matrix printer. When a full screen image is represented, it is typically printed on the matrix printer and reproduced photographically as white on black to emphasize the image of a television screen. Full color reproduction is used for the several pages where actual Apple II output to a color TV is shown.

The manual begins with an introduction on the basics of the hardware and its interconnection. There is a description of the built-in 5 K integer BASIC. The introduction concludes with operation of one of the standard games supplied on cassette with the machine, Breakout. The next chapter is entitled Beginning BASIC, which in turn is followed by Elementary Programming. The formal presentation ends with Strings, Arrays and Subroutines as the last chapter. Several appendices complete the book. Photo 2 illustrates several points about the *Apple II BASIC Programming Manual.* First, note the light type and the heavy type in the photograph. The lighter printing is green in the original, the heavier printing is black. Second, there is Jef Raskin's inimitable sense of humor which makes the manual an enjoyable experience. Look at page 24 of the *Apple II BASIC Programming Manual* at a local computer store for one of the most elegant modifications of a standard typing test string ever seen. (The string begins "THE QUICK BROWN FOX . . . and in its original form is known to everyone, but in its modified form shows a certain humorous familiarity with the urban geography of the northeastern United States.)

While not a reference document by intent, users of Apples will find much information and a verbal delight in the form of this BASIC manual by Jef Raskin. . .CH■

Circle 597 on inquiry card.

Photo 2.



Software for the North Star Disk System

According to its developers, the Comprehensive Mailing List Program Package, #ML-1NS, is a modular program set which enables the user to start and maintain one or more mailing lists. Operations include: add, delete, search, sort, auto-sort, and sequential printout. Features include: user selectable defaults for ease of entry, user selectable number of labels across page for different printers and label sheets, and user selectable 3 or 4 line address for each independent entry. The software is available with documentation and diskette for $25 from Williams Radio and TV Inc, Computer Division, 2062 Liberty St, POB 3314, Jacksonville FL 32206.■

Circle 598 on inquiry card.

EMPL Interpreter for 8080

EMPL is a micro version of APL for the Intel 8080. It resides in the first 5632 bytes of memory. EMPL has numeric and character vectors, user defined niladic, monadic and dyadic functions, 22 primitive functions and nine system commands. It can be run either in the ASCII or APL character set. The range is ±32767 and double byte integer arithmetic is used. EMPL comes with a user's manual that includes information on implementing it on any system using Z-80 or 8080 processors with at least 8 K of memory. EMPL is $10 on Tarbell cassette; $20 on paper tape, North Star disk, CUTS cassette, or MITS cassette from Erik T Mueller, Britton House, Roosevelt NJ 08555.■

Circle 599 on inquiry card.

Utility Package for North Star Micro Disk System

A complete disk utility package for the North Star Micro Disk System is now said to be available from Micro Logistics, POB 922, Madison Square Station, New York NY 10010. PKGUT1 on diskette includes the following four 8080 machine language programs origined at 0: Packit: packs and unpacks disk files so you can get more storage per disk; Changit: prints, dumps and/or changes data in disk files up to a global level; Sortit: a generalized sorting utility; Compit: file comparison utility which will compare disk files sequentially or by key and display differences. Diskette with full user's documentation is priced at $80.■

Circle 600 on inquiry card.

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NLS MS-215 DUAL TRACE MINISCOPE $435.00

1¢ SALE

- LM3A 3 dig 1% DC $134.00
- LM3.5A 3½ dig .5% DC $158.50
- LM40A 4 dig .1% DC....... $209.00
- LM4A 4 dig .03% DC $250.00

- Rechargeable batteries and charger included
- Measures DC Volts, AC Volts, Ohms and Current
- Automatic polarity, decimal and overload indication
- Rechargeable batteries and charger
- Measures DC Volts, AC Volts, Ohms and Current
- Automatic polarity, decimal and overload indication
- No zero adjustment and no full-scale ohms adjust
- Battery-operated — NiCad batteries; also AC line operation.
- Large LED display for easy reading without interpolation
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$318. MS-15 MINISCOPE

With Rechargeable Batteries & Charger Unit

- 15 megahertz bandwidth
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- MS-216 Dual Trace Version of MS-15 **$435.**

SALE S 100 BUS EDGE CONNECTORS SALE

Other Popular Edge Connectors

3 LEVEL GOLD WIRE WRAP SOCKETS

	1-24	25-49	50-99	100-249	250-999	1K-5K
8 pin*	.41	.38	.35	.31	.27	.23
14 pin*	.39	.38	.36	.32	.29	.27
16 pin*	.43	.42	.39	.35	.32	.30
18 pin	.63	.58	.54	.47	.42	.36
20 pin	.80	.75	.70	.63	.58	.53
22 pin*	.90	.85	.80	.70	.61	.57
24 pin	.90	.84	.78	.68	.63	.58
28 pin	1.10	1.00	.90	.84	.76	.71
40 pin	1.50	1.40	1.30	1.20	1.04	.89

Sockets purchased in multiples of 50 per type may be combined for best price.

All sockets are GOLD 3 level closed entry *End and side stacable. 2 level, Solder Tail, Low Profile, Tin Sockets and Dip Plugs available. CALL FOR QUOTATION

Vector 8803 MOTHER BOARD FOR S100 BUS MICRO-COMPUTERS

Price: $29.50

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8800V Universal Microcomputer/processor plugboard, use with S 100 bus. Complete with heat sink & hardware 5.3 x 10 x 1/16

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3690 6.5" 22/44 pin 156 ctrs. Extenders $12.00

1/16 Vector BOARD

.042 dia holes on 0.1 spacing for IC's

	PART NO	SIZE	PRICE 1-9	10-19
Phenolic	64P44XXXP	4.5x6.5"	$1.49	1.34
	169P44XXXP	4.5x17"	$3.51	3.16
Epoxy Glass	64P44	4.5x6.5"	$1.70	1.53
	84P44	4.5x8.5"	$2.10	1.89
	169P44	4.5x17"	$4.30	3.87
	169P84	8.5x17"	$7.65	6.89

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Wraps insulated wire on .025" square posts FOUR TIMES FASTER

P180 $24.50

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NO PRE STRIPPING* NO PRE-CUTTING* SPOOL FED WIRE*

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2708 8K 450 ns EPROM

FACTORY PRIME $10.00 EA.

25 + Call For Price

WOW 14 & 16 PIN GOLD 3 LEVEL WIRE WRAP SOCKETS

14 - G3 100 for $30.00
16-G3 100 for $30.00
50 of each for $32.00

Sockets are End & Side stackable, closed entry

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- Small in size (2x2⅛x⅝)
- Push button for seconds release for date.
- Clocks mount anywhere with either 3M double-sided tape or VELCRO, included
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Perfectly balanced, fluorescent lighting with precision magnifier lens. For prof'l, techn'l & hobbist. Has die cast protective shade, inst. start 3 diopter lens 42" reach

$44.95 SPECIAL

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MICRO-KLIP

for .042 dia holes (all boards on this page)
T42-1 pkg 100 $ 1.50
T42-1 pkg 1000 $11.00
P-149 hand installing tool $ 2.83

.8" LED ALARM CLOCK

12 hr LED Alarm Clock uses 3½ digit .8" LED Display with AM/PM indicators and colons. Direct drive, PIN to PIN interface with 5. I.C. Just add switches, AC Supply Alarm Display and I.C. only

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Price Breakthrough! $17.50 MA1003 CAR CLOCK

Bright Green Fluorescent Display Crystal Time Base Assembled, just add switches and 12 VDC.

SPECIAL

- 14CS2 100 for $14.00
- 16CS2 100 for $16.00
- 14 pin CS2 10 for $2.00
- 16 pin CS2 8 for $2.00

These low cost DIP sockets will accept both standard width plugs and chips. For use with chips, the sockets offer a low profile height of only .125" above the board. These sockets are end stackable.

Vector WRAP POST

for .042 dia. holes (all boards on this page)
T-44 pkg 100 $ 2.28
T-44 pkg 1000 $14.00
A-13 hand installing tool $ 2.80

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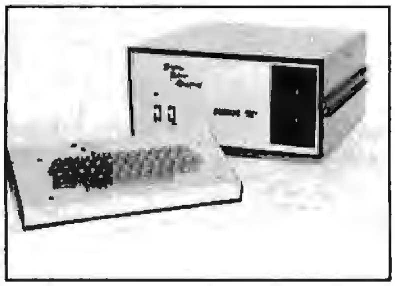
Circle 304 on inquiry card.

Compact Yet Versatile

The ZMS-70 contains a microcomputer system with up to 64 K bytes of memory, a 15 inch diagonal video display, an extensive keyboard, a telecommunications interface and 143 K bytes of on line disk storage. An optional internal hard copy printer interface and external printer is also available. The system is said to include an extensive set of software for both application program development and the day to day operational use of the system. This software comprises a general purpose disk based executive, a file manager, and a complete assembly language development package. In addition, a full set of test, diagnostic and utility programs are provided. Price is less than $5000 from Zentec Corp, 2400 Walsh Av, Santa Clara CA 95050.■

Circle 588 on inquiry card.

Sirius II Complete Computer System



The Sirius II computer system features two processors: the Mostek Z-80 for main computations and a Fairchild 3870 that handles all keyboard and video interfacing. Also included are 32.768 K bytes of programmable memory, an RS-232 interface for IO, 8.192 K bytes of programmable read only memory with a 1 K byte monitor supplied, minifloppy disk drive, a 64 key keyboard with alphanumeric and graphic capabilities, and a video interface. Other features include a full disk operating BASIC interpreter, monitor and software programs ranging from home management, personal finance, educational learning programs and process control to business software and games.

The Sirius II sells for $1850. For more information contact Digital Sport Systems, 7th and Elm Sts, West Liberty IA 52776.■

Circle 590 on inquiry card.

Desktop Computer from Cabinet to Complete System

This UC2000 S-100 based computer is presently available in five system configurations ranging from empty mainframe card rack to complete system with processor, memory, multiple floppy disk and printer. The console is provided with a 12 MHz 12 inch video display, 8 card slot mainframe, 18 A power supply, axial blower and various keyboard options. All subsystem modules are plug connected for easy maintenance. A 230 V 50 cycle power option is available and EMI filtered power connector is standard equipment. DB25 type connector slots are provided on the rear panel for peripheral interfacing. Although the complete systems B through E are supplied with a microcomputer using the 8080 processor, any S-100 compatible computer can be used in the A system version. Extensive software is available for the 8080 system. Prices start at $995. Contact Infinite Inc, 1924 Waverly Pl, Melbourne FL 32901.■

Circle 591 on inquiry card.

A New Desktop System

This new microcomputer system, designated System 88, is designed for professional and small business problem solving. The hardware consists of a main unit, upper and lower case keyboard with control keys, and quick updating video monitor. Hardware features include full eight level vectored interrupts and full graphics. The main unit uses an 8080 processor and accommodates from one to three minifloppy drives. The system includes complete operating software on disk plus word processor, BASIC and assembler. Software features include: system software with a file system and built-in application aids; BASIC on disk that has multidimensional strings and numeric arrays, MAT statement, PLOT statement to support graphics, program CHAINing, variable cross-reference listing by line number, inverse trigonometric functions, array functions SUM, PROD, MEAN, STD; text editor; integral RS-232 printer interface; and complete macroassembler on disk. The main unit of the System 88 has a walnut cabinet with a brushed aluminum front panel. Price for the system, excluding printer, starts at $2795. Contact PolyMorphic Systems, 460 Ward Dr, Santa Barbara CA 93111.■

Circle 589 on inquiry card.

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Factory "lay-arounds." Do they work? Who knows! A micro digital technicians bonanza. The complete guts are there. With black case and featherette band. 5 functions: HOURS, MINUTES, SECONDS, MONTH, & DATE. Sorry, no specs.
Cat. No. 955267 Wt 4 oz.

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□ 10-IC "DICE", microscopic circuits, teaches theory (#955068)	1.19	2 for 1.20
□ 1-6" HI-FI SPEAKER, full range, for car-n-home (#955204)	4.95	2 for 4.96
□ 1-LED WATCH GUTS, men's, how good? We don't know (#955267)	1.95	2 for 1.96
□ 1-UHF TUNER, solid state, standard type (#952927)	1.00	2 for 1.01
□ 10-SLIDE SWITCHES, asst pop styles (#951408)	1.00	20 for 1.01
□ 4-TANTALUM CAPACITORS, 6.8 uf 35V, dipped (#952281)	1.00	8 for 1.01
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□ 1-100KHZ MARKER CRYSTALS, approx for marker gen. (#952896)	1.95	2 for 1.96
□ 1-MOTHERBOARD EDGE CONNECTOR, 100 pins, .125" (#952987)	3.50	2 for 3.51
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□ 100-TERMINAL STRIPS, from 2 lugs up (#953136)	2.00	200 for 2.01
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□ 100-DISC CAPACITORS, long leads, marked, asst'd (#952886)	2.00	200 for 2.01
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□ 30-PANEL SWITCHES, slides, rotaries, mod, etc (#953268)	2.00	60 for 2.01
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□ MAN-4 READOUTS, bubble, red, com. anode, .19" (#951503)	2 for 1.00	4 for 1.01
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□ 8-PIN MINI-DIP (#952123)	4 for $1.19	8 for $1.20
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□ 18-PIN DIP (#953378)	6 for 1.19	12 for 1.20
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□ 800	2.50	2.51
□ 1000	2.75	2.76

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Type No.	Each	2 For	Type No.	Each	2 for	Type No.	Each	2 for
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□ SN7401	.19	.20	□ SN7470	.19	.20	□ SN74154	1.75	1.76
□ SN7402	.25	.26	□ SN7471	.35	.36	□ SN74155	.79	.80
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□ SN7407	.39	.40	□ SN7480	.19	.20	□ SN74161	1.25	1.26
□ SN7409	.39	.40	□ SN7482	.29	.30	□ SN74163	1.39	1.40
□ SN7410	.25	.26	□ SN7483	.99	1.00	□ SN74164	.79	.80
□ SN7416	.35	.36	□ SN7486	.49	.50	□ SN74165	.99	1.00
□ SN7417	.35	.36	□ SN7488	.79	.80	□ SN74166	1.99	2.00
□ SN7420	.32	.33	□ SN7489	3.49	3.50	□ SN74173	.99	1.00
□ SN7421	.49	.50	□ SN7490	.99	1.00	□ SN74174	1.79	1.80
□ SN7423	.29	.30	□ SN7491	1.29	1.30	□ SN74175	.99	1.00
□ SN7426	.19	.20	□ SN7492	.79	.80	□ SN74177	.79	.80
□ SN7430	.29	.30	□ SN7493	.69	.70	□ SN74179	1.99	2.00
□ SN7437	.19	.20	□ SN7494	.79	.80	□ SN74180	.49	.50
□ SN7438	.25	.26	□ SN7495	.59	.60	□ SN74182	.49	.50
□ SN7440	.19	.20	□ SN7496	.29	.30	□ SN74190	1.99	2.00
□ SN7443	.59	.60	□ SN7498	.79	.80	□ SN74191	1.75	1.76
□ SN7444	.19	.20	□ SN74107	.29	.30	□ SN74192	.85	.86
□ SN7446	1.25	1.26	□ SN74113	.39	.40	□ SN74193	.99	1.00
□ SN7450	.19	.20	□ SN74114	.25	.26	□ SN74194	1.25	1.26
□ SN7451	.19	.20	□ SN74121	.59	.60	□ SN74197	.75	.76
□ SN7453	.19	.20	□ SN74123	.69	.70	□ SN74198	1.50	1.51
□ SN7454	.29	.30	□ SN74126	.99	1.00	□ SN74200	3.50	3.51
□ SN7455	.19	.20	□ SN74136	.49	.50	□ SN74251	.79	.80
□ SN7460	.35	.36	□ SN74140	.49	.50	□ SN74284	5.99	6.00
□ SN7462	.35	.36	□ SN74145	.69	.70	□ SN74298	3.75	3.76
□ SN7464	.19	.20						

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□ LM300N	.49	.50	□ LM340T-6	1.49	1.50	□ LM704H	.19	.20
□ LM301V	.45	.46	□ LM340T-8	1.49	1.50	□ LM709N	.19	.20
□ LM301H	.45	.46	□ LM340T-12	1.49	1.50	□ LM709H	.49	.50
□ LM307V	.45	.46	□ LM340T-15	1.49	1.50	□ LM733N	.79	.80
□ LM308V	.29	.30	□ LM340T-18	1.49	1.50	□ LM741V	.25	.26
□ LM308H	.69	.70	□ LM340T-24	1.49	1.50	□ LM741H	.30	.31
□ LM309K	1.49	1.50	□ LM350N	.49	.50	□ LM747H	.59	.60
□ LM311V	.29	.30	□ LM376V	.29	.30	□ LM1304	1.49	1.50
□ LM311H	1.49	1.50	□ LM377N	2.25	2.26	□ LM1310	1.79	1.80
□ LM318V	.99	1.00	□ LM380N	1.39	1.40	□ LM1312	2.49	2.50
□ LM320H-5	.99	1.00	□ LM381N	1.99	2.00	□ LM1414V	.19	.20
□ LM320H-12	.99	1.00	□ LM386N	1.49	1.50	□ LM1458V	.39	.40
□ LM320H-15	.99	1.00	□ LM531H	1.49	1.50	□ LM1800N	.79	.80
□ LM320T-6	1.49	1.50	□ LM532N	.25	.26	□ LM3028H	.65	.66
□ LM322N	1.19	1.20	□ LM532H	.25	.26	□ LM3900N	.49	.50
□ LM324N	1.79	1.80	□ NE540H	5.95	5.96	□ LM3909V	1.25	1.26
□ LM339N	1.79	1.80	□ LM555V	.75	.76	□ LM4250	1.20	1.21
□ LM340K-5	1.49	1.50	□ LM556N	1.79	1.80	□ LM75451	.69	.70
□ LM340K-6	1.49	1.50	□ LM558V	.39	.40	□ LM75453	.69	.70
□ LM340K-8	1.49	1.50	□ LM558H	.39	.40	□ LM75491	.80	.81
□ LM340K-12	1.49	1.50	□ LM561N	1.00	1.01	□ LM75492	.80	.81
□ LM340K-15	1.49	1.50	□ LM565N	1.00	1.01	□ LM75494	.60	.61
□ LM340K-18	1.49	1.50	□ LM565H	1.00	1.01	□ PA263	1.50	1.51
□ LM340K-24	1.49	1.50	□ LM566	2.49	2.50	□ DM8864N	1.29	1.30
			□ LM567	2.39	2.40			

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			2.51

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□ 15. V	3 for 1.	6 for 1.01
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□ 24. V	3 for 1.	6 for 1.01
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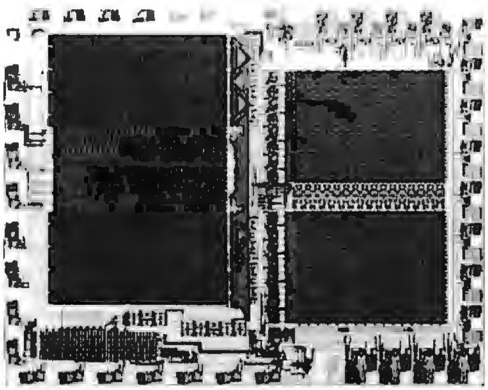
System Memory Interface Forms 2 Chip Microcomputer



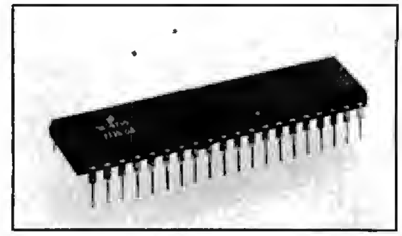
A single integrated circuit for microprocessor interfaces which incorporates its own memory, internal timing and IO ports is now available from Signetics. The 2656 system memory interface (SMI) can be combined with the Signetics 2650 processor to form a 2 chip microcomputer that provides system flexibility and additional memory and IO port expansion capabilities. The unit is useful for applications where both reduced chip count and system flexibility are necessary.

The Signetics SMI is a mask programmable circuit that offers 2 K by 8 bit programmable read only memory, 128 by 8 bit static random access memory, eight multipurpose IO pins for external chip selects or IO data port bits, an 8 bit latch for output data, and an internal clock generator programmed with crystal, RC or external input.

As an aid to system designers Signetics offers an SMI emulator on a single PC card that duplicates all the functional capabilities of the 2656 SMI chip. The emulator is priced at $250. The SMI chip is available in quantities of 1000 for $17. Contact Signetics, POB 9052, 811 E Arques Av, Sunnyvale CA 94086.■

Circle 610 on inquiry card.

Easy to Interface Chip Select USART



This Astro universal synchronous asynchronous receiver transmitter (USART), the UC 1971 Astro-Chip Select, is now available from Western Digital, 3128 Red Hill Av, POB 2180, Newport Beach CA 92663. This UC 1971 has many of the features of Western Digital's UC 1671 Astro Multiplexed Address: bisynchronous, asynchronous or isochronous modes, double buffered receiver and transmitter data, convenient interface to data sets and parallel processors. The UC 1971 Astro will interface with all popular microprocessors on the market.

The UC 1971, now second sourced, features the generalized computer interface control signals CS, AO, AI, RE and WE. Another design and operational plus for the UC 1971 Astro is the receiver clock and last transmitter bit outputs for external CRC generation and checking. The operating speed is DC to M bps. For further information and price contact Western Digital.■

Circle 611 on inquiry card.

Hexadecimal Label Switches Break Keyboard Cost Barriers

Stuck on any panel by its self-adhering backing, this microprofile keyboard avoids the congestion and the mounting hardware difficulties of mechanical keyboards. Label switches produce matrix coded output directly and will interface directly with integrated circuit 74C922 for conversion to a binary code. Labels do not bounce and so do not require the usual debounce electronics. Label switches are gold plated inside and outside and are sealed against the entry of dust or soft drinks. Life is estimated at 100 million operations. A self-contained flexible cable plugs into standard 0.1 inch (2.54 mm) spacing socket. Price is $3.95 in single quantities from Computronics Engineering, 7235 Hollywood Blvd, Hollywood CA 90046.■

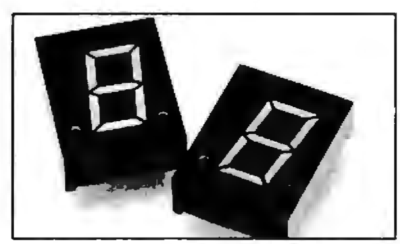
Circle 614 on inquiry card.

Optical Comparator for Rapid PC Board Inspection

An optical comparator for inspection of printed circuit boards or other flat electrical and mechanical assemblies is now available from TM Systems Inc, 25 Allen St, Bridgeport CT 06604. The Model 1013 optical comparator is a fully portable, compact device which optically compares production circuit boards with a master or standard assembly. Both boards are placed in the comparator and alternating images are superimposed for viewing by the inspector. Any errors are immediately identified and located. An image sequence rate from 1 to 10 per second can be front panel selected and the illumination intensity is infinitely variable. The comparator features all solid state electronics and is designed for operation under all lighting conditions at any assembly station. Power requirements are 115 V ±10%, 50/60 Hz, at 1 A.■

Circle 612 on inquiry card.

New .6 Inch LEDs from IEE



A line of red .63 inch LED digital displays designated as IEE-Hercules Series 1800 has been announced by Industrial Electronic Engineers Inc, 7740 Lemona Av, Van Nuys CA 91405. Series 1800 includes high brightness, dual element models and also single element models. The dual element LEDs consist of two chips of light emitting material which are electrically interconnected in series and act functionally as single segments. Both types of red LEDs have wide angle and long distance viewing with a high contrast ratio. Common anode and common cathode versions are available with right-hand and left-hand decimal points and ±1 overflow. Series 1800 LEDs are directly interchangeable with Litronix. At the 500 piece level, prices range from $1.65 each for single element to $1.88 each for dual element.■

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Kit $119.00 Assembled $149.00

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FEATURES

1 FULLY STATIC - USABLE WITH ALL DMA DEVICES
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7 PRICES QUOTED ARE FOR 300nS 200mW MEMORIES

— ASSEMBLED UNITS ARE FULLY TESTED AND BURNED IN
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10 AUXILIARY & CURSOR CONTROL KEYS
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—MAIN KEYBOARD SECTION OF 58 KEYS
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2517V	1.50	5554	1 90
2518B	1.50	5555	2.50
2519B	1 50	5556	2.50
2521	1 50	5055	1.25
2522	1 50	5312	4 00
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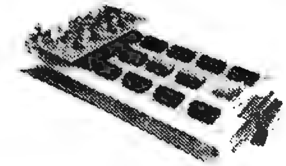

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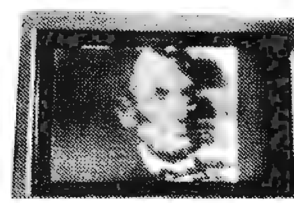

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Ear Ear for the June Bomb

Two "ear" oriented articles were at the top of the June 1978 BOMB results. First prize of $100 goes to Steve Ciarcia for his article "Talk to Me: Add a Voice to Your Computer for $35," page 142. The $50 second prize goes to Bill Georgiou for "Give an Ear to Your Computer," page 56. The two articles placed 1.6 and 1.3 standard deviations above the mean, respectively.■

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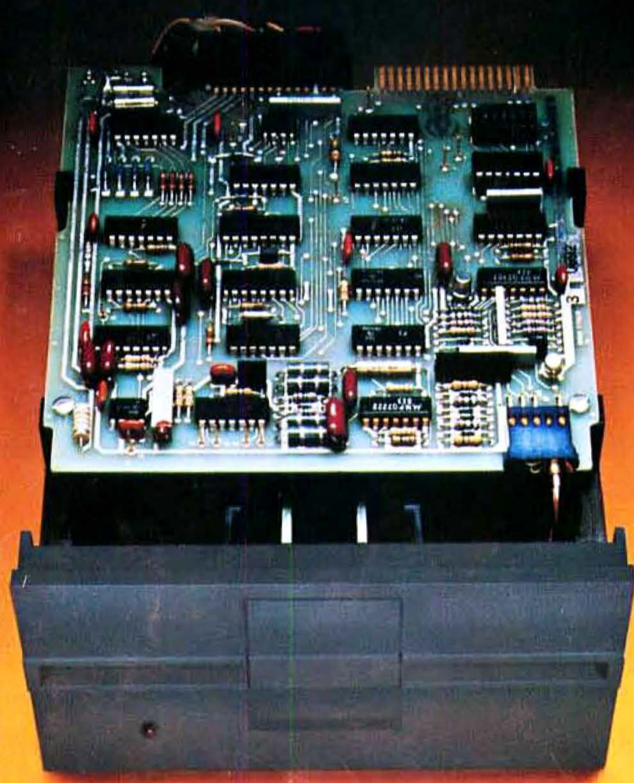

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