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the small systems journal


SYSTEM B
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CT-64 TERMINAL SYSTEM

see next page

In the Queue

BYTE October 1978
Volume 3 Number 10

Foreground

Background

Nucleus

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…y's painting on the cover this month is a fanciful image of computer chess. A Knight floats above an ancient stone chessboard with the ubiquitous floppy disk beneath. Four articles in this issue are devoted to the art of computer chess, including the first part of a 4 part series by the creators of Chess 4.6, the world championship chess program.

In This BYTE

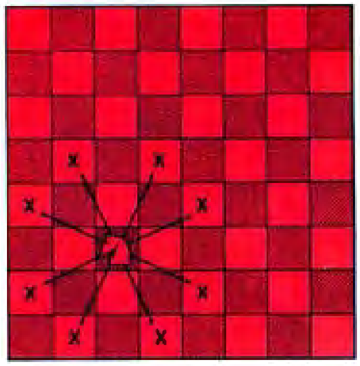
One cause of seemingly unexplainable program errors may be incorrectly operating memory. A Memory Pattern Sensitivity Test discussed by Don Kinzer will help to determine if your memory is operating correctly. *page 12*

If you need −12 or +15 V for your latest hardware design, and have only +5 V, what can you do? Read No Power for Your Interfaces? Build a 5 W DC to DC Converter by Steve Ciarcia. Several inexpensive, practical designs are described, to give you everything from −15 to +15 V from a +5 V source. *page 22*

In Part 1 of A "Tiny" Pascal Compiler, in the September 1978 BYTE, Kin-Man Chung and Herbert Yuen described the syntax of a Pascal subset and described a hypothetical stack machine, called a p-machine. This month they describe a compiler that generates codes for the p-machine. *page 34*

Would you like a fast and easy way to test your new memory board? Author Russell Adams shows you how in Testing Memory in BASIC. A simple program loads the memory locations with alternating 1s and 0s to spot those bad bits. *page 58*

The H8 computer from Heath features a novel firmware front panel monitor comprised of both hardware and software elements. Gordon Letwin, Heath software designer, describes the design philosophy and the features of the system in PAM/8: A New Approach to Front Panel Design. *page 70*



The winning program at the Second West Coast Computer Faire's Microcomputer Chess Tournament in March of 1978 was Sargon, written in Z-80 assembler language. Sargon's creators, Dan and Kathe Spracklen, describe the move generating portion of their program in First Steps in Computer Chess Programming. *page 86*

A computer allows you to try out a variety of ideas with nothing more than a program to see if they will work. One way to use this potential is to model electrical circuits in software. Leonard H Anderson describes how to perform Linear Circuit Analysis on your computer. *page 100*

The eight Queens problem is a venerable puzzle in recreational mathematics. Terry Smith describes his thought processes in working out a solution in his article, Solving the Eight Queens Problem. An occasional dose of cleverness is often the key to solving a difficult problem, as Terry demonstrates. *page 122*

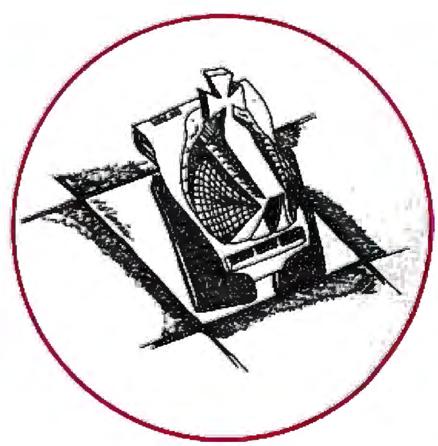
For someone who is looking for a good quality video terminal which is easy to work with and will be user serviceable, the Heathkit H9 is the solution. Terry Steeden describes his pleasant experiences Assembling the H9 Video Terminal and having it work correctly the first time. *page 130*

Digital recording of computer programs and data is an attractive alternative to standard audio cassette recording techniques because of its reliability and simplicity. Ralph Burhans describes an updated version of earlier digital recording schemes in A Simpler Digital Cassette Tape Interface. *page 142*

If you own a SwTPC 6800 computer and want to increase the processor clock speed with a minimum of fuss, read Souping Up Your SwTPC 6800 by Steve A Hughes. The article describes a simple circuit that plugs directly into a socket on the 6800 processor board. Changing the clock speed is then done by simply plugging in a new crystal oscillator. *page 144*

Last year we ran a contest in which readers were asked to design their own PAPERBYTE™ bar code readers and submit them to us. One of the winning entries, by Campbell Farnell and Glen Seeds, is described in their article, A Novel Bar Code Reader. *page 162*

For a short introduction to the world of computer chess, read Norman Whaland's A Computer Chess Tutorial. The basic principles of chess strategy and tactics are covered in discussions of game trees, alpha-beta pruning, minimax strategies and so on. *page 168*



Creating a Chess Player was written by two people at the forefront of research in computer chess: David Frey, editor of *Chess Skill in Man and Machine*, and Larry Atkins, coauthor of Chess 4.6, the world champion chess program that recently beat a Grandmaster in a simultaneous exhibition. The article discusses the thinking processes in the chessplayer's mind and how such processes are transformed into a computer program. *page 182*

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On Using a Personal Computer for a Practical Purpose

Editorial

by Carl Helmers

Finally, it had to happen to me. We all know that personal computers are supposed to be a cross between a necessity and a luxury. But the critics tend to harp on our tendency to get carried away by the fun and to ignore the practical uses of our wonderful servants. As if to answer that justified criticism, I finally came up with a genuine practical use for a small computer in the monthly operations of BYTE's editorial office. Now this practical application is by no means the kind of automated editing and type preparation facility I would like to have some day if and when I ever become rich and famous. But this is a genuine, once a month, cyclically run application program.

At BYTE, we have so far purchased two Apple II computers (among others) for use in educating our employees, and in order to have some facilities around the office. One of these Apple II computers sits in my office, and at the time of this exercise

Continued on page 147

Rank	Topic	Total Weighted Count	Standard Deviations Away from Mean
1	Applications to everyday life	12888	2.178
2	Household automation with computers	12886	2.177
3	Personal data base design and implementation	10911	1.179
4	Applications to personal business	10683	1.064
5	Voice recognition by computers	10654	1.049
6	The art of programming	10552	.997
7	Logical games (require much thinking, no dexterity)	10277	.858
8	Voice synthesis with computers	10014	.725
9	The art of hardware design	9875	.655
10	Computer control of mechanisms	9832	.633
11	Graphics software design	9707	.570
12	Artificial intelligence: general interest in AI	9523	.477
13	Action games (require much thinking, no dexterity)	9465	.448
14	Educational uses of computers	9439	.435
15	Computer system design	9311	.370
16	Text editing and processing	9233	.330
17	Graphics hardware design	8876	.150
18	Applications of computers to engineering	8766	.092
19	Experimentation with designs	8723	.073
20	General robotics: whole systems	8642	.032
21	Applications of computers to physical science	8593	0.
22	Chess and computers	8553	−.013
23	Computer communications networks	8424	−.079
24	Simulations of real or mythical situations	8315	−.134
25	AI: pattern recognition	8221	−.181
26	Design of information structures	8111	−.237
27	Use of graphic displays for artistic purposes	7556	−.517
28	Mathematical analysis and algorithm design	7551	−.520
29	Language design	7534	−.529
30	Compiler or interpreter design	7273	−.669
31	AI: representations of knowledge	6982	−.848
32	AI: Natural language parsing	6531	−1.035
33	Computers used for musical purpose: real time performance	6477	−1.062
34	Applications of computers to biological sciences	5785	−1.412
35	Amateur radio and computers	5369	−1.623
36	Computers and music: stochastic composition	5138	−1.739
37	Application of computers to social sciences	4745	−1.938
38	AI: theorem proving	4686	−1.968

Table 1: Respondents were asked to assign a numerical preference from 0 (no interest) to 10 (highest interest) for each of these 38 categories. The column labelled total weighted count contains the sum of counts in each possible response (1 to 10) multiplied by the response itself. Thus if a count of 29 were found in the interest weight 7 for some category, the contribution to the weighted sum would be 7 x 29 = 203. The standard deviation and mean were calculated for the data, and the deviation from the mean was expressed in the rightmost column in units of one standard deviation for each category. These data were "output" to a typewriter from the screen of the Apple II using a manual process, then typeset in the usual method.

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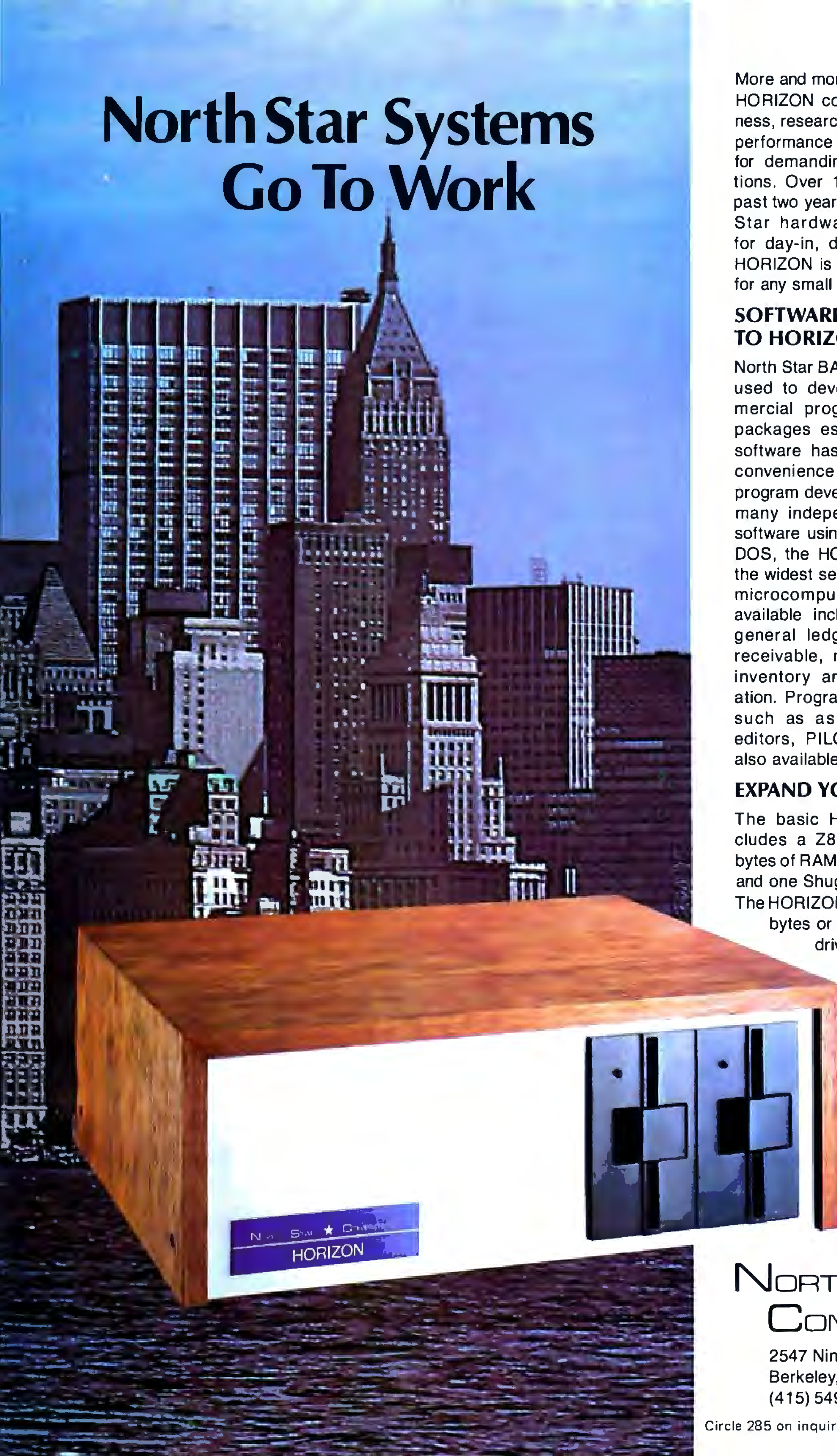

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Letters

TOP-DOWN MODULAR PROGRAMMING

I enjoyed the article, "Top-Down Modular Programming," by Albert D Hearn in July 1978 BYTE, page 32; I thought he did a good job of explaining the subject. While I realize that he was purposely trying to simplify matters, I do take exception to his comment that a module should be no more than 50 lines long.

The concepts of structured programming are intended as guidelines, not as the dogma for a programmer's religion. All of the better known proponents of the methodology stress this point, along with the idea that you must approach the study of structured programming with your eyes open, making your own evaluation. In this light let us explore the 50 line limit.

One of the bases for breaking a program up into modules is so that a complex problem can be handled with *small*, easy-to-understand pieces of code. One of the thoughts about module size is, therefore, that a module ought to be able to fit on the printed page. This is so that all the information about the module is in one place and the programmer doesn't have to thumb through several pages to read the code for a single module. (Having experienced "modules" running as long as 10 to 15 pages, I heartily agree with this philosophy.)

In professional programming installations this idea has frequently been translated into a local standard of about 50 lines of code, since this is the number of lines which are printed on an 8½ by 11 inch (21.25 by 27.5 cm) page coming out of a line printer (allowing for headers, footers, etc). For the personal computer enthusiast, however, this limit might be more conveniently set at 24, 32 or 40 lines — the size of the video display.

For many more complex problems, it is possible that a significant module cannot be constructed in 24 lines. This is no problem — just make the modules longer. The point is to try to restrict the module size to a length which enhances the programmer's ability to understand the code.

The basics of structured programming must be studied, evaluated, and possibly modified to work in each individual situation. There are a lot of great ideas included in the structured programming lore, but they should not be adopted blindly.

Jim Fleming
2220 Sims Dr
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Continued on page 156

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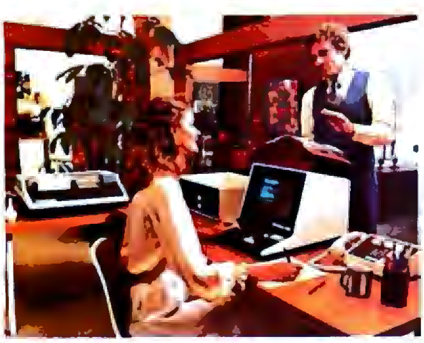

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You'll find a fully equipped service department to provide whatever assistance is required to keep your computer running in top-notch condition. You'll find computer user's clubs to join, where you can share ideas with people as enthusiastic as yourself. And, with each new visit, you'll find excitement—from the people you deal with, the equipment they offer, and from your own ever-growing personal involvement.

Enough about us. How about what computers do. To attempt to describe all the things your computer might do, would be to describe your imagination. So instead, we'll briefly list some of the many things for which small computers are already being used.

In business, the advent of the versatile and compact microcomputer has put the benefits of computing within reach of small companies. With systems starting at less than $6000, the businessman can computerize things like accounting, inventory control, record keeping, word processing and more. The net result is the reduction of administrative overhead and the improvement of efficiency which allows the business to be managed more effectively.

COMPUTERS FOR THE HOME

In the home, a computer can be used for personal budgeting, tracking the stock market, evaluating investment opportunities, controlling heating to conserve energy, running security alarm systems, automating the garden's watering, storing recipes, designing challenging games, tutoring the children . . . and the list goes on.

In industry, the basic applications are in engineering development, process control, and scientific and analytical work. Users of microcomputers in industry have found them to be reliable, cost-effective tools which provide computing capability to many who would otherwise have to wait for time on a big computer, or work with no computer at all.

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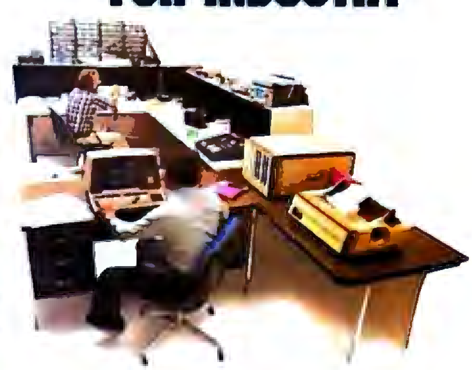

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A Memory Pattern Sensitivity Test

Don Kinzer
3885 NW Columbia Av
Portland OR 97229

Faulty memory is a very difficult problem to detect. Most distributors of memory board kits supply a simple memory test designed to detect assembly errors such as misplaced components, solder bridges, etc. These tests are ineffective in detecting certain types of memory related problems. One of these problems, called pattern sensitivity, manifests itself in the very disturbing fact that accessing one memory location alters another memory location, but only when the memory contains a certain pattern of bits.

It is my intention, through this article, to make the experimenter aware of potential memory problems and to provide some information which may be helpful in diagnosis of the problems by discussing a recent experience.

Every memory test is capable of detecting only a certain few of the many possible memory faults. Because of this, the user should be armed with a battery of memory tests and run them all at the first sign of trouble. Better yet, the tests could be run at regular intervals. A very good selection of such tests is contained in a package available from Technical Systems Consultants (POB 2574, W Lafayette IN 47906) as their SL68-23 Diagnostic Package. This package contains, among other tests, five memory tests, written in 6800 code, to expose bad bits, convergence problems and some types of pattern sensitivity. This package is highly recommended for all system users as the tests can be rewritten for the user's own machine.

As indicated before, the more tests, the better. The new test I am about to describe was discovered quite by accident. I was writing a resident assembler for my 6800 and was working on the sort routine which alphabetizes the symbol table. The sort, called a shell sort, works by comparing symbol table entries and exchanging them if they are not in alphabetical order. The process involves a tremendous amount of data shuffling. To my dismay, after the sort, the labels and their values had changed. TEMP1 became TEMQ1. Before the sort MASK was hexadecimal 3E; after the sort it was hexadecimal BE. Needless to say, I wasted a lot of time looking for a software bug before I decided to test the memory. The tests from the Technical Systems Consultants diagnostic package revealed a 2102 with pattern problems. However, replacing the bad memory did not stop the errors.

It occurred to me that writing a test program which operated in a manner similar to the sort routine would help track down

Listing 1: Memory EXCHANGE program written for the 6800 to test for memory pattern sensitivity.

```
                  *
                  *
                  *          EXCHANGE
                  *              A MEMORY TEST
                  *
                  *
                  *
                  *  EXTERNAL ROUTINES (MIKBUG ROUTINES)
E07E              PDATA   EQU   $E07E
E1D1              OUTCH   EQU   $E1D1
E067              OUTHL   EQU   $E067
E06B              OUTHR   EQU   $E06B
                  *
                  *
                  *  STORAGE
0000                      ORG   0
0000              BEGIN   RMB   2
0002              END     RMB   2
0004              XTEMP1  RMB   2
0006              XTEMP2  RMB   2
0008              COLCNT  RMB   1
                  *
                  *
0009  8E A0 7F    INIT    LDS   #$A07F      set up stack
000C  BD 00 9D    START   JSR   PCRLF       go do CRLF
000F  37          LOOP    PSHB              save starting point
0010  DE 00               LDX   BEGIN       get beginning address
0012  09                  DEX               adjust
0013  08          INITLP  INX               point next location
0014  E7 00               STAB  0,X         initialize
0016  5C                  INCB              set next value
0017  9C 02               CPX   END         see if done
0019  26 F8               BNE   INITLP      if not, do again
                  *
                  *
001B  DF 06       BUBBLE  STX   XTEMP2      save end pointer
001D  DE 00               LDX   BEGIN
001F  DF 04       EXCHG   STX   XTEMP1      save top pointer
```

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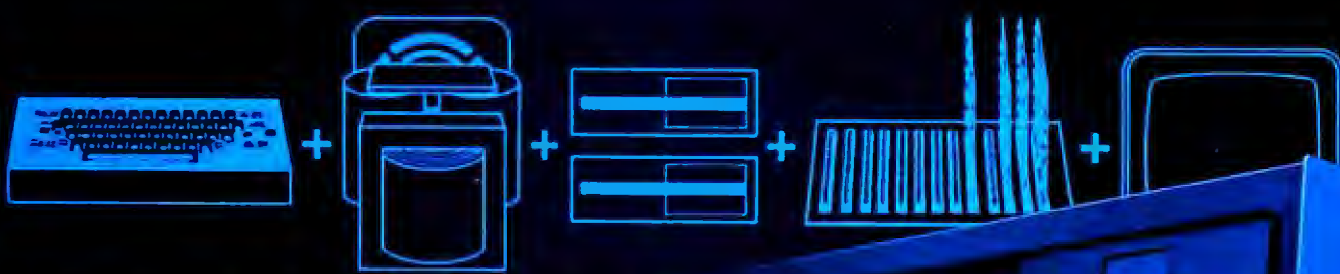

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Listing 1, continued:

```
0021  A6 00             LDAA  0,X       get byte
0023  DE 06             LDX   XTEMP2
0025  E6 00             LDAB  0,X       get other
0027  A7 00             STAA  0,X       put alternate
0029  09                DEX
002A  DF 06             STX   XTEMP2
002C  DE 04             LDX   XTEMP1    get other pointer
002E  E7 00             STAB  0,X       put byte
0030  9C 06             CPX   XTEMP2    check done
0032  27 05             BEQ   CHK1
0034  08                INX
0035  9C 06             CPX   XTEMP2    check done
0037  26 E6             BNE   EXCHG
0039  32         CHK1   PULA
003A  36                PSHA            get starting value
003B  4A                DECA            adjust
003C  DE 02             LDX   END       get end pointer
003E  DF 06             STX   XTEMP2    set end pointer
0040  DE 00             LDX   BEGIN     get begin pointer
0042  DF 04             STX   XTEMP1    save
                 *
                 *
0044  DE 06      CHECK  LDX   XTEMP2    get current pointer
0046  4C                INCA            set value
0047  A1 00             CMPA  0,X       check match
0049  26 1F             BNE   ERROR     if not, error
004B  9C 00      CONTIN CPX   BEGIN     see if checked all
004D  27 0C             BEQ   GOOD      if so, good pass
004F  DE 04             LDX   XTEMP1
0051  08                INX
0052  DF 04             STX   XTEMP1    advance pointer
0054  DE 06             LDX   XTEMP2
0056  09                DEX
0057  DF 06             STX   XTEMP2    retard pointer
0059  20 E9             BRA   CHECK     go check next
                 *
                 *
005B  86 21      GOOD   LDAA  #'!'
005D  8D 33             BSR   PRINT     signal good pass
005F  7A 00 08          DEC   COLCNT    need CRLF?
0062  26 02             BNE   PASS      if not, skip
0064  8D 37             BSR   PCRLF     perform CRLF
0066  33         PASS   PULB            get old value
0067  5C                INCB            set new value
0068  20 A5             BRA   LOOP      do again
                 *
                 *
006A  E6 00      ERROR  LDAB  0,X       get contents
006C  37                PSHB            save
006D  36                PSHA            save check value
006E  8D 2D             BSR   PCRLF     new line
0070  96 06             LDAA  XTEMP2
0072  8D 21             BSR   OUT2H
0074  96 07             LDAA  XTEMP2+1
0076  8D 16             BSR   OUT2HS    print address
0078  96 04             LDAA  XTEMP1
007A  8D 19             BSR   OUT2H
007C  96 05             LDAA  XTEMP1+1
007E  8D 0E             BSR   OUT2HS    print alternate address
0080  32                PULA
0081  16                TAB
0082  8D 0A             BSR   OUT2HS    print check value
0084  32                PULA
0085  8D 07             BSR   OUT2HS    print contents
0087  8D 14             BSR   PCRLF     new line
0089  17                TBA
008A  DE 06             LDX   XTEMP2    get pointer back
008C  20 BD             BRA   CONTIN    start new pass
                 *
                 *
008E  8D 05      OUT2HS BSR   OUT2H     print 2 characters
0090  86 20             LDAA  #' '
0092  7E E1 D1   PRINT  JMP   OUTCH     print character
                 *
                 *
0095  36         OUT2H  PSHA            save byte
0096  BD E0 67          JSR   OUTHL     print left hexadecimal digit
0099  32                PULA
009A  7E E0 6B          JMP   OUTHR     print right hexadecimal digit
                 *
                 *
009D  CE D0 A7   PCRLF  LDX   #CRLF     point to string
00A0  86 20             LDAA  #32
00A2  97 08             STAA  COLCNT    set column count
00A4  7E E0 7E          JMP   PDATA     go print string
                 *
                 *
00A7  0D 0A      CRLF   FCB   $D,$A
00A9  00 00             FCB   0,0
00AB  00 00 04          FCB   0,0,4
                 *
                 *
00AE                    END
```

the trouble. The result is a program called EXCHANGE which is shown in listing 1. The program works by initializing the memory to be tested to a sequence of the 256 eight bit numbers. Then pointers are set to the beginning and end of that same block of memory, XTEMP1 and XTEMP2 respectively. Next, the data at each of the pointers is exchanged. The pointers are then moved toward one another. The process of exchanging and moving repeats until the pointers meet. The inverted sequence is then checked for accuracy. Any discrepancies are reported by printing the memory location which is incorrect, the location where the data resided before the exchange, what the data was supposed to be and what the data actually was.

The first time I ran the test, the program crashed. The memory problem had caused a byte of the program to change. After several tries with the same results, I took my machine to work and attached an oscilloscope to the data bus. I found that the data lines had an unbelievable amount of noise. At the advice of a friend, I installed resistive terminations on the data lines, which immediately cleaned up the signals. This eliminated the majority of the memory problem and even allowed the EXCHANGE program to run without crashing. Several hours of further testing using EXCHANGE exposed three more malfunctioning 2102s in my 12 K byte system.

After all of this I am happy to say that the sort routine was in fact working properly. Furthermore, the pattern sensitivity problem explains away several bugs in other programs I have worked on.

Before closing I would like to offer a few pointers on using EXCHANGE. If you suspect memory problems, run a bit test or convergence test to rule out physical problems (like shorted wires) and bad bits (nonfunctioning memory parts). If the problem persists, run EXCHANGE on the entire contiguous memory (except, of course, where EXCHANGE is located) noting any errors as they are printed. Next, run EXCHANGE on smaller areas corresponding to each set of 2102s. Replace the memory chips as necessary but don't throw them away yet. If the memory is still bad in the same area then the memory chips are not to blame and it is time to put an oscilloscope on your system to see what the problem is.

Based on my own experience with a homebrew computer I recommend running a battery of tests after any system hardware changes to uncover memory problems before they turn up as a bug in your next program.■

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No Power for Your Interfaces?

Photo 1: *5 W DC to DC converter, which produces 0.2 A at +12 and −12 VDC from a 5 VDC source. The circuit uses a special custom wound toroidal transformer (see figures 5a and 5b). Note: the prototype shown uses 1000 µF 25 V capacitors, which were later replaced with 100 µF 25 V versions.*

Ciarcia's Circuit Cellar

Build a 5 W DC to DC Converter

Steve Ciarcia
POB 582
Glastonbury CT 06033

Recently I attended a local computer club meeting where we discussed the question of power supplies. Many people were remarking that, while they enjoyed building the projects in my articles, often their power supplies were not compatible with the multiple voltages I required. Many of the newer single board computers that some members owned contained only a hefty +5 V supply and a note that the user should add additional supplies if the basic board is expanded.

This is not an industry copout by any means. The newest digital designs from companies like Intel are made to run on +5 V and this is considered an advance in technology. The 8080A processor requires +12, +5 and −5 V for operation, while the new 8085 uses only a single +5 V supply. As long as all other components such as universal asynchronous receiver-transmitters (UARTs), programmable memories, erasable read only memories (EROMs) and read only memories (ROMs) in the computer are all +5 V, we can eliminate additional power supplies and save money. Computer manufacturers have done just that.

This situation does not cause any problems as long as the user stays with the basic unit, or expands it using single +5 V supply devices. Erasable read only memories such as the Intel 2716 and programmable peripheral interfaces such as the 8255 are designed specifically for this application.

The problem arises when the single supply computer tries to be communications compatible with the rest of the world, or when a bipolar analog interface is added. The RS-232C interface generally requires + and −12 V potentials, and digital to analog converters such as the Motorola 1408L8, which run on +5 and −12 to −15 V.

The Whole World Isn't TTL Compatible

What is the experimenter to do when a −15 V supply is needed and the computer has only +5 V, or when one wishes to tie an RS-232 terminal into a system? Obviously the answer is to add an additional power supply or two—but, what kind?

Power supply requirements should be based on load requirements. If 0.5 A at +15 V is needed to power a particular interface, then perhaps a 1 A traditional transformer-rectifier-filter-regulator design is in order. More often than not, though, the interface might use one or two dual supply

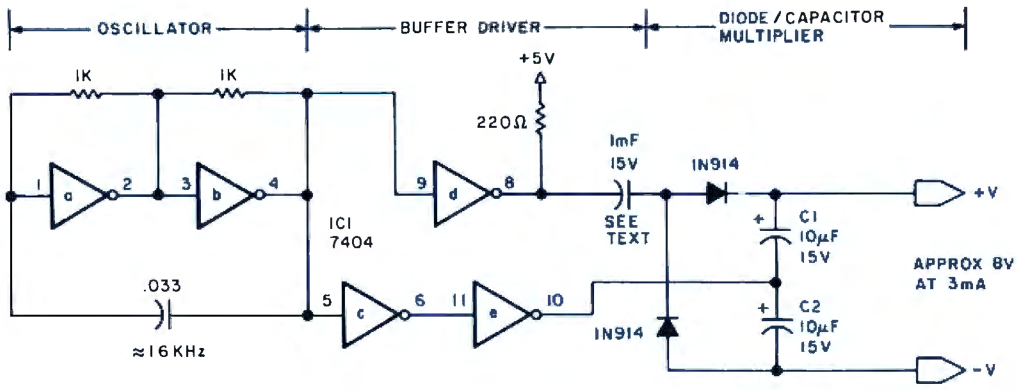

Figure 1: Typical DC to DC converter, a device used to convert one DC voltage into another. The oscillator section supplies a train of square waves to the buffer drivers. On the first half cycle, capacitor C1 is charged to approximately 4 V, and on the second half cycle, C2 is charged to −4 V. The voltage across the two capacitors is twice the input voltage, or approximately 8 V (open circuit). The 1 mF capacitor between IC1d and the two diodes isolates the circuit so that the 8 V can be referenced to ground.

integrated circuits and require only 50 mA, or if the interface is designed with CMOS circuitry, the current requirement could be 5 mA or less. While the 60 Hz transformer design may be more than adequate, the volume and weight of the low frequency magnetics is bulky and may not fit easily within the present enclosure.

The DC to DC Converter

In an application that requires higher voltage at low current, the DC to DC converter is the natural choice for the designer. As its name implies, it converts one DC voltage to another, usually a higher one. All DC to DC converters incorporate oscillator sections to provide AC either to drive transformers or to drive diode-capacitor voltage multipliers. The converters operate at high frequencies to reduce transformer weight. We'll explore the particulars later.

A DC to DC converter need not be low power, but the designs and applications presented here are specifically for low current and limited space applications. The majority of the circuits occupy less than 2 square inches (12.9 square cm).

A DC to DC converter draws its power from some major power bus, such as a +5 V or +12 V computer supply, and converts this source voltage to a higher level of either the same or reversed polarity. The simplest configuration is shown in figure 1. IC1a and IC1b form the oscillator which is common to all DC to DC converters. IC1c, IC1d and IC1e are buffers with the outputs of IC1d and IC1e 180 degrees out of phase,

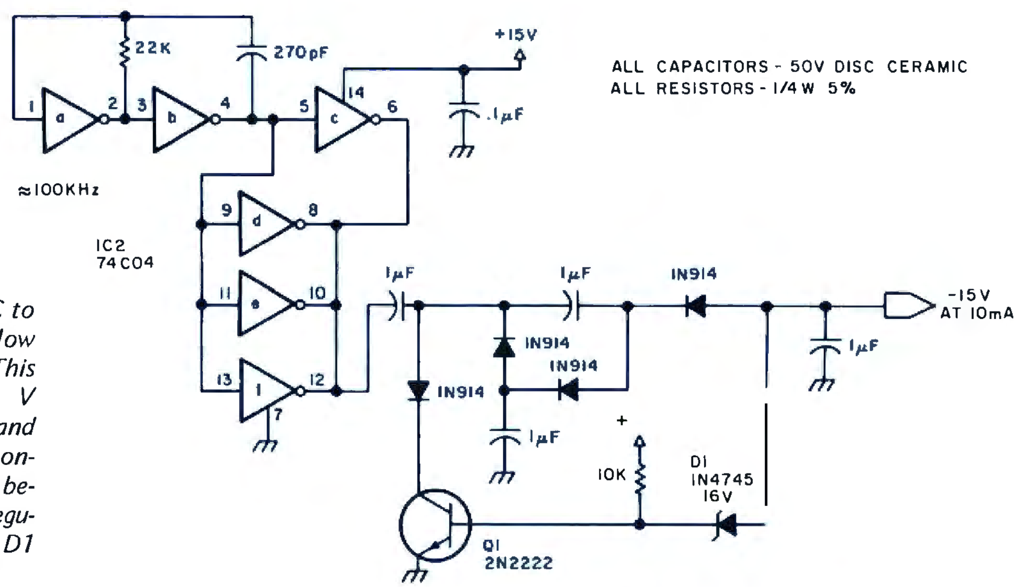

Figure 2: A CMOS DC to DC converter used for low current applications. This circuit produces −15 V from a +15 V source and provides a relatively constant output voltage because of the shunt regulator formed by diodes D1 and Q1.

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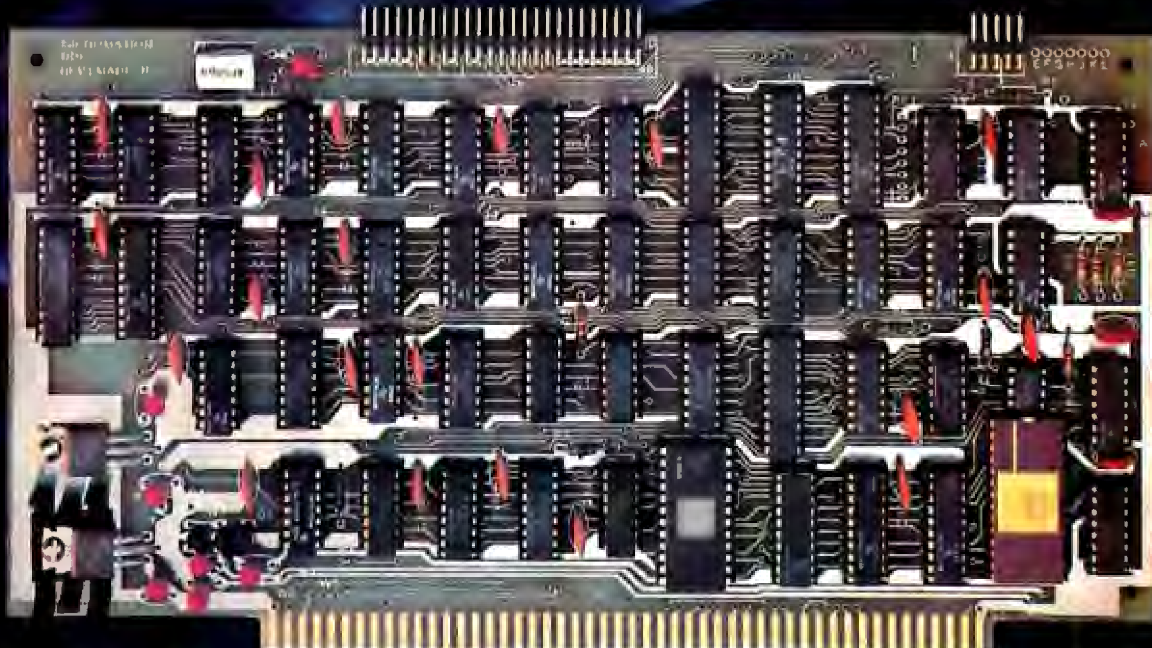

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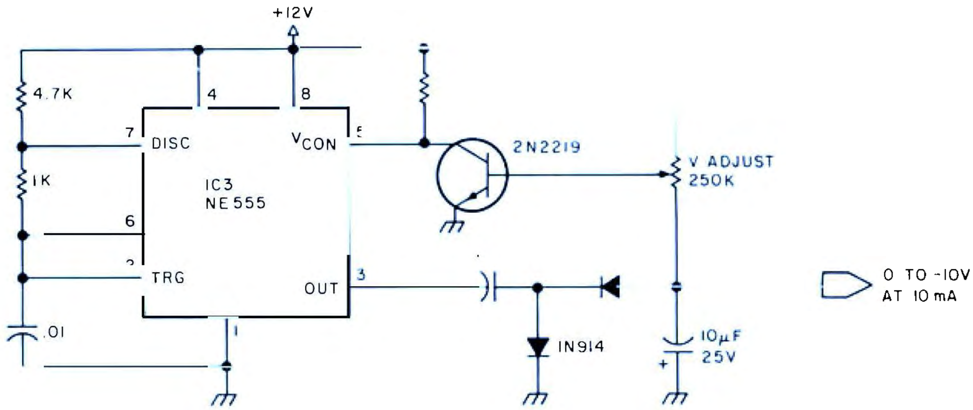

Figure 3: A variable output DC to DC converter capable of producing 0 to −10 V.

simulating a pseudo AC signal to the voltage multiplier. During the first half cycle, the capacitor, C1, is charged to approximately 4 V, and during the second half cycle, C2 is oppositely charged. The voltage across the two capacitors is twice the input voltage, or approximately 8 V (open circuit). If this circuit were not isolated from the drivers (IC1d and IC1e), neither +V nor −V line can be grounded or the multiplier section will be shorted out. The 1 mF 15 V capacitor between pin 8 and the junction of the two IN914 diodes provides isolation and allows the −V lead to be grounded. The output is then approximately 8 V, referenced to ground.

Type	Function	+5 V	−5 V	−12 V	+12 V
Ay-5-1013A	UART	20 mA		18 mA	
2708	1 K x 8 EROM	10 mA	45 mA		65 mA
2716 (Intel)	2 K x 8 EROM	100 mA			
2716 (TI)	2 K x 8 EROM	22 mA		12 mA	45 mA
MC1408L8	8 bit digital to analog converter	8 mA		20 mA	
LM301	op amp			3 mA	3 mA
LM741	op amp			2.8 mA	2.8 mA

Table 1: Worst case current requirements for a variety of integrated circuits.

Inverting Supplies

Most often DC to DC supplies are used where a negative voltage is required to power a bipolar linear interface or a dual supply large scale integrated circuit such as a keyboard encoder.

Figures 2 and 3 are examples of converters which would be suitable for these low current applications. Figure 2 produces −15 V from a +15 V source and provides a relatively constant output voltage because of the shunt regulator formed by the diode, D1, and the transistor, Q1. Changing the zener diode, D1, to 13 V makes the output −12 V instead of −15 V. The circuit outlined in figure 3 uses the voltage control input of an NE555 timer circuit to produce a variable output of 0 to −10 V.

Dual Voltage Converters

In most cases single voltage converters use diode steering and charged capacitor voltage multiplication. Transformers or other inductive devices must be incorporated if dual outputs are a requirement. Figure 4 is a very simple ±15 V converter which is powered from a +5 V supply.

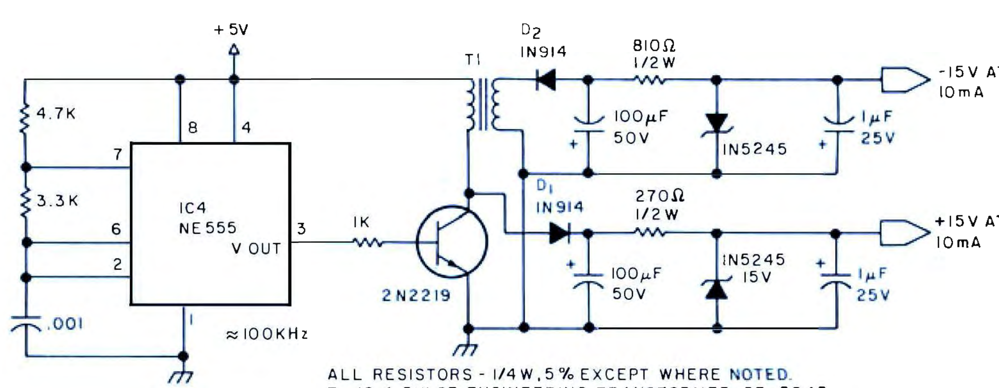

Figure 4: Low current dual voltage output DC to DC converter which supplies −15 and −15 V from a +5 V input.

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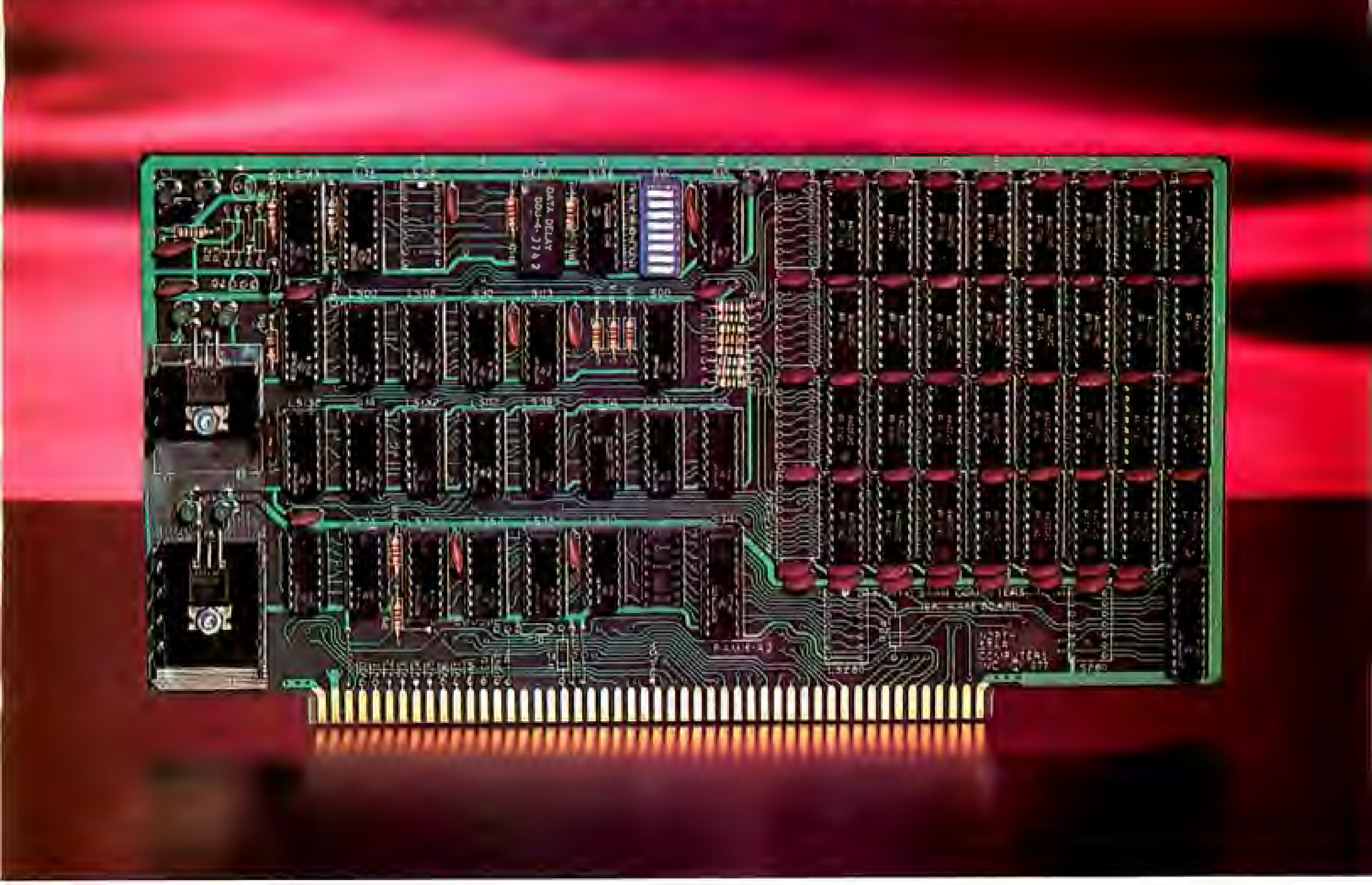

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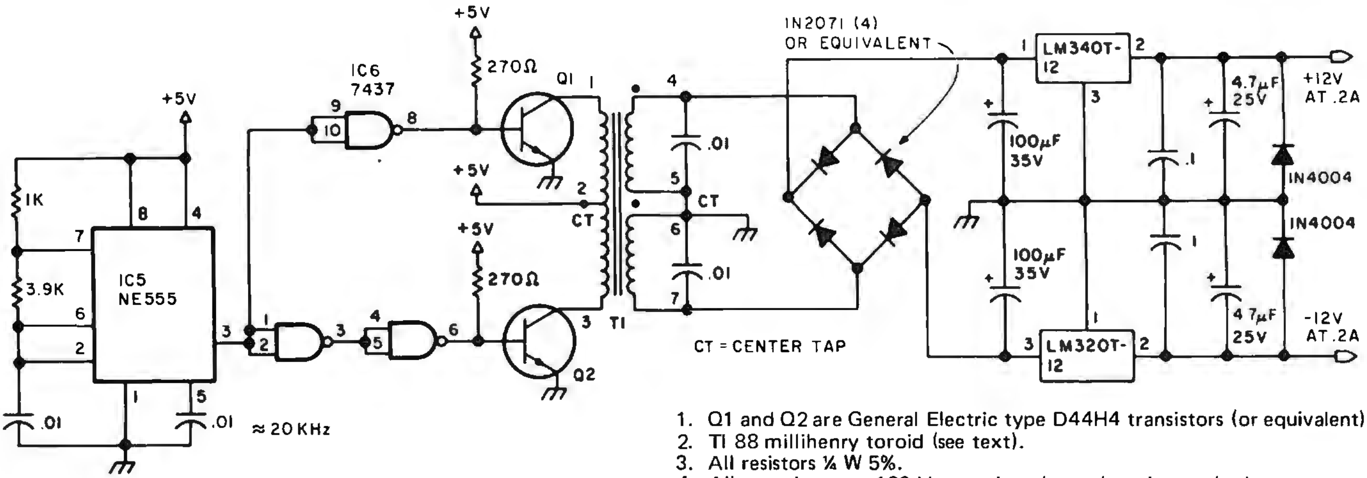
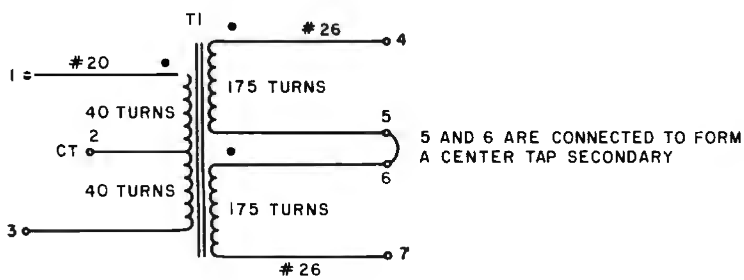


1. Q1 and Q2 are General Electric type D44H4 transistors (or equivalent).
2. TI 88 millihenry toroid (see text).
3. All resistors ¼ W 5%.
4. All capacitors are 100 V ceramic unless otherwise marked.

Figure 5a: 5 W DC to DC converter pictured in photo 1, which produces 0.2 A at +12 and −12 V from a 5 V source. See figure 5b for details of winding a toroidal transformer for this circuit.



1. Use enamel or Fomvar coated wire for each winding.
2. Be careful when winding not to scratch protective insulation.
3. Primary consists of 80 turns of #20 wire with center tap.
4. Secondaries can be wound as two #26 wire, 175 turn windings or as a single 350 turn winding with center tap.
5. For toroid source see text.
6. Use sandpaper or similar material to remove insulation from terminal wires before soldering.

Figure 5b: Toroid winding details for the custom transformer used in the circuit of figure 5a (see photos 2 thru 5).

Photo 2: Surplus 88 millihenry toroidal transformer rewound with two secondaries of 175 turns of #26 wire each (after first unwinding the existing two windings of approximately 350 turns each). The unit is used in the circuit of figure 5a.

Number	Type	+5 V	Gnd
IC1	7404	14	7
IC2	74C04	14	7
IC3	555	8	1
IC4	555	8	1
IC5	555	8	1
IC6	7437	14	7

Table 2: Power wiring table for figures 1 thru 5.

A 100 kHz oscillator switches a transistor on and off, inducing a current into the primary of transformer, T1. The voltage produced at the secondary is rectified and regulated to −15 V.

As with all inductive devices which are pulsed, a high voltage spike is reflected back to the collector of the transistor. Rather than shunting this voltage, as would be the case when we put a diode across a coil, D1 routes this spike to a filter and regulator combination to provide a +15 V output.

Building a DC to DC Converter

One of the first things to determine after deciding to use a DC to DC converter in your system is just how much current it must provide. Table 1 lists the typical voltages and operating current requirements (worst case) of a sampling of devices.

It should be apparent from this listing that EROMs are power-hungry devices and will use more than the 10 mA that the converters discussed thus far can supply. For this reason the unit described in figure 5 is designed to produce a full 200 mA at ±12 V.

This design uses a push/pull inverter technique to create AC which drives transformer, T1. T1 is a toroid transformer and

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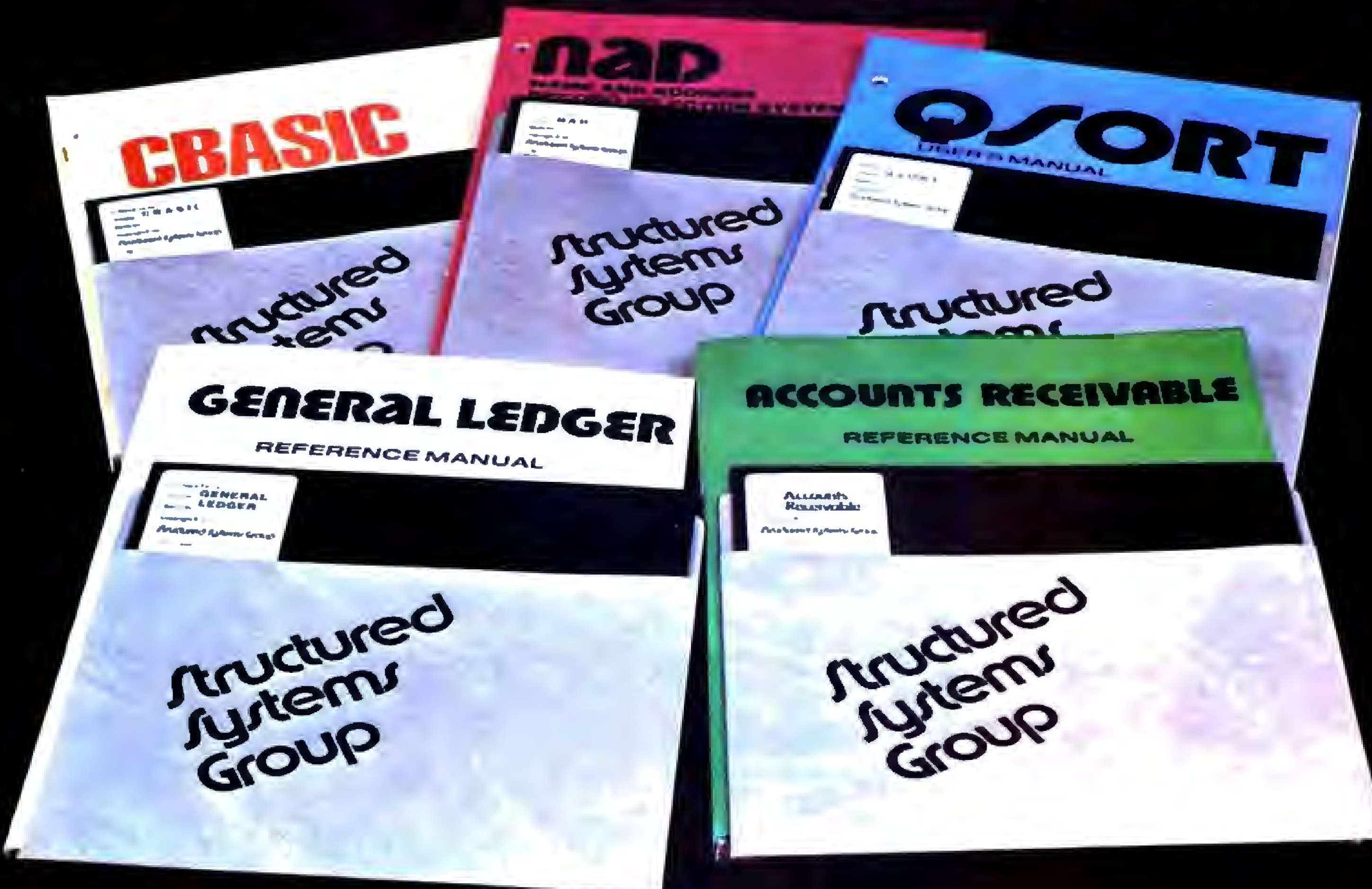

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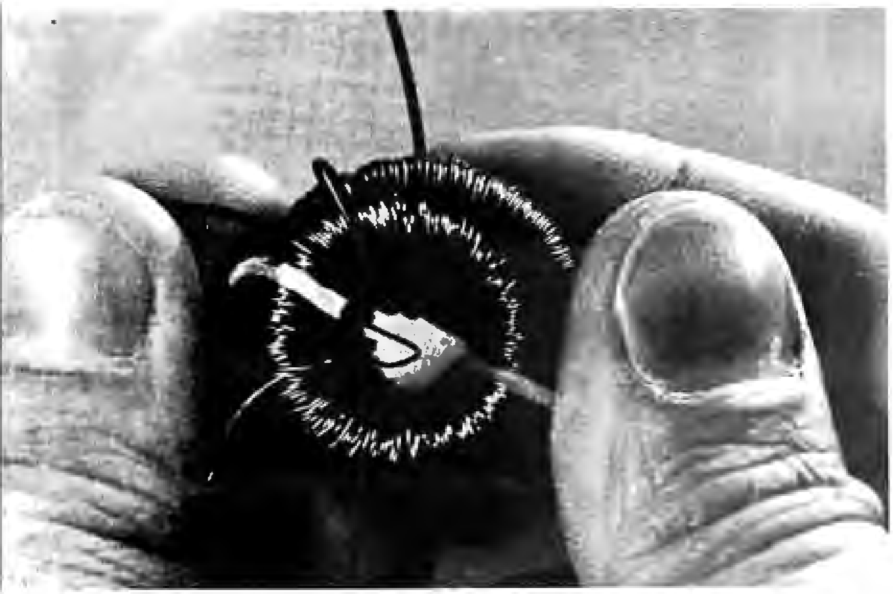

its doughnut shape is quite unlike the more common rectangular filament transformers. The shape and style of the toroid are specifically designed for high frequency operation, which is the main attribute of this inverter design. Heavy magnetic cores are necessary only for low frequencies such as 60 Hz. Since this converter's switching speed is 20 kHz, relatively little magnetic material is necessary, and high power output can be obtained.

The toroid in this design is a surplus 88 millihenry toroid, frequently advertised in the amateur radio magazines. A source I

Photo 3: Adding the primary winding, step 1: wind 40 turns of # 20 wire evenly around the toroid.

Photo 4: Adding the primary winding, step 2: make a loop for the center tap and continue with 40 additional turns.

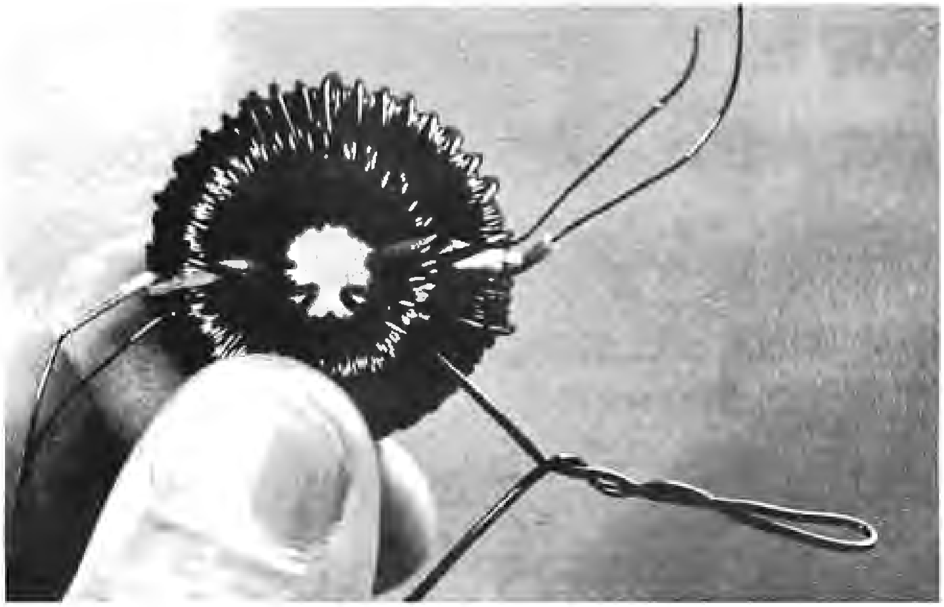

Photo 5: The completed transformer. The ends of all enameled wires should be cleaned of insulation before soldering.

have found is: M Weinschenker, POB 353, Irwin PA 15642. Order 88 millihenry unpotted toroids. The price is five for \$2.95 plus \$1 postage.

There are two ways to wind this toroid. Since it presently contains two windings of approximately 350 turns each, adding a primary sounds most logical. In reality though, 180 turns of #20 wire couldn't possibly fit in the remaining space, and the number of windings seems to vary from source to source. To obtain a properly wound toroid, it is best to first completely unwind the toroid and then rewind two 175 turn secondaries. The rewound toroid looks like photo 2. Since inductors exhibit an output polarity that is important when tying two secondaries in series, it is advisable to mark the starting lead on each coil and wind each in the same direction. It is not catastrophic if you don't. Polarity can be determined empirically later.

The primary is wound with #20 wire over the two secondaries as in photo 3, and should be distributed evenly around the toroid. When 40 turns have been wound, make a loop in the wire so that it will stick out (as shown in photo 4) and then continue winding the next 40 turns in the same direction. The complete toroid should look like photo 5.

The design outlined in figure 5a is a DC inverter. The NE555 20 kHz oscillator sources the high current 7437 buffers which are necessary to drive the push/pull transistor combination of Q1 and Q2. The continuous on/off action of the transistors produces an alternating current of 20 kHz in the primary winding of the toroid. This in turn induces a voltage proportional to the ratio of the primary to secondary turns, times the primary input voltage into the secondary winding. With approximately 4 V into the primary (taking into account the collector to emitter voltage drop, V_{CE}, transistors Q1 and Q2), 18 to 20 V should be present on each secondary.

The output of the toroid is treated as it would be in a traditional DC regulator design. The two secondaries are connected in series (terminals 5 and 6 connected) to produce 45 V between terminals 4 and 7. If a low voltage is obtained instead of 45 V, then the secondaries are out of phase and the terminals of one of the coils should be reversed. The two terminals which are connected at this point are the center tap and should be grounded.

Four diodes and two capacitors function as the full wave rectifier and filter input to a pair of 3 terminal voltage regulators. The result is a well-regulated + and −12 V supply with output current in excess of 200 mA on each. Overall conversion efficiency is better than 50%.

One note to keep in mind when testing this device: since the output is 5 W with 50% efficiency, the continuous input current to the converter will be approximately 2 A (at 5 V). Peak current will be higher at each clock transition. Use a supply with sufficient current capabilities or it will degrade the performance of the converter and possibly not even work.

In next month's BYTE: build an inexpensive infrared detection system.■

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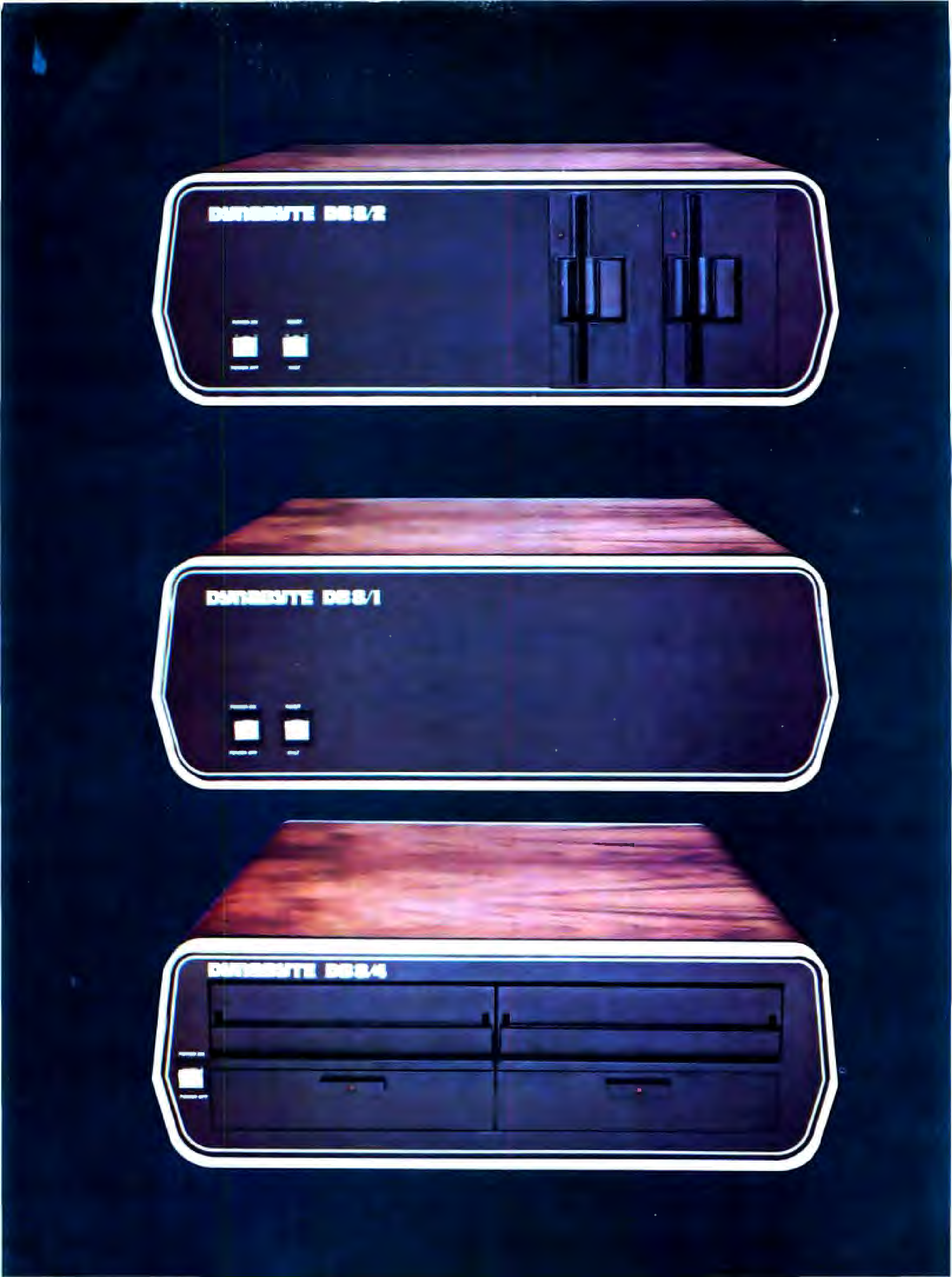
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A "Tiny" Pascal Compiler

Part 2: The P-Compiler

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Urbana IL 61801

Herbert Yuen
POB 2591 Station A
Champaign IL 61820

When Niklaus Wirth introduced Pascal in 1971, one of the design objectives was to allow efficient program compilation. As far as we know, all existing Pascal compilers use the one pass compilation technique.

Newcomers to Pascal sometimes criticize features of the language such as declaring variables before use, and having constant and type declarations precede variable declarations. But such features are necessary to make a one pass compiler work (aside from the fact that it is also good programming practice to declare identifiers before use). Compared with multipass compilers, the job of writing a one pass compiler is relatively simple, since there is no need to store the program in its intermediate form.

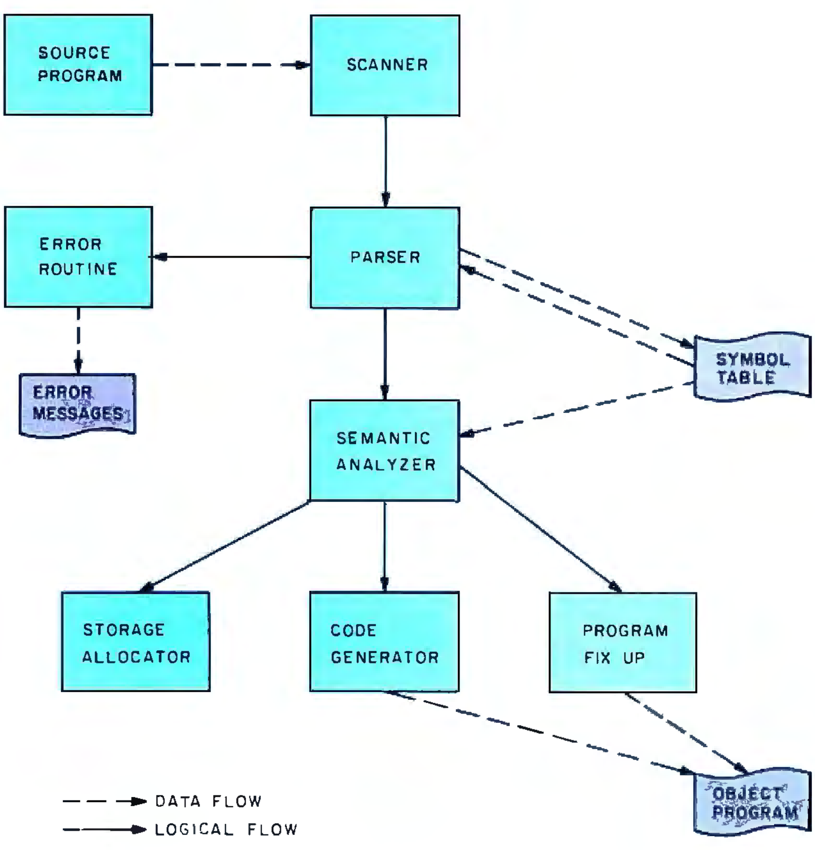

Figure 1: Logical arrangement and interconnections of the p-compiler modules.

Figure 1 shows the structure of our one pass Pascal compiler. The main portion is made up of the scanner, syntax analyzer, semantic analyzer and code generator. A brief overview of these functional portions of the compiler follows. Detailed descriptions will be given later.

The syntax analyzer is commonly called the *parser*. Its main function is to detect syntactical errors in the source program. The smallest unit of the source program that the parser looks at is called a *token*. For instance, the reserved word while, the symbol :=, or the identifier *idname* would be tokens. The main job of the scanner is to read the source program and output a token when needed by the parser. Irrelevant information such as blanks, comments and line boundaries are ignored.

To further simplify the work of the parser, the values of numeric constants are also evaluated by the scanner. The parser then parses the program according to the rules laid down by the syntax diagrams which were described in part 1 ("A Tiny Pascal Compiler," September 1978 BYTE, page 58) and generates error messages if illegal constructs are found. Identifier names are entered into a symbol table as they are declared. The symbol table is consulted by the parser as well as the semantic analyzer. After a Pascal construct is recognized, its meaning is analyzed by the semantic analyzer and appropriate p-codes are generated. Occasionally, there are forward references whose addresses cannot be determined at the time the codes are generated, but have to be resolved at a later time. Thus updates to the object program have to be done at the appropriate time.

This may sound complicated, but in fact a one pass compiler is actually the simplest compiler imaginable. The technique used by our parser is usually referred to as *top-down* parsing or goal oriented parsing. The top-down parsing algorithm assumes a general goal at the beginning. This goal is then broken down into one or more subgoals, depending on input strings and the rules in the syntax diagrams. The subgoals are realized by breaking them down into finer subgoals.

This is usually not a very efficient algorithm if backups are needed. The need for backups occurs if at some point we choose one subgoal from several others and find

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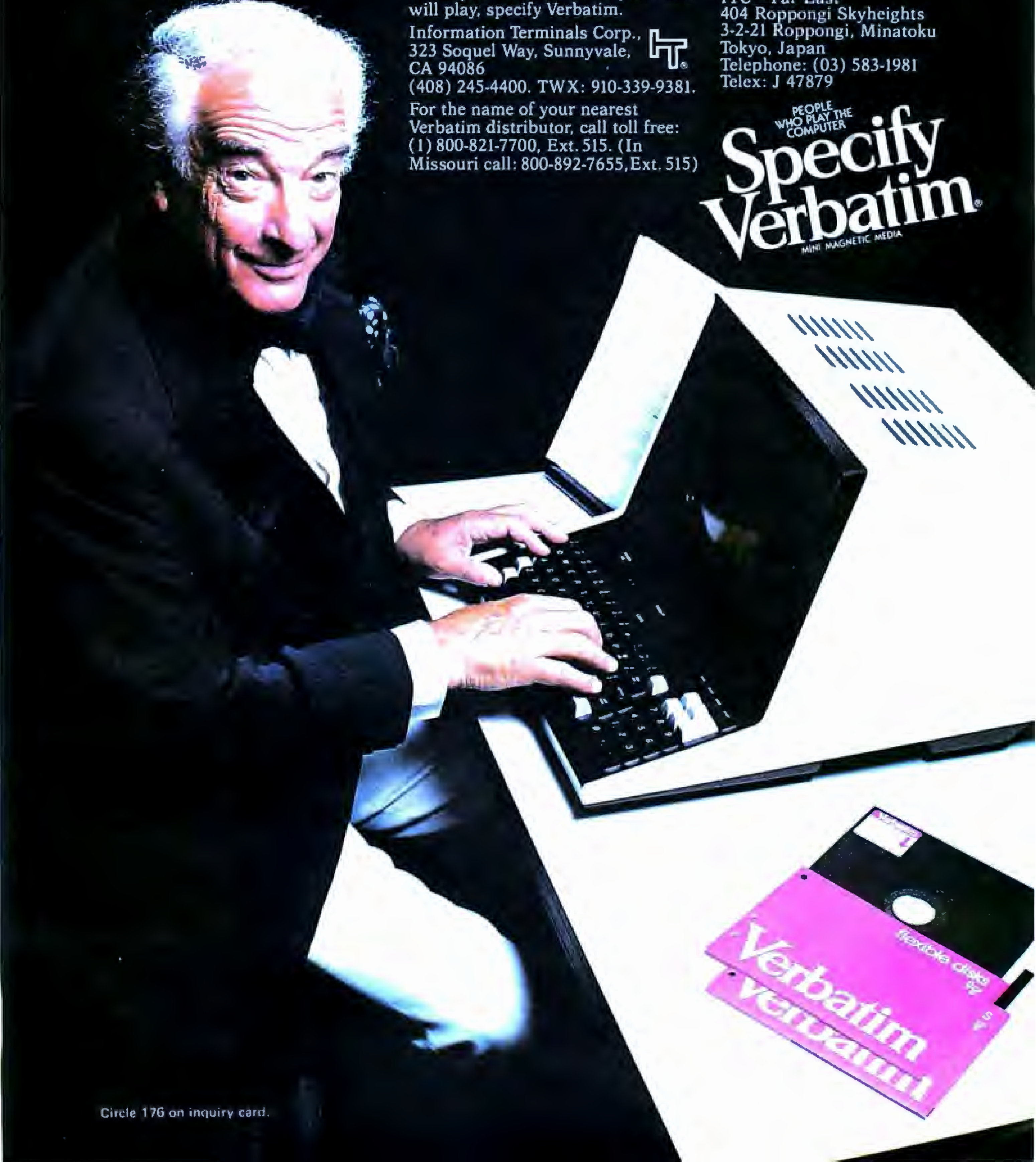

Circle 176 on inquiry card.

Listing 1: BASIC version of the p-compiler. This program takes the Pascal program and compiles it into p-code. The term p-code stands for pseudocode, an assembler language code for a hypothetical computer which can be converted into an existing assembler language. Listing continues thru page 48.

```
10REM PASCAL SUBSET COMPILER FOR P-MACHINE
20REM BY KIN-MAN CHUNG
30REM 1/78. LAST VERSION 4/78.
40 N0=32\REM # OF RESERVED WORDS
50 T0=50\REM SYM TABLE SIZE
60 N1=32767\REM LARGEST INT
70 N2=8\REM IDENT LEN
80 DIM W0$(5*N0)\REM RESERVED WORDS
90 DIM T$(T0*N2)\REM SYMBOL TABLE
100 DIM T0$(T0)\REM KIND OF IDENT IN SYM TAB\C,V,P
110 DIM L$(64)\REM LINE BUFFER
120 DIM A$(N2),B$(5)
130 DIM S(100),S$(100)\REM STACKS
140 DIM T1(T0)\REM LEVEL OF ID IN SYM TBL
150 DIM T2(T0)\REM VAL(FOR CONST) OR ADR(FOR INT)OF ID IN S.T
160 DIM T3(T0)\REM ARRAY DIM OR# OF PROC PARAMETERS
170 W0$(1,40)="AND  ARRAYBEGINCALL CASE CONSTDIV  DO   "
180 W0$(41,80)="DOWNTELSE END  FOR  FUNC IF   INTEGMEM  "
190 W0$(81,120)="MOD  NOT  OF   OR   PROC READ REPEASHL  "
200 W0$(121,160)="SHR  THEN TO   TYPE UNTILVAR  WHILEWRITE"
210 DIM M$(27),C$(80)
220 M$="LITOPRLODSTOCALINTJMPJPCCSP"\REM P-CODE MNEMONICS
230 P8=1
240 P7=0\P9=P7\REM START CODE=0000
250 !"P-CODES STARTS AT 0000"
260 Q9=4096*2\REM LAST USABLE MEM
270 F5=-1
280 INPUT "WANT CODE PRINTED?",Y$
290 IF Y$="Y" THEN Y9=0 ELSE Y9=1
300 X$=" "\GOSUB 1240\REM GET A TOKEN
310 GOSUB 5340\REM BLOCK
320 Z=FNE1(".",9)
330 FILL P9,255\FILL P9+1,255\REM FILL IN EOF MARK
340 INPUT"INTERPRET(I), OR TRANSLATE(T)?",Y$
350 IF Y$="" THEN END
360 IF Y$="I" THEN CHAIN "INTERP"
370 IF Y$="T" THEN CHAIN "TRANS"
380 END
390REM **********
400REM ERROR ROUTINES
410REM ***
420REM FNE1..IF CURRENT TOKEN<>K$ THEN ERROR #E
430 DEF FNE1(K$,E)
440 IF S0$<>K$ THEN Z=FNE(E)
450 RETURN 0
460 FNEND
470REM ***
480REM FNE2..IF NEXT TOKEN<>K$ THEN ERROR #E
490 DEF FNE2(K$,E)
500 GOSUB 1240
510 IF S0$<>K$ THEN Z=FNE(E)
520 RETURN 0
530 FNEND
540REM ***
550REM PRINT ERROR MSG
560 DEF FNE(E9)
570 !TAB(C0+4),"↑",E9
580 GOSUB 610
590 STOP
600 RETURN 0\FNEND
610REM ERROR MSGS
620 ON INT((E9-1)/5)+1 GOTO 630,640,650,660,670,680,690,700
630 ON E9 GOTO 710,720,730,740,750
640 ON E9-5 GOTO 990,990,990,760,770
650 ON E9-10 GOTO 780,790,800,990,990
660 ON E9-15 GOTO 810,820,830,840,850
670 ON E9-20 GOTO 860,870,880,990,890
680 ON E9-25 GOTO 900,910,920,990,930
690 ON E9-30 GOTO 940,990,950,960,970
700 ON E9-35 GOTO 980
710 !"MEM FULL"\RETURN
720 !"CONST EXPECTED"\RETURN
730 !"'=' EXPECTED"\RETURN
740 !"IDENTIFIER EXPECTED"\RETURN
750 !"';' OR ':' MISSING"\RETURN
760 !"'.' EXPECTED"\RETURN
770 !"';' MISSING"\RETURN
780 !"UNDECLARED IDENT"\RETURN
790 !"ILLEGAL IDENT"\RETURN
800 !"':=' EXPECTED"\RETURN
810 !"'THEN' EXPECTED"\RETURN
820 !"';' OR 'END' EXPECTED"\RETURN
830 !"'DO' EXPEXTED"\RETURN
840 !"INCORRECT SYMBOL"\RETURN
850 !"RELATIONAL OPERATOR EXPECTED"\RETURN
860 !"USE OF PROC IDENT IN EXPR"\RETURN
870 !"')' EXPECTED"\RETURN
880 !"ILLEGAL FACTOR"\RETURN
```

after some processing that we have made the wrong choice. We would then have to undo what had been done by the wrong choice and back up to the point where we could try other alternatives. This is usually a messy business and involves a lot of bookkeeping. Fortunately, in the parsing of Pascal, no backup is necessary. A keyword is present at each decision point, and it determines what subgoal we should choose. An example will make this clear.

Suppose our goal is to recognize a *statement*. A statement can be a number of basic constructs: it can be an assignment statement, an if statement, a case statement or any other construct defined by the syntax diagram. The Pascal grammar is so designed that we know which type of statement we should choose by just looking at the next token. If the token is if, then we know it is going to be an if statement; if the token is case, it is going to be a case statement, etc. There would seem to be a problem if the token is an identifier, since the statement can be the beginning of an assignment statement or a procedure call. But this can be easily resolved by consulting the symbol table, where we also keep the attributes (data types, addresses, etc) of the identifiers. This is one of the reasons why identifiers and procedures must be declared before use: it makes compiler writing easier.

A top-down parser without backup can be implemented by using a technique called *recursive descent*. Such a parser uses a recursive procedure for each nonterminal in the syntax diagrams. A call is made to this procedure whenever a parse for such

Line Number	Remark
400	Error routines — FNE, FNE1, FNE2
1030	Get a character
1090	Input a line
1240	Get a token
1950	Enter entry into symbol table
2060	Search symbol table
2170	Constant declaration
2240	Get constant
2340	Variable declaration
2380	Simple expression
2610	Term
2850	Factor
3290	Expression
3490	Statement
5340	Block
6120	Push numeric
6150	Pop numeric
6180	Push string
6240	Pop string
6310	Code Generation — FNG
6520	Fixup forward references

Table 1: For easy reference the main subroutines of the p-compiler are listed here along with remarks regarding their uses.


signetics
HELLO
INSTRUCTOR 50
The Instructor 50
Side 1
The Instructor 50
Side 2

```
890 !"'BEGIN' EXPECTED"\RETURN
900 !"'OF' EXPECTED"\RETURN
910 !"ILLEGAL HEX CONST"\RETURN
920 !"'TO' OR 'DOWNTO' EXPECTED"\RETURN
930 !"NUMBER OUT OF RANGE"\RETURN
940 !"'(' EXPECTED"\RETURN
950 !"'[' EXPECTED"\RETURN
960 !"']' EXPECTED"\RETURN
970 !"PARAMETERS MISMATCHED"\RETURN
980 !"DATA TYPE NOT RECOGNIZED"\RETURN
990 !"BUG"\RETURN
1000REM ******************
1010REM SCANNER
1020REM ******************
1030REM GETCHAR
1040 IF C0<L0 THEN 1060
1050 GOSUB 1090\GOTO 1040
1060 C0=C0+1\X$=L$(C0,C0)
1070 RETURN
1080REM **********
1090REM INPUT A LINE
1100 !%4I,C1," ",
1110 IF F5<0 THEN INPUT L$ ELSE 1160
1120 IF L$="" THEN 1100
1130 IF L$(1,1)="$" THEN 1210\REM MACRO FILE?
1140 L$=L$+" "\C0=0
1150 L0=LEN(L$)\RETURN
1160 IF TYP(F5)<>0 THEN 1190\REM EOF IF TYP=0
1170 CLOSE #F5\F5=F5-1\REM RETURN TO LAST ACTIVE FILE
1180 GOTO 1110
1190 READ #F5,L$\!L$
1200 GOTO 1130
1210 F5=F5+1\OPEN #F5,L$(2,LEN(L$))
1220 GOTO 1090
1230REM **********
1240REM GET A TOKEN
1250REM RETURN S0$=TOKEN, A$=STRING, N3=NUMERIC
1260 IF X$<>" " THEN 1280
1270 GOSUB 1030\GOTO 1260\REM FLUSH BLANKS
1280 IF X$<"A" THEN1460\REM INDENTIFIER?
1290 IF X$>"Z" THEN1460
1300 K=0\A$="                    "
1310 IF K>=N2 THEN 1330\REM ONLY 1ST N2 LETTERS ARE USED
1320 K=K+1\A$(K,K)=X$
1330 GOSUB 1030
1340 T=ASC(X$)
1350 IF T>47 AND T<58 OR T>64 AND T<91 THEN 1310\REM DGT OR LTTR
1360REM BIN SERACH FOR RES WORDS
1370 I=1\J=N0*5-4
1380 B$=A$
1390 K=INT((I+J)/10)*5+1
1400 Z$=W0$(K,K+4)
1410 IF B$<=Z$ THEN J=K-5
1420 IF B$>=Z$ THEN I=K+5
1430 IF I<=J THEN 1390
1440 IF I-5>J THEN S0$=B$ ELSE S0$="IDENT"
1450 RETURN
1460 Z$=""
1470 IF X$<"0" THEN 1580\REM AN INTEGER?
1480 IF X$>"9" THEN 1580
1490 S0$="NUM"
1500 Z$=Z$+X$
1510 GOSUB 1030
1520 IF ASC(X$)>=48 AND ASC(X$)<=57 THEN 1500
1530 N3=VAL(Z$)
1540 IF N3<=N1 THEN RETURN
1550 E9=30\GOSUB 550
1560 N3=N1\RETURN
1570REM CHECK FOR SPECIAL SYMBOL
1580 IF X$<>":" THEN 1640
1590 GOSUB 1030
1600 IF X$="=" THEN 1620
1610 S0$=":"\RETURN
1620 S0$=":="
1630 GOSUB 1030\RETURN
1640 IF X$<>"<" THEN 1710
1650 GOSUB 1030
1660 IF X$=">" THEN 1690
1670 IF X$="=" THEN 1700
1680 S0$="<"\RETURN
1690 S0$="<>"\GOSUB 1030\RETURN
1700 S0$="<="\GOSUB 1030\RETURN
1710 IF X$<>">" THEN 1750
1720 GOSUB 1030\S0$=">"
1730 IF X$<>"=" THEN RETURN
1740 S0$=">="\GOSUB 1030\RETURN
1750 IF X$<>"'" THEN 1790
1760 S0$="STR"\C$=""
1770 GOSUB 1030\IF X$="'" THEN 1030
1780 C$=C$+X$\GOTO 1770
1790 IF X$<>"(" THEN 1820\REM IGNORE COMMENTS
1800 GOSUB 1030\IF X$<>")" THEN 1800
1810 GOSUB 1030\GOTO 1240
1820 IF X$<>"%" THEN 1930\REM HEX CONSTANT
1830 GOSUB 1030\S0$="NUM"\N3=0
1840 FOR I=1 TO 4
```

a nonterminal is required. It is easy to see why such a scheme would work. The stacking mechanism of the run time procedures ensures that we get back to the correct position in the syntax diagram after completing the parse of the nonterminal.

If you look at the syntax diagrams carefully, you will see that diagrams for certain nonterminals actually contain the nonterminal itself, either immediately or after several expansions. In terms of compiler writing this means that the procedures corresponding to these nonterminals would call themselves recursively.

BASIC Recursive Subroutines

Most versions of BASIC do not adequately support recursive subroutine calls. In North Star BASIC, the multiline function call can be invoked recursively, in a limited fashion. This is because the function parameters are local within the function definition and are pushed onto a stack when making a call.

The surprising fact is that most BASICs do not forbid a recursive call if one is made. For instance, the following BASIC subroutine, which is an inefficient way of printing the first N integers in descending order, is probably permitted in most BASICs:

```
100 PRINT N
200 IF N=0 THEN RETURN
300 N=N−1
400 GOSUB 100
500 RETURN
```

The problem of doing recursive calls in BASIC is that of preserving the values of the identifiers in the subroutines. This can be done by using a stack. The values of the identifiers are pushed onto the stack before a recursive call, and popped out of the stack in the reverse order when returning from the call. In BASIC, the stack can be simulated by an array:

```
10 DIM S(100)
11 P=0
12 REM INITIALIZE STACK POINTER
.
.
.
1000REM PUSH X INTO STACK
1010 S(P)=X
1020 P=P+1
1030 RETURN
2000REM POP X FROM STACK
2010 P=P−1
2020 X=S(P)
2030 RETURN
```

```
1850 T=ASC(X$)
1860 IF T>=48 AND T<=57 THEN 1880
1870 IF T>=65 AND T<=70 THEN T=T-7 ELSE 1910
1880 T=T-48
1890 N3=N3*16+T\GOSUB 1030\NEXT
1900 RETURN
1910 IF I>1 THEN Z=FNE(27)
1920 S0$="%"\RETURN
1930 S0$=X$\GOTO 1030
1940REM **********
1950REM ENTER SYMBOL INTO TABLE
1960 T1=T1+1
1970 T$((T1-1)*N2+1,T1*N2)=A$
1980 T0$(T1,T1)=K$\REM STORE TYPE
1990 IF K$<>"C" THEN 2010
2000 T2(T1)=N3\RETURN\REM STORE VALUE
2010 T1(T1)=L1\REM STORE LEVEL OF IDENT
2020 IF K$<>"V" THEN RETURN
2030 IF NOT F9 THEN RETURN\REM SP WAS ALLOCATED FOR PROC PARS
2040 T2(T1)=D0\D0=D0+1\RETURN\REM STORE OFFSET
2050REM **********
2060REM FIND IDENT A$ IN T$,STARTING FROM T1 AND UP
2070REM RETURN POINTER TO TABLE IF FOUND, ELSE RETURN 0
2080 J=(T1-1)*N2+1
2090 FOR I=T1 TO 1 STEP -1
2100 IF A$=T$(J,J+N2-1) THEN EXIT 2130
2110 J=J-N2\NEXT
2120 I=0
2130 RETURN
2140REM *******************
2150REM PARSER AND CODER
2160REM *******************
2170REM CONSTANT DECLARATION
2180 Z=FNE1("IDENT",4)
2190 Z=FNE2("=",3)
2200 GOSUB 1240\GOSUB 2240
2210 K$="C"\GOSUB 1950
2220 GOTO 1240
2230REM **********
2240REM CONSTANT
2250 IF S0$="NUM" THEN RETURN
2260 IF S0$="IDENT" THEN 2290\REM CONST?
2270 Z=FNE1("STR",2)
2280 N3=ASC(C$)\RETURN\REM TAKE 1ST CHAR
2290 GOSUB 2060\IF I=0 THEN FNE(2)
2300 IF T0$(I,I)<>"C" THEN FNE(2)
2310 N3=T2(I)\RETURN
2320 GOTO 1240
2330REM **********
2340REM VARIABLE DECLARATION
2350 Z=FNE1("IDENT",4)
2360 K$="V"\GOSUB 1950\GOTO 1240
2370REM **********
2380REM SIMPLE EXPRESSION
2390 IF S0$="+" THEN 2420
2400 IF S0$<>"-" THEN 2590
2410 Y$=S0$\GOSUB 6180
2420 GOSUB 1240
2430 GOSUB 2610
2440 GOSUB 6240
2450 IF Y$="-" THEN Z=FNG(1,0,1)
2460 IF S0$="+" THEN 2500
2470 IF S0$="-" THEN 2500
2480 IF S0$="OR   " THEN 2500
2490 RETURN
2500 Y$=S0$\GOSUB 6180
2510 GOSUB 1240
2520 GOSUB 2610
2530 GOSUB 6240
2540 IF Y$="-" THEN 2570
2550 IF Y$="+" THEN 2580
2560 Z=FNG(1,0,14)\GOTO 2460
2570 Z=FNG(1,0,3)\GOTO 2460
2580 Z=FNG(1,0,2)\GOTO 2460
2590 GOSUB 2610\GOTO 2460
2600REM **********
2610REM TERM
2620 GOSUB 2850
2630 IF S0$="*" THEN 2700
2640 IF S0$="DIV  " THEN 2700
2650 IF S0$="AND  " THEN 2700
2660 IF S0$="MOD  " THEN 2700
2670 IF S0$="SHL  " THEN 2700
2680 IF S0$="SHR  " THEN 2700
2690 RETURN
2700 Y$=S0$\GOSUB 6180\REM PUSH
2710 GOSUB 1240\GOSUB 2850
2720 GOSUB 6240
2730 IF Y$="DIV  " THEN 2790
2740 IF Y$="MUL  " THEN 2800
2750 IF Y$="*" THEN 2810
2760 IF Y$="SHL  " THEN 2820
2770 IF Y$="SHR  " THEN 2830
2780 Z=FNG(1,0,15)\GOTO 2630\REM "AND"
2790 Z=FNG(1,0,5)\GOTO 2630
2800 Z=FNG(1,0,[illegible])\GOTO 2630
```

One important part missing from our compiler is the ability to recover from errors. Of course all syntactical errors are caught by our compiler and somewhat meaningful messages are printed to indicate errors. However, if an error is found, the compiler is aborted prematurely and will not resume compiling. Such a compiler is, of course, not acceptable in practice. But with the understanding that this compiler will be used as a bootstrap compiler, as discussed in part 1, it is tolerable. A compiler with simple error recoveries would not be particularly difficult to implement but would involve a lot of programming codes and processing time. We hesitate to add things to an already big and slow program.

It is generally difficult to implement a compiler with sophisticated error recovery features. Such a compiler would not only detect errors, but would also try to repair the damages caused by such errors. The compiler has to make some assumptions about the nature of the errors and the intention of the author. This is usually difficult.

If our concern is solely that of locating all errors in a single parse of the source program, there are simple ways of doing it. Upon detecting an error, the compiler simply skips the input text until it can safely resume the compilation process. To do this the compiler looks for certain keywords or *stopping* symbols for hints to resume the parsing process. For instance, if we find an error while parsing a conditional expression, we skip the input tokens and search for symbols, such as =, > =, etc, and keywords such as then and do or perhaps begin. If we do this for all the parts of the language constructs, we will at least have a compiler that would resume compilation after an error is encountered in the hope of finding all syntactic errors in one pass, and which would give meaningful diagnostics for most errors.

To reduce the size of the program shown in listing 1, comments are kept to a minimum. Each module or subroutine is clearly identified. To facilitate easy reference, the important subroutines and variables are shown in table 1 and table 2, respectively.

Scanner and Symbol Table Management

Each time the p-compiler calls the scanner (line 1260, listing 1), the input text is scanned and a new token is produced. This is done by calling a subroutine (line 1040) that returns a character from the input string. Since the input/output (IO) routines are line oriented instead of character oriented, a line buffer (L$) is used to

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```
2810 Z=FNG(1,0,4)\GOTO 2630
2820 Z=FNG(1,0,17)\GOTO 2630
2830 Z=FNG(1,0,18)\GOTO 2630
2840REM **********
2850REM FACTOR
2860 IF S0$="IDENT" THEN 2940
2870 IF S0$="NUM" THEN 3060
2880 IF S0$="STR" THEN 3080
2890 IF S0$="(" THEN 3100
2900 IF S0$="MEM  " THEN 3140
2910 IF S0$="NOT  " THEN 3260
2920 Z=FNE(23)
2930REM *** IDENTIFIER
2940 GOSUB 2060
2950 IF I=0 THEN Z=FNE(11)
2960 IF T0$(I,I)="P" THEN Z=FNE(21)\REM PROC NAME
2970 IF T0$(I,I)<>"Y" THEN 3000
2980 Z=FNG(5,0,1)\REM FUNC
2990 I=I-1\GOTO 4290\REM T2(I)=ADD OF FUNC
3000 IF T0$(I,I)="A" THEN 3190\REM ARRAY
3010 IF T0$(I,I)<>"C" THEN 3030
3020 Z=FNG(0,0,T2(I))\GOTO 1240\REM CONST
3030 Z=FNG(2,L1-T1(I),T2(I))\REM ID
3040 GOTO 1240
3050REM *** NUMERIC CONST
3060 Z=FNG(0,0,N3)\GOTO 1240
3070REM *** STRNG CONST
3080 Z=FNG(0,0,ASC(C$))\GOTO 1240
3090REM *** PAREN EXPR
3100 GOSUB 1240\GOSUB 3290
3110 IF S0$=")" THEN 1240
3120 Z=FNE(22)\RETURN
3130REM *** READ MEMORY
3140 Z=FNE2("[",33)
3150 GOSUB 1240\GOSUB 3290
3160 Z=FNE1("]",34)
3170 GOSUB 1240
3180 Z=FNG(2,255,0)\RETURN
3190 X=I\GOSUB 6120
3200 Z=FNE2("[",33)
3210 GOSUB 1240\GOSUB 3290
3220 Z=FNE1("]",34)
3230 GOSUB 6150\Z=FNG(18,L1-T1(X),T2(X))
3240 GOTO 1240
3250REM *** NEGATE
3260 GOSUB 1240\GOSUB 2850
3270 Z=FNG(1,0,16)\RETURN
3280REM **********
3290REM EXPRESSION
3300 GOSUB 2390\REM SIMPLE EXP
3310 IF S0$="=" THEN 3380
3320 IF S0$="<>" THEN 3380
3330 IF S0$="<" THEN 3380
3340 IF S0$="<=" THEN 3380
3350 IF S0$=">" THEN 3380
3360 IF S0$=">=" THEN 3380
3370 RETURN
3380 Y$=S0$\GOSUB 6180\REM PUSH
3390 GOSUB 1240\GOSUB 2390
3400 GOSUB 6240\REM POP
3410 IF Y$="=" THEN Z=FNG(1,0,8)
3420 IF Y$="<>" THEN Z=FNG(1,0,9)
3430 IF Y$="<" THEN Z=FNG(1,0,10)
3440 IF Y$=">=" THEN Z=FNG(1,0,11)
3450 IF Y$=">" THEN Z=FNG(1,0,12)
3460 IF Y$="<=" THEN Z=FNG(1,0,13)
3470 RETURN
3480REM **********
3490REM STATEMEMT
3500 IF S0$="IDENT" THEN 3630
3510 IF S0$="IF   " THEN 4440
3520 IF S0$="FOR  " THEN 5170
3530 IF S0$="WHILE" THEN 4800
3540 IF S0$="CASE " THEN 4890
3550 IF S0$="REPEA" THEN 4730
3560 IF S0$="BEGIN" THEN 4590
3570 IF S0$="READ " THEN 4040
3580 IF S0$="WRITE" THEN 3870
3590 IF S0$="MEM  " THEN 4650
3600 IF S0$="CALL " THEN 4240
3610 RETURN
3620REM *** ASSIGNMNT
3630 GOSUB 2060
3640 IF I=0 THEN Z=FNE(11)
3650 IF T0$(I,I)="A" THEN 3700\REM ARRAY
3660 IF T0$(I,I)="V" THEN 3760\REM INT VAR
3670 IF T0$(I,I)="Y" THEN 3760\REM FUNC RETURN VALUE
3680 IF T0$(I,I)="P" THEN 4290\REM PROC CALL
3690 Z=FNE(12)
3700 X=I\GOSUB 6120\REM PUSH TBL ADD
3710 X=16\GOSUB 6120\REM INDEX ADD MODE
3720 Z=FNE2("[",33)
3730 GOSUB 1240\GOSUB 3290
3740 Z=FNE1("]",34)
3750 GOTO 3780
3760 X=I\GOSUB 6120
```

hold a line, and a counter (C0) is used to indicate the character just read. When the end of a line is reached, the line input routine (line 1100) is called to read in a new line.

In our compiler we also provide the capability of invoking or recalling a file of Pascal text from disk. This is initiated by a command that starts with a dollar sign (*$*) in the first column followed immediately by the name of the disk file to be inserted and compiled. Since North Star BASIC allows four disk files to be open at the same time, there can be four levels of file nesting. The variable F5 is used to indicate this level. If it is equal to −1, then input is taken from the keyboard. The initial input is from the keyboard. This feature is quite useful, since we can store procedures that are commonly used in a disk library, and have them recalled when needed.

Usually, the token that the scanner returns is a number that represents the token class the symbol is in. To make the program more readable, we use string variable S0$. Possible values returned by the scanner are: ; , :=, BEGIN, IDENT, and NUM. The last two tokens, which are tokens for identifiers and numbers, require some further information. A$ and N3 are also used to store the textual representation of the identifier and the value of the number, respectively.

The recognition of a valid token is a straightforward process and will not be detailed here. Since : and := are both valid tokens, the scanner, after seeing the : , must also look at the next character to determine the correct token. This can be done by using a one character look ahead. When the scanner is entered, a character is assumed to have been read, and upon exit from the scanner, a character beyond the current token is read.

Another problem that the scanner may have is that of recognizing reserved words. The reserved words are stored in a table in sorted order. When an identifier is found, it is compared with the entries in the table, by performing a binary search. If it is not in the table, it is assumed to be a user defined identifier.

In Pascal programs, identifiers are declared at the beginning of each procedure block. The scope of an identifier covers the entire block containing it (and any of the blocks inside that block). A simple symbol management scheme that reflects such scope rules makes use of a stack. When the compiler enters a procedure block, a segment of the stack is used to store identifiers for the block. If the procedure block contains another procedure block, then another

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```
3770 X=0\GOSUB 6120
3780 GOSUB 1240
3790 IF S0$=":=" THEN 3810
3800 Z=FNE(13)\GOTO 3820
3810 GOSUB 1240
3820 GOSUB 3290\GOSUB 6150
3830 K=X\GOSUB 6150
3840 Z=FNG(3+K,L1-T1(X),T2(X))
3850 RETURN
3860REM *** WRITE
3870 Z=FNE2("(",31)
3880 GOSUB 1240\IF S0$<>"STR" THEN 3950
3890 L=LEN(C$)\IF L>1 THEN 3910
3900 Z=FNG(0,0,ASC(C$))\Z=FNG(8,0,1)\GOTO 3940
3910 FOR I=1 TO L
3920 Z=FNG(0,0,ASC(C$(I,I)))\NEXT
3930 Z=FNG(0,0,L)\Z=FNG(8,0,8)
3940 GOSUB 1240\GOTO 4000
3950 GOSUB 3290\K=1
3960 IF S0$="#" THEN K=3\REM DEC
3970 IF S0$="%" THEN K=5\REM HEX
3980 IF K>1 THEN GOSUB 1240
3990 Z=FNG(8,0,K)
4000 IF S0$="," THEN 3880
4010 Z=FNE1(")",22)
4020 GOTO 1240
4030REM *** READ
4040 Z=FNE2("(",31)
4050 Z=FNE2("IDENT",4)
4060 GOSUB 2060\IF I=0 THEN Z=FNE(11)
4070 X=I\GOSUB 6120
4080 IF T0$(I,I)="A" THEN 4190
4090 IF T0$(I,I)="V" THEN L=0 ELSE Z=FNE(4)
4100 GOSUB 1240\K=0
4110 IF S0$="#" THEN K=2\REM DEC
4120 IF S0$="%" THEN K=4\REM HEX
4130 Z=FNG(8,0,K)
4140 IF K>0 THEN GOSUB 1240
4150 GOSUB 6150\Z=FNG(L+3,L1-T1(X),T2(X))
4160 IF S0$="," THEN 4050
4170 Z=FNE1(")",31)
4180 GOTO 1240
4190 Z=FNE2("[",33)
4200 GOSUB 1240\GOSUB 3290
4210 Z=FNE1("]",34)
4220 L=16\GOTO 4100
4230REM *** ABSOLUTE MEM CALL
4240 Z=FNE2("(",31)
4250 GOSUB 1240\GOSUB 3290
4260 Z=FNE1(")",22)
4270 Z=FNG(4,255,0)\GOTO 1240
4280REM *** PROC OR FUNC CALL
4290 K2=0\K3=I
4300 IF T3(I)=0 THEN 4400\REM NO PARAMETER
4310 Z=FNE2("(",31)
4320 X=K2\GOSUB 6120
4330 X=K3\GOSUB 6120
4340 GOSUB 1240\GOSUB 3290
4350 GOSUB 6150\K3=X
4360 GOSUB 6150\K2=X\K2=K2+1
4370 IF S0$="," THEN 4320
4380 IF K2<>T3(K3) THEN Z=FNE(35)
4390 Z=FNE1(")",22)
4400 Z=FNG(4,L1-T1(K3),T2(K3))
4410 IF K2 <>0 THEN Z=FNG(5,0,-K2)
4420 GOTO 1240
4430REM *** IF
4440 GOSUB 1240
4450 GOSUB 3290
4460 Z=FNE1("THEN ",16)
4470 GOSUB 1240
4480 X=C1\GOSUB 6120\REM FORWARD REF POINT
4490 Z=FNG(7,0,0)\REM JPC
4500 GOSUB 3490
4510 IF S0$<>"ELSE " THEN 6520
4520 GOSUB 6150\K=X
4530 X=C1\GOSUB 6120
4540 Z=FNG(6,0,0)\REM JMP
4550 X=K\GOSUB 6540\REM FIXUP FORWD REF
4560 GOSUB 1240\GOSUB 3490
4570 GOTO 6520
4580REM *** COMPOUND STTMNT
4590 GOSUB 1240
4600 GOSUB 3490
4610 IF S0$=";" THEN 4590
4620 IF S0$="END  " THEN 1240
4630 Z=FNE(17)\RETURN
4640REM *** WRITE MEM
4650 Z=FNE2("[",33)
4660 GOSUB 1240\GOSUB 3290
4670 IF S0$<>"]" THEN Z=FNE(34)
4680 Z=FNE2(":=",13)
4690 GOSUB 1240\GOSUB 3290
4700 Z=FNG(3,255,0)
4710 RETURN
4720REM *** REPEAT .. UNTIL
```

segment of the stack on top of the existing segments is used for identifiers of this block. After successful compilation of a procedure, its segment of the stack can be discarded, since there is no further use for this part of the symbol table. In this way, we can also eliminate possible interference with identifiers in some other blocks. We also see that since the block delimiting mechanism is hierarchical, use of stack is also appropriate. Figure 2 illustrates two-level block nesting.

Readers may have noticed the similarities between this symbol table stacking scheme and the run time storage allocation scheme discussed in part 1. Since the symbol table deals with a static structure, it is much simpler.

Within the segment of the symbol table for a procedure block, further data structures can be set up for storing the identifiers. We chose to use what we feel is the simplest method: store the identifiers sequentially, in their order of appearance. This means that search also has to be done sequentially. Since most procedures have only a small number of identifiers, this should work well in most cases. Other more sophisticated structures such as a balanced binary tree or hashed table are commonly used in larger compilers.

The symbol table also contains some information about the identifiers. The identifier type has to be kept with the symbol table. Specific information is needed

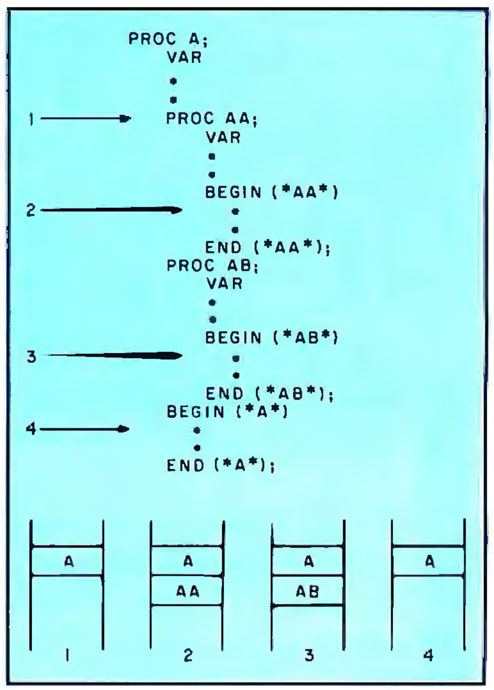

Figure 2: Example symbol table at various points of compilation.

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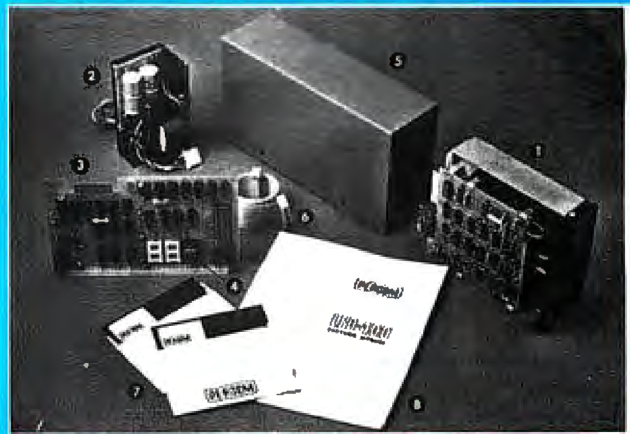

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```
4730 X=C1\GOSUB 6120
4740 GOSUB 1240\GOSUB 3490
4750 IF S0$=";" THEN 4740
4760 Z=FNE1("UNTIL",10)
4770 GOSUB 1240\GOSUB 3290
4780 GOSUB 6150\Z=FNG(7,0,X)\RETURN
4790REM *** WHILE .. DO
4800 GOSUB 1240\X=C1\GOSUB 6120
4810 GOSUB 3290\X=C1\GOSUB 6120
4820 Z=FNG(7,0,0)
4830 Z=FNE1("DO   ",18)
4840 GOSUB 1240\GOSUB 3490
4850 GOSUB 6150\K=X\GOSUB 6150
4860 Z=FNG(6,0,X)
4870 X=K\GOTO 6540
4880REM *** CASE .. OF
4890 GOSUB 1240\GOSUB 3290
4900 Z=FNE1("OF   ",25)
4910 I2=1\REM # OF CASE STATMNTS
4920 I1=0\REM # OF CASE LABELS
4930 GOSUB 1240\GOSUB 2240
4940 Z=FNG(1,0,21)\Z=FNG(0,0,N3)\Z=FNG(1,0,8)
4950 GOSUB 1240\IF S0$=":" THEN 4990
4960 Z=FNE1(",",5)
4970 X=C1\GOSUB 6120\Z=FNG(7,1,0)\REM A MATCH FOUND?
4980 I1=I1+1\GOTO 4930
4990 K=C1\Z=FNG(7,0,0)\REM GOTO NEXT CASE STMNT IF NO MATCH
5000 FOR I=1 TO I1\GOSUB 6520\NEXT\REM FIXUP FORWD REFS
5010 X=K\GOSUB 6120
5020 GOSUB 1240\X=I2\GOSUB 6120
5030 GOSUB 3490\GOSUB 6150\I2=X
5040 IF S0$="ELSE " THEN 5090
5050 IF S0$<>";" THEN 5130
5060 K=C1\Z=FNG(6,0,0)\REM EXIT AFTER A CASE STMNT
5070 GOSUB 6520
5080 X=K\GOSUB 6120\I2=I2+1\GOTO 4920
5090 K=C1\Z=FNG(6,0,0)\GOSUB 6520
5100 X=K\GOSUB 6120
5110 GOSUB 1240\X=I2\GOSUB 6120
5120 GOSUB 3490\GOSUB 6150\I2=X
5130 Z=FNE1("END  ",17)
5140 FOR I=1 TO I2\GOSUB 6520\NEXT\REM FIXUP FORWD REFS
5150 Z=FNG(5,0,-1)\GOTO 1240\REM POP VAL OF CASE EXP
5160REM *** FOR
5170 Z=FNE2("IDENT",4)
5180 GOSUB 3630\GOSUB 6120
5190 F9=1\IF S0$="TO   " THEN 5210\REM REMEMBER UP OR DOWN
5200 Z=FNE1("DOWNT",28)\F9=0
5210 GOSUB 1240\GOSUB 3290
5220 GOSUB 6150\K=X\X=C1\GOSUB 6120
5230 Z=FNG(1,0,21)\Z=FNG(2,L1-T1(K),T2(K))
5240 Z=FNG(1,0,13-F9-F9)\X=C1\GOSUB 6120\Z=FNG(7,0,0)
5250 X=F9\GOSUB 6120\X=K\GOSUB 6120
5260 Z=FNE1("DO   ",18)\GOSUB 1240
5270 GOSUB 3490\GOSUB 6150\Z=FNG(2,L1-T1(X),T2(X))
5280 K=X\GOSUB 6150\Z=FNG(1,0,20-X)
5290 Z=FNG(3,L1-T1(K),T2(K))
5300 GOSUB 6150\K=X\GOSUB 6150\Z=FNG(6,0,X)
5310 X=K\GOSUB 6540
5320 Z=FNG(5,0,-1)\RETURN\REM POP OFF VAL OF LOOP CNTRL VAR
5330REM **********
5340REM BLOCK
5350 D0=3\REM RESERVED FOR STATIC LINK,DYNAMIC LINK & RETN ADD
5360 T2(T1-K1)=C1\REM INIT ADD OF THE PROC BLOCK
5370 Z=FNG(6,0,0)\REM JMP TO STARTING BLK ADD
5380 X=T1-K1\GOSUB 6120
5390 IF S0$="CONST" THEN 5460
5400 IF S0$="VAR  " THEN 5550
5410 IF S0$="PROC " THEN 5730
5420 IF S0$="FUNC " THEN 5770
5430 IF S0$="BEGIN" THEN 5980
5440 Z=FNE(25)
5450REM *** CONST DCL
5460 GOSUB 1240
5470 GOSUB 2170
5480 Z=FNE1(";",5)\GOSUB 1240
5490 IF S0$="VAR  " THEN 5550
5500 IF S0$="PROC " THEN 5730
5510 IF S0$="FUNC " THEN 5770
5520 IF S0$="BEGIN" THEN 5980
5530 GOTO 5470
5540REM *** VARIABLE DCL
5550 L=0\F9=1
5560 GOSUB 1240\GOSUB 2340
5570 L=L+1\IF S0$="," THEN 5560
5580 Z=FNE1(":",5)
5590 GOSUB 1240\IF S0$="ARRAY" THEN 5610
5600 Z=FNE1("INTEG",36)\GOTO 5670
5610 Z=FNE2("[",33)\GOSUB 1240\GOSUB 2240
5620 Z=FNE2("]",34)\Z=FNE2("OF   ",26)\Z=FNE2("INTEG",36)
5630 D0=D0-L
5640 FOR I=T1-L+1 TO T1
5650 T0$(I,I)="A"\T3(I)=N3+1
5660 T2(I)=D0\D0=D0+N3+1\NEXT
```

for each type of identifier. For constants, the information is the values of the constants; for program variables, the information is the address pair (level, offset from base address); for procedures and functions, it is the address pairs and the number of parameters; and, lastly, for array variables, the information is the address pair as well as array sizes. See table 2 for actual variables that are used to store these quantities.

The symbol table is used by both the parser and the semantic analyzer. The information in the symbol table is used in a number of ways. The type of identifier is used, for instance, to check the type consistency in an expression. When a variable is referenced or a procedure or function called, the symbol table is searched to obtain the level and relative address from the base address. The number of parameters in a procedure or function is used to check the correct matching of parameters in actual procedure or function calls.

An identifier is searched for by starting from the end of the symbol table and working towards the beginning. (Viewing the table as a stack, we say that we search from the *top* of the stack down to the *bottom*.) There are two reasons for this searching direction. First, identifiers in the current block are more likely to be referenced and should be searched first. Secondly, suppose that a variable X is declared in both an outer and an inner block: by searching for X from top to bottom of the stack, we can be sure that we will find X of the inner block first, in accordance with the scope rule.

Parser, Semantic Analyzer, and Coder

The parser, the semantic analyzer and the coder are not separate routines, but are intermixed in a large routine. In most cases, after the successful parsing of a statement, its meaning is also understood by the compiler. Thus the semantic analyzer either requires minimal extra processing or is implicit in the parser and disappears altogether.

The parser, as we have mentioned before, uses a top-down technique called recursive descent. Since there is a close correspondence between the parser and the syntax diagrams of the Pascal grammar, there should be no difficulties in understanding the parsing process. The parser adopts the convention of one token look ahead which is similar to the one character look ahead convention used by the scanner. The variable S0$ is used to hold the next token to be read by the parser.

There is a part of the Pascal grammar, commonly referred to as the dangling

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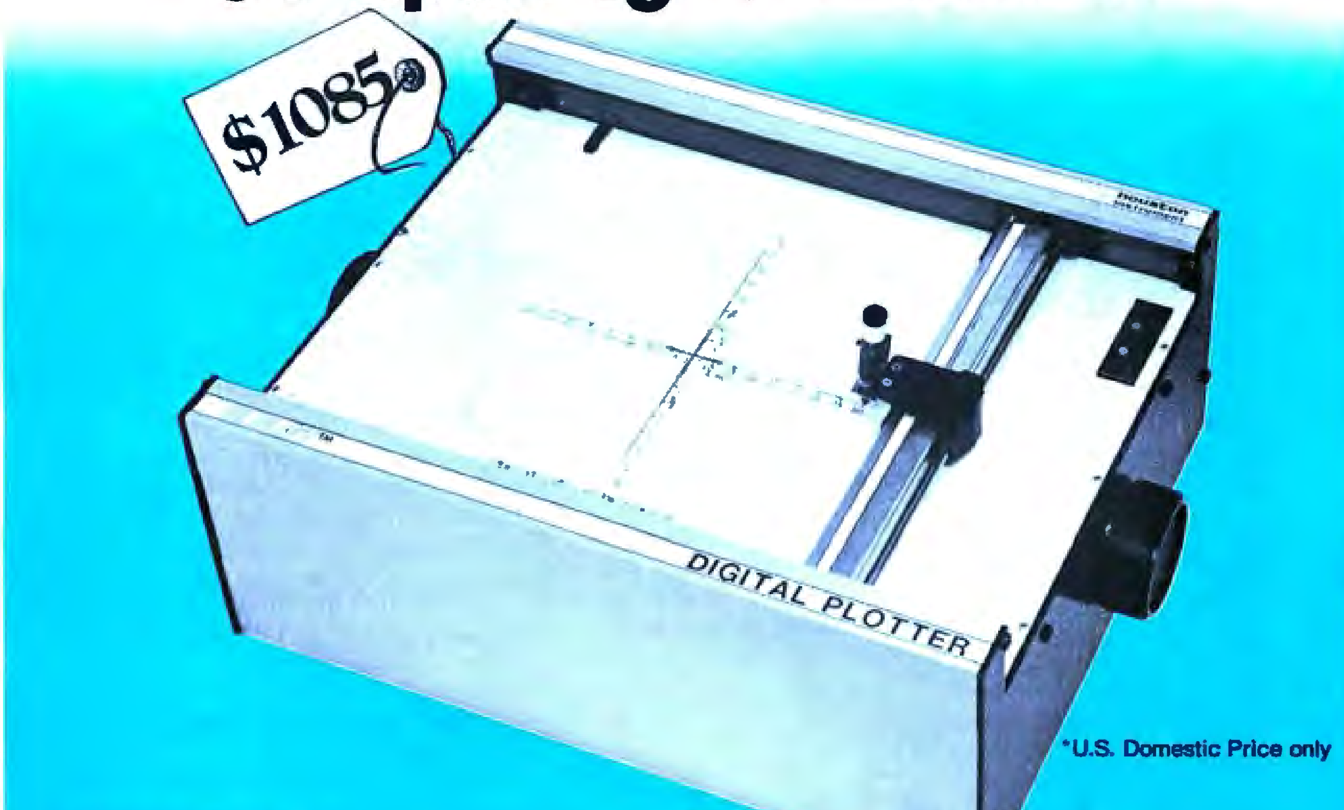

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```
5670 Z=FNE2(",",5)
5680 GOSUB 1240\IF S0$="PROC " THEN 5730
5690 IF S0$="FUNC " THEN 5770
5700 IF S0$="BEGIN" THEN 5980
5710 L=0\F9=1\GOSUB 2340\GOTO 5570
5720REM *** PROC DCL
5730 Z=FNE2("IDENT",4)
5740 K1=0\K$="P"\GOSUB 1950
5750 L1=L1+1\GOTO 5810
5760REM *** FUNC DCL
5770 Z=FNE2("IDENT",4)
5780 K$="F"\GOSUB 1950\REM FUNC ADDRSS
5790 L1=L1+1\K1=1
5800 K$="Y"\GOSUB 1950\REM FUNC VALUE
5810 K2=K1\GOSUB 1240
5820 X=T1\GOSUB 6120
5830 X=D0\GOSUB 6120
5840 IF S0$<>"(" THEN 5890
5850 GOSUB 1240\F9=0\GOSUB 2340\K1=K1+1
5860 IF S0$="," THEN 5850
5870 Z=FNE1(")",22)
5880 GOSUB 1240\T3(T1-K1)=K1-K2
5890 Z=FNE1(";",5)
5900 FOR I=1 TO K1\REM FUNC VALUE & PARS HAVE - OFFSET
5910 T2(T1-I+1)=-I\NEXT
5920 GOSUB 1240\GOSUB 5340\L1=L1-1
5930 GOSUB 6150\D0=X
5940 GOSUB 6150\T1=X
5950 Z=FNE1(";",5)
5960 GOSUB 1240\GOTO 5410
5970REM *** START OF EXECUTIBLE STTMNTS
5980 GOSUB 1240\GOSUB 6150\K=X
5990 X=T2(K)\GOSUB 6540
6000 T2(K)=C1\REM START BLOCK ADDR
6010 Z=FNG(5,0,D0)
6020 GOSUB 3490
6030 IF S0$<>";" THEN 6050
6040 GOSUB 1240\GOTO 6020
6050 IF S0$<>"END  " THEN Z=FNE(17)
6060 GOSUB 1240
6070 Z=FNG(1,0,0)
6080 RETURN
6090REM ***********
6100REM END PARSER AND CODER
6110REM ***********
6120REM PUSH X INTO STACK
6130 S(S9)=X\S9=S9+1\RETURN
6140REM **********
6150REM POP X FROM STACK
6160 S9=S9-1\X=S(S9)\RETURN
6170REM **********
6180REM PUSH Y$ INTO STACK
6190 L=LEN(Y$)
6200 S$(P8,P8+L-1)=Y$
6210 X=P8\GOSUB 6120\REM PUSH START & END STRNG POS
6220 X=P8+L-1\GOSUB 6120
6230 P8=P8+L\RETURN
6240REM POP Y$ FROM STACK
6250 GOSUB 6150
6260 L=X\GOSUB 6150
6270 Y$=S$(X,L)
6280 P8=P8-L+X-1
6290 RETURN
6300REM **********
6310REM GENERATE CODES
6320 DEF FNG(X1,X2,X3)
6330 B$="    "
6340 FILL P9,X1\FILL P9+1,X2
6350 FILL P9+2,FNA(X3)\FILL P9+3,FNB(X3)
6360 IF Y9 THEN 6400\REM IF INPUT FROM KEYBOARD THEN DONT ECHO
6370 IF X1<16 THEN 6390
6380 B$(1,1)="X"\X1=X1-16\REM INDEX
6390 !%4I,C1,"  ",M$(X1*3+1,X1*3+3),B$,%3I,X2,%6I,X3
6400 C1=C1+1\P9=P9+4
6410 IF P9>=Q9 THEN Z=FNE(1)
6420 RETURN 0
6430 FNEND
6440REM **********
6450 DEF FNB(Z)
6460 N=INT(Z/256)
6470 IF N<0 THEN N=256+N
6480 RETURN N
6490 FNEND
6500 DEF FNA(Z)=Z-INT(Z/256)*256
6510REM **********
6520REM FIXUP FORWORD REF
6530 GOSUB 6150
6540 N=P7+X*4
6550 FILL N+2,FNA(C1)\FILL N+3,FNB(C1)
6560 IF Y9 THEN RETURN
6570 !"ADD AT",X," CHANGED TO",C1
6580 RETURN
READY
```

else, that is ambiguous. The statement:

if *cond1* **then if** *cond2* **then** *stat1* **else** *stat2;*

can be parsed in two ways. The else statement can be associated with the first if or with the second if, producing entirely different results.

We resolve this difficulty by always associating the else statement with the most recent if. If an else statement with the first if is desired, one of these two methods should be used:

```
if cond1 then
    if cond2 then stat1 else
else stat2;
```

or:

```
if cond1 then begin
    if cond2 then stat1
    end
else stat2;
```

The situation is similar to the case statement with the added feature of an optional else statement. If the statement for the last case label is an if statement, we then have the dangling else problem. This is resolved in the same manner.

There are three functions used to print messages when errors are detected. The function FNE(X) prints the error message corresponding to error code X. FNE1(A$,X) checks to see if the current token is equal to A$, and prints the error message corresponding to error code X if not. FNE2 is similar to FNE1 except that the scanner is first called to get a new token. As we mentioned earlier, the compiler aborts as soon as an error is found. Therefore these error routines do not return to the calling procedure.

The code generator requires more work: care must be taken to store important values in stacks due to the inability of BASIC to fully support recursive subroutine calls. Otherwise the coder is more or less straightforward, since the p-codes are so designed (see part 1) that there is a direct correspondence between simple Pascal statements and p-codes. Table 3 shows the almost direct translation of Pascal statements into p-codes.

The declarative statements (const, var, proc, and func) do not produce any executable statements; they merely provide information about declared identifiers. The first executable code encountered when entering a procedure or function block is a forward jump instruction to the main body of the block. This jump is necessary since in general there may be procedures and func-

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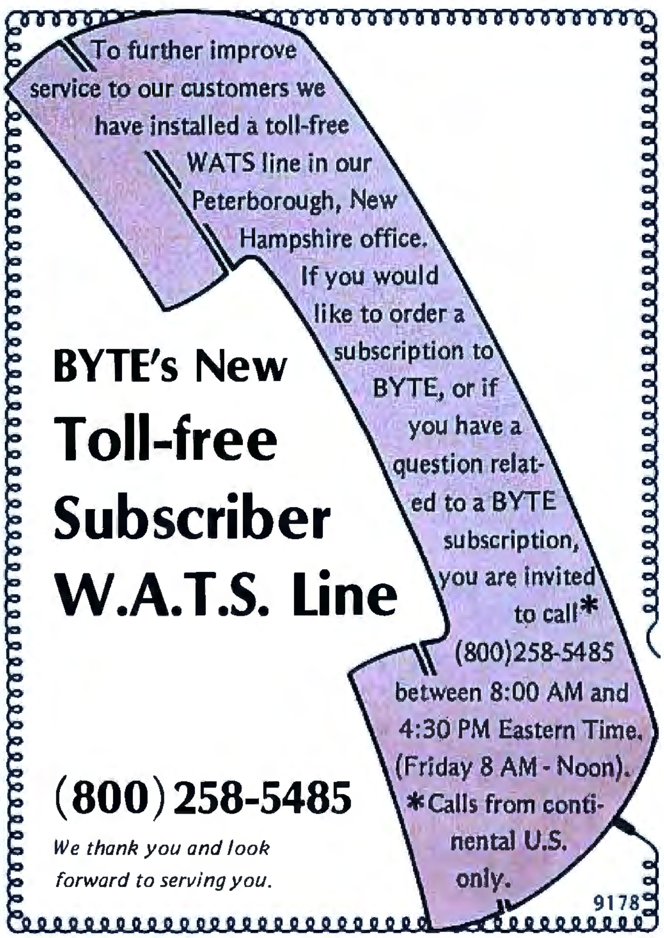
```
P-CODES START AT 0000
WANT CODE PRINTED?N
   0 ?$LST2.2
   0 CONST CR=13;LF=10;
   1 VAR A,B,C,D:INTEGER;
   1 FUNC MAX4(X1,X2,X3,X4); {LARGEST OF 4 NUMBERS}
   1     FUNC MAX2(X1,X2); {LARGEST OF 2 NUMBERS}
   2         BEGIN
   3             IF X1>X2 THEN MAX2:=X1
   9             ELSE MAX2:=X2
  12             END;
  14     BEGIN
  14         MAX4:=MAX2(MAX2(X1,X2),MAX2(X3,X4))
  28         END;
  30 BEGIN
  30     REPEAT
  31         READ (A#,B#,C#,D#);
  39         WRITE ('THE LARGEST IS',MAX4(A,B,C,D)#,CR,LF)
  67         UNTIL A<0
  69     END.
INTERPRET(I), OR TRANSLATE(T)?N
READY
LOAD DECODE
READY
RUN
   0  JMP   0     30  JMP   0     14  JMP   0      3  INT   0      3
   4  LOD   0     -2  LOD   0     -1  OPR   0      >  JPC   0     11
   8  LOD   0     -2  STO   0     -3  JMP   0     13  LOD   0     -1
  12  STO   0     -3  OPR   0    RET  INT   0      3  INT   0      1
  16  INT   0      1  LOD   0     -4  LOD   0     -3  CAL   0      3
  20  INT   0     -2  INT   0      1  LOD   0     -2  LOD   0     -1
  24  CAL   0      3  INT   0     -2  CAL   0      3  INT   0     -2
  28  STO   0     -5  OPR   0    RET  INT   0      7  CSP   0  INNUM
  32  STO   0      3  CSP   0  INNUM  STO   0      4  CSP   0  INNUM
  36  STO   0      5  CSP   0  INNUM  STO   0      6  LIT   0     84
  40  LIT   0     72  LIT   0     69  LIT   0     32  LIT   0     76
  44  LIT   0     65  LIT   0     82  LIT   0     71  LIT   0     69
  48  LIT   0     83  LIT   0     84  LIT   0     32  LIT   0     73
  52  LIT   0     83  LIT   0     14  CSP   0  OUTST  INT   0      1
  56  LOD   0      3  LOD   0      4  LOD   0      5  LOD   0      6
  60  CAL   0     14  INT   0     -4  CSP   0  OUTNM  LIT   0     13
  64  CSP   0  OUTCH  LIT   0     10  CSP   0  OUTCH  LOD   0      3
  68  LIT   0      0  OPR   0      <  JPC   0     31  OPR   0    RET
```

Listing 2: Sample Pascal program with compiled p-code. The number at the beginning of each source line is the offset of the corresponding p-code from the base address.



Variable Name	Remark
A$	String of the token returned by the scanner
C0	Input buffer pointer
C1	P-code address pointer
D0	Run time storage counter
E9	Error code
F5	Active input file unit number; keyboard=−1
K1	Number of parameter in the previous block
L0	Length of the input line
L1	Static level of procedure
L$	Input line buffer
M$	P-code mnemonics
N0	Reserved word table size
N1	Largest integer
N2	Length of identifier name
N3	Numeric value of token (token = "NUM") or ASCII value of string (token = "STR")
P8	Stack pointer for S$
P9	P-code absolute memory address counter
S	Stack for numeric values
S9	Stack pointer for S
S$	Stack for strings
S0$	Next token
T0	Symbol table size
T1	Symbol table pointer
T$	Symbol table: identifier
T0$	Symbol table: type of identifier V: variable A: array C: constant P: procedure F: function Y: parameter
T1( )	Symbol table: level
T2( )	Symbol table: value (constant) or displacement (variable) or address (proc or func)
T3( )	Symbol table: array size (array) or number of parameter (proc or func)
X	Value to be pushed or popped
X$	Next character to be read by the scanner
Y$	String to be pushed or popped
W0$	Table for reserved words

Table 2: Important variables used in the p-compiler.

tions whose codes take up space. The second executable code of the block increments the stack pointer (INT). This allocates space for the triplet (static link, dynamic link and return address) plus any variables declared. The number of spaces for the variables is already known from the declaration portion of the procedure block. The variable D0 is used to keep track of the space to be allocated at the activation of the block.

Note that no space is allocated for constants. If a constant is referenced, a load literal (LIT) instruction is generated instead of a load (LOD) instruction. Also note that the procedure or function parameters and the function return value do not reserve any space in the procedure or function block called. Space is reserved before the call is made. Therefore, these values have negative displacement from the base address of the called procedure or function.

When a call is made to a function, the space for function return value is allocated by incrementing the stack pointer (line 2980 in listing 1) (this step is skipped for a procedure call). The parameter expression is then evaluated (line 4250), putting the resultant value on the stack. Thus, space is allocated for each parameter and initialized with the value of the parameter expression. Upon return from a procedure, the stack pointer is decremented by an amount equal to the space allocated

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Pascal source		p-codes	
*x+10*y[5]*		LOD	X
		LIT	10
		LIT	5
		LODX	Y
		OPR	*
		OPR	+
a:=exp;		(exp)	
		STO	A
if *exp* then *stm1* else *stm2;*		(exp)	
		JPC	0,1b1
		(stm1)	
		JMP	1b2
	1b1	(stm2)	
	1b2	. . .	
for *i:=exp1* to *exp2* do *stm;*		(exp1)	
		STO	I
		(exp2)	
	1b1	OPR	CPY
		LOD	I
		OPR	>=
		JPC	0,1b2
		(stm)	
		LOD	I
		OPR	INC
		STO	I
		JMP	1b1
	1b2	INT	–1
while *exp* do *stm;*	1b1	(exp)	
		JPC	0,1b2
		(stm)	
		JMP	1b1
	1b2	. . .	
case *exp* of		(exp)	
c1b1,c1b2:stm1;		OPR	CPY
c1b3 :stm2;		LIT	c1b1
else *stm3*		OPR	=
end;		JPC	1,1b1
		OPR	CPY
		LIT	c1b2
		OPR	=
		JPC	0,1b2
	1b1	(stm1)	
		JMP	1b4
	1b2	OPR	CPY
		LIT	c1b3
		OPR	=
		JPC	0,1b3
		(stm2)	
		JMP	1b4
	1b3	(stm3)	
	1b4	INT	–1
repeat *stm* until *exp;*	1b1	(stm)	
		(exp)	
		JPC	0,1b1
i:=funca(exp1,exp2);		INT	1
		(exp1)	
		(exp2)	
		CAL	funca
		INT	–2

Table 3: Code generation for various Pascal constructs. For readability, the p-codes are given in assembly form. The italic identifiers in the Pascal statements are nonterminals that can be substituted by any valid expansion. The codes for these quantities are represented by parenthesized identifiers.

for the parameters, getting back to the state before the procedure call. Upon returning from a function call, the stack pointer is also decremented by the same amount, but since a space has been allocated before the function call, the function return value is now on top of the stack, ready for further processing. This simple scheme works very efficiently and should lower the overhead usually associated with procedure or subroutine calls.

Listing 2 gives an output from the compiler for a Pascal program that prints out the maximum of four numbers. There are of course better ways of writing the program, but it does illustrate some ideas of the compiler discussed so far.

There is no optimization of the p-codes produced. Limited optimization can be done on the local level, and some optimization is actually done in the p-code to machine code translator. The problem of producing efficient codes is a difficult one, and is not addressed properly in our project. Given the simplicity of the p-machine and p-code, the p-compiler is efficient. But whether the combination of p-compiler and translator produces efficient 8080 code is uncertain.

This completes our discussion of the p-compiler. In part 3 (see November 1978 BYTE), we give a detailed discussion of a translator for converting the p-code into executable 8080 machine code.■

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1. Wirth, N, "The Programming Language Pascal," *Acta Informatica,* 1, pages 35 thru 63, 1971.

2. Jensen, K, and Wirth, N, *Pascal: User Manual and Report* (second edition) Springer Verlag, New York, 1974.

3. Wirth, N, *Algorithms + Data Structures = Programs,* Chapter 5, "Language Structures and Compilers," Prentice-Hall, Englewood Cliffs NJ, 1976.

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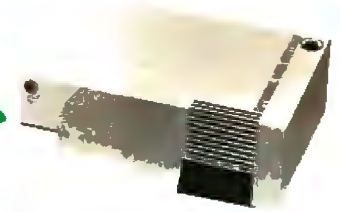

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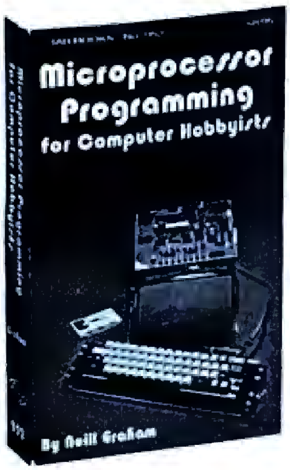

Microprocessor Programming for Computer Hobbyists is an intermediate programming text intended for users of any 8 bit word computer. The focus is on systems programming and data structures rather than on applications programming. In order to make the discussion machine independent, all the examples are presented in a high level systems programming language which is a superset of PL/M.

There are six parts to the book. The first introduces numbers systems and the second introduces the high level language which is used throughout the rest of the book. The third discusses techniques for programming various types of arithmetic such as multiple precision, floating point, etc. The fourth section introduces data structures and treats programming techniques for arrays, stacks, strings, chains, trees and graphs. The fifth part discusses techniques for searching with various structures; and the last part discusses sorting algorithms.

The book provides a good introduction and a reference to a number of programming techniques which are not dealt with in introductory programming texts. Most subjects discussed in *Microprocessor Programming for Computer Hobbyists* do not appear in the average BASIC or assembler text. Because the examples are given in a concise, high level language, they are easy to follow no matter what computer you have.

There are also several shortcomings to the book. First, I indicated that the examples are written in a superset of PL/M. I would have preferred the use of standard PL/M, since I have access to a PL/M cross compiler. Those who do not know PL/M will probably not suffer from this confusion. For the benefit of such readers, the book promises to show you how to translate between its high level language and your machine code, but this is hardly mentioned at all outside of the introduction.

All in all, this is a very good reference book. My only real quibble is that is uses a nonstandard high level language, and does not deliver all that it promises in the way of transferring this to a hobbyist computer.

John A Lehman
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Technical Forum

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What Have You Found?

I would like to express my opinion about Mr O'Reilly's letter advocating the discovery and use of undefined op codes ("Instruction Search," May 1978 BYTE, page 153). Let me state what *I* think could be the reasons for the existence of undocumented op codes in a microprocessor instruction set:

- The op code was implemented unsuccessfully and under certain circumstances does not work correctly. The manufacturer was unable to justify correcting the problem, and chose to omit the instruction from the documentation.
- The instruction is an accident, an artifact of the specific implementation. It will work on some devices, but perhaps not on devices from a second source or even from another production run from the same vendor.
- The documentation of the instruction was accidentally left out. In this case, the vendor should have already issued corrections to the documentation, and you have not in fact disclosed any new information.
- The device you tested was defective. The feature does not work for anybody else.

Now I'm not out to criticize you for discovering new things about your processor; I'm just out to warn you that if the feature you think you have discovered is not acknowledged and supported by your vendor, you are taking a chance if you expect it to function correctly and to continue to be a feature in future versions of the processor.

If you refer to *The Mythical Man-Month* by Fred Brooks, you will find a revealing discussion of the consequences of the extra op codes on the IBM 7090. Brooks makes a very strong case for the significance of the "architecture specification" of a system, which states clearly what is to be expected of a piece of hardware, and equally clearly specifies those situations in which the results of an operation are "undefined." Briefly, the outcome of undefined operations is left up to the implementers, and may be chosen by them as they see fit. Cost, convenience and plain luck have much to do with the eventual results.■

Testing Memory in BASIC

Russell E Adams
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Alexandria VA 22305

I hate to toggle in a program through the front panel of my computer. Yet every time I finish a new memory board I have to do this to a machine language memory test program. I therefore resolved to write a memory test program in BASIC which could be loaded with an 8 K interpreter in 8 K of proven memory. The BASIC program in listing 1 is the result.

The program is written in MITS 8 K version 4.0 BASIC and uses multiple statement lines with statements delimited by a colon (:). In addition to the normal functions of most BASICs, the program requires PEEK and POKE with arguments between 0 and 32767. In addition, the program needs the following BASIC primitives which may not exist on every system:

```
CLEAR 80
INPUT". .prompt. ."
IF. . .OR. . .OR. . .THEN
INT
GOSUB
LEN
RIGHT$
STR$
```

```
LIST

0 REM               ** BASIC MEMORY TEST REV.5 **
1 REM                COPYRIGHT 1977 R.E.ADAMS
25 CLEAR 80
30 INPUT"START WITH BEGINNING OF PAGE";A
35 IF A<2 OR A>7 OR A<>INT(A) THEN PRINT"ERROR":GOTO30
40 INPUT"END WITH END OF PAGE";B
45 IF B<>INT(B) OR B<A OR B>7 THEN PRINT"ERROR":GOTO40
50 A=4096*A:B=4096*(B+1)-1
55 PRINT:PRINT"TEST PATTERN #1 LOADING":PRINT
60 P1=85:P2=170:GOSUB 300
70 R=8:X=A:GOSUB 500:A$=N$
75 X=B:GOSUB 500:B$=N$
80 PRINT:PRINT"MEMORY TEST #1 FROM ";A$;" TO ";B$;" OCTAL"
85 PRINT:PRINT"ADDRESS","DATA","SHOULD BE"
90 GOSUB 350
95 PRINT:PRINT:PRINT"TEST PATTERN #2 LOADING":PRINT
100 P1=170:P2=85:GOSUB 300
110 PRINT:PRINT"MEMORY TEST #2 FROM ";A$;" TO ";B$;" OCTAL"
115 PRINT:PRINT"ADDRESS","DATA","SHOULD BE"
120 GOSUB 350
125 PRINT:PRINT"TEST COMPLETED"
130 END
300 FOR I=A TO B-1 STEP 2
305 POKE I,P1:POKE I+1,P2
315 NEXT:RETURN
350 D=P1:FOR I=A TO B-1 STEP 2
352 Z=PEEK(I):IF Z<>D THEN GOSUB 365
353 NEXT I
354 D=P2:FOR I=A+1 TO B STEP 2
355 Z=PEEK(I):IF Z<>D THEN GOSUB 365
360 NEXT I:IF F=0 THEN PRINT"NO BAD BITS DETECTED"
363 F=0:RETURN
365 F=1:R=8:X=I:GOSUB 500:BA$=N$
370 R=2:X=Z:GOSUB500:D$=N$
375 X=D:GOSUB 500
390 IF LEN(D$)<>8 THEN D$="0"+D$:GOTO390
395 IF LEN(N$)<>8 THEN N$="0"+N$:GOTO395
410 PRINTBA$,D$,N$
415 RETURN
500 N$=""
505 K=INT(X/R):L=X-R*K
510 N$=RIGHT$(STR$(L),1)+N$
515 IF K<>0 THEN X=K:GOTO505
520 RETURN
OK
```

Listing 1: A BASIC memory test program. The memory to be tested is first loaded with the alternating patterns "01010101" and "10101010" in the even and odd memory locations, respectively. After testing all the locations, a second pattern (the logical inverse of the first) is loaded and tested. If any bit is influencing the state of an adjacent bit, the bad bit will be detected.

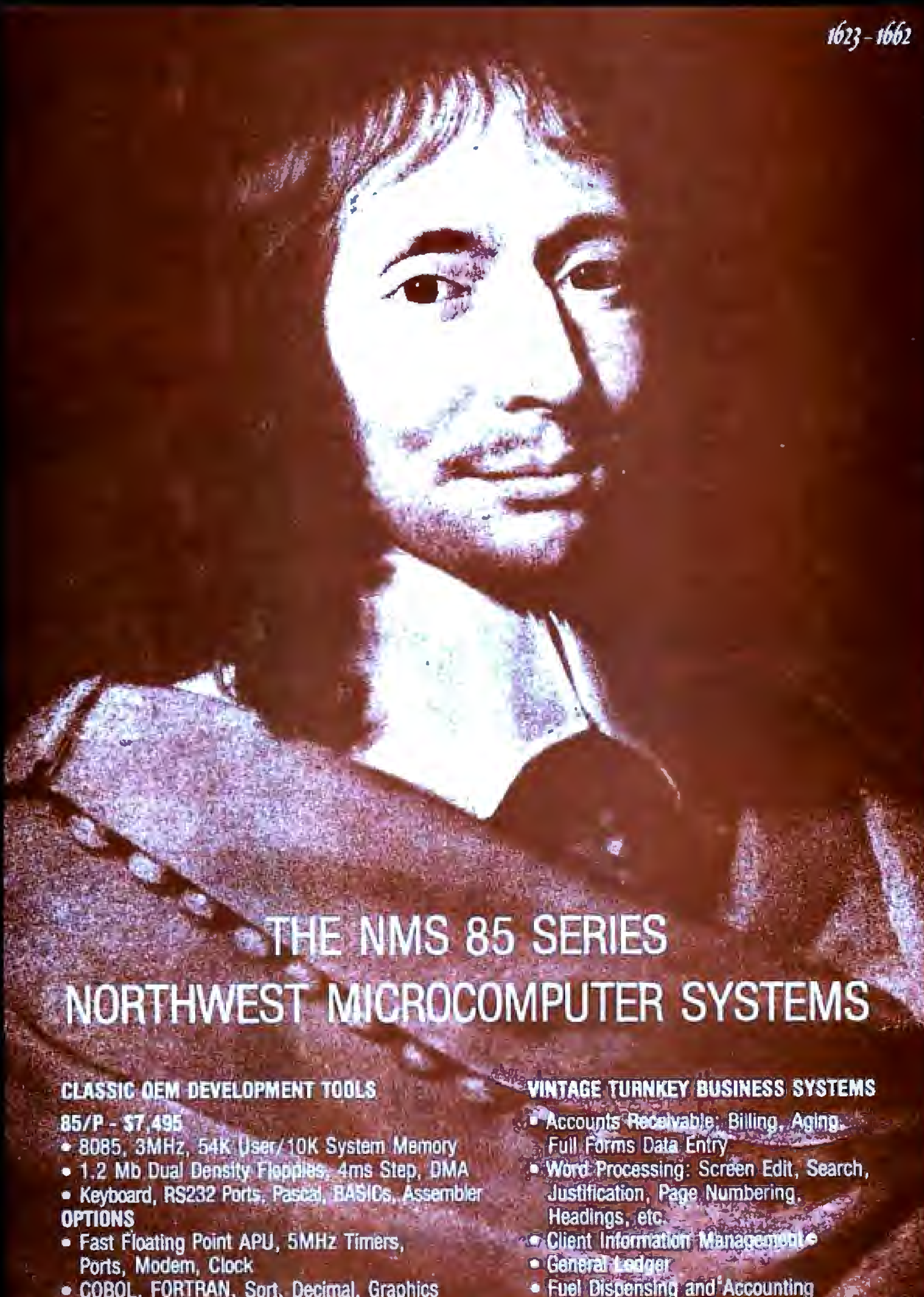
The program has two parts: lines 25 to 130 contain the main program, while lines 300 to 520 contain four subroutines. Subroutine 300 loads a test pattern into memory; subroutine 350 reads back the data in memory and compares it to what the data should be; subroutine 365 prints out the bad address and the data; and subroutine 500 converts a base ten number into a base R number.

The memory under test is subjected to two test patterns. The memory is first loaded with the alternating pattern 0101-0101, 10101010, the first byte being placed in all the even addresses and the second being placed in all the odd addresses. After reading and comparing the first pattern, the second pattern is loaded. The second pattern consists of 10101010 loaded in all the even addresses and 01010101 in all the odd addresses. This alternating pattern is used so that if a bit is influencing the state of another adjacent bit, the bad bit will be detected (the pattern assumes that adjacent addresses are physically wired up as in the memory parts specifications).

The BASIC interpreter must be limited to the lowest 8 K of memory. In MITS 8 K you answer the initial dialog MEMORY SIZE? with 8191. Also the trigonometric functions must be deleted. The program asks which pages of memory are under test. The first 4 K of memory is defined as page 0 and the last 4 K of memory is defined as page 15. The memory under test must be addressed between page 2 and 7, inclusive. This is sufficient space to test six 4 K boards, three 8 K boards, or one 16 K board.

The program takes about two minutes

Blaise Pascal



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to test 4 K of memory. A sample printout is shown in listing 2. The program first asks the questions START WITH BEGINNING OF PAGE? and END WITH END OF PAGE?. These questions are answered with the appropriate page numbers of the memory under test. The program then prints TEST PATTERN #1 LOADING and starts loading the memory with the first test pattern. Next, the two lines MEMORY TEST #1 FROM   TO OCTAL and the headings ADDRESS, DATA, and SHOULD BE are printed. The program then reads back the data in the memory and compares it to what the data should be. If the data does not compare, the address in octal is printed under the heading ADDRESS, the data in the memory address is printed in binary under the heading DATA and the data that should have been in the address is printed in binary under the heading SHOULD BE. The bits of the two bytes which do not compare indicate that they are defective. If no bad locations are detected, NO BAD BITS DETECTED is printed. The program then prints TEST PATTERN #2 LOADING and repeats basically the same above described display only for test #2.

This program should not only detect inoperative memory but also "slow" memory, "forgetful" memory and "bleeding" memory. Just type in the program and save it on tape; then the next time you have a new memory board to test, no more toggling!■

Listing 2: A sample run of the memory test program.

```
RUN
START WITH BEGINNING OF PAGE? 6
END WITH END OF PAGE? 6

TEST PATTERN #1 LOADING


MEMORY TEST #1 FROM 60000 TO 67777 OCTAL

ADDRESS          DATA              SHOULD BE
NO BAD BITS DETECTED


TEST PATTERN #2 LOADING


MEMORY TEST #2 FROM 60000 TO 67777 OCTAL

ADDRESS          DATA              SHOULD BE
NO BAD BITS DETECTED

TEST COMPLETED
OK
RUN
START WITH BEGINNING OF PAGE? 7
END WITH END OF PAGE? 7

TEST PATTERN #1 LOADING


MEMORY TEST #1 FROM 70000 TO 77777 OCTAL

ADDRESS          DATA              SHOULD BE
70000            11111111          01010101
70002            11111111          01010101
70004            11111111          01010101
70006            11111111          01010101
70010            11111111          01010101
70012            11111111          01010101
70014            11111111          01010101
70016            11111111          01010101
70020            11111111          01010101
70022            11111111          01010101


TEST PATTERN #2 LOADING


MEMORY TEST #2 FROM 70000 TO 77777 OCTAL

ADDRESS          DATA              SHOULD BE
70000            11111111          10101010
70002            11111111          10101010
70004            11111111          10101010
70006            11111111          10101010
70010            11111111          10101010
70012            11111111          10101010
70014            11111111          10101010
70016            11111111          10101010
```

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RA6800ML: AN M6800 RELOCATABLE MACRO ASSEMBLER is a two pass assembler for the Motorola 6800 microprocessor. It is designed to run on a minimum system of 16 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (such as Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

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This book provides the necessary background for coding programs in the 6800 assembly language, and for understanding the innermost operations of the Assembler.

ISBN 0-931718-10-4
Author: Jack E. Hemenway
Pages: approx. 120
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LINK68: AN M6800 LINKING LOADER is a one pass linking loader which allows separately translated relocatable object modules to be loaded and linked together to form a single executable load module, and to relocate modules in memory. It produces a load map and a load module in Motorola MIKBUG loader format. The linking Loader requires 2 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (for instance, Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

It was the express purpose of the authors of this book to provide everything necessary for the user to easily learn about the system. In addition to the source code and **PAPERBYTE™** bar code listings, there is a detailed description of the major routines of the Linking Loader, including flow charts. While implementing the system, the user has an opportunity to learn about the nature of linking loader design as well as simply acquiring a useful software tool.

ISBN 0-931718-09-0
Authors: Robert D. Grappel
& Jack E. Hemenway
Pages: 48
Price: **$8.00**
Publication: Summer 1978

TRACER: A 6800 DEBUGGING PROGRAM is for the programmer looking for good debugging software. TRACER features single step execution using dynamic break points, register examination and modification, and memory examination and modification. This book includes a reprint of "Jack and the Machine Debug" (from the December 1977 issue of BYTE magazine), Tracer program notes, complete assembly and source listing in 6800 assembly language, object program listing, and machine readable **PAPERBYTE™** bar codes for the object code.

ISBN 0-931718-02-3
Authors: Robert D. Grappel &
Jack E. Hemenway
Pages: 24
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TINY ASSEMBLER 6800, Version 3.1 is an enhancement of Jack Emmerichs' successful Tiny Assembler. The original version (3.0) was described first in the April and May 1977 issues of BYTE magazine, and later in the **PAPERBYTE™** book **TINY ASSEMBLER 6800 Version 3.0.**

In September 1977, BYTE magazine published an article entitled, "Expanding The Tiny Assembler". This provided a detailed description of the enhancements incorporated into Version 3.1, such as the addition of a "begin" statement, a "virtual symbol table", and a larger subset of the Motorola 6800 assembly language.

All the above articles, plus an updated version of the user's guide, the source, object and PAPERBYTE™ bar code formats of both Version 3.0 and 3.1 make this book the most complete documentation possible for Jack Emmerichs' Tiny Assembler.

ISBN 0-931718-08-2
Author: Jack Emmerichs
Pages: 80
Price: **$9.00**
Publication: Summer 1978

SUPERWUMPUS is an exciting computer game incorporating the original structure of the WUMPUS game along with added features to make it even more fascinating. The original game was described in the book **What To Do After You Hit Return,** published by the People's Computer Company. Programmed in both 6800 assembly language and BASIC, SUPERWUMPUS is not only addictively fun, but also provides a splendid tutorial on setting up unusual data structures (the tunnel and cave system of SUPERWUMPUS forms a dodecahedron). This is a **PAPERBYTE™** book.

ISBN 0-931718-03-1
Author: Jack Emmerichs
Pages: 56
Price: **$6.00**
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MONDEB: AN ADVANCED M6800 MONITOR-DEBUGGER has all the general features of Motorola's MIKBUG monitor as well as numerous other capabilities. Ease of use was a prime design consideration. The other goal was to achieve minimum memory requirements while retaining maximum versatility. The result is an extremely versatile program. The size of the entire MONDEB is less than 3 K.

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ISBN 0-931718-06-6
Author: Don Peters
Pages: approx. 72
Price: **$5.00**
Publication: Summer 1978

BAR CODE LOADER. The purpose of this pamphlet is to present the decoding algorithm which was designed by Ken Budnick of Micro-Scan Associates at the request of BYTE Publications, Inc., for the **PAPERBYTE™** bar code representation of executable code. The text of this pamphlet was written by Ken, and contains the general algorithm description in flow chart form plus detailed assemblies of program code for 6800, 6502 and 8080 processors. Individuals with computers based on these processors can use the software directly. Individuals with other processors can use the provided functional specifications and detail examples to create equivalent programs.

ISBN 0-931718-01-5
Author: Ken Budnick
Pages: 32
Price: **$2.00**
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Technical Forum

F D Sodamann
2603 N Greenwood
Pueblo CO 81003

In Defense of Analog?

I am an avid and enthusiastic supporter of the personal computing hobby and of BYTE. (At present I am building a full 6502-based OSI machine which pleases me very much.) But I am an old timer in electronics and think that all the fantastic digital devices which have been developed over the last few years have convinced people that general purpose analog computers belong in museums.

I feel there are a couple of things we digital hackers ought to consider:

1. Computing is computing. Setting up an analog machine to solve a differential equation is as satisfying as writing an elegant software program and, given some proper peripheral equipment, the results can be useful and aesthetically pleasing.
2. In some areas, analog machines can do a better job more easily; compare rewiring an analog machine to writing a a Runge-Kutta program or performing a slow digital computation when a less precise but real time analog computation will do).
3. The present CA3XXX series of op amps should be able to increase the accuracy of an analog machine by several orders of magnitude, especially when using a good analog/digital design for a digital readout.

Surely among your readers there are people who think as I do; I'd like to contact such people and find out the following things:

1. Does any manufacturer produce printed circuit boards or kits to build a reasonably powerful machine — say 4 or 5 integrators?
2. Does anyone have an old general purpose machine which could be updated? Is it for sale?■

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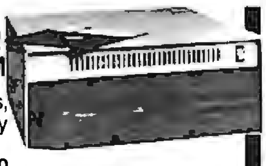

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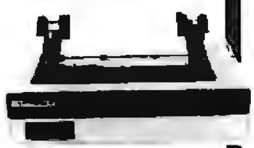

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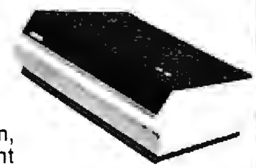

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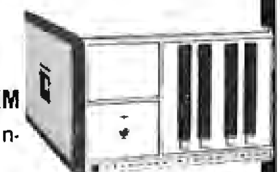

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Programming Quickies

Formatting Dollars and Cents

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Most of the BASIC interpreters available on the microcomputer market today do not provide the PRINT USING option. I have written a formatting subroutine that will perform some of the PRINT USING functions for monetary output:

- Round the monetary amount to the nearest cent.
- Convert the numeric value to a character string and check the digits after the decimal point. If the last one or both digits are missing, insert zeroes.
- Insert a dollar sign in front of the converted amount. If the amount is less than 1, insert a 0 in front of the decimal point.
- Supply the length of the amount.

Before calling the subroutine, we have to pass the dollar figure to be processed to the variable X1. The converted figure is passed back in the variable X$. The length of the formatted amount is passed back in X3.

The routine in listing 1 has been written in the Commodore PET-2001 version of Microsoft BASIC. Modifications may be required for other BASIC interpreters. The remarks can be deleted for faster execution and memory savings.

I use this subroutine in most of my programs. I place it rather high in the program (line numbers 3000 thru 3099) so I can always use the same line numbers.■

```
  10 INPUT A
  20 X1=A:GOSUB 3000
  30 PRINT TAB(20-X3);X$
  40 GOTO 10
3000 REM ******************************
3001 REM  THIS SUBROUTINE WILL FORMAT
3002 REM  DOLLARS AND CENTS
3003 REM  ******************************
3004 REM  ROUND THE AMOUNT
3005 X1=INT(X1*100+.5)/100
3010 X0$="":X$=""
3020 IF X1=0 GOTO 3030
3025 IF X1<1 THEN X0$="0"
3030 X1$=STR$(X1)
3035 X2=LEN(X1$)
3040 X2=X2-1
3041 REM  DELETE SPACE IN FRONT
3042 REM  OF THE FIRST DIGIT
3045 X1$=MID$(X1$,2,X2)
3050 FOR I=1 TO X2
3055 X2$=MID$(X1$,I,1)
3060 X3=I
3065 IF X2$="." GOTO 3085
3070 NEXT I
3075 X$=".00"
3080 GOTO 3090
3085 IF X3=(X2-1) THEN X$="0"
3086 REM  CREATE THE FINAL STRING
3090 X$="$"+X0$+X1$+X$
3091 REM  FIND THE STRING LENGTH
3095 X3=LEN(X$)
3099 RETURN

RUN

?2                 $2.00
?2.2               $2.20
?2.22              $2.22
?2.222             $2.22
?222             $222.00
?75.756           $75.76
```

Listing 1: BASIC program for formatting dollars and cents in BASIC interpreters that do not have the PRINT USING function. Also shown is a sample run of the program.

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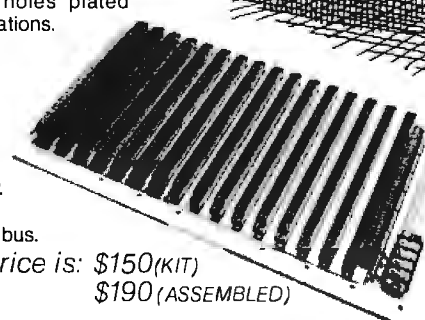

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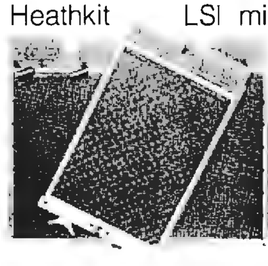

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PAM/8: A New Approach to Front Panel Design

Gordon Letwin
Heath Company
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Since the first personal computers appeared about three years ago, the field has been growing and advancing at an ever increasing rate. The variety and complexity of products increases even while the cost decreases. Indeed, the field has evolved so rapidly that it has gone through two generations (using the term somewhat loosely) in those three years. The first generation machines were typified by the first 8800 system sold by MITS, a bare bones machine festooned with switches and lights. It took a fair amount of technical know how to build one of these to get it operational. Before long, however, a new generation of machines was available. These, such as the SwTPC 6800, were usually cheaper and simpler to build, using fewer but more powerful integrated circuits.

And in July 1977, the Heath Company announced its two versions of the home computer idea, the H8 and H11 systems. I write as one of the persons who took part in the design of the H8's front panel firmware, an 8080 program called "PAM/8" which shows how software and hardware are often intimately related.

Microprocessor Front Panels

The ideal front panel for a microcomputer should allow its user total control and access to the processor's workings. A good panel system should allow an instantaneous display of the processor's states, register contents, memory contents, and other operating flags. An operator should be able to force a new state, register value, or memory value upon the processor with ease at any time without otherwise interfering with the executing program. In other words, it should be possible to examine any memory location or any register at any time without disturbing the program.

Ten years ago the implementation of such a front panel was obvious. The processor was built up from components such as integrated circuits, and the flags and registers were directly available on the circuit cards. In the remainder of this article, I will refer to this type of machine as a *discrete processor*, although it may be built out of high level integrated circuits. To build a suitable front panel for such a discrete processor, it is merely necessary to run a wire to a front panel indicator. Likewise, special logic can be built to allow flags and registers to be set from the front panel switches, usually when the machine is in a halted condition. Readers may have had experience with some of these minicomputer systems, such as the CDC 1700 or the IBM 1130 and 1620. This design works reasonably well, but the binary format is inconvenient and the cost of the front panel hardware and logic can be prohibitive for use in a personal computing system.

The situation was considerably changed with the advent of microprocessors. Now, for the first time, a full-fledged computer is within the financial reach of the general public. Unfortunately, the very development which brought this exciting possibility also brought problems. With a 1 integrated circuit microprocessor, the processor flags and register contents were no longer available for a front panel system, being buried out of reach of any possible hardware hookups. A typical microprocessor integrated circuit only has 40 connection pins (or pinouts). These are partly taken up with power supply and clocking signals, as well as the data and address buses. The remaining pins are allocated to receiving and providing signals to interface the processor to the rest of the computer system. As a result, there is no direct way to determine the contents of the processor's registers.

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Aiea	Delcoms Hawaii
Honolulu	Integrated Circuit Supply
IDAHO	
Boise	Custom Electronics
Caldwell	A-Gem Supply Inc.
Idaho Falls	Audiotronics
ILLINOIS	
Carbondale	Layfayette Radio
Evanston	Itty Bitty Machine Co.
Evanston	Tri-State Electronic Corp.
Granite City	Computer Systems Center
Groveland	Moyer Electronics
Mount Prospect	Tri-State Electronic Corp.
Niles	Computer Land
Oak Park	Spectronics Inc.
Peoria	Warren Radio Co.
Rockford	Imperial Computer Systems
Schaumburg	Data Domain
INDIANA	
East Chicago	Acro Electronics Corp.
Hammond	Quantum Computer Works
IOWA	
Clinton	Bridge Elec. Computer Center
Davenport	Computer Store of Davenport
Des Moines	Radio Trade Supply Co.
Indianola	Electronix Limited
KANSAS	
Kansas City	Electronic Surplus Sales
KANSAS (Continued)	
Manhattan	Communications Specialties Ltd.
Wichita	Amateur Radio Equipment Company
KENTUCKY	
Lexington	Radio-Electronic Equipment Co.
LOUISIANA	
Baton Rouge	Davis Electronics Supply Co.
Baton Rouge	Menard Electronics Inc.
New Orleans	Wm. B. Allen Supply Co.
MARYLAND	
Baltimore	Computers Unlimited
Baltimore	Computer Workshop of Baltimore
Baltimore	Everything Electronic
La Vale	J & M Electronics
Rockville	Computer Workshop
Silver Spring	Computers Etc.
Towson	Baynesville Electronic Inc.
Towson	Computers Etc.
MASSACHUSETTS	
Medford	Tufts Electronics
North Adams	Electronics Supply Center
Waltham	Computer Mart Inc.
Worcester	RM Electronics Inc.
MICHIGAN	
Ann Arbor	Airway Electronic Communications
Flint	Hobby Electronic Center
Grand Rapids	Micro Computer World
Lansing	Fulton Radio Supply Co.
Midland	Computronix Corp.
Mt. Clemens	The Computer Store
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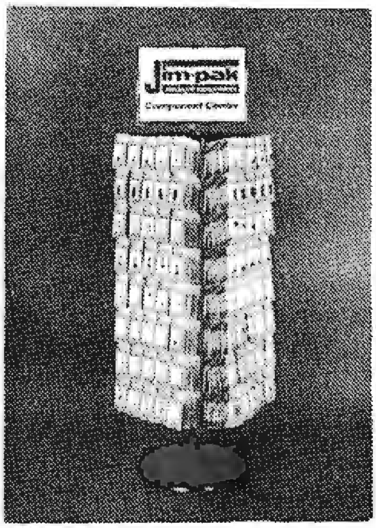

MINNESOTA	
Duluth	Northwest Radio of Duluth
Eagan	Computer Room Inc.
Hopkins	Heathkit Electronic Center
St. Paul	Heathkit Electronic Center
MISSOURI	
El Dorado Springs	Beckman Electronics
Florissant	Computer Country
Parkville	Computer Workshop of Kansas City
MONTANA	
Billings	Conley Radio Supply
Bozeman	Electronic Service & Distributing
Great Falls	Art's Electronics
NEBRASKA	
Lincoln	Altair Computer Center
Lincoln	Scott Electronic Supply Inc.
North Platte	Scott Radio Supply Corp.
Omaha	Heathkit Electronic Center
Omaha	Omaha Computer Store
NEVADA	
Las Vegas	Century 23
NEW JERSEY	
Bayville	A. R.S. Communications Services
Bricktown	Radio Shack Associate Store
Cherry Hill	The Computer Emporium
Hoboken	Hoboken Computer Works
Paterson	All-tronics
Pompton Lake	Computer Corner of New Jersey
Ramsey	Typetronic Computer Store
NEW YORK	
Albany	Fort Orange Electronics
Kingston	Greylock Electronics
New York	Computer Mart of New York
Rensselaer	Com-Tech Electronics
Rochester	2001 Microsystems
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Utica	Am-Com Electronics
NEW YORK (Continued)	
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Williamsville	Hirsch Sales Co.
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Durham	Futureworld
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Fargo	The Computer Company
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Bucyrus	Mead Electronics
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Previous Front Panel Systems

Attempts to solve this fundamental problem of control over the microprocessor have been responsible for the major differences between competing machines. The first widely available machine, the MITS 8800, used a direct approach to front panel design: it simply had LED readouts for each pinout on the microprocessor chip and a bank of switches hooked across the data and address busses. Some additional logic was incorporated to control the running state of the microprocessor and to allow memory locations to be read to and written from via the front panel. This scheme is a straightforward adaptation of traditional panel design; unfortunately, there wasn't a great deal of correspondence between the useful items a programmer might want and the data available on the processor pinouts.

The difficulties of using such a panel system are by now nearly legendary: it is very awkward and time consuming to get information in and out of the processor. For example, to simply determine the contents of a register, it is necessary to stop the processor, write a small program to store the register in a memory location, key it in to some unused portion of memory, run it, read the stored value from memory, and then restore control to the interrupted program. Needless to say, this is a tedious process with many opportunities for error.

The problems with this approach no doubt influenced the designers of the second generation machines. They used a different approach wherein a console terminal was used in conjunction with a monitor program (usually in read only memory) to provide the equivalent of front panel service. With such a system, a programmer could display desired information such as memory or register contents directly in octal or hexadecimal. This represented a great step forward: entry speed was increased, and the clerical task of encoding and decoding binary values was eliminated. Another great benefit of this system was that most of the monitors incorporated a bootstrap loader so that the loader did not have to be keyed in each time.

This technique has been rapidly gaining popularity at the expense of the lights and switches system, for obvious reasons. Several companies are offering such monitors encoded in read only memory boards to allow users to convert their old systems. However, this new technique still has a few disadvantages: it requires a console terminal, which adds considerably to the system cost, and once a user program has started execution the services of the monitor system are no longer available.

PAM/8 Design Goals

It was mentioned above that the front panel system is the area in which many of the differences between computer systems are found; this holds true for the Heath H8 system as well. The H8 employs a new concept in microprocessor front panels: it uses a unique combination of software and hardware to allow the emulation of a complete real time front panel system which I believe to be superior in performance to even the discrete minicomputer panel systems.

When the H8 project began, Heath engineers studied the requirements for a good front panel system closely and drew up a list of the major features to be satisfied. There were nine major requirements of a good front panel:

- The front panel system must present and accept data in a convenient octal format. Encoding and decoding binary is a job more suited to a computer than a human being.
- The front panel system must incorporate facilities to load and dump memory to and from an external device such as a cassette interface. A nearly foolproof error detection scheme must be used so that mysterious errors will not be introduced by bad loads.
- The front panel system must allow memory and register contents to be conveniently displayed and changed. In addition, data display has to be in real time. That is, if the front panel is displaying the contents of a register and the running program changes those contents, the change should be immediately visible on the panel.
- The front panel system must be capable of execution control. That is, the programmer should be able to step through a program one instruction at a time, and be able to set breakpoints within his code.
- The front panel system must provide facilities for inputting and outputting to IO ports.
- The front panel system must be easy to use, and (as much as possible) should reduce the opportunity for operator error. Whenever a front panel operation is performed, the programmer must be informed of the operation's success or failure.

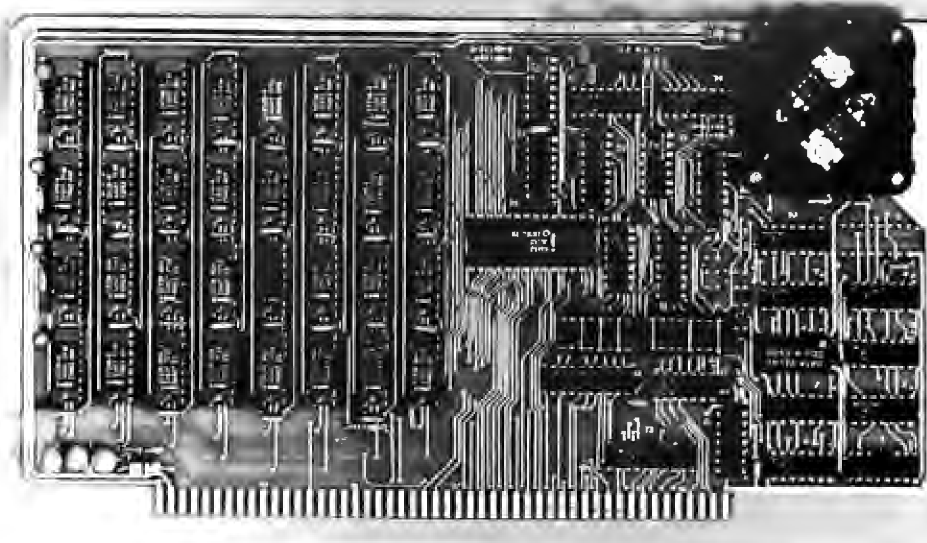

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Photo 1: Front panel of the Heath H8 computer. At left are nine 7 segment LED displays and four single LED lamps; at right is the 16 key keypad. The front panel is controlled by a novel firmware panel monitor (PAM/8) made up of both hardware and software elements.

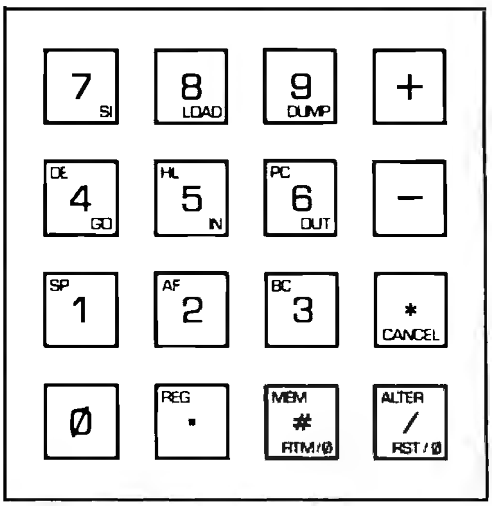

Photo 2: H8 16 key keypad, the sole input source for the panel monitor (PAM/8). The keypad is used to enter commands and data. Some keys have more than one function, but the monitor provides an indication of which meaning will be taken for these keys.

- The front panel system must be transparent. In other words, it must emulate a hardware panel system so that no changes are necessary to any program to allow it to be run under the PAM/8 (PAnel Monitor) system. Likewise, the front panel firmware must present a light processor load to the system so that program execution proceeds at a normal pace.
- The front panel system must be versatile. No system can be all things to all people. Some sophisticated users may have special requirements; the system must be designed to allow the sophisticated user to circumvent part or all of the system.
- The front panel system must be inexpensive. Advanced design techniques must be used to keep the cost of the panel system at or below the cost of current front panel systems.

Undoubtedly, this was a formidable list. Happily, though, Heath was able to report success with the creation of the PAM/8, the panel monitor for the H8 computer.

PAM/8 Description

The front panel of the H8 computer is shown in photo 1. Three features are immediately obvious: a 16 key keypad, nine 7 segment LED displays, and four single LED lamps.

The 16 key keypad (see photo 2) is the sole input device to the PAM/8 system. It is used for commands for PAM/8, to enter data into memory and registers, and as a bank of sense switches. Some keys have more than one function; however, no confusion results because PAM/8 provides a clear indication at all times of which meaning will be taken for such keys.

The second visible feature is the group of nine 7 segment LED displays. These are used to display addresses, data, and register names. 16 bit values are displayed in "split octal" notation. Each byte is represented as three octal digits; therefore, a 16 bit value is simply presented as two such byte groups together. Thus, in split octal notation, 377 + 001 = 001 000.

The third visible feature consists of four LED lamps (see photo 3). Three of these lamps display true hardware conditions: power on (PWR), processor running (RUN), and interrupts enabled (IE). In fact, these are the only hardware indicators in the PAM/8 system. All other displays, indicators, and keypads are under firmware control. The remaining LED, MTR, is lit when the computer is in monitor mode. Monitor mode means that the user program is not running, and the keypad is available for PAM/8 commands. When the user program is running, PAM/8 ignores most keypad commands so that the user program can use it as an input (sense switch) device.

The best way to describe the operation of the PAM/8 monitor is to go through the list of design goals again, describing how it fulfills each objective. In the process, I will touch upon some other pieces of PAM/8 hardware not visible on the front panel.

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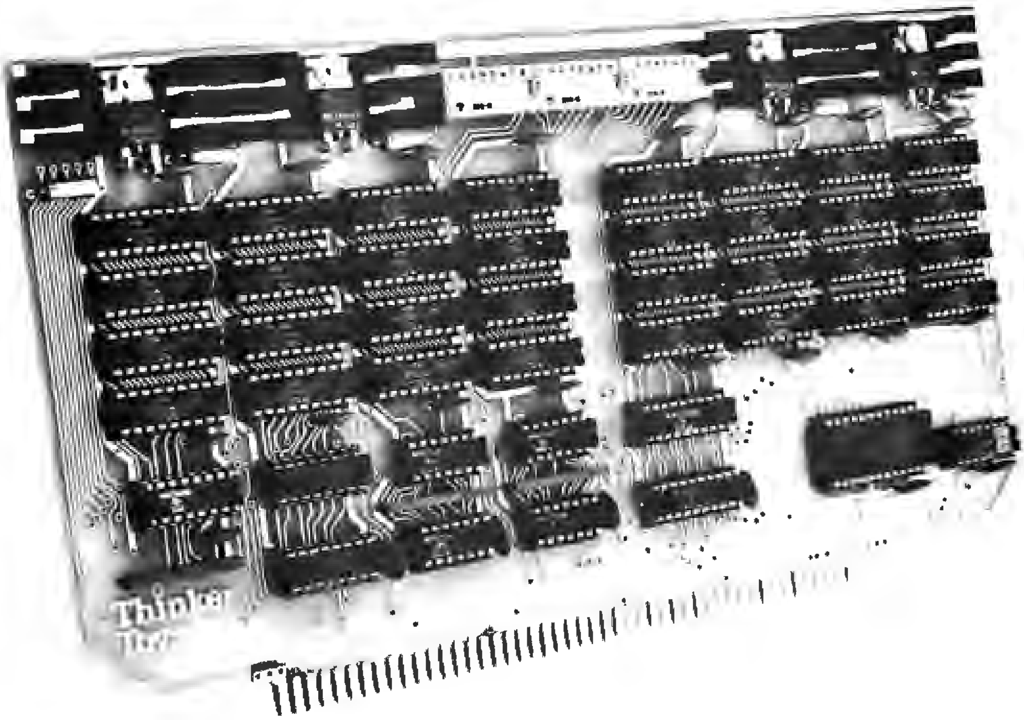

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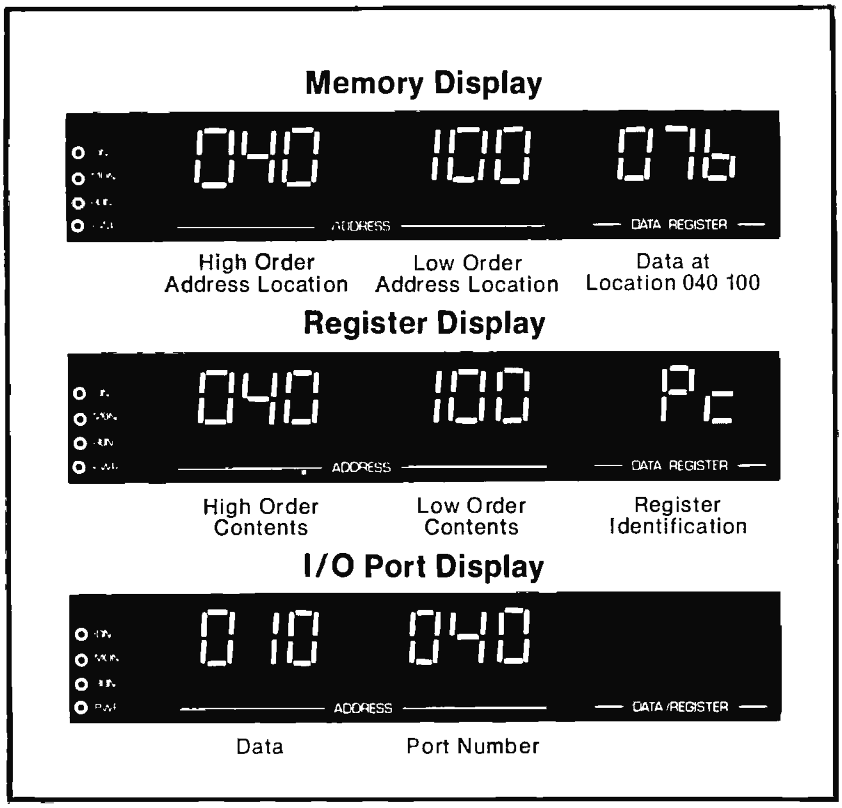

Photo 3: Three examples of the H8 LED readout format for memory display, register display and IO port display.

"The front panel system must present and accept data in a convenient octal format." This has already been discussed: PAM/8 displays and accepts octal values. 16 bit values are represented in a convenient byte octal notation.

"The front panel must incorporate facilities to both load and dump memory." The 8 and 9 keys are used for loading and dumping memory. In order to dump a block of memory to an output device (usually magnetic or paper tape), one must supply PAM/8 with the starting dump address, the ending dump address, and the entry point address. When the DUMP key is struck, PAM/8 writes a formatted record containing the memory contents. The dump record produced contains the starting address, the entry point address, and the memory data. The record is followed with a 16 bit cyclic redundancy check (CRC-16).

To reload a memory dump tape, place the tape in the transport (cassette or paper tape) and strike the LOAD (8) key. PAM-8 will read the tape and discard any information until the *beginning of record* sequence is found. The load operation then begins. When the load is complete, the computed CRC-16 is compared to the one on the tape. If the load is correct, PAM/8 gives a single beep. Since the program counter (PC) register was loaded with the entry point address, striking the GO key will begin execution. If the load is incorrect, PAM/8 displays the error code 001 (CRC error) and repeatedly beeps the horn. Pressing CANCEL (*) silences the horn.

During the load and dump operations, the six leftmost LEDs display the address being loaded or dumped, while the three remaining LEDs display the data value going into or out of that location. This allows the operator to see if the load is progressing, and gives an idea of how much is left. The H8 cassette system runs at 1200 bps, allowing the loading of 8 K BASIC in about 60 seconds.

The CRC-16 check value used in PAM/8 is nearly foolproof: single bit errors, double bit errors, and error bursts of less than 16 bits are always detected. The chance of a larger error escaping undetected is less than 0.0002%.

"The front panel system must be capable of displaying and altering both memory and registers conveniently." To display the contents of a memory location or register, strike the MEM (#) or REG (.) key followed by a 6 digit address (for MEM) or a 1 key register select (for REG). In the case of memory display, the address will appear in the left six digits, the value in the right three. In the case of a register, the value of the register (if 16 bits) or the register pair (for 8 bit registers) is displayed in the left six digits, and the register name(s) is displayed in the right two digits. See photo 3 for examples.

To change the contents of a register or memory location, first display the old contents as described above. Next strike the ALTER (/) key. You can then alter the register or location by entering six (or three) octal digits. As each 3 digit group is entered, the PAM/8 monitor provides a beep in acknowledgement. In the case of memory alteration, the memory address is automatically incremented by one. This allows you to enter a series of memory locations by entering a steady stream of values.

When the altering is complete, restriking the ALTER key clears the alter mode and restores the 0 through 7 keys to their usual function.

It is important to note that the register and memory displays are real time: if the contents of that register or location change, the display will immediately show the new value. Thus, to watch the PC register in a

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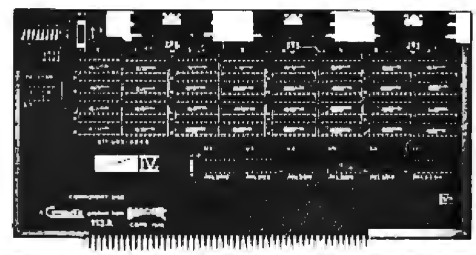

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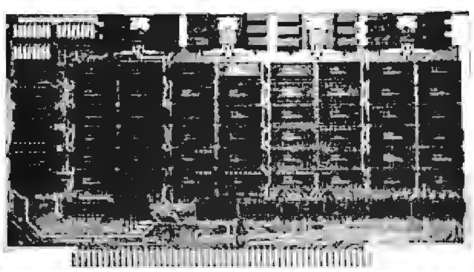

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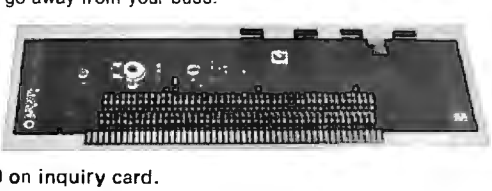

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running program, merely select it for display and type GO. Should you now decide to watch the contents of a memory byte, press RTM/0 (# and 0 simultaneously) to halt the program, select the memory location, then press GO to resume execution from where it halted.

"The front panel system must be capable of execution control." PAM/8 provides five types of execution control:

- Run
- Halt
- Jump
- Breakpoints
- Single Instruction

Pressing the GO key starts a program running at the current value of the PC register. The desired start address can be entered into the program counter beforehand. To stop a running program, press RTM (return to monitor, keys 0 and # simultaneously). Execution of the program will immediately halt, and the MTR light will come on. The operator can now examine registers and memory locations and may alter them if desired. Pressing GO causes execution to resume where it left off. To jump the processor to a section of code, press RTM, alter the PC register and press GO.

When a HLT instruction is encountered by a user program, the PAM/8 gives a single alarm beep and execution of the user program is halted. The PC register points to the byte following the HLT operation. Pressing GO causes execution to resume following the HLT opcode. The user can make use of breakpoints to debug programs by assembling or patching in HLT operations.

PAM/8 also includes a single instruction facility. Each time the SI key is struck, the instruction pointed to by the program counter is executed and the user program is immediately halted. This works for all 8080A instructions except DI (disable interrupts) including jumps, subroutine calls, and other control-transfer instructions. Holding down the SI key causes the execution of an instruction every 400 ms. It is especially instructive to display a register and use the SI key to execute instructions one by one while watching the effect these instructions have on the registers being displayed.

"The front panel system must provide facilities for communicating with IO ports." To communicate with an IO port, use the MEM key to enter the 3 digit data value and the 3 digit port address as a 6 digit memory address. Striking the OUT key causes the data value to be output to the port. Striking the IN key causes the value read from the port to be displayed in the leftmost three digits.

"The front panel system must be easy to use and should reduce the possibility for error." In order to increase convenience and minimize operator errors, PAM/8 is designed to maximize the bandwidth of the operator-machine communication channel. Thus, PAM/8 communicates in three different ways: by the digit displays, by the alarm horn, and by the display decimal points. The use of the digit displays in communication is obvious. Many panel operations, such as entering addresses and values, cause the display to change. For instance, when altering memory, the value of each key struck is shown in the displays. The front panel horn actually serves three purposes:

- Verify keystrokes.
- Provide information (such as the beep when entering byte values).
- Provide alarm indications (such as a CRC error when loading).

The PAM/8 uses the digit decimal points independently of the values on the digits themselves. As can be seen from photo 1, some keys have multiple uses. PAM/8 uses the decimal points to indicate which use of the key is currently *active*. When the REG or the MEM key is struck, PAM/8 expects an address (or register number). The decimal points are lit continuously, indicating that the address must be entered and that the keys 0 through 7 will be taken as address values. When the ALTER key is struck, PAM/8 displays a rotating pattern on the decimal points, indicating that a value must be entered, and the keys 0 through 7 will be taken as data values.

"The front panel system must be transparent." In operation, PAM/8 is totally transparent to a task program; ie: the program need not take any notice of the presence of the PAM/8 system; any existing 8080A program can run on the H8 without change (assuming it is ORGed correctly, and the IO is compatible). Since PAM/8 is implemented partially in system software, it does require processor service for operation. Normally, PAM/8 uses about 15 percent of the processor's capacity, leaving 85 percent for task programs. Most programs are compute bound for very short periods of time, and this presents no difficulties. Programs which must run at full speed can set a flag bit in the PAM/8 programmable memory area to turn off the front panel, which then gives the task program 100 percent of the

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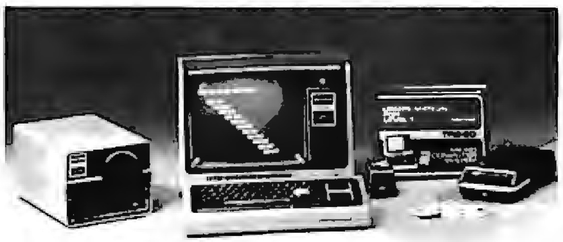

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processor's capacity. The task program can then reenable PAM/8 when it desires.

"The front panel system must be versatile." Although a user program need not communicate directly with PAM/8, such communication is possible. In general, there is a set of special control bytes in the PAM/8's programmable memory area which can be used to control system operation. For example, a user program can cause PAM/8 to display any arbitrary segment pattern on the LED displays. Likewise, the user program can cause PAM/8 to stop refreshing the displays so that the program can refresh them itself. In general, it is possible to totally *close down* PAM/8 operations and to have a user program take them over, thus totally replacing the PAM/8 monitor with a homebrew system. Of course, user programs can make use of the PAM/8 utility subroutines to communicate with the tape system, read the keypad (with audio feedback and auto repeat), sound the horn, and so forth.

"The front panel system must be inexpensive." PAM/8 provides powerful features at a low cost due to its firmware design. The read only memory software handles display decoding and refreshing, keypad debouncing, and all high level functions. The necessary hardware consists of the keys, the LED displays, and a few SSI and MSI logic gates. In general, the PAM/8 design costs less than a good toggle switch and lamp panel.

How It Works

As mentioned above, PAM/8 is a firmware system, meaning that its functions are implemented by a closely integrated combination of hardware and software. The hardware resides on the front panel circuit board itself, and the software resides in a 1 K read only memory on the processor board. This read only memory contains a program which does most of the work for the PAM/8 system. Actual hardware was used only when the function could not be implemented by the program.

The central concept in the PAM/8 system is its built-in clock interrupt. When the system is powered on (or master cleared) PAM/8 sends a command to the panel control port requesting an interrupt every 2 ms. This interrupt interval is derived from the system's crystal clock and is therefore called the clock interrupt. The presence of this interrupt allows PAM/8 to perform two processes, or tasks, *simultaneously*. Of course, they are not actually performed simultaneously, since the computer has only one processor, but to a being as slow as a human the operations appear simultaneous.

This division of the work load between two independent tasks, the task time and the interrupt time processes gives PAM/8 its power. For the sake of clarity, the functions of these two tasks will be discussed separately and it will be assumed that they are truly simultaneous.

Interrupt Time

The interrupt time task is always running (unless shut off by the user program) and has three main jobs:

- Process display refreshing and updating.
- Maintain system clock.
- Allow user program clock servicing.

The most important job of the interrupt time process is to refresh the front panel displays. The displays are not latched and decoded; the display hardware consists of a 4 bit digit select field and an 8 bit pattern select field. Every interrupt cycle (2 ms), a segment pattern and digit number are output by the code. The digits are refreshed round robin so that each digit is lit every 18 ms (nine digits at 2 ms each). This gives an overall refresh rate of 55 times a second, which is sufficient to eliminate flicker. The segment patterns being refreshed are obtained from a 9 byte programmable memory area. Each 8 bit byte contains the pattern for a digit (seven segments, one decimal point). Every 32 clock interrupts, or about 16 times a second, the 9 byte pattern being displayed is updated. The PAM/8 monitor examines flag locations to determine which memory location or register is being displayed and decodes its value into nine bytes of display bar code. If a register is being displayed, the program finds its value on the stack where it was pushed when the clock interrupt occurred. It should be noted that both of these processes, refreshing and updating, may be controlled by a user program. There is a bit for each function allocated in a PAM/8 control byte; setting the bit causes the function to be discontinued. Most programs which make use of this feature turn off display updating, but they leave display refreshing turned on. Then the program can display any arbitrary pattern by simply placing segment bar patterns into the 9 byte area in memory.

The second main job performed by the interrupt time task is the maintenance of the system clock. The PAM/8 monitor

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maintains a 16 bit count of the clock interrupts received. Since this count is updated during the clock interrupts, it appears to task time programs that the location "magically" increments itself. Many programs, including the task time portion of PAM/8, make use of this counter.

The third major job of the interrupt time task is the handling of user clock processing. Normally, PAM/8 returns directly from the clock interrupt so that the operation will be transparent to the user program. However, a user program can set a bit in a PAM/8 control byte requesting that a user subroutine be called during every clock interrupt. This allows the user to also write task time and interrupt time systems, as well as giving multitasking capability.

Task Time Task

While all this clock interrupt processing is taking place, the H8 is also running a *task time* program. Task time refers to the "problem solving" program which runs when interrupts are not being serviced. Under the PAM/8 system, the task time program may be the user program itself, or it may be the PAM/8 command processing program.

When the system is initialized after power up, the task program is the PAM/8 command processor, which continually reads the keypad for operator commands. Keypad debouncing, key strike verification (beeps) and auto repeat on the keypad are all time dependent functions; PAM/8 makes use of the system clock to implement them. When a command is recognized, it is executed immediately. Having the interrupt time task running simultaneously with the command loop greatly simplifies command processing. For example, pressing the + key (when displaying memory) is supposed to cause the next location to be displayed. All the command processor needs to do is to increment the "address being displayed" word in memory. Sometime during the next 32 clock interrupts the interrupt task will decode this new address and its contents, causing the new address and value to be "magically" displayed (after a maximum wait of 1/6 of a second). In a similar manner, the routines to handle the LOAD and DUMP functions merely update the address being displayed word after every byte is loaded or dumped; the interrupt time task sees to it that the address being loaded is continuously displayed on the panel LEDs.

After reading this discussion, you can probably guess how the GO command is implemented: the PAM/8 monitor merely restores the user registers from the stack. The PC register is restored last, which causes execution to begin at the specified location. The interrupt time task proceeds as before, decoding and displaying the selected memory or register contents. Should the location or register be altered by the running program, the front panel will very quickly (typically in 32 ms) show the change.

HLT and Return to Monitor

So far, we've seen that the interrupt time and task time processes don't intermingle; each keeps to its own. The processing of the HLT instruction and the RTM (return to monitor) command are exceptions to this principle. When a HLT instruction is encountered the processor waits with the program counter pointing to the next byte. When the next clock interrupt comes along, the interrupt processing code takes a look at the preceding instruction; if it is a HLT, the code passes control directly to the PAM/8 task time command loop, never

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returning to the user program. Naturally, a little bit of cleaning up is performed to smooth over the abrupt transition from interrupt time to task time. This feature allows the use of the HLT instruction as a breakpoint and also provides transparent support of the HLT operation. When a program halts, the front panel comes alive, and user program execution stops. Striking the GO key causes execution to resume following the HLT instruction.

The RTM command is a key command executed by pressing the 0 and # keys simultaneously. This command serves the purpose of the RUN/HALT switch on hardware front panels: striking RTM causes execution of the user program to cease, and it causes the front panel to become active. The RTM command is implemented by a joint hardware and software effort: on a hardware level, the pressing of the two keys causes a clock interrupt to be requested immediately, without waiting through the 2 ms interval. On the software level, the clock interrupt code in PAM/8 checks the keypad for the special RTM key combination. If it is present, the same process that was used for the HLT operation is used: control passes directly to the PAM/8 task time command loop, not back to the interrupted user program.

Using the PAM/8

The design of recent microcomputer systems has shown a trend away from front panel designs toward the "no front panel" monitor. This is being done for a very good reason: a terminal monitor based on programmable memory or read only memory is much easier to use and is more powerful than hardware front panels. This fact also applies to the PAM/8 system: a good console oriented monitor and debugger, such as Heath's HBUG, is much more convenient for debugging programs. This is not to say that PAM/8 does not perform an indispensable task, as I will try to show in the following real life examples.

A typical experience in the life of a computer experimenter is the debugging of some peripheral interface. I've spent many a long hour slaving over a processor, trying to make some new device or interface talk to my computer. A favorite technique I use for this is to enter a 2 statement program into memory:

```
L1    IN     <port number>
      JMP    L1
```

This program simply inputs from the port assigned to the recalcitrant device into the accumulator, then loops back to do it again and again. Then all I do is set the PC register to the L1 address, punch up the accumulator for display, and press GO. The value read from the port will be continuously displayed in the A register, even while I adjust the hardware. By watching the panel displays, I can instantly see any results of my labors, such as, "if I ground this line, will that bit come on?"

Another important use for PAM/8 is as an aid to debugging software. Often I find myself debugging a complex piece of software that maintains various state flags in memory. For example, a command completion subroutine, which examines characters as they are entered for valid syntax, is a state dependent program. As each character is entered, the program sets flag bits indicating various things such as "two alphabetic characters entered," or "have just seen a blank," etc. When debugging this code, I simply display the address (or register) containing the state flags on the front panel. Then, as I strike test keys one by one, I can immediately judge the program's reaction by examining the state flags. This technique can be used to monitor working programs as well. For example, I have a loader program which I use to download programs from other computers. It keeps the address currently being loaded in the HL register pair. By simply displaying this register pair, I can watch the load progress (or fail!).

A real time front panel can be used for more than just debugging. The presence of the displays and keypad provides another channel of communication with the processor, independent of the console terminal. The displays can be used to indicate any desired status, and the keypad can be used as a bank of "sense switches," even while the console is being used by the program. For example, the BASIC interpreter supports commands to control the displays and read the keypad.

Conclusions

The PAM/8 front panel system provides an inexpensive and effective "firmware front panel" which emulates a complete hardware front panel. Its design combines the capabilities of a true hardware panel with the flexibility of firmware and ultimately provides the user with a greater communications bandwidth to a personal computer.■

First Steps in Computer Chess Programming

Kathe and Dan Spracklen
10832 Macouba Pl
San Diego CA 92124

The fascination of chess gains a new dimension with microcomputer chess. No longer are the struggles confined to giant machines. With the advent of the Chess Mate, Chess Challenger, Boris, and Compuchess, as well as some custom software packages, the day of microcomputer chess has dawned. Writing a program to play chess on a small system is no small matter, though. Consider just for a start the challenge of meaningfully representing the board and its pieces in computer memory: there are 64 squares, 32 pieces, 6 piece types and 2 piece colors. Since the machine is a microcomputer, storage requirements must be kept to a minimum. Next comes the job of moving the pieces. Only when these first problems of piece representation and move generation have been solved can the chess programmer go on to consider strategy.

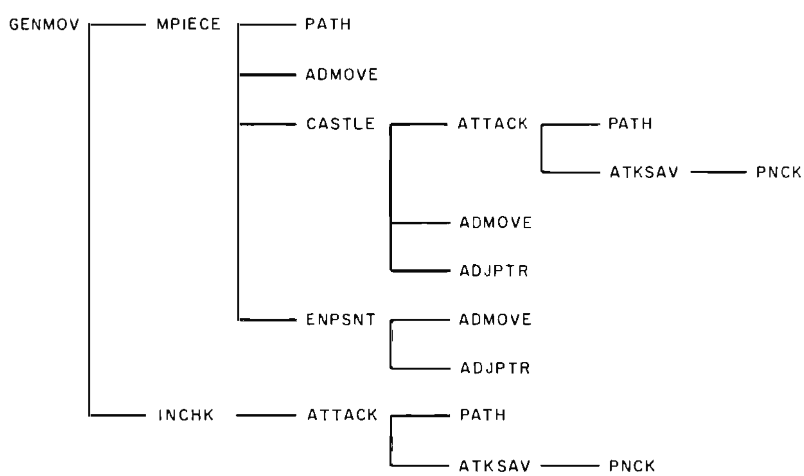

Figure 1: Block structure of the move generation routine of Sargon, the authors' chess playing program written for Z-80 assembler language.

Sargon, a chess playing program we developed for Z-80 machines, solves the representation problem through the use of a board array. Move generation is accomplished through a network of routines diagrammed in figure 1. The functions of the routines are as follows:

GENMOV	Generate move routine. Generates the move set for all of the pieces of a given color.
MPIECE	Piece mover routine. Generates the move set for a given piece.
INCHK	Check routine. Determines whether or not the King is in check.
PATH	Path routine. Generates a single possible move for a given piece along its current path of motion.
ADMOVE	Admove routine. Adds a move to the move list.
CASTLE	Castle routine. Determines whether castling is legal and adds it to the move list if it is.
ENPSNT	En passant routine. Tests for an en passant pawn capture and adds it to the move lists if it is legal.
ATTACK	Attack routine. Finds all the attackers on a given square.
ADJPTR	Adjust move list pointer. Links around the second move in a double move (ie: castle or en passant pawn capture).
ATKSAV	Attack save routine. Saves attacking piece value in the attack list and increments the attack count for that color piece.
PNCK	Pin check routine. Checks to see if an attacking piece is in the pinned piece list.

Several of the routines involved are multipurpose routines. Their involvement in move generation is incidental to a main function elsewhere in the move selection logic. The key routines in move generation are MPIECE, PATH, CASTLE and ENPSNT. Of these,

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(a)

110	111	112	113	114	115	116	117	118	119
100	101	102	103	104	105	106	107	108	109
90	91	92	93	94	95	96	97	98	99
80	81	82	83	84	85	86	87	88	89
70	71	72	73	74	75	76	77	78	79
60	61	62	63	64	65	66	67	68	69
50	51	52	53	54	55	56	57	58	59
40	41	42	43	44	45	46	47	48	49
30	31	32	33	34	35	36	37	38	39
20	21	22	23	24	25	26	27	28	29
10	11	12	13	14	15	16	17	18	19
0	1	2	3	4	5	6	7	8	9

(b)

6E	6F	70	71	72	73	74	75	76	77
64	65	66	67	68	69	6A	6B	6C	6D
5A	5B	5C	5D	5E	5F	60	61	62	63
50	51	52	53	54	55	56	57	58	59
46	47	48	49	4A	4B	4C	4D	4E	4F
3C	3D	3E	3F	40	41	42	43	44	45
32	33	34	35	36	37	38	39	3A	3B
28	29	2A	2B	2C	2D	2E	2F	30	31
1E	1F	20	21	22	23	24	25	26	27
14	15	16	17	18	19	1A	1B	1C	1D
A	B	C	D	E	F	10	11	12	13
0	1	2	3	4	5	6	7	8	9

Figure 2: Decimal (a) and hexadecimal (b) representations of the chessboard used in the Sargon program. Each square of the board is represented by a single byte in memory. Border squares are assigned a flag value of hexadecimal FF. The use of the border simplifies move generation, since it becomes easy to determine when a piece moves off the board.

MPIECE and PATH will be discussed here. The routines will be described in a language independent narrative. The Z-80 assembler code in which they are implemented will also be presented and exhaustively commented.

The Board in Memory

The chessboard in memory is an array of 120 bytes that can be visualized as in figure 2. Each square of the board is represented in memory by a single byte. Border bytes are assigned a flag value of hexadecimal FF. The border simplifies move generation, since it becomes easy to determine when a piece moves off the board.

The Pieces in Memory

Each piece is represented in memory by one byte of data. The meaning and function of the bits are as follows:

Bit 7 — color of the piece.
1 — Black
0 — White
Bit 6 — not used.
Bit 5 — not used.
Bit 4 — castle flag for Kings only. Set if the King has castled.
Bit 3 - moved flag. Set if the piece has moved.
Bits 2-0 . Piece type.
1 Pawn
2 Knight
3 Bishop
4 Rook
5 Queen
6 King

The pieces in play occupy squares of the board. If a board square is empty, it has the value 00. Thus the board set up for play would be as shown in figure 3.

Piece Mover Data Base

In order to generate moves for the pieces on the board, data must be maintained to describe the possibilities for each piece. This is accomplished through the use of three tables. Values for the tables are given in table 1.

DIRECT	Direction Table. Used to determine the direction of movement of each piece.
DPOINT	Direction Table Pointer. Used to determine where to begin in the direction table for any given piece.
DCOUNT	Direction Table Counter. Used to determine the number of directions of movement for any given piece.

FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
FF	84	82	83	85	86	83	82	84	FF
FF	81	81	81	81	81	81	81	81	FF
FF	00	00	00	00	00	00	00	00	FF
FF	00	00	00	00	00	00	00	00	FF
FF	00	00	00	00	00	00	00	00	FF
FF	00	00	00	00	00	00	00	00	FF
FF	01	01	01	01	01	01	01	01	FF
FF	04	02	03	05	06	03	02	04	FF
FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

Figure 3: Representation of the pieces on their home squares. Pieces are identified by means of unique byte values.

About the Authors

Dan and Kathe Spracklen are the creators of Sargon, the microcomputer chess program that won the microcomputer chess tournament at the 1978 West Coast Computer Faire. Dan Spracklen is a 13 year programming veteran. His experience ranges from scientific simulation programs to real time commercial applications. He is currently a senior applications analyst for Sperry-Univac. Kathe Spracklen is a graduate student in computer science at San Diego State University. An experienced tournament player, Kathe provided the chess background for Sargon.

Listing 1: The Sargon move generation routine, written in Z-80 assembly language.

```
;**********************************
; EQUATES
;**********************************
PAWN     =   1
KNIGHT   =   2
BISHOP   =   3
ROOK     =   4
QUEEN    =   5
KING     =   6
WHITE    =   0
BLACK    =   80H
BPAWN    =   BLACK+PAWN
```

Equate statements supply symbolic equivalents for the piece types and colors.

```
;**********************************
;TABLES SECTION
;**********************************
START:
```

Start is the first address in Sargon and should lie on an even 256 byte page boundary.

```
          .LOC    START+80H
TBASE     =       START+100H
```

Indexing in the Z-80 makes use of an address, contained in either the IX or IY index registers, plus a displacement. The displacement is a signed number +127 to −128. Thus a 256 byte area of memory centered on the index address is accessible. For this reason TBASE is placed in the middle of the tables section.

```
;**********************************
;DIRECT – DIRECTION TABLE
;**********************************
DIRECT    =       .–TBASE
```

The value of "." is the current program counter. Direct is now the displacement of the direction table from the table base. So if the value of TBASE is loaded in the IY index register, "DIRECT(Y)" will reference the first element in the direction table.

```
                .BYTE +09,+11,–11,–09
                .BYTE +10,–10,+01,–01
                .BYTE –21,–12,+08,+19
                .BYTE +21,+12,–08,–19
                .BYTE +10,+10,+11,+09

                .BYTE –10,–10,–11,–09
```

Diagonal directions used for Bishop, Queen, and King.
Rank and file directions used for Rook, Queen, and King.
Knight move directions.

White pawn directions including two forward moves and two diagonal moves for captures.
Black pawn directions.

```
;**********************************
;DPOINT-DIRECTION TABLE POINTER
;**********************************
DPOINT    =       .–TBASE
          .BYTE  20,16,8,0,4,0,0
```

Displacement from table base.
Starting point in direction table. In the order BP, WP, N, B, R, Q, K.

```
;**********************************
;DCOUNT-DIRECTION TABLE COUNTER
;**********************************
DCOUNT    =       .–TBASE
          .BYTE  4,4,8,4,4,8,8
```

Number of directions to use from table. In the same order as DPOINT.

```
;**********************************
;BOARD – BOARD ARRAY
;**********************************
BOARD     =       .–TBASE
BOARDA  .BLKB    120
```

The board array consists of 120 bytes in memory.

```
;**********************************
;TABLE INDICES SECTION
;**********************************
          .LOC    START+0
M1:       .WORD  TBASE
M2:       .WORD  TBASE
M3:       .WORD  TBASE
M4:       .WORD  TBASE
T1:       .WORD  TBASE
T2:       .WORD  TBASE
T3:       .WORD  TBASE
```

Uses the area of memory between START and START+80H. These indices are used to index into the various tables. Since TBASE is on an even boundary, its address is of the form XX00, where XX depends on the load address. The table address needed for a particular routine is formed by storing a one byte value in the 00 portion. Since addresses are stored in memory with the low order byte first, XX00 would be stored as 00XX. Then changing the 00 portion is simply a matter of storing a one byte value in the index.

```
;**********************************
;VARIABLES SECTION
;**********************************
P1:       .BYTE 0
P2:       .BYTE 0
P3:       .BYTE 0
```

Working storage area to hold the contents of the board array for a given square.

```
;**********************************
;PIECE MOVER ROUTINE
;**********************************
MPIECE:   XRA      M
```

Gets the piece to be moved into register A. In GENMOV, the routine which calls MPIECE, the piece value in register A, had been exclusive ORed with COLOR, the color of the piece to determine whether or not to call MPIECE. Another exclusive OR restores the piece.

```
          ANI      87H
```

This clears all the flag bits and leaves just piece type and color.

```
          CPI      BPAWN
```

Is it a Black pawn?

Listing 1, continued (Listing 1 is concluded on page 95):

	JRNZ	MP2	No–Skip.
	DCR	A	Decrement, making piece type a 0 for a Black pawn.
MP2:	ANI	7	Clears color bit and leaves just the piece type.
	STA	T1	This is the first step in forming the index into DPOINT and DCOUNT. T1 contains the value of TBASE (XX00) stored in low-high order (00XX). After storing the piece type (0–6) in T1, it contains the address of TBASE + TYPE.
	LIYD	T1	This operation loads the entire TBASE + TYPE address into the IY index register.
	MOV	B,DCOUNT(Y)	DCOUNT is the displacement from TBASE to the start of the direction count table. So DCOUNT + TBASE is the starting address of the direction count table. Then DCOUNT(Y) is: DCOUNT + CONTENTS IY Register = DCOUNT + TBASE + TYPE (0–6) = START OF TABLE + TYPE (0–6) This move instruction pulls the direction count for the given piece type and places it in register B.
	MOV	A,DPOINT(Y)	Similarly, this instruction pulls the direction table pointer for the given piece type and places it in register A.
	STA	INDX2	The direction table pointer will be used to index into the direction table.
	LIYD	INDX2	
MP5:	MOV	C,DIRECT(Y)	Gets the direction and places it in register C.
	LDA	M1	Gets the "from" position which was stored in M1 in GENMOV.
	STA	M2	Save in M2 to form the address of the current position.
MP10:	CALL	PATH	Generate a single move in the given direction.
	CPI	2	Did the moving piece encounter a piece of the same color, or is new position off the board?
	JRNC	MP15	Jump if yes to either question. No move to add to move list. Ready for new direction.
	ANA	A	Was the square moved to empty?
	EXAF		Save the answer to this question by swapping flag register for alternate flag register.
	LDA	T1	Get type of moving piece.
	CPI	PAWN+1	Is it a pawn?
	JRC	MP20	If so, jump to special pawn handling logic. PAWN+1 is equal to the number 2. A White pawn would be of type 1 while a Black pawn would have type set to 0. In either case the carry flag would be set upon a comparison to a value of 2.
	CALL	ADMOVE	Valid move, so add it to the move list.
	EXAF		Restore the answer to the empty square question.
	JRNZ	MP15	If it is not empty, go get ready for next direction. No further moves are possible in this direction.
	LDA	T1	Get piece type. Some pieces may only make one move in a given direction.
	CPI	KING	The King is such a piece. Is this piece a King?
	JRZ	MP15	If so, go get ready for a new direction.
	CPI	BISHOP	Compare piece type to a Bishop.
	JRNC	MP10	If piece type is bishop or greater (ie: Bishop, Rook, or Queen) go make another move in this same direction.
MP15:	INX	Y	Increment direction index for next direction in the direction table.
	DJNZ	MP5	Decrement the direction count (in register B). If count is not yet 0, go back and repeat this process for the new direction. Otherwise all of the directions have been considered.
	LDA	T1	Fetch piece type again.
	CPI	KING	Is it a King?
	CZ	CASTLE	If so, call castle to add it to the move list if legal.
	RET		Return to GENMOV.
;***********PAWN LOGIC************			
MP20:	MOV	A,B	Get the number of move directions left to consider. If this is the first direction, register A=4.
	CPI	3	Are there three directions left to look at?
	JRC	MP35	A carry on this compare indicates a diagonal move. If so, branch to diagonal logic.
	JRZ	MP30	Equality on this compare indicates a forward move of two squares. Branch to check for legality.
	EXAF		Otherwise this is a forward move of one square. Restore the answer to the empty square question.
	JRNZ	MP15	If the square is not empty, this is not a valid move. Go check the next direction.
	LDA	M2	Get the "to" position of the move.
	CPI	91	Is it on the last rank and therefore a promotion of a White pawn?
	JRNC	MP25	If so, go set promotion flag.
	CPI	29	Otherwise, is it on the first rank and therefore a promotion of a Black pawn?
	JRNC	MP26	If no, skip setting flag.
MP25:	LXI	H,P2	Load the address of the promotion flag.
	SET	5,M	Set the flag (bit 5 of P2).

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The subroutines in Sargon that handle the actual move generation rely heavily on the indexing capabilities of the Z-80 microprocessor. For this purpose several sets of indices are maintained to access elements of the tables. The piece mover routines depend especially on the following groups of indices.

M1–M4	Working indices used to index into the board array.
T1–T3	Working indices used to index into direction count, direction value, and piece value tables.
INDX1 INDX2	General working indices. Used for various purposes.

Variables and constants used in the routines PATH and MPIECE include:

PAWN	= 1	(Identification of the piece types is made through use of equate statements. Numbers are hexadecimal.)
KNIGHT	= 2	
BISHOP	= 3	
ROOK	= 4	
QUEEN	= 5	
KING	= 6	
WHITE	= 0	
BLACK	= 80	
BPAWN	= Black + pawn	
P1–P3	= Working area to hold the contents of the board array for a given square.	

DPOINT *(a)*

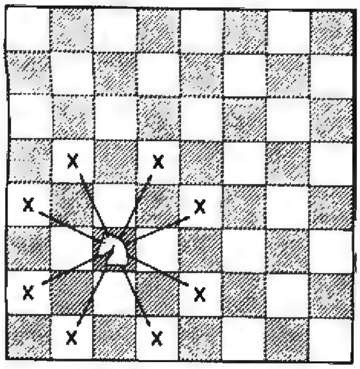
0	+09	+11	−11	−09
4	+10	−10	+01	−01
8	−21	−12	+08	+19
12	+21	+12	−08	−19
16	+10	+10	+11	+09
20	−10	−10	−11	−09

(b)

Piece Type	DPOINT	DCOUNT
Black Pawn	20	4
White Pawn	16	4
Knight	8	8
Bishop	0	4
Rook	4	4
Queen	0	8
King	0	8

Table 1: Direction table (a) and direction table pointer and counter (b). In order to generate moves for the chess pieces, data describing the possibilities for each piece is kept in table 1a. Table 1b shows the direction table pointer, which tells where to start in the table for a given piece, and the direction table counter, which determines the number of directions of movement for a given piece.

KNIGHT BEGINS AT WHITE'S QB3
DECIMAL BOARD ARRAY INDEX = 43



Direction Table Values	Direction Calculation	New Board Array Index	Resulting Square
−21	43 − 21	22	QN1
−12	43 − 12	31	QR2
+08	43 + 08	51	QR4
+19	43 + 19	62	QN5
+21	43 + 21	64	Q5
+12	43 + 12	55	K4
−08	43 − 08	35	K2
−19	43 − 19	24	Q1

Figure 4: Generating all the possible Knight moves from the Queen Bishop 3 (QB3) square. The Knight is piece type 2 (see text) and has a DPOINT (direction table pointer) value of 8 and a DCOUNT (direction table counter) value of 8 also. So in generating the Knight's moves, DIRECT+8 will be the starting point in the direction table, and 8 values will be used: −21, −12, +08, +19, +21, +12, −08 and −19. The Knight starts at White's QB3 square, which is square 43 (see figure 2a, decimal representation). Thus the first possible Knight move is 43 − 21 = 22 (QN1), and so on.

Sample Move Generation

Suppose a Knight occupies the QB3 square. A Knight is piece type 2 and has a DPOINT of 8 and a DCOUNT of 8 (see table 1b). So in generating the Knight's moves, DIRECT + 8 will be the starting point in the direction table and 8 values will be used. Those values are −21, −12, +08, +19, +21, +12, −08, and −19. The Knight starts at White's QB3, which is square 43 (see figure 2a, decimal representation). Thus the first possible Knight move is 43 − 21 = 22. Now 22 is QN1, so the first Knight move returns the Knight to its starting square. Figure 4 summarizes all possible Knight moves from QB3.

Move Generation—The Algorithms Explained

Move generation is controlled by GENMOV, which scans the board array and calls MPIECE for each piece encountered.

Then MPIECE, the piece mover routine, generates all possible legal moves for that piece (moves that place the King in check are eliminated later in the program). The piece is brought in from memory. It is a one byte data value, as previously discussed, which contains piece type, flags and color. The flags are deleted from the piece before checking for type. Basic piece types are indicated by values from 1 to 6. Except for pawns, White and Black pieces move alike. So a special case is needed for the Black pawn. If the given piece is a Black pawn, the piece type is decremented, making it type 0.

The type of the piece, now one from 0 to 6, is used as an index into the DCOUNT, direction table count, and DPOINT, direction table pointer arrays. The values for the given piece are fetched. The direction table pointer is then used as an index into DIRECT, the direction table, and the first move direction is fetched. The "from" position of the piece is the square on which the piece currently stands. This "from" board index and the direction table value are passed as parameters to the routine PATH.

PATH generates the move indicated and returns a flag which describes the status of the "to" position of the piece. Flag values are:

- 0 "to" position is empty.
- 1 "to" position contains a piece of the opposite color.
- 2 "to" position contains a piece of the same color.
- 3 "to" position is off the board.

PATH accomplishes its task by fetching the "from" position, adding the direction counter, and storing the result as the "to" position. It then uses the "to" position to form an index into the board array. The current contents of the square are fetched. If the square contains hexadecimal FF, it is off the board. The off board flag is set and control is returned to MPIECE.

If the square is on the board, the contents of the square are saved in memory location P2. The color and flag bits are then cleared and the remaining piece type is saved in T2. If the square is empty, control is returned to MPIECE with the flag value still set to 0. Otherwise the color of the piece on the "to" square is compared with that of the moving piece. The appropriate flag is set to indicate whether or not the pieces are of the same color, and control is returned to MPIECE.

Upon return from PATH, piece mover

checks to see if the square is occupied by a piece of the same color or is off the board. If so, this cannot be a legal move, so a check for further moves must follow a new direction. Otherwise a check is made to see if the square is empty. The answer is saved. A check is made to see if the piece being moved is a pawn. If so, control is passed to the special pawn logic. Otherwise the move generated must be added to the move list. ADMOVE is called for the job. After the move has been added to the move list, the answer to the empty square question is recovered. If the square is empty and the piece is a Bishop, Rook, or Queen, it is possible to continue moving in the same direction. In this case control passes back to the call to PATH for another move in that direction. Kings and Knights may make only one move in a given direction.

When the time comes to consider a new direction of movement for the piece, the index into the direction table is incremented. DCOUNT, the number of directions to con-

Listing 1, continued:

```
MP26:   CALL    ADMOVE      Add this move to the move list.
        INX     Y           Increment direction index for two square move direction.
        DCR     B           Decrement the direction count.
        LXI     H,P1        Load the address where the piece was saved.
        BIT     3,M         Check the flag in the piece which tells whether it has moved
                            before.
        JRZ     MP10        If the pawn has never moved, go generate a second forward
                            move. (The pawn can move two squares on the first move.)
        JMP     MP15        Otherwise go get new direction, skipping second forward
                            move.
;********MOVE OF 2 SQUARES********
MP30:   EXAF                Restore the answer to the empty square question.
        JRNZ    MP15        If the square is not empty, this is not a valid move. Go check
                            the next direction.
MP31:   CALL    ADMOVE      Otherwise add this move to the move list.
        JMP     MP15        Go check the next direction.
;*********DIAGONAL MOVE**********
MP35:   EXAF                Restore the answer to the empty square question.
        JRZ     MP36        If the square is empty, it is not a normal pawn capture.
                            Go try en passant.
        LDA     M2          Get the "to" position of the move.
        CPI     91          If the board index is 91 or greater, this is the last rank and
                            a White pawn promotion.
        JRNC    MP37        If so, go set promote flag.
        CPI     29          Otherwise, if the board index is less than 29, this is the first
                            rank and a Black pawn promotion.
        JRNC    MP31        If not, just go add the move to the move list.
MP37:   LXI     H,P2        Load the address of the promotion flag.
        SET     5,M         Set the flag (bit 5 of P2), and go add the move to the move
        JMPR    MP31        list.
;*****DIAGONAL SQUARE EMPTY *****
MP36:   CALL    ENPSNT      Check for possible en passant capture and add it to the
                            move list if legal.
        JMP     MP15        Go check the next direction.
;***********************************
;PATH ROUTINE
;***********************************
PATH:   LXI     H,M2        Get the address of the location where the "from" position
                            was stored.
        MOV     A,M         Get the "from" position from that memory location.
        ADD     C           Add in the direction from the direction table, giving the
                            "to" position.
        MOV     M,A         Use "to" position to form an index into the board array.
        LIXD    M2          Load the board index.
        MOV     A,BOARD(X)  Get the contents of the board at the "to" square.
        CPI     0FFH        Is the "to" position off the board?
        JRZ     PA2         If so, go set off-board flag.
        STA     P2          Save contents of the board at "to" square.
        ANI     7           Isolate piece type.
        STA     T2          Save piece type.
        RZ                  Return if the square is empty. The flag value is returned in
                            the A register and it is already 0.
        LDA     P2          Get piece again.
        LXI     H,P1        Load the address of the moving piece.
        XRA     M           Compare the pieces.
        BIT     7,A         Check to see if the colors match. If so, after the exclusive
                            OR the color bit will be 0.
        JRZ     PA1         If they match, go set match flag.
        MVI     A,1         Otherwise, set different color flag and return.
        RET
;***********SAME COLOR************
        MVI     A,2         Set same color flag and return.
        RET
;************OFF BOARD************
        MVI     A,3         Set off-board flag and return.
        RET
```

sider, is decremented. When DCOUNT reaches zero, all the moves for the piece have been generated. If the piece involved is the King, a call to castle will add any legal castling moves. Then control is returned to GENMOV.

All that remains is to discuss the special pawn logic. Pawns are peculiar in that they capture diagonally, but move straight ahead. They also have the option of moving one or two squares forward on their first move. Furthermore, if they reach the eighth and final rank, they may be promoted to another piece. Sargon always promotes its own pawns to Queens. A flag in variable P2 indicates pawn promotion.

The pawn logic in MPIECE first checks to see if the direction of movement is along a diagonal. If so, the square must be occu-

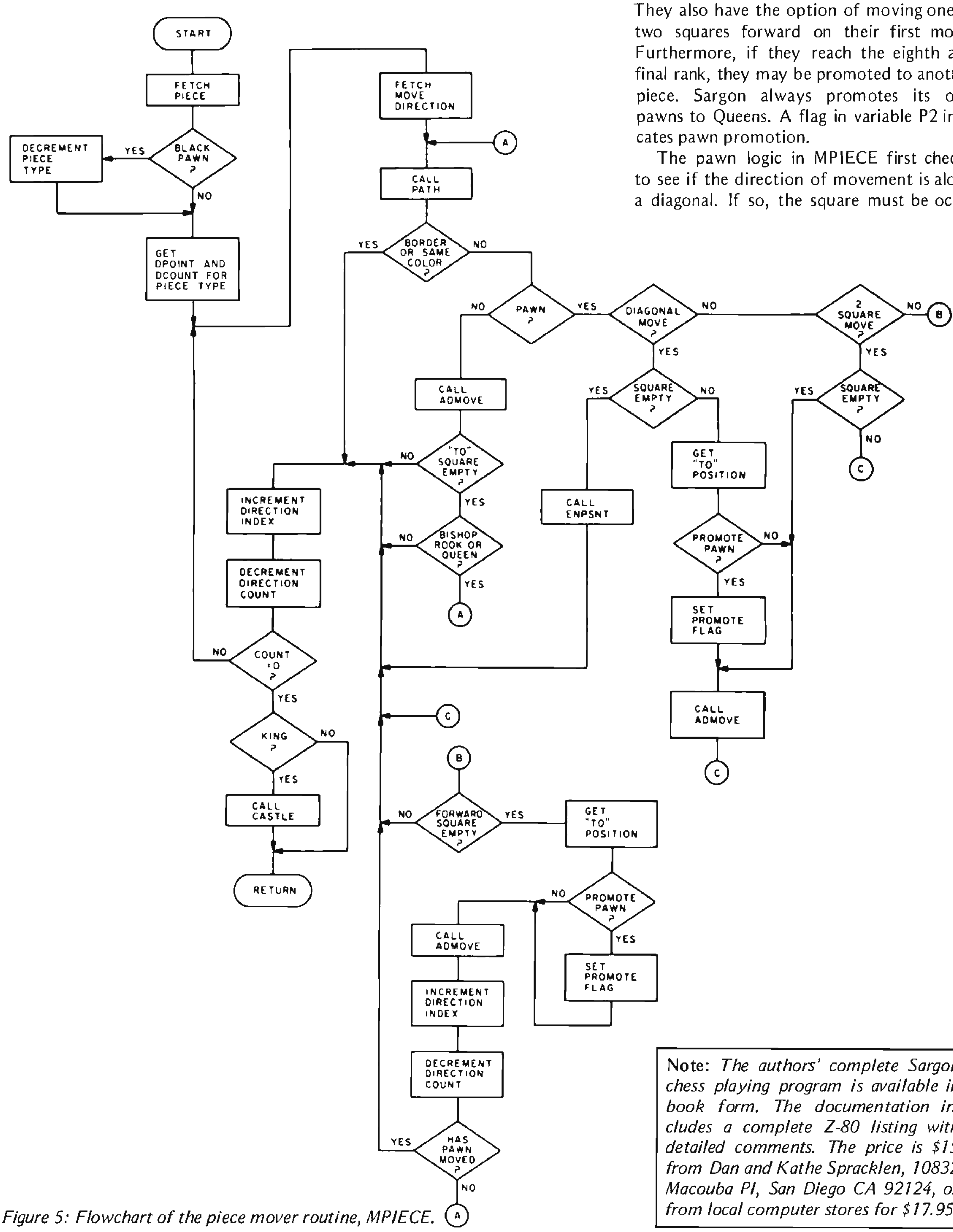


Figure 5: Flowchart of the piece mover routine, MPIECE.

Note: *The authors' complete Sargon chess playing program is available in book form. The documentation includes a complete Z-80 listing with detailed comments. The price is $15 from Dan and Kathe Spracklen, 10832 Macouba Pl, San Diego CA 92124, or from local computer stores for $17.95.*

pied by an enemy piece. It may also be possible to move to the eighth rank in capturing, so pawn promotion must be considered here as well. Another type of diagonal pawn move is the *en passant* capture. It must be considered by a call to ENPSNT. Finally it is time to consider a new direction, as is done for the other piece types.

If, however, the direction of movement is forward, the "to" square must be empty. Pawn promotion must be checked for on forward moves. If the piece has never moved before, another move in the same direction is a possibility. Otherwise it is time to consider a new direction. Figures 5 and 6 are flowcharts of MPIECE and PATH, respectively.

The Other Move Generation Routines

The move generation driver is GENMOV, the generate move routine. The basic function of GENMOV is to generate the move set for all pieces of a given color. It scans the board checking for a piece of the same color and calls MPIECE, the piece mover routine.

CASTLE and ENPSNT are also key routines in move generation. CASTLE checks the legality of both King side and Queen side castling. It adds them to the move list if legal. Basic checks must include:

- Has King moved?
- Is King in check?
- Has Rook moved?
- Are the intervening squares empty?
- Are any squares that the King passes through under attack?

ENPSNT checks for any en passant pawn captures and adds them to the move list if legal. The tests must include:

- On the fifth rank?
- Was previous move the first move for the enemy pawn?
- Is the enemy pawn on an adjacent file?

INCK, the check routine, performs the function of determining whether or not the King is in check. The basic method used is to scan outward from the King looking for attackers, by calling ATTACK.

The attack routine finds all attackers on a given square by scanning outward from the square until one of the following occurs:

- A piece is found that attacks this square.
- A piece is found that doesn't attack this square.
- The edge of the board is reached.

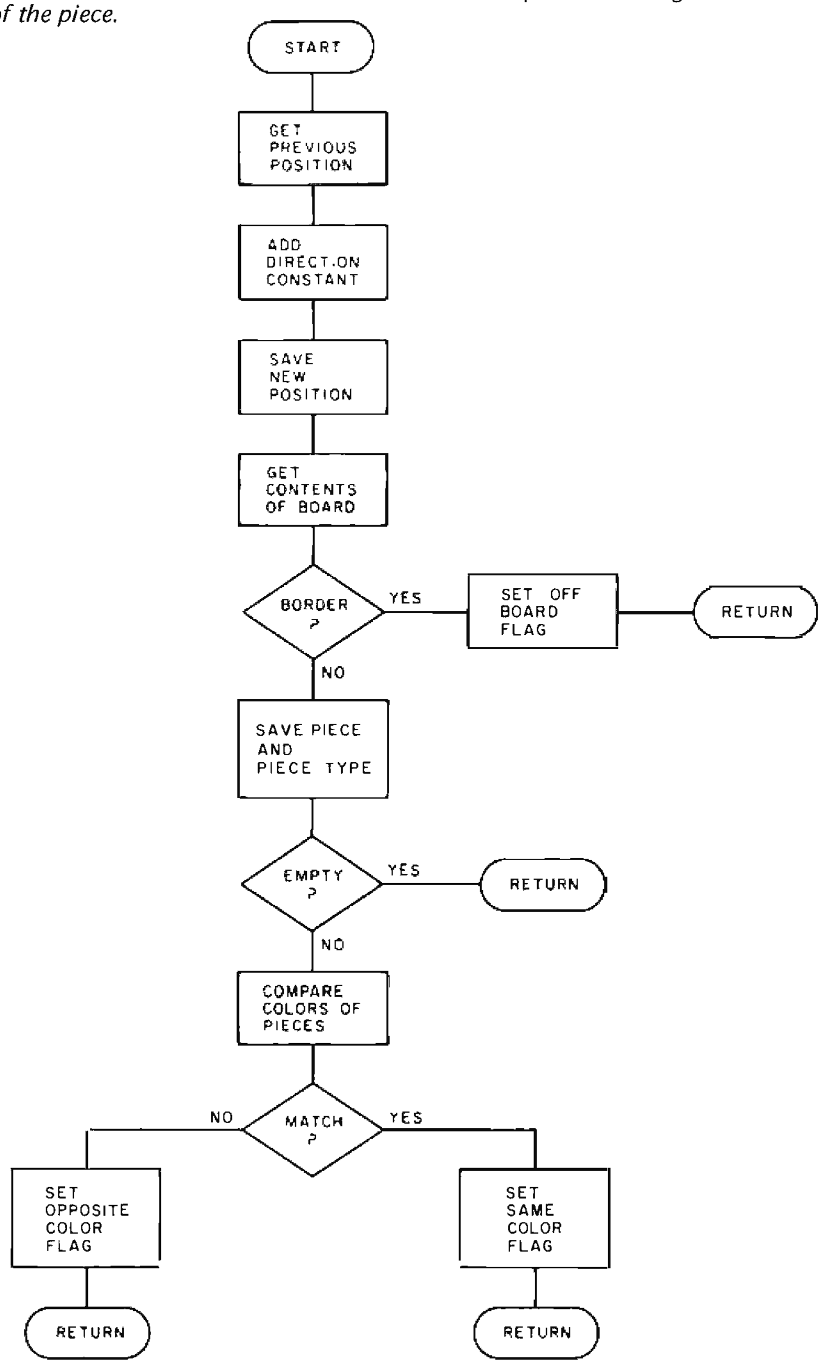
Note: *Next month the authors discuss their Sargon Exchange Evaluator.*

In the case where this routine is called by CASTLE or INCHK, the routine is terminated as soon as an attacker of the opposite color is encountered.

ADMOVE adds a move to the move list. The move list is a linked list. Each move in the move list is stored in a 6 byte area. The meaning of each byte is as follows:

0&1	MLPTR – Move list pointer. A pointer to the next move in the move list. Used to facilitate sorting the list.
2	MLFRP – Move list from position. The board position from which the piece is moving.
3	MLTOP – Move list to position. The board position to which the piece is moving.
4	MLFLG – Move list flags.
5	MLVAL – Move list value. Contains the score assigned to the move in evaluation.

Figure 6: Flowchart of the PATH routine, which performs the actual move of the piece.



It is hoped that this introductory discussion will assist potential chess programmers in getting started. With the essentials of move generation out of the way, the fun part of evaluation can begin. ■

BIBLIOGRAPHY

In writing Sargon, it was our original intention to put together the first version without any research into the attempts made by others. In this respect Sargon is a unique creation. After competing in the Second West Coast Computer Faire, we began to investigate some of the literature. This bibliography presents some of the references we found most helpful, together with our evaluations.

1. Michie, Donald, *On Machine Intelligence,* Edinburg University Press, 1974.
   Michie's book provides an excellent treatment of exchange evaluation. He uses the concept of an exchange polynomial for accurately determining the outcome of battles engaged on the board. The basic approach we used in XCHNG, the Sargon exchange evaluator, turned out to be surprisingly similar. Sargon's approach, however, is far less computationally complex. We highly recommend this reference to anyone planning to write a chess program without look-ahead.

2. Samuel, A L, "Some Studies in Machine Learning Using the Game of Checkers. 11-Recent Progress," *IBM Journal,* November 1967.
   Samuel provides a complete though sometimes difficult treatment of alpha-beta pruning. One of the few articles we encountered before writing Sargon, Samuel's article is the basis for the tree search used in the Sargon program.

3. Fine, Reubin, *Ideas Behind the Chess Openings,* David McKay, New York, 1943.
   Fine's book makes a great starting point for anyone contemplating the addition of an opening book. Although Fine does not present enough lines of play for a complete book, it does provide a good orientation to other references.

4. Chernev, Irving, *Practical Chess Endings,* Dover Publications, New York, 1961.
   Perhaps the greatest weakness we've seen in microcomputer chess programs is the play of the endgame. Chernev's book presents a marvelously readable introduction to this phase of the game.

5. Kmoch, Hans, *Pawn Power in Chess,* D McKay Company, New York, 1959.
   Alas, too many microcomputer chess programs shoot out pawns like photon torpedoes. Kmoch provides an excellent introduction to what constitutes good pawn structure.

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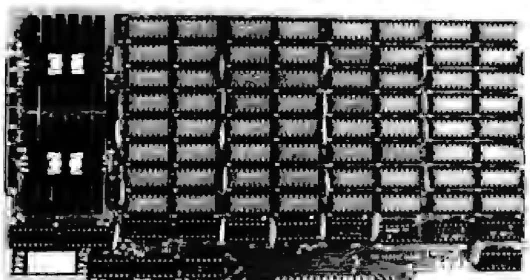

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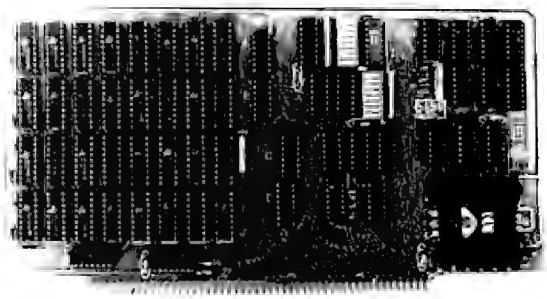

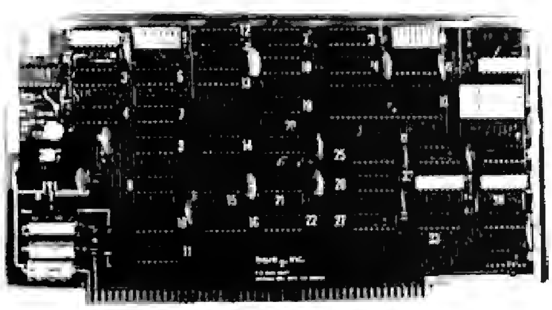

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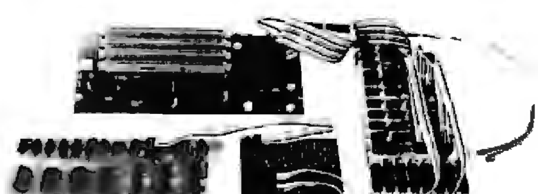

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Linear Circuit Analysis

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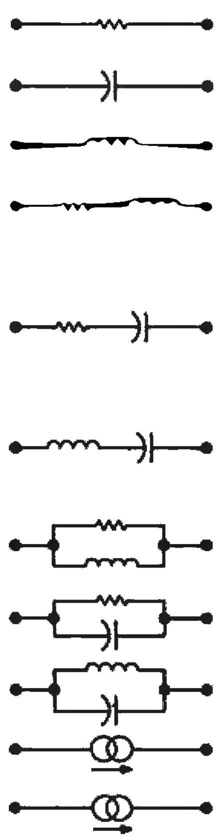
Editor's Note:

Readers wishing to obtain more details about the electrical concepts discussed in this article will find a concise treatment of complex impedance and related topics in The Radio Amateur's Handbook *published by the American Radio Relay League, Newington CT 06111. For a good programmed learning introduction to electricity and DC circuits, see* Basic Electricity and DC Circuits *by Oliva and Dale, published by Texas Instruments Inc, POB 5012, Dallas TX 75222.*

R = entered resistance in ohms.
L = entered inductance in henries.
C = entered capacitance in farads.
I = entered current in amperes.
F = solution frequency in hertz.



Branch Type	Plus Node	Minus Node	Calculation of Admittance
Resistor			$Y = (1/R) + j0$
Capacitor			$Y = 0 + j(2\pi FC)$
Inductor			$Y = 0 - j[1/(2\pi FL)]$
Series RL			$Y = R/(R^2 + X^2) - j[X/(R^2 + X^2)]$ $X = 2\pi FL$
Series RC			$Y = R/(R^2 + X^2) + j[X/(R^2 + X^2)]$ $X = 1/(2\pi FC)$
Series LC			$Y = 0 + j[X/(1 - 2\pi FLX)]$ $X = 2\pi FC$
Parallel RL			$Y = (1/R) - j[1/(2\pi FL)]$
Parallel RC			$Y = (1/R) + j(2\pi FC)$
Parallel LC			$Y = 0 + j[(2\pi FC) - (1/2\pi FL)]$
Current generator			$Y = I + j0$
Current generator with θ			$Y = I\text{cosine}(\theta) + j[I\text{sine}(\theta)]$

Table 1: Admittance calculations for simple branches. On both of the generators the direction of electron flow is shown by the arrow.

Circuit analysis programs are valuable tools that can tell you how a circuit *will* work before you build it — "paper breadboards" in effect that don't require any component purchases, expensive equipment or debugging time spent on the bench. Analysis programs fall into two general categories: frequency domain and time domain. Presented here are the fundamentals of a frequency domain *linear* analysis program. In practice, linear analysis means that no active devices are operated at saturation or cutoff. Frequency domain tells us what circuits do at different frequencies, a type of analysis well-suited to model amplifiers, filters and operational amplifier circuits operating over any desired frequency range. You can make voltage and impedance readings at any point in the circuit without experiencing the loading problems that can occur with conventional equipment.

Because of the variations in small computer systems, primarily in memory, no specific language is given. All of the necessary flowcharts are presented along with necessary mathematical operations. You will need the four basic floating point functions plus array handling (single dimension arrays are acceptable, but two-dimensional arrays are preferred) and at least arctangent and logarithmic functions.

Matrix operations are done but you don't need BASIC MAT functions; the matrix is fully explained later. Using charts and explanations, you can write the program in any form from assembler to BASIC and higher languages. Assembler will work faster since this is a "number crunching" program. The main constraints are memory and the ability to hold many arrays in main memory.

Modeling the Circuit

Each component of a circuit with two connections is called a *branch*. Connection points are called *nodes*. Several branches can be connected to the same node. Signal sources are also branches; these have specific requirements in node descriptions and are covered later.

Table 1 shows the basic branch types with only two nodes. The complex number

Circle 318 on inquiry card.

admittance value is also given; the program is required to calculate the admittance as part of analysis.

Review of Complex Numbers

If you are unfamiliar with complex number notation or admittance, some review is necessary before beginning any programming. Complex numbers exist in either *rectangular* or *polar* form; rectangular form is used here. This requires two floating point numbers for every complex number. The lefthand number is called the *real* component and the righthand number, separated by the j, is called the *imaginary* component. Don't let the imaginary term fool you — it is very real. The naming comes from mathematical notation. [*Note that electronics applications use j instead of the mathematical symbol i to avoid confusion with the symbol for current* . . . BWL]

Admittance is the reverse of impedance. You may be more familiar with impedance and the notation:

$$Z = R + jX$$

with X being *reactance,* either positive or negative. Admittance is:

$$Y = G + jB$$

with G being *conductance* and B *susceptance,* either positive or negative. The relationship $Y = 1/Z$ is true but there are special rules governing complex number mathematics. These rules are summarized in the text box on complex number arithmetic.

The circuit to be analyzed is converted into a model for the computer by copying each component as a branch. Each branch has two node numbers corresponding to connections in the circuit. All nodes above ground must have sequential numbering, beginning with 1, but the node numbers may be in arbitrary positions. A ground node is signified by 0.

A complete set of branch descriptions comprises a circuit list. The circuit list we use requires three integer values and two floating point values to completely define a node. The three integer values are for the connections to other nodes and for indicating what number node we are presently at. The two floating point values define the complex admittance of the branch. To be useful, the minimum number of branches available should be at least 20.

You will notice that signal sources are currents and not voltages. This and use of admittances are deliberate in the solution of a node voltage. Consideration of node voltage solutions is important for our analysis.

Fundamental Circuit Matrix

A simple resistor network is shown in figure 1. This circuit can be analyzed quickly using pencil and paper, but will serve to show the mechanism of solutions. Keeping this circuit in mind, inspect the general

Complex Number Arithmetic

The rules for rectangular *form arithmetic are shown in the table below. Note that division and inversion have equal value denominators for both real and imaginary parts. Finding the denominator first in the division routine will increase computational speed. Note also that inverting (C + jD) is equal to dividing (A + jB) by (C + jD) and setting A at unity and B at zero.*

Actual test equipment such as oscilloscopes present magnitude and phase angle. This is the polar form, and conversion is as follows:

Given rectangular form A + jB,
magnitude = MAGN = A + B and
phase angle = PHA = (B/A).

Conversion from polar to rectangular form is:

Given polar form MAGN at angle PHA,
real part = MAGN x cosine (PHA) and
imaginary part = MAGN x sine (PHA).

Trigonometric functions in the language will determine whether angles are in radians or degrees. Most are in radians. The conversion factor from radians to degrees is:

Degrees = 57.29577951 x radians.

Given Complex Numbers of (A + jB) and (C + jD)

Addition:

$$(A + jB) + (C + jD) = (A + C) + j(B + D)$$

Subtraction:

$$(A + jB) - (C + jD) = (A - C) + j(B - D)$$

Multiplication:

$$(A + jB) \times (C + jD) = (AC - BD) + j(AD + BC)$$

Division:

$$\frac{(A + jB)}{(C + jD)} = \left[\frac{AC + BD}{C^2 + D^2}\right] - j\left[\frac{AD - BC}{C^2 + D^2}\right]$$

Inversion:

$$\frac{1}{(C + jD)} = \left[\frac{C}{C^2 + D^2}\right] - j\left[\frac{D}{A^2 + D^2}\right].$$

Summary of complex arithmetic used for analysis.

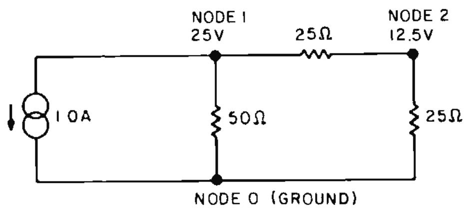


Figure 1: Simple resistive network with a current generator. The direction of the electron flow from the generator is indicated by an arrow. Note that nodes are numbered sequentially.

Matrix Representation

$$\begin{bmatrix} Y_{1,1} & Y_{1,2} & Y_{1,3} & Y_{1,4} & \cdots & Y_{1,N} \\ Y_{2,1} & Y_{2,2} & Y_{2,3} & Y_{2,4} & \cdots & Y_{2,N} \\ Y_{3,1} & Y_{3,2} & Y_{3,3} & Y_{3,4} & \cdots & Y_{3,N} \\ Y_{4,1} & Y_{4,2} & Y_{4,3} & Y_{4,4} & \cdots & Y_{4,N} \\ \cdot & \cdot & \cdot & \cdot & \cdots & \cdot \\ Y_{N,1} & Y_{N,2} & Y_{N,3} & Y_{N,4} & \cdots & Y_{N,N} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \\ \cdot \\ E_N \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ \cdot \\ I_N \end{bmatrix}$$

Simultaneous Equations

$$\begin{array}{l} Y_{1,1}E_1 + Y_{1,2}E_2 + Y_{1,3}E_3 + Y_{1,4}E_4 + \ldots Y_{1,N}E_N = I_1 \\ Y_{2,1}E_1 + Y_{2,2}E_2 + Y_{2,3}E_3 + Y_{2,4}E_4 + \ldots Y_{2,N}E_N = I_2 \\ Y_{3,1}E_1 + Y_{3,2}E_2 + Y_{3,3}E_3 + Y_{3,4}E_4 + \ldots Y_{3,N}E_N = I_3 \\ Y_{4,1}E_1 + Y_{4,2}E_2 + Y_{4,3}E_3 + Y_{4,4}E_4 + \ldots Y_{4,N}E_N = I_4 \\ \quad \cdot \qquad \cdot \qquad \cdot \qquad \cdot \qquad \cdot \qquad \cdot \\ Y_{N,1}E_1 + Y_{N,2}E_2 + Y_{N,3}E_3 + Y_{N,4}E_4 + \ldots Y_{N,N}E_N = I_N \end{array}$$

Figure 2: Matrix and simultaneous representations of any circuit. In the figure, and also in the text, the following conventions hold:
Y := circuit branch admittance
E := circuit node voltage
I := circuit node current
The circuit branch admittance is determined by the node description.

Branch Type	Matrix Array Subscripts: Row	Column	Enter into Array by
Passive	Plus node	Plus node	Addition
	Plus node	Minus node	Subtraction
	Minus node	Minus node	Addition
	Minus node	Plus node	Subtraction
Generator	Plus node	NMAX + 1	Addition
	Minus node	NMAX + 1	Subtraction

Table 2: Matrix insertion subscript rules for branches. Any row and column node combination that contains a zero will not enter the matrix. NMAX is the maximum node number in the circuit. Remember that the nodes must be numbered sequentially.

matrix and simultaneous equations given in figure 2.

The mathematical matrix form and the simultaneous equations form are identical. Mechanizing the solution will require parts of both forms. Admittance subscripts will depend on node numbers (in the branch list) and follow certain rules depending on type. Those rules are given in table 2.

The simple example, expressed in the general equations of figure 2 is:

$$Y_{1,1}E_1 + Y_{1,2}E_2 = I_1 \qquad (1)$$

$$Y_{2,1}E_1 + Y_{2,2}E_2 = I_2 \qquad (2)$$

The conductance of 50 ohms is 0.02 mho, 25 ohms is 0.04 mho. [*The* mho *is a unit of conductance, the inverse of the* ohm. *The* mho *is also called the* siemens . . . CM] Using only the real parts of admittance and following the rules of table 2 yields the numeric forms:

$$0.06\,E_1 - 0.04\,E_2 = 1.0 \qquad (1A)$$

$$-0.04\,E_1 + 0.08\,E_2 = 0 \qquad (2A)$$

Solving for E_2 can be done by multiplying equation (1A) by 2/3 and adding the product to equation (2A) to give:

$$0.05333\,E_2 = 0.66667$$

$$E_2 = 12.5$$

Substitution of E_2 into equation (1A) gives:

$$0.06\,E_1 - 0.50 = 1.0$$

$$E_1 = 1.50/0.06$$

$$E_1 = 25$$

The preceding straightforward mathematics becomes impractical for models with many nodes. Note that the subscript rules of table 2 are different than the example just given. A slightly different matrix arrangement is actually used.

Fundamental Properties of Matrices

Mechanization of the solutions requires a matrix in two dimensions having N rows and N+1 columns, N being the highest node number in the model. The first subscript is the row, and the second is the column position. The rightmost column is used only for signal sources.

Figure 3 shows the example represented

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BASIC-E Compiler

Designed to work with CP/M Disk Operating System this software requires a total of 20K bytes of memory. Included are 26 compiler error messages and 23 run-time error messages. Disk files may be read, written or updated by using both sequential and random access. Included are blocked and unblocked files. Price for compiler and run-time monitor on diskette is $10.00. Manual is available separately for $5.00. (Public domain software by Gordon E. Eubanks, Jr.).

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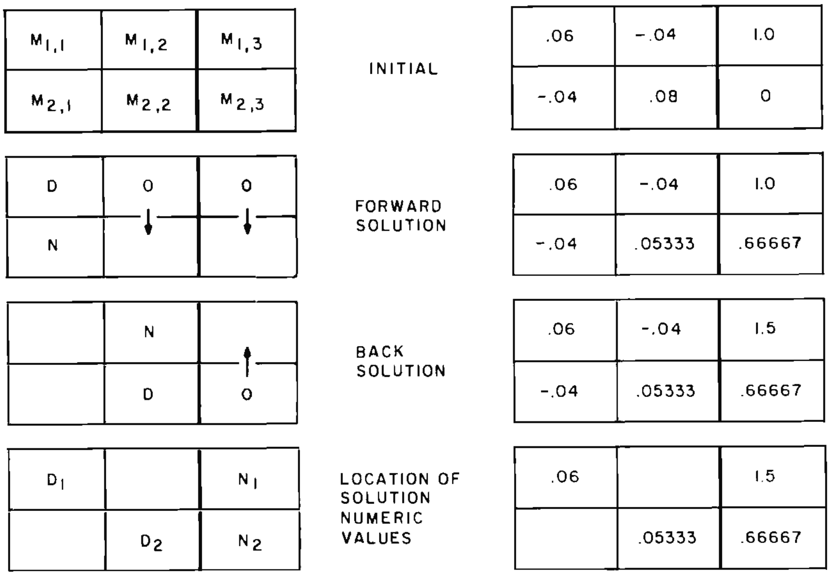

Figure 3: Graphical representation of a matrix solution to the simple example given in the text. Solutions are found at both of the nodes. The denominator of the solution is always found in the main diagonal, and the numerator of the solution is found in the generator column.

by an array of two rows (maximum node number is 2) by three columns. Variable name M has been used for any matrix position. At the beginning of a solution all Ms are set to 0. The branch list is then inspected, values calculated and added or subtracted into the matrix array positions according to the rules of table 2.

The variable N is used to denote a numerator value. D denotes a denominator value of a multiplying factor. A circle indicates that the array variable is multiplied by the factor; an arrowhead indicates that the product is subtracted from the array position. Only arrowhead marked positions are changed; all others are extracted and held in temporary storage.

Numeric values in figure 3 are the same as our simple example. The forward operation has these steps:

$$\text{Multiplication factor} = \left(\frac{M_{2,1}}{M_{1,1}}\right) = -0.66667.$$

$$\text{New } M_{2,2} = M_{2,2} - (\text{MULT.FACT} \times M_{1,2}) = 0.05333$$

$$\text{New } M_{2,3} = M_{2,3} - (\text{MULT.FACT} \times M_{1,3}) = 0.66667$$

Note that the steps are equivalent to finding E_2 by conventional mathematical operations. The *back* operating steps are the same as those for finding E_1 and are:

$$\text{Multiplication factor} = \left(\frac{M_{1,2}}{M_{2,2}}\right) = -0.75$$

$$\text{New } M_{1,3} = M_{1,3} - (\text{MULT.FACT} \times M_{2,3}) = 1.50$$

Final node voltage solutions are indicated by numbered subscript Ns and Ds, where the subscript stands for the node of solution.

We have used a slightly different number handling scheme and have arrived at the same solution. This technique can be expanded to larger arrays in order to provide an algorithm that solves all node voltages. It should be noted that solutions provide node voltages with reference to circuit ground; modeling techniques allow finding the voltages between nodes.

A consideration for programming is array size. The array consumes 2 X NMAX X (NMAX + 1) floating point variables with NMAX referring to the maximum number of nodes allowed in any circuit. The actual physical size of the array is twice as large since both real and imaginary parts of the complex number must be stored. The example showed only real parts.

Final Matrix Solution Algorithm

A flowchart for the MATRIX solution algorithm is shown in figure 4. The routine assumes that all admittance values of a circuit have been calculated using the formulae in table 1 and have been entered into an initially 0 matrix at positions according to the rules of table 2. Figure 5 is a pictorial of a 4 node solution sequence using the same symbology as figure 3. The pictorial assumes that the optional tests in figure 4 are not performed. This will give voltage solutions to all nodes.

IBM's venerable ECAP program yields all node voltages at each frequency. While useful, it can be difficult to interpret. A better way is to command the program for a specific node of solution (NS in the flowchart). The matrix must be solved at each frequency, so including the optional tests will reduce the number of back solutions to a minimum. A solution printout can then be made of all node voltage data at one node for the desired frequencies.

Calculation speed is increased by inverting the denominator in the outer loop. Division is invariably one of the most time-consuming functions; the inverted denominator allows multiplication instead of time-consuming division.

Another timesaving technique, not shown, is to include a 0 test of numerator

M(K,J) in the optional section. A 0 numerator will have no effect on inner loop variables, so a bypass could occur on 0s. (Remember to check both the real and imaginary parts of 0.) Many circuits will have only about one half array positions nonzero, so this test will help running time.

A similar test can be made by bypassing the inner loop if M(J,I) is equal to 0. This helps reduce running time on large node circuit models; at 20 nodes or less, the help is arbitrary. All such tests take time, so it is worthwhile to perform these tests outside the inner loop since the inner loop iterates the most.

It is interesting to note where the node voltage solution numerators and denominators are located. Numerators are always in the righthand or generator column. Denominators are always in the main diagonal from upper left to lower right. Row position is equal to node of solution. Highest node numerators and denominators are always found; back solution is required only for nodes less than the highest node. The back solution algorithm is called the *Gaussian elimination* or *Gauss-Jordan* method of solution.

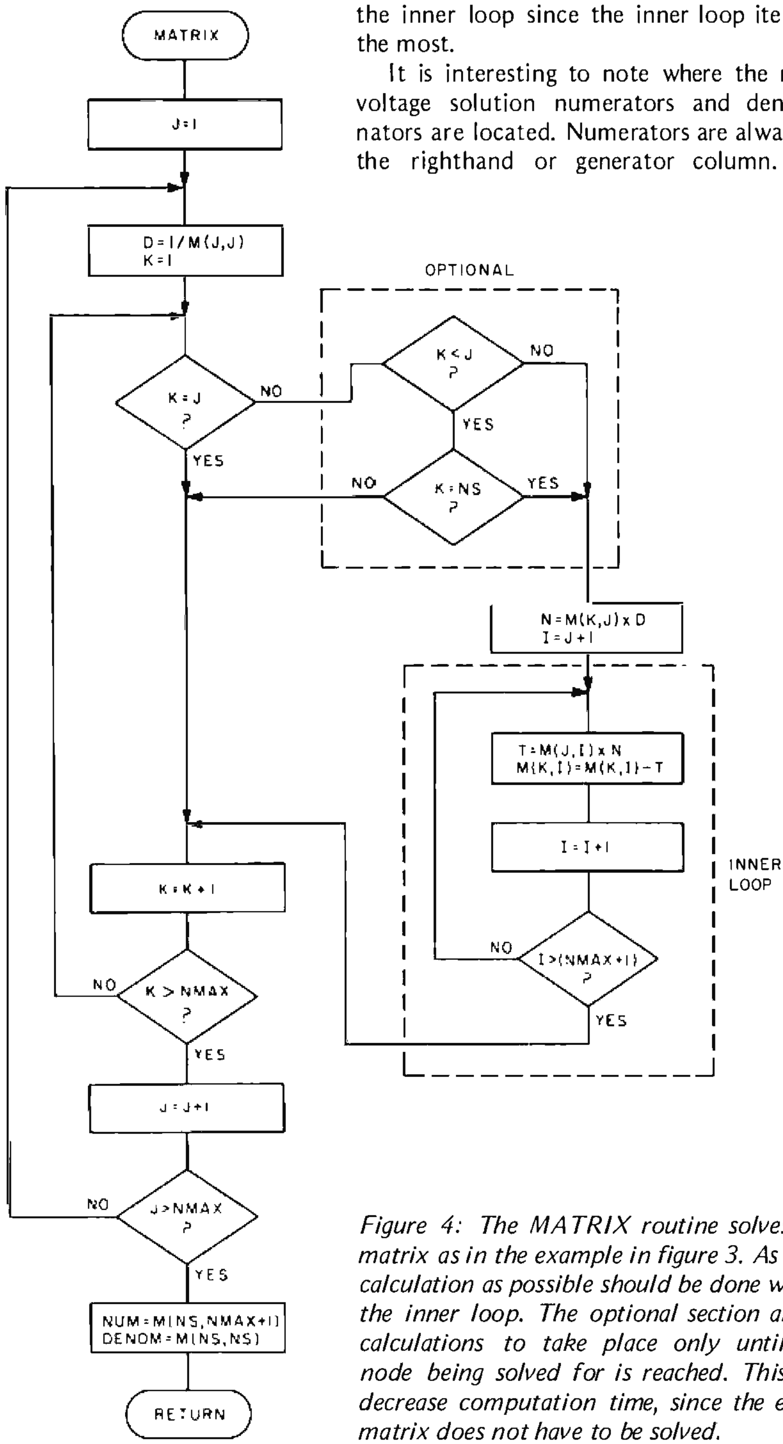

Figure 4: The MATRIX routine solves the matrix as in the example in figure 3. As little calculation as possible should be done within the inner loop. The optional section allows calculations to take place only until the node being solved for is reached. This will decrease computation time, since the entire matrix does not have to be solved.

Complete Frequency Solution

The flowchart shown in figure 6 is the ANALYSIS routine. This routine assumes that the admittance of each branch, Y, is already calculated. Before the matrix branch values can be calculated, the entire matrix is set to 0. Zeroing the matrix will allow simple addition and subtraction in the matrix fill section.

Variable W is the frequency in radians per second. Variable W1 is the negative inverse of W. These simplify admittance calculations. An often used constant is 2π which should be stored as a single variable. Variable F is the solution frequency.

Variable Y is the calculated complex admittance for passive branches but is the stored value of current for generators. Variable M is the two-dimensional complex matrix array used in figure 3, and variable S is the solution matrix, which is capable of storing complex values. Variable L is the subscript value for array S.

Most of the flowchart involves an examination of each branch, calculation of the admittance, and addition or subtraction of that value into the matrix. Positioning tests seem to be rather complex, but they do follow the rules of table 2. The flowchart and table 2 can be expanded to fit a special branch type.

Current flow of a generator branch is determined by node number entry order. This will be illustrated further under modeling techniques. A generator with one node set to zero will enter the matrix at only one position. If both nodes are nonzero the generator will enter the matrix at two positions.

Passive branches can have arbitrary node ordering. The test flow allows for this. One node specified as 0 will cause calculated admittance to add at only one matrix position. If both nodes are nonzero, calculated admittance will add at two positions and subtract at two other positions.

To check the node test flow, go back to the example of figure 1 and the matrix values shown in figure 4. Remember that admittance, matrix and solution arrays of figures 4 and 6 require handling *two* floating point values per complex number. There is no way around this fact.

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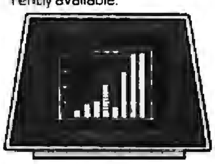
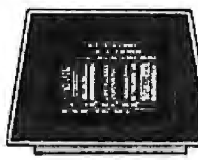


Bar Graphs



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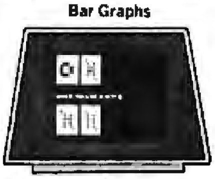

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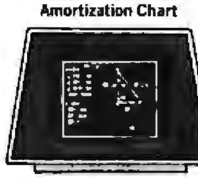

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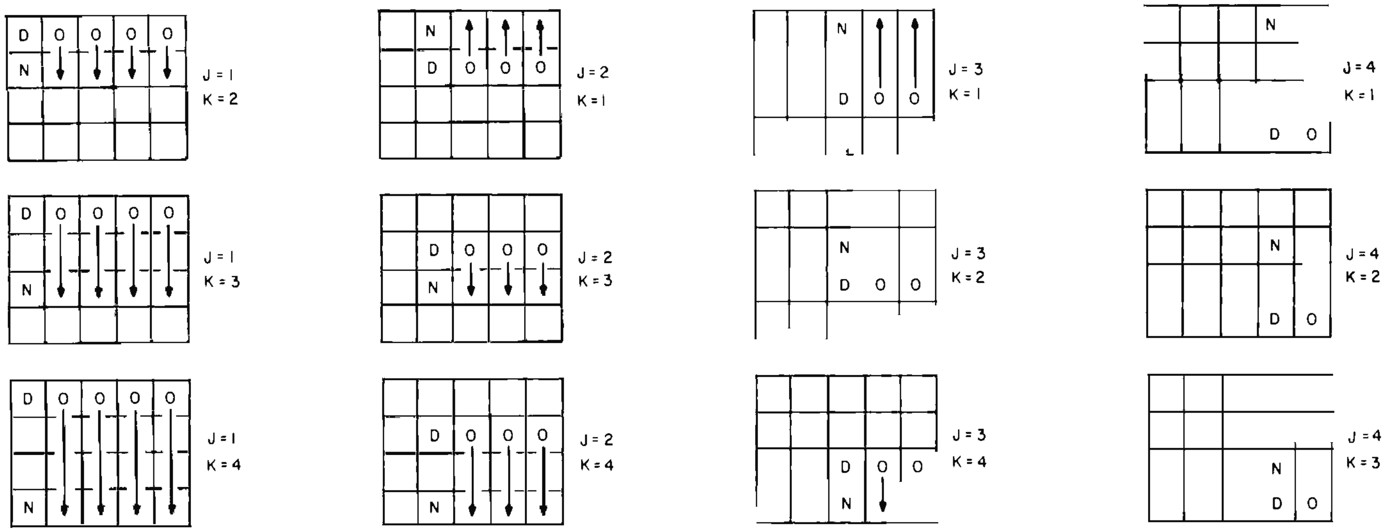

Figure 5: Sequential solution for all nodes of a 4 node circuit. This solution is the type that would take place if the optional section of figure 4 were deleted.

Branch Types and Passive Calculations

Small systems need simple rules, so it is probably easier to identify branch types in storage by integer numbers. One is sufficient. The number of different types should be considered in terms of calculation code and analysis needs.

Multicomponent branch types are strongly recommended since they reduce the number of nodes required in a model. Multicomponent branches are given in table 3 in terms of ohms, farads and henries stored in the branch list. List array storage positions should be considered in regard to the calculations.

Radian frequency, W, and its inverse negative, W1, are from the single frequency analysis routine. All of the parallel combinations are calculated as impedances first and then inverted. Series combinations should require less coding if calculated as impedances first; this can be seen by comparing table 3 with the complex values given in table 1.

Direct admittance calculations may be slightly faster for series combinations. The choice is determined by the amount of memory, possibly by external memory control. All analysis matrices should be in main memory when ANALYSIS is called.

Branch Value Storage		
Type	**V1 (First Floating Point Variable)**	**V2 (Second Floating Point Variable)**
Parallel RL	R	L
Parallel RC	R	C
Parallel LC	L	C
Series RL	R	L
Series RC	R	C
Series CL	C	L
Admittance Value Calculation		
Type	**YR (Real Part)**	**YI (Imaginary Part)**
Parallel RL	1/V1	W1/V2
Parallel RC	1/V1	WXV2
Parallel LC	0	WXV2 + (W1/V1)
Series RL	V1	WXV2
Series RC	V1	W1/V2
Series CL	0	WXV2 + (W1/V1)

Table 3: Calculations showing how a multicomponent branch admittance calculation is performed. The three series calculations (RL, RC, CL) are actually impedance calculations since they are so much easier to perform. To obtain the admittance, perform the complex inversion $Y = 1/(R+jX)$.

Passive Branch Values at DC

Direct current (DC) analysis can be considered as analysis at 0 Hz. Resistances remain the same but capacitors have 0 susceptance. Their susceptance (imaginary part) is effectively bypassed. Single inductors should have their susceptance value replaced by a low resistance, say a hundredth of an ohm (100 mhos susceptance), to avoid calculating difficulties. In actuality, inductors have finite resistance at DC.

Series combinations can be bypassed for certain types. A series resistor-capacitor (RC) or inductor-capacitor (LC) branch will have 0 admittance. In a series RL branch calculation, the susceptance calculation can be omitted and only the conductance calculation performed. Parallel combinations are also modified. A parallel RC branch requires only the conductance calculation. Parallel RL or LC branches would have the nominal

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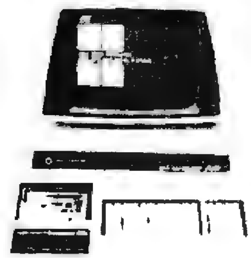

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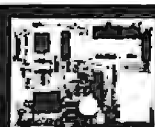

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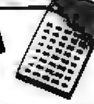

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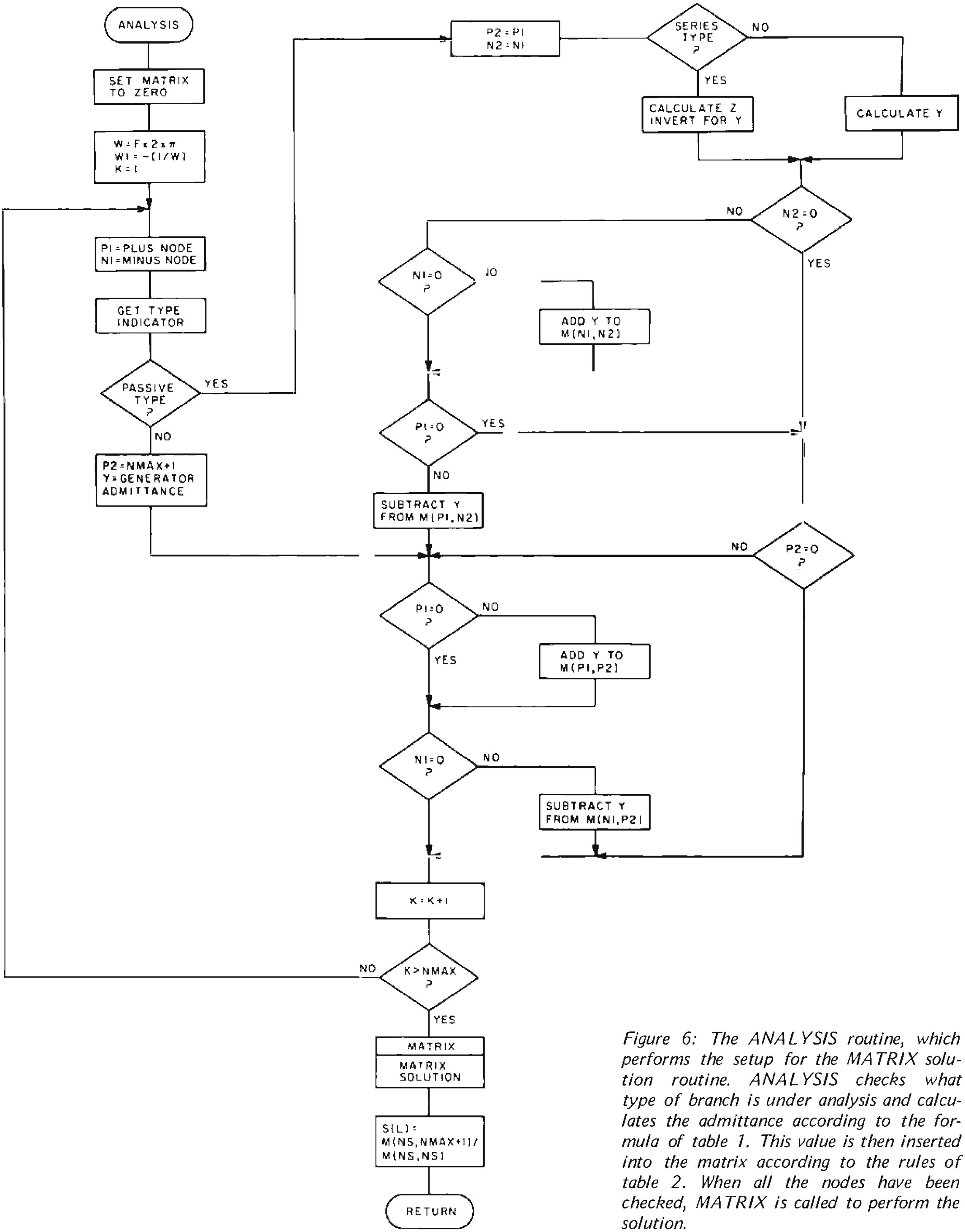

Figure 6: The ANALYSIS routine, which performs the setup for the MATRIX solution routine. ANALYSIS checks what type of branch is under analysis and calculates the admittance according to the formula of table 1. This value is then inserted into the matrix according to the rules of table 2. When all the nodes have been checked, MATRIX is called to perform the solution.

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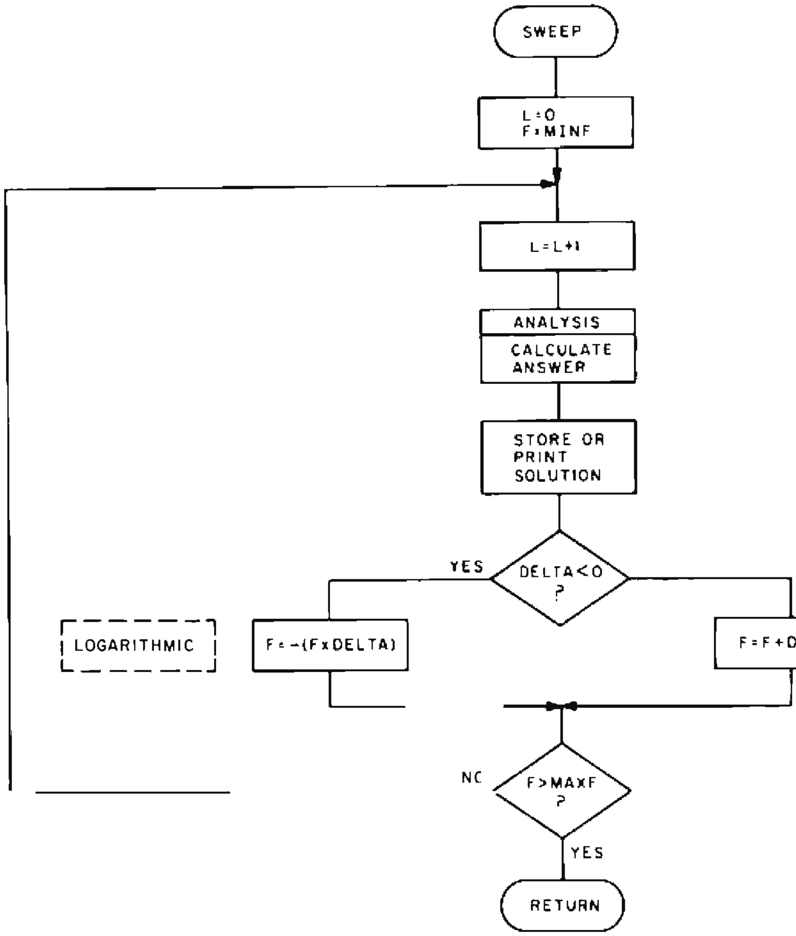
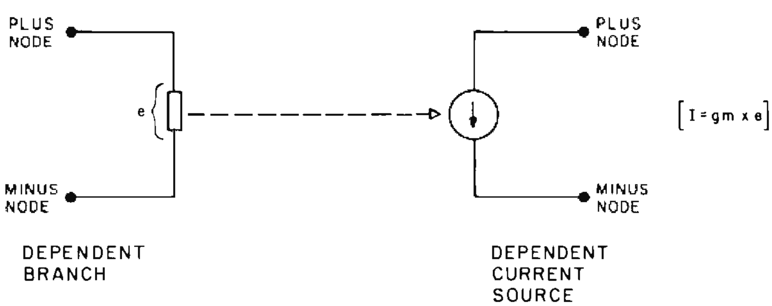


Figure 7: The SWEEP routine, used to perform a number of analyses on a particular circuit over a frequency range. Two types of sweeps are possible: linear and logarithmic. The variable DELTA is used as an increment and also as an indicator of which type of sweep analysis is to be performed. If DELTA is negative, a logarithmic analysis will be performed; if DELTA is positive, a linear analysis will occur.



Matrix Array Subscripts		
Row	Column	Enter into Array by
Plus node	Dependent branch minus node	Addition
Plus node	Dependent branch plus node	Subtraction
Minus node	Dependent branch plus node	Addition
Minus node	Dependent branch minus node	Subtraction

Table 4: Turning a dependent branch into a dependent current source. The source is entered into the matrix by the stated rules. Remember that any row and column combination with a zero node will not enter the matrix.

100 mhos conductance specified above. In all branches at 0 Hz the susceptance would be 0.

Frequency Sweeping

For this analysis, minimum and maximum analysis frequencies must be specified plus an increment. Most solutions over a narrow range will have a small increment but it is often useful to have a logarithmic frequency sweep with wide bandwidths. The main program should have a command point to which all major routines return. Frequency range can be selected at this command point with a minimum (MINF), a maximum (MAXF) and an increment (DELTA).

A choice between linear and logarithmic sweep can be done by simply checking for a negative or positive DELTA. A positive DELTA is the incremental change for a linear sweep, and a negative DELTA can be the frequency interval multiplier. The multiplier can be precalculated for the number of frequencies per decade:

$$DELTA = -(EXP(2.302585/NFD))$$

which reduces to

$$DELTA = -10^{(1/NFD)}$$

where NFD is the number of frequencies per decade and EXP is a function to raise e (the base for the natural logarithms which is approximately 2.71828) to the power of the following argument. For example, twenty frequencies per decade would have a DELTA equal to −1.122018.

Figure 7 is the flowchart for a frequency sweep analysis routine. The option of storing results or printing them directly depends on the operating system and memory. Subscript L is used only for solution matrix purposes.

There is a caution to be observed with solution storage: the number of frequencies to be analyzed must not exceed the storage matrix size. Other storage matrices may be written over if no check on the total number of frequencies analyzed is made. This is a very easy error to make.

Branch Switching

Implementing this function is useful for circuit modeling. In effect it allows you to disconnect or reconnect a branch from analysis and yet retain it in the branch list. It is the same as removing or replacing a component in a breadboard. If removed, it is still on the bench and can be installed later.

There are two easy ways to implement switching. Since we are using a numeric value to designate the branch type, we can define a positive value as a connected branch and a negative value as an open branch. Another method is to devote one byte per branch with a numeric value of +1 if connected and 0 or −1 if open. Another test can be inserted in the ANALYSIS routine of figure 6, just before the *passive type?* test. An open condition would bypass any calculations and go on to the next branch.

Dependent Current Sources

This branch type, not mentioned before, enables a model to duplicate transistors or operational amplifiers. It is a current source dependent on the voltage across another branch and is specified by a gain factor called *transconductance.* The symbology and matrix entry rules are given in table 4.

Transconductance is specified in mhos and is equal to the current divided by the voltage. Branch value entry is the transconductance, and admittance calculation for solution takes this as the stored value for the real part with an imaginary part of 0. You can think of transconductance as a *current gain* factor. A transconductance of 0.1 with a dependent branch voltage of 24 V produces a dependent source current of 2.4 A. A transconductance of 1.0 gives 24 A.

You do not have to be concerned about the dependent branch voltage. The matrix entry and solution will determine the current from the specified transconductance. The *direction* of electron flow is another

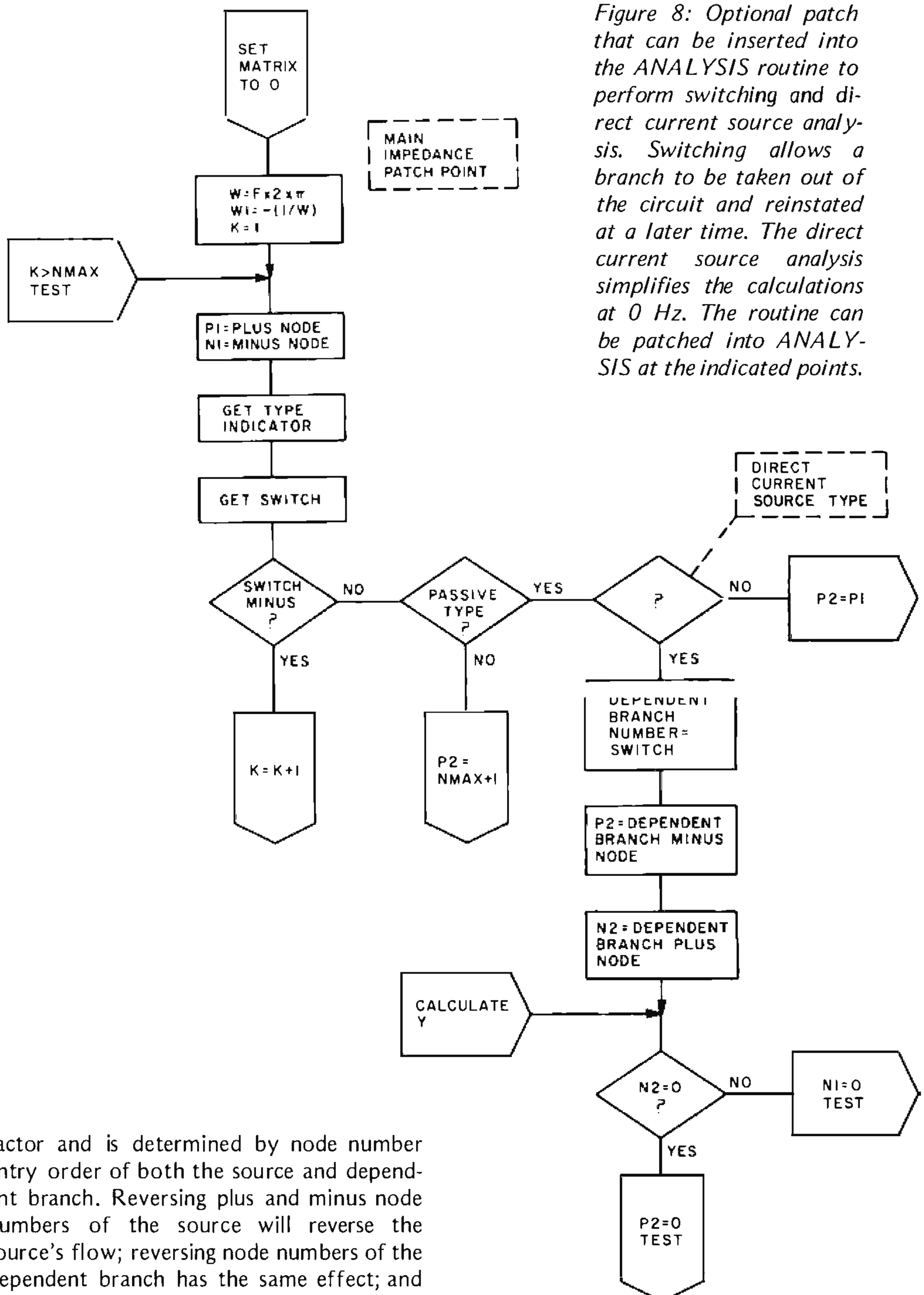


Figure 8: Optional patch that can be inserted into the ANALYSIS routine to perform switching and direct current source analysis. Switching allows a branch to be taken out of the circuit and reinstated at a later time. The direct current source analysis simplifies the calculations at 0 Hz. The routine can be patched into ANALYSIS at the indicated points.

factor and is determined by node number entry order of both the source and dependent branch. Reversing plus and minus node numbers of the source will reverse the source's flow; reversing node numbers of the dependent branch has the same effect; and reversing both source and dependent nodes returns electron flow to the original direction in the source.

One node of either source or dependent branch may be 0. Inspection of matrix entry subscript rules will show this. The only problem left is to allow the program to identify the dependent branch for subscripting.

Dependent Branch Identification

All passive components and generators may be entered into the branch list in any order. The ANALYSIS routine of figure 6 scans the entire list in order to fill the matrix for solution. A dependent source should be allowed to enter the list either ahead of or behind its dependent branch.

Two options come to mind. The extra integer byte mentioned under branch switching can be used to identify the dependent branch number in the list. Since transconductance is specified as the real part only, the second value storage might be used to hold the dependent branch number. Make sure that the particular floating point storage method that you are using will not change the value of the integer slightly. If there is

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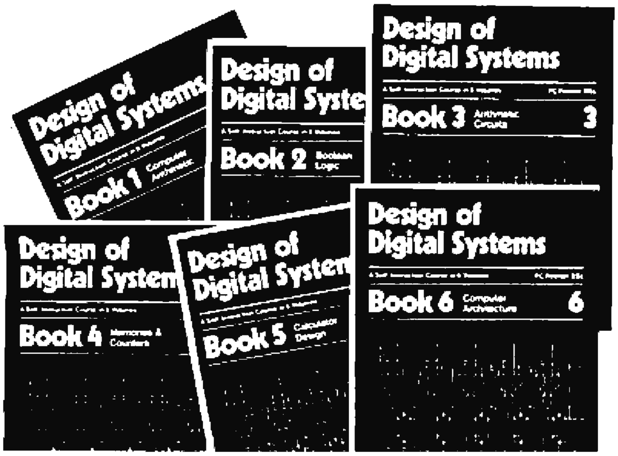

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any doubt about whether your floating point to integer conversions are totally accurate, use the extra integer per branch for both switching and dependent branch identity. A dependent source can be switched by signing the extra integer. This method will be assumed for all further discussion.

Entering branch data in the list requires an extra entry for dependent sources to identify the dependent branch. The ability to print out a branch list should also include printing the dependent branch number.

Modification of the ANALYSIS routine to handle dependent current sources is shown in figure 8. This modification also includes the switch function with the extra integer SW acting as the switch and identifier of dependent branch list number.

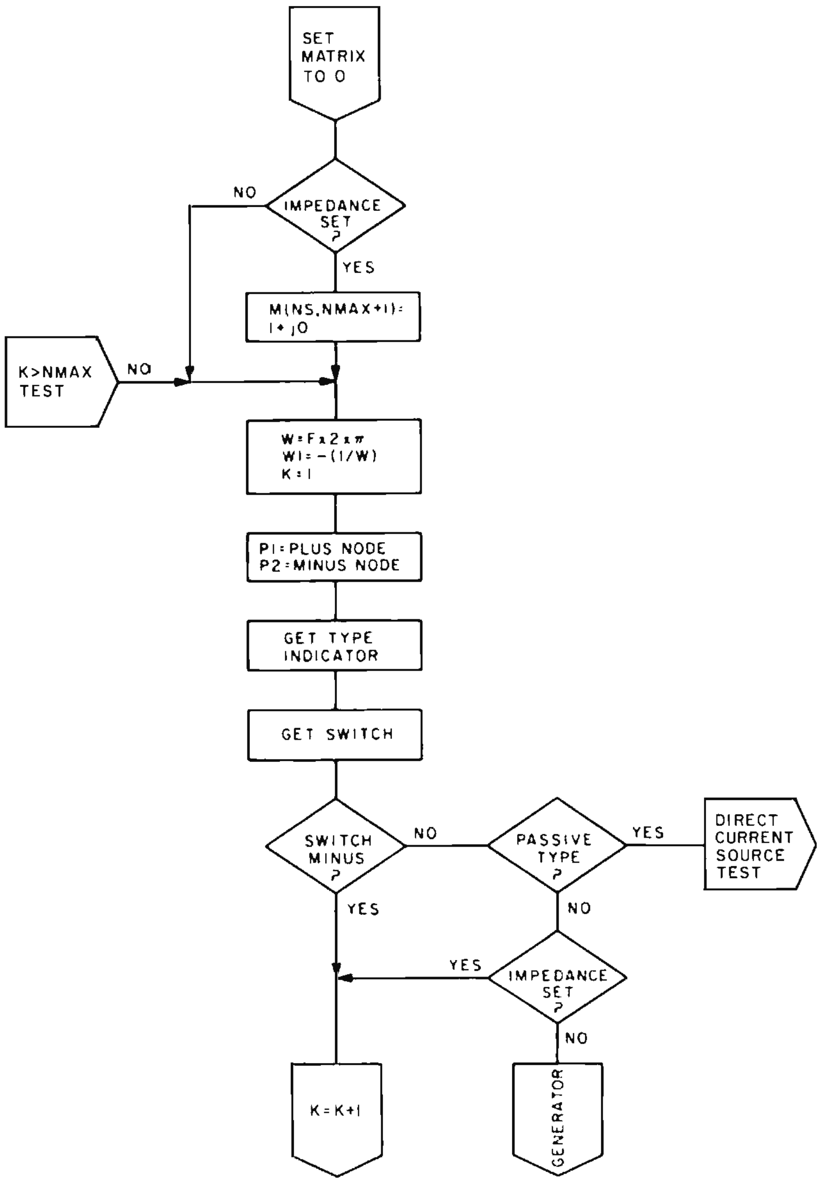

Figure 9: A patch that can be made to figure 8 to further increase the calculating power of the program. This patch will allow the solution of the matrix with impedance entries. It can be added to figure 8 at the instructions indicated.

Impedance Analysis

All analysis procedures have so far given only voltage solutions. The last analysis we will consider is readily determined by disregarding all generators, placing a value of unity in the proper generator column position and then solving the matrix as before.

This may seem too simple. To understand it, consider once again the circuit of figure 1 and the position of solution numerators and denominators. Denominators always lie in the main diagonal and numerators always lie in the generator column. Impedance analysis will have only one generator column entry since all other generator branches automatically bypass any entry into the matrix.

A unity current is simply (1.0 + j0), 1 A with no phase shift. This is the condition of figure 1 if an impedance is desired at node 1. The resistance of the total figure 1 circuit looking into node 1 is simply 25 ohms. In the model all generators are pure current sources; that is, they have no admittance themselves and can therefore be disregarded.

Addition of impedance analysis is shown in figure 9, a modification of figure 8. A flag variable must be held in the main program to identify analysis type. It is considered to be on for impedance and off for voltage analysis. It can be logical, integer or a single bit, but must be available if both types are desired.

Implementing impedance analysis requires a solution at only one node. It is best to use the optional tests in the flowchart of figure 4 and have all solutions at only one node. Direct printouts of impedance will be in rectangular form but the polar form can also be printed at the same time by using temporary variables and form conversion. Both forms are useful in studying analysis.■

REFERENCES

1. Huelsman, Lawrence P, *Basic Circuit Theory with Digital Computations,* Prentice-Hall, Englewood Cliffs NJ, 1972. Contains a great number of FORTRAN routines along with good basic circuit theory in both frequency and time domain.

2. Cornetet, Wendell H Jr, and Battocletti, Frank E, *Electronic Circuits by System and Computer Analysis,* McGraw-Hill, New York, 1975. Again, FORTRAN oriented, but contains complete source code for Ohio State's linear and transient analysis programs.

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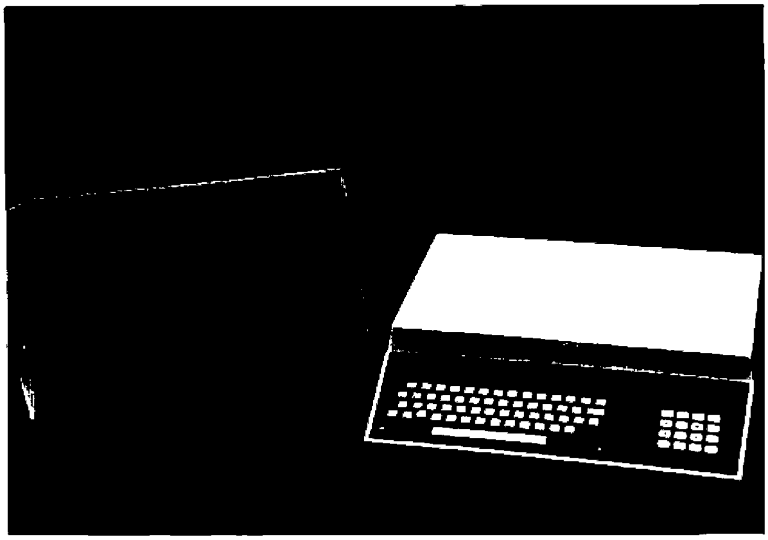

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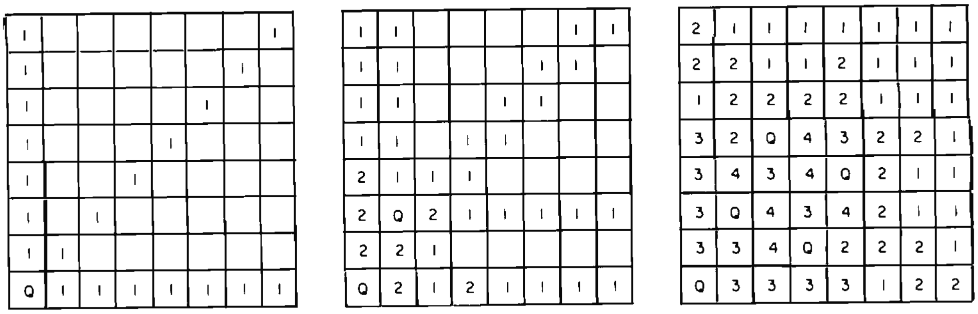

(a) (b) (c)

Figure 1: The author's algorithm for solving the eight Queens problem, in which eight Queens are to be placed on a chessboard so that no Queen attacks any other Queen. (In chess, the Queen can capture any piece that is in direct line with it horizontally, vertically, or diagonally.) The method consists of placing the first Queen on the lower lefthand corner square. Markers are placed on all squares that the Queen can attack (a). Moving one column to the right, another Queen is placed on the first empty square from the bottom. Markers are again placed (b). The process is repeated. Eventually, either the problem will be solved or there will be no more spaces for one or more Queens; (c) illustrates the latter situation where corrective action is taken by altering details of the trial solution.

Solving the Eight Queens Problem

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The eight Queens problem is a chess related puzzle, the object of which is to place eight chess Queens on an 8 by 8 chessboard in such a way that no Queen can take another. *[For the benefit of nonchessplaying readers, the Queen can capture any piece that is in direct line with it horizontally, vertically or diagonally. No detailed knowledge of chess is required in order to understand the rest of this article. . . .*CM*]* 8 is the maximum number that is not obviously impossible, since 9 would force one Queen to be in at least one other Queen's row or column. I will explain how I solved this problem using a computer, since a look into the mind of a problem solver from start to finish might help you with your own problems.

The First Method

The first method I tried was to place the Queens at random on the board and check the board for a proper position. There are 64!/56! or 1.7846289×10^{14} such permutations. I would never have thought about this except that I grossly overestimated the speed of the IBM 370 (the machine on which I was working). Even 370s have their limits, I was to discover. If the 370 evaluated 10,000 positions per second, it would have taken 565 years to find all the answers, and then only if I could have written a program that would create all the permutations one after another with no duplications. This is very difficult. I tried writing one and failed. If you can actually do this, I'd like to see it.

The Second Method

I then divided the board into eight columns and placed one Queen at random in each column and realized that with one Queen in each column, I could represent any permutation with an 8 digit number, each digit representing the position of one Queen in its column. Since no two Queens could have the same column position (for example, if the leftmost Queen was at 1 or the bottom, obviously no other Queen could also be at the bottom), what I needed was a list of permutations of all numbers from 1 to 8. With this method I would have to check only the diagonals; much of the work would already have been done. This also reduced my problem to 8! or 40,320

About the Author

Terry Smith is 21 years old, has studied data processing at Humber College in Rexdale, Ontario CANADA, and is a mathematics oriented computer hobbyist. He works as a computer programmer and is saving to buy a computer of his own on which to develop programs.

```
10  DIM A(8,8),A$(10),F(8)
11  FOR T=1 TO 10
12  READ A$(T)
13  NEXT T
14  DATA "0","1","2","3","4","5","6","7","8","9"
20  C=0
30  C=C+1
40  IF C=9 THEN 250
50  FOR E=1 TO 8
60  IF A(C,E)=0 THEN 89
70  NEXT E
80  GOTO 330
89  F(C)=E
90  A(C,E)=-1
91  D=1
92  GOSUB 100
93  GOTO 30
100 FOR X=-1 TO 1
110 FOR Y=-1 TO 1
120 IF X*Y+X+Y=0 THEN 220
130 FOR Z=1 TO 8
140 A=C+Y*Z
150 B=E+X*Z
160 IF A>8 THEN 220
170 IF A<1 THEN 220
180 IF B>8 THEN 220
190 IF B<1 THEN 220
200 A(A,B)=A(A,B)+D
210 NEXT Z
220 NEXT Y
230 NEXT X
240 RETURN
250 FOR X=8 TO 1 STEP -1
260 FOR Y=1 TO 8
270 IF A(Y,X)=-1 THEN 290
280 PRINT A$(A(Y,X)+1);
281 GOTO 300
290 PRINT "Q";
300 NEXT Y
310 PRINT
320 NEXT X
321 PRINT
330 REM NO SPACES, NOW WHAT?
340 C=C-1
350 A(C,F(C))=0
360 E=F(C)
380 D=-1
390 GOSUB 100
391 IF E=8 THEN 340
400 FOR X=E+1 TO 8
410 IF A(C,X)=0 THEN 440
420 NEXT X
430 GOTO 340
440 A(C,X)=-1
441 F(C)=X
450 D=1
451 E=X
460 GOSUB 100
470 GOTO 30
480 END
```

Listing 1: A BASIC program for solving the eight Queens problem.

positions to search, a far cry from 1.7846289 x 10^{14} or even 8^8. But a program to create all these numbers? Much later I discussed this with some friends whom I consider to be software experts. They shook their heads saying, "This is a difficult task." They were right, for as it turned out, I had to give up. An easy solution just wasn't going to work.

Final Method

A determined human, after trying permutations and finding the problem is not trivial, would get a set of pawns to represent Queens and, using pennies for markers, attempt to find a solution by placing a Pawn (to represent each Queen) on a chessboard and a penny on each square that comes under that Queen's influence. By inspection (s)he would determine where to put subsequent Queens. A methodical procedure would be as follows (I have shown in parentheses the line in the program which is relative to the step in the manual solution):

Place a Queen in the lower lefthand corner of the board (line 90) and then, on all the squares that would come under that Queen's influence, place one penny (GOSUB 100, D=1). Then moving one column to the right (line 30), place a Queen on the first empty square from the bottom. This entails having to move up two squares. Place a penny on each square (even the ones already marked) in this Queen's domain. You'll see why in a minute. Continue moving right and repeating this algorithm until you hit a column that is all pennies (line 80). You use a lot of pennies here. If you run off the righthand edge of the board (line 40) you have solved the problem. However, you probably won't find one the first time. Three columns from the end you will have to stop, having run out of spaces. Now you remove the latest Queen (line 350) and then remove one penny from each of its dominion squares (line 380, GOSUB 100 D=-1). This is why you placed pennies on already covered squares because if you didn't, you wouldn't know if the penny there was the subject Queen's or not. Continuing from the subject Queen's square (line 400) look up the column for a new blank spot (line 410) to place a new Queen and continue. If there are none or if your last Queen was at the top of the board (I check for the top first, line 391), move back one column (line 340 again). Remove that Queen and remove her pennies, and check for blanks above, etc. If you are trying this by hand by now you will have noticed how slow and messy it is. It was only the feelings of frustration from the manual simulation that kept me moving on this seemingly hopeless computer simulation.

The final program started off at half its present length and I spent three days repairing it by adding one line after another as it failed time and again. I added line 391 to eliminate a subscript error.

I was beginning to get worried because the program was twice its original size and I was no longer capable of understanding it at a glance. I typed RUN for the 100th time and waited for the next error. My method of repair depended on my being able to comprehend the program. I added several GOTOs and I knew I couldn't keep it up much longer.

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Suddenly to my amazement, the printer started to hammer out the solutions as fast as it could! I peeled off the paper to check the first one by hand and it was right! I include the final program exactly as it was written, a blow to the cause of structured programming and a glorious victory for dumb luck. If you want to try it, go ahead, but be forewarned that only on the Humber College VM370-135 CMS system was the solution instant. On a Heathkit H8 it took 20 minutes for the first solution and 5 minutes for the next. There are 92 solutions of which 23 are discrete. So beware! I feel this is the most efficient algorithm possible. (Using brute force to generate and file all those 40,320 8-digit numbers, and having the computer run through them probably qualifies for the epithet "inefficient.")

The eight Queens problem was a challenge, and the pleasure of beating it was tremendous. I feel the approach described here demonstrates a good heuristic for general problem solving, which is: don't check all the other situations in search of a solution, but custom design your own situation to match your specifications. I think now I'll see if I can place eight Maharajahs (a piece combining the Queen and Knight moves) on a board. Excelsior!■

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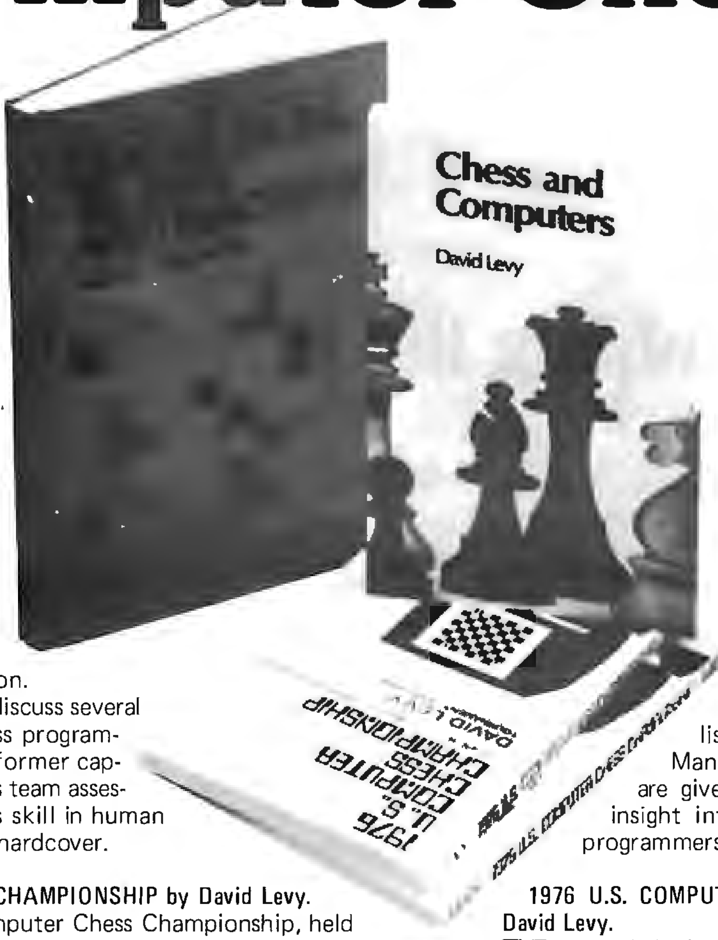

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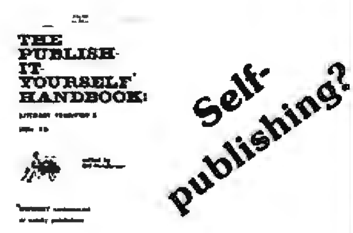

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Assembling the H9 Video Terminal

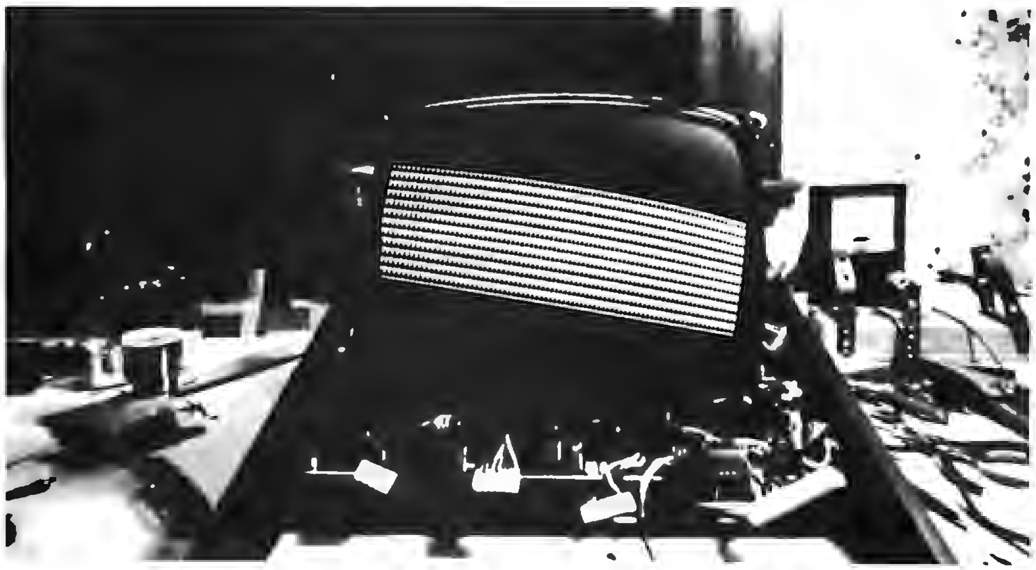


Photo 1: The most exciting part follows the construction of a good portion of the chassis, power supply, high voltage circuits and the character generators: the terminal is fired up for the first time, and the pleasant aura of success is evident in the display. The deflection yoke has yet to be aligned to produce horizontal rows of characters, but just the fact that characters appear at all is exciting.

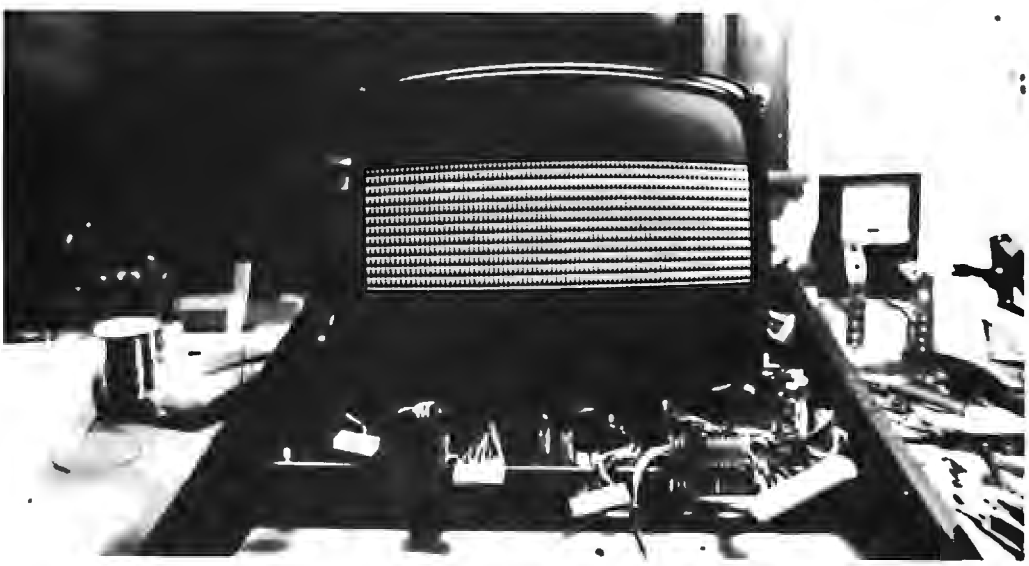


Photo 2: Several steps later in the manual, the deflection yoke has been carefully twisted around the neck of the cathode ray tube to produce horizontal rows of null ("?") characters.

I have just completed one of the more satisfying electronic experiences in my life. I think a lot of the feeling is a result of everything working the first time. Everyone should have such an experience at least once every ten years. More often is preferable, but Murphy's Law usually prevents it. I have just finished assembling the Heathkit Model H9 video terminal.

At first I thought that everything worked the first time because of my great skill as an assembler. However, as a long time Heathkit builder (automotive testers, amateur radio equipment, and now microprocessor equipment), I have sensed something better about this kit and its construction manual. While they appear in the familiar and efficient format of past Heathkits, there is something which made them easier to follow, and therefore helped contribute to the "works the first time" result. First, the printed circuit boards are clearly and legibly marked. Double and triple referencing of all components by manufacturer's part number, Heathkit part number, and reference designation made part location much easier, faster, and more accurate. The only place where something might go wrong is in the placement of integrated circuits and diodes (correct placement of pin 1 and band). Second, each printed circuit board is electrically checked as soon as it is completed. It is much easier to check each board as it is completed (there are six printed circuit boards to build) than to troubleshoot the entire finished unit. Each check assures that the board is functioning in a go or no go sort of way. Generally, you can be assured the unit is working up to the point of inserting the last printed circuit board. If something does not work, you can assume it was the last board added. This cuts down troubleshooting time. Resistance checks at each board completion (before applying power) further assure that you will not do severe damage to a board because of shorts or integrated circuits installed backwards.

The entire building procedure took me about 18 hours *[but reports from other builders, such as yours truly, indicate that it can take as long as 40 hours. . .CH]*. Sometimes you just get hooked and can't quit. This also contributes to the little mistakes which cause things not to work the first time. As Heathkit advises, if you get tired, quit and go rest. I might mention that this is the prime reason previous Heathkits, which I assembled, did not work. At 2 AM diodes and integrated circuits can go in backwards very easily and wires can get soldered to the wrong places.

The chassis took about two and a half hours to set up. A lot of mechanical as-

Notes on Construction of the Heathkit H9 Terminal. . .

This series of pictures illustrates several aspects of the construction of the Heathkit H9 terminal. The pictures begin about midway through the construction of the kit, and are presented in the order of assembly of the kit per the manual.

Photo 3: One of the most tedious tasks when assembling the H9 is manually checking each switch of the keyboard. Here, two metal cake pans are used as input (background) and output (foreground) of the process of checking each switch with an ohmeter.

Photo 4: After soldering the switches to the keyboard printed circuit board, each switch must be individually tagged with a preprinted self-sticking key identification. The key identification fits into a recessed flat area on the upper side of the keytop.

Photo 5: Eventually all the keys are marked properly and the completed keyboard is ready for installation.

sembly, as opposed to electrical assembly, is required. I hardly used my soldering iron, except to make the occasional small cable assembly. The major cable assemblies are already assembled and supplied in the kit. I thought I would never run out of plugs to put into the chassis, and interconnect. There seemed to be a lot of them. All are necessary to support and interconnect the seven printed circuit boards, and to interface to the outside world.

The power supply circuit card was the first electrical assembly. It went very fast, half an hour, and after resistance checks, it fired up and regulated beautifully. The tests at this point check the regulators on the circuit card, and also check the power wiring on the chassis.

The character generator circuit card was also quickly assembled. The testing at this point was a resistance check, and voltage measurement after power on. The video circuit card must be completed before you can be assured that the character generator board is working. The video circuit card took just a little longer, but then it was just a little bigger.

The next part of the assembly was one of the most enjoyable (enjoyable only if it works; remember Murphy). Even though less than half of the circuit cards were assembled and installed, there were enough to fire the terminal up to see how it worked. The cathode ray tube was installed, more mechanical work. Not too hard, but a little time consuming, as well it should be. It is not wise to be careless with a cathode ray tube. It can implode and must be handled carefully, as noted in the manual. Temporary jumpers, supplied with the kit, are used to set up the character generator and video cards. If all is going well, when you turn the power switch to on, twelve rows of 80 "?" characters with underlines appear magically on the screen (see photo 1 and photo 2). I couldn't believe it when it worked just as the manual said. It was 3:30 AM and I went to bed a very happy person.

Next day started with the keyboard circuit card. This was the most time consuming board to assemble, with lots of pushbuttons to test and install (see photo 3, photo 4 and photo 5). There were also a large number of jumpers to install. I would almost pay a few dollars more for a double sided printed circuit board rather than put in all those jumpers. The pushbuttons have a much better feel to them than what I had expected. My wife contributed significantly by inserting the logos onto the top of each key. The keyboard resistance check was made and power applied. Behold, I could make

Photo 6: After installation of the keyboard, another live test of the display is performed, this time using the keyboard to vary the content of the display.

letters and numbers appear on the screen (photo 6).

The memory and counter circuit card was next, the board with the most integrated circuit sockets to solder in. As in all submodules of a Heathkit, the assembly process begins with a parts tally (see photos 7a and 7b). It takes a while. However, look at the positive side; I personally would rather solder in sockets than try to remove even one soldered in integrated circuit. Sockets for each and every integrated circuit on every board are supplied.

The final board to be assembled is the IO circuit card. It does not take too long to build, but the most impressive thing here is the schematic. Working professionally with microprocessor systems, one of the biggest problems I've run across is interfacing. Heathkit has designed one of the most flexible IO cards I have ever seen. Serial RS-232, TTL, and 20 mA loop are all jumper selectable. Parallel IO is also included.

The timing and processing unit circuit card is preassembled, tested, and calibrated by Heathkit. It is simply plugged in. The final adjustments are easily accomplished. A good VOM or VTVM is all that is required through the whole procedure, with ranges of 10, 100 and 1000 ohms for resistance measurements.

One final electrical note: there have been reports of blown Darlington transistors because of insufficient current limiting. While this fix was not in the manual when I assembled the H9, the friendly guys at the local Heathkit store provided both the information and the components to effect it. Readers with H9 kits should check to make sure that this fix is present.

Reflecting on the H9 design, I found two things I do not like. 12 rows of data does not seem sufficient. Anyone writing software and needing to see more than the last 11 statements will feel limited. This is offset a bit by the short form mode which creates four columns with 12 rows and 20 characters. Now 48 statements, rather than 12, can be displayed at once if they are all less than 20 characters long. The second thing I found disconcerting was that the characters displayed on the video screen were slightly blurred on the left and right edges of the picture. After playing with the adjusting magnets, and other adjusting controls, this was minimized. It is barely noticeable through the front protective screen.

Other controls include page or scroll selection, independent cursor controls, erase page, erase to end of line, automatic line carry over selection (automatic return to next line after 80 characters), controls for timeshare (half or full duplex, transmit page, break). Serial and parallel interfaces, adjustable to rates between 110 and 9600 bps, are very flexible and functional. Un-

Photo 7a: *A good practice when assembling complicated kits is built into the Heathkit manuals: a parts check off. In this photograph, the parts for the "RAM and counter circuit board" have been unpacked from the paper bags, with loose parts placed in the baking pan at the left.*

fortunately, few of the standard ASCII formatting commands are decoded: if you want to clear the screen from your computer, 12 line feeds in a row is about the only way to do it, in spite of the fact that an equivalent key is available.

After searching for several months, I was very pleased to find an 80 character per line terminal with so many functions. I saw units that cost 50 to 70 percent more which did not have the features of the H9. The documentation is equal or better than past Heathkits. Physically, it looks professional and is clean and neat. It would be hard to find a unit so flexible for the investment. I use mine with a modem for timesharing as well as using it as a terminal for my home microprocessor system. And what's more, it worked the first time.■

Photo 7b: *As the parts are checked off against the parts list, they are moved from the pan at the left into the pan at the right, and arranged in order for access later during assembly. In this photo, the circuit board for the new module and a conductive foam pad with the integrated circuit parts are both placed at the back of the two pans.*

Maze

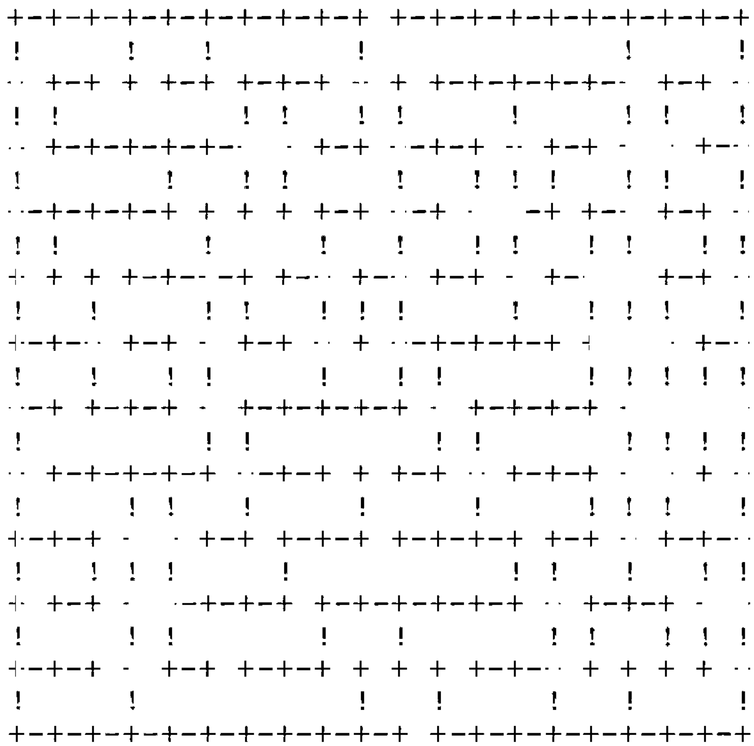
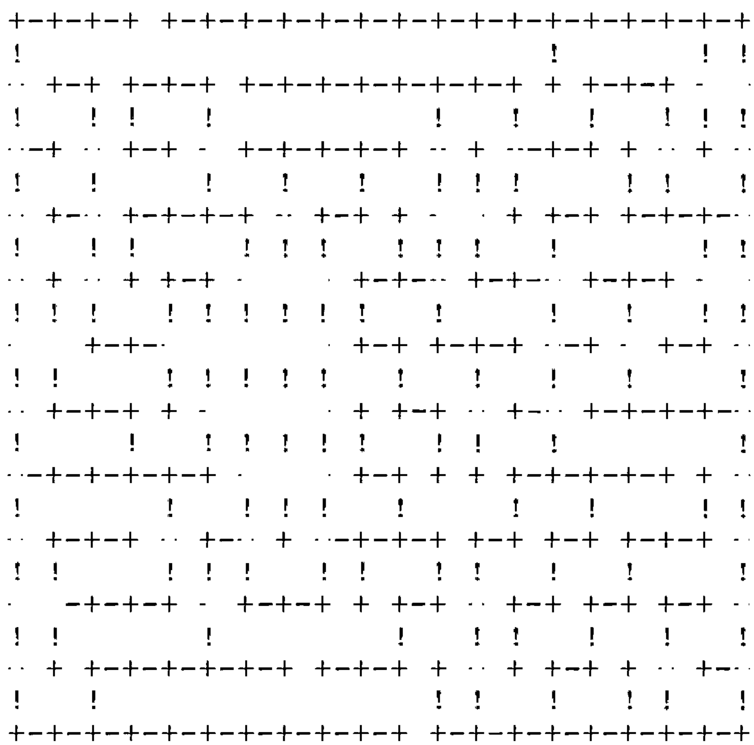


Figure 1: Two typical mazes as generated by the program of listing 1. A series of these will entertain you for hours and furnish you with another response to that age old question, "What do you do with it?"



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Here is an interesting novelty program that you can leave running on your video display whenever you are planning to have guests over to see your computer. The program automatically generates and displays a different maze about once a minute on an Apple I computer. Each maze is 11 squares high and 19 squares wide, and has only one path through it. The size, 11 by 19, was chosen so that a display with 24 lines of 40 characters each would just fill the screen.

Basically, here's how the program works. The entrance and exit points are randomly chosen first. Next, a random walk is performed from both of these points until the two paths cross. This determines the one, and only one, way through what will become the maze. As each "cell" is visited via these random walks, the location of the cell is placed in a *queue.* A queue is simply a list of items in which all insertions are made at one end, and all accesses are made from the other end, ie: it's a first in-first out (FIFO) list. When either of the walks runs out of places to go (gets stuck in a corner, or gets boxed-in), it goes back to the queue and restarts from the node indicated by the next item in the queue. This restarting process continues until the queue becomes empty, at which point the maze is complete. The resulting maze is then displayed, and the whole process starts over again.

The program is written in Apple BASIC and requires less than 2 K bytes of memory; an additional two pages (512 bytes) are required for the queue and grid array. Along with the BASIC interpreter the whole thing easily fits in 8 K bytes. In order to conserve space, the grid array and the queue are accessed via PEEK and POKE functions. The queue, indicated by the variable Q in the program, is located starting at decimal location 768; the grid array G starts at decimal location 1024. These values are set in line 100 of the program. Each of these

arrays requires one 256 byte page of memory.

If you have a random access display (if your hardware lets you change displayed characters without having to regenerate the complete display), you might want to modify the program to become an interactive game. After the maze is displayed, let players try to move some type of cursor through it before a set time limit is reached.■

Listing 1: An Apple I BASIC listing of the maze program. This program should be easy to convert to any BASIC language which uses PEEK and POKE functions.

```
10 DIM A(3), B(3), C(3), E(4), N(2)
20 E(1)=1:E(2)=2:E(3)=4:E(4)=8
100 Q=768:G=1024:R=-1:F=-1:M=0:L=2
120 FOR K=1 TO 209: POKE G+K-1,0: NEXT K
140 N(1)=3+ RND (7):N(2)=205- RND(7)
160 POKE G+N(1),2: POKE G+N(2),24
180 P=N(1): GOSUB 1000: P=N(2): GOSUB 1000
200 L=3-L: P=N(L)
250 GOSUB 3000: IF P<0 THEN 350
300 GOSUB 1000: GOTO 400
350 GOSUB 2000: IF P<0 THEN 500
400 N(L)=P: GOTO 200
500 FOR K=1 TO 24: PRINT : NEXT K
510 FOR K=1 TO 11
520 FOR L=1 TO 19
540 T= PEEK (G+19*(K-1)+L-1)/2
560 0$= " ": IF T=2*(T/2) THEN 0$= "-"
580 PRINT "+";0$;
600 NEXT L: PRINT "+"
620 FOR L=1 TO 19
640 T= PEEK (G+19*(K-1)+L-1)/4
660 0$= " ": IF T=2*(T/2) THEN 0$= "!"
680 PRINT 0$;" ";
700 NEXT L: PRINT "!"
720 NEXT K
740 P= PEEK (Q+1): T=P-19*(P/19)
760 FOR K=1 TO T:PRINT "+-"; : NEXT K:PRINT "+ ";
780 FOR K=T+2 TO 19: PRINT "+-" ; : NEXT K: PRINT "+"
800 GOTO 100
1000 R=R+1: POKE Q+R,P: RETURN
2000 F=F+1: P=-1: IF F<=R THEN P=PEEK (Q+F): RETURN
3000 K=0
3100 T=P+1: IF T/19#P/19 THEN 3200
3150 S=1: GOSUB 4000
3200 T=P-19: IF T<0 THEN 3300
3250 S=2: GOSUB 4000
3300 T=P-I: IF T/19#P/19 THEN 3400
3325 IF T<0 THEN 3400
3350 S=3: GOSUB 4000
3400 T=P+19: IF T>=209 THEN 3500
3450 S=4: GOSUB 4000
3500 IF K#0 THEN 3600: P=-1: RETURN
3600 K=1+ RND (K):T=C(K)
3610 IF PEEK (G+T) #0 THEN M=1
3620 IF M=0 THEN B(K)=B(K)+16*(PEEK (G+P)/16)
3630 POKE G+P, PEEK (G+P)+A(K)
3640 POKE G+T, PEEK (G+T)+B(K)
3650 P=T: RETURN
4000 IF PEEK (G+T)=0 THEN 4300
4050 IF M#0 THEN RETURN
4100 IF PEEK (G+P)/16= PEEK (G+T)/16 THEN RETURN
4300 K=K+1: C(K)=T: A(K)=E(S)
4400 S=S+2-4*((S+1)/4): B(K)=E(S)
4500 RETURN
```

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Programming Quickies

Converting North Star's Deletion Characters

Alan R Miller
New Mexico Tech
Socorro NM 87801

I own a North Star floppy disk operating system and have patched in my own IO routines. I found that attempting to correct a single error by using the DEL (or RUB OUT) key doesn't work. Or if I try to cancel a complete line with the ESC key, nothing happens. The problem is that North Star's disk operating system uses the BASIC commands of the at symbol "@" for canceling a line and the back arrow (or underline) for correcting a single character. All my other programs, monitors, assemblers and so on use the ESC key to cancel a line and the DEL (RUB OUT) key for deleting the previously typed character.

The solution is fairly simple and is shown in listing 1. Since I had to write a set of IO routines anyway, I incorporated a section to look for ESC and DEL input. When either is found, the byte is changed to the corresponding value needed by the operating system. The extra 16 bytes will readily fit into the space allocated to the user.

Of course, the original correction characters, at sign and arrow, can still be used.■

```
294D DB00    CHIN:   IN    STAT     ; CHECK STATUS
294F E601            ANI   MASK     ; MASK FOR INPUT READY
2951 CA4D29          JZ    CHIN     ; LOOP UNTIL READY
2954 DB01            IN    DATA     ; GET DATA BYTE
2956 E67F            ANI   7FH      ; STRIP PARITY
2958 FE1B            CPI   1BH      ; ESC?
295A CA6329          JZ    CESC     ; DELETE LINE IF SO
295D FE7F            CPI   7FH      ; DEL?
295F CA6629          JZ    CDEL     ; DELETE CHARACTER IF SO
2962 C9              RET            ; OTHERWISE RETURN
             ;
2963 3E40    CESC:   MVI   A, "@"   ; CHANGE ESC TO @
2965 C9              RET
             ;
2966 3E5F    CDEL:   MVI   A, 5FH   ; CHANGE DEL TO BACK ARROW
2968 C9              RET
```

Listing 1: 8080 assembly language listing of the changes to the North Star disk operating system to allow usage of DEL and ESC key codes for deleting characters and lines.

A Simpler Digital Cassette Tape Interface

Ralph W Burhans
Ohio University
E E Dept
Athens OH 45701

To our department at Ohio University, "Saturation Recording's Not All That Hard" by David M Allen, page 34, January 1977 BYTE, was a sleeper until we happened to visit Abex Corporation here in Athens OH. While we were there, Dave Weeks showed us a direct digital interface which he was building from an old cassette deck. Bernie Hutchins in the *Electronotes Applications Note No 32,* March 25 1977, published a short item on the 555 used as a window comparator. Putting the two ideas together results in the interface of figure 1, where the 555 performs the function of upper and lower limit comparators with adjustable threshold along with a flip flop to recover the serial data stream. It even supplies an extra open collector output to drive a read indicator LED. A cassette deck by Western Auto was obtained at the local surplus store for $10 and was modified by removing all the original audio electronics, but saving the wire motor control and power on and off switching features. An evening of bench tests indicated that the head would provide a 10 to 20 mV peak to peak output on direct saturation. Installation of a single Darlington transistor (SE4022) provided 40 db gain to bring the read level up to a volt or so, which fires the 555 comparators by pulling down the 555 control point threshold with an adjustable resistor to ground. That is about all there is to the unit except for a 4049 buffer inverter driver.

Photo 1: The author's tape recorder as modified for direct digital recording. IO switch is at bottom left; LEDs are at bottom right.

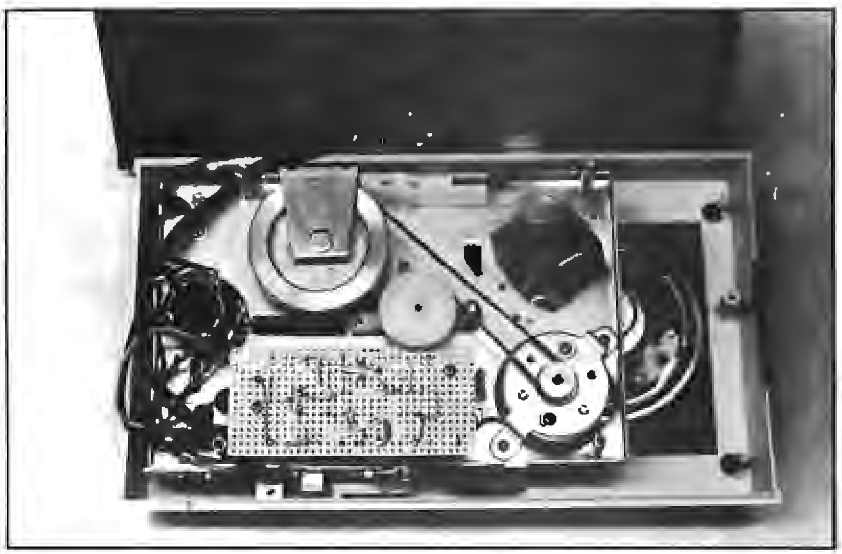


Photo 2: Interior view of digital cassette unit showing additional circuitry on perforated circuit board.

In our department, Larry Eichman fabricated a neat packaging of the system for a senior lab project. The recorder works fairly well over the range of 100 to 1200 bps. At 2400 bps, though, the tape recorder drive is somewhat erratic because of the motor speed drive mechanical on and off control. Some users of similar older tape machines have modified the drive motor by bending the regulator spring such that power is always applied to the motor with a regulated power source, rather than depend on the centrifugal rotating regulator mechanism. The same kind of machine has been used on a homebrew 8008 system, and Larry Eichman has used it with a COSMAC 1802 processor. Photos 1 and 2 illustrate the front panel controls and IO indicators, as well as the circuit board wiring for the electronics.

The older style rotary switching deck is not suited to more complex software start and stop controls, but it does provide a quick serial data IO system for those who are willing to cannibalize an existing audio cassette recorder.■

IC Number	Type	+5 V	Ground
IC1	555	8	1
IC2	4049	8	1

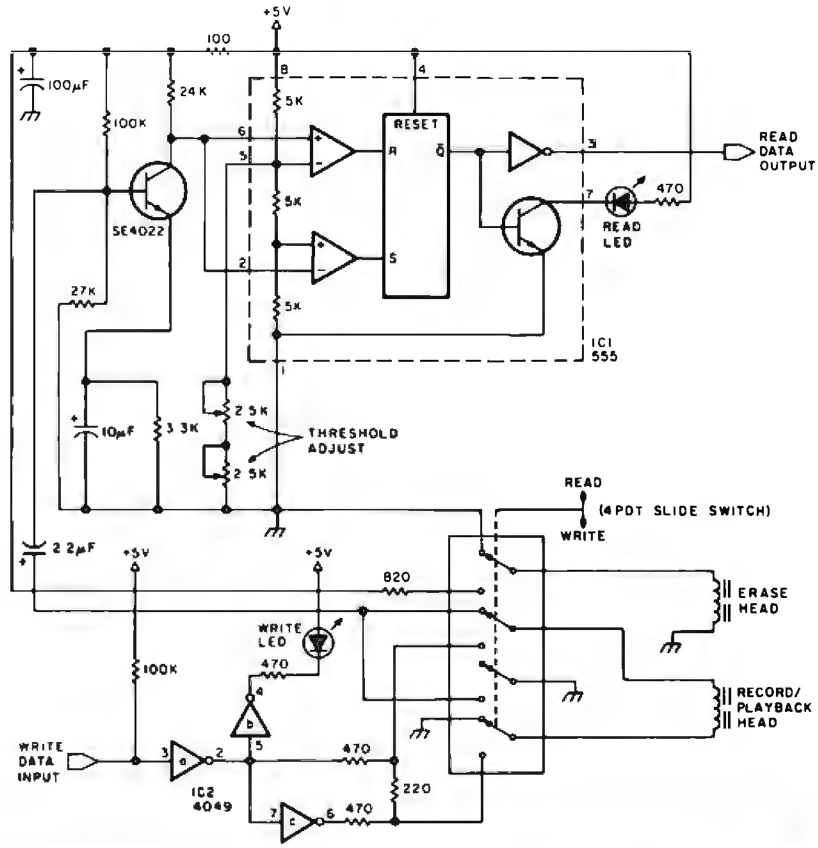


Figure 1: Circuitry to modify a standard cassette recorder for direct digital recording. During the write process a DC current of approximately 1 V is passed through the record head, which saturates the tape. The polarity of the saturation recorded signal depends on the polarity of the DC current going through the head winding. During the read cycle, a voltage is induced in the head winding only when a transition between two oppositely polarized zones moves past the head. The 555 circuit (IC1) is used as a combination level detector and flip flop to recover the serial data.

REFERENCE

Electronotes Applications Note No 32, March 25, 1977. Available from *Electronotes,* 203 Snyder Hill Rd, Ithaca NY 14850.

Souping Up Your SwTPC 6800

Steve A Hughes
5831 Hillside Dr
Doraville GA 30340

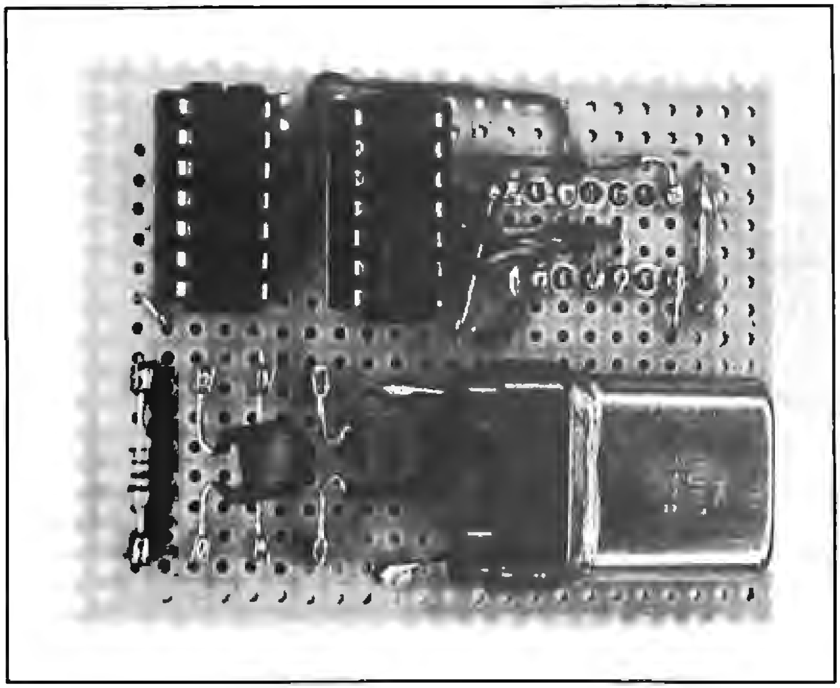


Photo 1a: Top view of the SwTPC 6800 processor clock speed modifier circuit.

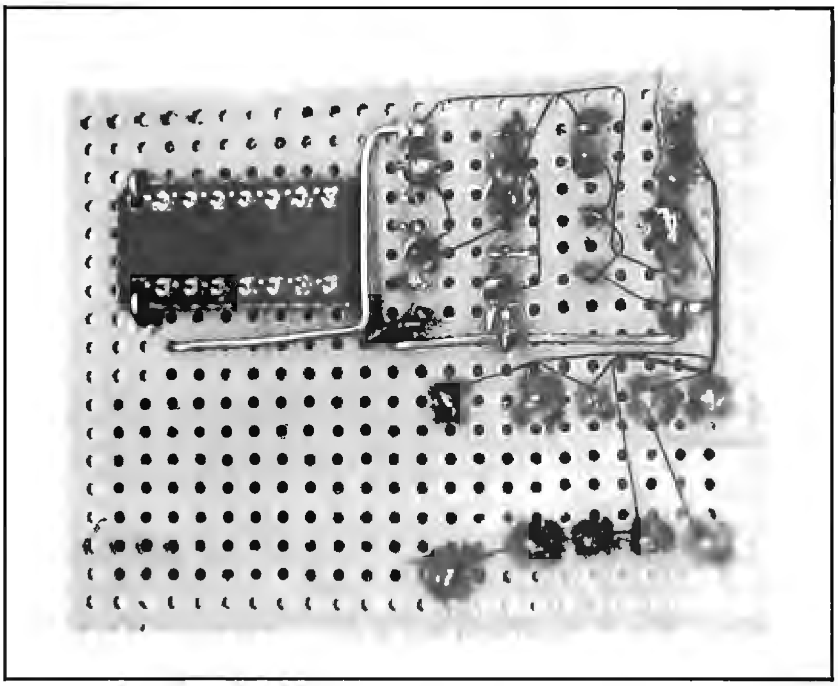


Photo 1b: Bottom view of the SwTPC 6800 processor clock speed modifier circuit.

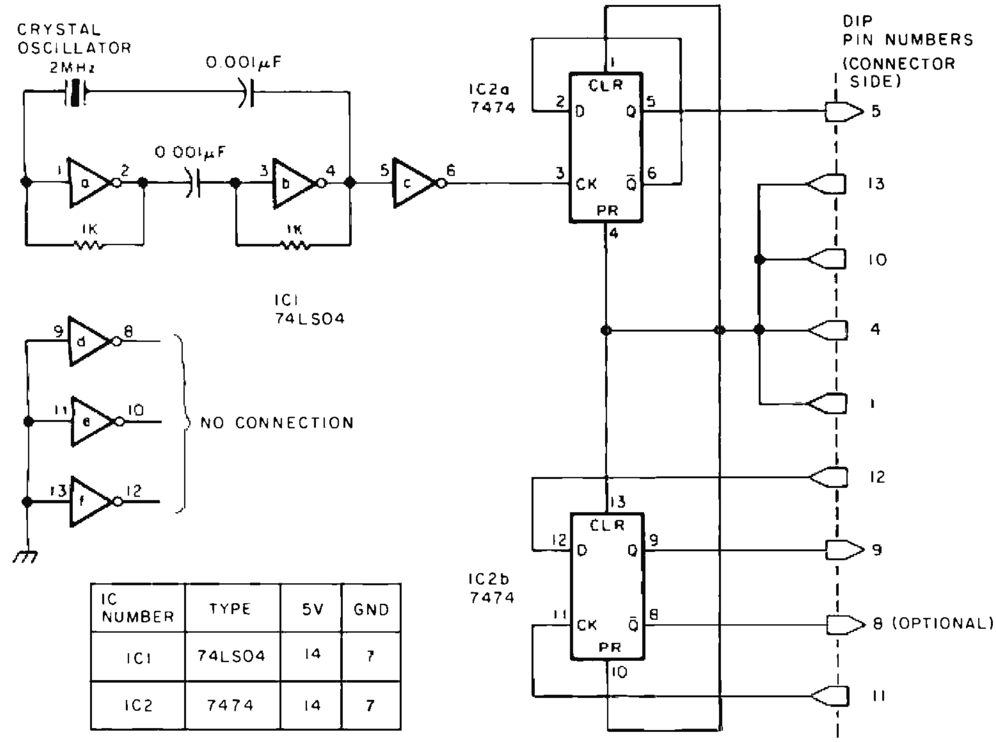
One of the design economies in the SwTPC 6800 is the use of the same clock to set data transfer rate and to control processing speed. It avoids the need to build a separate processor clock and reduces the processing speed by only 10 percent. For most applications, this speed loss is unimportant, but it can become important if you are interested in heavily processor based activities such as process control or robotics. It is also inconvenient if you use timing loops frequently, since it is more difficult to calculate timing loops which are based on a slightly more than 1 μs period rather than on an even 1.0 μs period for the processor states. Therefore, I decided a little "souping up" was in order.

The 10 Percent Solution

The processing speed of the SwTPC 6800 is governed by the data rate generator clock, which is based on a 1.7971 MHz crystal timebase. A 7474 flip flop is used to divide the data rate generator timebase down to provide the processor clock with its 1.11 μs clock period. By replacing this 7474 with a socket into which you can plug a 2 MHz crystal oscillator, you can provide the desired 1 MHz signal source. This oscillator can be built cheaply and simply on a small piece of perforated circuit board (see photos 1a and 1b). It provides a separate source for the processor clock without interfering with the data rate generator or the action of the 7474.

Memories used with a 1 MHz processor must have access times of no more than 500 ns. This means that, although all factory supplied memories should run at the increased processor speed with no difficulty, other memories may not. For example, 2102-2s will *not* work reliably at the higher speed. To simplify confirming that your memories are fast enough, I've included a table of access times for the more commonly available types of 2102 memories (see table 1).

One advantage of making this improvement in your system is that you are no longer limited to one unchangeable clock speed. If you want to use the 1.5 MHz or 2.0 MHz versions of the 6800 processor, ACIA (Asynchronous Communications



IC NUMBER	TYPE	5V	GND
IC1	74LS04	14	7
IC2	7474	14	7

Figure 1: Simple custom circuit that modifies the SwTPC 6800 computer so the user can change the processor clock speed by plugging in different crystal oscillators. The entire circuit can be mounted on a small perforated circuit board (see photos 1 and 2) which plugs directly into the SwTPC 6800 board in place of the existing 7474 data rate generator timebase divider.

Memory Number	Access Time	Usable at 1 mHz?
2102	1000 ns	No
2102-1	500 ns	Yes
2102-2	650 ns	No
2102A	350 ns	Yes
2102A-2	250 ns	Yes
2102A-4	450 ns	Yes
2102A-6	650 ns	No
2102AL	350 ns	Yes
2102AL-2	250 ns	Yes
2102AL-4	450 ns	Yes

Table 1: Some commonly used memory integrated circuits (ICs) and their compatibility with a 1 MHz processor speed.

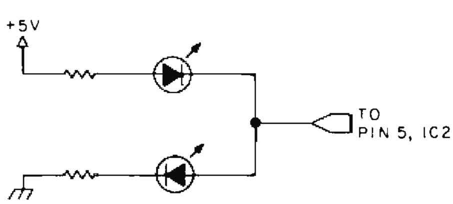


Figure 2: Simple test rig to verify that the oscillator circuit (shown in figure 1) is working. Both LEDs should light up when connected to pin 5 of IC2.

Interface Adapter), PIA (Peripheral Interface Adapter), and the like, which are currently available, you can adjust the timebase simply by replacing the 2.0 MHz crystal with one specified at 3.0 MHz (for a 1.5 MHz processor clock) or at 4.0 MHz (for a 2 MHz processor clock). Increasing the processor speed above 1 MHz will necessitate replacing (or adding a slow memory interface for) memories not suited to the increased speed, and replacing the MIKBUG read only memory (not currently available in higher speed versions). But for some applications the increased speed is undoubtedly worth the effort.

Building the Oscillator Card

The schematic shown in figure 1 indicates how the oscillator card works. This is one of the most common circuits of its type and was chosen for its simplicity. The parts as shown in photo 1a are mounted on top of the board and the connector (a 14-pin DIP [dual in line package] header) mounts underneath with its upper pins sticking through the top of the board. The reverse of the board is seen in photo 1b.

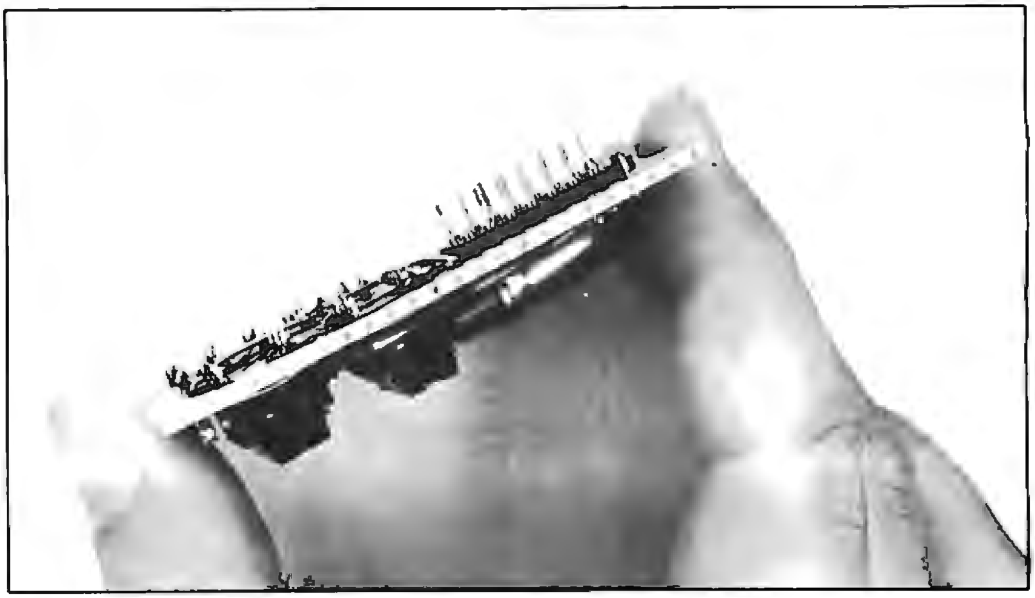


Photo 2: Side view of the clock modifier circuit, showing the pins of the dual in line connector (DIP) plug, enabling the experimenter to plug the entire board into the SwTPC board in place of the existing 7474 flip flop, which serves as the data rate generator timebase divider.

All the components of the oscillator fit nicely on a 2 3/8 inch by 1 1/2 inch (6 cm by 4 cm) piece of perforated circuit board, but the components must be carefully placed to avoid conflict with the components on the processor board to which it is attached. One satisfactory arrangement is shown in photos 1a and 1b. The wiring arrangement on the card is not critical so long as the wires are correctly connected to the connector pins. Capacitance values also are not critical. Any value from 0.001 μF to 0.1 μF will probably work. The entire board then plugs into the SwTPC 6800 board in place of the existing 7474 (see photo 2 for a side view of the DIP plug).

This is largely a foolproof card and should work as soon as it is assembled, but testing can do no harm and provides additional certainty that all is well. A simple test rig using two resistors and two LEDs, such as the one shown in figure 2, lets you verify that the oscillator is oscillating.

Conclusion

The increased processor speed which results from this modification offers benefits in any heavily processor based application. The circuit shown on the card is also convenient as a 1 MHz source for any other development work you may be doing. As an inexpensive way to solve processor speed problems, it's hard to beat.■

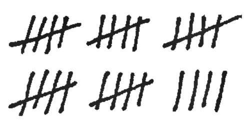
Circle 400 on inquiry card.

Continued from page 6

it had only the usual audio tape cassette interface for mass storage, and television for display purposes. (I have since ordered and received a floppy disk drive, which was plugged in and working within five minutes of setup.)

The immediate spur to writing this practical program was the need to analyze the editorial preferences section of the BYTE 1978 reader survey. This section, like the monthly BOMB analysis of articles in BYTE, gave a number of entries for which the respondent to the survey indicated a preference on a scale of 0 to 10. In the case of the survey, my goal was to find out what readers were interested in, so there was a list of 38 categories of interest to be rated 0 to 10. Each respondent's individual scale differs, but the idea here is to average the ratings of a large number of individuals and thus approximate an overall preference ranking. In the case of the survey, 2457 people responded out of 5000 subscribers picked at random from our mailing list.

In our monthly BOMB analysis, the ratings are acquired by the time-honored method of tallying with strokes on paper in groups of five strokes. Thus when Wai Chiu Li takes a monthly break from his normal job of "final paste" preparation for BYTE in order to tally the BOMB cards on a large sheet of paper, he accumulates strokes, thus:



In the survey analysis, with 2457 forms returned, our data processing contractor, Systemetrics, performed the keystroking of data and produced a report giving a count for each rating 0 to 10 in the 38 different categories of the preference survey.

Articles Policy

BYTE Publications Inc is continually seeking quality manuscripts written by individuals who are applying personal computer systems, designing such systems, or who have knowledge which will prove useful to our readers. For a more informal description of procedures and requirements, potential authors should send a self-addressed, stamped envelope to BYTE Authors' Guide, 70 Main St, Peterborough NH 03458.

Articles which are accepted are purchased with a rate of $45 per published page, based on technical quality and suitability for the intended readership. As to articles appearing in BYTE magazine, each month, the authors of the two leading articles in the reader poll (BYTE's Ongoing Monitor Box or "BOMB") are presented with bonus checks of $100 and $50. Unsolicited materials should be accompanied by full name and address, as well as return postage. ■

But this raw data is not the desired result. For the monthly BOMB analysis and for the survey analysis, I need a program which produces the following derived data from the input of ten counts (I exclude the 0 rating case) in n categories:

- Weighted sum total rating for each category.
- Mean and standard deviation over the field of ratings.
- Sorted rankings of each category by weight.
- Deviations for each category in units of one standard deviation.

The previous method of analyzing these results was to use a Commodore PR-100 programmable calculator, which has a mean and standard deviation calculation built into it. But this suffered from a number of awkward disadvantages. The procedure was essentially manual, with minimal automation through the use of the programmability of the calculator. The calculator has no way to enter enough data for the whole analysis, or to edit that data if a mistake is made, or to verify that data by examining details. Use of a calculator required an "expert" who knew the process, in order to accomplish the goal: calculation of mean, standard deviation, sorting of the categories by weight, and calculation of relative deviation from the mean for each category. With only 10 to 15 items I had put up with this procedure for a long time, but the prospect of 38 items and no way to verify the detail entries was not encouraging.

Thus I proceeded to create a program. Since the Apple II was the computer available to me in my office, I wrote the program using the Applesoft BASIC interpreter (Microsoft's product in Apple II clothing) as the high level language. It took me all of about five hours on July 11 1978 to go from the intention to a working BASIC program. If I had had the floppy disk accessory at the time, the result would have been even quicker since I would not have had to put up with the relative inconvenience of the audio tape mass storage system. Since this program was the first extensive one I have written in the Microsoft dialect of BASIC, I had to read the manuals as part of that process of creating the program. (Apple *II's* Applesoft interpreter is essentially identical to the Radio Shack Level II interpreter, the Commodore PET interpreter, and interpreters available for OSI and MITS Altair machines. All were written by Bill Gates and his associates at Microsoft Inc.) As many readers no doubt know, the language

Circle 140 on inquiry card.

was more than adequate to the task. Pascal it is not, but *any* high level language is better than no high level language.

So, with all the preparation carried out, and a program verified, I was able to analyze the 38 categories of preferences included in our survey, and proceed to begin analyzing BOMB results the same way.

Let's take a look first at what readers of BYTE found of interest based on our survey. The task presented to our survey participants was the following:

> *The following list contains a selection of topics drawn from computer science, mathematics, science and engineering. Please give your personal rating from 0 (no interest) to 10 (high interest). If a particular field within this list is your professional or occupational specialty, please record a check mark in the "Primary Interest" column to the left of the line. If you have already used a personally owned system for at least one nontrivial application in the field, please record a check mark in the "Have Implemented" column for that line.*

The complete list of 38 topics is presented in table 1, ranked according to weighted total count, along with the actual weighted total counts and a fraction representing the number of standard deviations away from the mean of 38 categories. The mean weighted count total of the 38 categories was 8579.5, and the standard deviation calculated was 1977.9.

The top ranked category was rather nebulous: "applications to everyday life." Thus its 2.2 standard deviation rank may be less than significant. If the survey had asked for a ranking of "motherhood and apple pie" the result might have come out the same. I tend to think that the whole motivation for having a personal computer is to use it in everyday life, and it is always a great ego trip to have such an appraisal measure out at the top. Household automation with computers is one way to accomplish such a task, and is also a fitting subject for the experimenter. Personal data base design is a natural, ranging from the oft mentioned kitchen recipe file to the record collector's inventory to the maintenance of tax records. The latter of course overlaps on the application of personal computers to personal business.

In the experimenter's corner, there is a high interest in voice recognition by computers. But no pattern matching and recognition of sounds is possible without heavy emphasis on the art of programming, a topic which turned up as the sixth ranked item.

Once the "compleat" home computer experimenter has mastered the voice recognition and programming arts, what more natural test application than some of the neat logical games ranging from computer chess and the game of Go, on downward in complexity.

In the top ten, the last three items are perhaps a trio of related interests (which also are related to the other members of the top 10 set). Voice synthesis by computers complements voice recognition, yet is an easier task than voice recognition and perhaps less of a challenge as a result. The art of hardware design is required in any event for work in the more action oriented real time applications of computers such as voice experiments, household automation and control of mechanisms.

And of course, the general interest in robotics enters into the top 10 category in the form of computer control of mechanisms. Most of the challenging but little understood topics enter into the picture in the second ranked ten categories of the survey. Here we find graphics topics, the first entry of artificial intelligence topics into the ranking, etc.

A surprise (in view of this issue's chess theme) was the slightly negative rating of chess relative to the mean. The bottom ranked item (related to chess) is the artificial intelligence category of theorem proving. Also included in the bottom ten interest areas were other topics related to abstract artificial intelligence. What is surprising, though, is the fact that for people to be practically interested in robots, this relatively abstract theory of knowledge and its representation is absolutely essential. Perhaps we have here the indication of a need for some good tutorial articles about these quite essential fields—to say nothing of some practical demonstrations of concepts which can be exercised by the personal computer user.

In summary, the program worked out just fine for measuring the data of the survey. Although not covered in any great detail at this point, the BOMB analysis figures beginning in the September 1978 BYTE were created using this program. And now that I've completed the editorial and the floppy disk is working, I'll think of some other tasks for my intellectual servant to do.■

BYTE's Bugs

A Bug in the Scanner

A small bug crept into Steve Ciarcia's article, "Let Your Fingers Do the Talking: Add a Noncontact Touch Scanner to Your Video Display" (August 1978 BYTE, page 156). The Q output of IC20 in figure 2d (page 163) should be shown as pin 6, not pin 1.■

BYTE's Bits

A Call for Papers:
Reliable Software Conference

The IEEE's Technical Committee on Software Engineering is seeking papers on specifications of reliable software, to be presented at their conference in Cambridge MA, April 3 thru 5 1979.

Suggested topics include: the theory of, and experiences with, formal specification languages; disciplined specification methods; verification of the consistency and completeness of specifications; quality, adequacy, and usefulness of specifications; and future research directions.

Deadline for submitting papers is November 1, 1978. Contact Marvin Zelkowitz, Dept of Computer Science, University of Maryland, College Park MD 20742, (301) 454-4251.■

Eighth World Computer Congress

The Eighth World Computer Congress (International Federation for Information Processing Congress 80) will be held jointly in Tokyo JAPAN from October 6 thru 9 1980 and in Melbourne AUSTRALIA from October 14 thru 17 1980. The Congress will be a gathering of computer scientists, managers, and administrators from all over the world. It will bring together both developers and users of information processing techniques and systems to share their knowledge and experience with colleagues from widely dispersed lands. The Eighth World Computer Congress will feature technical state-of-the-art developments in presentations on technology, equipment and applications, prepared by technical experts from approximately 35 countries. In addition, more than 100 international companies are expected to exhibit their products and services. In both Japan and Australia the Congress will also feature special events and entertainment. Write to Eighth World Computer Congress, Datapro Research Corp, 1805 Underwood Blvd, Delran NJ 08075.■

Clubs and Newsletters

South African Computer Club

We have heard from the Transvaal Amateur Computer Club, a South African club founded in June 1977. They currently have 120 members and publish a monthly newsletter called *TAC²* which they would be pleased to exchange for newsletters from clubs based in the US. The club project is the design of a M6800 microcomputer that can be manufactured locally. This club meets every first Wednesday at 8 PM, Senate House, Witwatersrand University, Johannesburg SOUTH AFRICA.

Help Wanted

A group of computer enthusiasts from Singapore need some assistance in starting a computer club in that area. They are requesting advice from existing clubs about how to get a club started and would like suggestions about a meeting format. Additionally, they would welcome technical information in the form of manuals, brochures and catalogs from manufacturers. Write to Steven Goh, 3 Bristol Rd, Singapore 8 SINGAPORE.

Washington Area KIM Enthusiasts

Formed in January 1978, the Washington Area KIM Enthusiasts meet monthly at the McGraw-Hill Continuing Education Center in Washington DC. Meetings are scheduled for the third Wednesday of every month to discuss items of interest to KIM owners and users. To receive a copy of the current *WAKE* newsletter, send a stamped, self-addressed envelope to *WAKE*, c/o Ted Beach, 5112 Williamsburg Blvd, Arlington VA 22207, (703) 538-2303.

Attention: Xitan/TDL Owners

A user's group for owners of Xitan/TDL hardware and software has recently been formed. A bimonthly newsletter is available on a $5 annual subscription basis, and its contents include application programs, hardware and software modifications, classified ads, technical articles and software exchange. For further information, write to Xitan User Group, c/o Bill Machrone, 121 N Av, Fanwood NJ 07023.

The New York Amateur Computer Club

The New York Amateur Computer Club meets on the second Thursday of every month at Bernard Baruch College, 17 Lexington Av (corner 23rd St), New York, room 903 at 7 PM. For further information, write The New York Amateur Computer Club, POB 106, Church St Station, New York NY 10007.

Monthly Newsletter Provides Reader Services

The *Personal Computer News* is a monthly newsletter dedicated to a variety of reader services. *PCN* features a regular news column detailing developments in the microcomputer industry, product and software evaluations geared to the small businessman and hobbyist, a software exchange and "Trading Post" classified advertisement section. A software sources listing culls the latest offerings from the microcomputer media and an index to computer related articles cross reference features in computer magazines. The subscription rate is $9 per year in the US. For more information, write to *Personal Computer News*, POB 425, Dayton OH 45419.

Digital Group User's Organization in Chicago

A Digital Group user's organization was formed in the Chicago area in February of this year to provide a forum for the exchange of ideas, software, fixes, etc, by owners of Digital Group computer systems. They meet on the last Tuesday of the month in the meeting room of Consumer Systems, 2107 Swift Rd, Oak Brook IL, at 7:30 PM. Membership dues are $5 annually which includes a newsletter. The newsletter is currently running about four to six pages and contains news of activities of club members, announcements of Digital Group compatible hardware and software and articles and reviews by members of the club. Prospective members can write to The Digital Group Group of Chicago, c/o W L Colsher, 4328 Nutmeg Ln, Apt 111, Lisle IL 60532.

TCH IMP-16 Users Group

TIPS is a fairly new publication which focuses on the TCH IMP-16 system. To date, this newsletter has informed its readers of the status of the system including what is available and from whom, where parts of interest are available, basic knowledge about building the system and additional hardware details. Frederick Holmes, editor of *TIPS*, has also mentioned that the upcoming issues of the newsletter will be expanded to support SC/MP based systems. Subscriptions to *TIPS* numbers 5 thru 7 are available for $1.50 and three SASE; back issues are $.50 and 1 SASE for each issue desired. Write to Fred Holmes, 101 Brookhead CT, Mauldin SC 29662.

Utah Computer Association

The *μCa* is a monthly publication of the Utah Computer Association, an association dedicated to hobbyist interaction and public education about minicomputers and microcomputers. The club meets the second Thursday of each month at 7 PM in room 131, Murray High School, Salt Lake City UT. The membership fee is $5. For more information about this club, call (801) 278-1907.■

Event Queue

October 5, Minicomputer and Microcomputer Seminar, Bluefield State College, Bluefield WV. This 1 day seminar and exhibition will feature business and engineering applications of minicomputers and microcomputers. The seminar will be conducted in the morning and afternoon and exhibits in the afternoon and evening. Contact Dr Alvin Hall, director of continuing education, Bluefield State College, Bluefield WV 24701, (304) 325-7102.

October 5-8, Midwest Personal Computing Show, Apparel Center's Expocenter, Chicago IL. More than 200 displays featuring the full spectrum of the latest personal computing developments are expected to be presented by manufacturers and distributors. The comprehensive program includes seminars, forums and practical application classes. Contact Midwest Personal Computing Exposition, ISCM, 222 W Adams St, Chicago IL 60606, (312) 263-4866.

October 9-13, Microcomputer Workshop, Carnegie-Mellon University, Pittsburgh PA. This intensive 5 day course is for individuals interested in applying microprocessor systems to a practical problem. Theory as well as practical experience will be emphasized in order to learn the capabilities and limitations of microcomputers and what it takes to apply them on the job. Contact Gerry Cohen, Post College Professional Education, Carnegie Institute of Technology, Carnegie-Mellon University, Schenley Park, Pittsburgh PA 15213, (412) 578-2207.

October 25-27, International Computer Retailers Conference, Chicago IL. The main purpose of this conference is to provide existing and future computer dealers with an in-depth look at the opportunities and pitfalls for developing sales and profits in computer retailing. For more information contact registration manager, Management Research Associates, 60 East 42nd St, New York NY 10017, (212) 687-2560.

October 27-29, BizComp '78, Marriott Motor Hotel, Atlanta GA. BizComp '78 will highlight the small budget necessary for the independent business operator to be able to purchase an in-house computer system. All facets of the small business computer industry will be on display from the latest innovations in computers to business software and word processing, supplies and services. Contact Felsburg Associates Inc, 12203 Raritan Ln, POB 735, Bowie MD 20715, (301) 262-0305.

October 31-November 3, Tulsa Computer Conference, Skyline Sheraton East, Tulsa OK. Contact Tulsa Chapter Association for Systems Management, 4110 S 100 East Av, Suite 128, Tulsa OK 74145.

November 3-5, Third West Coast Computer Faire, Los Angeles Convention Center. This is a conference and exposition on personal computers for home, business and industry. For more details about this computer faire, write for a free copy of the Silicon Gulch Gazette. Contact Computer Faire, POB 1579, Palo Alto CA 94302, (415) 851-7075.

November 5-8, Computer Applications in Medical Care, Washington DC. This IEEE sponsored symposium on computer applications in medical care is designed to inform physicians and health care professionals about current and potential applications of computer technology to patient care; and to identify areas of future research and development that need to be addressed. Contact Abund O Wist, PhD, general chairman, Medical College of Virginia, (804) 770-4957.

November 6-8, Asilomar Conference on Circuits, Systems and Computers, Asilomar Hotel and Conference Grounds, Pacific Grove CA. This conference, sponsored by the IEEE Computer Society, will delve into areas such as circuit theory and design, communication and control systems, computer systems, computer aided design, etc. Contact Donald E Kirk, Electrical Engineering Dept, Naval Postgraduate School, Monterey CA 93940.

November 13-16, COMPSAC, The Palmer House, Chicago IL. The IEEE Computer Society's second international computer software and application conference. This conference will bring together computer practitioners, users and researchers to share their ideas, experiences and requirements for applications software, management techniques, and software development support, including automated techniques. Contact Wallace A Depp, executive director, Processor and Computer Software System Division, Bell Laboratories, Naperville IL 60540, (312) 690-2111.

November 19-22, The 11th Annual Microprogramming Workshop, Asilomar Conference Ground, Pacific Grove CA. This worksop will provide a forum for the discussion and comparison of design techniques for firmware and for the supporting hardware. Informal interaction between groups working in similar research and application environments will highlight the topical session. For more information contact Dr Alice G Parker, Micro-11 program chairman, Dept Electrical Engineering, Carnegie-Mellon University, Pittsburgh PA 15213, (412) 578-2472.

November 27-December 1, Micro Programming Workshop, Lafayette IN. This 5 day hands-on advanced programming workshop is for individuals interested in developing skills required to plan, prepare, test and document 6800/6801 microprocessor applications software. Contact Jerilyn Williams, Wintek Corp, 902 N 9th St, Lafayette IN 47904.

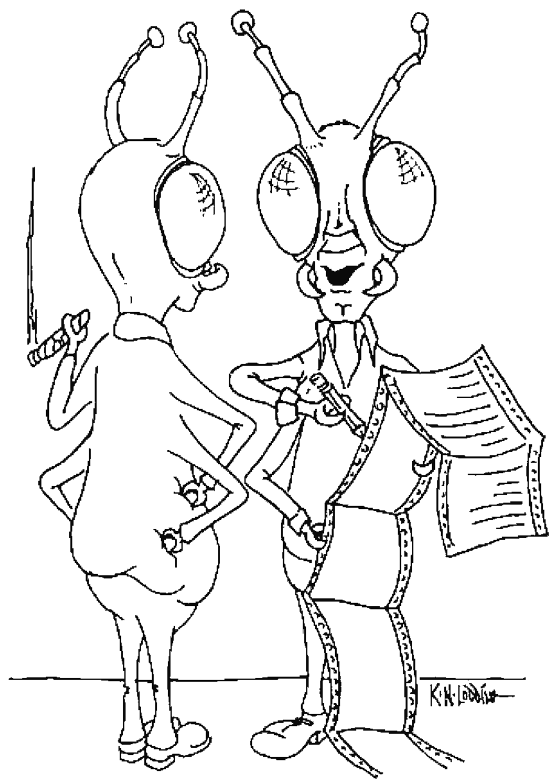
November 28-30, 9th Annual Canadian Computer Show, International Centre, Toronto CANADA. Products displayed at this show will include: computer and data processing equipment, supplies and services, including minicomputers, peripheral hardware and software, keypunch services, consulting and contract programming and timesharing. Contact Industrial Trade Shows of Canada, 36 Butterick Rd, Toronto Ontario M8W 328, (416) 252-7791.

December 3-5, Ninth North American Computer Chess Championship, Sheraton Park Hotel, Washington DC. The 1978 annual meeting of the Association for Computing Machinery will be the site of this chess championship. This will be a 4 round Swiss style tournament with participants restricted to computers. Two rounds will be played on December 3 (1 PM and 7:30 PM), one on Monday (7:30 PM) and the last round on Tuesday (7:30 PM). Deadline for entries is October 20. Contact Prof M M Newborn, School of Computer Science, McGill University, Montreal Quebec H3A 2K6 CANADA.

December 12-14, Midcon/78, Dallas Convention Center, high technology electronics show and convention. Contact Electronic Conventions Inc, El Segundo CA, (800) 421-6816 (toll free).

December 13, Computer Networking Symposium. Sponsored by the IEEE Computer Society's Technical Committee on Computer Communications and the Institute for Computer Sciences and Technology of the National Bureau of Standards. This symposium will highlight papers of practical and research experiences concerning both computer and communication networks. Contact Dr George Cowan, Computer Sciences Corp, 6565 Arlington Blvd, Falls Church VA 22046.■

Cartoon by
K N Lodding



"I think I found the human in your code."

Continued from page 10

A TALL ORDER, BUT IN PRINCIPLE DOABLE...

I am an experimental psychologist and have purchased a Radio Shack TRS-80 microprocessor for research purposes. I've run into some of the following problems. First and foremost I am having difficulties in setting up the following as an experiment. I would like to present either a letter, word or object on the screen for 100 ms or more. This is an easy thing to do in Radio Shack BASIC. The observer's task is to respond as quickly as possible by pushing one of two keys (either a 1 or 0) based on what was presented. I am having trouble computing the reaction time, the interval of time lapsing between stimulus presentation and the response. The program should be able to measure the reaction time in ms and record which response was made. Could you offer some assistance on developing such a program?

My second problem is how to convert my TRS-80 so that I can use a television instead of the Radio Shack video screen. This would allow the use of an S-100 bus and the Cromemco Dazzler for color video.

A third problem I've run into is the following: research-wise I am into workload measurement or dual task analysis. Using a normal television I've hooked up a pong game. I would like to present simultaneously by means of the TRS-80 a list of words for the observer to memorize and recall while the pong game is on. How can one go about doing this?

Fourth, I believe the cassette transfer program for the TRS-80 is limited in that I must transfer all the information on the tape into memory. Is there no way to run a search and only transfer part of the information on the cassette tape into memory?

Finally, I am interested in determining why one needs to buy the Radio Shack interfaces for memory expansion purposes. Why can't one buy an S-100 bus and mother board and additional static memory and accomplish the same thing at a lower cost?

If one of your readers can help me with these matters, please let me know.

Asst Prof Joseph Dalezman
New College of USF
Division of Natural Sciences
5700 Tamiami Tr
Sarasota FL 33580

We suggest that you get in touch with your nearest local computer club (see Clubs and Newsletters Directory, September 1978 BYTE, page 124).

TIMELY COMMENTS ON KIM

I just tried Robert Baker's KIMER (KIMER: A KIM-1 Timer, July 1978 BYTE, page 12). The clock operated but the calibration was not wide enough for my crystal.

Since the BIT instruction (line 0220) is used to test the timer status, the timer is not being used in the interrupt mode even though memory location 170F was loaded. The status of PB7 in this case has nothing to do with the timing. The major time delay is determined by the JSR SCANDS command which takes several milliseconds to perform. The timer status is tested on each return from SCANDS and so will always be some multiple of this time delay. The 1 ms calibration resolution cannot be obtained.

Here are a few ways the program could be fixed:

- The clock could be written as an interrupt routine. SCANDS would then be interrupted at any point in the subroutine.
- The number of JSR SCANDS commands could be counted in a loop which would be exited before the timer times out.
- The calibration could be reduced to EF or F0 and a longer fine adjustment used.

There have been several programs in the *KIM-1 User Notes* which illustrate the use of the timer. My version of a clock using the interrupt mode was printed in the March 1977 *User Notes* and also in *The First Book of KIM*. When using the program in the latter publication, go by the detailed listing since line 036A is incorrectly printed in the HEX DUMP.

I hope this is of help.

Charles H Parsons
80 Longview Rd
Monroe CT 06468

A SwTPC 6800 FIX

Here is a problem with the SwTPC 6800 and a fix that I haven't seen published before:

You can't reset the 6800 from a wait-for-interrupt state!

On the SwTPC MP-A board, the reset signal is transmitted to the MCM6800 chip via a DM8098 hexadecimal inverting three state buffer that is disabled when the processor enters a hold condition, as occurs after the execution of a WAI (3E hexadecimal) instruction. Once the 6800 is in the wait state, the reset signal generated by pushing the front panel reset button is stopped at the 8098 and never gets to the 6800 chip. A hardware fix is to break the traces to pins 2 and 3 of the 8098 (labeled IC15 on the SwTPC schematic and parts layout) and reroute the signal through a new, permanently enabled 8098. This permits the reset signal to reach the 6800 and you can then recall your 6800 from the "never-never land" it inhabits after performing a WAI.

I hope this will help anyone who's been annoyed by his SwTPC not responding to reset on mysterious occasions. I don't know if SwTPC fixed this on their new MP-A/2 board or not.

William R Hamblen
946 Evans Rd
Nashville TN 37204

PERSONAL COMPUTER COMMUNICATIONS NETWORK

I was certainly surprised by the degree of negativity expressed by Donald Newcomb, commenting on my article ("Personal Computers in a Communications Network," February 1978 BYTE, page 80) in the July 1978 BYTE. Perhaps some comment is in order.

First, I certainly do not wish to characterize a distributed communications network as anything less than highly complex. However, I do believe that in principle these complexities can be solved with a combination of sophisticated software and straightforward hardware. What makes a problem like this particulary difficult is that it is not isolated in the same way that the development of a language processor or operating system can be isolated. The first step in the creation of complicated software interfacing to a myriad of systems has to be communication in generalities. In that spirit I welcome Mr Newcomb's comments.

A second large point is made by Mr Newcomb that such a scheme runs contrary to the sensible regulation of the radio spectrum. Again, I acknowledge the difficulties, but I would like to mention that Dr John deMercado, head of Canada's Telecommunication Regulatory Service (analogous to the FCC) and an early developer of ARPA, characterized my article as "forward thinking" and has solicited my further opinions. Perhaps regulatory agencies are not quite as committed to maintaining the status quo as Mr Newcomb assumes.

On the specific question of "Why not use the phone?", I believe there are several responses. First, I agree that the phone system is fine for well-defined transfers between two individuals. But, there is a strong possibility that "Ma Bell" will soon begin charging data communications automatically at a different rate. Further, and this is the primary point of the article, new types of network activities will evolve if the environment is open-ended.

Finally, it is simply not true that unsupervised transmitters are rarely approved by the FCC; there are hundreds, if not several thousand, VHF and UHF repeaters operating in the amateur bands on a 24 hour basis with only periodic maintenance. When the FCC modified its regulations for commercial broadcasters to allow operation over a remote control link by nontechnical personnel, a clear statement was made that the Commission felt that the technology had progressed to the point that broadcasters should no longer be burdened by unnecessary rules. Yes, it was still possible that there might be situations where an on site technician would save the day, but the FCC seemed willing to take the risk in that case. I would prefer to think positively about the matter and hope that the FCC will view networks as another case where the benefit can outweigh the risk.

I am not certain that the network structure I have discussed is workable, but I do know that it can never work without a beginning. I am slowly working toward such a beginning, and I hope that others will as well.

Jeff Steinwedel
715 Reseda Dr, Apt 2
Sunnyvale CA 94087

PERSONAL COMPUTERS REQUIRE INSURANCE, TOO...

In shopping around for insurance on my house (renewal due in August), I discovered that none of three large insurance firms in this area would cover—specifically—a personal computer of any significant value. None of the three would add any rider or offer any separate insurance coverage. The general concensus was that personal computers were considered no more than "hi-fi" equipment.

The specific area of insurance on a personal computer does not affect me yet since I am just starting to collect the components for a fairly large system. Medium to large microcomputer systems can run from \$3 K to \$8 K, the price of a new or nearly new auto.

Auto insurance is commonplace and there is a good reason for it. Only part of such insurance is devoted to the auto itself. Home insurance covers only part of personal property within a dwelling and is generally covered as half the amount of the dwelling itself. With the increase in overall prices, replacement of personal property will probably not cover a system of \$3 K or greater. This is especially true in a household having expensive relatives such as children.

Perhaps some reader might comment on insurance for such expensive devices?

Leonard H Anderson
10048 Lanark St
Sun Valley CA 91352

Where there is demand, the marketplace is sure to follow. Here is a niche for some enterprising underwriter.

REGIONAL BASIC CONTEST NOTES

Thank you for the nice article in the July 1978 issue of BYTE about the regional BASIC contest. I would like to make a couple corrections. First, Scott Parker is really Scott Porter, and the second man was Newton B White Jr of St Louis MO. Mark Grundler, the advisor, was unable to make the trip.

If the truth must be known, it was Newton, and not Porter, who led the team. He spent the weekend teaching BASIC to Scott, a situation which was a major handicap to the team's effort. I am happy to report that next year Grinnell will be able to field a team of four BASIC programmers.

White and Porter were members of Grinnell's FORTRAN team, which took second in this year's Midwest Regional FORTRAN contest and competed in the national FORTRAN contest. The other two members of the team were Bruce Albrecht and Steve McKelvey. Both Albrecht and McKelvey had strong permances to help the Grinnell team to a second place in its first outing. An interesting side note: at the FORTRAN regional, Porter taught White how to program in batch FORTRAN. Porter was a batch FORTRAN programmer and White was an interactive BASIC (redundant, but anything for a parallel construction) programmer, and both had the faults of each style. This last summer White was working in some batch environments and, likewise, Porter is working mostly with interactive BASIC.

Since Grinnell is a liberal arts college without an applied math or computer science major, it was necessary to go looking among the other majors for programmers. The makeup of the team was a math/philosophy double major, a physics major, and a chemistry/math major. The blend of that group's problem solving ability was its major asset.

Scott Porter
Office of Computer Services
Grinnell College
Grinnell IA 50112

SOME ACES NEED ENGINEERING

After reading your magazine avidly for a couple of years we felt we could write to you and request the assistance of you and your readers. First a few words about our aims: the Awareness, Consciousness and Energy Studies Group (ACES Group) is devoted to the scientific study of the various manifestations and attributes of consciousness. Today the "consciousness explosion" is well under way and more and more people are practicing some sort of technique to bring about an expansion of their awareness. Success becomes apparent through the subjective experience of joy and well-being. However, our society has long been indoctrinated with the need to provide objective proofs of every experience. We reasoned, as other groups have done, that an increase in awareness or a change in one's state of consciousness should have some corresponding effect on the body's physiology and therefore be physically detectable. Research during the last eight years shows that this is indeed the case. Stress is apparently the biggest hindrance to increased awareness. A reduction in stress shows itself in such ways as an increase in galvanic skin resistance (GSR), normalization of the blood pressure and increased alpha activity of the brain (to mention but a few). In order to study the effectiveness of different methods of reducing stress the ACES Group has developed its own equipment. Continuous monitoring of EEG, GSR, heart rate and body temperature is possible.

The outputs from our present monitoring equipment are eight analogue voltages which we wish to sample at not less than 100 times per second. This information should then be passed to our microprocessors for storage and analysis. For this purpose we have purchased two processors, one being the Digital Group Z-80 and the other the OSI Challenger; both have VDUs, four digital tape drives and in excess of 20 K memory.

Our main problem is interfacing the analogue monitoring equipment to our processors. Perhaps some of your readers with experience in analog to digital conversion could offer us some helpful suggestions. We welcome contact with anyone (professional or hobbyist) who has experience of biomedical monitoring systems and we are constantly on the lookout for methods of increasing the speed of computation. Another problem we have not yet resolved is that of designing a simple but accurate noninvasive method of monitoring blood pressure for use in a nonlab environment. Ideas, anybody?

Thank you for a most informative and interesting journal.

Graham Else, Ian Wales
ACES Group
Koenigsberger Straße 10
6107 Reinheim/Odenwald 1
WEST GERMANY

9900 DOWN UNDER

Living as we do on the other side of the world from where it is all happening on the microcomputer scene, we depend very heavily upon what we can read in the pages of BYTE and the other magazines. We can hardly tell you with what avid interest each issue of BYTE is perused (we get it shipped out to us airmail in order to get it as early as possible). Keep up the good work.

We ourselves use TMS-9900 based equipment, so every mention of this rare but wonderful beastie in your pages

Circle 77 on inquiry card.

evokes a heightened response of interest.

I would like to get in touch with users of 9900-based systems in the States so we can exchange notes, ideas, etc.

B Ward Powers
IMPACT Ltd
POB 177
Petersham NSW 2049
AUSTRALIA

A FEW NOTES FROM A CANADIAN READER

1. Items move faster through our mail system if you include the postal code. This is that funny series of letters and numbers that appear above, after the province. My postal code is V6S 1B2. Note that the format is letter, number, letter, *space*, number, letter, number. Although this may not be quite as simple as your ZIP code, it does mean that a letter addressed:

Andrew Bates,
Canada V6S 1B2

will be delivered to me. The postal code pinpoints the side of the street in a residential block or even the floor of a building in a business district. How's that for precision!

Software writers take note: we Canadians need at *least* six characters for the postal code and four characters for the province (state). And if you are going to check the ZIP for all numbers, please put the check in a subroutine so we can replace it with a suitable check for our postal code.

2. WATS lines do not cross international borders (at least that is what the telephone operator told me). This means that we people in Canada can't phone you for free like everyone else in the United States can. How about letting your people accept collect phone calls from Canada, only so we can use A G Bell's famous invention, instead of having to spend hours slugging away at the typewriter and then waiting for what is an erratic mail service on both sides of the border?

3. Another small request for software writers who are mailing things to Canada: if your package costs $75 and is distributed on North Star diskette, for instance, please mark the customs declaration as:

DISKETTE $6
PRINTED MATTER $69

If you mark the price as $75, we end up paying duty on the *diskette* as though it cost $75. Printed matter comes across the border duty free and there is no duty on an item of less than $10 value.

Andrew Bates
3261 W 18th Av
Vancouver BC
CANADA V6S 1B2

EROM CONFUSION: THE 2716

Elaborating on David Marke's letter (July 1978 BYTE, page 11), it seems to me that Intel bears the blame for the 2716 single voltage versus 3 voltage supply EROM confusion.

Intel gave their new generation 16 K part an old generation number. They have essentially acknowledged the confusion by introducing the 2758, a 1 K by 8 EROM like the 2708, but single

I suggest we use the Texas Instruments part number, 2516, when referring to either the TI part *or* the Intel 2716.

Al Anway
Poly Micro Systems Inc
2616 Lansing Dr SW
Roanoke VA 24015

IN SEARCH OF SPEED

There are some things that retard communication between people having no contradictory interests, eg: vendor and customer. Vendor has something to sell. Customer finds something to purchase.

One of these retarding things is a slow answer to a request. Surface mail for Sweden travels the distance from the United States in six weeks. Air mail, the same distance, arrives within a week.

So please, if at all possible, use air mail for overseas requests.

Hans Nordström
Tingvallavägen 7F
S-195 00 Märsta
SWEDEN

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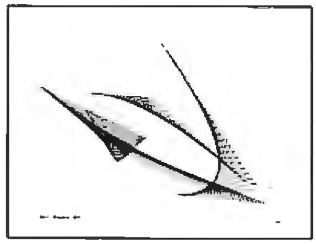
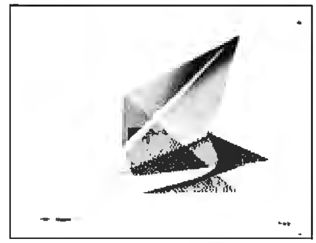


File 1



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A Novel Bar Code Reader

In the March 1977 BYTE, page 130, we announced a bar code reader contest in which readers were asked to decode a page of Paperbyte™ bar code copy using a reading technique of their own design. Winning points for originality was this entry by Campbell Farnell and Glen Seeds. While the method described here is not the intended method of reading the codes, it shows what is perhaps the world's least expensive drum read only memory as a serendipitous sidelight to printing software on paper.

Campbell Farnell and Glen Seeds
RR #1
Seeley's Bay, Ontario
CANADA K0H 2N0

Photo 1: The authors' bar code reader entry. The page of bar code is shown taped to a fruit juice can sitting on a phonograph turntable. The reading arm, shown at bottom left, features two small lamps and a focusing lens. Light reflected from the rotating bar code energizes a phototransistor at the other end of the reading arm. The signal is then translated into binary voltage levels and sent to the computer's input port.

Technical Description

Our Paperbyte™ bar code reader consists of three parts: (1) an old turntable set at 33 RPM on which sits the page to be read, attached to a 48 ounce juice can; (2) a read head with light source which is attached to a parallelogram assembly to allow the head to be moved up and down while remaining level; (3) an interface that brings the output of the phototransistor in the read head up to a 5 V digital level.

The Turntable and Juice Can

A juice can with one end removed supports the page while the turntable (a junked one obtained for free) rotates the page. For purposes of this contest we simply taped the page to the can. However, for everyday use some sort of clip-on system would be reasonable. Even four small magnets should work to hold the paper on the can. Centering the juice can on the turntable was no problem since the plastic record mat on the turntable platter has a series of raised concentric circles on it. On turntables lacking this feature it is an easy matter to draw a circle on a piece of cardboard placed on the turntable to indicate the proper position. In use, we found that the can did not tend to wander as the turntable went around.

```
            BLABBERWA
CKYww    Twas brilliant
 and   the   slimy  toads
wDid  go  and  gander  i
n  the  wave:wALL  mist
y  were  the  bluish  gr
oves.  wAnd  the  mole  r
uns     outraged.ww"Bewa
re  the  Blabberwack,
my  son!  wThe  words  th
at  bite,   the  barbs   t
hat  catch!  wBeware  th
e  mynah  bird,  and  sh
unwThe     frivolous    Ben
dersnitch!   "wwHe   took
 his    vicious    words    i
n  hand:wLong  time  th
e  slanderous foe he
sought--wSo       remained
 he   by   the   titling   t
ree,  wAnd  stood  awhil
e  in  thought.  wwAnd,
as    in    malign    thought
 he  stood,  wThe  Blabb
erwack,    with    eyes    of
 flame,    wCame    whistli
ng    through    the    state
ly  wood,  wAnd  bluffed
 as  it  came!  wwOne,  t
wo!,   One,   two!   And   t
hrough    and    throughwT
he    vicious    blade    wen
t  crushing--crash!  wHe
 left   it   dead,   and   w
ith   its   headwHe   went
 galloping   back.   ww"A
nd    hast   thou   slain    t
he  Blabberwack?  wCome
 to  my  arms,  my  boun
cing   boy!   wO   fabulous
 day!    Hoorah!    Hooray
!"wHe    chortled    in    hi
s   joy.   ww'  Twas  brilli
ant  and  the  slimy  to
adswDid   go   and   gande
r   in   the   wave:wAll   m
isty    were    the    bluish
 groves.  wAnd  the  mol
e runs outraged.w
```

Listing 1: Walter Banks' "Blabberwacky." The output was produced on a printer that does not respond to ASCII control characters, so the line feeds were printed as lower case ws.

The Read Head

The read head consists of a 2N5777 phototransistor, a lens and two penlight bulbs. These items were mounted on a block of wood. The lens we used was a 25 mm lens from an 8 mm movie projector, but any lens of similar focal length can be used because color rendition and edge focus are of no concern. The phototransistor was mounted on its side rather than vertically so that the lens effect of the T092 package would tend to pick up more of one particular bar rather than picking up adjacent bars. It was also covered with black tape on all sides but the front, to exclude stray light.

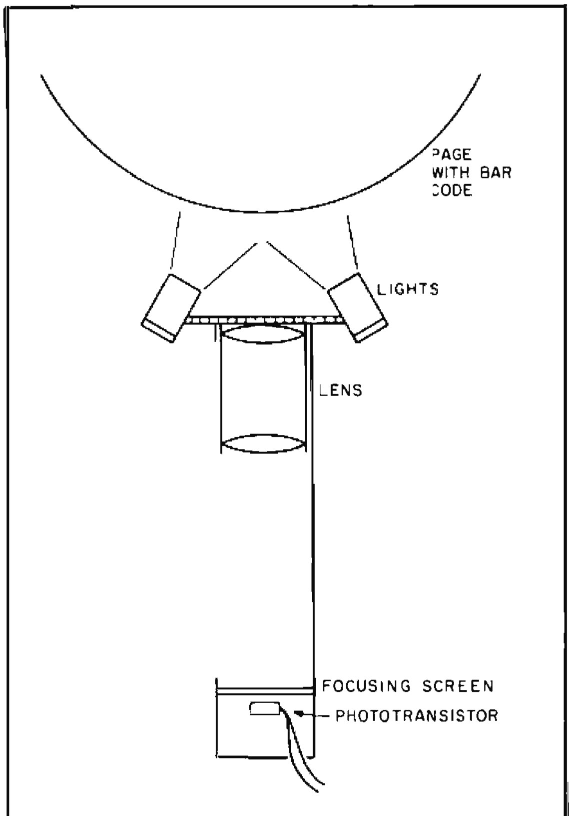

Figure 1a: Top view of the read head.

The phototransistor was mounted peeking through some translucent tape which served as a focusing screen. The entire assembly was covered on the top and sides with a cardboard hood to exclude ambient light. The block of wood on which the read head was assembled was attached to two strips of wood, which were in turn attached to a base. This allows us to move the read head up and down while keeping it level.

The system was focused by moving the the base plate back and forth. A pair of type 222 prefocused penlite bulbs were mounted on either side of the lens and angled toward the bar being read. These bulbs are rated at 2.25 V; when wired in series they ran fine from the +5 V used for the logic, and drew 250 mA. A strip of ordinary black tape was wrapped around each bulb to prevent stray light from reaching the lens.

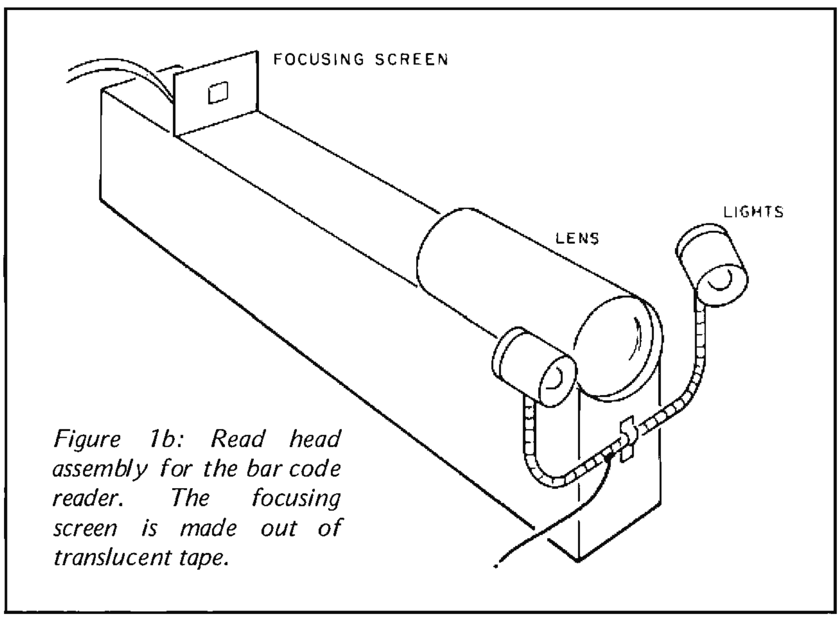

Figure 1b: Read head assembly for the bar code reader. The focusing screen is made out of translucent tape.

The Interface

The interface consists of a 500 k trimpot and a 74C04 CMOS hex inverter, as shown in figure 2a. Since the input port on our computer accepts CMOS logic, no further buffering was required. In order to drive standard TTL logic, the remaining CMOS inverters can be used or a transistor and two resistors (see figure 2b). This interface owes its simplicity to the high gain of the 2N5777 and the very high input impedance of the CMOS chip.

Calibration and Use

The calibration and use of this system are simple. Once physically assembled, the read head is moved close to the page to be read and is adjusted to bring the page into focus on the screen. This requires some experimenting at first. The phototransistor is positioned about 3 inches behind the lens, which provides a magnification of about 2. To adjust the sensitivity, focus the head and then, with the turntable turned off, turn the platter until the read head faces plain white paper. Observe the voltage at the collector of the phototransistor at point A in figure 2a. With a lot of light from the white paper on the phototransistor, and the potentiometer set to its highest value, this point is pulled low by the transistor. The potentiometer is adjusted until it just pulls the line high and then it is backed off just enough to let the line go low. This completes the sensitivity adjustment. While spinning the turntable by hand, you can watch the output of the transistor alternate. In our case we had a voltage swing of about 4 V at point A.

In order to actually read the lines, the output of the CMOS interface is hooked to a single bit of an input port on the computer. The computer then waits for a line to start, times the light and the dark times, and decides if the bit is a one or a zero. The computer program itself is straightforward, if somewhat long-winded. The computer we used is an MCM/800 manufactured by Micro Computer Machines, Kingston, Ontario. The processor is a discrete bipolar affair that has the same instruction set as the 8008, with a few enhancements.

Notes and Conclusions

Because this reader was produced and documented within a period of 48 hours, we did not have time to go through many revisions. From our experiences we gained a considerable amount of information that could be applied to the development of an improved reader.

When we set out to build the reader, we assumed that the mechanical portion would be easy and that most difficulties would be with the electronics. This was not the case. Although the entire electronic portion of our reader turned out to be extremely simple, (it cost under four dollars), it performed flawlessly. We have had no difficulties with it and we do not suggest any modifications. In one test performed while checking the reader, we read a single line 255 times without glitches.

The mechanical portions of the reader, however, could stand some improvements. Our most serious problem was keeping the read head focused on the page. The juice can was not perfectly round, particularly at the end with the top removed, and minor variations tended to put things out of focus at one end or the other of the line. The can had to be centered exactly on the turntable or similar problems would arise. Anyone seriously considering this approach might use a full unopened juice can, remove the turntable spindle and glue the can (after careful centering) to the turntable.

Probably the weakest link in the design is the head support mechanism, which we do not recommend. Given some sort of reasonably round support for the page, it would be nice to have the head permanently mounted on a slide arrangement so it could be focused once and then slid back and forth in front of the page being read. If you standardize on a fixed spacing for the lines, it would be possible to add a detent mechanism so that the head would stop only in the middle of lines. It would be reasonably easy to add some automatic method of advancing the head.

We feel we should also mention something that we discovered in the course of testing our reader. It applies to bar code readers of our type and to wands as well. As Keith Regli points out in his article "Software for Reading Bar Codes" (December 1976 BYTE, page 18), readers will tend to read light and dark areas of equal width as being somewhat different. Our reader was no exception, and in fact the amount of bias shifted from one part of the line to another as the focus changed a bit. This caused quite a bit of jitter in the light time to dark time ratios, which are, in theory, what is used to separate 1s from 0s. However, we also observed something that is of considerable use: while the light to dark ratio jittered a lot on our reader, the timing of a full bit (light time plus dark time) was very stable. This suggests an improved software decoding routine in which you can compare the total time (light plus dark) for the current bit with the total time of the previous bit. Since you know if the previous bit is a 1 or 0, you can determine what this next bit is by appropriate comparison. This automatically compensates for the jitter in the light to dark ratio introduced by the reader, and also allows tracking on wands where the time will tend to wander a lot.■

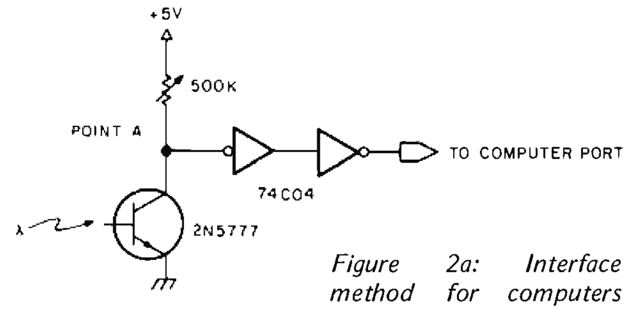

Figure 2a: Interface method for computers that accept CMOS logic.

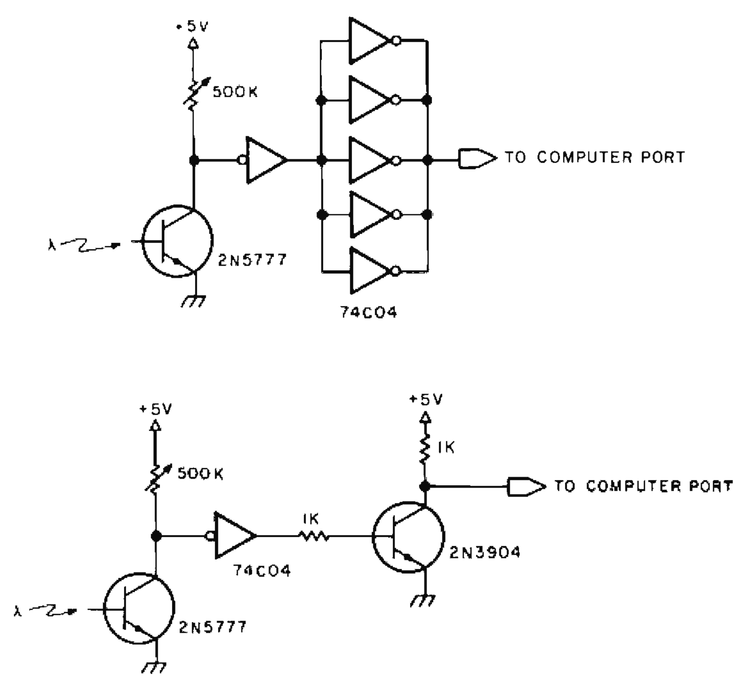

Figure 2b: Two interface methods for computers that accept TTL logic.

Product Description

Micro-Scan Corp Bar Code Scanner

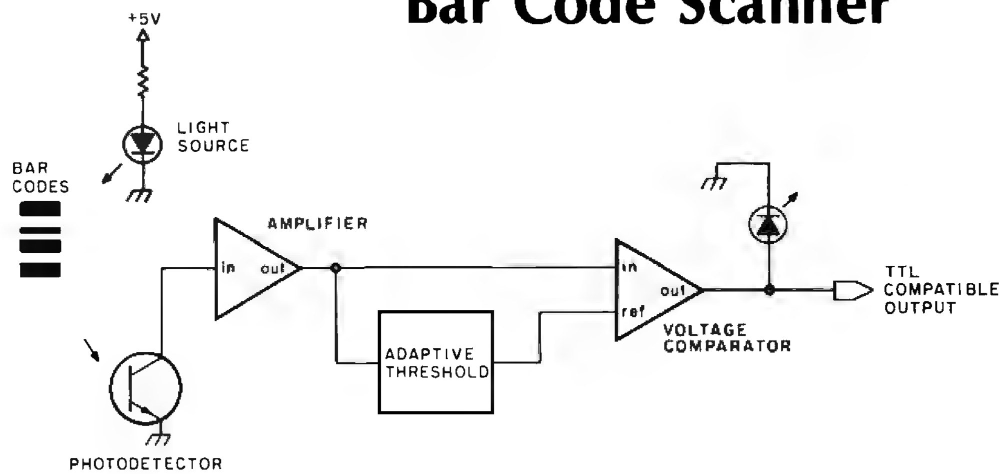

Figure 1: Functional diagram of the BCS-1 hand held bar code scanner.

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The Data-Scan bar code scanner is designed for reading bar codes such as those presented in BYTE. The scanner can read degraded bar codes (such as Xeroxed patterns) as well as black bars on a gray background or gray bars on a white background without adjustments.

Photo 1: Micro-Scan Corp bar code scanner. Circular area at left contains aperture for viewing bar codes.

Functionally, the scanner specifications include: a scanning rate of 10 to 40 inches (25.4 to 101 cm) per second, power supply requirements of +12 V at 50 mA, and a transistor-transistor logic (TTL) compatible output in the form of a serial bit stream suitable for application to an input port.

The scanner consists of a light source, a phototransistor and the signal conditioning circuitry shown in figure 1. The light source, an infrared light emitting diode (LED), illuminates the surface of the paper through an aperture slightly smaller than the area of a unit width bar. Viewing this same surface area through the aperture is a phototransistor. The transmitted and reflected light either passes directly through the aperture or travels through a bifurcated fiber optic cable as described in my article, "Signal Processing for Optical Bar Code Scanning," December 1976 BYTE, page 77.

As reflected light impinges on the photo surface of the detector, a light induced current of several hundred nanoamperes flows into the collector. This minute current is amplified, converted to a voltage, and applied to one input of the voltage comparator. Simultaneously, the average of the peak to peak output voltage is applied to the reference input of the comparator. Those voltages in excess of the reference voltage (corresponding to the white areas between the bars) cause the output of the comparator to conduct, resulting in a logic zero at the interface input. Those voltages below the reference (corresponding to black bars) cause the comparator output to turn off, resulting in a logic one at the interface input. The process of using the average of the peak to peak voltage as the reference input to the comparator is known as adaptive thresholding.

As the line of bar coded data is scanned, a string of 1s and 0s is serially applied to the IO interface. At this point the software loader is continually inputting the value of the parallel interface and testing a specific bit for 1s and 0s. To optimize the human engineering aspects of the scanner, an LED is turned on every time a bar is detected. Also available, as an option, is a beeper to signal the operator when a line of bar codes is scanned successfully.

I mentioned earlier that the transmitted and reflected light passes either through the aperture directly or first through a fiber optics cable. These variations represent a number of scanner models I have designed and developed for sale. For further information on the bar code scanner write to Micro-Scan Corp, POB 705, Natick MA 01760.■

Figure 1: White to play. This example illustrates some of the basic problems of strategy and tactics that must be evaluated by any chess playing computer in a typical position. The computer (White) must evaluate a variety of possibilities: two good first moves for White include 1 R-B7 and 1 BxN ch. 1 R-B7 threatens BxB. Therefore Black must either exchange Bishops or gain time by the counterattack 1. . .B-K4. If 1. . .BxB, White must complete the exchange by playing 2 RxB or 2 BxN ch, and so on. The position is analyzed in detail in the game tree shown in figure 2.

A Computer Chess Tutorial

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On February 20 1977, the Minnesota Open chess tournament was won by a computer program, Northwestern University's Chess 4.5. This was a far better result than any program had previously achieved, considering that all the other entrants in the tournament were human beings. An improved version, Chess 4.6, went on to wrest the world computer chess championship from the Soviet program KAISSA (see "The Second World Computer Chess Championships" by Peter Jennings, January 1978 BYTE, page 108). Professional chess players are beginning to worry about the competition from machines. They would seem to have little to fear at the moment, however. The consensus is that Chess 4.5's tactical skill is impressive but its strategy is weak.

Against such competition, what can a personal computer experimenter expect to accomplish? Perhaps a great deal. There have been few new ideas in computer chess since Claude Shannon (see references) outlined the basic principles in a paper published in 1950. (The superiority of Chess 4.6 is due primarily to faster hardware.) Experimenters can participate in the search for the conceptual breakthroughs that will be needed before computer programs can be a match for the best human players. With that thought in mind, this article deals with the questions: What is a good structure for a chess program? What are the major functions that it must perform? In what directions can we seek innovations?

The Game Tree

To get a notion of what a chess program must do, let's look at a position from an actual game (see figure 1). First we must grasp the important features of the position. White has an extra pawn, a passed pawn far from Black's King. Black's mobility is very limited: neither the Knight nor the Rook can move. Black's Bishop is attacking White's Rook and, indirectly, the Bishop behind it. Of less importance, because of Black's lack of mobility, is the fact that two of White's pawns are unguarded. White's task is to save

GLOSSARY

Analysis: the calculation of variations in order to assess a position or find the best move.

Backward pawn: a pawn that lags behind the pawns on the adjoining files. When the opponent has no pawn on the file, a backward pawn is usually a serious weakness.

Development: the process of initially moving the pieces from their original squares.

Diagonal: a diagonal row of squares on the chessboard.

File: a vertical row of squares on the chessboard.

Material: the chess pieces considered as assets. A pawn is traditionally considered to have a material value of one unit. Programs often use smaller units to avoid using fractions for positional advantages.

Minor piece: a Knight or a Bishop.

Passed pawn: a pawn not hindered by enemy pawns on its file or on adjoining files.

Piece: a chess piece other than a pawn.

Positional advantage: any advantage other than an advantage in material.

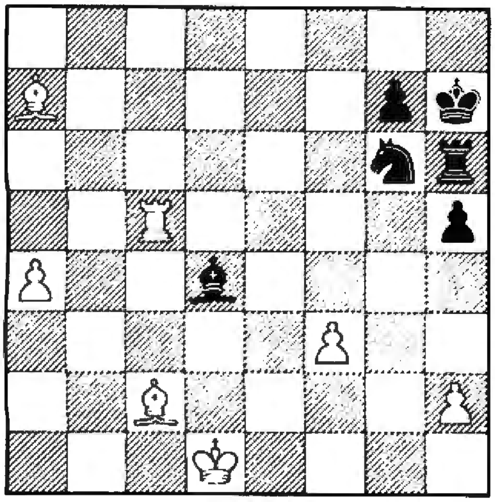
Rank: a horizontal row of squares.

Strategy: that aspect of chess concerned with long-range planning.

Tactics: that aspect of chess concerned with move-by-move changes in the position. Tactics include the methods for winning material and advancing strategic plans.

Variation: a sequence of moves considered as one of several from a given starting position.

BLACK



WHITE

his Rook and to profit from Black's lack of mobility. White should win if he can find satisfactory solutions to these problems.

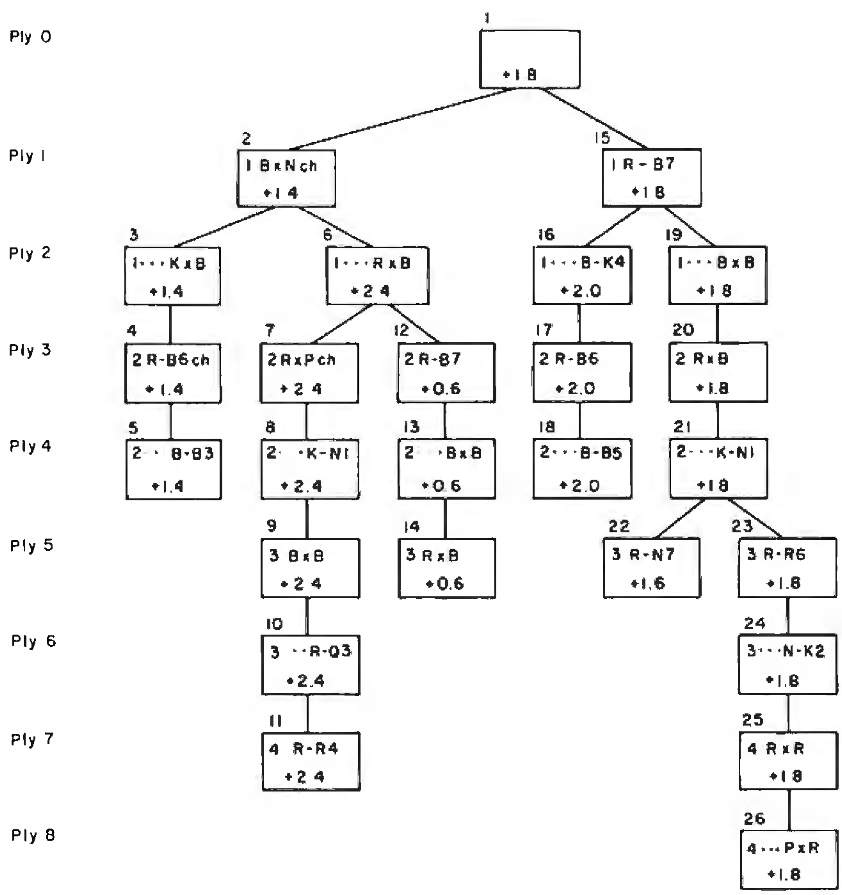
Next we calculate variations — sequences of moves that we would visualize in an actual game before deciding on a move to play. We will follow a systematic procedure that will serve as a first approximation to a computer program. We construct a tree whose nodes represent positions and whose edges represent moves. The variations are the paths from the root to the leaves. Initially, the tree will consist of one node representing the given position. We expand the tree as follows:

> Expansion — Choose a leaf that has not been marked as final. (If one cannot be found, the expansion phase is ended.) Either mark it as final or select a set of legal moves in the position represented by the node. To the leaf attach *sons* representing the positions reached by the moves. Repeat from the beginning.

This procedure might yield the tree shown in figure 2. The size of the tree has been limited somewhat for illustrative purposes. Some of the variations I considered and rejected are not included. Most programs generate much larger trees since it is hard to build into a program the chess knowledge needed for rigorous selection of moves. The length of paths in the tree is expressed in *plies* (*half-moves*). A move consists of a play by one player and a response by the other; a ply is a move by one player alone. Because the term *move* can be confusing (the chess literature speaks of looking three *moves* ahead for example, but are two or three moves by the opponent meant to be included?), in discussions of chess programming one speaks more precisely of a 5 or 6 ply look ahead.

In the expansion procedure, no rule was given for deciding whether to expand a node or for selecting the moves. To gain insight into the way human players make these choices, let us consider the variation that runs down the right side of the tree. In the initial position, Black threatens . . . BxR. White can either make a counterthreat or move his Rook to guard the Bishop. Thus the possible moves include 1 BxN ch, 1 R-B7, and 1 R-R5. I rejected the last alternative because the Rook would have less mobility on R5 and it seemed unimportant to keep it on the fifth rank. 1 R-B7 threatens BxB and moving the Bishop to another diagonal allows B-K3, attacking Black's Rook. Therefore, Black must either exchange bishops or gain time by the counterattack 1 . . . B-K4. If 1 . . . BxB, White must complete the exchange by playing 2 RxB or 2 BxN ch. The latter move was omitted because the reply 2 . . . RxB leads to the position at node 13 (see figure 2), already seen to be unsatisfactory for White. After 2 RxB White threatens R-R6 followed by the exchange of all the pieces and the triumphant advance of the Queen's Rook pawn (QRP). Black must play 2 . . . K-N1 or 2 . . . K-R1. The square closer to the center was chosen on general principles.

Figure 2: A game tree developed from the position in figure 1. Each node represents a position; the root, the initial position. The move leading to the position is written in the top of the box, the evaluation of the position in the bottom. The number above the box identifies the node. A node's ply number is its distance from the root.



Free of threats at last, White can move in pursuit of his goals. White could play 3 R-N7, preparing to position his Rook behind the passed pawn; 3 K-Q2, bringing his King toward the center; 3 P-R5, advancing the passed pawn; or 3 R-R6, to force the exchange of Rooks. Somewhat arbitrarily, I included in the tree only the two moves that seemed best. 3 R-R6 forces the Knight to move. Obviously it should approach the passed pawn, but it is not immediately clear which square is best. After 3 ... N-K2 4 RxR PxR the assessment is clear: having two passed pawns in a minor-piece ending, White should win easily. There is no need to consider other Knight moves, because the effect on the evaluation of the position would be too small to affect White's choice of move in the initial position.

From this brief discussion we can see some of the factors that determine the selection of moves. When there is a definite threat, it is necessary either to answer the threat directly or to make a counter-threat. Otherwise you must decide which goals are most important and choose the moves that best advance these goals. When two moves have similar effects, not much is learned by including both in the tree, particularly at a deep level.

We can also see some of the reasons for terminating a node (that is, choosing not to expand it). In this example, a node is terminated when the position can be evaluated sufficiently well or when the previous move was not forcing and the side to move has no forcing move that accomplishes anything. At node 14, for example, it is already clear that White doesn't have a won position, and it follows that one of his moves must have been a mistake. Thus we can evaluate the position sufficiently well (but not accurately: further analysis would lower the estimated evaluation given in the figure). At node 5 White has the forcing move 3 B-K3, but after 3 ... R-R1 his position hasn't improved. We consider these moves but don't add them to the tree, because the resulting position is merely compared with the position at node 5, not evaluated.

Once the tree is complete, the next step is to evaluate the terminal positions:

> Evaluation — Label each leaf with the value of the position from the point of view of the player whose turn it is to move in the *initial* position. Positive values mean the player has the advantage; negative values mean the player's opponent does. A value of ±1 means an advantage

barely enough to win; a value of ±2 means an easy win (see figure 2).

In the present example, material, mobility and pawn structure were the most important factors in making the evaluation. In a middle game position, King safety would also be taken into consideration.

The final step is a completely mechanical procedure called the *minimax* algorithm, which is guaranteed to choose the best move provided the evaluations are accurate and that the best move at each node is included in the tree.

> Backup — Select an unevaluated node, all of whose sons have been evaluated. If the node is at even ply, label it with the maximum of the sons' values; at odd ply, choose the minimum. Repeat from the beginning until all of the nodes have been evaluated. Then choose the move leading to the ply-1 node with the greatest value.

This method of assigning evaluations to nonterminal nodes is based on the assumption that each player always makes the best move. The minimax algorithm will *not* always choose the move that affords the best winning chances against a weak opponent.

Our 3 part procedure for generating a game tree is somewhat unnatural. For one thing, a person analyzing a position would return to the expansion phase if the moves originally selected didn't work out as well as expected. Also, the evaluation phase reflects the human assessment process poorly. No provision is made for recording degree of confidence in the evaluation. Human players make relatively coarse absolute evaluations: they judge which of two similar positions is better, but do not attempt to assign slightly different values to them.

In chess programs, expansion, evaluation and backup are carried out simultaneously. One reason is that time can be saved by using backed-up values to demonstrate that some nodes need not be expanded at all. For example, the variation 1 BxN ch RxB 2 RxP ch gives White a great advantage; we say that 2 RxP ch refutes 1 . . . RxB. Once one refutation is found, it is pointless to look for another: 2 R-B7 need not be considered if not considered already. What does this mean in terms of the minimax algorithm? Once node 3 has been assigned the value +1.4, we know that the value of the minimizing node 2 will not be any greater. Similarly, once node 7 has the value +2.4, we know that the value of the maximizing node 6 will not be any less. Therefore the minimax algorithm will not choose the value of node 6, and it

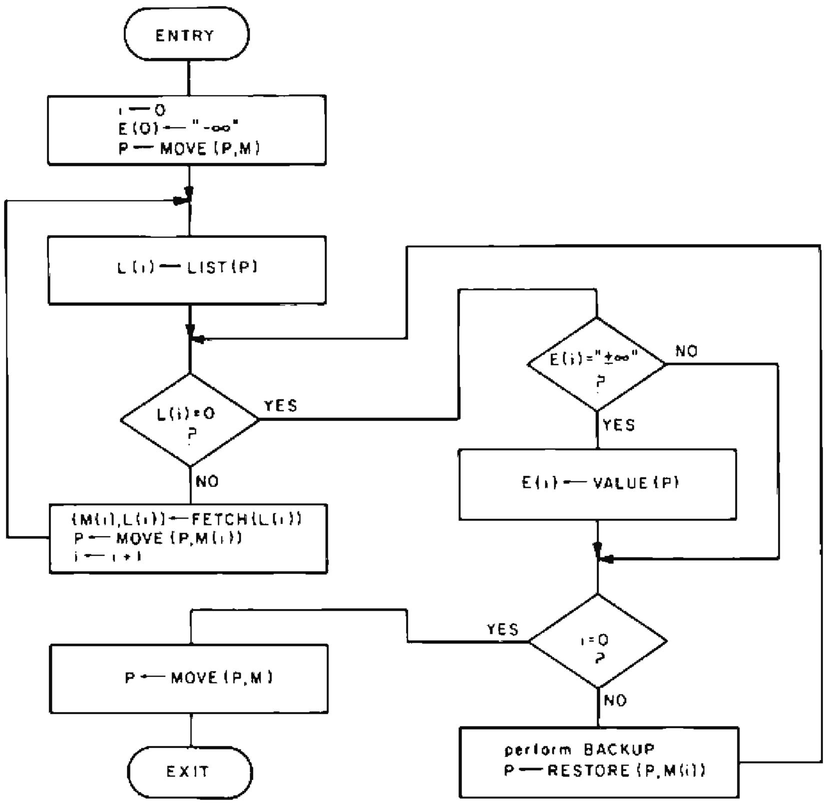


Figure 3: A routine to choose a move. A ply table *(so called because it is indexed by the ply number, i) is used to choose moves. (A ply is a move on the part of one player; two plies equal one chess move.) The entries in the ply table correspond to nodes in the game tree (see figure 2). Each entry contains three fields: L(i), a pointer to the list of moves selected at each node; M(i), the move currently being processed; and E(i), the evaluation. Most of the subroutines are written as functions in order to show which data areas they use and affect. Only those data areas that play a central role are indicated. ∞ refers to a number which is larger than any returned by subroutine VALUE. Its additive inverse, —∞, is used as the initial value of E(0).*

can be eliminated from the tree without expanding node 12. Although in this example only one branch can be eliminated in this way, it is an important method for limiting the size of the "bushier" trees generated by chess programs.

We have seen that there are three major aspects of chess reasoning that need to be analyzed to create a chess program: selection, termination and evaluation. The handling of these functions by existing programs is only a crude approximation to the human reasoning process. It has proven particularly difficult to limit the number of moves considered at each node without inadvertently eliminating the best move. Consequently, Chess 4.6 uses no selection or termination at a depth of less than six plies, and generates trees with hundreds of thousands of nodes. Even those programs that exercise some selection generate, in most cases, trees too large to store in programmable memory. Fortunately our procedure can be reformulated so as to require only a small part of the tree to be retained in memory at any time.

The Depth-First Minimax Procedure

A tree can be traversed systematically by the following procedure:

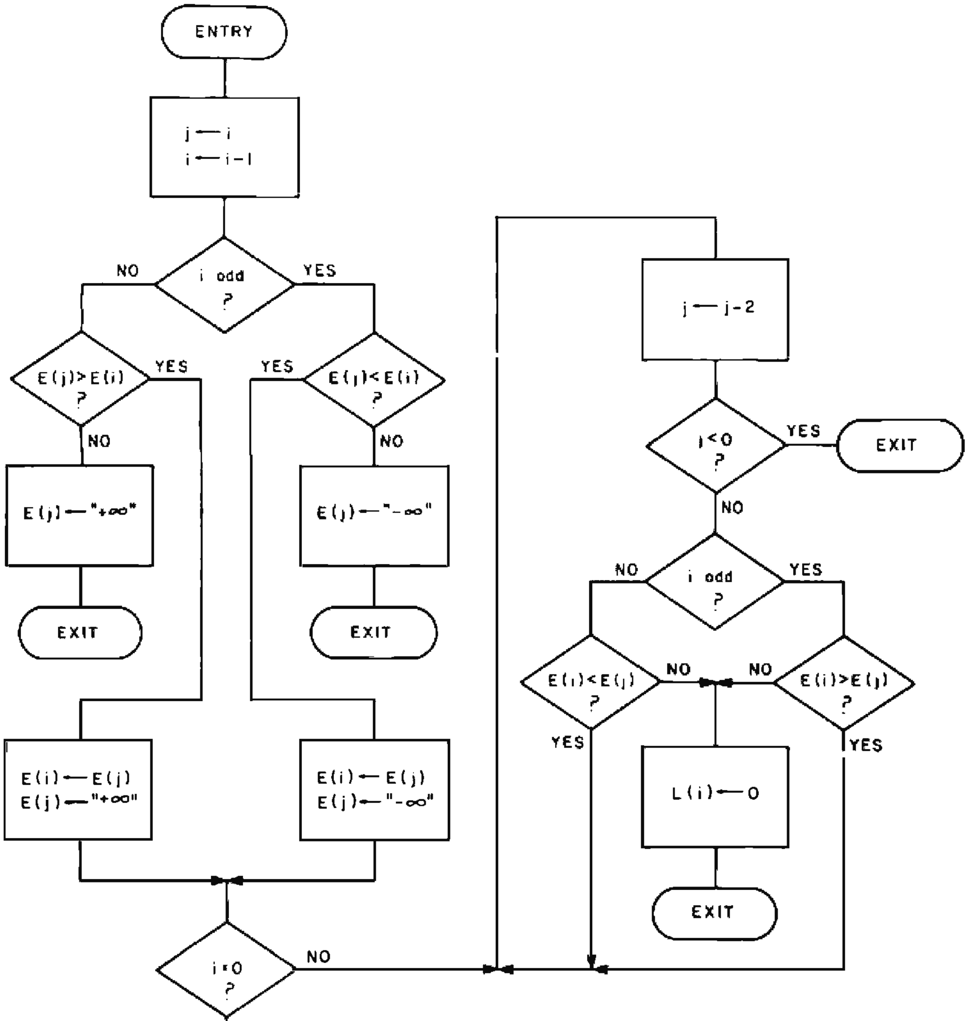
> Start at the root — At each step, move to the leftmost unmarked son and mark it. If there is no unmarked son, move to the father. If there is no father, stop. (The terms *son, father* and *brother* are analogous to those in a family tree.)

The depth-first minimax procedure traverses the game tree in this way, simultaneously doing the expansion, evaluation and backup. Storage is required only for one path from root to leaf and for the brothers of the nodes on the path.

Figure 3 shows one way to organize the procedure. The processing is centered on the *ply table,* so named because it is indexed by the ply number i. The entries in the ply table correspond to nodes in the game tree. Each entry contains three fields: L(i), a pointer to the list of moves selected at the node; M(i), the move currently being processed; and E(i), the evaluation. The data area P contains the board position. As the tree is traversed, P is modified to show the position at the current node. At the start of the routine, the position is as it was presented to the opponent. The routine applies the move in location M to the position, chooses its move, stores it in M, and applies it to the position.

The subroutines named in figure 3 are discussed briefly here and in greater detail in the following sections. MOVE applies a move to the board representation P. It may also update auxiliary information describing the position. RESTORE simply reverses the changes made by MOVE. LIST generates the list of selected moves and places a pointer to the list in L(i). If the list is empty, L(i) is set equal to zero. FETCH moves the first move on the list to M(i) and advances the pointer L(i) to the next move. VALUE places the evaluation of a terminal position in E(i). BACKUP moves the evaluations E(i) up the table in accordance with the minimax rules.

Programs that generate a large tree generally use a depth-first search and have an overall structure similar to that shown in figure 3. The inflexibility of the depth-first search is a significant disadvantage, though. For example, suppose that shallow analysis of the first ply-1 move casts doubt on its



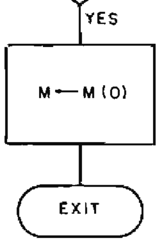


Figure 4: The BACKUP routine. The lefthand side of the flowchart depicts the minimax algorithm, a method which is guaranteed to choose the best move provided that the evaluations of the nodes in the game tree are accurate and that the best move at each node is included in the tree. The right side of the flowchart illustrates the alpha-beta algorithm, used to "prune" refuted nodes - that is, nodes which are known to represent inferior positions. Trimming the tree in this way reduces the amount of information that must be stored in memory and speeds up the evaluation process (see text).

value. Time might be saved by proceeding at once to the other moves and returning to the first move only if they seem no better. But in a depth-first search, the decision to terminate a variation cannot be changed on the basis of later information. Consequently, programs that generate small trees usually maintain the entire tree in programmable memory. Then it is possible to skip around in the tree, expanding those nodes that look most promising. Although such programs aren't structured like depth-first programs, they perform many of the same functions, and so the following discussion of the subroutines partially applies to them.

The BACKUP Routine

The movement of values up the tree is controlled by BACKUP, which also prunes refuted nodes. The procedure is shown in detail in figure 4. The minimax part of the procedure manipulates the fields E(i), which can contain initial values, provisional values, and final values. The initial values are $-\infty$ for even ply and $+\infty$ for odd ply, where ∞ is a number larger than any returned by VALUE. E(i) is always set to the initial value when the table entry is not being used. The values produced by VALUE are final values. Whenever a final value E(i) appears in the ply table, BACKUP compares it with the value E(i–1). E(i) replaces E(i–1) if i is even and E(i–1) is greater than E(i) or if i is odd and E(i–1) is less than E(i). E(i–1) then contains a provisional value. A provisional value becomes final when the move list at its ply becomes empty. Whenever E(1) replaces E(0), M(0) is saved in M. As a result, M ultimately contains the first move in the list L(0) that produces a maximum final value in E(1).

The Alpha-Beta Algorithm

The elimination of refuted moves from the tree is accomplished by a procedure called the *alpha-beta* algorithm. *[The alpha-beta algorithm is discussed in Slagle and*

Dixon's paper (see reference 6). . . .CM] To get a clear understanding of the alpha-beta algorithm, let's view the minimax procedure as a contest to determine which leaf's evaluation will reach the root. The provisional evaluations in the ply table are obstacles to the progress of an evaluation up the tree. Maximizing nodes stop evaluations that are too small; minimizing nodes stop those that are too large. Suppose that i is odd and that a new evaluation has just been backed up into E(i). Because E(i) is now smaller, it may not be able to get past the provisional values in maximizing nodes higher in the tree. To find out, the alpha-beta algorithm searches at even ply for an evaluation greater than or equal to E(i). If one is found, the level-i node is terminated by setting L(i) to zero. The procedure is similar when i is even. The termination of a node by the alpha-beta algorithm is called an *alpha-beta cutoff* or just a *cutoff*.

The LIST Routine

The decisions that determine the size and shape of the game tree are made by LIST. It has three main functions: termination of nodes, selection of moves and the sorting of the list of moves. If the program is to play under a time limit, LIST must also monitor the elapsed time and modify its decisions accordingly. Existing programs handle these functions in widely differing ways. Their selection and termination procedures range from trivial to complex. It's discouraging that the trivial methods have so far yielded the best results, for surely a sophisticated LIST routine will be needed for first-rate chess.

Most chess programs condition termination primarily on depth and the availability of certain types of forcing moves. The simplest method would be to terminate always at some fixed depth. Then VALUE would have to give special handling to positions with an exchange in progress, lest material be reckoned incorrectly. Consequently, many programs use two depth limits. Beyond the first limit are selected only certain forcing moves, typically checks and captures. Termination occurs, of course, when there are none. At the second depth limit termination always occurs.

Other criteria for termination have been tried. The Ostrich program (developed on a Data General Supernova minicomputer at McGill University in Montreal, Canada) terminates variations in which material is sacrificed and not recovered within three plies. Several people have suggested that termination should occur only if the position can be accurately evaluated. The

Newell-Shaw-Simon program used this philosophy. When the entire tree is maintained in programmable memory, termination decisions as such need not be made at all. For example, the program COKO expands those nodes that promise the greatest yield of information, no leaf being permanently excluded from consideration.

For selection and sorting, LIST might assign to each legal move a plausibility rating designed to indicate the probability that the move will prove best. Many programs don't explicitly assign a rating; nevertheless, it is convenient to imagine that their decisions are based on an implicit rating. Selection and sorting can then be done as follows: select all moves with ratings greater than some threshold. If too few moves are selected, add highest-rated moves to make up the minimum number. (The threshold and number of moves might depend on depth.) Sort the selected moves by rating.

For sorting, the requirements on the rating procedure are not stringent. It suffices that moves good enough to cause cutoffs often appear early in the list. Occasional inaccurate ratings will merely increase the processing time, not cause a blunder. The number of cutoffs can be markedly increased by simply assigning high ratings to a few easily defined categories of moves: captures, checks, moves by attacked pieces, etc. Another simple rating method is to assign a high rating to moves that have proven to be good in other parts of the tree. For example, the "killer" heuristic assigns to a refutation found at one node a high rating at its brother nodes. This heuristic works well in positions containing threats, because all moves that ignore the threat can be refuted by the same reply.

For selection, the plausibility rating must be more accurate. A best move markedly better than the second best move must only rarely receive a rating low enough to cause its rejection. Simple criteria that are adequate for sorting are bound to fail. The rating must be based on all of the move's important effects, which can in turn be determined only by elaborately tracing the relationships of the pieces. For this reason, programs that use selection generally maintain a tactical description of the position. In the program we are considering, it is the responsibility of the MOVE routine to keep such information current.

The VALUE Routine

The evaluation is usually computed as a sum of numerical scores, each representing one aspect of the position. Chess programmers tend to include only those aspects that are easiest to program. Unfortunately they are not always the most important ones. The traditional chess literature is more explicit about evaluation than about selection and termination. The books in the bibliography are particularly helpful.

The evaluation of a position depends mainly on material, mobility and vulnerability. The calculation of material is straightforward, although experts disagree about the exact values of the men. Chess 4.6 uses the values: P=100, N=325, B=350, R=500 and Q=900. Like most programs, it adjusts the material score to encourage the exchange of pieces when ahead in material. The values of the pieces vary with the strategic character of the position: Rooks are better when the opponent has weak pawns, Knights are better in blocked positions, and so on. Such considerations are important, but I know of no program that takes them into account.

The assessment of mobility is more difficult. Counting the legal moves of each man is easy but inadequate. It is necessary also to take into account the exclusion of men from squares controlled by the opponent and the immobilization of men by defensive functions, such as the shielding or guarding of a man or important square. Detecting these factors is complicated and may involve tracing the relationships between several men.

Under vulnerability we have to consider unguarded pieces, the safety of the King, weaknesses in the pawn structure and pieces exposed to attack by less valuable men. Pawn weaknesses are easy to detect, and most programs take them into account. Measuring danger to the King is more complicated, but it is easy to detect some of the relevant features, such as disturbances of the King's pawn cover or the absence of friendly minor pieces nearby. Detecting unguarded and exposed pieces seems to be relatively simple, but oddly it is often neglected.

The MOVE Routine

Because of the rapid expansion of the game tree with depth, most of the processing time is spent in selecting and evaluating the terminal positions. It is therefore desirable for MOVE to maintain, along with the current position, information helpful to the LIST and VALUE routines. For example, it is more efficient for MOVE to keep track of changes in the material score than for VALUE to scan the board to do the same thing. Also, some programs maintain lists of the locations of each side's men to facilitate the generation of moves.

We have seen that sophisticated LIST

and VALUE routines would have to detect relationships between the men. Since each move changes only some of the relationships, it is more efficient to compute them in MOVE than to compute them all from scratch in LIST and VALUE. In general, the features needed for selection are the same as those needed for evaluation. For example, a backward pawn affects the evaluation and also suggests moves for both sides. The possessor of the pawn will try to advance it or protect it, while his opponent will try to prevent its advance and win it. Likewise any advantage suggests moves to maintain and exploit it; any disadvantage, moves to eliminate or mitigate it.

Levels of Skill

The United States Chess Federation rates its members at eight levels of skill based on performance in tournaments. In descending order they are Senior Master, Master, Expert and Classes A through E. From time to time computer programs have played in rated tournaments. Until recently their performance has been in the Class C or Class D range. Against this background the strong showing of Chess 4.5 startled everyone. At the conclusion of the Minnesota Open its rating had risen to Expert. It is still too early to assess its true strength, however. Although it is strong tactically, its grasp of strategy is well below the Expert level. The weak showing of Class A players against Chess 4.5 was caused largely by their unfortunate tendency to get into tactically complex positions, thereby playing into the computer's strength. The program may not be so successful once people learn how to play against it.

The sudden improvement in Chess 4.5 coincided with its transfer to a faster machine, enabling it to search two plies deeper in most positions. This supports the belief that chess skill depends mainly on the number of moves one can see ahead. It's difficult to give a precise equivalence between depth of search and level of skill, though. The following rule of thumb is, I think, close enough to the truth to give some idea of the design requirements for strong programs. Let a search depth of four plies correspond to Class C, and assume that each additional two plies yields an increase of one level of skill. Thus, play at the Expert level would require a 10 ply search.

The Exponential Explosion

The depth of search is limited by the increase in the size of the game tree with depth. Suppose that B moves are selected

Search Depth	Number of Terminal Nodes
2	59
3	929
4	1,800
5	27,900
6	54,000
7	837,000

Table 1: Tree size as a function of search depth (D), assuming exhaustive search and the maximum possible number of alpha-beta cutoffs. The branching factor (B) is assumed to be 30. The number of terminal nodes is $2B^{D/2}-1$ when D is even and $B^{(D+1)/2}+B^{(D-1)/2}-1$ when D is odd.

at each node. This number is called the *branching factor* or *fanout*. If D represents the depth of search, the tree has B^D leaves; the tree grows exponentially with depth. A typical position might have 30 legal moves, and if no selection is exercised, the tree will have 27,000 leaves at a depth of three plies. This is probably already too large a tree to examine with a microcomputer in a reasonable time. We have not, however, yet taken alpha-beta pruning into consideration.

The effectiveness of the alpha-beta algorithm depends on how well the move list is sorted. The greatest possible reduction in tree size is achieved when the best move is always first on the list. Table 1 shows the tree size under this condition, assuming a branching factor of 30. Clearly, exhaustive search beyond six plies is impossible for a small computer. To play strong chess a microcomputer will have to use selection. The question is: how much?

Branching Factor	Depth of Search	Tactical Skill
31.6	4	Class C
15.8	5	
10.0	6	Class B
7.2	7	
5.6	8	Class A
4.6	9	
4.0	10	Expert
3.5	11	
3.2	12	Master
2.9	13	
2.7	14	
2.5	15	

Table 2: Depth of search (D) and tactical skill as a function of the branching factor (B). It is assumed that the alpha-beta algorithm reduces the effective branching factor to $B^{2/3}$ and that 10,000 terminal nodes can be processed. These assumptions yield the formula $B=10^{6/D}$.

To derive a relationship between the branching factor and the depth of search, we have to make some assumptions. Let us assume that we must limit the size of the tree to 10,000 leaves, and that the alpha-beta algorithm reduces the effective branching factor from B to $B^{2/3}$. Then table 2 gives the desired relationship. Although much guesswork went into this table, it seems safe to conclude that an Expert-level program must be very fast or very selective.

The TECH Program

How simple can a program be and still play reasonable chess? The TECH program was developed in order to answer that question. It would be a good model to follow if you want to have a running program in the shortest possible time. Despite its simplicity, or perhaps because of it, TECH placed higher in computer chess tournaments than some of the more complicated programs. It is good enough to defeat only inexperienced human players, but that is true of most programs. For the newcomer to chess programming, the design of a TECH type program would be a good way to gain experience.

TECH considers all moves to a fixed depth, beyond which it considers only captures. The evaluation of terminal positions is based only on material. Hence there is no need for a VALUE routine; the evaluation is computed on the run whenever captures occur. When the program has an advantage of two pawns or more, it reduces the value of its own pieces slightly so that exchanges are favored. TECH sorts moves for two purposes: to increase the frequency of alpha-beta cutoffs, and to bring factors other than material to bear on the choice of a move. At ply 2 and lower, captures are considered first and the killer heuristic is used. The positions at ply 1 are assigned a rating that includes such factors as the number of legal moves, the advancement of the center pawns, and the proximity of the pieces to the center, to the enemy King, and to passed pawns. The program expands the ply-1 nodes in descending order of the rating, which thus breaks ties in the backed-up evaluation.

Because TECH does very little processing at each node, it is able to generate a relatively large tree. Cutoffs are frequent; basing the evaluation only on material ensures that the alpha-beta comparison will often give an equal result. The ply 1 rating procedure could be made more elaborate without slowing down the program noticeably. It would be interesting to see how much the program's play could be improved in this way.

New Directions

Chess programming is still a young field. There are many ideas that have never been tried or never been developed sufficiently to determine their value. Experimentation by computer enthusiasts could play a major role in developing the innovations that will be needed for a Master-level chess program. Some of the less successful chess programs use ideas worth further consideration. Papers describing some of these programs are listed in the bibliography. Additional ideas can be found by comparing the behavior of programs and human players.

Some Ideas for the Future

Chess games between computers are often dull because the programs don't follow any plan. They pursue general goals such as development and control of the center, but don't formulate goals specifically appropriate for the position at hand. Goals are represented in the evaluation and rating procedures. Setting a specific goal is accomplished by making changes in these procedures. For example, the general goal of center control might be implemented in part by a term in the evaluation polynomial for the number of pieces bearing on the center. A routine for setting specific goals might add a term for the number of pieces bearing on a center square that the routine had determined to be particularly important.

Here are some of the types of specific goals that occur frequently:

- Get control of a key square.
- Attack an area of the board where the opponent is weak.
- Free an immobile piece.
- Save an attacked man.
- Maneuver a particular piece to a square where it will have a strong influence.

It should be fairly easy to determine how to modify the evaluation and rating procedures in such a way as to set these goals. However, it might be difficult to devise a procedure for choosing the specific goals.

Most chess programs spend almost all of their time considering silly moves. There are two main types of silly moves: moves irrelevant to the important goals of the position, and sacrifices that gain nothing that could be worth the cost. To safely reject irrelevant moves, the program must avoid overlooking important goals, lest it reject a vital move and blunder. Because of the difficulty of writing a comprehensive goal setting routine, it is not surprising that highly selective programs haven't performed well. Nevertheless, it is only a matter of time until enough chess knowledge is formalized to permit accurate selection. In the meantime, it might be possible to devise an algorithm that would reliably identify at least some of the silly moves.

Chess programs usually compare moves or positions by assigning numbers to them and then comparing the numbers. This method precludes certain possibilities of reliably rejecting moves. Suppose we have an algorithm that, given two similar positions, lists all of the important differences between them, together with limits on the effect each difference could have on the evaluation. It is then sometimes possible to determine which position is better, even though it might not be possible to evaluate either position reliably. We saw an example of this in the analysis of figure 1, where 2 . . . K—N1 appeared to be clearly better than 2 . . . K—R1. The position-comparing algorithm could be used for selection and for a variant of a alpha-beta pruning. We meet with a familiar difficulty, however: the algorithm would have to incorporate comprehensive knowledge in order to avoid overlooking important differences.

To summarize, a program to play Master-level chess might contain algorithms to

- Find the important features of the position.
- Determine the relevant goals and rate their importance.
- Compare two similar positions to determine whether one is clearly better than the other.
- Select a list of reasonable moves in a given position.

Each algorithm would use the results of the previous ones in the list. The program would contain much chess knowledge, which would best be represented in a form both compact and easily alterable.

Prerequisites

How good a chess player do you have to be to tackle some of these problems? Most people need only a basic understanding of chess strategy and the ability to find simple combinations. Far more important than chess knowledge is the ability to teach what you know to a very dull, nonhuman pupil.

Circle 40 on inquiry card.

You will have to be able to state explicitly the reasons for the choices you make while analyzing a chess position. It's not as easy as it sounds. Above all, it's important to keep in mind that writing a chess program is a big project. A methodical approach, using structured programming and careful documentation, is absolutely essential.

Concluding Remarks

In this article I have tried to cover the basic ideas of chess programming and indicate some new directions for experimentation. I hope that many of you will be stimulated to get involved in this growing field of research. ■

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Creating a Chess Player

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An Essay on Human and Computer Chess Skill

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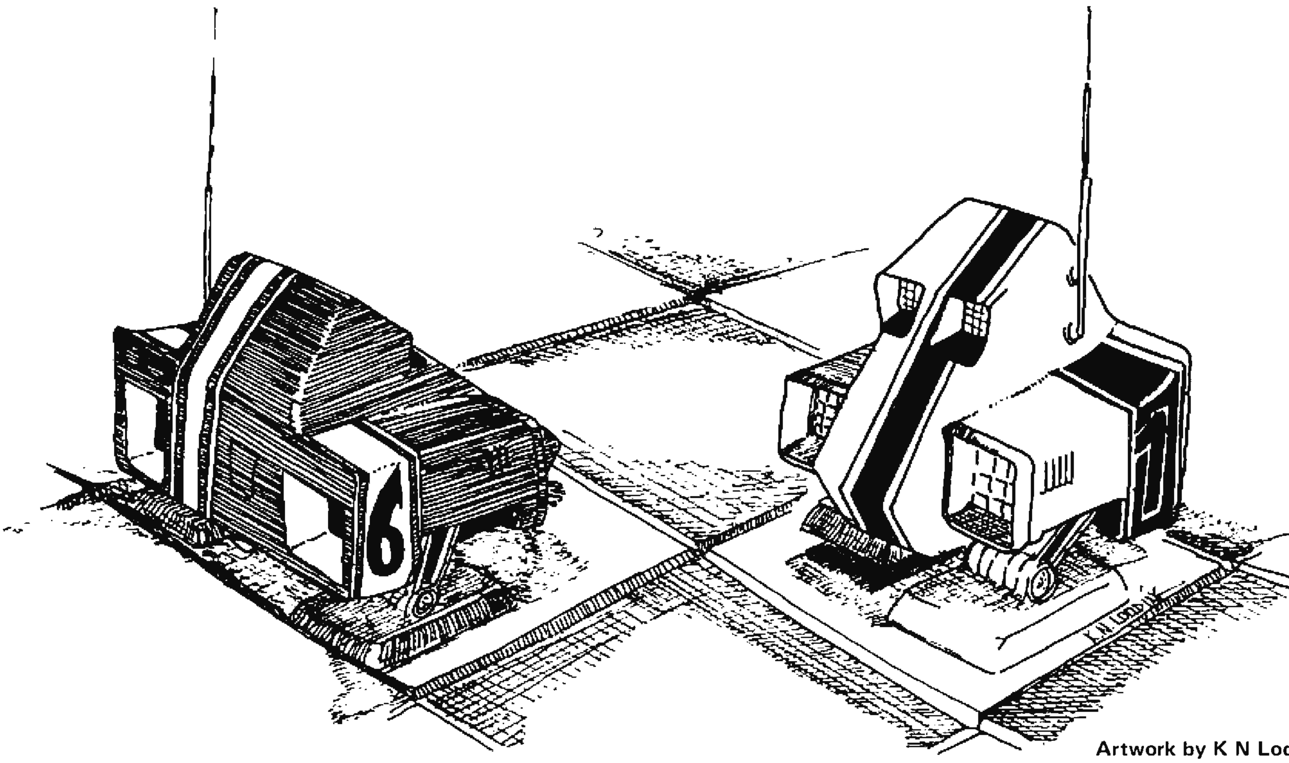
In a recent *Time* essay (see references) Robert Jastrow, director of NASA's Goddard Institute for Space Studies, predicted that history is about to witness the birth of a new intelligence, a form superior to humanity's. The pitiful human brain has "a wiring defect" that causes it to "freeze up" when faced with "several streams of information simultaneously." Jastrow suggests that "the human form is not likely to be the standard form for intelligent life" in the cosmos. Even on our own small planet, a new day is near at hand: "In the 1990s, . . . the compactness and reasoning power of an intelligence built out of silicon will begin to match that of the human brain."

We have always been fascinated by the idea of a machine that is capable of rational thought. Jastrow is neither the first nor the last person who is betting on rapid improvements in machine intelligence. His expectation that computers will rival humanity within 15 years seems optimistic to anyone who has watched half-a-dozen excited technicians flutter about for several hours trying to bring a crashed system back to life. This prophecy seems even more fanciful to those who have attempted to program machines to cope with pattern recognition, language translation or a complex game such as chess.

The chess environment, in fact, provides a particularly good example of the difficult problems which still need to be solved before silicon intelligence can become a reality. More than 20 years ago, Herbert Simon, a recognized expert in the field of artificial intelligence, predicted that within a decade, the world's chess champion would be a computer. This prognostication has not come to pass. Why was an informed scientist like Simon so wrong in his assessment of computer capabilities? A major factor is that computer scientists have often failed to appreciate the level of knowledge which is required to play master-level chess. They have also commonly underestimated the tremendous information-processing capacity of the human brain. Even though chess is a game of logic in which all legal moves can be precisely specified and in which nothing is left to chance, several centuries of intensive analysis have not exhausted the perennial challenge and novelty of the game. Psychologists have been actively studying the human brain for several decades and have discovered a fascinating mystery wrapped within an enigma. The more we learn about the brain, the more we are aware of our lamentable state of ignorance.

The Mind of the Chess Player

At a general level of knowledge, we have several provocative insights on the nature and structure of human chess skill. We know, for example, that the skilled chess player does not examine hundreds of possible continuations before selecting a move. We also know that superior chess players are not formidable "thinking machines" but in fact display a normal range of intelligence scores. Strong chess players, as a group, do not even appear to have special retention abilities such as having "photographic" memories. In most respects, top-flight chess players have the same intellectual capacities as the rest of the population and, in the technical details of move selection, seem to engage in the same type of information processing that is observed in much weaker players.



Artwork by K N Lodding.

Our knowledge in these matters is based on the early work of Binet in France and that of de Groot in Holland and on more recent investigations by other scientists in the USSR and the United States. In the late nineteenth century, Binet was surprised to discover that masters did not have a vivid image of the board when playing blindfolded chess. Instead, they seemed to remember positions in abstract terms such as by specific relations among pieces. Interviews with masters clearly indicated that a photographic memory was not a prerequisite for being able to play many simultaneous games of blindfolded chess. In the 1930s and 1940s, de Groot worked with a number of strong chess players (from Grandmasters to strong club players) and had them verbalize their thought processes while selecting a move in a complicated position. His research indicated that the Grandmasters' general approach was highly similar to that of weaker players. They analyzed a similar number of moves (about four) from the initial position, a similar number of total moves (about 35), made a similar number of fresh starts (about six), and calculated combinations to the same maximal depth (about seven plies or half-moves, where a move is defined as a play by one side and a response by the other). The only clear measurable difference was that the Grandmasters invariably chose the strongest move while the weaker players did not. Thus de Groot concluded that Grandmasters play better chess because they pick better moves. Unfortunately, this conclusion is not very informative since it is obviously circular. The fact that de Groot's extensive study did not uncover any prominent differences in the move-selection strategies used by strong and average players implies that the analysis procedure itself is not the critical factor which determines chess skill.

An important clue to the difference between skilled and unskilled players was discovered by de Groot when he displayed an unfamiliar chess position to his subjects for a few seconds and then asked them to recall the position from memory. He found that masters recalled almost all the pieces while club players remembered only about half of them. Recent work in this country by Chase and Simon at Carnegie-Mellon University has indicated that novice players recall only about a third of the pieces. Chase and Simon also added an important control procedure. They demonstrated that the differences in recall ability completely disappear if the pieces are positioned randomly. This outcome indicates that the superior memory of the chess master is chess-specific and not a general trait.

De Groot's "law" of chess is that Grandmasters play better chess simply because they pick better moves.

Simon and Gilmartin have proposed that skilled chess players learn to recognize a large number of piece combinations as perceptual chunks and perform well in the recall task because they remember four or five chunks rather than four or five pieces like the novice. If the average chunk size is three to four, the skilled player will recall 16 to 18 pieces.

On the basis of this analysis, skill in chess depends on a learned perceptual ability which is highly similar to that acquired by every schoolchild as he or she slowly builds up a large repertoire of words. Initially the child learns to read each word character by character and often does not understand the meaning of the word. The novice chess player perceives the chessboard in a similar way, assessing a position piece by piece and failing to recognize the *meaning* of common piece configurations. The adult reader recognizes words and phrases as basic units (chunks) rather than individual characters and has a recognition vocabulary of approximately 50,000 words. The skilled chess player, in a similiar vein, recognizes a very large number of piece configurations (chunks) and understands what they imply both individually and in combination.

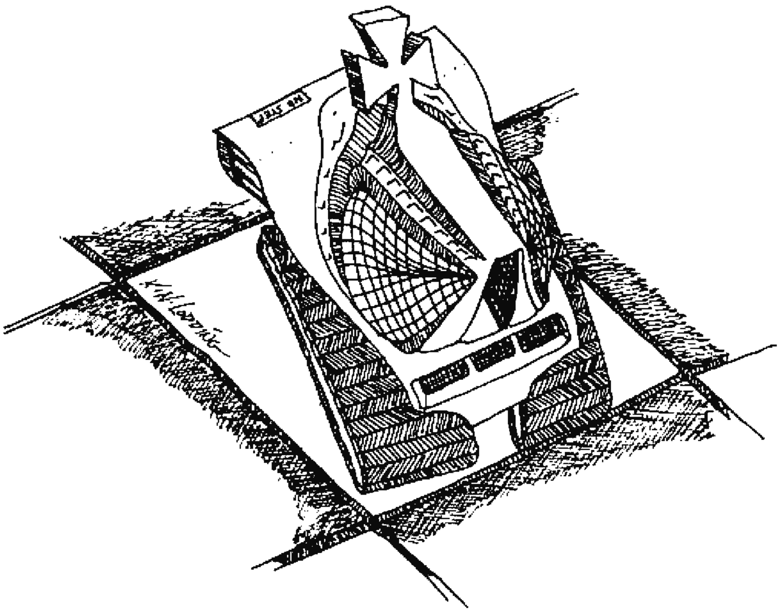
The critical aspect of move selection occurs in the first few seconds of the task. Based on his assessment of the position, the skilled player immediately recognizes appropriate long-term and short-term goals and has a good feel for the specific moves which are compatible with these goals. For this reason, only two to four moves on the average are given serious consideration. The difference between the Grandmaster and the expert lies in the fine distinctions which are made in the first few seconds of their analysis. Skilled chess players can play a remarkably strong game when they are given only five seconds for each move. In this short time, it is not possible to make a careful analysis of many different continuations. The player must have an "instinctive" feel for the correct move and be able to recognize key features and to understand both their immediate and long-term implications.

Human chess skill, therefore, is based on two highly refined capacities, pattern recognition and rapid information retrieval. The latter ability depends on the fact that human memory is content-addressable rather than location-addressable like that of a computer. Computer systems often have to search for a specific item of information in memory by conducting an exhaustive, linear search of an entire file. Human memory however is organized in an amazingly complex fashion such that most of us can easily recall a specific fact on the basis of a completely novel retrieval cue. For example, name a flower that rhymes with *nose*. In this case, your quick response demonstrates that words are grouped together on the basis of their phonetic similarity (ie: sound). Your ability to quickly recall words which are similar in meaning to the word *fat* (such as obese, chubby, rotund, flabby, plump and stout) demonstrates that human memory is also organized by semantic similarity (ie: meaning). When a person is given a retrieval cue which does not elicit an immediate response, he or she can usually find the correct information after a brief search of related ideas or concepts. This facility contrasts sharply with the extremely limited linear searches which are generally conducted with large computer based storage systems. Even sophisticated computer retrieval strategies which arrange the data base in multilinked lists with elaborate tree structures presently lack the large system efficiency displayed by their biological counterparts.

Pattern recognition and rapid information retrieval are not only key capacities for chess, but are also essential for a wide range of important human problem solving skills. Whether your field is medicine, engineering, plumbing or computer programming, you would be a complete failure at your job without these essential abilities. Jastrow's claim that machine intelligence will soon equal man's intelligence seems to overlook the important points made in BYTE by Ernest Kent (see references). Kent emphasizes the fact that biological information processors have a vastly different architecture than their silicon imitations. In fact, he suggests that our lack of success in building a thinking machine stems from our attempts "to make a wrench do a screwdriver's job." Our modern high-speed computers were designed to do important tasks which men are not very good at, such as complex mathematical calculations.

The human brain evolved, in contrast, on its ability to identify important environmental events and to quickly recognize their significance. Natural selection has never placed much emphasis on our ability to multiply or our ability to compute the inverse of a matrix. Kent also reminds us that organic evolution worked with a very different kind of hardware than that which is available to the modern computer engineer. Biological information processors have an incredibly slow cycle time, less than 100 operations per second. The basic unit, the neuron, operates in milliseconds rather than in nanoseconds. The brain, however, makes up in quantity and in structural complexity what it lacks in speed. Computers, on the other hand, have many fewer components and a much simpler gating architecture, but are orders of magnitude faster.

It may be that present machine hardware configurations are simply inappropriate for efficient pattern recognition or semantic recall. An analysis of the history of computer chess is instructive. Although there have been numerous advocates for chess programs which imitate human playing methods, only a few have been attempted, and none of these have played reasonable chess. The eariliest paper on machine chess, written by Claude Shannon in 1950 (see references), proposed a mechanical algorithm which was not modeled on human chess play. Shannon suggested a workable procedure for representing the board and piece locations, specified simple mathematical algorithms for generating the legal moves of each piece and gave an example of a straightforward technique for evaluating a position (see *Chess Skill in Man and Machine*, chapter 3). The key feature of Shannon's proposal was the adoption of the *minimax* technique as described by von Neuman and Morgenstern in 1944. The basic idea of the minimax technique is to assume that the player whose turn it is to play will always choose the move which minimizes his opponent's maximum potential gain. Hence, the name minimax.



The Type B Strategy

One of the difficulties of this approach is that a complete analysis of all possible continuations (type A strategy) very rapidly leads to an overwhelming number of potential positions. The look-ahead tree grows at an exponential rate and with an average, according to de Groot, of 38 legal moves at each position, a search involving three moves (three half-moves for each player) produces over 3 billion (38^6) terminal positions. You may recall that de Groot's research indicated that human players regularly searched a tree to seven plies and sometimes much deeper. Because of this, Shannon concluded that it would not be possible for the machine to consider all possible legal continuations at each *node* of the game tree. Instead, he proposed a type B strategy in which only reasonable (ie: plausible) moves are pursued at each branching point. If the program considered only five continuations at each node instead of all 38, a 6 ply look-ahead would involve only 15,625 (5^6) terminal positions.

The superior memory of the chess master is chess-specific and not a general trait.

The attractiveness of the type B approach seems overwhelming when the number of terminal positions increases exponentially with depth. The fact that skilled human players explore only a limited number of continuations at each choice point is additional evidence which favors the adoption of this strategy. It is not surprising, therefore, that most programmers have used Shannon's type B strategy in designing a chess program.

Sometimes our understanding of the real world, however, is not always as accurate as we presume. In selecting a type B strategy in preference to a type A strategy, the programmer does not necessarily simplify the problem. This approach was competently implemented in 1967 by Greenblatt at MIT. His program played reasonable, and at that time, fairly impressive chess. The major design problem in a selective search is the possibility that the look-ahead process will exclude a key move at a low level in the game tree. The failure to consider an important move can lead to a very serious miscalculation. A chess game can be lost by a single weak move. For this reason, it is of critical importance that a necessary move not be missed. The type B programs place a critical dependence on the accuracy of their plausible move generator. Chess is an extremely complex game and in many situations a move which at a superficial level seems unlikely, is, in fact, the best one. Grandmasters find these moves while lesser players, including machines, fail to see them. For a decade, several dozen individuals have tried to create a plausible move generator that is superior to Greenblatt's. The evidence is fairly clear, however, that type B programs have improved very little since 1967.

As strange as it may seem, recent progress in computer chess has come by abandoning the type B strategy. Shannon's logical analysis was made in a "stone-age" hardware environment and without knowledge of several important algorithms. Today, the type A strategy is not as ridiculous as it seemed in 1950. In addition, very few individuals anticipated the immense difficulty involved in constructing a competent plausible move generator. To become a chess master, a man has to study chess intensively (20 hrs or more a week) for at least 5 years. During this time he acquires an immense amount of detailed knowledge about the game of chess. Subtle features of a particular position are recognized immediately and suggest both short-term and long-term goals as well as specific moves. This kind of knowledge is sufficiently abstract that most players find it impossible to verbalize the relevant thought processes. The one factor which stands out clearly, however, is that the chess master has acquired a tremendous library of factual information which can be retrieved quickly and applied in apparently novel situations. No chess program has been able to duplicate this facility and, without it, the creation of a workable plausible move generator is next to impossible.

When a type A strategy is employed, however, this problem can be bypassed. By making all the moves *plausible*, the program never overlooks a subtle but important one. In fact, by reverting to a brute force search of all possible continuations, the program often finds interesting combinations that are commonly missed even by strong human players. It seems ironic that the brute force approach (full width searching) produces many more brilliant moves than the smart approach (selective searching). This important discovery was made independently by Slate and Atkin at Northwestern (the authors of the current world champion chess program, Chess 4.6) and by the Russian KAISSA team.

Minimax and the Alpha-Beta Algorithm

Slate and Atkin's work has demonstrated that a full width search can be conducted considerably more efficiently than anyone had previously suspected (including Slate and Atkin; see references). There are a number of important developments which are responsible for this reassessment. The most important discovery was made in the late 1950s by Newell, Shaw and Simon as well as by Samuels. Because of the basic logic underlying a minimax search, it is not necessary to search the entire look-ahead tree before selecting the best move. Consider a simple 2 ply search (one move for you and one for your opponent). First you examine one of your possible moves and the 38 or so terminal positions which result from each of your opponent's legal replies. You select the one reply which is best, according to your evaluation function, for your opponent (ie: the one which minimizes your own maximum potential gain). Next, you consider a second move for yourself and the 38 or so replies that your opponent can make to this move. In considering these moves, you discover that the third reply you examine would give your opponent a better outcome than his best reply to your first candidate. Immediately you realize that it is a complete waste of time for you to analyze any more of his replies to your second candidate. Since you are already guaranteed a worse position after the second move than after the first, it is reasonable to reject the second one and turn to your third candidate. This decision eliminates the need for evaluating 35 of the potential replies to your second candidate. A very tidy savings.

Historically, the score for the best move so far for White has been designated as α and the score for the best move so far for Black has been called β. Thus the name alpha-beta (α–β) algorithm. When the tree is both wide and deep, this algorithm can reduce the number of terminal nodes to a small fraction of the number which would be examined by a complete minimax search. The beauty of this procedure is that it always produces the same result as the full minimax search.

An important factor in determining the efficiency of the alpha-beta algorithm is the order in which the moves are examined. If White's best moves and Black's best replies are considered first at each choice point, the search of the uniform game tree of height h (number of plies deep) and width d (number of successors at each node) will involve approximately $2 \cdot d^{h/2}$ terminal positions instead of d^h (see references, Knuth and Moore). The potential magnitude of this saving can be appreciated by considering our previous example with a 6 ply search: 38^6 is more than 3 billion while 2×38^3 is about 110,000. Shannon might have given more consideration to the type A strategy if he had been aware of the alpha-beta algorithm and some of the other technical improvements which were to follow.

General Strategy

To maximize the benefit of the alpha-beta procedure, it is necessary to devise an efficient strategy for generating the moves at each node in an order which is likely to produce a cut-off, such that searching can be terminated at that node. There are several general heuristics which have proven their value time and time again. One is extremely simple and powerful: try capturing moves first. Because a full width search includes many ridiculous moves, a reply which involves a capture will often remove a piece which was "stupidly" placed *en prise* (ie: attacked and insufficiently defended).

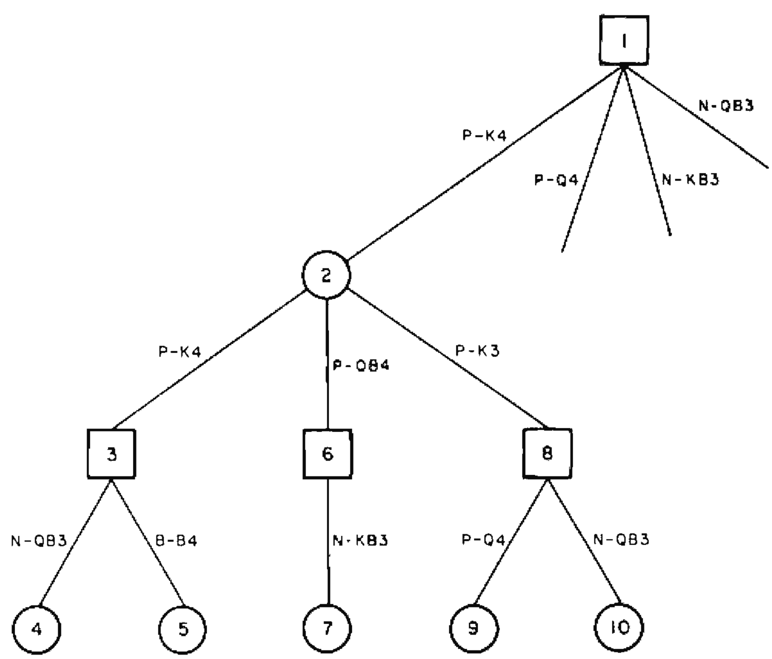


Figure 1: Portion of a game tree for the opening game in chess. Square nodes indicate that White is to play; round nodes that Black is to play. Techniques such as alpha-beta pruning and minimax strategy are used to optimize the use of trees like this.

Captures also have the beneficial effect of reducing the number of potential offspring. An additional important characteristic of a capturing move is that it will generally have to be examined sooner or later in order to insure the quiescence of the terminal position. Because of this, every capture that is examined early generally reduces the amount of work which will have to be done later. In practice, investigators have reported a speed-up in search time of as much as 2 to 1 by simply putting all the captures at the beginning of the move list.

In addition to captures, there is another class of moves which is also effective for producing cut-offs. These are called *killers* because they are moves which have produced cut-offs in the immediate past and have been specifically remembered for that reason. A short list of killers is maintained by the program and whenever the legal capturing moves fail to produce a cut-off, each of the killers (if legal in the given position) is then examined. This *killer heuristic* is quite effective in producing a move order which enhances the probability of a quick cut-off.

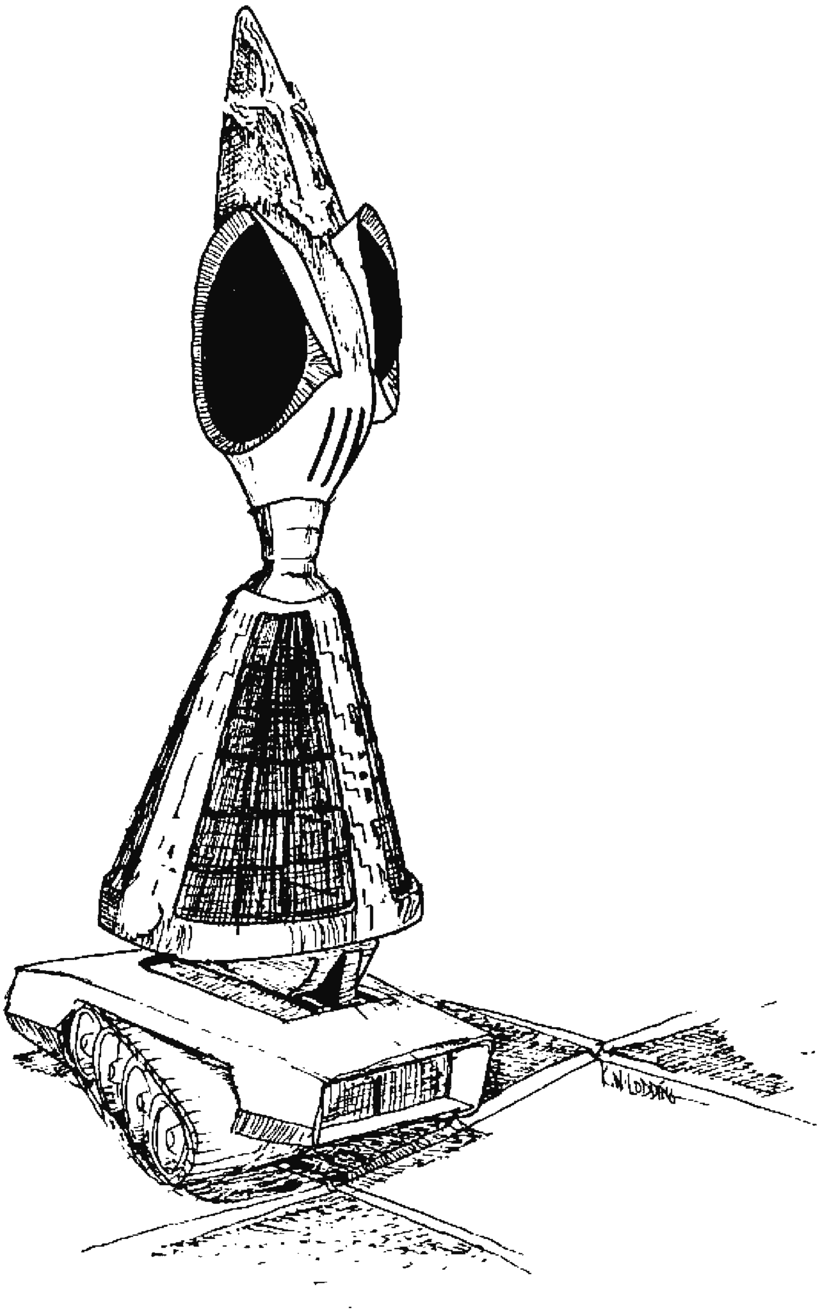
The general features of the alpha-beta algorithm and its important servants, the capture and killer heuristics, were reasonably well-known late in the 1960s. In recent years, several important refinements have been added to this list. One of the most important is the staged or iterative alpha-beta search. For example, instead of conducting a 5 ply search all at once the search is done in stages, first a 2 ply search, then a 3 ply search, then a 4 ply search, and finally a 5 ply search. Superficially this might appear to be wasteful since the staged search requires the full 5 ply search eventually anyway. This is not at all the case. As each search is completed, the principal variation (best moves for each side at each depth) is used as the base for the next (1 ply deeper) search. The 3 ply search therefore starts with a move at ply 1 and a reply at ply 2 which has already been proven to be reasonable (from the machine's limited perspective). The 4 ply search starts with reasonable moves at its first three plies. The 5 ply search has the benefit of reasonable moves at its first four plies. Because the efficiency of the alpha-beta algorithm is tremendously sensitive to move ordering, the spill-over in information from one iteration to the next has a surprisingly powerful effect. A single 1 stage 5 ply search might require 120 seconds of processor time. The last segment of the staged 5 ply search might require only half as much time (ie: 60). Since each iteration requires about five times as much processor time as its predecessor (the exponential character of the look-ahead tree is diminished somewhat by the alpha-beta algorithm), the staged 4 ply search would take about 12 seconds, the staged 3 ply search about 3 seconds, and the 2 ply search about 1 second. The total time for the iterative search would be approximately 76 seconds (1 + 3 + 12 + 60) rather than 120 seconds.

An added benefit of the iterative search, and, incidentally, the reason for its discovery in the first place, is that it provides a useful mechanism for time control. In tournaments, a move must be calculated within a fixed time limit such as 90 to 120 seconds. If one decides to do a 5 ply search in a single stage, it is possible to find oneself tied up in calculation after 120 seconds with no idea of how much more time will be needed to complete the search, and without a move to make until the search is completed. In some complex situations the search might take as long as 10 minutes — a disaster for time control. An iterative search allows one to predict the probable duration of the next iteration and to make a decision whether it is cost effective to initiate the next one. If this decision is a go and the search, for some reason, fails to terminate in the anticipated time, the machine can abort and play the move selected by the last iteration. This provides relatively neat and tidy time control. The iterative search was first mentioned by Scott in 1969 and was apparently discovered independently several years later by Jim Gillogly at Carnegie-Mellon, by Slate and Atkin at Northwestern and by the Russian KAISSA team.

Refinements to the Type A Strategy

Several other refinements have also made the type A strategy more manageable. One of the time intensive activities involved in tree searching is move generation. This can be minimized by generating only one move at a time and seeing if it produces a cut-off before generating the next move. If a cut-off occurs and the node is abandoned, one can avoid generating a large number of potential moves. With the n-best approach, it is customary to generate all moves at each node and then invest time attempting to decide which ones are worthy of further consideration. Thus the smaller tree, obtained by selective searching, has to be partially paid for by an additional time investment in plausibility analysis.

Another time-intensive activity in the tree search is the repeated use of the evaluation function. Since many thousands of terminal nodes have to be evaluated in each move selection, any refinement that reduces the work of the evaluation function will pay rich dividends. There are three important



techniques which fall in this category. One of these is called *incremental updating.* In order to make an evaluation of a node, it is necessary to have certain key facts available, such as which squares are attacked by each piece, which pieces are present, etc. This information can be newly calculated at each terminal node or can be incrementally maintained by updating the appropriate tables as the tree is generated during the search. This latter procedure is more complex to program but tremendously more efficient in terms of computing time because neighboring terminal positions are highly similar. They usually differ in respect to only a single piece, and therefore the updating procedure requires about 10 percent of the computations that would be expended if the evaluation data base were recalculated from scratch for each evaluation.

A second refinement in this category is the use of serial organization in the evaluation function. In order to assess the relative merit of a chess position, most programs place heavy emphasis on the material balance (ie: the relative number of pieces for each side). This tradition is founded on the idea that winning or losing is strongly correlated with being ahead or behind in material. An additional rationale is that this information is readily available and easily updated.

In most programs material factors are so dominant that the other evaluation terms, such as mobility, pawn structure, King safety, area control, etc, taken together almost never account for more than two pawns. Because of this, it makes sense to compute the material balance factor first and then determine if the result is within two pawns of the target value. If not, there is no need to assess the other factors, because the final decision will be independent of their value.

This simple idea encourages one to organize the evaluation function in strict serial order such that influential (heavily weighted) terms are analyzed first and the result examined to see if a decision is possible based on this initial information. If not, the next most influential term(s) are examined and another determination is made. This process is repeated until an escape condition occurs or until all terms have been examined. In most cases, the evaluation will be terminated long before the list of potential terms has been exhausted. This technical refinement can save a significant amount of time.

A third procedure for speeding the evaluation process is to remember past evaluations. For instance, one should avoid reassessing the same position two or more times. In chess, there are many pathways by which one can reach identical positions. In a 3 ply sequence in which the middle move remains constant, for example, the first and third moves can be interchanged and the resulting position will be the same. Transpositions such as this occur frequently in the end game where the King may have literally hundreds of 4 move pathways that end on the same square. Rooks, Bishops and Queens also have a special facility for reaching a particular destination square in multiple moves rather than in one or two.

A full width search (ie: type A strategy) greatly accentuates this foolishness. By creating a large table of past positions which have been already evaluated, and using a hashing procedure to check if the present position is in the table, the programmer can completely eliminate a portion of the evaluation effort. In most middle game positions, this technique will produce a 10 to 50 percent saving. In certain end game positions, however, the transposition table can eliminate more than 80 percent of the evaluation effort. This idea seems to have been implemented first by Greenblatt in 1967.

An extension of this idea is to use the table to store likely moves as well as evaluations. By remembering a move which previously produced a cut-off, the table can facilitate move ordering decisions. In addition, the use of the same reply at a familiar position may have the added benefit of increasing the number of transpositions which will be encountered at later nodes. Additional details on the use of a transposition table are discussed in chapter 4 of *Chess Skill in Man and Machine*.

One of the most difficult challenges for a chess program is the end game. A machine which calculates a move for each position has difficulty competing with humans who "know" the correct move on the basis of their own or someone else's past experience. There are a huge number of end game situations in which a specific and highly technical strategy is required. Strong chess players study these intricacies at great length and use this knowledge at the chessboard to avoid unnecessary calculations. For example, a King and a pawn against a lone King is a win in some positions, and a draw otherwise. The same is true for a King and two pawns against a King and a pawn. If a Rook or minor piece is added to each side, the situation changes dramatically. Unfortunately our present day programs are oblivious to these subtleties. For this reason they can find the correct move only by engaging in prodigious calculations. Their human counterpart, on the other hand, "knows" the correct move after a cursory glance at the position.

Newborn (see references) has introduced a useful technique for reducing this knowledge gap. The main idea is to categorize familiar end game positions as wins or draws. Many games end with a King and a pawn fighting a lone King. Skilled players usually terminate the contest before it runs its inevitable course because the outcome is not in doubt. Newborn has shown that it is feasible, taking advantage of the symmetries of the chessboard, to make a bit map that indicates either a win (1) or a draw (0) for each potential square on which the lone King might reside for each of the potential locations of the opposing King and pawn. This knowledge can be encoded in approxmately 300 bit boards of 64 bits each (see chapter 5 of *Chess Skill in Man and Machine*).

Although a tremendous amount of work and chess knowledge is required to complete this task, the end result is well worth the effort. When a position involving two Kings and a pawn is encountered anywhere in the look-ahead tree, it can be immediately scored with 100 percent accuracy as a win or a draw. This extends the look-ahead horizon of the program by as much as 12 to 15 plies for these specific situations, and eliminates all the tree searching effort which would normally be required. Furthermore, it permits accurate evaluations at the end points of a deep search, which allows the program to select a continuation which leads to a favorable end game. If this approach were extended to a wider range of situations, the machine's present knowledge deficit with respect to the end game would be greatly reduced.

These programming refinements, together with rapid hardware advances, have made the Shannon type A strategy feasible if not particularly elegant. For this reason it is possible to program a machine to play a game of chess which is free of gross blunders and which sometimes even contains an innovative move or two. Although this approach is clearly not a final solution, it does provide a solid base which can be used as a reliable starting point for future developments.■

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What's New?

A Chess Playing Program for the TRS-80 Microcomputer

Microchess 1.5 for the Radio Shack TRS-80 microcomputer has been announced by Personal Software in conjunction with Peter Jennings of Micro-Ware Ltd. Microchess is a 4 K byte Z-80 machine language chess playing program described in "Microchess 1.5 versus Dark Horse," March 1978 BYTE, page 166. The program has three separate levels of play designed for beginners, intermediate players and experienced players.

The program is available in both Level I and II BASIC versions for the TRS-80. Standard algebraic notation is used to describe the moves to the computer. Every move is verified for legality to prevent user error, and a simple command allows temporary numbering of the squares to assist in move entry. The chessboard is displayed using the graphics mode available on the TRS-80.

Microchess 1.5 is being offered at a temporary introductory price of \$19.95. Microchess 1.0 was described in What's New, February 1978 BYTE, page 200. Contact Personal Software, POB 136, Cambridge MA 02138. If you have questions on Microchess call (617) 783-0694. For Visa and Mastercharge credit card orders dial toll-free (800) 325-6400; in MO dial (800) 342-6600.■

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Open Item Billing System for Small Business Use

According to a release from Structured Systems Group Inc, 5615 Kales Av, Oakland CA 94618, accounts receivable can now be processed on your 8080 or Z-80 based CP/M microcomputer system.

The general ledger compatible accounts receivable system is a full open item billing system for small businesses. The programs are designed for use by business oriented professionals who need reliable and simple operations. The system is documented with a 120 page reference manual that orients the first time user and provides depth for the experienced hand.

The accounts receivable system is priced at \$750 and features itemized statements, two aged trial balance reports, late charges, reminder letters, recurring receivables, sales reports and more.■

Circle 588 on inquiry card.

Match Your Chess Skills with Boris

Boris is a recently developed chess computer that can flash messages to its opponent such as *Illegal move, Congratulations, Stalemate,* and *I expected that.* It is designed for all levels of ability from the beginner to the master player.

The electronic position programming permits the player to set up any board position desired. This programming flexibility is designed to allow advanced players to set up board situations and practice specific strategies. Also, beginners can use the feature to remove pieces at any time during a game for handicapping. Boris displays each rank electronically so the player always knows where the pieces are.

Boris will play either black or white or even play itself. If a player is unsure of what move to make, Boris is programmed to suggest the best possible move. When Boris gets his opponent into a corner, you can change places with it and see how it battles its way out of its own trap.

All the classic chess moves are in the computer's programs, such as castling, capturing en passant and queening, and Boris will solve all mate-in-two problems. Players will not get the same game twice since the computer is programmed for random play.

Boris costs \$299.95 in a solid walnut case along with a compact chess board plus a set of pieces. Contact Chafitz Inc, 1055 First St, Rockville MD 20850.■

Circle 589 on inquiry card.

Palo Alto Tiny BASIC Extended for North Star

California Software has made available Palo Alto Tiny BASIC Extended (PATB) for use with the North Star DOS. According to the firm, all save and load functions are available for disk storage and loading of programs. Programs are said to be automatically sized, typed and saved without leaving PATB, even the disk directory can be accessed while still in PATB. The extended version of the software allows string handling along with other advancements. Although originally designed as a memory saving interpreter, it provides an alternative language of North Star users at an affordable price. The product is available on diskette for $30 (plus 6% sales tax for California residents), including user's manual. Contact California Software, POB 275, El Cerrito CA 94530.■

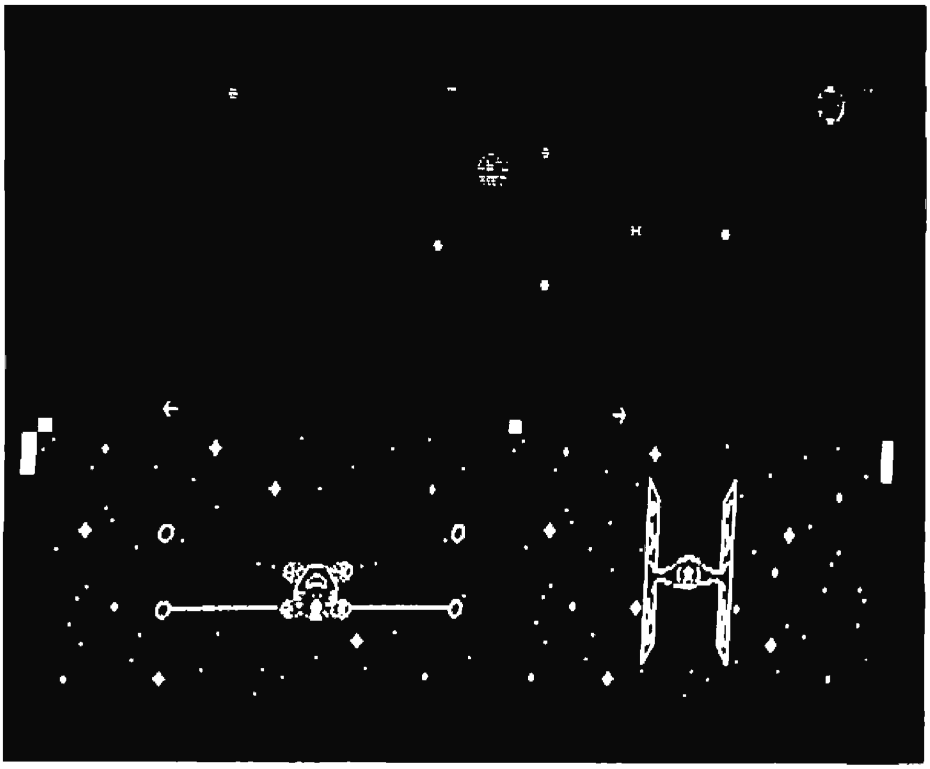
Circle 605 on inquiry card.

Software for North Star Disk Systems

The following software programs have been announced for the North Star Micro-disk System: Maillist is a general purpose mailing label program. It is said to be capable of producing formatted lists for tractor fed or Xerox type labels. Maillist will also sort lists for any field, name, address, city, state or zip. DOS In-Out Driver Version 4.0 is designed to set up mapped memory video boards with its driver located at C700H and a terminal at port 1. Register is a flexible cash register and inventory control program which records transactions, writes sales receipts and flags items which fall below prespecified reorder quantities. Prices are $39.95 for Maillist, $12.95 for In-Out Driver, and $299.95 for Register. Contact Alpha Data Systems, POB 267, Santa Barbara CA 93102.■

Circle 606 on inquiry card.

Star Wars Simulation Now Available



The Star Wars simulation game, an adaptation of the end of the movie battle against the Death Star, is a real time simulation. Under player control, ships move in three dimensions to create a realistic simulation of actual space flight. Objects increase in size as the ships approach and diminish as they pass. Weapons, deflector screens, and a directional control joystick are implemented in each ship. Ships of the rebel forces must pass through Imperial defenses and Tie-fighters to enter a channel on the Death Star.

The game requires the high density graphic display provided by Objective Design's programmable character generator. Written in 14 K bytes of 8080 assembly language, the program code is offered on Tarbell and CUTS tape. Game rules and instructions for assembling the required ship control boxes are included in the total price of $7.50. The game is available from Objective Design Inc, POB 20325, Tallahassee FL 32304.■

Circle 607 on inquiry card.

Air Conditioner Selection Program in North Star BASIC

An Air Conditioner Selection Program (ACSP) written in North Star BASIC has been developed by HSC Computer Services Ltd, POB 43, Brooklyn NY 11236. The package allows the calculation of the necessary capacity of an air conditioner in BTUs per hour, taking into account the heat gain through windows, walls, ceiling, floor, electrical equipment, number of people in room and heat loss through doors and arches. The program applies a correction factor depending on locality in the United States. Also available are North Star error messages and their meaning.

Price of the ACSP package on diskette with a user manual is $19.95, and the North Star Error Message Summary is $5.■

Circle 609 on inquiry card.

SOLOS Tied to North Star DOS and BASIC

Microcomputer Resources Inc has announced a software package which is said to tie the North Star disk operating system (DOS) and North Star BASIC to the SOLOS IO routines and allow the use of the CUTS tape IO port for archive storage of data. The tape routines are accessed as IO devices. The cursor control keys on the SOL are interfaced to BASIC, allowing most edits in the line editor without the use of control keys. The package is said to allow the user to list the directory of a disk while in BASIC. Documentation for the software is included on the disk.

The package sells for $10 for the diskette and program, and a $2 shipping and handling charge. Contact Microcomputer Resources Inc, 3000 Medical Park Dr, Suite 107, Tampa FL 33612.■

Circle 610 on inquiry card.

PDP-8 Simulator for 8080

The Simul8tor is said to be a complete PDP-8 simulator for the 8080. Simul8tor enables 8080 owners to utilize the thousands of PDP-8 programs available both commercially and through the Digital Equipment Corporation User's Society (DECUS). DECUS software such as ALGOL, BASIC, FOCAL, SNOBOL, FORTRAN, LISP, assemblers, editors, debuggers, floating point, etc, is readily available. The simulator is available in two formats: Intel paper tape and Intel Tarbell cassette. It comes complete with a user's manual, PDP-8 programming tutorial, PDP-8 loader, DECUS library information, and a source listing of its IO routines for users who wish to modify them. Prices are: one to three, $20 each; four to ten, $18 each; and 11 and up $15 each. Discounts may be applied to any format combination. Add $3 for each cassette ordered. Contact The Amide Corp, POB 600, Sag Harbor NY 11963.■

Circle 608 on inquiry card.

Personal Software Catalog Offers Large Selection of Software Packages

This new catalog is filled with software ranging from entertainment and self-education to personal finance, home information management and a variety of hobbies. A sampling of some of the software available includes: Stimulating Simulations, a set of ten games that simulate a situation that may be realistic or fanciful; Microchess, which enables the user to play chess against a TRS-80 computer; assembler in BASIC to make it possible to write programs in assembly language for the 6502 processor and have them translated to machine language for direct execution on the PET; and a word processing package available for PET owners who would like to compose and edit letters, articles and manuscripts at the computer and obtain corrected output at high speed. For a catalog containing these and other software packages, PET and TRS-80 owners should write to Personal Software, POB 136, Cambridge MA 02138, giving their serial numbers, memory size, and describing their most wanted software products.■

Circle 642 on inquiry card.

Software Publication

A publication called *The Software Exchange* has been announced by its publisher Alan Bartholomew. Intended as a sort of "want ad" publication devoted to software produced by individuals, the plan is to put out six issues per year at a $5 per year subscription fee. For further details contact *The Software Exchange*, POB 55056, Valencia CA 91355.■

Circle 646 on inquiry card.

Attention Readers, and Vendors. . .

Where Do New Product Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the neat new whizbang gizmo or save the world software package is of interest to the personal computing experimenters and homebrewers who read BYTE, we print the information in some form. We openly solicit such information from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications.

Computer Chess Program Available in Assembly Language

Software Specialists, POB 845, Norco CA 91760, have announced a computer chess program for 8080 and Z-80 based microcomputers. This assembly language program conforms to all rules and conventions including castling, en passant captures, and promotion of pawns. The entire program, including input/output (IO) routines, will run in 8 K bytes of programmable memory.

The user can select one of two board sizes for display. . .large for 24 by 80 inch videos, or small for television typewriters and Teletypes. A level of difficulty between 2 and 5 is selected, with level 3 playing an average game. Both the user's and the computer's moves are displayed in standard chess notation.

For users with a North Star disk system, the program is available on disk and uses the DOS IO routines. The program is also available on paper tape with a 256 byte block reserved for the user's IO routines. Instructions are provided for loading the program and patching the IO routines.

The program is available in either form for $35. A deluxe version which allows presetting of the board to any playing situation is available on North Star disk only for $50. The standard starting addresses are 2A00H for disk and 0000H for paper tape. Other starting addresses are available on request at no extra charge.■

Circle 647 on inquiry card.

Assembler for Microprogramming of Bit Slice Microprocessors

The Signetics Micro Assembler is a software package designed to be used for the complete microprogramming cycle including defining microinstructions, writing and assembling programs, and generating paper tape output for read only memory programming. The assembler permits flexible editing for debugging and program alterations through iterated loops, updates, and replacements, and includes a built-in test program to check system accuracy.

The assembler is written in ANSI FORTRAN IV and can be run on any 16 or 32 bit computer with FORTRAN capability.

The microassembly language provides direct support for the 3002 and 2901-1 bipolar processors and the 8X02 Control Store Sequencer. Through the inclusion of explicit definitions, similar support can be obtained for the 3001 Microprogram Control Unit, as well as other bipolar processing elements and sequences.

The Micro Assembler is available in source form on 9 track tape for $775. Contact Signetics Corp, POB 9052, 811 E Arques Av, Sunnyvale CA 94086.■

Circle 643 on inquiry card.

System Monitor for 8085 Microprocessor

The Micro Mate-85 is a hardware connected system monitor for the 8085 processor. When operating in conjunction with a terminal or video display, it provides a means of examining and modifying memory locations and microprocessor registers at any point in an operating program through the implementation of addressable traps. The operating program may be started or stopped at any location, or the program may be stepped one location at a time. The monitor provides a means of loading or punching a paper tape of memory data for microprocessor systems not containing conventional peripheral IO. Contact Spectrogram Corp, 385 State St, North Haven CT 06473.■

Circle 644 on inquiry card.

Timeshare Disk BASIC System for North Star

A timeshare disk BASIC system is now available for users of the North Star floppy disk system. Designed to operate with microcomputers using the 8080 or Z-80 processors, Northshare provides up to four independent users with selectable memory partitions and buffered terminal outputs.

Minimum memory requirements for operation are 24 K bytes. There are no special hardware requirements other than additional terminals and IO ports to support the multiple users.

System includes one diskette with release 3 of North Star BASIC and DOS with Northshare supervisor and documentation package. Price is $48 from the Byte Shop of Westminster, 14300 Beach Blvd, Westminster CA 92683.■

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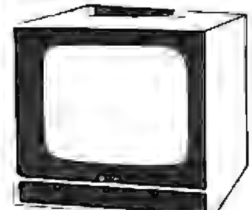

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Convert T.V set to Video Monitor
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apple II

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S-100 Bus compatible
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Upper case, lower case and Greek,
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Dynamic Ram Chip can be used for expanding Apple II Memory or the TRS-80 (200ns)

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$495.00

MODEL 801R Shugart Disc with Cabinet

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* 2 Serial interfaces with RS232 interfaces or 1 Kansas City cassette interface.
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Cards Welcome

The Piggy is coming!

Circle 195 on inquiry card.

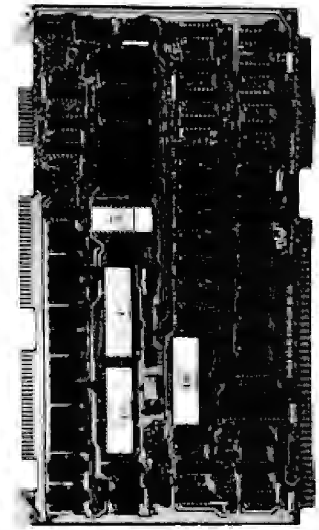
A New Appliance Computer from Pertec

Sometimes a few surprises happen. A recent case in point is the appearance of a new computer from Pertec Computer Corp's Microsystems Division (iCOM and MITS). This new computer, called Attaché, is a surprise because it fits the functional definition of the "appliance" computer: it can be purchased off-the-shelf in a ready to use condition. The base price of $1449 gets an assembled and tested computer, to which (at extra cost) one must add a BASIC interpreter on a read only memory board for the internal S-100 bus.

The Attaché comes with a full ASCII keyboard, upper and lower case. It has a 10 slot board capability, LED indicators for on and off status, a reset switch which returns to the programmable read only memory monitor, a monitor PROM that controls operation of the computer from the keyboard, and a 75 Ω video output jack. The video output provides 16 lines of 64 characters and a choice of black on white or white on black display. The system includes forced air conditioning over the vertically mounted cards and a power supply which provides 10 V at 10 A (regulated to 5 V on boards), with preregulated +18 V and −18 V, each rated at 2 A. A 1 K volatile memory region and extra sockets for programmable read only memories are standard. The basic configuration includes keyboard, processor board, video board, and turnkey monitor board. Contact Pertec Computer Corp, Microsystems Division, 21111 Erwin St, Woodland Hills CA 91367.■

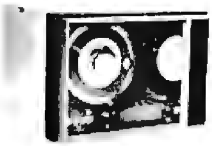
Circle 596 on inquiry card.

Intel Introduces Improved Single Board Computer

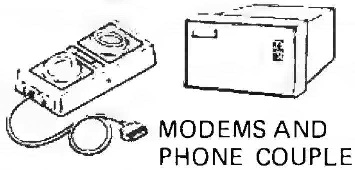


The iSBC 80/10A Single Board Computer, an enhanced version of the iSBC 80/10, has been introduced by Intel. The 80/10A gives the user up to twice the read only memory capability presently available on the 80/10, for the same price. The 80/10A sells for $495 and includes the Intel 8080A central processor, system clock, 1 K bytes of programmable memory, up to 8 K bytes of nonvolatile read only memory and both parallel and serial IO. The unit is available from Intel Corp, 3065 Bowers Av, Santa Clara CA 95051.■

Circle 597 on inquiry card.



TAPE DRIVES



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Bell 202:
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- VADIC PCB only, with interface instructions, with Reverse Channel, Manual DAA $149.95
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CONVERT IBM OFFICE SELECTRIC to I/O Typewriter: solenoids, switches, wire harness, magnet driver PCB plus instructions +8080 Interface Diag. $150.00

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3½ in	86	2 80	5 12/K	4 55/K
4 in	90	3 00	5 52/K	4 88/K
4½ in	94	3 21	5 93/K	5 21/K
5 in	98	3 42	6 34/K	5 52/K
5½ in	1 02	3 65	6 75/K	5 86/K
6 in	1 06	3 85	7 16/K	6 19/K
6½ in	1 15	4 05	7 57/K	6 52/K
7 in	1 20	4 25	7 98/K	6 85/K
7½ in	1 25	4 45	8 39/K	7 18/K
8 in	1 29	4 65	8 80/K	7 53/K
8½ in	1 32	4 85	9 21/K	7 84/K
9 in	1 36	5 05	9 62/K	8 17/K
9½ in	1 40	5 25	10 03/K	8 50/K
10 in	1 45	5 51	10 44/K	8 83/K
Addl. inches	10	41	82/K	66/K

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Ribbon cable connectors for connecting boards to front panels or board to board

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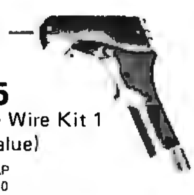
	14 pin	16 pin	24 pin	14 pin	16 pin	24 pin
6"	1 24	1 34	2 05	2 24	2 45	3 37
12"	1 33	1 44	2 24	2 33	2 55	3 92
24"	1 52	1 65	2 63	2 52	2 76	4 31
48"	1 91	2 06	3 40	2 91	3 17	5 08

WIRE WRAP TOOLS



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WSU 30 Hand Wrap-Unwrap Strip Tool	6.25
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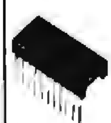

	1-9	10-24	25-99	100-249	250-999	1K-5K
• 8 pin	.35	.33	.31	.29	.25	.23
• 14 pin	.35	.33	.31	.29	.28	.27
• 16 pin	.37	.35	.33	.31	.30	.29
• 18 pin	.60	.55	.45	.43	.40	.37
20 pin	.84	.78	.71	.63	.59	.54
• 22 pin	.90	.85	.82	.78	.70	.60
24 pin	.91	.84	.78	.68	.64	.59
25 pin strip	1.25	1.05	.95	.80	.70	.65
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40 pin	1.50	1.40	1.30	1.20	1.05	.90

Gold 3-Level Closed Entry Design.

*End & Side Stackable. All prices include Gold.

2 Level Sockets Also Available.

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44 Pin	Solder Tail	$1.75	$15/10
100 Pin	Solder Tail	3.50	$30/10
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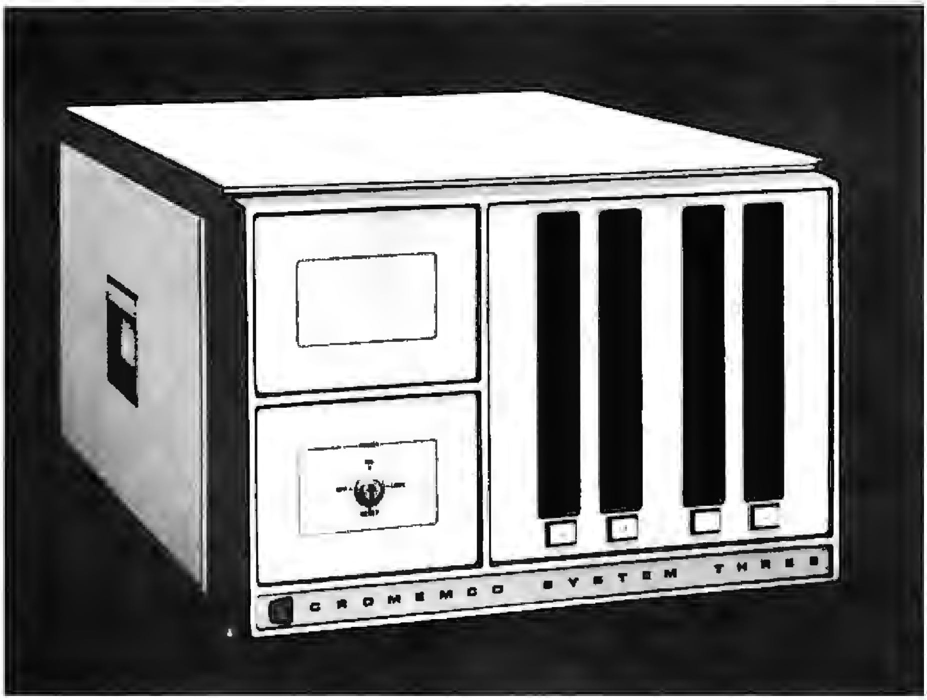
Cromemco Features a Z-80 Based Microcomputer



Cromemco's System Three is ideal for a wide range of professional work in almost any field. It consists of a 4 MHz Z-80 based microcomputer, 32 K bytes of programmable memory (two 16 K byte cards) expandable to 512 K bytes, an RS-232 interface, a parallel printer interface, a video terminal with line editing and block mode transfer capabilities, and a fast line printer with 132 columns.

System Three is available with a number of options including a programmable read only memory programmer for development work, an additional dual disk drive and additional memory. With the optional second disk drive, System Three provides a megabyte of disk storage.

It has several provisions for protection of disks including software control for ejection of disks if desired, a key switch that will disable the disk eject buttons when in the LOCK position and motor driven disk loading and unloading.

Currently available software includes a FORTRAN IV compiler, a 16 K byte Z-80 BASIC, and a Z-80 macroassembler and linking loader. All software is available on standard, IBM format, soft sectored diskettes.

The System Three mainframe is available for $5990. The additional video is available in two models for either $1595 or with expanded capabilities including line editing and block mode transfer for $1995. The additional line printer is also available in two models including a 180 character per second model for $2995 and a 60 character per second model for $1495. For more information, contact Cromemco Inc, 280 Bernardo Av, Mountain View CA 94040.■

Circle 601 on inquiry card.

Compucolor Introduces Series of Color Home Computer Systems

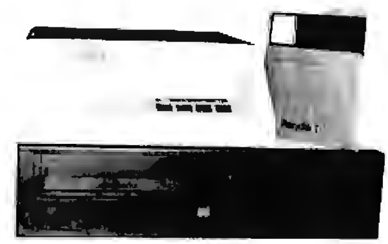
The Compucolor II is a personal computer system available in five models, with its own 8 color, 13 inch (33.02 cm) diagonal display, a typewriter-like keyboard with 3 key rollover, 8080A processor, 4 K bytes to 16 K bytes memory (depending on the model), and a built-in minidisk drive mass storage device. The Compucolor II utilizes BASIC 8001, a conversational programming language with English-type statements and familiar mathematical notations.

Games like Star Trek, Blackjack, Chess, Checkers, Othello, and educational games for youngsters are available on diskettes. In addition, there are programs available for checkbook balancing and income tax compilation.

Prices for the Compucolor II range from $795 to $1995. Further information can be obtained from Compucolor Corp, POB 569, Norcross GA 30091.■

Circle 602 on inquiry card.

New Microcomputer Based on TI TMS 9900



The SS-16, a 16 bit microcomputer based on the Texas Instruments TMS 9900, has been introduced by Technico Inc, 9130 Red Branch Rd, Columbia MD 21045. System memory is expandable up to 64 K bytes, and the unit is available with dual floppy or minifloppy disks. Expansion cards provide up to six RS-232 and 20 mA current loop interfaces. Also available are a 64 color video board and a 128 bit parallel input and output board, a complete editor, assembler, linking loader and BASIC. European 220 V, 50 Hz models are also available.■

Circle 603 on inquiry card.

S-100 Microcomputer Price Reduction

Quay Corp, POB 386, Freehold NJ 07728, has announced that its Q80AI, Z-80 based, S-100 compatible microcomputer has been reduced in price. The Q80AI, formerly priced at $550, is now available, factory assembled and tested for $350. The unit includes 1 K byte static programmable memory, 1 K byte programmable read only memory resident monitor, on board programmable read only memory programmer, keyboard interface and serial (RS232C/TTY) input and output (IO).

Quay has also package priced the Q80AI, the Q80SMB (8 K byte static memory board) and the Q-TBPE-80 (Palo Alto Tiny BASIC-extended) to sell for $495.■

Circle 604 on inquiry card.

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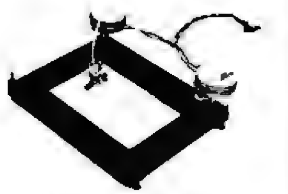
FEATURING THE IEEE 488 BUSS
THE RS 232 SERIAL DATA INPUT
INTERFACE OPTIONS
OR DIRECT FROM ANY TTL PORT



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UHF Version. Operates above channel 14. Eliminates worms

Operates above the switching harmonics of the computer, thereby yielding a cleaner, worm-free picture. Tunable over a minimum of 4 channels. Interfaces directly with the Apple II as well as most other micros. Comes with video cable and RF output stub coupler. Two-toned cowl type decorator cabinet. Size: 5.5cm x 8.5cm x 11.5cm. Power:+5V. Current approx. 1 ma. Self-powered with 4 pencell batteries. Operating life in excess of 1000 hours or near shelf-life of batteries. Excellent stability. Precise frequency adjustment. No assembly required except for installation of batteries, not supplied. MODEL MVX-500.

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16/4+1 EPROM/RAM BOARD KIT	$130.00
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11 SLOT MOTHER BOARD with sockets	$80.00
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16K E-PROM CARD

New!

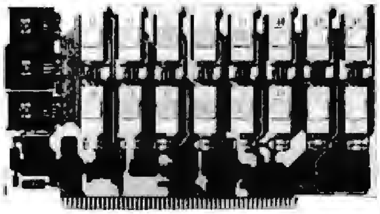
IMAGINE HAVING 16K OF SOFTWARE ON LINE AT ALL TIME!

S-100 (Imsai/Altair) Buss Compatible!

KIT FEATURES:

1. Double sided PC board with solder mask and silk screen and gold plated contact fingers.
2. Selectable wait states.
3. All address lines & data lines buffered!
4. All sockets included.
5. On card regulators.

KIT INCLUDES ALL PARTS AND SOCKETS (except 2708's). Add $25. for assembled and tested.



PRICE CUT!

$57.50 kit

WAS $69.95

SPECIAL OFFER: Our 2708's (450NS) are $8.95 when purchased with above kit.

8K LOW POWER RAM KIT-$149.00

Fully Static!

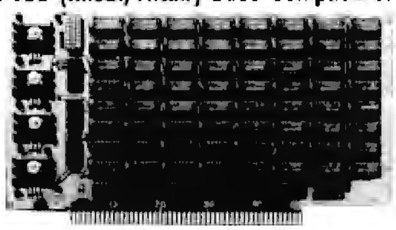
ADD $20 FOR 250NS

S-100 (Imsai/Altair) Buss Compatible!

KIT FEATURES:

1. Doubled sided PC Board with solder mask and silk screen layout. Gold plated contact fingers.
2. All sockets included.
3. Fully buffered on all address and data lines.
4. Phantom is jumper selectable to pin 67.
5. FOUR 7805 regulators are provided on card.

(450NS)



USES 21L02 RAM'S!

2 KITS FOR $279

Fully Assembled & Burned In $179.00

Blank PC Board w/ Documentation $29.95

Low Profile Socket Set 13.50

Support IC's (TTL & Regulators) $9.75

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MC 3401 PIN FOR PIN SUB. FOR POPULAR LM 3900
3 FOR $1

ALARM CLOCK CHIP
N.S. MM5375AA Six Digits With full Data **New!**
$2.49 each

FULL WAVE BRIDGE
4 AMP. 200 PIV.
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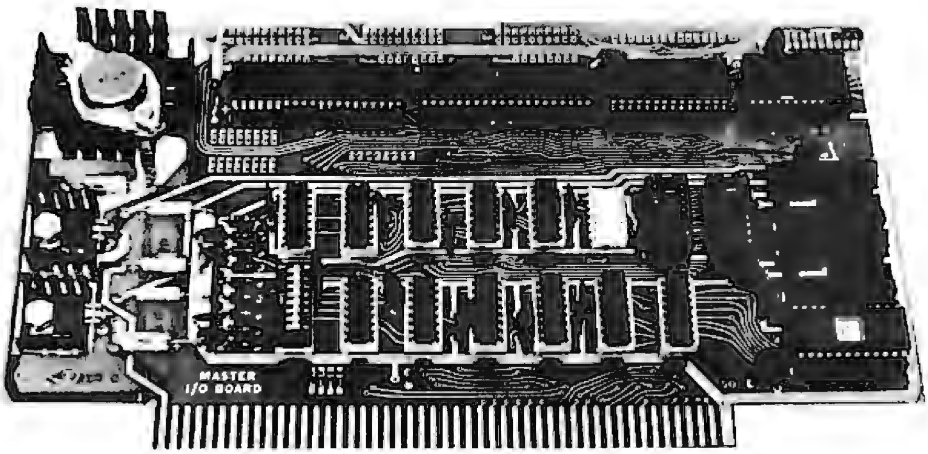
S-100 IO Read Only Memory Board



The Master IO contains enough read only memory and IO to allow a 2 board S-100 system and can be used to emulate the Intel SBC IO functions. This board can replace a real time clock, a frequency and period counter, programmable read only memory and programmable memory, and parallel and serial IO cards.

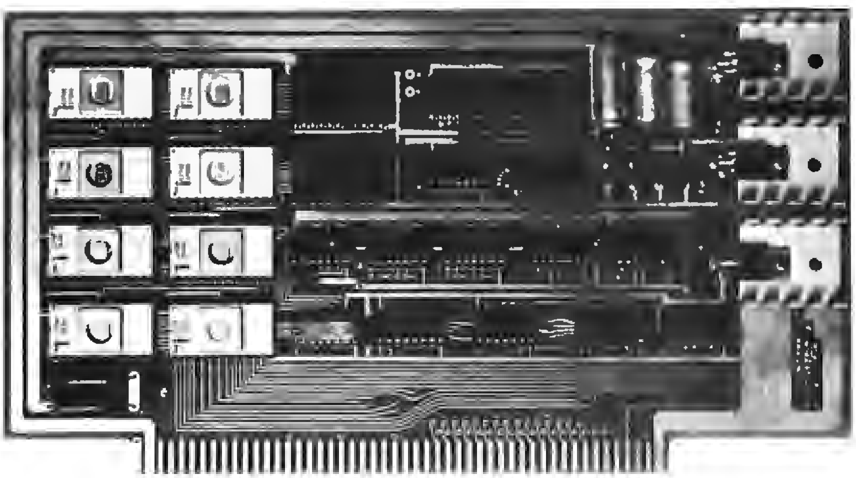
Besides 1 K bytes programmable memory and 3 K read only memory, the board has the following peripheral chips: two 8255s which can be programmed to be input ports, output ports, handshaking ports and a bidirectional data port. One of the ports on each chip can use bit and reset commands. Each 8255 has a total of 24 possible IO lines. One 8253 has three 16 bit counters and timers in each chip. Each counter and timer can be programmed to be a binary counter or a binary coded decimal counter, a programmable one shot, a digital delay, a pulse wave rate generator (divide by N), a square wave rate generator, a software triggered strobe and a hardware triggered strobe.

The 8251 universal synchronous and asynchronous transceiver can be programmed for various clock division ratios. All the usual UART functions are available plus synchronous serial IO to 56 bps. One of the 8253 counters is dedicated to the USART (8251). This allows complete software programability of bps rates. Over 60,000 bps data rates are available.

For further information, write to Space Time Productions, 2053 N Sheffield, Chicago IL 60614.■

Circle 549 on inquiry card.

S-100 PROM Board



This programmable read only memory (PROM) board for the S-100 bus can be used with eight 2708 type E read only memories with provisions for using 2716s or the pin compatible 8316 memories. This provides for a total storage capacity of 12 K bytes.

While the board is prejumpered for the use of the programmable read only memories as a continuous block of memory, the address decoding scheme provides for using any programmable read only memory anywhere within the memory map. This addressing scheme provides monitors at both the low and high order end of the memory map.

The memory ready line is pulled low when slower memories are utilized. Three spare 16 pin pads are provided on board for user electronics.

The board is available in kit form, fully socketed at $59.95; assembled and fully tested versions are also available at $109.95. Bare boards can also be obtained. For further information contact Mini Micro Mart, 1618 James St, Syracuse NY 13203.■

Circle 550 on inquiry card.

Memory Board Compatible with SBC 80 Multibus

This 32 K byte programmable read only memory board is compatible with Intel's SBC 80 Multibus. The PROM-32 accepts 16 2716 erasable read only memories. All integrated circuits are socketed. Base addresses fall on 16 K byte boundaries and are jumper selectable. Any number of 2 K byte memory address blocks may be deselected by jumper removal. Memory access time is 475 ns maximum. The board uses 5 V at 0.38 A typical, and 0.72 A maximum fully loaded. The board is priced at $195 in unit quantity and can be obtained from Electronic Solutions Inc, 7969 Engineer Rd, San Diego CA 92111.■

Circle 553 on inquiry card.

EMM Cuts Prices on 2 K Static Memory

A major price cut on the 3539 2 K byte static programmable memory has been announced by EMM Semi Inc, 3883 N 28th Av, Phoenix AZ 85107. In quantities of 500, the price has been cut from $7.80 to $4.05.

The 3539 is a byte organized 256 by 8 static programmable memory comprising a small memory on an integrated circuit. It replaces the older 256 by 4 programmable memories (2101 and 2111) for many small memory applications, since only one component is required instead of two. For more information, contact EMM Semi Inc.■

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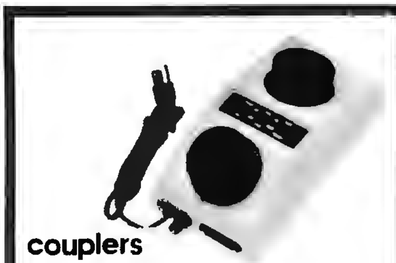

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Priced at ONLY **$199.95** Basic Software Included

SPECIAL FEATURES:

- S-100 bus compatible
- Parallel keyboard port
- On board 4K screen memory (optional)* relocatable to main computer memory
- Text editing capabilities (software optional)
- Scrolling: up and down through video memory
- Blinking characters
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- Provision for on board ROM
- CRT and video controls fully programmable (European TV)
- Programmable no. of scan lines
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- Cursor controls: up, down, left, right, home, carriage return
- Composite video

*Min. 2K required for operation of this board.

DISPLAY FEATURES:

- 128 displayable ASCII characters (upper and lower case alphanumeric, controls)
- 64 or 32 characters per line (jumper selectable)
- 32 or 16 lines (jumper selectable)
- Screen capacity 2048 or 512
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OPTIONS:

Sockets	$10.00
2K Static Memory (with Sockets)	$45.00
4K Static Memory (with Sockets)	$90.00
Complete unit, assembled and tested with 4K Memory	$335.00
Basic software on ROM	$20.00
Text editor on ROM	$75.00

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8080 SUPPORT

8212	$3.00
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Plugs Into Slot of Apple II Mother Board

18 Bit Parallel Output Port (Expandable to 3 Ports)

1 Input Port

15mA Output Current Sink or Source

Can be used for peripheral equipment such as printers, floppy discs, cassettes, paper tapes, etc.

1 free software listing for SWTP PR40 or IBM selectric

PRICE:

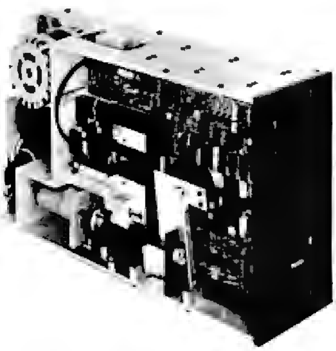
1 Input and 1 Output Port for $49.00

1 Input and 3 Output Ports for $64.00

Dealer Inquiries Invited

Circle 130 on inquiry card.

New 4 Headed Voice Coil Floppy



This 4 headed flexible disk drive stores up to 3.2 M bytes of data in the space required by a standard size floppy drive. The new PerSci Model 299 diskette drive interfaces to microcomputers using the 8080, 6800, or Z-80 processors, as well as minicomputers.

The Model 299 is a dual headed, dual diskette drive, reading and writing both sides of two 8 inch diskettes. Data can be encoded in single or double density in IBM compatible soft sectored formats or expanded hard and soft sectored formats on IBM diskette I, II, IID or equivalent media. The drive will store up to 1 M byte of data in IBM type format, 1.6 M bytes unformatted single density and up to 3.2 M bytes in unformatted double density encoding.

PerSci's voice coil positioning system gives the PerSci drives an average seek time of 33 ms, five to seven times faster than stepper motor positioned drives. The speed and the capacity of the drive are achieved while maintaining industry standard data reliability figures of 1 in 10^9 soft errors and 1 in 10^{12} hard errors.

The Model 299 features electric autoload and can be unloaded by remote, host software control. Optical write protect secures the file.

The PerSci 4 headed drive measures 4.38 by 8.72 by 15.4 inches (11.1 by 22.1 by 39.1 cm) so two drives can be mounted horizontally or four vertically in a 19 inch (48.3 cm) rack.

The price is $1595 from PerSci Inc, 12210 Nebraska Av, W Los Angeles CA 90025.■

Circle 525 on inquiry card.

A Low Cost Minifloppy System

Techtran's low cost minifloppy system, the 950 Microdisk, features over 200 K characters of storage. RS-232 or 20 MA current loop plug compatibility make the 950 a reasonable addition to timesharing and minicomputer or microcomputer based systems. The unit incorporates a Shugart drive and data can be recorded in either file or batch modes with the 950 automatically entering file names into the directory for total random access. Switch selectable data rates to 9600 bps supply fast on line or off line operations. A binary mode is an additional standard feature providing for code transparent applications.

The 950 is list priced at $1395. Contact Techtran Industries Inc, 200 Commerce Dr, Rochester NY 14623, (716) 334-9640.■

Circle 527 on inquiry card.

New Unbundled Floppy Disk Based Computer Systems

Two fully assembled unbundled floppy disk based computer systems have been announced by Ohio Scientific, 1333 S Chillicothe Rd, Aurora OH 44202. Both of these computer systems feature a 6502A processor, 16 K bytes of dynamic programmable memory and an 8 inch floppy disk drive and interface. Both systems have a full 8 slot backplane which will accommodate system expansion. The systems are available as C2-8SK which includes a standard RS-232 serial IO port for use with an external computer terminal and Model C2-8VS which includes a 32 by 64 (81.3 by 162.6 cm) character video display board and a keyboard. Only a video monitor is required to complete the system. Both systems come fully assembled with software and manuals but without cases or power supplies. The C2-8SK with serial interface is $1590 and the C2-8VS with video interface is $2090.■

Circle 528 on inquiry card.

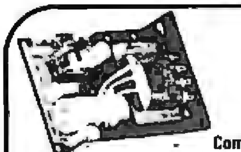
Floppy Disk System for SwTPC 6800

The Southwest Technical Products Corp DMAF1 is a dual drive, single density, double sided 8 inch floppy disk system. The hardware consists of a SS-50 bus (SwTPC 6800) compatible direct memory access controller capable of handling up to four drives, two CalComp 143 M double density rated disk drives, 5 3/4 by 17 1/8 by 20 1/2 inch (14.5 by 43.5 by 52 cm) aluminum chassis, regulated power supply, drive motor control board, cooling fan, diskette and interfacing cables.

The supplied software includes a disk operating system. An 8 K byte BASIC interpreter with disk file capability and string functions is also included with the system. Each diskette holds approximately 600 K bytes of data; with two drives there is over one megabyte of data online.

The system is available in assembled and kit form (the drives are fully assembled). The unit weighs approximately 45 lbs (20.4 kg) and sells for $2095 assembled and $2000 as a kit, plus postage. Contact Southwest Technical Products Corp, 219 W Rhapsody, San Antonio TX 78216.■

Circle 526 on inquiry card.



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PART NO.	RATINGS WATTS	VOLTS	AMPS	PRICE
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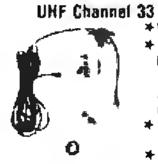
SOLV30-12	30	12	3	59 95
OVP1	over voltage protection for SOLV30-5, 12			9 95

*SOLV15-5, 12 includes OVP installed

SUP 'R' MOD II

UHF Channel 33 TV Interface Unit Kit



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CY3 27	3 2768MHz	HC33	4 95
CY3 57	3 579545MHz	HC33	4.95
CY3A	4.000MHz	HC18	4 95
CY4 91	4 916MHz	HC18	4 95
CY7A	5 000MHz	HC18	4 95
CY5 18	5 185MHz	HC18	4 95
CY5 14	6 144MHz	HC18	4 95
CY6 40	6 400MHz	HC18	4 95
CY5 55	6 5536MHz	HC18	4 95
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CY14A	14 31818MHz	HC18	4 95
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As Featured in August - Popular Electronics

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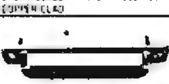
	169P44 062XXXP	4 50	17 00	3 69	3 32
EPOXY	64P44 062WE	4 50	6 50	2 07	1 86
GLASS	84P44 062WE	4 50	8 50	2 56	2 31
	169P44 062WE	4 50	17 00	5 04	4 53
	169P84 062WE	8 50	17 00	9 23	8 26
EPOXY GLASS COPPER CLAD	169P44 062WEC1	4 50	17 00	6 80	6 12



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DB25S	SOCKET	4.95
DB51226-1	Cover for DB25 P or S	1 75

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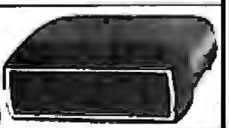
Pre-packaged in strips

INSTRUMENT/ CLOCK CASE

Injection molded unit. Complete with red bezel 4½" x 4" x 1-9/16"



$3.49

MICROPROCESSOR COMPONENTS

P8085	CPU	$29 95
8080A	CPU	10 95
8212	8-Bit Input/Output	4 95
8214	Priority Interrupt Control	7 95
8216	Bi-Directional Bus Driver	4 95
8224	Clock Generator/Driver	5 95
8228	System Controller/Bus Driver	5 95
8251	Prog. Comm. Interface	9 95
8255	Prog. Periph. Interface	10 95
CDP 1802	CPU	$19 95
Z80	CPU	24 95
2650	MPU	26 50
MC6800	MPU	19 95
MC6810API	128 x 8 Static Ram	5 95
MC6820	Periph. Interface Adapter	7 95
MC6821	Periph. Interface Adapter	11 50
MC6830L8	1024 x 8 Bit ROM	14 95
MC6850	Asynchronous Comm Adapter	14 95

RAM'S

1101	256 x 1	Static	$ 1 49
1103	1024 x 1	Dynamic	99
2101	256 x 4	Static	3 95
2102	1024 x 1	Static	1 75
2107 (5280)	4096 x 1	Dynamic	4 95
2111	256 x 4	Static	3 95
2112	256 x 4	Static	3 95
2114	4K x 1	Static 450ns	9 95
2114L	4K x 1	Static 450ns Low Power	10 95
2114-3	4K x 1	Static 300ns	10 95
2114L-3	1K x 4	Static 300ns Low Power	11 95
2489	16 x 4	Static	3 75
8101	256 x 4	Static	3 95
8111	256 x 4	Static	6 95
8599	16 x 4	Static	1 49
21L02	1024 x 1	Static	1 95
74200	256 x 1	Static	6 95
93421	256 x 1	Static	2 95
MM5262	2K x 1	Dynamic	1 00
[illegible]	[illegible]	Dynamic 16 Pin	1 95
[illegible]	[illegible]	Dynamic 16 Pin	11 95
[illegible]	4K	Static	14 95

ROM'S

2513(2140)	Character Generator (upper case)	$ 9 95
2513(3021)	Character Generator (lower case)	9 95
2516	Character Generator	10 95
MM5230N	2048 Bit Read Only Memory	1 95

USER MANUALS

1802M	COP1802 Manual	$ 7 50
Z80M	Z80 Manual	7 50
2650M	2650 Manual	5 00

PROMS

1702A	2048 x 1	Famous	$ 5 95
5203	2048 x 1	Famous	14 95
82S23	32 x 8	Open C	5 00
82S115	4096 x 1	Bipolar	19.95
82S123	32 x 8	Tristate	5 00
74S287	1024 x	Static	7 95
TMS2532	32K	EPROM	99 95
2708	8K	EPROM	10 95
2716 T.I	16K	EPROM	29 95
2716 Intel (2516 T.I.)	16K	EPROM	59 95
6301-1	1024 x 1	Tri-State Bipolar	3 49
6330-1	256 x 1	Open C Bipolar	2.95

SHIFT REGISTERS

MM5013N	1024 BitAccumulator Dynamic	2 95
MM5016H	500/512 Bit Dynamic	89
MM5017N	Dual 500/512 Bit Dynamic	2 95
2504T	1024 Dynamic	3 95
2518	Hex 32 Bit Static	4 95
2519	Hex 40 Bit Static	4 00
2522	Dual 132 Bit Static	2 95
2524	512 Dynamic	99
2525	1024 Dynamic	2 95
2527	Dual 256 Bit Static	2 95
2528	Dual 250 Static	4 00
2529	Dual240 Bit Static	4 00
2532	Quad 80 Bit Static	2 95
2533	1024 Static	2 95
3341	Fifo	6 95
74LS670	4 X 4 Register	1.95

UART'S

AY-5 1013	30K BAUD	$ 5 95

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AY-5 9500	4 95
AY-5-2376	14 95
HD0165	7 95
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ICM7045	$24 95
ICM7205	11 95
ICM7207	7 50
ICM7208	19 95
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NMOS READ ONLY MEMORIES

MCM6571	$11 50
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TV GAME CHIP SET — AY-3-8500 + Crystal + 8 Component Layout **$7.95**

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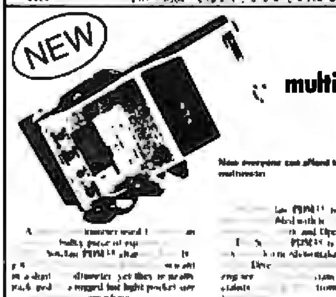
MC1408L8	5 75	95H90	11 95
LD110/111	$25.00/set		
MC4016(74416)	7 50		
4N33	3 95		

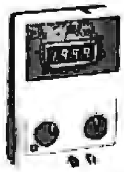
The Sinclair PDM35. A personal digital multimeter foronly $59.95

NEW



PART NO	DESCRIPTION	PRICE
PDM35	Digital Multimeter Completely Assembled	$59.95
PDM-AC	117volt AC Adapter	6.95
PDM DP	Deluxe padded carrying case	6.95

B&K PRECISION — 3½-Digit Portable DMM



* Overload Protected
* .3" high LED Display
* Battery or AC operation
* Auto Zeroing
* 1mV 1V 0.1 ohm resolution
* Overange reading
* 10 meg input impedence
* DC Accuracy 1% typical

Ranges: DC Voltage 0 1000V
AC Voltage 0-1000V
Freq Response 50-400 HZ
DC/AC Current 0-100mA
Resistance 0 10 meg ohm
Size 6 4 x 4 4 x 2

Model 2800 $99.95

Accessories:

AC Adapter BC-28	$9.00
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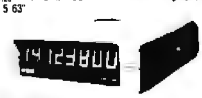
CSC — 100 MHz 8-Digit Counter

* 20 Hz-100 MHz Range
* 6' LED Display
* Crystal-controlled timebase
* Fully Automatic
* Portable — completely self-contained
* Size — 1 75" x 7 38" x 5 63"
* Four power souces, i e batteries, 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply

MAX-100 $134.95



ACCESSORIES FOR MAX 100:

Mobile Charger Eliminator use power from car battery — Model 100 — CLA $3 95

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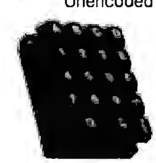
63-Key Unencoded KEYBOARDS Hexadecimal Key Pad Unencoded

This is a 63-key, terminal keyboard newly manufactured by a large computer manufacturer. It is unencoded with SPST keys, unattached to any kind of PC board. A very solid molded plastic 13 x 4" base suits most application. IN STOCK **$29.95/each**



19-key pad includes 1-10 keys, ABCDEF and 2 optional keys and a shift key **$10.95/each**

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Spec Sheets — 25¢
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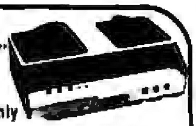
The Incredible "Pennywhistle 103"



$139.95 Kit Only

The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone hamming and communications for the deaf. In addition it is free of critical adjustments and is built with non-precision readily available parts.

Data Transmission Method	Frequency-Shift Keying, full-duplex (half-duplex selectable)
Maximum Data Rate	300 Baud.
Data Format	AsynchronousSerial (return to mark level required between each character)
Receive Channel Frequencies	2025 Hz for space; 2225 Hz for mark
Transmit Channel Frequencies	Switch selectable Low (normal) 1070 space 1270 mark; High 2025 space, 2225 mark
Receive Sensitivity	-46 dbm accoustically coupled
Transmit Level	-15 dbm nominal. Adjustable from -6 dbm to -20 dbm.
Receive Frequency Tolerance	Frequency reference automatically adjusts to allow for operation between 1800Hz and 2400 Hz
Digital Data Interface	EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar)
Power Requirements	120 VAC, single phase, 10 Watts
Physical	All components mount on a single 5 by 9" printed circuit board All components included

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align.

The Original the 3rd Hand

$9.95 each

* Leaves two hands free for working
* Clamps on edge of bench, table or work bench
* Position board on angle or flat position for soldering or clipping
* Sturdy, aluminum construction for hobbyist, manufacturer or school rooms

DIGITAL STOPWATCH

* Bright 6 Digit LED Display
* Times to 59 minutes 59.59 seconds
* Crystal Controlled Time Base
* Three Stopwatches in One: Times Single Event — Split & Taylor
* Size 4 5 x 2 15 x 90 (4½ ounces)
* Uses 3 Penlite Cells

Kit — $39.95
Assembled — $49.95
Heavy Duty Carry Case $5 95

Stop Watch Chip Only (7205) $19.95

3½ DIGIT DPM KIT

* New Bipolar Unit
* Auto Zeroing
* 5" LED
* Auto Polarity
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* Single IC Unit

Model KB500 DPM Kit	**$49.00**
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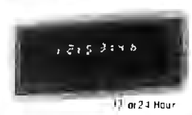
JE700 CLOCK



The JE700 is a low cost digital clock ... MAN72 high brightness readout and the MM5314 clock chip

12 or 24 Hour

115 VAC

KIT ONLY **$16.95**

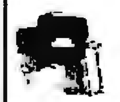
JE803 PROBE

The Logic Probe is a unit which is for the most part indespensible in trouble shooting logic families TTL DTL RTL CMOS It derives the power it needs to operate directly off of the circuit under test drawing a scant 10 mA max It uses a MAN3 readout to indicate any of the following states by these symbols (HI 1 (LOW) 0 (PULSE) P The Probe can detect high frequency pulses to 45 MHz It can't be used at MOS levels or circuit damage will result

$9.95 Per Kit

printed circuit board

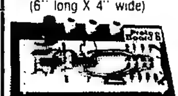
T²L 5V 1A Supply



This is a standard TTL power supply using the well known LM309K regulator IC to provide a solid 1 AMP of current at 5 volts We try to make things easy for you by providing everything you need in one package including the hardware for only **JE225 $9.95 Per Kit**

CSC PROTO BOARDS

PROTO BOARD 6
$15.95
(6" long X 4" wide)



PB100 - 4.5" x 6"	$ 19 95
PB101 - 5.8" x 4.5"	29 95
PB102 - 7" x 4.5"	29 95
PB103 - 9" x 6"	44.95
PB104 - 9.5" x 8"	54 95
PB203 - 9.75 x 6½ x 2¾	75 00
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14 PIN	$4 50
16 PIN	4 75
24 PIN	8 50
40 PIN	13 75

Circle 200 on inquiry card.

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SN7412N	.25	SN7491N	.59	SN74175N	.79
SN7413N	.40	SN7492N	.43	SN74176N	.79
SN7414N	.70	SN7493N	.43	SN74177N	.79
SN7416N	.25	SN7494N	.65	SN74179N	1.95
SN7417N	.25	SN7495N	.65	SN74180N	.79
SN7420N	.20	SN7496N	.65	SN74181N	1.95
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SN7423N	.25	SN74107N	.35	SN74185N	1.95
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SN7427N	.25	SN74121N	.35	SN74190N	1.25
SN7429N	.39	SN74122N	.39	SN74191N	1.25
SN7430N	.20	SN74123N	.49	SN74192N	.79
SN7432N	.25	SN74125N	.49	SN74193N	.79
SN7437N	.25	SN74126N	.49	SN74194N	.69
SN7438N	.25	SN74132N	.75	SN74195N	.69
SN7439N	.25	SN74136N	.75	SN74196N	.89
SN7440N	.20	SN74141N	.79	SN74197N	.89
SN7441N	.89	SN74142N	2.95	SN74198N	1.49
SN7442N	.49	SN74143N	2.95	SN74199N	1.49
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SN7444N	.75	SN74145N	.79	SN74251N	1.79
SN7445N	.75	SN74147N	1.95	SN74279N	.79
SN7446N	.69	SN74148N	1.29	SN74283N	2.25
SN7447N	.59	SN74150N	.89	SN74284N	3.95
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CD4006	1.19	CD4029	1.19	CD4076	1.39
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CD4023	.23	CD4059	9.95	CD4511	1.29
CD4024	.79	CD4060	1.49	CD4515	2.95
CD4025	.23	CD4066	.79	CD4518	1.29
CD4026	1.25	CD4068	.39	CD4520	1.29
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74C04	.75	74C89	5.49	74C173	2.60
74C08	.75	74C90	3.00	74C192	3.49
74C10	.65	74C93	3.00	74C193	2.75
74C14	3.00	74C95	3.00	74C195	2.75
74C20	.65	74C107	1.25	74C922	9.95
74C30	.65	74C151	2.90	74C923	8.95
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LM308H	1.00	LM340T-24	1.25	LM748N	.39
LM308CN	1.00	LM350N	1.00	LM1303N	.90
LM309H	1.10	LM351CN	.65	LM1304N	1.19
LM309K	1.25	LM370N	1.15	LM1305N	1.40
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LM320T-15	1.25	NE561B	5.00	MC5558V	1.00
LM320T-18	1.25	NE562B	5.00	LM7525N	.90
LM320T-24	1.25	NE565H	1.75	LM7534N	.75
LM323K-5	5.95	NE565N	1.25	8038B	4.95
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LM339N	.99	NE567H	1.25	75451CN	.39
LM340K-5	1.35	NE567V	.99	75452CN	.39
LM340K-6	1.35	NE570N	10.50	75453CN	.39
LM340K-8	1.35	LM703CN/H	.45	75454CN	.39
LM340K-12	1.35	LM709H	.29	75491CN	.79
LM340K-15	1.35	LM709N	.29	75492CN	.89
LM340K-18	1.35	LM710N	.79	75494CN	.89
LM340K-24	1.35	LM711N	.39	RC4151	5.95
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LM340T-6	1.25	LM723N	.55	RC4195	4.49

74LS00 TTL

74LS00	.23			74LS139	.69
74LS01	.23			74LS151	.69
74LS02	.23	74LS51	.23	74LS155	.69
74LS03	.23	74LS54	.23	74LS157	.69
74LS04	.29	74LS55	.23	74LS160	.89
74LS05	.29	74LS73	.35	74LS161	.89
74LS08	.23	74LS74	.35	74LS162	.89
74LS09	.29	74LS75	.49	74LS163	.89
74LS10	.23	74LS76	.35	74LS164	.99
74LS13	.49	74LS83	.75	74LS175	.79
74LS14	.99	74LS85	.99	74LS181	2.49
74LS15	.29	74LS86	.35	74LS190	.89
74LS20	.23	74LS90	.49	74LS191	.89
74LS21	.29	74LS92	.59	74LS192	.89
74LS22	.29	74LS93	.59	74LS193	.89
74LS26	.29	74LS95	.79	74LS194	.89
74LS27	.29	74LS96	.89	74LS195	.89
74LS28	.29	74LS107	.35	74LS253	.79
74LS30	.23	74LS109	.35	74LS257	.69
74LS32	.29	74LS112	.35	74LS260	.55
74LS37	.35	74LS123	.99	74LS279	.59
74LS40	.29	74LS132	.79	74LS367	.59
74LS42	.69	74LS136	.39	74LS368	.59
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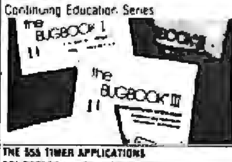

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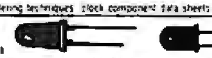
Starts at basic structure of CMOS devices through integration into MSI.

COMPLETE MANUAL FOR DIGITAL CLOCKS by John Watts and John Brooks
Familiarizes technician or hobbyist with basic theories behind digital clocks. Includes trouble shooting guides, basic characteristics of clocks, soldering techniques, clock component data sheets and construction tips. — $3.95

DISCRETE LEDS



.125" dia									.190" dia		
XC209	Red	5/$1							XC111	Red	5/$1
XC209	Green	4/$1							XC111	Green	4/$1
XC209	Yellow	4/$1				.200" dia.			XC111	Yellow	4/$1
.200" dia			.185" dia						.085" dia.		
						XC556	Red	5/$1	MV50	Red	6/$1
XC22	Red	5/$1	XC526	Red	5/$1	XC556	Red	100/$8	.170" dia.		
XC22	Green	4/$1	XC526	Red	100/$8	XC556	Green	4/$1	MV10	Red	4/$1
XC22	Yellow	4/$1	XC526	Green	4/$1	XC556	Yellow	4/$1	[illegible]		
SSL-22	RT	4/$1	XC526	Yellow	4/$1	XC556	Orange	4/$1	[illegible]		
			XC526	Clear	4/$1	XC556	Clear	7/$1			$1.00

DISPLAY LEDS

TYPE	POLARITY	HT	PRICE	TYPE	POLARITY	HT	PRICE
MAN 1	Common Anode-red	270	2.95	MAN 6680	Common Cathode-orange	560	.99
MAN 2	5 x 7 Dot Matrix-red	300	4.95	MAN 6710	Common Anode-red-D D	560	.99
MAN 3	Common Cathode-red	125	.25	MAN 6730	Common Anode-red ±1	560	.99
MAN 4	Common Cathode-red	187	1.95	MAN 6740	Common Cathode-red-D D	560	.99
MAN 52	Common Anode-green	300	1.25	MAN 6750	Common Cathode-red ±1	560	.99
MAN 71	Common Anode-red	300	1.25	MAN 6760	Common Anode-red	560	.99
MAN 72	Common Anode-red	300	.99	MAN 6780	Common Cathode-red	560	.99
MAN 74	Common Cathode-red	300	1.25	DL701	Common Anode-red ±1	300	.99
MAN 81	Common Anode-yellow	300	.99	DL702	Common Cathode-red	300	1.25
MAN 82	Common Anode-yellow	300	.99	DL704	Common Cathode-red	300	.99
MAN 84	Common Cathode-yellow	300	.99	DL707	Common Anode-red	300	.99
MAN 3620	Common Anode-orange	300	.99	DL741	Common Anode-red	600	1.25
MAN 3630	Common Anode-orange ±1	300	.99	DL746	Common Anode-red ±1	630	1.49
MAN 3640	Common Cathode-orange	300	.99	DL747	Common Anode-red	600	1.49
MAN 4610	Common Anode-orange	300	.99	DL749	Common Cathode-red ±1	630	1.49
MAN 4640	Common Cathode-orange	400	.99	DL750	Common Cathode-red	600	1.49
MAN 4710	Common Anode-red ±1	400	.99	DL338	Common Cathode-red	110	.35
MAN 4730	Common Anode-red	400	.99	FND70	Common Cathode	250	.69
MAN 4740	Common Cathode-red	400	.99	FND359	Common Anode	350	.75
MAN 4810	Common Anode-yellow	400	.99	FND503	Common Cathode (FND500)	500	.99
MAN 6610	Common Anode-orange-D D	560	.99	FND507	Common Anode (FND510)	500	.99
MAN 6630	Common Anode-orange	560	.99	5082-7300	4 x 7 Sgl Digit-RHDP	600	19.95
MAN 6640	Common Cathode-orange-D D	560	.99	5082-7302	4 x 7 Sgl Digit-LHDP	600	19.95
MAN 6650	Common Cathode-orange ±1	560	.99	5082-7304	Overrange character (±1)	600	15.00
MAN 6660	Common Anode-orange	560	.99	5082-7340	4 x 7 Sgl Digit-Hexadecimal	600	22.50

RCA LINEAR

CA3013	2.15	CA3082	2.00
CA3023	2.56	CA3083	1.60
CA3035	2.48	CA3086	.85
CA3039	1.35	CA3089	3.75
CA3046	1.30	CA3130	1.39
CA3059	3.25	CA3140	1.25
CA3060	3.25	CA3160	1.25
CA3080	.85	CA3401	.49
CA3081	2.00	CA3600	3.50

CALCULATOR CHIPS AND DRIVER

[illegible]	$5.00
MM5725	2.95
MM5736	1.95
MM5738	2.95
DM8864	2.00
DM8865	1.00
DM8887	.75
DM8889	.75
5030	.95

CLOCK CHIPS

MM5309	$8.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
[illegible]	6.95
[illegible]	9.95
[illegible]	[illegible]
[illegible]	4.95
[illegible]	5.95

9374 7-segment LED driver common Anode LEDs $ .99

IC SOLDERTAIL — LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin LP	$.17	.16	.15	22 pin LP	$.37	.36	.35
14 pin LP	.20	.19	.18	24 pin LP	.38	.37	.36
16 pin LP	.22	.21	.20	28 pin LP	.45	.44	.43
18 pin LP	.29	.28	.27	36 pin LP	.60	.59	.58
20 pin LP	.34	.32	.30	40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100		1-24	25-49	50-100
14 pin ST	$.27	.25	.24	28 pin ST	$.99	.90	.81
16 pin ST	.30	.27	.25	36 pin ST	1.39	1.26	1.15
18 pin ST	.35	.32	.30	40 pin ST	1.59	1.45	1.30
24 pin ST	.49	.45	.42				

SOLDERTAIL STANDARD (GOLD)

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin SG	$.30	.27	.24	24 pin SG	$.70	.63	.57
14 pin SG	.35	.32	.29	28 pin SG	1.10	1.00	.90
16 pin SG	.38	.35	.32	36 pin SG	1.75	1.40	1.26
18 pin SG	.52	.47	.43	40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin WW	$.40	.38	.35	22 pin WW	$.95	.85	.75
10 pin WW	.45	.41	.37	24 pin WW	1.05	.95	.85
14 pin WW	.39	.38	.37	28 pin WW	1.40	1.25	1.10
16 pin WW	.43	.42	.41	36 pin WW	1.59	1.45	1.30
18 pin WW	.75	.68	.62	40 pin WW	1.75	1.55	1.40

50 PCS. RESISTOR ASSORTMENTS $1.75 PER ASST.

		10 OHM	12 OHM	15 OHM	18 OHM	22 OHM		
ASST. 1	5 ea	27 OHM	33 OHM	39 OHM	47 OHM	56 OHM	1/4 WATT 5%	50 PCS
		68 OHM	82 OHM	100 OHM	120 OHM	150 OHM		
ASST. 2	5 ea	180 OHM	220 OHM	270 OHM	330 OHM	390 OHM	1/4 WATT 5%	50 PCS
		470 OHM	560 OHM	680 OHM	820 OHM	1K		
ASST. 3	5 ea	1.2K	1.5K	1.8K	2.2K	2.7K	1/4 WATT 5%	50 PCS
		3.3K	3.9K	4.7K	5.6K	6.8K		
ASST. 4	5 ea	8.2K	10K	12K	15K	18K	1/4 WATT 5%	50 PCS
		22K	27K	33K	39K	47K		
ASST. 5	5 ea	56K	68K	82K	100K	120K	1/4 WATT 5%	50 PCS
		150K	180K	220K	270K	330K		
ASST. 6	5 ea	390K	470K	560K	680K	820K	1/4 WATT 5%	50 PCS
		1M	1.2M	1.5M	1.8M	2.2M		
ASST. 7	5 ea	2.7M	3.3M	3.9M	4.7M	5.6M	1/4 WATT 5%	50 PCS.

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) **$9.95 ea.**

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WIRE WRAP WIRE — 30 AWG
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- Cuts wire to desired length
- Strips 1" of insulation **Specify** — Blue-Yellow-White-Red

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XR2206KA $14.95
Function Generator Kit (includes chip, P.C. Board and instructions)

EXAR

XR2206KB $19.95
Function Generator Kit (includes 19 components, P.C. Board and instructions)

XR-L555 $1.50
Micro-Power version of the popular 555 Timer and directly interchangeable. Dissipates 1/15th the power and operates down to 2.7 volts. Perfect for battery operation and CMOS circuits.

XR2242CP $1.50
Precision timing circuit for generating timing pulses in minutes, hours and days or up to 1 year by using two. Reduces cost of time delaycircuits. Basic 555 Timer with built-in 8-bit Counter.

XR205	$8.40			XR2556	$3.20
XR210	4.40	XR1489	1.39	XR2567	2.99
XR215	4.40	XR1800	3.20	XR3403	1.25
XR320	1.55	XR2206	4.40	XR4136	1.35
XR555	.39	XR2207	3.85	XR4151	2.85
XR556	.99	XR2208	5.20	XR4194	1.45
XR567CP	.99	XR2209	1.75	XR4202	3.60
XR567CT	1.25	XR2211	5.25	XR4212	2.05
XR1310P	1.30	XR2212	4.15	XR4558	.75
XR1468CN	3.85	XR2242	3.45	XR4739	1.15
XR1488	1.39	XR2264	4.25	XR4741	1.47

ZENERS — DIODES — RECTIFIERS

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
1N746	3.3	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N751A	5.1	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N3600	50	200m	6/1.00
1N754	6.8	400m	4/1.00	1N4148	75	10m	15/1.00
1N959	8.2	400m	4/1.00	1N4154	35	10m	12/1.00
1N965B	15	400m	4/1.00	1N4305	75	25m	20/1.00
1N5232	5.6	500m	.28	1N4734	5.6	1w	.28
1N5234	6.2	500m	.28	1N4735	6.2	1w	.28
1N5235	6.8	500m	.28	1N4736	6.8	1w	.28
1N5236	7.5	500m	.28	1N4738	8.2	1w	.28
1N456	25	40m	6/1.00	1N4742	12	1w	.28
1N458	150	7m	6/1.00	1N4744	15	1w	.28
1N485A	180	10m	5/1.00	1N1183	50 PIV	35 AMP	1.60
1N4001	50 PIV	1 AMP	12/1.00	1N1184	100 PIV	35 AMP	1.70
1N4002	100 PIV	1 AMP	12/1.00	1N1185	150 PIV	35 AMP	1.70
1N4003	200 PIV	1 AMP	12/1.00	1N1186	200 PIV	35 AMP	1.80
1N4004	400 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR (2N1849)	$1.95
C38M	35A @ 600V	SCR	1.95
2N2328	1.6A @ 300V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC	1.95

TRANSISTORS

C106B1	.50			2N3904	4/1.00
MPSA05	.30	2N3055	.89	2N3905	4/1.00
MPSA06	5/1.00	MJE3055	1.00	2N3906	4/1.00
TIS97	6/1.00	2N3392	5/1.00	2N4013	3/1.00
TIS98	6/1.00	2N3398	5/1.00	2N4123	6/1.00
TIS133	5/1.00	PN3567	3/1.00	PN4249	4/1.00
TIS135	5/1.00	PN3568	4/1.00	PN4250	4/1.00
40409	1.75	PN3569	4/1.00	2N4400	4/1.00
40410	1.75	MPS3638A	5/1.00	2N4401	4/1.00
40673	1.75	MPS3702	5/1.00	2N4402	4/1.00
2N918	4/1.00	2N3704	5/1.00	2N4403	4/1.00
2N2219A	3/1.00	MPS3704	5/1.00	2N4409	5/1.00
2N2221A	4/1.00	2N3705	5/1.00	2N5086	4/1.00
2N2222A	5/1.00	MPS3705	5/1.00	2N5087	4/1.00
2N2369	5/1.00	2N3706	5/1.00	2N5088	4/1.00
2N2369A	4/1.00	MPS3706	5/1.00	2N5089	4/1.00
MPS2369	5/1.00	2N3707	5/1.00	2N5129	5/1.00
2N2484	4/1.00	2N3711	5/1.00	PN5134	5/1.00
2N2906	4/1.00	2N3724A	.65	PN5138	5/1.00
2N2907	5/1.00	2N3725A	1.00	2N5139	5/1.00
2N2925	5/1.00	2N3772	2.25	2N5210	5/1.00
MJE2955	1.25	2N3823	1.00	2N5449	3/1.00
2N3053	2/1.00	2N3903	4/1.00	2N5951	3/1.00

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-99	100-		1-9	10-99	100
10 pf	.05	.04	.03	.001µF	.05	.04	.035
22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470pf	.05	.04	.035	.1µF	.12	.09	.075

100 VOLT MYLAR FILM CAPACITORS

.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+20% DIPPED TANTALUMS (SOLID) CAPACITORS

.1/35V	.28	.23	.17	1.5/35V	.30	.26	.21
.15/35V	.28	.23	.17	2.2/25V	.31	.27	.22
.22/35V	.28	.23	.17	3.3/25V	.31	.27	.22
.33/35V	.28	.23	.17	4.7/25V	.32	.28	.23
.47/35V	.28	.23	.17	6.8/25V	.36	.31	.25
.68/35V	.28	.23	.17	10/25V	.40	.35	.29
1.0/35V	.28	.23	.17	15/25V	.63	.50	.40

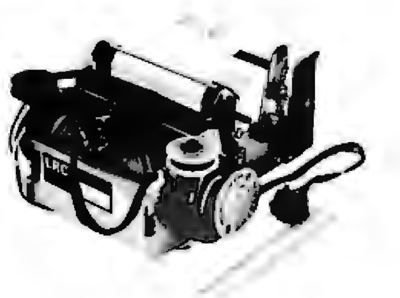
MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead				Radial Lead			
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.14	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

Circle 200 on inquiry card.

PERIPHERALS

LRC Improved Series of Matrix Impact Printers

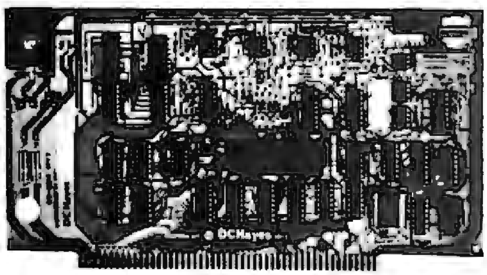


LRC Inc, Technical Research Park, Riverton WY 82501, has announced the availability of improved versions of its 7000 series matrix impact printers. Improvements include a new drive cam for the print head which is said to result in a uniform character width at the extreme ends of the print line as well as a decreased failure rate.

Available in ticket printer models as well as in roll paper models, all units have multiple copy capability with the print line capacity of 40 columns at 12 characters to the inch. Ticket printer versions are available in 22 column models. 1 line or 5 line document validation is optional on rollpaper models. Prices range from $66.50 to $282 depending upon model, options and quantity.■

Circle 564 on inquiry card.

Data Communications Adapter



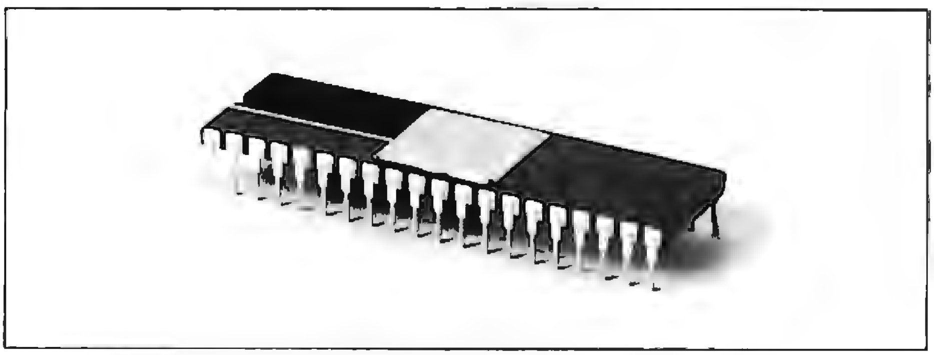
This 80-103A Data Communications Adapter has been developed to function as a S-100 bus compatible serial interface incorporating a fully programmable modem and Telco interface. These functions are usually accomplished by the use of two separate modules: a serial IO board and an external modem. The 80-103A combines these features on a single board.

A S-100 computer and a Telco 1001D data access arrangement (DAA) are all that is needed to control the adapter and interface to the telephone network.

The price of the 80-103A is $279.95 from DC Hayes Associates Inc, POB 9884, Atlanta GA 30319.■

Circle 565 on inquiry card.

New Programmable UART Interface



The COM6402, a programmable universal asynchronous transceiver (UART) with high clock frequencies, low power requirements and independent programming capabilities, has been introduced by Standard Microsystems Corp. Compatible with industry standard UARTs, the COM6402 is a pin for pin replacement for Harris HD-6402 and Intersil IM6402.

CMOS/LSI technology permits operator clock frequencies up to 3.2 MHz (200 k bps) while requiring only 10 mW of power. Duplex mode, bps rate, data word length, parity mode and number of stop bits are independently programmable through the use of external controls. There may be five, six, seven and eight data bits, odd, even or no parity, and one or two stop bits or 1.5 stop bits when utilizing a 5 bit code.

COM6402 is TTL compatible and requires only a single ±5 V power supply. It is fully double buffered to eliminate the need for external timing and provides start bit verification to decrease error rate. Three state outputs are bus structure oriented.

For further information, contact Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge NY 11787.■

Circle 568 on inquiry card.

Pertec Announces Double Head, Double Density Microfloppy

The new FD250 Microfloppy disk drive stores up to 437.5 K bytes without operator intervention. Double density, hard or soft sectoring, and write protect are all standard features. The unit can write and read data on both sides of a diskette.

Measuring 3.25 inches by 5.75 by 8 inches (8.26 by 14.61 by 20.32 cm), the FD250 weighs 3.2 lbs (1.45 kg). Its seek time is 25 ms track-to-track, with head settling time of 10 ms (last track addressed) and a maximum head loading time of 35 ms.

The recommended recording mode is frequency modulation (FM) on single density and modified frequency modulation (MFM) on double density. Recording density (inside track) is 2768 to 5536 bpi, with 1750 K bits per disk (single density and unformatted) or 3500 K bits per disk (double density and unformatted).

The FD250 is priced at $325 per unit for quantities of 100. For further information contact Pertec Computer Corp, Pertec Division, 9600 Irondale Av, Chatsworth CA 91311.■

Circle 566 on inquiry card.

Put Your PET on the Bus

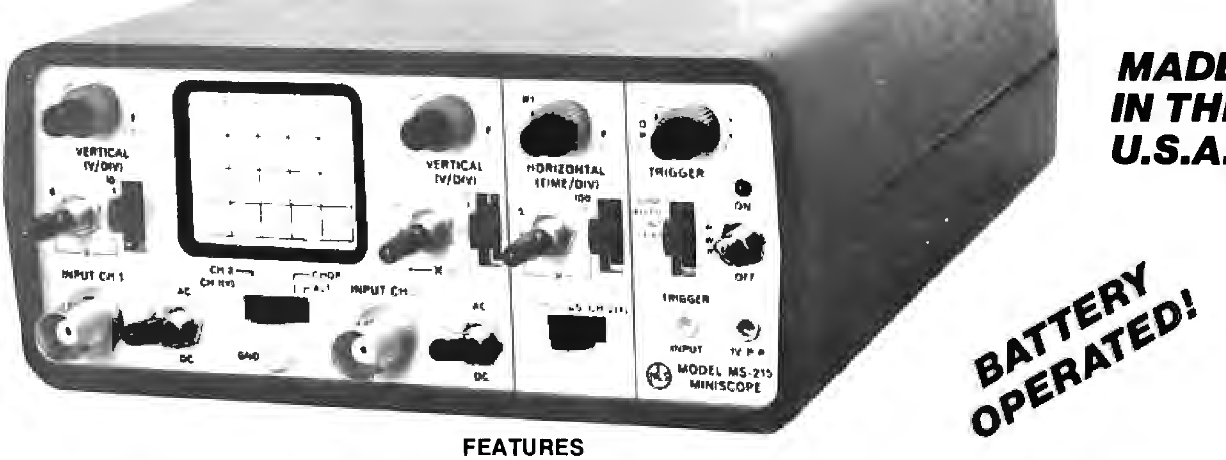
The PET-488 cable assembly makes the PET computer plug-compatible with any device using the IEEE 488 bus. The PET computer can become the controller for a variety of electronic test equipment and computer peripherals. The cable assembly plugs directly into the edge connector on back of the PET computer and has an IEEE-488 compatible connector on the other end. The cable meets all IEEE-488 specifications for shielding and crosstalk and is 18 inches (45 cm) long. The price of the PET-488 cable assembly is $30 (California residents add 6% sales tax). Contact Pickles & Trout, POB 1206, Goleta CA 93017.■

Circle 567 on inquiry card.

DUAL TRACE 15 MEGAHERTZ PORTABLE MINISCOPE

$435.00

NLS



MADE IN THE U.S.A.!

BATTERY OPERATED!

FEATURES

- Dual Trace- 2 channel: separate, chopped or alternate modes.
- 15 megahertz bandwidth.
- External and internal trigger.
- Time Base - 0.1 microseconds to 0.5 Sec/div - 21 settings.
- Battery or line operation.
- Automatic and line sync modes.
- Power consumption less than 15W.
- Verticle Gain - 0.01 to 50 volts/div —12 settings.
- Weight is only 3 pounds.

From the originator of the Digital Voltmeter, Non-Linear Systems comes the MS-215 Miniscope. It is a fine electronic instrument with a great deal of measuring capability and excellent accuracy. Its design is modern, utilizing the latest in low-powered integrated circuits, and it is packaged into the smallest practical size. The instrument fits into many briefcases and tool boxes with room to spare.

Operating characteristics have been chosen so that the MS-215 will make all of the measurements needed in servicing most electronic equipment. It is field-portable so its use is not restricted to the bench.

SPECIFICATIONS:

Vertical

Mode: CH1, CH2, CH1 & CH2 (Chopped) & CH1 & CH2 (Alt.)
The Following Specifications apply to each channel

Y Axis

Verticle Input: 10mV/div to 50V in 12 Calibrated ranges, as follows:
x1-10mV/div to 10V/div in four ranges, each continuously variable.
x2-20mV/div to 20mV/div in four ranges, each continuously variable.
x5-50mV/div to 50mV/div in four ranges, each continuously vairiable.
Accuracy is 3%

Input Impedence: 1M ohm shunted by 50 pF.

Bandwidth: DC/DC to 15 Mhz ±6 db(DC to 8 Mhz ±3 db). AC, same as DC down to 3Hz.

Rise Time: Approximately 23 nS @ 1 division deflection.

Input Voltage: 250 maximum (DC and Peak AC).

Horizontal

Mode: Internal Time Base or External Horizontal, switch selectable. In the XY mode, vertical input is through CH1 and horizontal input is through CH2

Bandwidth: DC to 200 KHz (±3 db).

Coupling: AC, DC or ground, switch selectable. Low frequency point on AC is 3 Hz.

Input Impedence: 1Meg ohm shunted by 50 pF.

Deflection Factor: 10mV/div to 50V/div in 12 calibrated ranges. The ranges can be calibrated with the CH2 gain control

Input Voltage: 250V maximum (DC and Peak AC)

Time Base: **0.1uS/div to 0.5 Sec/div in 21' calibrated ranges, as follows:**
x1, uS-0.1 uS/div to 100 uS/div. x2, uS-0.2uS/div to 200 uS/div.
x5, uS-0.5uS/div to 500 uS/div. x1, mS-0.1 mS/divto 100 mS/div
x2, mS-0.2mS/div to 200 mS/div. x5, mS-0.5mS/div to 500 mS/div.
all in four ranges, each continuously variable. (Range incrementsar .1, 1, 10, 100.) With vernier in full clockwise position, calibrated time measurements are possible. Accuracy is 3%.

Triggering

Internal: Sweep triggered from internal trigger source (In the dual trace modes, the internal trigger source is CH1).

Automatic: Trigger source is internal calibrater frequency To be used if there is no other trigger source available to synchronize the sweep.

Line Trigger is derived from line frequency when using the battery charger

External: Controls function as for internal triggering (1 Megohm input impedance).

Slope: Selects sync to positive- or negative- going waveform.

Coupling: AC

Sensitivity: Less than 1 div for internal trigger and less than 1 volt for external trigger.

Level: Trigger Level control permits continuous adjustment of trigger point in all modes except Auto.

Internal Calibrater: A square-wave signal of 1 volt p-p ± 5% is provided. Frequency is approximately 1KHz.

Display

Graticule: 4x5 div, each division is 0.25 inch. Viewing area 1.1"Hx1.35"W

CRT: Bluish-white phospher, medium peristence. CRT uses low power filament for low battery drain. Instant onl

Power

On-Board Batteries: Three sealed, rechargeable lead acid "D" Cells

Operating Time: Typically 4 hours.

Charging Time Scope Operating: Will run indefinitely but notreach full charge.

Non-operating: Sixteen hours.

External Power: Battery charger 115 vac (220 vac on request). 50-400Hz, less than 15 watts.

Dimensions: 3.1"Hx6.4"Wx8.0"D.

Weight: Three pounds.

Environment

Operating Temperature: 0° to 40°C

Shock and Vibration: Designed to with stand normal shock and vibration encountered in commercial shipping and handling.

Accessories

Furnished: Tilt stand, battery charger, 2 input cables, and 3 miniature banana plugs.

Optional: Leather carrying case and probes

Warrranty: One year parts and labor. Made in the U.S.A.

MS-215 with Rechargeable Batteries and Charger
$395.00

Leather Carrying Case

The leather case has 2 separate compartments. One to hold the scope, the other to hold the charger, probe, shoulder strap, etc. The case can be worn on the belt, or over the neck.

The snaps used on the case are "one way", thus accidental striking of the case against an object will not undo the snaps or let it be pulled off your belt.

41-140 **$45.00**

Probes

10 to 1 probe with 10 megohm input.

Probe uses spring hook tip for sure connection. Compensation network is located at the connector rather than at the probe, so as to keep size and weight to a minimum

41-141 **$27.00**

Deluxe Combination Probe

Switchable 10to1/1 to1 probe with an assortment of probe tips to suit any situation.

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Circle 306 on inquiry card.

New 1978-79 General Semiconductor Industries Product Catalog

The new 1978-79 General Semiconductor Industries Product Catalog contains a complete listing of the company's entire line of Zener diodes, temperature compensated diodes, NPN switching transistors, TransZorb silicon transient voltage suppressors, and C^2R high speed and high voltage switching transistors.

This 238 page publication contains detailed device characterization and applications information for many of the units listed. The catalog lists the devices numerically within specific categories. General Semiconductor's environmental facilities and equipment is also listed. Contact General Semiconductor Industries Inc, 2001 W 10th Pl, Tempe AZ 85281.■

Circle 622 on inquiry card.

Surge, Hash and Transient Protection

A new flyer from Electronic Specialists, POB 122, Natick MA 01760, discusses AC power line surges and hash. Suggestions are offered for protection from microprocessor damage or malfunction. Included are protection against lightning and error-producing power line hash. When writing for this free flyer, specify flyer AEP-7. Send stamped, self-addressed envelope.■

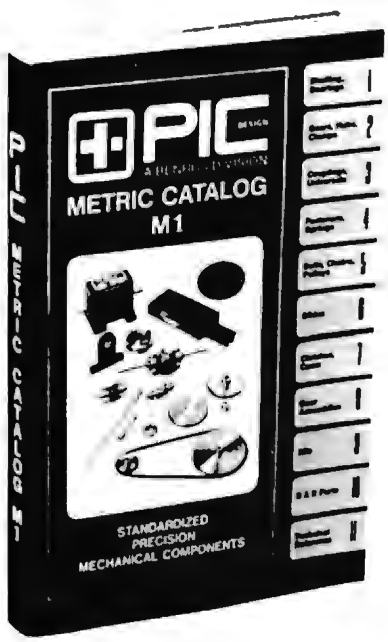
Circle 623 on inquiry card.

New Electronic Test Equipment Catalog

This new 76 page 1978 catalog features electronic test equipment from major manufacturers including B & K Precision, Continental Specialties, Hickok and Simpson. North American Electronics specializes in direct catalog marketing of name brand electronic test equipment. The free catalog can be obtained by writing to Dept AA 78, North American Electronics, 1468 W 25th St, Cleveland OH 44113.■

Circle 624 on inquiry card.

New Metric Components Catalog



A compilation of metric system standardized precision mechanical components and assemblies has been produced by PIC Design, POB 335, Benrus Center, Ridgefield CT 06877.

The 208 page edition contains over 25,000 components covering 24 different product categories. Also included in the catalog are working prints, technical reference data tables, gear data, metric terms and formulas, and many other design and production aids.■

Circle 625 on inquiry card.

Radio Shack Microcomputer Catalog

Now available from Radio Shack is the 8 page *TRS-80 Microcomputer System Products* catalog. The catalog features Radio Shack's $599 TRS-80 microcomputer system and provides information on upgraded systems, peripherals and ready to use software developed specifically for the TRS-80. The basic TRS-80 system offers Level I BASIC with 4 K bytes of read only memory and 4 K bytes of programmable memory.

Also included in the catalog is information on expanding your existing TRS-80 system with details of Level II BASIC, and an order worksheet that helps customers to custom tailor a TRS-80 system to their particular needs. The Radio Shack *TRS-80 Microcomputer System Products* catalog is available free on request from Radio Shack stores and dealers.■

Circle 626 on inquiry card.

Free Book and Educational Products Catalog

Sybex's 12 page book and educational products catalog contains a broad range of books (including foreign versions), self-study courses and video cassettes for TV systems for the personal computer user. For a free copy of this catalog, write Sybex, 2161 Shattuck Av, Berkeley CA 94704.■

Circle 621 on inquiry card.

1977 Periodical Guide for Computerists

The January thru December *1977 Periodical Guide for Computerists* indexes over 2200 articles from 25 hobby and professional electronic and computer publications. Articles, editorials, book reviews and letters from readers which have relevance to the personal computing field are indexed by subject under 100 categories. An author index is included which lists the subjects that each author wrote about. The more than 60 page book is available postpaid for $5 from E Berg Publications, 1360 SW 199th Ct, Aloha OR 97005.■

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Circle 356 on inquiry card.

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- BCD Code

These terminals are from a large airline reservation system. They are heavy duty and were under continuous maintenance. The units have been in storage. We make every effort to ensure that all essential parts are included. Most work when plugged in. No warranties are given or implied.

Selectric Controller

The 3S-01 is a complete controller for the IBM Model 731 I/O typewriter for both input and output operations. With this controller the 731 becomes a versatile ASCII printer with the world famous Selectric quality and an alphanumeric ASCII-encoded keyboard with the wonderful Selectric feel. An eightbit parallel input/output port (bidirectional or separate) is all that is necessary to add the KING of the hardcopy terminals to your system. Serial RS-232C is also available for connection to a serial communications port or modem.

Power supply requirements are 5VDC at .75A and 48VDC at 1A for the basic parallel controller. Additional power needed for the serial unit is ± 12VDC.

PRICE $249.95
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Surplus power supply for above $30.00

Print only interface unit
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Complete Terminal Unit

This unit consists of:

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3. Power supply (used)
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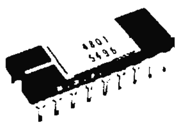
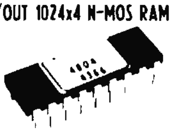
4801 STATIC, TTL IN OUT 4096x1 N-MOS RAM



GENERAL DESCRIPTION
Part Number 4801 is a 4K semiconductor random access memory organized as 4096 1-bit words. It is fully static and needs no clock or refresh pulses. It requires a single +5 volt power supply and is fully TTL compatible on input and output lines. The 4801 is packaged in a convenient 18 pin dual-in-line package.

FEATURES
- Single +5V Power Supply
- 4Kx1 Organization
- Replaces 4 1024x1 Static RAMs
- Completely Static—No Clocks or Refresh
- 18 Pin Package
- Access/Cycle Times 600 nsec max
- 250 mw Typical Operating Power
- Separate Data In and Data Out
- TTL Compatible I/O
- Three State Outputs
- Data Bus Compatible I/O Function

4804 STATIC, TTL IN/OUT 1024x4 N-MOS RAM



GENERAL DESCRIPTION
Part Number 4804 is a 4K semiconductor random access memory organized as 1024 4-bit words. It is fully static and needs no clock or refresh pulses. It requires a single +5 volt power supply and is fully TTL compatible on input and output lines. The 4804 is packaged in a convenient 18 pin dual-in-line package.

FEATURES
- Single +5V Power Supply
- 1Kx4 Organization
- Replaces 4 1024x1 Static RAMs
- Completely Static—No Clocks or Refresh
- 18 Pin Package
- Access/Cycle Times 600 nsec max
- 250 mw Typical Operating Power
- Common I/O Bus
- TTL Compatible I/O
- Three State Outputs

4801 or 4804 4K RAM's
$8.95 8/$60.00 16/$100.00

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The MCM4116 is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs. By multiplexing row and column address inputs, the MCM4116 requires only seven address lines and permits packaging in standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated. All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116 is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes. The MCM4116 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible timing with read-modify-write, RAS-Only refresh, and Page-Mode capability.
- Industry standard 16 pin package
- 16,384 X 1 organization
- ±10% tolerance on all power supplies
- All inputs are fully TTL compatible
- Three-state fully TTL-compatible output
- Common I/O capability when using "Early Write" mode
- On chip latches for addresses and data in
- Low power dissipation-462mW active, 20mW standby(Max)
- Fast access time: 200nS
- Easy upgrade from 16-pin 4K RAMs
- Pin compatible with 2117, 2116, 6616, uPD416 and 4116

MCM4116 .... $24.95
Specs .... $.60

- For premium shipping (first class, special handling, etc.) add extra. Excess will be refunded.
- Please give street address for UPS shipping when possible.
- C.O.D. NO parcel post C.O.D. UPS C.O.D. Add 85¢ to order
- Any correspondence not connected with your order, please use separate sheet and include SASE for reply.
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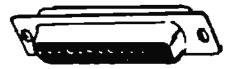
- Terms. Check, money order, credit card. Net 30 days to rated firms, schools and government agencies
- Claims for defective material must be made within 60 days of receipt of parcel. Claim must include invoice number date & defective parts



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Popular 25 pin subminiature "D" connector as used in RS232 interfaces.
Special sale prices!

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Set of 2 Male/Female screw lock adapters for joining socket and plug connectors.
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IMSAI S-100: Cont./Ctrs. .125" Row Spacing, .250"

50/100 Dip Sold.	$4.20 ea.	5 pcs.	$3.95 ea.
50/100 W/Wrap 3	3.75 ea.	5 pcs.	3.50 ea.
IMSAI CARD GUIDES	0.19 ea.	5 pcs.	0.16 ea.

CROMEMCO S-100: Cont./Ctrs. .125" Row Spacing, .250"

50/100 Dip Sold. (Or short W/Wrap)	$6.50 ea.	5 pcs.	$6.00 ea.

OTHER CONNECTORS AVAILABLE

.100" Contact Ctrs., .140" Row Spacing.

22/44 Dip Sold.	$2.30 ea.	5 pcs.	$2.10 ea.
25/50 Sold. Eye.	2.95 ea.	5 pcs.	2.75 ea.
40/80 Sold. Eye.	4.80 ea.	5 pcs.	4.50 ea.
43/86 Dip Sold.	4.90 ea.	5 pcs.	4.70 ea.
43/86 Sold. Eye.	4.90 ea.	5 pcs.	4.70 ea.

.156" Contact Ctrs., .140" Row Spacing.

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15/30 W/Wrap 3	$1.05 ea.	5 pcs.	$0.95 ea.
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IO-2 S-100 8 bit parallel I/O port, ⅔ of boards is for kludging. Kit ....$46.00 PCBD.........$25.95

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82S23	$1.50		
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2521	1.50	5055	1.25
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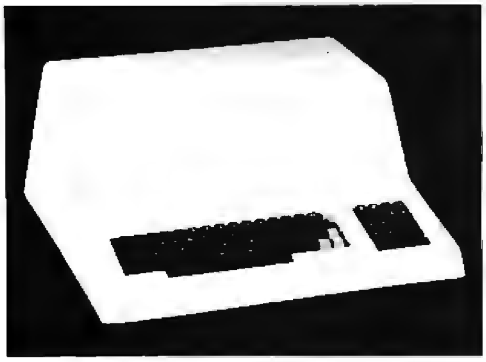
What's New?

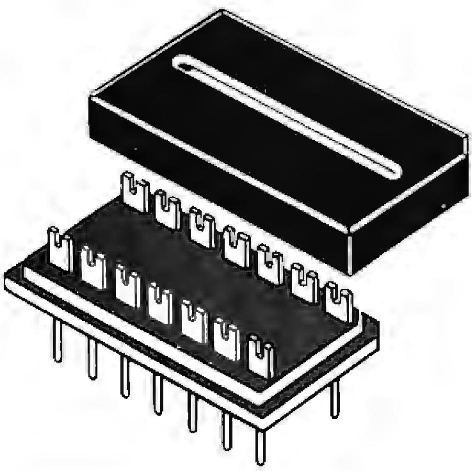
New Enclosure for Homebuilt Microcomputers and Terminals



Designed with the personal computer user in mind, this new case is now available for home built microcomputers and terminals. Constructed of molded fiberglass, the case is large enough (18 by 20 by 8 inches (46 by 51 by 20 cm)) to enclose a variety of components and sturdy enough to support a monitor or portable TV. The keyboard area will accommodate both a full-size keyboard and a hex pad (not included with case). The textured polyester finish is available in beige, white or black. Cutouts may be easily made with an ordinary sabre saw. Cast-in brackets are provided for mounting to a base plate. The price of the case is $59.95. An optional aluminum base plate is available for $15.95. For more information contact Technical Products Company, POB 12983, Gainesville FL 32604.■

Circle 582 on inquiry card.

New DIP Plugs and Covers



For the personal computer user or prototype engineer who needs to make interconnection assemblies, OK Machine and Tool Corp, 3455 Connor St, Bronx NY 10475, offers 14 and 16 pin plugs that fit into standard dual in line package (DIP) sockets. Plugs feature United Laboratories recognized glass filled thermo plastic bodies, and solder lugs on the top side are slotted for easy attachment of cable leads. Rectangular legs aid in the insertion into the socket. The leg and solder lug are one piece gold plated phosphor bronze. Packed two to a package, complete with slotted top-entry covers, the plugs are $1.45 for two 14 pin units and $1.59 for the 16 pin version.■

Circle 583 on inquiry card.

DM-1 Design Mate Adds Power, Metering to Solderless Breadboards

The Design Mate-1 is a self-contained unit that adds a 5 to 15 V variable regulated power supply and a 0 to 15 VDC voltmeter to a solderless breadboard terminal and bus strips.

The output of the DM-1 variable regulated power supply is 5 to 15 VDC at up to 600 mA for 9 W maximum of electronic drive.The 0 to 15 VDC meter and the power supply are brought out to their own binding posts on the face of the Design Mate case. The meter can then be used to set up the power supply voltage and reconnected to measure voltage parameters within the circuit being designed. Load and line regulation is better than 1%; ripple and noise are less than 20 mV at full load.

The package weighs 3 pounds (1.4 kg) and comes assembled with detailed operating instructions. The 117 VAC 60 Hz version is priced at $69.95. A 220 V 50/60 Hz version is available for 10% more. For further information contact Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509.■

Circle 585 on inquiry card.

Combination Coding and Video Layout Form Introduced for BASIC Users

A new coding form designed for BASIC or other line number oriented languages is available from Stirling/Bekdorf, 4407 Parkwood, San Antonio TX 78218. With grid lines lithographed in soft blue on a white sheet, Form 78C1 combines coding and interactive video layout functions into one unit. The form has 28 coding lines and retains the 6 mm by 3 mm (.02 inches by .01 inches) grid needed for comfortable writing.

Both 16 line by 64 character and 24 line by 80 character standard video formats are indicated on the form. Developed for minicomputer and microcomputer programming, Form 78C1's paper stock is a 22# opaque sheet which will take a plastic tip marker without spreading and will accept soft pencil equally well.

According to the company, it is pure enough for magnetic ink character recognition scanning equipment. For maximum writing ease and legibility, pens with fine hard plastic capillary action points and black ink should be used. Such pens as the Pilot Razor Point, Sanford's Expresso Fine Point or Big Sig II, Berol Super Flash and Flair Ultra Fine give sharp, crisp coding. The Pentel 0.5 mm mechanical pencil using 0.5 mm HB soft lead will give good results.

The BASIC coding and video layout form is available in 3 hole punched loose-leaf style in 100 sheet packages and as 3 hole punched 50 sheet pads with chipboard backing.■

Circle 584 on inquiry card.

Let the 3rd Hand Hold Your Circuit Boards

The 3rd Hand is an aluminum circuit board holder featuring one hand operation. Clamped to the edge of the workbench it holds the board at a convenient angle for placing parts and then is flipped forward to solder parts in place. The vinyl gasket protects the board from damage while holding it securely in place. The open end design allows it to hold circuit boards of any size. The price is $9.95 and the unit can be obtained from Studio 3, POB 1184, Kailua HA 96734.■

Circle 586 on inquiry card.

VISIBLE OR INFRA RED	USED FOR CHARACTER RECOGNITION FOR COMPUTERS WITH EXTERNAL CIRCUITS	MAY BE USED IN A VACUUM, UNDER WATER, HIGH ALTITUDE	IN MAGNETIC ENVIRONMENT BECAUSE THERE IS NO HIGH VOLTAGE OR MAGNETIC DEFLECTION

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202 VIDEO CAMERA KIT

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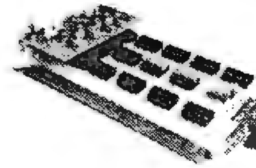

ADVANTAGES

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- We supply the power board, so only a 5V 1 Amp power source is needed
- The circuitry has been simplified for easier assembly
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FEATURES

- Sensitive to infra red as well as visible light
- May be used for IR surveillance with an IR light source
- Excellent for standard surveillance work, because of light weight and small size
- All components mounted on parallel 3¾″ × 6½″ single sided boards
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We supply all semiconductors, boards, data sheets, diagrams, resistors and capacitors, and 8MM lens. Sorry we do not supply the case, batteries and 5V supply.

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4002 –	.18	4020 –	.90	4050 –	.35	74C74–	45
4006 –	.95	4021 –	.90	4053 –	1.10	74C83–	1.15
4007 –	.18	4022 –	90	4055 –	1.25	74C86–	40
4009 –	.37	4023 –	18	4066	.70	74C93–	75
4010 –	.37	4024 –	75	4071 –	.18	74C151	1 40
4011 –	.18	4025 –	18	4076 –	.97	74C160	1 05
4012 –	.18	4027 –	37	4520 –	.70	74C161	1 05
4013 –	.29	4028 –	80	74C00–	.22	74C174	1 05
4014 –	.75	4029 –	.95	74C02 –	.22	74C175	1.05
4015 –	.75	4030 –	33	74C04 –	.24	74C193	1 20
4016 –	.29	4035 –	.97	74C08 –	.22	74C901	48
4017 –	.90	4042 –	65	74C10 –	.27	74C902	40
4018 –	90	4046 –	1 35	74C42	85	74C914	1 70

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7412–	.13	7485–	.87	74175–	.85
7413–	.36	7486–	.28	74176–	.75
7414–	.60	7489–	1.25	74177–	.75
7416–	.22	7490–	.42	74180–	.65
7417–	.25	7491–	.58	74181–	1.90
7420–	.13	7492–	.43	74190–	1.00
7425–	.25	7493–	.43	74191–	1.00
7426–	.22	7494–	.67	74192–	.79
7427–	.19	7495–	.65	74193–	.79
7430–	.13	7496–	.65	74194–	.80
7432–	.22	74107–	.28	74195	.50
7437–	.21	74121–	.29	74196–	.86
7438–	.21	74122–	.38	74279–	.55
7440–	.13	74123–	.45	74367–	.50
7441–	.70	74125–	.40	75325–	1.50
7442–	.37	74126–	.40	75491–	.50
		74150–	.94	75492–	.50

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2 2 UF 20V 5 $1 00	30UF 6V 5/$1 00
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4.7UF 15V 5/$1.00	68 UF 15V $ 50
	100 UF 10V $ 40

74LS SERIES

74LS00	19	74LS132	70
74LS02	19	74LS138	70
74LS03	19	74LS139	70
74LS04	.21	74LS151 –	59
74LS05	21	74LS153	59
74LS08	21	74LS155	62
74LS09	21	74LS156	62
74LS10	20	74LS157	59
74LS11	28	74LS160 –	79
74LS13	[illegible]	74LS161 –	79
74LS14	[illegible]	74LS162	79
74LS15	21	74LS163 –	79
74LS20	21	74LS168 –	80
74LS21	21	74LS169	80
74LS22	21	74LS170	1 40
74LS26	29	74LS173 –	[illegible]
74LS27	25	74LS174 –	[illegible]
74LS28	26	74LS175 –	75
74LS30	21	74LS181 –	2.00
74LS32 –	25	74LS190 –	[illegible]
74LS37	28	74LS191	88
74LS38	[illegible]	74LS192	88
74LS40 –	[illegible]	74LS193	88
74LS42	[illegible]	74LS195 –	50
74LS47	[illegible]	74LS196	75
74LS51	[illegible]	74LS197	75
74LS54	25	74LS221	1 [illegible]
74LS73	35	74LS257 –	68
74LS74	34	74LS258 –	68
74LS75	[illegible]	74LS266 –	25
74LS76	[illegible]	74LS279 –	[illegible]
74LS85	75	74LS290	[illegible]
74LS86	35	74LS293 –	[illegible]
74LS90	50	74LS365 –	49
74LS92	50	74LS366 –	49
74LS93 –	50	74LS367 –	49
74LS109	35	74LS368 –	49
74LS112	35	74LS375 –	[illegible]
74LS113 –	35	74LS386 –	35
74LS114 –	35	74LS390 –	1 [illegible]
74LS125 –	45	74LS670 –	2 00
74LS126	.45		

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LM 358	– .70
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LM377	– 1.60
LM 380	– .95
LM 381	– 1.25
LM 382	– 1.25
LM387	1.25
LM537	– 2.50
LM553	– 2.50
LM 555	– 39
LM 556	– 85
NE540L	– 2 25
560	– 2 00
565	– .95
566	– 1.10
567	– 1 10
703	– 90
733H	.75
592H	.95
709	– .25
710	– .35
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747	– .50
LM 1310	– 2.50
1456	– 95
1458	– 50
3900	– .40
8038CC	– 3.90
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100	.40	.70	1.30	.40	.50	1.20
200	.70	1.10	1.75	.60	.70	1.60
400	1 10	1 60	2 60	1 00	1 20	2 20
600	1 70	2 30	3 60		1 50	3 00

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FOR SALE: Blank 4 K memory cards, 2102 memories, buffered address and data lines, provisions for on board regulation and standby power utilization, $18. Industrial quality G-10 glass epoxy boards with gold plated 44 pin edge connector, on board decoding to 32 K of memory. Specially manufactured for my personal system, but easily used for KIM or other expansion. I also have 5 slot mother boards — $20 — and power supplies. Bob Ribbeck, 10990 Howe Rd, Clarence NY 14031.

FOR SALE: MITS Altair 88-S4K Synchronous 4 K memory board. Built by experienced kit builder, and checked out by local MITS computer store. Full documentation pack included. Wish to use slot for higher density board. Asking $150. Dave Busse, 1510 W Dempster, Mount Prospect IL 60054, evenings (312) 364-0147.

FOR SALE: Distortion Analyzer TS-917/GG, Stelma model TDA-2 detects bias distortion and other faults of 5 level teleprinters. 60-75-100 WPM. With instruction manual, $40. John Riley, 914 N Cordova, Burbank CA 91505.

FOR SALE: Radio Shack ASCII keyboard assembled and tested for $40. Like new TI-58 programmable calculator–make offer or swap for SwTPC hardware. Dennis Doonan, 2307 Carlisle Av, Racine WI 53404.

FOR SALE OR TRADE: Stand and enclosure for chain printer. Can be modified to house a Centronics printer. Would consider trading for Teletype model 35 RO parts. James Mullen, RR 5, POB 106, Evansville IN 47711.

FOR SALE: Updating to bigger system. Must sell Digital Group Z-80 system complete with Z-80 processor, video and cassette IO board, four parallel ports, 8 K bytes static memory. Complete with case and full documentation. Originally $1400, will sell for $900. Ray Cote, POB 68, Peterborough NH 03458.

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Please note that it may take three or four months for an ad to appear in the magazine.■

FOR SALE: Autonetics ½ inch magnetic tape drive minideck and solid state electronic control circuits. Requires parallel interface. $75 plus shipping (weight 45 lbs). Dick Jugel, 3814 N 85th Av, Omaha NE 68134, (402) 572-8441.

FOR SALE: Programs for HP-25. Sniper, Cannon, Wumpus, Wumpus 2, Artillery, Artillery 2, Golf, Hi-Lo, Blackjack, Mastermind, (including Random number generator, Roulette, Poker-machine, Parachutist, Biorhythm (includes 100 year calendar), Amplifier (designs simple amplifiers). $4 each, 5 for $18, 10 for $32 or complete set for $45. Also, programs custom written to requirements and to run on any of Hewlett-Packard range (specify). $10 each. I Webber, 92 Royal Pde, St Johns Wood 4060, AUSTRALIA.

FOR SALE: A Heathkit H8 and H9 and cassette recorder, fully assembled and running with 16 K of memory, including many programs and three versions of BASIC. Will sell for $2450 or over $100 less than the price of the kits. Price includes shipping. George Walker, 67 Wyndham St, Guelph Ontario, CANADA (519) 823-1411.

WANTED: Intel 8008 (or −A) processor based system or parts thereto. Send specifications and requested pricing. Also need October 1977 BYTE in good condition. James Tucker, POB 471, APO New York NY 09305.

WANTED: Speech Synthesizer and Heuristics Speechlab in good condition. State price and condition. Contact William Yeap, 2217 7th Av, NW, Calgary Alberta, CANADA T2N 0Z9, (403) 283-6863.

WANTED: September 75 thru June 76, September 1976, January 1977 and February 1977 BYTE issues. Will accept all or separate copies. Will accept a reasonable price. Randy Pray, 3209 SW 2nd, Des Moines IA 50315, (515) 288-8189.

FOR SALE: TRS-80 sci-fi games (4 K, L1): Galactic Blockade Runner–a sophisticated space war game. You control your ship and its weapons, fight off enemy attacks and cope with hazards to run the blockade and to deliver vital supplies on time. $9.95 for cassette and 12 page manual. SASE for list of games. Tim Quinlan, 219 Washington Av, Chelsea MA 02150.

FOR SALE: Two IMSAI 4A-4 static programmable memory boards. Professional construction, from an operational IMSAI 8080 system. Going to Z-80 and do not want the 450 ns slow programmable memory in the system. $200 buys both boards. K J Halliwell, 2373 John Smith Dr, Apt F, Schaumburg IL 60194, or call after 6 PM (312) 885-0362.

FOR SALE: Heathkit H-8 Computer system, 16 K memory, H-8-5 serial IO and cassette interface. All available Heath software, assembled and working, $900. Lear Siegler model 7700 Display Terminal, serial RS-232 output, 25 lines with 80 characters per line, service manual, $450. Bob Majanski, 214 Coolidge Av, Hasbrouck Heights NJ 07604, (201) 288-3742.

FOR SALE: One Processor Technology 8 K programmable memory board, working, $150. One Ithaca Audio 8 K programmable memory board, working, $100. Two Godbout 4 K programmable memory boards, working, $50 each. One Vector Graphics 18 slot mother board, assembled, $75. One ICOM microfloppy system (board and floppy) complete with FDOS III for the SOL, working, $800. One PerSci dual floppy drive, working, $800. All prices are negotiable. Jeff Roloff, 2214 Brookshire, Champaign IL 61820.

FOR SALE OR TRADE: Hewlett-Packard Model 180E dual trace oscilloscope. Excellent condition asking $300 or trade for KIM-1 or similar system. Also power supply with ±24 VDC, ±12 VDC, ±5 VDC and −6 VDC all outputs rated at 5 A. Asking $30. Contact Roger at (904) 651-4153.

FOR SALE: Five computer memory and IO boards (all units from Digital Equipment Corp). They are all in new condition, but I cannot guarantee any of them as I do not have the equipment. Three of the boards are core memory (nonvolatile). There is a 4 K by 12 DEC part number H220 P-33, unmarked board, and a 64 by 64 by 18 IO part number CF-4. The remaining boards plug into a PDP-II. One is a memory driver G231E-P2; the other is a control and data loops board number G109C. Boards go to the highest bidder. Marty Bunshaft, 29A Forest Acres Dr, Bradford MA 01830.

FOR SALE: 12 issues of BYTE (October 1976 thru September 1977). Best offer or trade for what have you. G F Sabin, 6022 Sage Dr, Orlando FL 32807.

FOR SALE: PDP-15 computer 24 K of 18 bit core memory, 4 DEC tapes, Teletype, paper tape reader /punch, Fortran and Focal. Always on DEC full maintenance. Dr L K Steinrauf, Dept of Biochemistry, I U Medical School, Indianapolis IN 46202, (317) 264-7544.

FOR SALE: OSI-400 computer system. Assembled and tested by a professional. 4K programmable memory (unfinished 2nd 4 K board included). Cassette IO, video display, keyboard; $900 value, best offer takes it. Assembled and running. Robert W Warfield, 3202 Boyd, Midland TX 79701, (914) 694-7035.

WANTED: IMSAI/iCOM/DEBBI owners to join European based users group for software exchange, mutual assistance; or alternatively CP/M European users group. Contact K A Geiger, 66, Rue Rothschild, 1202 Geneva SWITZERLAND.

FOR SALE: Fine 1959 SULLIVAN pipe organ with electric key and stop action ideal for artist/hobbyist integration of micro based C^3 as described in two articles in February 1978 BYTE. Two manuals (61 keys), 32 pedals, nine ranks, 498 pipes, chimes, pistons, shutters; suitable for home or church installation (in daily use in home now). $6200 plus optional packing and shipping. Send SASE for complete specification and details. Phil Bergstresser, 128 Jackson Av, Madison AL 35758.

I am looking for an individual or company willing to provide on site service contracts for the metroplitan New York City area. Equipment would be microcomputers and related peripherals. Also looking for other owners who would like to have on site service and maintenance for their equipment. B Rabinowicz, 1061 54 St, Brooklyn NY 11219.

MUST SELL: 3P+S Processor Technology IO card. Two parallel IOs and one serial IO. $100, assembled and tested. Paper tape reader, Oliver Audio OP-80A, used only several times, assembled and tested, $50; all that is needed is to interface a parallel input. PerCom Electronics cassette interface; all that is needed is a serial or parallel IO and cassette recorder. Assembled and tested, $50. Godbout PROM board, holds 8 K (5204) and has Godbout monitor. $75 takes assembled board and PROMs. Larry Belmontes Jr, 1762 Yale St, Corpus Christi TX 78416, (512) 855-2687 or (512) 854-2662.

PROM PROGRAMMING: From binary paper tape: 1702A ($4), 2708 ($8). From hexadecimal or octal listing: 1702A ($5), 2708 ($16). You supply the read only memory. Quantity discounts for multiple copies. 48 hour turnaround. David Corbin, 11704 Ibsen Dr, Rockville MD 20852, (301) 881-7571 after 6 PM.

FOR SALE: First 16 issues of BYTE except number 11 (July 1976 BYTE). Also February, March and April 1977 *Data Communications* for free. No reasonable offer refused. L R Chauvenet, 11 Sussex Rd, Silver Spring MD 20910.

FOR SALE: Sharp Associates Selectric typewriter interface kit model SK2. Converts any selectric typewriter to printer and keyboard input peripheral. Includes power supply and transistor-transistor logic (TTL) compatible outputs, assembly and interface manuals. Partly assembled $180. Contact Jeff Duntemann, 6208 N Campbell Av, Chicago IL 60659, (312) 454-2755 during business hours, otherwise (312) 764-5069.

FOR SALE: Altair 8800 with 16 slot motherboard and 16 edge connectors, cooling fan modification, 2SIO serial IO with both ports, 88PIO parallel IO board, 1 K static memory with 512 bytes of memory, 12 K static memory, 4 K read only memory software board with 8080 assembler, text editor, system monitor and all documentation. All A and T, original cost over $2000, yours for $1500 and you pay shipping. Don Cheeseman, 8231 Creekline Dr, San Antonio TX 78251, (512) 681-4938.

WANTED: Cheap optical paper tape reader; RAECO, OAE, or similar. Also cheap high-speed 8 level paper tape punch, hopefully with enough documentation to build a parallel port interface. Chuck Johnson, 17104 Via Alamitos, San Lorenzo CA 94580, (415) 278-6595 evenings.

FOR SALE: Digital Group system with 8080 processor, 6502 processor, 26 K programmable memory, erasable read only memory card 64/32 character displays, two phidecks and interface, keyboard, video monitor, audio cassette, 25 A power supply, processor cabinet, software, BASIC, assembler, editor and games. All for $1500. Bill Seiler, number 202, 1717 Woodland Av, Palo Alto CA 94303, (415) 323-2083.

FOR SALE: A number of copies of BYTE, volume 1, number 1 at $10 per copy. Copies will be mailed insured as long as supply lasts. Joe Haran, 517 Bridge St, Mont Clare PA 19453, (215) 935-0484.

WANTED: Literature on Intel SDK-80 (the MDS-80 Systems Development Kit). I am interested in specific applications of your SDK-80 (ie: distributive processing). Dave Fashenpour, 5411 Cerro Vista, San Antonio TX 78233.

FOR SALE: TI-59, PC-100A, two libraries (master and statistics), 40 magnetic cards, 22 thermal paper rolls, three card holders, one battery charger, one carrying case, all in perfect condition. Plus my own special programs including Horse Race, Universal Calendar, Personal Finance (Expense Analysis and Cash Register), Alphanumeric Entry Routine. All documents came with original shipment (they are still brand-new). Please quote offer; if no reply, outfit has been sold. H T Chen, Physics Dept, University of Georgia, Athens GA 30602, (404) 546-1065.

FOR SALE: Altair 8800A mainframe microcomputer with 40 K memory, ¼ K programmable memory/read only memory resident bootstrap loader for diskette system, 88DCDD flexible diskette drive with controller and extended BASIC software version 4.1. Additional boards: vectored interrupt/real time clock, ARC tape IO, two SIO RS-232 IOs, PIO parallel IO etc. Retail value over $3,500; asking $2,000 for all, including many extras; will sell separates too. TVT Modified SwTPC 32 character line with video monitor and Pendar keyboard — $150. Burroughs terminal/printer with logic controller — $150. Ira Wilner, POB 582, Brattleboro VT 05301, (802) 254-8807.

WANTED: Any Micro Systems Design MF10-1 IO Board user. Help. Stephen Gladstone, 1103 Namdac Av, Bay Shore, Long Island NY 11706, (516) 666-8342.

PROM PROGRAMMING: From binary paper tape: 1702A ($4), 2708 ($8). From hexadecimal or octal listing: 1702A ($5), 2708 ($16). You supply the read only memory. Quantity discounts for multiple copies. 48 hour turnaround. David Corbin, 11704 Ibsen Dr, Rockville MD 20852, (301) 881-7571 after 6 PM.

WANTED: I need a design or kit to convert an IBM 2741 selectric terminal to ASCII. It presently uses correspondence code and requires a special element which I would like to replace with a regular element. Peter Baum, POB 399, Sunnymead CA 92388.

WANTED: Floppy disc drives (any condition), line printer (100+CPS), OSI boards, S-100 boards, 6502 hardware and software, C-MOD (MMM/Celetron) boards and software. I R Peterson, 669-23 Av NW, St Paul MN 55112, (612) 633-1599.

FOR SALE: Persci model 70 8 inch floppy drive and model 1070 intelligent controller. Never powered up — perfectly new, $1000. Elwood Downey, 1000 W Spring Valley, number 242, Richardson TX 75080, (214) 690-1523 home or 231-9303 ext 312 work.

WANTED: Modules/parts to restore a DEC RK05 disk drive for personal use. G180 read/write board, M7700 board, M7701 board, M7702 board, G938 board, H604 board, two 20 V regulator modules, 5 V regulator module. The above items do not have to be in working condition. Peter A Balkus, 18 Clearview Av, Lynn MA 01904.

GETTING MARRIED: So I'm selling the whole ball of wax to pay for my honeymoon: IMSAI with full motherboard and connectors, SDS Z-80 card, 24 K 500 ns memory, 3P+S IO card, Tarbell floppy controller, real time clock, Tarbell tape Interface, bus terminator, 2708/2716 erasable read only memory card (with two 2708s) 12 by 80 video display with built-in modem and much 8080/Z-80 Software. Complete documentation on everything. Worth much more than the $2,000 I'm asking. Judd Ellmers, (201) 967-2645, 9 AM to 5 PM. *[Congratulations from BYTE. . . .***DWH***]*

FOR SALE: Complete microcomputer system. IMSAI 8080 mainframe with Wunderbuss, 4 MHz Z-80 processor, 56 K bytes of fully static programmable memory (250 ns) PerSci 277 dual disk drive with PerSci power supply and cabinet, DMA disk controller, D C Hayes modem board (set up for autoanswer timeshare using CP/M software), Lear Siegler ADM-2 video display terminal, Data General Dasher terminal/printer (60 cps matrix), complete library of CP/M software (version 1.4) with documentation, approximately 20 diskettes. Many many extras! Individual components cost over $9800 in kit form. Asking price is $8900 or best offer for this completely integrated system. (714) 521-2344 or 738-8086.

CASINO BLACKJACK: For TI Programmable 59. Most complete version available for a hand held unit. Allows up to six players to bet, hit, stand, double down, insure and split pairs against the house. Keeps score and displays all cards automatically. Cost is only $3.50 and includes program listing and quality documentation. Send two mag cards and will record this 600+ step program for you as well. Game rules from Thorp's *Beat The Dealer*. Robert Griffin Jr, 104 Briar Rd, Nanuet NY 10954.

FOR SALE: TRS-80 level-1 tapes and program lists. Star Trek (runs on 12 K), list $7, tape $10. Lunar Lander (runs on 4 K), list $3, tape $6. Biorhythm (runs on 4 K), list $4.50, tape $9. J R Menzies, 7106 Colgate Dr, Alexandria VA 22307.

FOR SALE: Two Innovex floppy drives (compatible with Tarbell and Peripheral Vision interfaces), three 8 K memory boards (4 MHz), one Alpha Video II video board (4 MHz compatible, on board keyboard port with 5 V and status out, 1 K buffer, etc), one GRI keyboard (case and connector cable), one video monitor (as in Computer Warehouse ad). John Whiffen, 443-6324 or 279-1496, Toronto CANADA.

FOR SALE: Must sell ASAP an IBM 6420 computer system with 6425 magnetic ledger card reader attached. It contains 1 to 220 column tractor feed and 1 to 130 column friction feed selectric with a magnetic ledger card reader attached. Unit works and I have some manuals for it. Some boards and lots of extras are included. Unit sold new for $55,000 a few years ago, will sell to first person with certified check for $1200 or call and make offer above. Dave Dahlberg, 4375 Weber River Dr, number 95, Ogden UT 84401, (801) 399-2396.

HELP: Southern Connecticut New Haven area; anyone using Tarbell disk system please contact me for mutual system support. Also need help in maintenance, fine points of CP/M; will pay! James Van Pelt, 25 Sagamore Cv, Branford CT 06405.

WANTED: Programs for ecosystem and forest management simulation that could be used in a study of the feasibility of the utilization of wood for energy. Mitchell Bayersdorfer, 8325 New Second St, Elkins Park PA 19117, (215) 635-2126.

M6800 CROSS ASSEMBLER: A two pass cross assembler written in FORTRAN IV is available for the M6800 Motorola micro. Input is in fixed format; statements are similar to Motorola assembler language, most features of the language being supported. Additionally, a system symbol table is supported, enabling symbolic reference to system addresses, and assembly of routines to contiguous memory locations. Send $1 for the manual, and $5 for the listing, (or $14 for a paper tape) to: G A R Trollope, 466 Caswallen Dr, West Chester PA 19380, (215) 431-2885.

FOR SALE: HP-25 Game Programs. I have several games including a neat golf game, two versions of Master Mind (or Comp IV), Football, Tic-Tac-Toe, Mortar Battlefield, Battle the Dive Bomber and others. $2 each or trade. Jerry Hansen, 420 West 800 South number 1, Richfield UT 84701, (801) 896-6110.

FOR SALE: Fully assembled and fully operational Morrow Micro Stuff/Thinker Toys front panel processor board. All documentation included. First certified funds for $300 gets rid of that "knucklebuster," double clutching front panel, including UPS shipping charges. W Howard Adams, 1590 South Krameria St, Denver CO 80224, (303) 756-4052.

FOR SALE: ACT II, a video terminal capable of over the telephone communication with its built-in acoustic coupler. Complete with video display and RF Modulator. $600. Contact: (516) 671-3957.

FOR SALE: Paper tape reader and punch; Heathkit H10, assembled and tested. 50 character per second reader, 10 character per second punch. $320 delivered with manuals, cable and supply of tape. Write D T Mears, 32-E S Westmoor Av, Newark OH 43055.

FOR SALE: Built and tested SwTPC 6800 with 8 K (extra 2 K unbuilt), Hazeltine 2000 video display terminal, and Hazeltine thermal printer (with extra Texas Instruments print head) in excellent condition. Will make super system just by adding diskette or tape drive. $1595 complete or best offer. Also BYTE volume one, number 1 in excellent condition. V Farmer, 78 Harvard St, Walpole MA 02081, (617) 668-7339.

FOR SALE: Elf II with 4 K memory, the giant board, and expansion power supply. $200. Winston Cope, 302 Anderson St, Apt G, Durham NC 27705, (919) 684-0893.

FOR SALE: TVT II with keyboard, monitor and modem. Ready to go on line. Asking $350. Jack S Davis, POB 5, Endwell NY 13760.

FOR SALE: Assembled SwTPC CT-64 terminal with Hitachi model P-05 TV monitor $450. The ASCII terminal is in excellent condition and is configured for 16 lines of 64 characters. The serial interface is RS232 and can be strapped for various baud rates. Jim Crane, 5650 Windsor Way number 308, Culver City CA 90230, (213) 649-4187.

FOR SALE: PET BASIC action games including Bomber, Seawolf, Indy 500 and Aerial Dogfight. All four on cassette. Send $6. Andy Fraley, 1753 York Rd, Reading PA 19610.

HELP: I have a DEC PDP-8/I mini with a Dataram Corp memory stack, P/N 2100270, S/N DR5049D. Does anyone know if the firm is still in business and the address where they may be contacted: or does anyone have any information on the stack? If you can help with any information please write. Thomas Parquette, 116 Sanford Av, Clinton New York 13323.

LEARN: Complete self-study microcomputer training system. Includes microcomputer, workbooks, texts, interfacing board and power supply. Will send full information to all sending me SASE. First $500 takes this $1200 package. Tony Durr, 2802 W Kenmore, Tampa FL 33614. ■

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BOMB–BYTE's Ongoing Monitor Box

Readers Choose "Choosing a Microprocessor"

The first place winner in the July BOMB (BYTE's Ongoing Monitor Box) was "How To Choose a Microprocessor" by Louis Frenzel, page 124. Second prize went to Lane T Hauck for "Who's Afraid Of Dynamic Memories?", page 42. The first place article score was 1.4 standard deviations above the mean, and the second place article was 1.34 standard deviations above the mean—quite a close score. The authors will receive prizes of $100 and $50, respectively. "Antique Mechanical Computers," page 48, placed third, and the other two history articles tied for fourth place.■

BYTE READER SERVICE

October 1978

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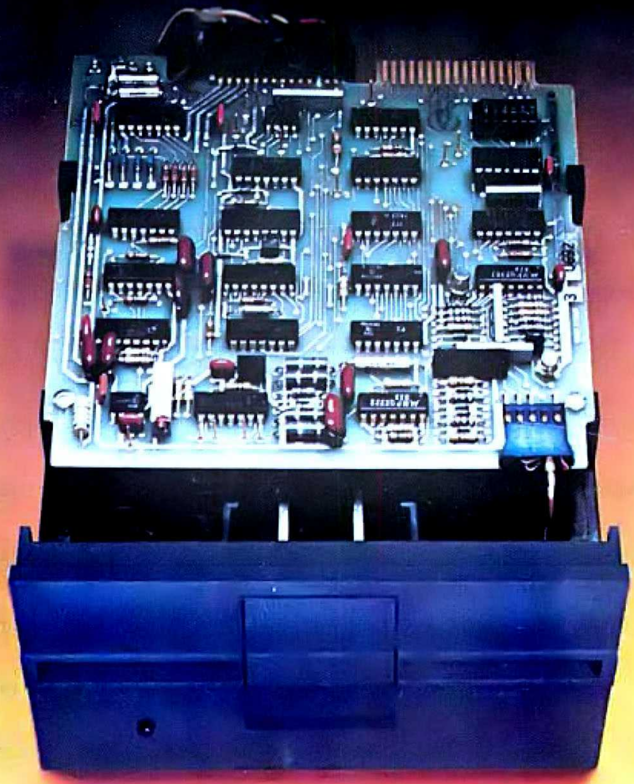

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