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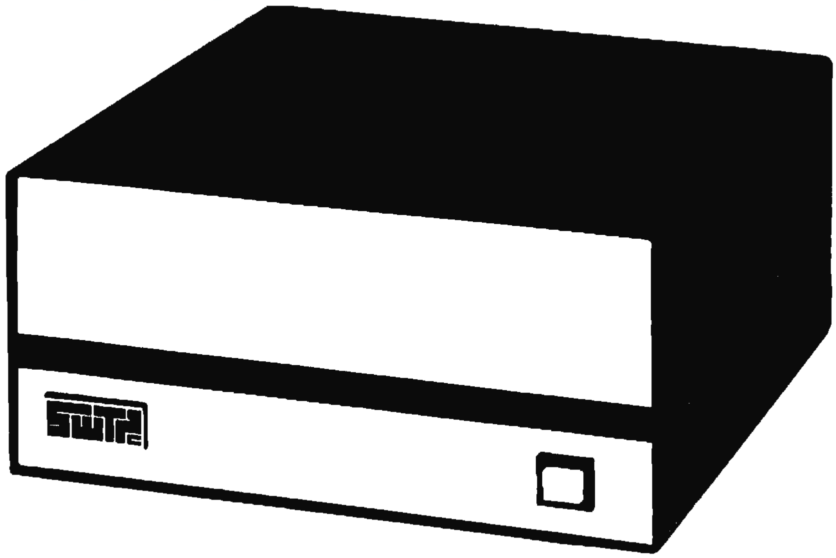
BYTE

the small systems journal

The World's Most Powerful 8-Bit Microcomputer



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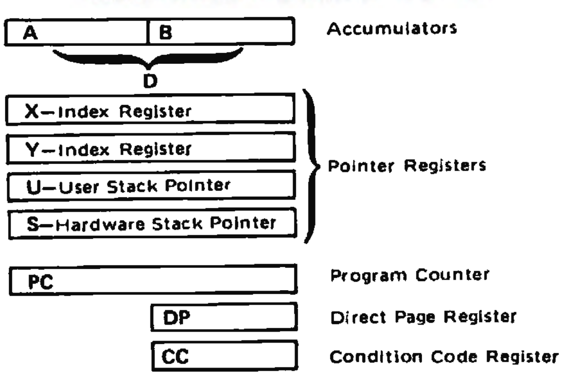

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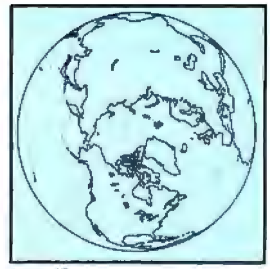
In The Queue

BYTE May 1979
Volume 4, Number 5

Foreground



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Background

Nucleus

Cover Art: BENEATH THE GRID, *by Robert Tinney.*

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In This BYTE

This issue's theme is provided by an article on various cartographic projections by William Johnston. To emphasize this theme of mapping terrain with computer models, Robert Tinney's painting "Beneath The Grid" shows a landscape with a superimposed grid of luminescent white lines as might be projected in the mind's eye by an appropriate graphic output device.

Microcomputers allow the quick and easy performance of operations that take an extemely long time to perform by hand. One of these operations is drawing maps from accumulated tables of data. William Johnston describes the simple programs used to produce **Computer Generated Maps.** *page 10*

A data tablet is a graphical input device that enables you to enter visual images into your computer. Richard Blum has a program for **Representing Three-Dimensional Objects in Your Computer.** *page 14*

If you need to communicate digital information from one point to another through an electrically noisy environment, then optical communications may be one solution. If you are going to communicate over long distances or at high speeds, then a laser may be the best choice for a light source. This month Steve Ciarcia explains how to **Communicate on a Light Beam.** *page 32*

The people interested in just wetting their feet in the field of microcomputers are usually not looking for a very big system. A single board computer is often a good first experience. The Ohio Scientific Superboard II is one single board computer which has some interesting capabilities. Find out what Chris Morgan thinks about **The Superboard II.** *page 50*

Flexible video displays have been made possible by special display controllers. Bob Haas describes four devices from different manufacturers and tells how he used a specific video display controller in a successful construction project. You can learn more about these single integrated circuit marvels in **Single Chip Video Controller.** *page 52*

If you do not have documentation for a machine language program, it is almost impossible to determine how the program works. Bob Lentz describes a **6800 Disassembler** that he wrote for his SwTPC 6800 system. *page 104*

Possession of an integer arithmetic language does not preclude the writing of intricate programs involving trigonometric functions. David J Beard describes how he used an integer BASIC to develop navigation routines for **Spacewar in Tiny BASIC.** *page 110*

The most prevalent form of output from a personal computer seems to be a video display. Therefore, the serious hobbyist should be aware of the number of different video display controllers that are available. Chris Tennant looked at the Intel 8275 video display controller and liked what he saw. In his article he describes a video interface using **The Intel 8275 CRT Controller.** *page 130*

In part 2 of **Smart Memory,** Randy Smith presents a series of black box diagrams to describe the workings of an associative memory. *page 150*

The "wraparound" queue can save you time during input and output operations on your computer. W D Maurer explains how the queue works and how to implement it on 8080 computer systems in **Simultaneous Input and Output for Your 8080.** *page 164*

Last month Len Gorney described how to implement a queue on a computer. This month he talks about real life queues and how the science of **Queuing Theory** can be applied. *page 176*

The CORDIC algorithm is a venerable and efficient method for calculating trigonometric functions. John A Ball gives some practical suggestions to experimenters in **Trigonometry in Two Easy Black Boxes.** Find out how you can streamline your number crunching with CORDIC. *page 184*

Good programming techniques are vital in personal computing as well as in computing in general. Author Delmer D Hinrichs, using tic-tac-toe as an example, describes the strategies of the game programmer in **Tic-Tac-Toe: A Programming Exercise.** *page 196*

Ralph Stirling describes how to turn a motorized wire wrap tool into a motorized unwrapping tool in **The Hobby Unwrap.** *page 218*

For owners of Signetics 2650 based computer systems, Edward R Teja and Gary Gonnella have provided a useful disassembler program to help make sense of those hexadecimal machine language listings. Read **A Mini-Disassembler for the 2650.** *page 233*

If your microcomputer lacks an assembler or high level language, it will be necessary to hand assemble all of your programs. To do this quickly and accurately it is a good idea to develop a consistent routine. Erich Pfeiffer describes a useful technique in **Aids for Hand Assembling Programs.** *page 238*

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Editorial

Don't Forget the Hardware...

by Carl Helmers

With respect to manufactured products for the small computer user, we live in a time of plenty. There are at least 20 to 30 different manufactured or kit versions of complete personal computer systems, many featuring numerous models and sets of options. The hardware of these computers is complete, and in the better brands comes with ample documentation of the system's internals. The systems software comes in various stages of completeness and usefulness as a software development tool to satisfy particular personal computer users' needs.

Many readers, like myself, may tend to hesitate at the thought of experiments which involve building hardware to couple with appropriate software, in order to accomplish an application. But what is the mystery of peripheral hardware?

In this era of integrated circuits, standard logic levels, and a wealth of solid state parts, even the most hesitant software addict can, with a small amount of effort, create custom hardware for personal applications by the simple act of wiring. I come from a software oriented background, and use programs in place of dedicated hardware wherever possible. But when I want to use my program to turn the lamps on and off in my house, in response to voice inputs, I "somehow" have to make my computer talk to 110 VAC 60 Hz. There is no way that my software can switch several amperes without some assistance.

One alternative means to accomplish this goal is to purchase one of several fairly elaborate AC wiring control interfaces which are coming on the market. But, if you want to learn about hardware and the simplicity of interfacing, you can make a simple evening's project of wiring several optically isolated solid state relays to a parallel output port for your computer. The ease of interfacing is phenomenal.

I recently purchased several solid-state relays (see photo 1) from a local electronics parts distributor. This hybrid relay takes a standard TTL (transistor-transistor logic) signal of 5 V as its input, the same kind of a signal which is supplied by any typical computer's TTL output port lines. It is optically isolated, so there is no direct electrical connection to the computer. Short of dropping a screwdriver across the 110 VAC lines, there is no chance of errant 110 VAC entering the back side of your computer.

Text continued on page 123

Photo 1. At $12.80 (quantity one) from an electronics distributor, optically isolated solid-state relays like this open up a whole world of practical personal computing experiments around the home.

"My 8 to 5 minifloppy™ now works nights and weekends."

"I own a fast-growing business and before I bought my computer system I put in a lot of late hours keeping up with my accounting and inventory control. Now the computer does my number crunching quickly, so I have time after hours to have some fun with the system. My son and I started out playing Star Trek on the system, and now we're learning to play chess.

"When I was shopping around for my system, the guys in the computer stores demonstrated all the unique features of the minifloppy. I've got to admit that at first I didn't really understand all the technical details. But now that I use the system every day, I really appreciate the minifloppy's fast random access and data transfer. I like the reliability, too.

"I'm glad I went with Shugart drives. Look, when you lay out your own money for a system, you want dependable performance and good value. Do what I did. Ask for the system with the minifloppy."

If it isn't Shugart, it isn't minifloppy.

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See opposite page for list of manufacturers featuring Shugart's minifloppy in their systems.

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Letters

KUDOS FOR ITHACA

I have recently had the pleasure of *doing business with* a company which deserves recognition. I ordered a 16 K byte expansion kit from Ithaca Audio and installed it in my TRS-80 expansion interface box. Over several months I discovered that most of the time it didn't work. I also discovered that this was a design problem with the Radio Shack expansion interface, not the memory.

Radio Shack was not helpful. After all, I *had installed* additional memory not purchased through Radio Shack. I called Ithaca Audio, expecting a similar reaction. On the contrary! They knew about the various problems with the interface expansion box and offered the following free aid:

- a replacement set of eight NEC memories which require less frequent refresh signals.
- Should this fail, I would send them my expansion interface box and both sets of memory. They would return the interface in working order.
- If the new memory did work, I would then return the original set.

The NEC memory worked fine. All problems were solved. Now I *know* that when Ithaca Audio guarantees that their upgrade kit will work, they mean it.

Al Baker
2327 S Westminster St
Wheaton IL 60187

COMMENTS ON COMPUTER ASSISTED INSTRUCTION

I appreciated the articles by Davidson, Gerhold, and Kheriaty (November 1978 BYTE) and by Gerhold (December 1978 BYTE) relating to computer assisted instruction (CAI) on microcomputers. The discussion on what constitutes good and bad CAI courseware was helpful, and the description of PILOT software they are using was also informative. I am pleased to learn of work being done in the area of CAI on microcomputers, for my experience suggests it can be a very useful teaching tool.

One concern I have is that the microcomputer system described in these articles does not include the capability to prepare courseware on the small computer system. The approach taken by the authors to prepare and test courseware on a larger computer system, and then to use that courseware with microcomputers, has merit for their situation where the larger machine is readily available. However, many persons do not have access to such systems. Moreover, course objectives change rather frequently and individual teachers will prefer to present materials differently. It seems to me the small computer system should permit the teachers to write, test, and edit the courseware without being dependent on a large computer. This might possibly generate low quality courseware, but I feel many teachers could make good courseware who would not do so if a large (and probably less accessible) computer were required. People with experience in CAI could be of great assistance by publishing guidelines for writing good courseware along with methods of determining its quality.

Professor Gerhold presents a strong case for the use of PILOT instead of other languages for CAI; however, good courseware can be prepared using BASIC or other languages if that is all that is available to a particular user. I am using North Star BASIC and a Horizon II computer with 32 K bytes of programmable memory for computer aided instruction in soil physics at Oklahoma State University. Three BASIC programs were developed here to enter and edit courseware, process the courseware and interact with students and store their responses, and analyze student responses. The system is capable of performing complex matches of the kind described by Mr Gerhold (December 1978 BYTE, page 125) in one to five seconds, as well as jumping to specific parts of the courseware depending upon the student's responses to previous questions. Moreover it is very easy to create and edit courseware once the teacher has planned the material to be presented.

I hope to see more articles in BYTE relating to computer aided instruction on microcomputers. I would appreciate articles on software (such as PILOT), software and hardware required for preparing good courseware, methods of assessing the quality of courseware, and low cost video terminals with special features needed in instruction such as graphics, subscripts, and superscripts.

Asst Prof David L Nofziger
Oklahoma State University
Stillwater OK 74074

PASCAL COSTS ADD UP

I would like to respond to BYTEs comment on "Pascal Critique and a Comment," by J O'Loughlin (December 1978 BYTE, page 179). I feel that the UCSD Pascal system is *not* an affordable implementation of Pascal. Although the software costs "only" $200, you need 56 K bytes of programmable memory to use it productively ($800), plus 8 inch floppy disk ($1000), and a terminal with cursor control ($1000). Add this to a $1000 mainframe and this "affordable" system costs $4000. Compare this to a $600 TRS-80! Sure, Pascal is more readable than BASIC, but there are other con-

Text continued on page 223

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Enough about us. How about what computers do. To attempt to describe all the things your computer might do, would be to describe your imagination. So instead, we'll briefly list some of the many things for which small computers are already being used.

In business, the advent of the versatile and compact microcomputer has put the benefits of computing within reach of small companies. With systems starting at less than $6000, the businessman can computerize things like accounting, inventory control, record keeping, word processing and more. The net result is the reduction of administrative overhead and the improvement of efficiency which allows the business to be managed more effectively.

COMPUTERS FOR THE HOME

In the home, a computer can be used for personal budgeting, tracking the stock market, evaluating investment opportunities, controlling heating to conserve energy, running security alarm systems, automating the garden's watering, storing recipes, designing challenging games, tutoring the children . . . and the list goes on.

In industry, the basic applications are in engineering development, process control, and scientific and analytical work. Users of microcomputers in industry have found them to be reliable, cost-effective tools which provide computing capability to many who would otherwise have to wait for time on a big computer, or work with no computer at all.

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Computer Generated Maps, Part 1

William D Johnston
1808 Pomona Dr
Las Cruces NM 88001

Cartography, the art of mapmaking, originated in ancient times. It came of age in 1538 when Gerhard Mercator revolutionized the science with the introduction of the first modern mathematically derived map projections. Those projections, which bear his name, have stood the test of four and a half centuries, and to this day are of great value in a wide variety of applications. Many of the world's most famous cartographers lived, worked, and made great theoretical contributions more than 200 years ago. The names of Lambert, Mollweide, Lagrange, Gauss, and others will ring familiar to even the casual user of maps.

While these men all had brilliant minds, they shared an extraordinary handicap: that which they could conceive in theory they could put in practice only through enormous labor in manual computation. The construction of maps through mathematical projections begins with sets of geographical coordinates which define the boundaries of the areas to be mapped. These coordinates are manipulated with appropriate mathematical procedures to convert the geographical data to map coordinates, and these final numeric figures are used to draw the maps. In practice, accurate maps require defining literally tens of thousands, and frequently hundreds of thousands — or even millions — of reference points.

About the Author:

William D Johnston has worked in the fields of mathematics and computer systems since 1962. For the past ten years his professional position has been that of senior mathematician with primary responsibilities in computer graphics, user executives, and data reduction software for missile flight analysis. He built his first computer circuits (binary counters, ring counters, and half-adders) using vacuum tubes in 1959, the same year he received his amateur radio license.

Johnston has had articles in Sky and Telescope, Radio Communication, Ham Radio, QST, CQ, Ham Radio Horizons, RTTY Journal, *and other technical publications.*

It is no wonder that until recent times, these eminent scientists wasted years of their lives arduously computing complex mathematical conversions by hand. As recently as 20 years ago, it was still standard procedure in many government and private mapping agencies to create maps using nothing better than tables of precomputed conversion factors, between whose entries interpolation was required. The tables themselves had been computed manually, with the assistance of slide rules or mechanical calculators, at best. Over the years, cartographers frequently pointed out the need for various types of maps, and even developed the procedures for making them, but the manpower simply wasn't available to execute the task.

Now, with the power of the microcomputer, the rankest amateur can produce in minutes what might have taken Mercator or Lambert many years to accomplish. Not only can the mathematical computations be carried out on the microcomputer, but with a suitable graphics device the map itself can be drawn in final form. The practical applications are limitless. Such diverse fields as economic sector mapping for business, generating map overlays for direct reception of weather satellite photos in the home, aeronautical and maritime navigation, OSCAR satellite tracking for communications, topographic mapping, and celestial maps for astronomy are just a few of the many worthwhile applications.

For Space War fans, a vivid video graphics presentation of the changing Earth as seen from an orbiting spacecraft can add excitement to the game as battles rage over Antarctica, then shift to high above Europe, or wherever the Captain takes his ship. A whole new dimension can be added to such games as Battleship, when the combatants have the entire Pacific Ocean with all of its islands and atolls in which to maneuver, plan tactics, and try to outwit the enemy.

Classifications of Maps

The kinds of maps that you might generate on your own personal computer will depend upon the intended use, but, broadly speaking, map projections fall into two general categories: mathematical projections and perspective (or geometric) projections. Mathematical projections are defined by a mathematical function or procedure which will preserve or enhance the characteristics most important in the map's application. The Mercator map is a classic example of the mathematical projection.

Perspective projections are very much like perspective engineering drawings, which come under the category of perspective geometry. They are defined by, and may be created through, geometric constructions. (Perspective projections may also be described mathematically, but the converse is not true. Projections classified as mathematical cannot be defined geometrically.) A map made of the visible surface of the Earth, exactly as it appears from an orbiting spacecraft, is a perspective projection. The map outline overlays placed on weather satellite photos are common examples of this type of projection.

Ideally, a map should portray the Earth as it actually is, preserving both the shapes and the relative sizes of the areas being mapped. Distances throughout the map should be at a constant ratio to the actual distances on the Earth. For navigation and radio communication purposes, it would be convenient to have great circles on the surface of the Earth (which define the shortest distance between any two points) to appear as straight lines on the map.

Unfortunately, since the Earth is a sphere and maps are, of necessity, flat, it is impossible to incorporate *all* of these features into a single projection. Consequently, the various map projections are compromises selected to minimize the various distortions while enhancing other features, depending upon the particular application that the map is to be used for.

Any map which preserves the *relative sizes* of the areas portrayed is called an *equal-area* projection. Any map which preserves the *shapes* of the areas portrayed is said to be a *conformal* projection. In practice, if the error is no more than one or two percent, the map is considered to have met the requirements. A given map may be either conformal or equal-area, or it may be both, or it may be neither.

Hardware

The creation of maps by computer is exceedingly simple. The only hardware necessary is the computer itself, along with some type of graphics device. The graphics equipment may be a video display, or an X,Y pen plotter. If you are primarily interested in printed maps, then obviously a pen plotter (or a video display with hard copy attachment) would be your best choice. If, on the other hand, your first interest is in fast-changing maps for games, then a good video graphics display alone would serve quite well. Some dot matrix plotters can produce satisfactory maps, though often at a sacrifice in memory or mass storage I/O (input/output) time.

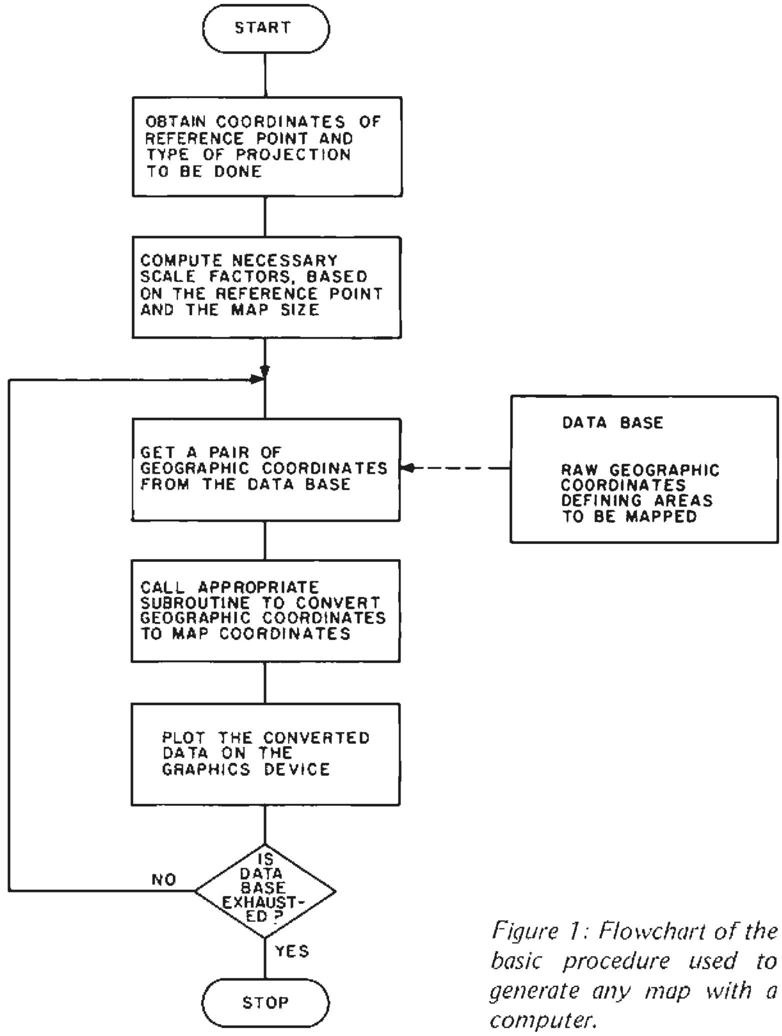

Figure 1: Flowchart of the basic procedure used to generate any map with a computer.

Map Generation Algorithms

One of the most appealing aspects of mapmaking by computer is the simplicity of the software. Figure 1 shows a flowchart of the fundamental procedure used to generate any map. The algorithm consists of a data base of raw geographic coordinates and a mathematical conversion procedure. Given a reference point (a point of projection or a set of mapping limits), the program loops through the conversion procedure, converting one pair of geographic coordinates to map coordinates each time, until the data base is exhausted. As each pair of map coordinates is computed, the information is used to draw that element of the map. If the program is to have the ability to generate several different projections, each projection conversion procedure can be written as a subroutine, and the appropriate subroutine would then be called at that point in the loop.

Most of the common projections, as we will see by the examples later, are defined by relatively simple mathematical equations. More often than not, the mathematical computations for a given conversion require no more than two to six statements in a BASIC program.

Data Base Requirements

As mentioned earlier, the data base consists of sets of geographic coordinates which describe the areas to be mapped. Since the map is generated by lines connecting the points, they must occur frequently enough to provide the desired resolution. The greater the resolution needed, the more data points required, and hence, the larger the storage requirements for the data base.

Of course if you are mapping the entire world, your data base will be much larger than if you are mapping, say, just the United States. Furthermore, the resolution of your graphics device, along with the scale factor of the finished map, sets an upper limit on both the number of data points and the angular resolution (that is, the number of significant digits) needed in the data base to secure the highest resolution possible with that particular device. The maps that accompany this article were generated from a data base that is far more extensive than most people would ever need. It consists of approximately 10,000 pairs of coordinates, sufficient to produce a satisfactory world map several feet (more than a meter) in diameter. The angular resolution of the latitudes and longitudes is 0.0001 radian, which is sufficient for maps down to a scale of 1:1,000,000 (ie: on the order of service station road maps).

The geographic coordinates (latitudes and longitudes) in the data base are almost universally stored in radians. The reason is that almost all map projections are computed by trigonometric formulas, and there is no sense having to convert the data base from degrees to radians every time the program is run.

Data Base Structure

The organization of the data base is straightforward. Each closed area represented by a continuous solid line which closes on itself is stored as a block of sequential coordinates (geographically sequential, that is). The last pair of coordinates in each block is the same as the first pair in the same block, so that the line drawn on the map will fully close. (Repeating the first pair of coordinates in this manner is not absolutely necessary, but it will save headaches later, at a very small cost in storage space.) Each of these blocks is separated by a flag – normally a pair of zeroes (ie: a zero for both the latitude and the longitude).

Islands which are so small as to require that only a dot be drawn for mapping purposes are grouped together into a single block. The program need know only the starting and ending addresses of that block so it can instruct the graphics device to draw only dots for these locations, rather than connecting them with lines. Political boundaries represented by dotted lines are handled in this same manner.

The size of your data base will determine whether it can be stored in main memory along with the program, or whether it will have to reside on a mass storage device. From the standpoint of computing efficiency, the ideal situation is to have it in main memory since this eliminates a tremendous amount of input/output (I/O) time. On the other hand, if the graphics device is relatively slow (as are many pen plotters), the lost I/O time will be masked by the time the computer spends waiting on the plotter, so no advantage is gained by using memory.

In cases where fast-changing maps are to be displayed on video display, programmable memory is definitely the best choice for locating the data base. Where sufficient main memory isn't available for the size of the data base in use, the data base can frequently be partitioned in such a manner as to permit the program to load portions of it from mass storage into memory at far less frequent intervals.

For certain special applications it has even been found advantageous to store data bases in read only memory. A number of amateur astronomers, for example, have stored the coordinates for the entire Messier catalogue of nonstellar objects, as well as limited star catalogues, in read only memory. The coordinates and catalogue numbers are used for both the real time control (pointing) of the telescope, as well as for generating star maps on the video display. Such applications of read only memory are generally limited to cases where the data base occupies no more than a few hundred bytes.

Compiling the Data Base

You can put together your own data base to fit your own particular requirements, if you have a mind to do so. Most libraries

Text continued on page 76

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Suddenly everyone is talking about personal computers. Are you ready for one? The best way to find out is to read Apple Computer's "Consumer Guide to Personal Computing." It will answer your unanswered questions and show you how useful and how much fun personal computers can be. And it will help you choose a computer that meets your personal needs.

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Representing Three-Dimensional Objects in Your Computer

Richard Blum
3 Mohawk Dr
Westboro MA 01581

How would you like to make still pictures "come to life"? Or perhaps draw or photograph objects and then animate them, on a video display? You can do it on your personal computer with the help of a data tablet and the program described herein. The program takes images from a data tablet and transforms them into a three-dimensional representation inside a computer.

Once a three-dimensional representation of an object is entered into a computer's memory, programs can be used to display the object in perspective on a graphical video display. The object can be displayed from an infinite variety of perspectives. One can look at objects from any desired viewpoint and generate different viewpoints rapidly — a capability that is very useful in animation.

Computer Animation

Animation with computers has several advantages over traditional animation techniques. First, a computer can draw faster than a person. In 16 millimeter films, 24 frames must be displayed every second. Thus a normal animation requires thousands of drawings. The speed of the computer can save the time required to draw the many pictures animation demands.

Second, a computer can quickly generate perspective drawings of objects. Perspective, the reduction in size of objects as they move further away from the viewer, gives pictures three-dimensional realism. Many cartoons do not use perspective drawings because of the time required to draw them. With the aid of computers, this realism in animation is easily achieved.

Third, computers can recreate the effects of wide angle or telescopic lenses, and can simulate lighting from any angle.

With all these effects at their disposal, artists have the potential to create realistic and exciting animation. To make computer animation available to artists not familiar with computer programming, there must be techniques which enable easy entry of visual data into the computer. This is made possible by the data tablet.

The Data Tablet

The data tablet is a graphical input device that enables the entry of visual images into a computer. Just as a keyboard enters alphanumeric characters (the elements of text), so a data tablet enters lines and points (the elements of images). Data tablets are now commercially available for personal computer systems. The Bit Pad™, manufactured by Summagraphics, is an example of a high quality data tablet available for personal computers.

In using the data tablet, a pen shaped stylus is moved over a flat electromagnetically sensitive board. The pen's position over the board is monitored by a controller which relays information to a computer. In this way it is possible to "draw" images directly into a computer's memory.

The tablet board is 11 inches square. Each point on the board represents a value in an X,Y coordinate system. Resolution is good, distinguishing as many as ten points per millimeter. There are three modes of operation. Data can be sent to the computer continuously, continuously while the stylus is touching the board, or at distinct moments while the stylus is touching the board.

Even if you are not interested in animation, you may still find it useful to manipulate images using a computer. A space game enthusiast could enter pictures of starships and then display them during the game. The homeowner needing to do some interior decoration could enter photographs of a room interior and furniture. Then different furniture arrangements could be viewed.

There are many other uses for a data tablet; only imagination is needed to discover them.

Preparing to Use the Picture Input Program

The program in listing 1 allows one to construct three-dimensional representations of objects inside a computer. These represensations will later be used to display the objects in perspective. The description of an object is entered using a data tablet, so that the process resembles drawing. For each side of the object entered, two pictures must be supplied. Either photographs or drawings may be used. The procedure described below assumes that photographs are used. If drawings are used instead, they must be prepared according to this procedure.

The two photographs must be taken such that they both center on the same point of the object (see figure 1). This point is to become the origin point. It is also necessary that the camera location for the second shot be directly behind where the camera was for the first shot, so that there is a straight line between the origin point and the center of the camera in both shots. Then the distance between the camera's positions should be measured. It is not necessary to know how far the camera was from the object, but only to know the difference in camera position. The only other measurement necessary is the X,Y,Z distance between the origin and one vertex on the object.

It is also necessary that the lens' effective focal length does not change between the two photographs. This may be achieved by using the same focus setting with a very small aperture, or more simply by using a

Photo 1: Two views of side view 1.

Photo 2: Two views of side view 2.

Listing 1: BASIC program for entering and manipulating data from a data tablet.

```
0010    LET X1=1
0020    REM (THIS PROGRAM ACCEPTS DATA FROM A TABLET AND TERMINAL)
0030    REM (AND CREATES THREE DIMENSIONAL MODELS OF THE OBJECTS ENTERED)
0040    REM X,Y,Z COORDINATES
0050    DIM X[100],Y[100],Z[100]
0060    REM X,Y,Z DISPLACEMENTS FROM SIDE 1'S ORIGIN
0070    DIM X9[6],Y9[6],Z9[6]
0080    REM INITIALIZE TOTAL NUMBER OF VERTICE TO 0
0090    LET I3=0
0100    PRINT "HOW MANY SIDE VIEWS ARE TO BE ENTERED"
0110    INPUT S1
0120    REM ENTER THE POINTS FROM EACH SIDE VIEW
0130    FOR S=1 TO S1
0140       PRINT "PROCESSING SIDE VIEW",S
0150       GOSUB 0230
0160    NEXT S
0170    OPEN FILE[1,1],"RESULT"
0180    FOR I7=1 TO I3
0190       PRINT FILE[1],I7,X[I7],Y[I7],Z8  Z[I7]
0200    NEXT I7
0210    CLOSE FILE[1]
0220    END
0230    REM (FIND THE USERS ORIGIN)
0240    PRINT "PLACE THE STYLUS ON THE ORIGIN FOR PICTURE 1"
0250    CALL 1,01,02
0260    PRINT "PLACE THE STYLUS ON THE ORIGIN FOR PICTURE 2"
0270    CALL 1,03,04
0280    PRINT "HOW FAR WAS CAMERA ONE FROM CAMERA TWO"
0290    INPUT L
0300    REM (FIND THE KNOWN VERTEX)
0310    PRINT "PLACE THE STYLUS ON THE KNOWN VERTEX IN PICTURE 1"
0320    CALL 1, K1, K2
0330    REM (TRANSFORM DATA TO THE USERS TABLET SPACE)
0340    LET K1=K1  01
0350    LET K2=K2-02
0360    PRINT "PLACE THE STYLUS ON THE KNOWN VERTEX IN PICTURE 2"
0370    CALL 1, K3, K4
0380    LET K3=K3-03
0390    LET K4=K4-04
0400    PRINT "ENTER THE X  Y-Z DISTANCES BETWEEN THE KNOWN VERTEX AND ORIGIN"
0410    INPUT V1,V2,V3
0420    REM (CALCULATE THE DISTANCE BETWEEN CAMERA ONE AND THE OBJECT)
0430    IF K1-K3=0 THEN GOTO 0460
0440    LET Z=(K3*L)/(K1-K3)
0450    GOTO 0500
0460    LET Z=(K4*L)/(K2-K4)
0470    REM (CALCULATE THE PERSPECTIVE TRANSFORM)
0480    LET D = Z * K2 / V2
0490    GOTO 0510
0500    LET D=Z*K1/V1
0510    IF S - 1 THEN Z8 = Z
0511    PRINT "HOW MANY VERTICES ARE TO BE ENTERED?"
0520    INPUT I1
0530    FOR I=1 TO I1
0540       IF S -1 THEN GOTO 0570
0550       IF I -S1 THEN GOTO 0570
0560       PRINT "VERTEX COMMON TO SIDE VIEW",I+1
0570       PRINT "IN PICTURE ONE POINT TO VERTEX",I
0580       CALL 1, X1, Y1
0590       PRINT "IN PICTURE TWO POINT TO VERTEX",I
0600       CALL 1, X2, Y2
0610       REM (CALCULATE THE X- Y COORDINATES FOR THE VERTEX)
0620       LET D1-X1-X2
0630       IF D1-  -0 THEN GOTO 0660
0640       LET Z [I + I3] = (Y2 * L) / (Y1 - Y2)
0650       GOTO 0670
0660       LET Z[I+I3]=(X2*L)/(X1 -X2)
0670       LET X[I+I3]=Z[I+I3]*X1/D
0680       LET Y[I+I3]=Z[I+I3]*Y1/D
0690       REM IF THIS IS THE FIRST SIDE FIND COMMON VERTICE
0700       IF S -1 THEN GOTO 0790
0710       REM IF WE HAVE FOUND ALL THE COMMON VERTICE LOOP AGAIN
0720       IF I -S1 THEN GOTO 0830
0730       LET X9[I+1]=X[I+I3]
0740       LET Y9[I+1]=Y[I+I3]
0750       LET Z9[I+1]=Z[I+I3]
0760       GOTO 0830
0770       REM PROCESSING A SIDE VIEW OTHER THAN SIDE ONE
0780       REM IF THIS IS FIRST VERTICE ITS A COMMON ONE
0790       IF I-1 THEN GOSUB 0870
0800       LET X[I+I3]=X[I+I3]-X9[S]
0810       LET Y[I+I3]=Y[I+I3]-Y9[S]
0820       LET Z[I+I3]=Z[I+I3]-Z9[S]
0830    NEXT I
0840    REM FIND TOTAL NUMBER OF VERTICE
0850    LET I3=I3+I1
0860    RETURN
0870    IF S=1 THEN GOTO 0920
0880    REM FIND THE DIFFERENCE BETWEEN SIDE ONE AND SIDE N
0890    LET X9[S]=X[I+I3] -X9[S]
0900    LET Y9[S]=Y[I+I3] -Y9[S]
0910    LET Z9[S]=Z[I+I3] -Z9[S]
0920    RETURN
```


Sol Terminal Computer

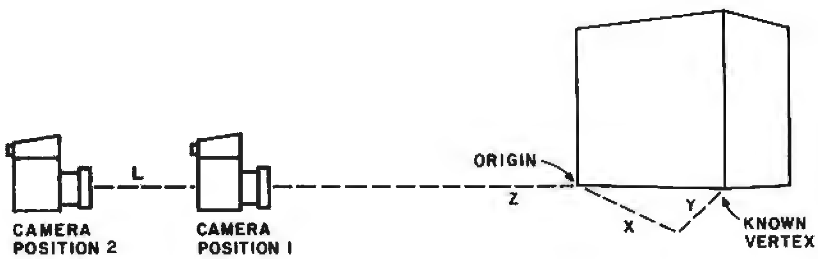

Figure 1: To analyze perspective, two pictures of each side must be taken from two different distances. The line of sight through both cameras should be in line with a point on the object.

fixed-focus camera. Under a discussion of theory there is a description of another technique, in which there is no restriction of constant focus.

Enlargements of the photographs should be made to make measurements more accurate. I have found that there are always errors in reading values from photographs; the smaller the photographs, the larger the error ratio.

Using the Picture Input Program

With photographs and measurements, the user is ready to run the picture input program. To illustrate the use of this program, a simulated run will be described. For this simulation a simple object was photographed (see photos 1, 2, 3 and 4), and measurements taken. Four photographs were needed to represent two side views. (Note that for this object only two side views are necessary to see all the vertices.)

In figure 2 each vertex of the object is associated with a letter. Table 1 gives the values of the coordinates measured from the four photographs. These measurements are provided to illustrate the simulation. In a normal run of the program these values would be provided to the program directly from the data tablet.

The picture input program, written in BASIC, receives the information from the data tablet by making use of the BASIC CALL statement. The CALL statement activates an assembly language routine which handles the interface to the data tablet. This routine, not included here, must be supplied by the user.

The simulation begins by having the program prompt with the question:

HOW MANY SIDE VIEWS ARE TO
BE ENTERED ? 2

In this example there are two side views.

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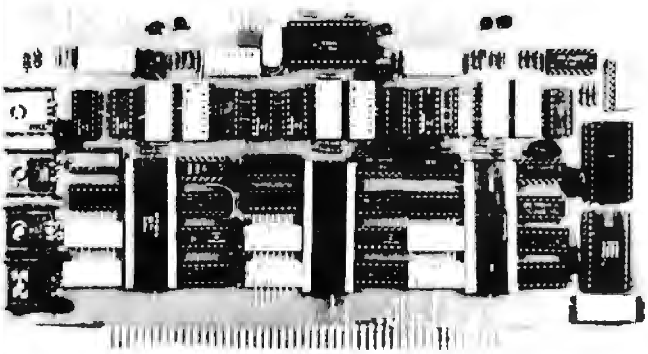

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The program next states:

READY TO PROCESS SIDE VIEW NUMBER 1.

At this time the user should put the two photographs of side view 1 onto the data tablet. The program tells the user:

PLACE THE STYLUS ON THE ORIGIN IN PICTURE ONE.

The user should find the location of the origin in the photograph and indicate it with the stylus. In this example it is point O. Knowing this point allows the program to relate the data tablet's coordinates to the photograph's coordinates. The same is asked for picture 2:

PLACE THE STYLUS ON THE ORIGIN IN PICTURE TWO.

In preparation for the program, the user should measure the distance between the two camera positions. In this example the distance was 26.7 inches.

HOW FAR WAS CAMERA ONE FROM CAMERA TWO ? 26.7

The program next needs to know where in the photograph the vertex whose distance to the origin has been measured lies. This point should be located twice. Once in response to:

PLACE THE STYLUS ON THE KNOWN VERTEX IN PICTURE ONE;

and once in response to:

PLACE THE STYLUS ON THE KNOWN VERTEX IN PICTURE TWO.

Vertex 1 is the known vertex. From table 1 we see that values (0,43.1) and (0,28.2) would be the values provided by the tablet. In preparing for the program, the distance between the origin and vertex 1 was measured. In X,Y,Z terms this distance is (0,11.75,0). This value should be entered in response to:

ENTER THE X,Y,Z DISTANCE BETWEEN THE KNOWN VERTEX AND THE ORIGIN: (0,11.75,0).

If more than one side view is to be entered, the other side views must somehow be related to the first coordinate system. This is done by finding points in the first side view which are also in other side views (see figure 3). Therefore, the program will ask the user to point to a vertex in side 1 which is also in side N. The first N vertices pointed to in side view 1 should be vertices which are also in other side views. That is, the first vertex in side view 1 should be a vertex which is also in side view 2. The second vertex pointed to in side view 1 should be a vertex found in side view 3, etc. (The program as presented in listing 1, for the sake of simplicity, assumes that only two side views are necessary, and that these side views are opposite (180°) to each other. For most objects these will be sufficient.)

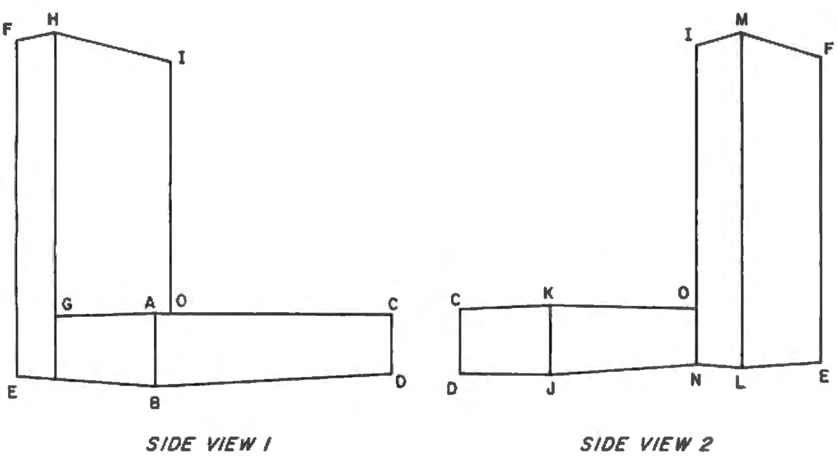

Figure 2: Each of the vertices of the object is given a designation letter.

	Side View 1			
	Picture 1		Picture 2	
Vertex	X	Y	X	Y
A:	− 3.3	0	−2	0
B:	− 3.3	−12.3	−2	− 7.6
C:	40.1	0	26	0
D:	40.1	−10.6	26	− 6.7
E:	−25.5	−10.6	−16.6	− 6.9
F:	−25.5	44.5	−16.6	28.9
G:	−19.4	0	−12	0
H:	−19.4	47	12	30
I:	0	43.1	0	28.2
	Side View 2			
	Picture 3		Picture 4	
C:	39.9	0	25.6	0
J:	25	−11.8	15.6	− 7.3
K:	25	0	15.6	0
L:	− 7.4	−10.9	− 4.7	− 7
M:	− 7.4	45.9	− 4.7	28
N:	0	−10.5	0	− 6.8
I:	0	43.8	0	28.3

Table 1: A compilation of the data obtained from photos 1 and 2. The vertex designations are the same as in figure 2. For photos 1a and 1b, L is 26.7 inches (67.8 cm) and the known vertex is I at location (0,11.75,0) inches (0,29.85,0) cm. For photos 2a and 2b, L is 27.3 inches (69.34 cm) and the known vertex is I at location (0,11.75,0) inches (0,29.85,0) cm. The common vertex to side views 1 and 2 is vertex C.

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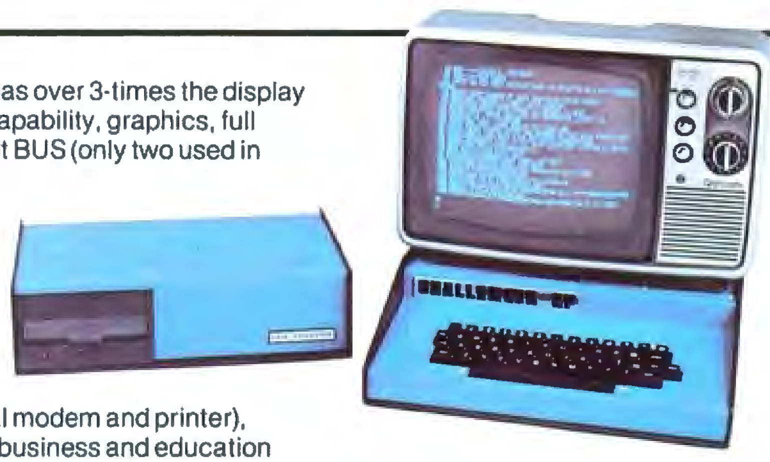

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All that remains is to point to a vertex in picture 1 and then again to that vertex in picture 2, and to continue until all of the vertices in that side view have been pointed out. The program will ask:

HOW MANY VERTICES ARE TO BE ENTERED : 8

Eight is the answer for the first side view of this simulation. Then the program will ask:

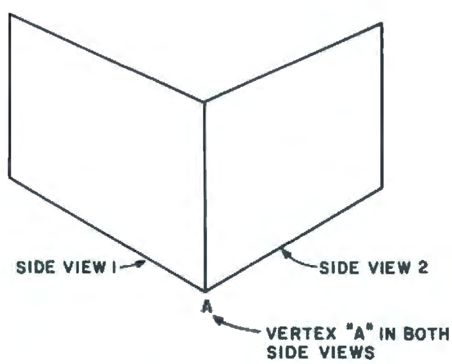

Figure 3: When processing two different views, at least one point must be common to two views. In this example, vertex A is seen in both side views.

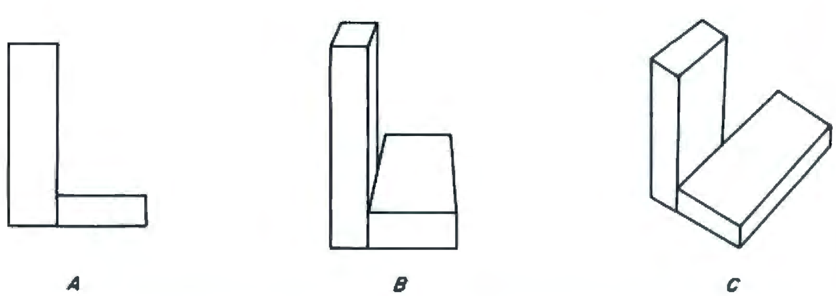

Figure 4: Three pictures drawn using data generated by the program in listing 1. The original information was obtained from photos 1 thru 4.

Results				
Vertex	Number	X	Y	Z
C:	1	10.7	0	1.3
A:	2	− 0.7	0	9.5
B:	3	− 0.7	− 2.7	9.5
D:	4	10.7	− 2.8	1.3
E:	5	− 6.9	− 2.8	0.7
F:	6	− 6.9	12	0.7
G:	7	4.5	0	7.2
H:	8	4.5	11	7.2
C:	9	10.6	0	1.3
J:	10	6.3	− 2.9	−4.9
K:	11	6.3	0	−4.9
L:	12	− 1.9	− 2.8	−2.3
M:	13	− 1.9	11.7	−2.3
N:	14	0.1	− 2.8	0

Table 2: Conversion of the measured data from table 1 into three-dimensional coordinates.

IN PICTURE ONE POINT TO VERTEX N;

and

IN PICTURE TWO POINT TO VERTEX N.

For example, the first vertex pointed to is the common vertex. C is the common vertex in our simulation, so it is indicated first in picture 1 and again in picture 2. The data tablet provides the values (40.1, 0) and (26, 0). Then vertex A is pointed to in picture 1 and picture 2. Values (−3.3, 0) and (−2, 0) will come from the data tablet. This continues until all of the vertices of a side view have been entered.

When it is time to process another side view, the program will say so, asking for the same information as it did in side view 1 (eg: where the origin and known vertex for this side view are, what are the measurements for the known vertex, and what was the distance between camera positions). Next, the different vertices should be pointed to, starting with the vertex common to side view 1.

When the program is finished, all the coordinates of the vertices will have been converted to three-dimensional coordinates, and represented inside the computer. Table 2 contains the results from this simulation.

Displaying the Object

With these results the object can be displayed from any desired viewpoint. For example, let us say that two side view pictures were taken such that the directions of the pictures were perpendicular to each other. It would be quite simple to display the object from a viewpoint between those from which the photos were taken, even though no picture was taken from such a position. Figure 4 shows examples of different viewpoints of the object photographed. These figures were developed mathematically, using the results of the picture input program, in the same manner that they would be developed by a program which displays objects three-dimensionally. Starting with just a few photographs, many such pictures of an object can be made.

Some Theory

How is it possible, that from two photographs of one side of an object, all of that side's dimensions can be calculated? To answer this question, let us first examine the way in which perspective pictures are displayed. For simplicity, we will assume that

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the outline of an object consists of straight edges which meet at vertices. Rounded edges are approximated by several straight edges. Putting an object into perspective entails transforming the edges' three-dimensional coordinates into two-dimensional coordinates. Internally, the computer represents the objects' edges as pairs of vertices. Since straight lines in three dimensions get transformed to straight lines in two dimensions, all that is necessary is to transform coordinates of their endpoints.

The screen of a video display device is two-dimensional. We will call this plane the picture plane (see figure 5). Putting an object into perspective involves drawing straight lines between the object and an imaginary viewer. The imaginary picture plane is also inserted between the viewer and the object. The objects' vertices are projected to where the lines adjoining object and viewer intersect the picture plane. These points of intersection can be computed using similar triangles. Triangle ABC is similar to triangle ADE. The equation for a perspective transform is therefore:

$$XP = DP(X)/Z \qquad YP = DP(Y)/Z$$

where the X,Y, and Z directions are as defined in figure 5:

XP = X coordinate in picture
YP = Y coordinate in picture
DP = distance between viewer and picture plane
X = vertex's X coordinate
Y = vertex's Y coordinate
Z = distance between vertex and viewer.

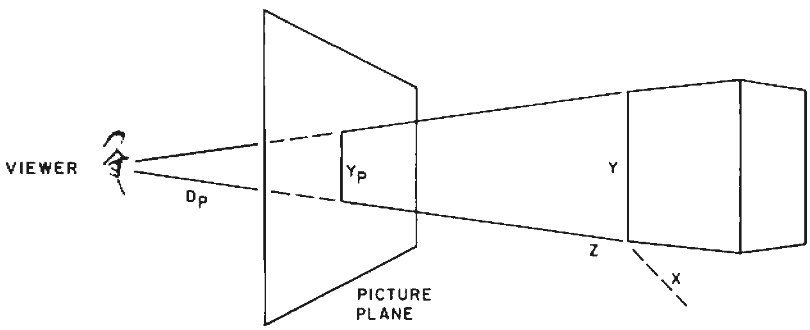

Figure 5: The viewing screen can be considered as the picture plane to be viewed. Putting an object into perspective involves drawing straight lines between the object and an imaginary viewer.

The location of the picture plane with respect to the viewer determines the angle of vision. If the picture plane is close to the viewer, there is a wide angle effect. If the picture plane is far from the viewer there is a telescopic effect (see figure 6). The term DP in the above equations is that distance, and it is referred to as the *perspective transform of the lens* of the camera.

The object is displayed according to the values put into several equations. We know that the distance between camera and object is given by term Z, and that the angle of vision is given by term DP. To achieve rotation of the object, we use the equations below:

$$XR = X \times \cos(\text{angle } 1) - Y \times \sin(\text{angle} 1)$$

$$YR = X \times \sin(\text{angle } 1) + Y \times \cos(\text{angle} 1).$$

By rotating the object around two axes, any angle of rotation in three dimensions can be achieved.

$$YR1 = YR \times \cos(\text{angle } 2) - Z \times \sin(\text{angle} 2)$$

$$ZR = Z \times \cos(\text{angle } 2) + YR \times \sin(\text{angle} 2).$$

Perspective is arrived at by applying the original transform equations:

$$XP = DP(XR)/ZR$$
$$YP = DP(YR)/ZR.$$

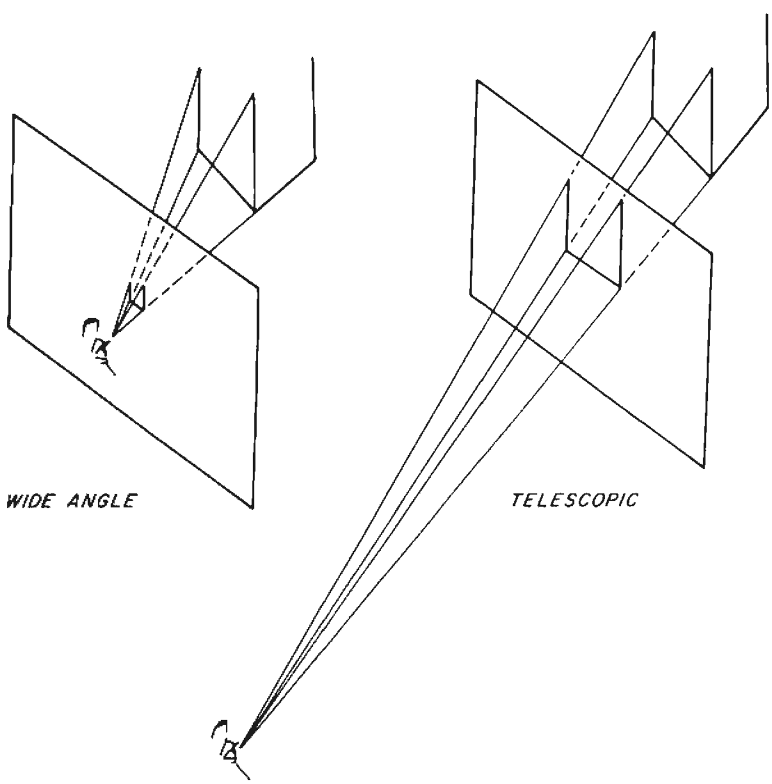

Figure 6: The location of the picture plane determines the angle of view. A wide angle effect is produced by having the plane close to the viewer. A telescopic effect is produced by a picture plane far from the viewer.

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A camera is a device which produces a perspective transform. The procedure with the photographs and data tablet is to reverse the transform to produce the three-dimensional coordinates of the vertex. From the equations above, we see that there are five variables. The photographs give us values for XP and YP. If DP and Z are determined, values for X and Y can be computed. It can be assumed that DP in one photograph will be the same as DP in another photograph, as long as the angle of vision does not change. With two photographs taken with camera positions one behind the other, and with the distance known between positions, we have two sets of perspective transform equations and a relationship between Z in one photo to Z in the other photo:

$$XP1(Z1) = DP(X) \quad (1)$$
$$XP2(Z2) = DP(X) \quad (2)$$
$$YP1(Z1) = DP(Y) \quad (3)$$
$$YP2(Z2) = DP(Y) \quad (4)$$
$$Z2 - Z1 = L\,. \quad (5)$$

Subtracting equation 2 from equation 1 and substituting $Z2 = L + Z1$:

$$XP1(Z1) = XP2(L + Z1) \text{ or}$$
$$Z1 = XP2(L) / (XP1 - XP2)\,. \quad (6)$$

Therefore, to learn how far the camera was from a vertex, all we need to know is the distance between camera positions.

Finding DP, the perspective transform, requires the knowledge of the coordinate in either the X or Y direction for one known vertex. For example, with a value for X known and a value for Z obtained through the use of equation 6, we can write an equation for DP as:

$$DP = Z(XP)/X\,. \quad (7)$$

Once a value for DP is obtained, values for X and Y are computed using the Z values computed and the equations:

$$X = Z\,(XP)\,/\,DP \quad (8)$$
$$Y = Z\,(YP)\,/\,DP. \quad (9)$$

Now every vertex's three-dimensional X,Y, and Z coordinates can be determined. These coordinates are given with respect to the edge of the camera. To orient them with respect to the origin, subtract the distance between origin and camera from each computed Z value. The first side of the object is now described three-dimensionally, independently of a viewing point or picture plane.

To describe other sides of the object, the above equations must be applied again. Also, two photographs taken as above, an origin, one known vertex, and an additional vertex common to both side views must be supplied. This additional common vertex will be used to relate the values obtained in one side view to the values obtained in the other side view (see figure 3). Once all of the values are computed for the second side, the differences are found between values computed in view one from values computed in the other view for the common vertex. These differences in value are the offsets from one side's coordinate system to the other side's coordinate system.

If these values are subtracted from one side's values, all vertices will be in relation to one origin. If this procedure is applied to all sides, the entire object is described. With the aid of your computer you can now display the object from any perspective you choose. You are not limited to the perspective of the photographs, and you can have the object placed at any distance or angle of rotation you like.

Another Input Method

There is another technique for entering three-dimensional information from photographs into a computer. This technique is useful in cases in which, rather than measuring between the camera positions and the object, it is easier to measure the positions of several points on the object. For example, you may be taking a picture of a house, and have no convenient way to measure the distance between the camera and the house. Yet it may be quite simple to measure the dimensions of a window frame. In this technique, rather than measure the distance between camera and object, the user measures two vertex coordinates in reference to a third vertex which is to serve as the origin.

The distance between object and camera need not be known, but the camera must point so that the origin of the object is in the center of the photos. Again, two photos are required. They should be taken parallel to each other, rather than taken one behind the other. Each photograph will have its own origin, and it is necessary to know the distance between the camera's positions, or distance between origins. Three vertices from one photograph yield three equations:

$$Z1 \times XP1 = X1 \times DP$$
$$Z2 \times XP2 = X2 \times DP$$
$$Z3 \times XP3 = X3 \times DP.$$

Measurements of the object give X1,X2,X3, Z1,Z2, and Z3. Measurements of the photograph give XP1,XP2, and XP3. We can substitute the differences for the Zs with Ls:

$$L1 = Z2 - Z1$$
$$L2 = Z3 - Z1$$
$$Z1 \times XP1 = X1 \times DP$$
$$Z1 \times XP1 = Z1 \times DP$$
$$(L1 + Z1) \times XP2 = X2 \times DP$$
$$(L2 + Z1) \times XP3 = X3 \times DP\ ;$$

and subtract the bottom equations from the top equations:

$$Z1 = \frac{(DP \times (X1 - X2)) + (L1 \times XP2)}{(XP1 - XP2)}$$

$$Z1 = \frac{(DP \times (X1 - X3)) + (L2 \times XP3)}{(XP1 - XP3)}$$

and solve for DP.

$$DP = \frac{((XP1-XP2) \times (LP2 \times XP3))-((XP1-XP3) \times (L1 \times XP2))}{((X1-X2) \times (XP1-XP3))-((X1-X3) \times (XP1-XP2)).}$$

Once DP is solved for, Z1 can be found for any vertex by using the two photographs' equations and knowing the distance between camera positions:

$$X1 = (Z1 \times XP1)/DP$$
$$X2 = (Z1 \times XP2)/DP$$
$$Z1 = (XP2 - DP)/(XP1 - XP2).$$

Of course with Z1 determined X1 and Y1 can easily be found:

$$X1 = (Z1 \times XP1)\ /\ DP$$
$$Y1 = (Z1 \times XP2)\ /\ DP.$$

To enter data from the tablet with this technique, first indicate through a keyboard the values for the three known vertices, and then point to them in one photograph. This would allow the program to compute DP. Then, as in the other technique, point to a vertex in one photograph, and again to that vertex in the other photograph. More sides can be added, and eventually the whole object will be described.

There are additional techniques for entering three-dimensional data. For example, photographs may be taken with added amounts of rotation. This is particularly true in cases in which the user cannot take actual photographs, but has some means of determining a few dimensions of the object. In these cases, the angles of rotation must be calculated in addition to DP, X, Y, and Z. Because the mathematics for solving the equations with rotation is more involved than the equations in this article, I have not discussed it here, except to mention that for each angle of rotation one more known value, a vertex coordinate, needs to be known before the equations can be solved.■

Technical Forum

M6809 is Silicon

Technical Forum is a feature intended as an interactive dialog on the technology of personal computing. The subject matter is open-ended, and the intent is to foster discussion and communication among readers of BYTE. We ask that all correspondents supply their full names and addresses to be printed with their commentaries.

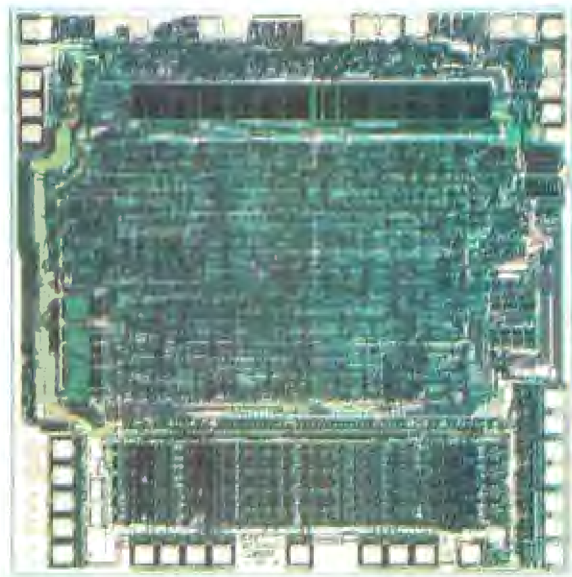

Photo 1: A look at the 6809 device.

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Austin TX 78721

In our recent article, "A Microprocessor for the Revolution: the 6809" (January, February, March 1979 BYTE), we tried to indicate that the specification, logic design, layout, and testing of a new microprocessor is a very big job. Throughout the project we were quite aware of the potential market for this new part, and the entire microprocessor design team made Herculean efforts to get it out as quickly as possible. The big push finally came down to getting the design ready for the mask shop before Christmas 1978 (we wanted to enjoy the holiday).

Every metal line, every polysilicon line, every connection, and every transistor in the entire layout had to be individually hand checked. A checking team consists of two individuals. The first member, and leader, is a circuit engineer who can read the layout to identify transistors, verify their logic function and size, and trace the connections between them. The second engineer monitors the checkout process on a logic-diagram blueprint, coloring each line and each gate as it is checked. This process continues until all gates and all lines are colored and until all paths are investigated on the layout. Uncovered errors are edited, replotted, and rechecked. The 6809 layout (with about 15,000 transistors) was completely hand checked three times in the last two weeks before Christmas 1978, in addition to sophisticated computer spacing checks.

Our EXORciser II based test system had been working for weeks with the 6809 breadboard (a gate-for-gate transistor-transistor-logic equivalent of the 6809). The working system had the new EXBUG09 monitor, and would run all our 6809 programs, including an

18,000 line diagnostic package. This program checks all registers, instructions, addressing modes, and numerous combinations. Correct execution provides a characteristic pattern of address positions as displayed on the logic analyzer.

We disconnected the breadboard, popped the first 6809 into the socket and started testing parts at 7:30 PM on Tuesday, January 9 1979. None of the devices worked the first time, but we did get two that failed in exactly the same way. This is one of nature's hints. Naturally, we were disappointed that none of the parts passed all tests, but we knew the complexity involved in an LSI (large scale integration) device.

After you have checked 5,000 gates they all tend to look alike, especially at 3 AM. All conductors look the same—there is no color coding on an integrated circuit. It is all too easy to miss a wrong connection, a shorted transistor, a floating gate, or any one of many possible errors. Thus, virtually all LSI devices require a sequence of mask iterations before a fully functional device is obtained. As weak areas are pinpointed by testing, new masks are obtained to improve yield. But the Motorola microcomputer design group has a history of producing functional, or nearly functional parts the first time, hence our disappointment.

Resigned to the worst, we proceeded to write programs to narrow the error to a particular instruction or sequence of instructions, and hopefully to a particular gate. After an hour of machine language testing, it became apparent that the error was random, not instruction dependent, and possibly parametric. That is, the malfunction was responsive to clock frequency, supply voltage, or operating temperature parameters.

Finally, the Microcomputer Design Manager picked up a heat gun and trained it on one of two suspicious devices. Everyone was transfixed, watching the logic analyzer with renewed hope. There was one false start, then the 6809 made it once through all tests. More heat, and the 6809 was running all 18,000 lines of test code over and over again. Pandemonium broke loose, with cheers and congratulations all around.

After some investigation, the minor temperature sensitive problems were identified, and masks were modified to produce customer samples... and Motorola is now in the 6809 business. ■

Ciarcia's Circuit Cellar

Photo 1: Example of an optical fiber transmitting a very bright light. The conductor is a single 40 mil plastic fiber. The light is generated by a helium-neon laser.

Communicate on a Light Beam

Steve Ciarcia
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Coming up out of the Circuit Cellar is a rare occurrence, to the point where some of my friends have accused me of being a mushroom. I prefer to be likened to a mole–a more dignified species. We share a common bond of subterranean existence and fear of bright sunlight, but the mole's predicament is dictated by nature, and mine by choice.

The Circuit Cellar is by no means a hole in the ground. It's heated, well-lit and looks more like a living room than a cellar. Even though it affords all the comforts of home, there are those occasions when a change of environment is required. It's not enough to walk out in the driveway, take a deep breath and run back into the cellar. Sometimes a complete change of surroundings is needed to shock the mind out of the doldrums and spark creativity (eg: a vacation). Since I usually don't have time for vacations, I take "business excursions for purposes of cerebral detoxification" or "ECDs" for short.

For two months I had been wrestling with the details of an article on fiber optics and laser communications (this one). The hardware was completed very quickly, as with most of my projects, but the text dragged on for weeks. Lighting the wood stove in the Circuit Cellar became an all too easy chore using the piles of scrap paper I was generating. My graphospasms (ie: writer's cramps) were not bearing fruit. One time I even found myself sitting at my desk pushing pencils through the electric pencil sharpener until it started smoking.

During times like this there was only one place to go – New Hampshire – to see the Colonel. My father-in-law, Colonel Foster, was the one person who could break me out of this slump. Between stories about old army buddies and spending the war in the Aleutians waiting for an invasion I would surely find some inspiration.

"Colonel? Are you there?" After anxiously dialing his telephone number and saying hello, I was left with silence at the other end of the line. . .

"Colonel?"

"Be right with you, Steve." As the receiver was picked up again he apologized, "Sorry Steve, my man was at bat and I had to see the hit. You're a Red Sox fan, aren't you?"

It would be in bad taste for me to suggest that my subterranean hideaway provided all the spiritual stimulation I needed and that chasing a little ball around in the grass was not in my spectrum of pursuits.

"I quite understand your enjoyment of the game, Colonel. I hope your team wins," I replied, evading his question. During my statement I heard him roar again in response to the activities on the television. When I sensed a lull, possibly precipitated by a commercial, I continued, "Colonel, I need to get away. How would you like some company tonight?"

"Sure, you know you're always welcome. I haven't had anyone to tell a good army story to in a long time."

I told him I'd pack all the gear in the car and be there in three hours. Possibly I would feel better about writing once I arrived.

The Colonel, sensing the termination of the commercial, quickly responded, "Three hours is great. The game is still in the first inning. If you hurry you may get here before it's over. . .gotta go now."

One of the good things about living in New England is that everything is close. It was a scant 3 hour drive between Connecticut and New Hampshire, but I dragged it out an extra half hour so I wouldn't be competing with the Red Sox for the Colonel's attention. As I pulled into the garage he came out to greet me.

"Howdy," he said, slapping me on the back. From his exuberance I could tell that the Red Sox had just won the game.

"Come on in and get settled. I'm expecting a telephone call. . .oops, there it is now."

Leaving the electronics junk in the car I followed him into the house. He was still wearing his lucky Red Sox baseball cap as he spoke.

"Chester, wasn't the game great? I thought they were going to blow it in the 6th. . .You bet, I'm ready for tomorrow's game. If they can play like that again, the pennant is in the bag. . ."

Suddenly Colonel Foster's expression changed, to amazement, then anger. He grabbed his cap, slung it into the chair he was standing near and complained, "Darn woman again!. . .What do you mean lucky! The Red Sox won through skill, not luck!. . .Go play with your WATS lines and let Chester and me talk." It was obvious that suddenly there was a third party to their conversation.

"Beatrice, I don't care if you think it was an error. It was ruled as a single!. . . Yes, I know the 6th looked bad but that still doesn't mean they're just lucky. . ."

It was becoming an argument between the Colonel and Beatrice. A hint as to her identity was provided when he responded, "Beatrice, would you keep your opinions to yourself and let me talk to Chester? Chester, come on over for a private talk!"

He slammed the reciever down on the phone, put his baseball cap back on, and slumped into the easy chair. "I just can't carry on a baseball conversation with that woman around."

"Who's Beatrice?"

"The switchboard operator for the town. We don't have all that new computer telephone stuff you city slickers have. We have Beatrice. When it's business or personal she's good and keeps her nose out. But, when it's baseball, Beatrice has to get her two cents in!"

(Obviously what the Colonel and Chester needed was an alternate means of communication, such as CB.)

"I've got a great idea, Colonel. Why don't you and Chester use CB radios instead of the telephone?" The Colonel led me to the bookcase in the study. I found myself staring directly at a CB radio. He flipped it on and said, "Tune in channel 19 and listen." The radio came to life. "Breaker one nine. . .breaker one nine. . . this is your Big Mama on this one niner. . . all you 18 wheelers just put the hammer to the floor and let Big Mama be your guide. . .I'll have a Smokey report in five, but first, the weather. . ."

My eyes opened wide. "Is that Bea. . ."

"Beatrice? You're darn tootin' it is. She's got an antenna tower on her house and radio gear that would put an FCC test laboratory to shame. I swear she's running a full gallon."

"We tried CB a while back and it was useless." This time the conversation came from behind. Chester had let himself in and joined us in the study. He continued, "It all started when we telephoned the games to the tower."

"Tower?"

"I'm sorry, I guess the Colonel didn't tell you." Walking over to the window of the study and pointing to the adjacent mountain top roughly two miles away. "You see that structure on top of that hill? That's my tower. Well, not exactly *my* tower. I just work there. It's a combination fire tower and radio relay station. Occasionally I have to sit up there and monitor equipment during important transmissions.

"What's that got to do with Beatrice?"

"With all the interference from the equipment up there I can't use a radio or television to watch the Red Sox."

(This was beginning to take on the aspects of a good mystery.)

"The Colonel would tune in the game on his television set here, telephone me in the tower and then lay the receiver near the television so I could listen to the game. When Beatrice found out she'd bust in and add her commentary to the game. Do you know what it's like having a nosey Howard Cosell-type beating on your ear for three hours at a time?"

I could only offer my sympathy. If there was a solution short of stringing two miles of wire I didn't see it yet. But I would continue to think about it.

"Tomorrow is a very important Red Sox game. The pennant may hinge on it.

Text continued on page 36

Warning: *due to the nature of lasers, any prolonged skin contact or viewing of the laser beam is hazardous.*

We've worked like mad to

Text continued from page 33:
Unfortunately, tomorrow is also a day I have to spend in the tower. I really want to listen to the game, but Beatrice is tough to listen to."

I ran over to the window, looked at the tower in the distance, and noted the glass windows circling the observation deck. "What's the weather report for tomorrow?"

"Cloudy and cool I think." Chester answered.

"Good! Clear weather. . .Colonel, could the television set be moved in this room for the game tomorrow?"

"I suppose so. Why?"

I scanned the study looking for a convenient AC power outlet and spied one by the window.

"Perfect," I said.

Both the Colonel and Chester were a little perplexed at my behavior.

"What if I told you there was a way for Chester to listen to tomorrow's game undisturbed by Beatrice?"

"We've tried everything. What are you planning?"

"Wait here and I'll show you." I dashed off to my car and took a tripod, a long white rectangular instrument, a small black box with a lens at one end and a few patch cords out of the trunk. Dragging all the equipment into the study, I proceeded to assemble it, much to their amazement.

"What's all this, Steve?" the Colonel asked.

With as straight a face as I could muster I replied. "It's a laser."

Both men, army veterans of two wars and thirty years' service, took two steps back and exclaimed, "A laser?" It was instantly apparent that the words laser and "death ray" were synonymous for them. Before I let them think I planned to rub out Beatrice, I quickly continued my explanation.

"There are big lasers and little lasers. This is a little one. It won't burn anything or hurt anyone if used properly. Eye protection is the only consideration necessary on this particular laser."

"Do you always carry this stuff around with you?" the Colonel asked.

"No. It just happens to be the topic of this month's article for BYTE."

"What has this got to do with tomorrow's game?" Chester asked.

"We're going to transmit the game to you in the tower on a beam of light."

Their eyes opened wider but they remained receptive.

"Let me demonstrate."

I took the transistor radio, tuned it to a station and placed it on the coffee table. Taking a long patch cord, I plugged one end in the radio earphone jack, automatically silencing the radio speaker, and plugged the other into the rear of the laser. Aiming the laser, I turned it on. A red spot, about 1/8 inch diameter, shone brightly on the wall 15 feet away.

"You're sure that won't burn the wall?"

"Trust me."

Next, I picked up the black box with the lens on it and turned it on. I walked over to the illuminated spot on the wall and interrupted the laser beam path with the box. When the beam intersected with the lens, music was heard!

"That's the radio station you tuned in, all right," Chester said.

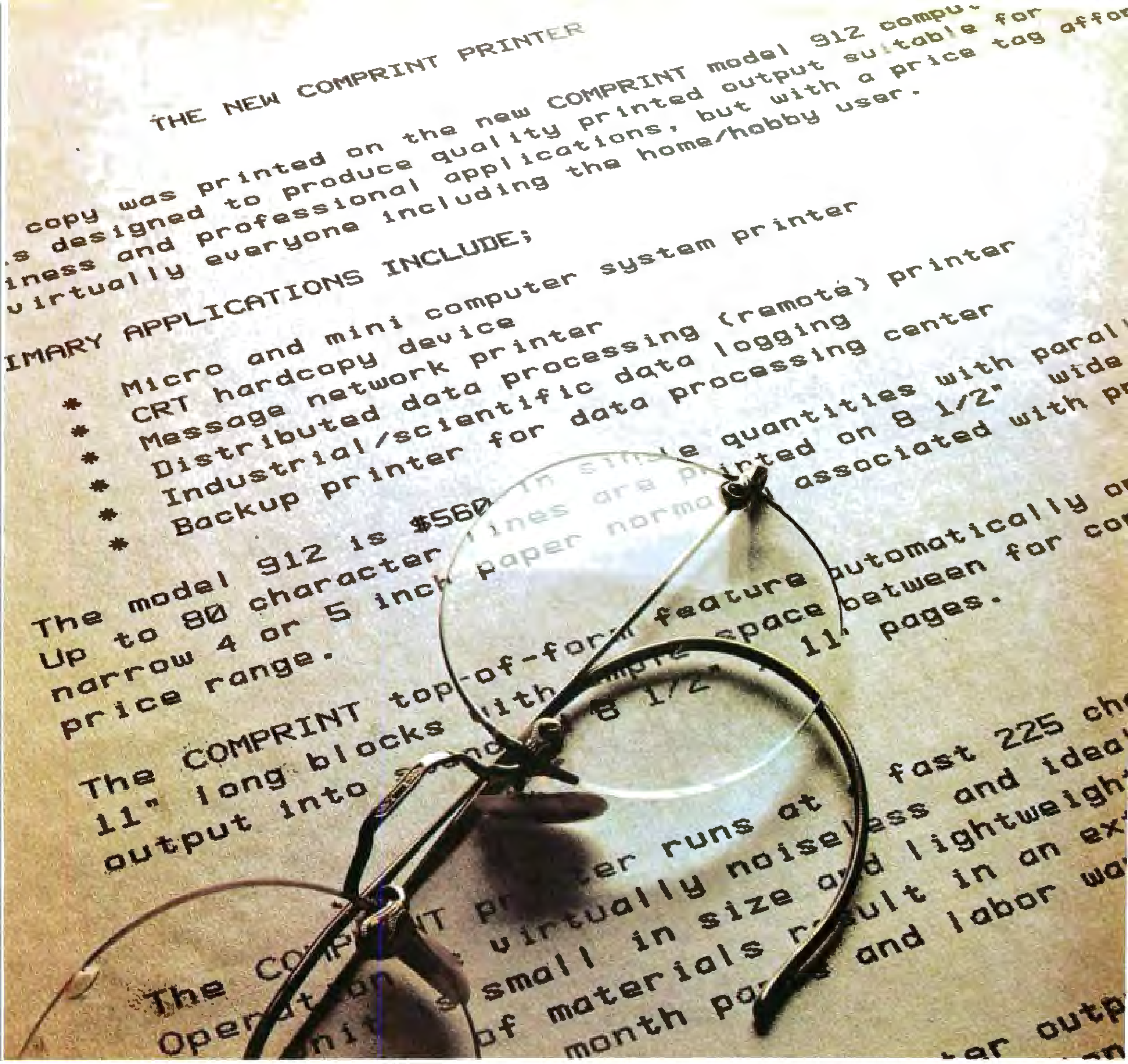
"Colonel, take that poker from the fireplace and wave it back and forth in front of the laser so it interrupts the beam."

"Why. . .the radio goes on and off," he exclaimed a minute later.

"Correction, Colonel. The radio doesn't go off, only the receiver, when it no longer "sees" the modulated laser light beam. Notice in addition that the beam barely spreads out at all over the 15 feet to the wall."

"I think I get what you're driving at, Steve."

"You've got it. Chester takes the re-



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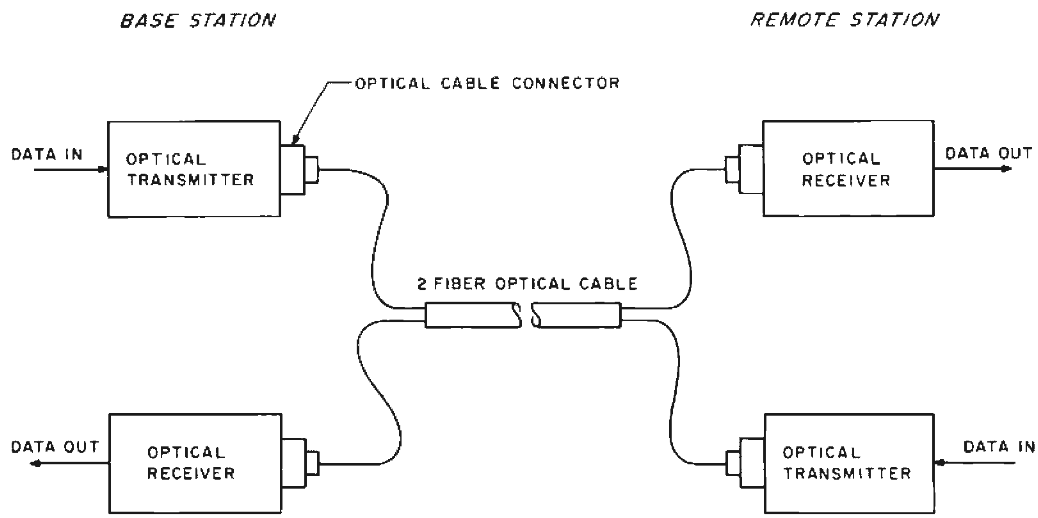

Figure 1: Block diagram of full duplex optical communications link.

ceiver up to the tower tomorrow, aims it at this window using the gun sight scope on top. Then we turn on the laser which, instead of being connected to the radio, comes from the television. Voila! Instant uninterrupted Red Sox baseball. And, no Beatrice!"

"Will it really work, Steve?" Chester asked.

"Sure, and tomorrow we'll prove it."

Before the next comment from anyone the telephone rang and Colonel Foster answered it. Chester and I listened and smiled.

"Look, Beatrice, your team doesn't have a chance for the pennant. . .Are you still claiming that that was an error?. . . It wasn't just luck in the 6th I tell you. . ."

Chester and I laughed. Beatrice was really giving the Colonel a run for his money, but there was a twinkle in his eye as he spoke. The Colonel was living what he enjoyed most – baseball. First on television and then blow by blow with Beatrice.

Communicate on a Light Beam

Most experimenters have never considered using a modulated light beam for data communication. I'm not suggesting that everyone throw out their twisted pair RS-232 lines and replace them with laser beams, but I do ask you to consider the commercial advantages of such a concept and try a few experiments.

When discussing modulated light communications, a definition of terms is in order. The two most often heard are lasers and fiber optics. It is important to recognize that one is a light source and the other is a light conductor. It is not necessary for them to be used together but this is often the case. I'll explain more about each later.

A full duplex optical communication link is shown schematically in figure 1. It consists of two pairs of optical transmitters and receivers which allow data to flow in two directions simultaneously. Data from the base to the remote travels on one line, while data from the remote to the base is on the other. This is a dedicated duplex hookup. Unlike the ones you've probably used, this one uses fiber optic cable rather than wire. In its commercial applications it can offer the following advantages:

- Immunity to strong electrical or magnetic noise. Fiber optic material is usually glass or plastic and since there is no electrical conduction there can be no induced electrical noise.
- High electrical isolation. Since the data conductor is a dielectric material, the isolation between the transmitter and receiver is a function of distance.
- Higher bandwidth and lighter cable. Optical modulation systems have inherently higher data rate capabilities and glass and plastic weighs less than copper. Bandwidth is typically 100 megabits.
- Lower loss than coaxial systems. New low loss fibers extend transmission distance.
- Negligible crosstalk. If each fiber optic channel is optically sheathed there is no crosstalk. Even adjacent unsheathed fibers rarely interfere with each other.
- Ultimately lower cost than either coaxial or twisted-wire systems. The raw material (sand) used in making fiber optics is abundant, while copper gets increasingly more expensive. Cost for a data transmission system is ultimately based on dollars per megabit times distance. Since fiber optic systems have higher bandwidths, the cost factor is slowly moving in their favor.

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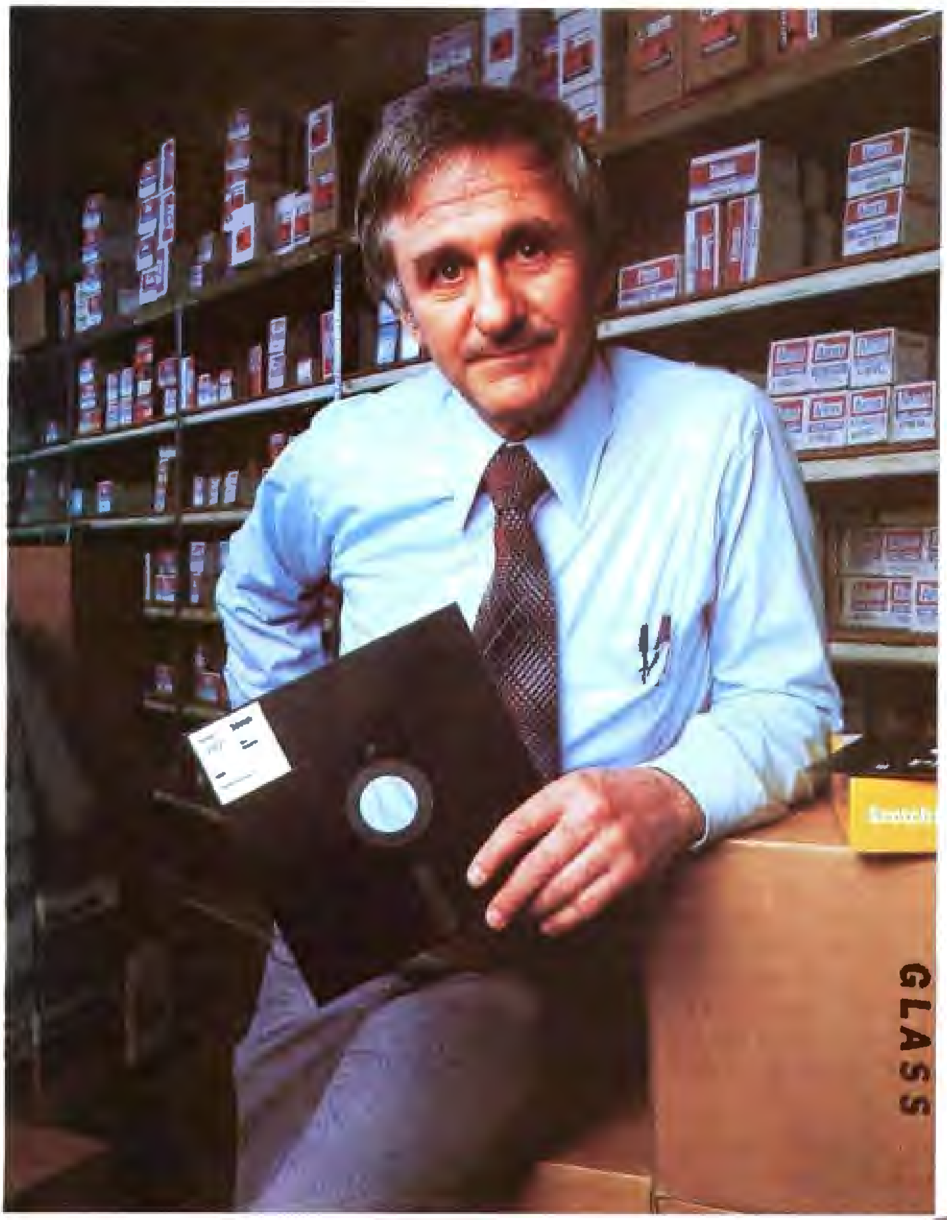

Don Stone, Vice-President, Mass. Auto Supply Company, Inc., Boston, Mass.

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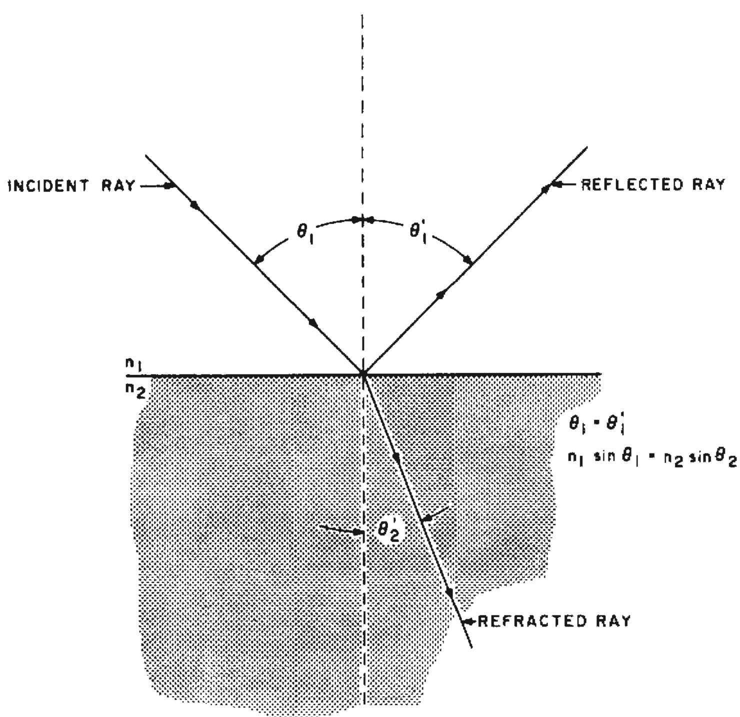


Figure 2: An example of reflection and refraction at an interface, such as the side of the optical cable.

Key ingredients in any optical communications system are the transmitters and receivers. The ultimate data rate is a function of how fast the transmitter can turn on and off, sending one bit of information, and whether the light sensitive receiver can track this transition. If the date rate is very low, say 110 bps in your experimental setup, a simple incandescent light and cadmium sulfide photocell will suffice. Higher data rates require much faster response and dictate use of LEDs (light emitting diodes) and phototransistors or photodiodes. Common red LEDs will easily handle 100 K bits per second and most common phototransistors, if properly biased, will also suffice. Higher frequencies require specially fabricated LEDs or, if the transmission line is especially long, then laser diodes might be in order.

It is important to know what each of the components in the system is and the way its selection affects the other components. The designs illustrated in this article are included to demonstrate a workable low frequency system which the personal computer enthusiast may wish to build. The physical electronics of high frequency commercial systems differ considerably, but the physical laws and general concepts are the same.

Fiber Optics

Fiber optics are just what they sound like – glass fibers which conduct light rather than electricity. To understand optical fibers we must look at a few definitions. An example of reflection and refraction is illustrated in figure 2. When a light ray strikes a boundary, partial reflection and partial transmission take place. The materials on either side of the boundary have particular constants n_1 and n_2 respectively (called *indices of refraction*) associated with them. These constants are dependent upon wavelength of the light transmission and the speed of light through the material. Reflection and refraction are related as follows:

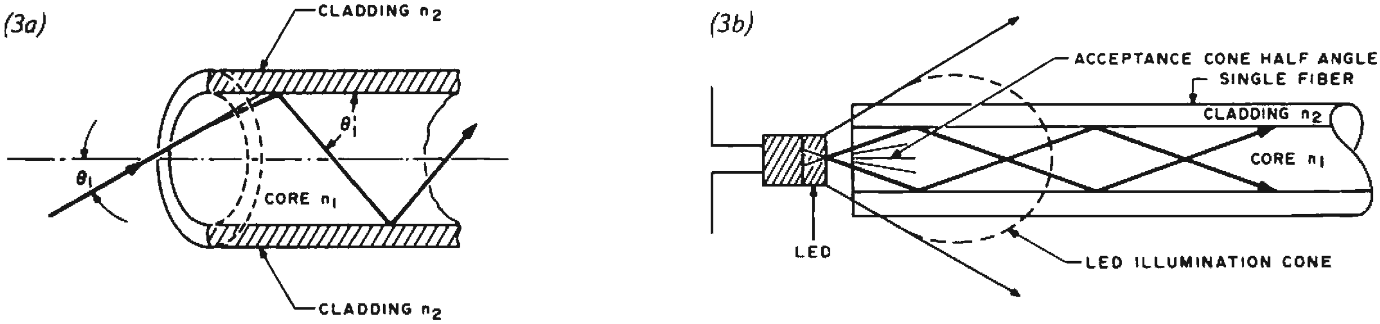
$$\text{Reflection } \theta_1 = \theta_1'$$
$$\text{Refraction } n_1 \sin\theta_1 = n_2 \sin\theta_2$$

The fiber has a *core,* a light transmitting material of higher index of refraction surrounded by a *cladding* or optical insulating material of a lower index of refraction. Figure 3a is a pictorial representation of a single fiber. Light enters the fiber at an infinite number of angles but only those rays entering the fiber at an angle less than the *critical acceptance angle* are transmitted. Light is propagated within the core of a multimode fiber at specific angles of internal reflection. When a propagating ray strikes the core/cladding interface, it is reflected and zigzags down the core. This is further illustrated in figure 3b.

Figure 3: Pictorial diagram of a single fiber illustrating the cladding and core boundary. Only light entering within the "acceptance cone" will be guided down the optical fiber as in figure 3b. Any rays outside this cone are not transmitted.

(3a)

(3b)



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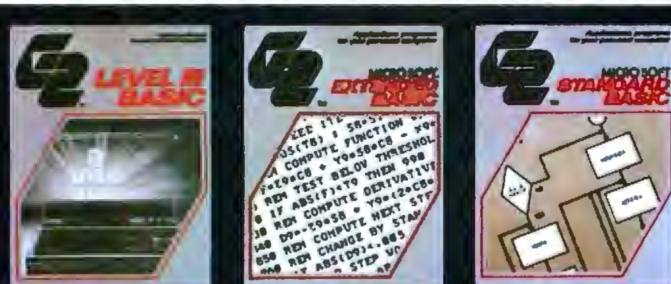

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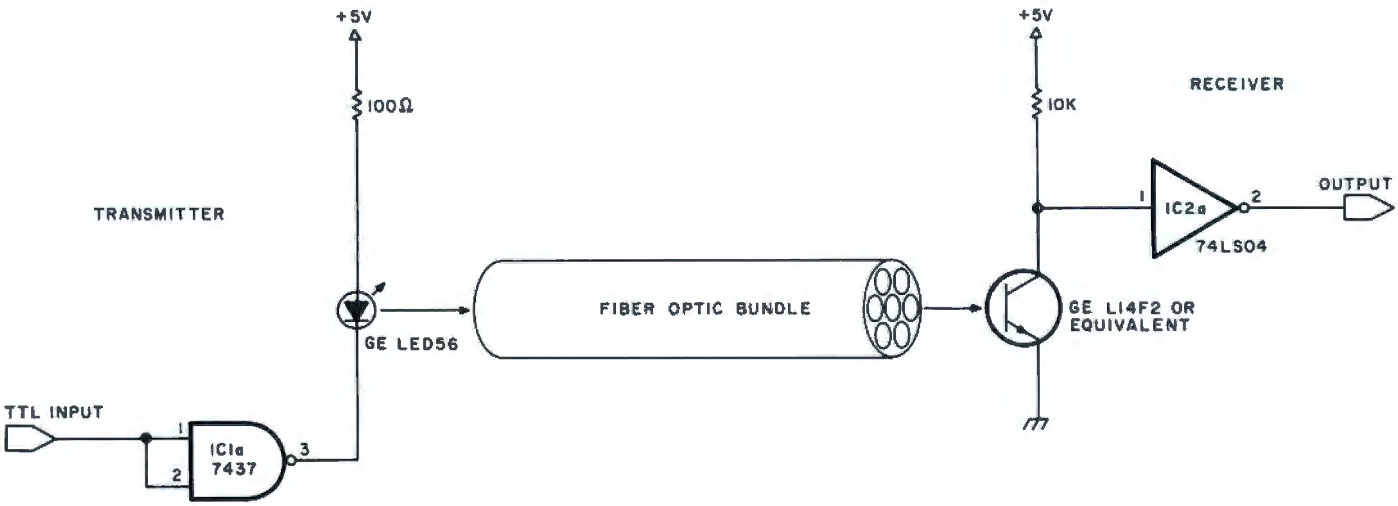


Figure 4: Schematic of a simple low speed and short distance fiber optics communications interface.

Photo 1 demonstrates that a very bright light can be transmitted through a single fiber. In this example the conductor is a single 40 mil plastic fiber with a helium-neon laser as an illumination source.

A fiber optic transmission system using readily available components can be constructed by any interested experimenter. A simple interface is shown in figure 4. An LED driven by a 7437 NAND buffer is focused into the end of a fiber optic bundle. The light emitted at the other end is focused on a phototransistor. When the light strikes the phototransistor it effectively grounds the input of the 74LS04, producing a high output. The connection between the LED, fiber optics, and phototransistor is facilitated through use of special optical connectors. Photo 2 shows an assortment of the type which should be used to build the interface in figure 4.

Lasers

The circuit of figure 4 is useful for only a short distance. This is due primarily to the low intensity of a standard LED. For greater distances a more intense light source is needed. This calls for a device such as a laser, an acronym that stands for *light amplification*

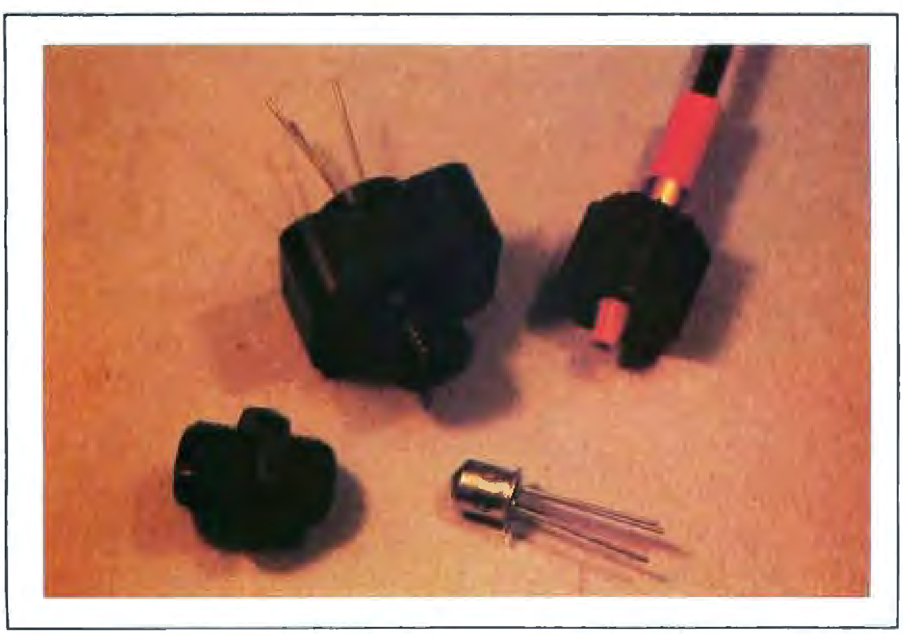
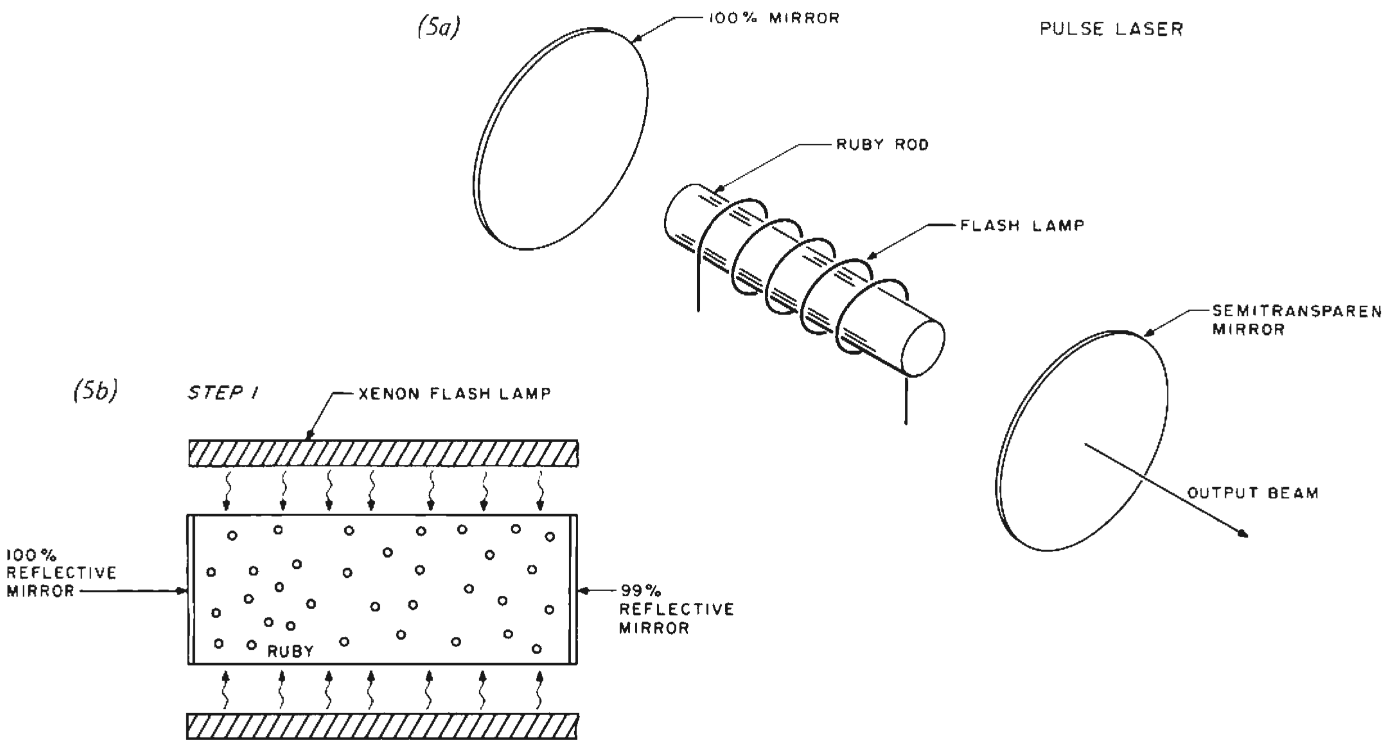


Photo 2: Special connectors necessary to use fiber optics properly. Shown here (starting in the upper right corner and continuing clockwise) are a fiber optic cable with an end connector, a phototransistor in a TO-18 package, an extension coupling which allows two cables to be connected, and a bulkhead receptical containing either an LED (light emitting diode) or phototransistor.



by *stimulated emission* of *radiation*. Light from a laser is all the same frequency, unlike the output of an incandescent bulb. Laser light is referred to as *coherent*, and has a high energy density. It can travel great distances without diverging from a tight beam.

The basic requirements for the creation of a laser are quite simple. We need a material that can absorb and release energy. Next, we need an energy source for exciting this material and a container to hold and control the lasing action, such as a glass tube or solid crystal.

In the actual lasing process, the laser material is placed inside the container, and then stimulated by means of an energy source into the emission of light waves. The laser beam is created by channelling the energy of these light waves into a particular and controlled direction. The result is a highly concentrated, brilliant beam of tremendous power. Figure 5 is a schematic of the first laser invented by Dr Theodore Maiman and a pictorial description of the lasing process.

The ruby laser is a pulse type laser which only produces a light output when the xenon lamp flashes. The best flash lamp can only be fired a few hundred times a second without extensive cooling apparatus. In a ruby laser this pulse mode operation is suitable for cutting stone and welding steel, but not for data communications, because the duty cycle is too short and the energy density too high for low cost fiber optics. The solution is to use a laser that operates continuously, such as a helium-neon gas laser

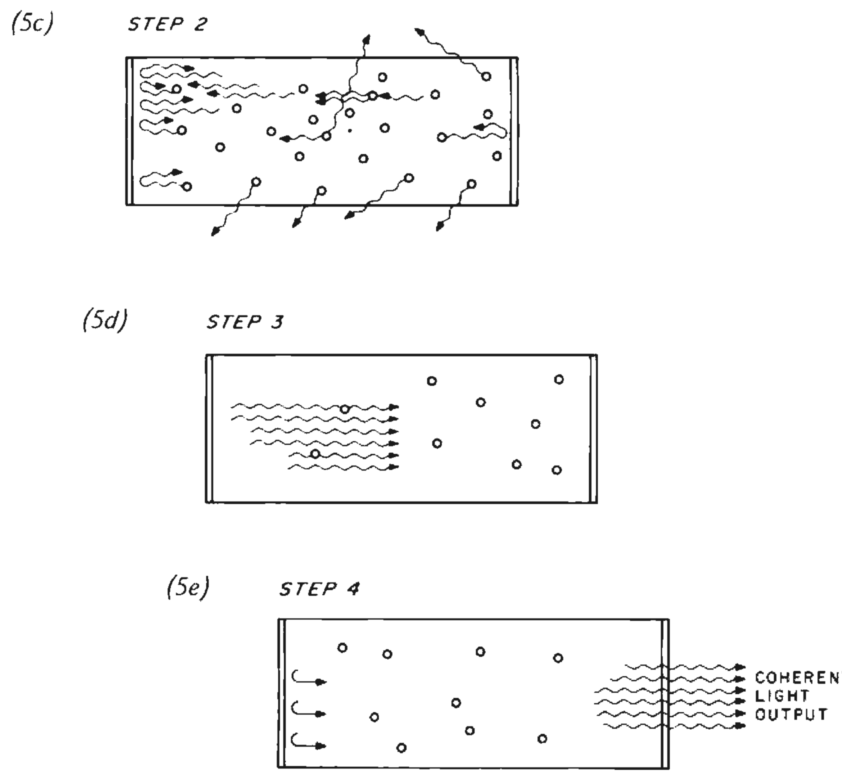
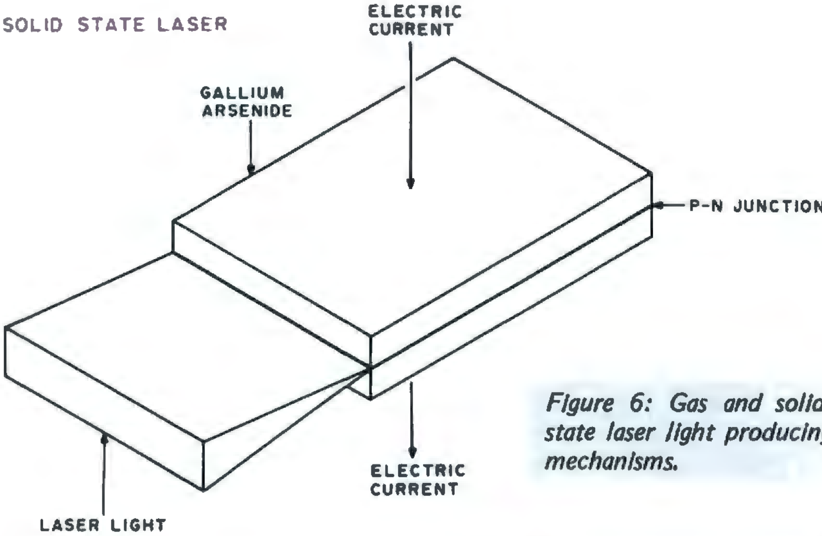


Figure 5: The first laser, invented by Dr Theodore Maiman, was made from a ruby rod excited by a xenon flash lamp. A schematic representation is shown in figure 5a. The laser builds up energy by the following process. In figure 5b the flash lamp is fired thereby exciting the electrons in the ruby rod. As the electrons drop back to their original energy level (step 2, figure 5c) they emit photons in random directions. In-step collisions of photons with other excited electrons start a wave front between mirrors (figure 5d). After many reflections back and forth between the mirrors, a wave front is built up until it contains sufficient energy to pass through the slightly less reflective of the two mirrors. This light output consists of coherent light.

(figure 6) or a laser diode which can be pulsed often enough to carry useful data.

The He-Ne laser uses mirrors and electrical excitation in a manner similar to the solid crystal type except that the lasing action is continuous. Photo 3 shows a He-Ne laser in operation. The particular unit has a power output of 2.2 mW and is made by Metrologic Inc. This type of laser can be modulated (the power supply high voltage is modulated) and used to drive a fiber optic bundle, but it is not normally used in that application. The light output of a He-Ne laser is usually red.



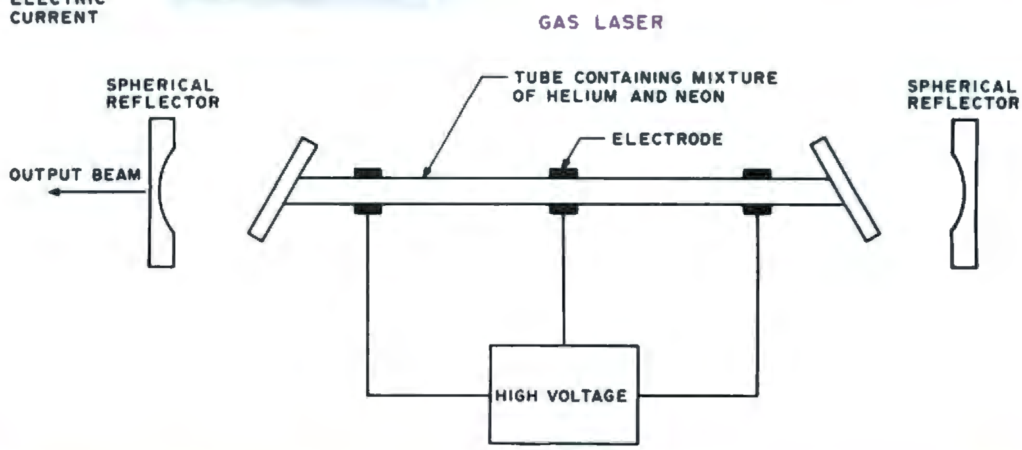


Figure 6: Gas and solid-state laser light producing mechanisms.

Photo 3: A laser on a tripod shooting across my living room. The laser is a 2.2 mW unit built by Metrologic Instruments of Bellmawr NJ 08031 (this particular model is the ML-969). This picture was taken at night; the trees outside are illuminated by outside flood lamps.

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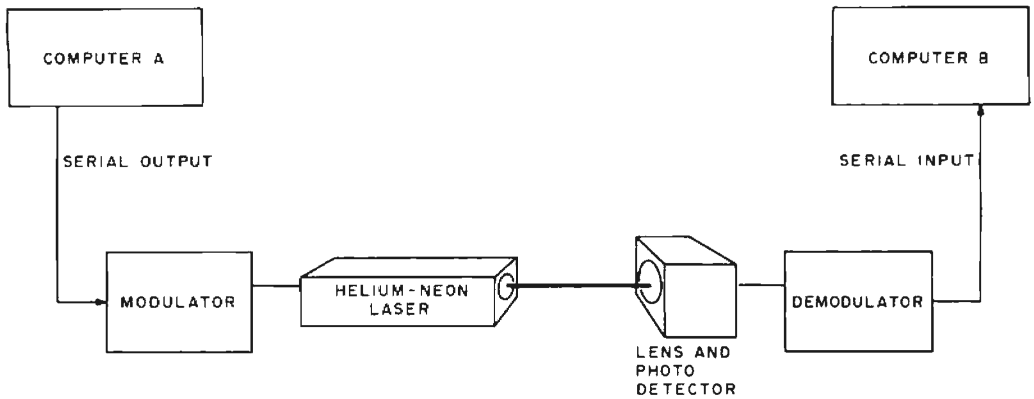


Figure 7: System configuration necessary for one computer to transmit data to another via a helium-neon laser beam. The schematic for the modulator and demodulator are shown in figures 8 and 9, respectively.

The most economical high intensity light source for long runs of fiber optics is the laser diode. Don't be so whimsical as to run out and buy one thinking you are going to make a ray gun – it should be just as easy to use as an LED. Laser diodes get very hot in operation and are generally operated only in pulse mode. An 8 W laser diode sold through the surplus dealer can have an average power of only a few hundred microwatts when used in pulse mode operation. Using laser diodes in continuous operation is beyond the talents and resources of most hobbyists and must be left to the commercial ranks for the moment. The light output from a laser diode is infrared and invisible to the human eye.

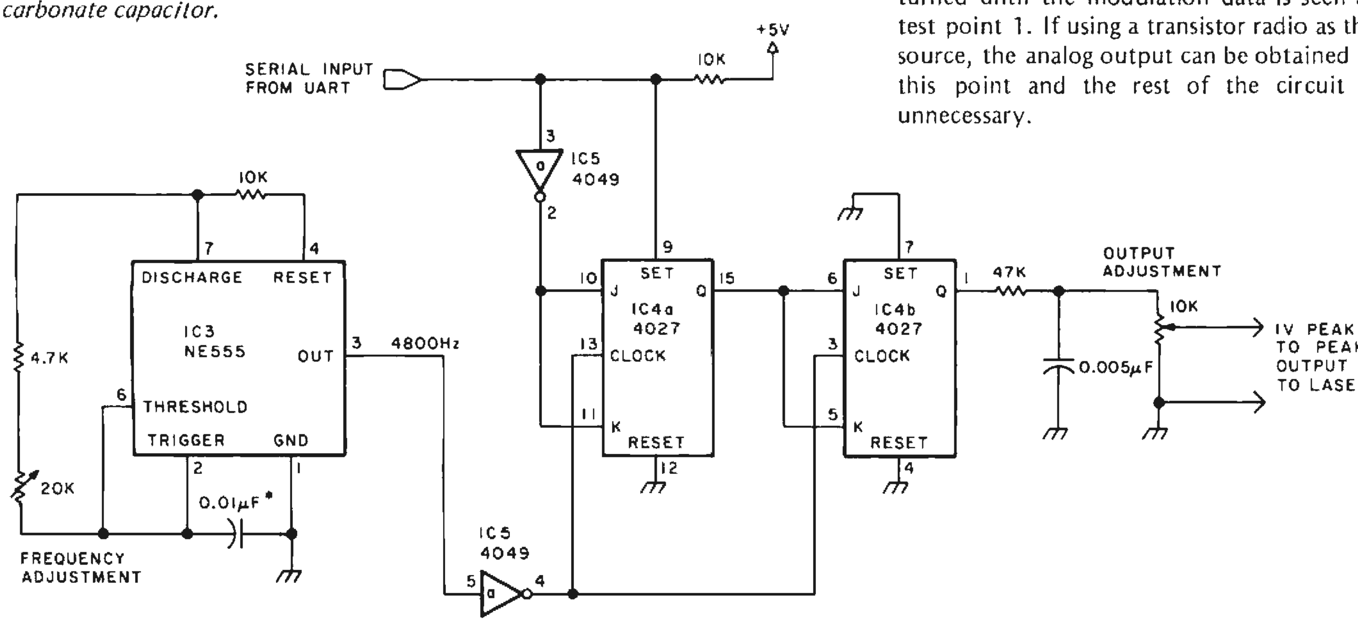
Communicating on a Laser Beam

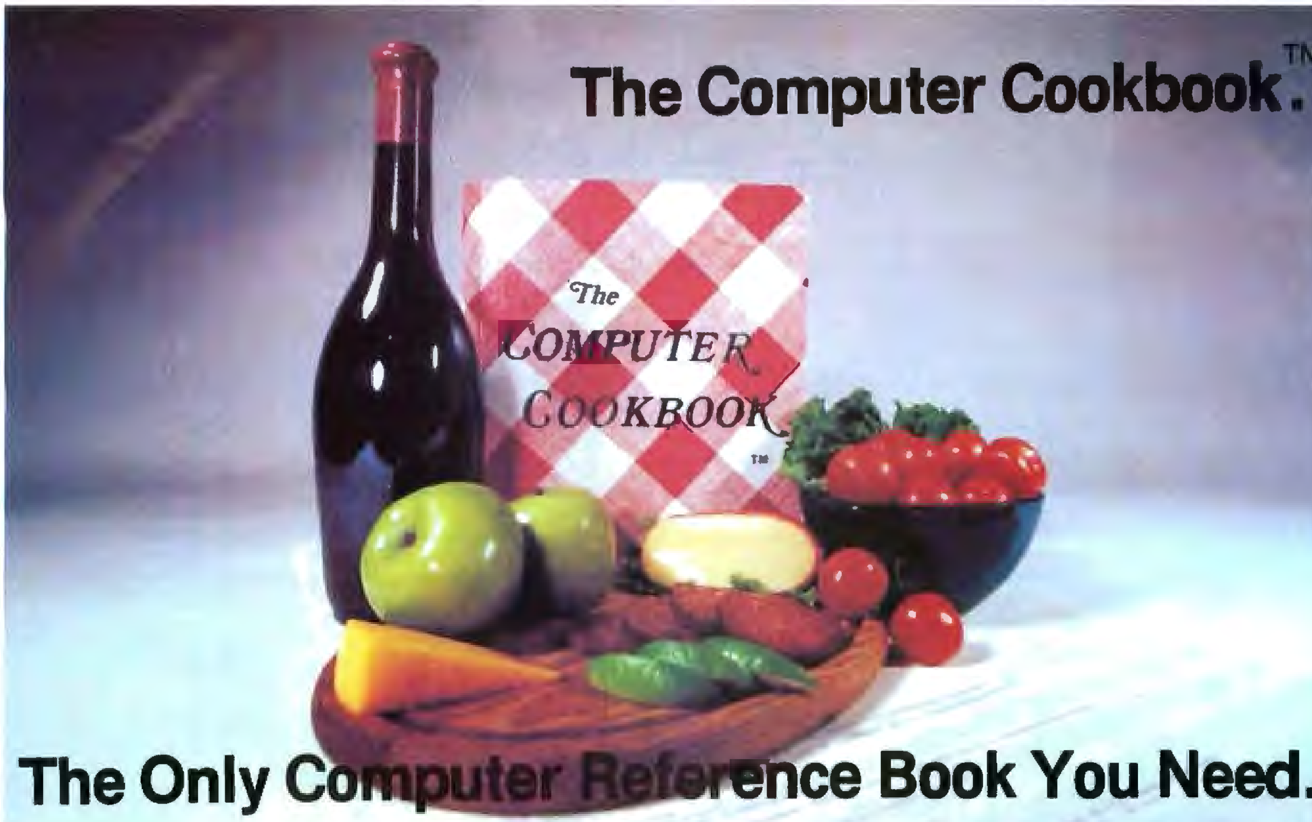
While it is possible to demonstrate communication with a laser diode, it is much more dramatic with a He-Ne laser since you can see the beam. A He-Ne laser can be modulated, but it cannot be turned on and off rapidly like an LED or diode. Instead the light intensity is modulated by the data signal. The Metrologic laser I used is a type ML-969 "modulatable" laser. It has a BNC connector on the rear and accepts a 0 thru 1 V input for 0 to 15 per cent intensity modulation. Any greater degree of modulation shuts off the lasing action.

Figure 7 illustrates the system configuration necessary to transmit data from one computer to another. Figure 8 is the schematic of a FSK (frequency shift keyed) modulation interface which can be used as the input to the laser. A 4800 Hz frequency reference produced by IC1 is divided by IC2 to give either 2400 Hz or 1200 Hz for a 1 or 0 logic input respectively. The modulation input to the laser can be any 1 V input up to 500 kHz bandwidth. A transistor radio is a good test source for experiments.

The receiver is shown in figure 9. The laser beam is directed at the phototransistor. With no modulation, the sensitivity is adjusted to set the phototransistor in the middle of its linear range. With the modulation turned on, the trigger adjust control is turned until the modulation data is seen at test point 1. If using a transistor radio as the source, the analog output can be obtained at this point and the rest of the circuit is unnecessary.

Figure 8: A frequency shift keyed laser modulation interface. This circuit accepts input from the computer's UART (universal asynchronous receiver and transmitter). A logic 1 input produces a 2400 Hz output. An input of logic 0 produces a 1200 Hz output. The power connections for the integrated circuits are shown in table 1. The starred capacitor is either a mylar or polycarbonate capacitor.

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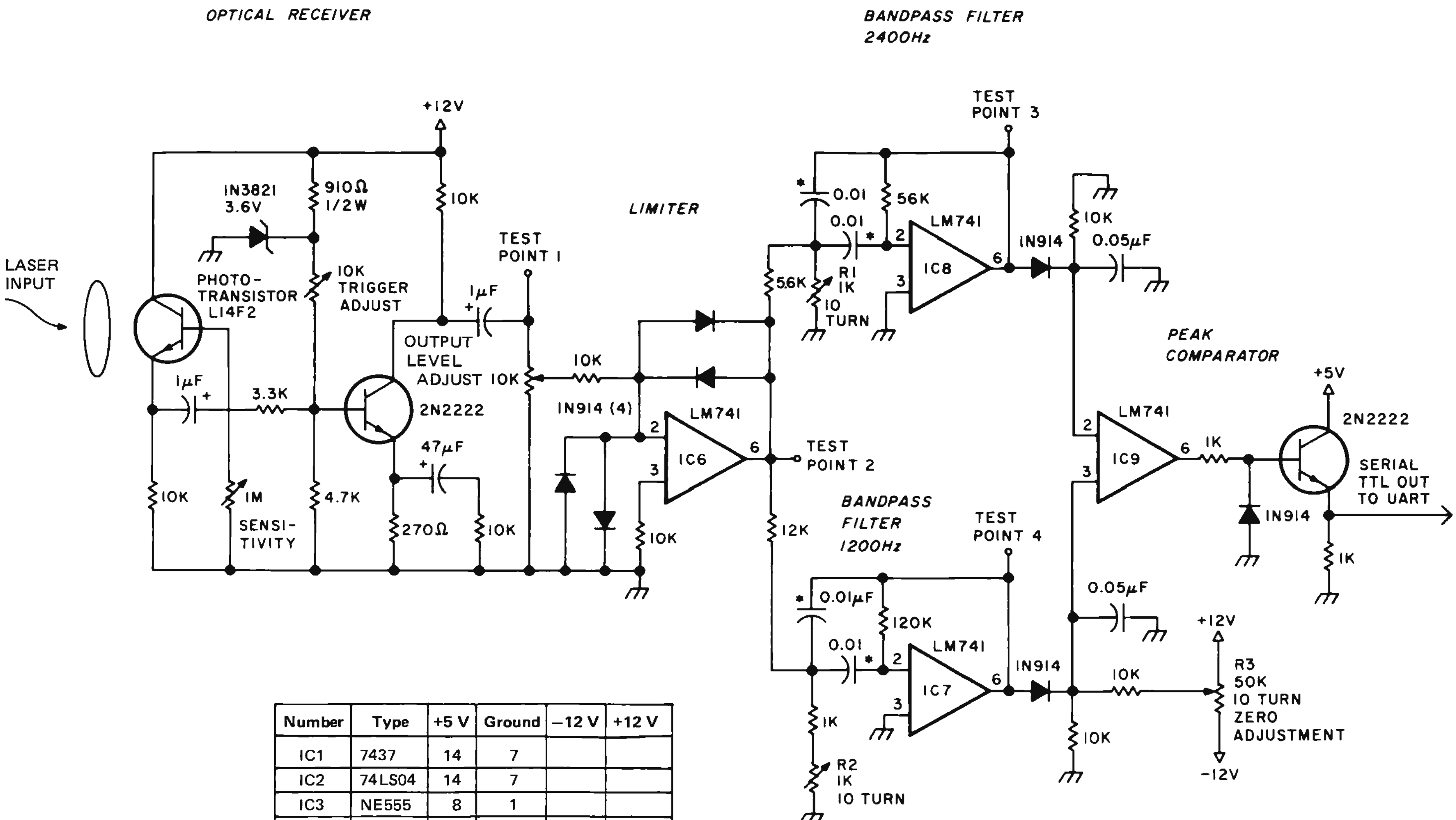

Number	Type	+5 V	Ground	−12 V	+12 V
IC1	7437	14	7		
IC2	74LS04	14	7		
IC3	NE555	8	1		
IC4	4027	16	8		
IC5	4049	1	8		
IC6	LM741			4	7
IC7	LM741			4	7
IC8	LM741			4	7
IC9	LM741			4	7

Table 1: Power pin connections for the integrated circuits used in constructing the laser communicator.

Figure 9: Modulated laser beam serial data receiver. The demodulator consists of two bandpass filters, one for 2400 Hz and the other for 1200 Hz. The power connections are given in table 1. The starred capacitors are mylar or polycarbonate capacitors. All resistors are 1/4 W unless otherwise specified. All diodes are type 1N914.

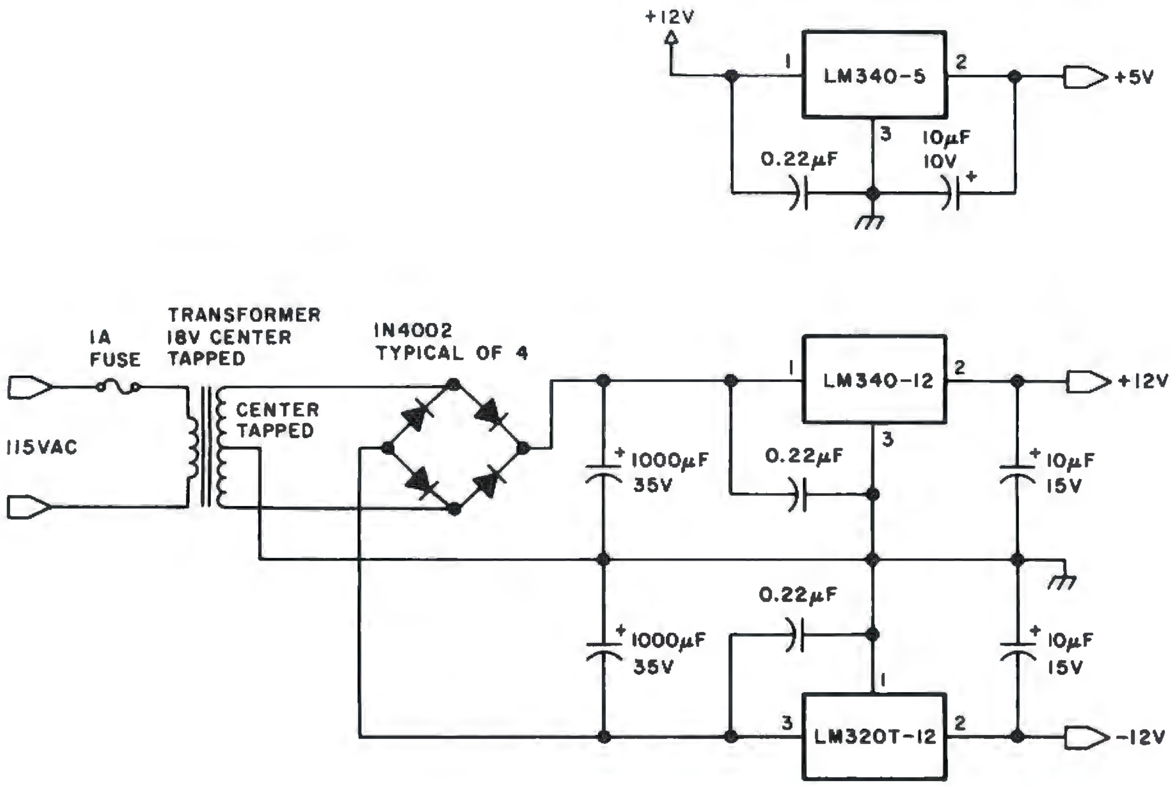

Figure 10: A triple voltage power supply for the laser modulator.

Integrated circuits 1 thru 4 form a frequency shift keyed demodulator with a TTL (transistor-transistor logic) output which is sent to a UART (universal asynchronous receiver-transmitter). To tune this section, first connect a 1200 Hz signal source to test point 1. Turn potentiometer R2 until the output amplitude of IC3 test point 4 peaks. Then applv 2400 Hz to test point 1 and adjust R1 until the amplitude at test point 3 also peaks. R3 adjusts the 'point at which circuit's output switches between logic levels. It should be set to follow the input at test point 1 with the shortest response time.

While the 15 per cent modulation could be detected directly and converted to NRZ (nonreturn to zero) formatted data, the receiver circuitry would be far more complicated. The combination of amplitude and frequency modulation techniques is intended to add significantly to the chances that an experimenter will have success building it. The critical parameters (as with any optical system) are alignment and light level. And, while you may not have to transmit a Red Sox baseball game across two miles of New Hampshire woods, it's nice to know how if you ever have to do it.

If you have any questions, ideas or comments on Ciarcia's Circuit Cellar please write to me and enclose a self-addressed, stamped envelope. I'm always interested in knowing what you readers think. Next month's "Circuit Cellar" topic will be biofeedback.■

Product Description

The Superboard II

A Surprising Single Board Computer From OSI

Photo 1: *The Ohio Scientific Superboard II single board computer, which features a 6502 processor, expandability, an 8 K byte Microsoft BASIC package on read only memory, and 1 K bytes of dedicated memory for video, sells for $279. +5 V power supply not included.*

Photo 2: *OSI Challenger 1P, electrically identical to the Superboard II, but with power supply and case, for $349.*

Christopher Morgan
Executive Editor

My first experience with an Ohio Scientific product (in fact, *my* first experience with a personal computer) was with an OSI single board computer I bought in 1976. The unit sold for $99 and featured a row of eight switches and accompanying LEDs (light emitting diodes) for entering machine language programs. It had 256 bytes of programmable memory, and no other I/O (input/output) besides the LEDs.

Much has happened to the personal computer industry since then, and this is reflected in OSI's latest single board computer, the Superboard II. Actually a stripped down version of the Challenger 1P, the Superboard II is a no frills computer with surprising capabilities. The $279 price buys an assembled and tested unit with a 53 key upper and lower case keyboard on one board. The user must supply a +5 V power supply and a video monitor or TV set with RF (radio frequency) converter in order to be up and running.

The Superboard II comes with a machine language monitor and 8 K byte Microsoft BASIC in read only memory, 4 K bytes of user memory, and a Kansas City standard cassette interface. A 6502 processor forms the heart of the system. An intriguing graphics package is also supplied: the direct access video display has 1 K bytes of dedicated memory.

BASIC PEEK and POKE commands are used to create the video display. 256 special graphics characters can be called by the user for special applications including tanks and spaceships for games, plus building block characters for generating bar graphs and the like.

The Superboard II can also be bought with a cabinet and power supply included in the form of the Challenger 1P; the price is $349 to which the cost of a television monitor must be added.

A variety of software is available from OSI for both units in the areas of games, business software, and educational software. Titles include: Tiger Tank; Lunar Lander; Breakout; Presidents Quiz; Trig Tutor; Math Think; Checking Account; Advanced Mathematics; Definite Integrals; Return on Investment; Load Calculator; Cash Flow Analysis; and many others.

Evaluation

Having an 8 K byte Microsoft BASIC package on board the Superboard II is a real plus, especially when you consider the price. I found the Kansas City standard cassette interface to be rather slow when entering long programs, but programs are listed on the screen while being read —a real convenience. The 25 character by 25 line display format took some getting used to, but the characters are big and easily read. There is no provision for screen clear. Not mentioned in the instructions is the fact that the keyboard must be in upper case mode for the user to enter programs and commands. This is a minor point, but one which might lead one to think that the unit is malfunctioning.

One of the attractive features of this computer is its expandability. The Superboard II (and the Challenger 1P) can be expanded with the addition of a 24 K byte programmable memory expander board, dual 5 inch floppy interface, port adapter for printer and modem, and an OSI 48 line expansion interface. An assember/editor and extended machine code monitor are also available. The unit can be upgraded to a 5 inch floppy system called PICODOS for approximately $650 additional cost. PICODOS is a limited single drive system that gives the user an 8 K byte work space and the ability to store up to eight programs on one disk. A full capability single drive computer system can be had for under $1000.

The Superboard II is an excellent choice for the personal computer enthusiast on a budget. ■

Single Chip Video Controller

Bob Haas
20887 SW Willapa Way
Tualatin OR 97062

Several semiconductor manufacturers have recently produced video display controllers contained on a single integrated circuit. While none of these is the "video terminal-on-a-chip" that some of the publicity would have you believe, these new devices perform many of the functions required in a video display, thereby reducing the number of integrated circuit packages required. In addition, they are all programmable to some degree, which allows adding new features to an existing design at low incremental cost, or changing display formats if required by changing needs. These characteristics make these devices particularly interesting to a computer experimenter. A user might start with a 16 line, 64 character, upper case only display, and as requirements (and budget) increase, convert to a "professional" 24 line, 80 character, upper and lower case format just by adding more memory and a new character generator.

In this article, I will present a survey of the characteristics of four video display controllers, namely, the Intel 8275, the Motorola MC6845, the NS (National Semiconductor) DP8350, and the SMC (Standard Microsystems Corporation) 5027. In addition, I will present a detailed description of the Motorola part and a design for a display using that device.

Device Characteristics

Table 1 summarizes the important characteristics of each device. All of the devices are programmable. The Intel, Motorola, and SMC parts are programmed by the microprocessor system to which they are attached. This means that when the system is powered up, a program must be executed to initialize the display controller, before a proper display will appear on the display screen.

The display formats of the Intel and Motorola devices are, within limits, completely variable. For the Motorola part, any line width from 1 to 256 characters can be chosen. (Of course, these limits are unreasonable values; the actual limits are determined by the display timing constraints, an example of which will be given in the detailed discussion of the Motorola unit, later in this article.) The SMC 5027 is manufactured with a fixed "menu" of line widths,

Text continued on page 56

About the Author:

Bob Haas leads a double life: by day he designs 6800 systems (for Tektronix's 4051 group); and by night he works on 6502 systems (on his own KIM-1 system). He uses the MC6845 display system described in this article with his KIM-1.

Acknowledgment

The author wishes to thank Mr Hank Trieckel of Motorola, Inc for his assistance in the preparation of this article.

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Microprocessor Compatability	8080 family (direct memory access only)	all	all	all
Simplest System Interface	direct memory access via Intel 8257	shared memory	shared memory	shared memory
Display Memory Size (maximum)	64 K	16 K	4 K	4 K
Addressing	linear	linear	linear	row/column
Scrolling	line, character, page	line, character, page	line, character, page	line only
Cursor	blink or steady, reverse video or underline	blink or steady, reverse video or underline	reverse video or underline, no blink	reverse video or underline, no blink
Interlace	none	video, or video and sync, or none	none	none or interlaced sync and video
Light Pen	yes	yes	no	no
Graphics Capability	limited	full	full	full
Process	MOS	MOS	IIL	MOS
Power	+5 V	+5 V	+5 V	+5, +12 V
Other Features (see text)	on board line buffers; visual attributes		high-speed timing on board	self-loading for stand-alone use

Table 1: Summary of characteristics of four video display controllers.

Text continued from page 52:
such as 20, 32, 40, 64, 72, 80, 96, and 132 characters, from which the initialization program can choose.

The NS DP8350 is mask programmed. Its characteristics are set by internal read only memories, the contents of which are determined when the device is manufactured. Changing the display format with this part means unplugging the current unit and plugging in a differently manufactured unit. A number of stock formats, among them 24 lines by 80 characters, will be available, but if your particular needs are not met by a stock part, you must contract with NS to program a custom part, agree to purchase a certain quantity, and perhaps pay a one time mask charge.

The SMC part has the ability to load its format parameters at power-up from an external read only memory, so that it does not have to be part of a microprocessor based system at all. It can therefore be used in a so-called "dumb" terminal.

All of the devices may theoretically be interfaced to any microprocessor, but practicalities limit the choices. The Intel part, being part of the 8080 family, is designed to interface to 8080 based systems via DMA (direct memory access) through the Intel 8257 DMA controller. This makes it difficult to interface the Intel part to non8080 systems. In fact, since many people's S-100 bus 8080 systems will not support direct memory access, the Intel part would be difficult to interface even to these systems.

The Motorola MC6845, a member of the Motorola 6800 family, is easily interfaced to 6800 and 6502 systems, and can be interfaced to 8080 and Z-80 systems. The NS and SMC parts have system interfaces similar to the Motorola part. The simplest method of interfacing the latter three parts is by means of shared memory, wherein the display memory appears to the processor to be ordinary programmable memory.

Memory Usage

The maximum size of the display refresh memory for each part is limited by the number of refresh memory address lines coming out of the package. The Motorola part has 14 address lines, and the NS and SMC parts each have 12. The Intel part has access to the entire system memory through an attached direct memory access controller, and the system memory may be as large as 64 K (65,536) bytes. The Intel, Motorola, and NS parts access linear (sequential) refresh memory addresses, so there is a simple relationship between the refresh memory address of a given character and its position on the display screen.

The SMC 5027, however, outputs addresses in a row and column format which (without the addition of hardware to do address translation) causes inefficient use of

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North Star additional disk drives are now available with the same high quality wood cover as the Horizon computer! The Additional Drive Cabinet (ADC) is designed to accept either one or two drives for the Horizon or for mounting North Star Micro Disk System drives. Like the Horizon, the ADC is available with either wood or blue metal cover. Included is a new power supply capable of powering one or two drives. The ADC is $129 in kit form. Assembled, with one drive the ADC is $599, with two drives $999.

Pascal Now Available for Horizon

The much-heralded Pascal language is now being offered for use with the North Star Horizon computer. North

Inside view of Horizon with processor board, RAM board, disk controller, two drives, and power supply.

Star, with the co-operation of the University of California at San Diego, is now delivering a Pascal Program Development system. North Star Pascal is ideally suited for developing large programs because of features such as: long variable names, block-structured control statements, and compilation. North Star Pascal is available on 5¼" diskettes for use with the Horizon or Micro Disk System. North Star Pascal will operate with either the Z80 or 8080 microprocessor.

Pascal, including documentation, is available in either single or double density versions for $49.

An auxiliary Pascal diskette, containing an 8080/Z80 assembler and some additional Pascal utilities, is available for $29. Complete information is available at your local retail computer store.

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The new North Star 32K RAM board (RAM-32) has doubled the memory density of the popular Horizon computer. Available either with the Horizon or other S-100 bus computers, the RAM-32 runs at full speed—no wait states—with the 4 MHz Z80A microprocessor (as well as with slower Z80 and 8080 processors). Addressability of the RAM-32 is switch-selectable in four 8K regions.

North Star RAM features like bank-switching and parity checking are standard. The parity checking capability means that the RAM-32 is constantly diagnosing itself. That's a plus for your system. The fact that parity checking is a North Star RAM-32 standard is a plus for your pocketbook! There is no extra charge for this important capability.

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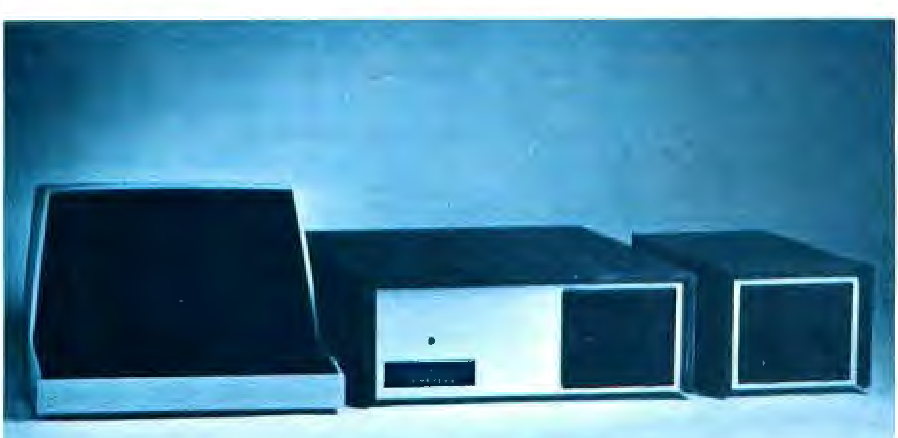

◀ A typical Horizon configuration: CRT, Horizon computer, Additional Drive Cabinet (ADC).

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display memory when the display dimensions are not integer powers of 2. For example, building a 24 line by 80 character display with the SMC part would require a refresh memory that is 24 by 128, or 3,072 bytes total. Of these, 1,152 bytes would not be displayed. Also, a program to manage the display would have to perform row and column calculations to locate a given screen position. Of course, additional hardware could be added to "linearize" the addresses, but this defeats the purpose of using one of these devices, namely, the reduction of hardware.

Scrolling and Cursing

All of the devices provide scrolling, that is, the ability to move data around on the display screen without actually moving the data in the refresh memory. The SMC device provides line scrolling only. An example of scrolling using the Motorola part is given in a later section of this article.

All the parts provide for the generation of a *cursor* (ie: some way for a human operator to determine the position at which the next character entered from a keyboard will be placed on the display). The Intel and Motorola devices allow a steady or blinking cursor consisting of an underscore or a reverse video (black on white) block. The NS and SMC parts allow for underscore or reverse video, but do not provide blinking.

Video Signal Characteristics

A standard North American television picture is composed of two frames of 262½ scan lines each, with scan lines from alternate frames interlaced vertically the width of one line, so that the resultant picture has 525 scan lines. Many computer video displays use only about 262 scan lines, and are not interlaced. This limits the maximum number of character rows on a display to about 25.

The Motorola part allows the use of interlacing to produce an aesthetically more pleasing display by doubling character dots vertically. This fills in what might otherwise be spaces on a high-resolution display. This is called *interlaced sync*, in Motorola's terminology. The Motorola and SMC parts also provide for *interlaced sync and video*, in which all 525 lines can be used for character formation, allowing as many as perhaps 50 character rows per display. The use of interlace does cause a flicker effect on ordinary white phosphor (P4) monitors, but computer experimenters with long persistence, green phosphor (P39) monitors may want to consider using interlace.

Other Features

The Intel and Motorola circuits provide support for a *light pen*, that is, a light-sensitive "wand" used by the display operator to point to areas on the display screen to signify something to the attached system. This requires additional hardware to implement.

The data displayed on the screen by the display controller need not be dot patterns from a character generator read only memory. They might be dots forming part of a graphic image. Except for the Intel part, the display controllers support whatever graphics-generation hardware the system designer cares to attach to them. The Intel part is limited in this area because of its line buffers, which orient it toward character generation only (more on this later).

The Intel, Motorola, and SMC display controllers are manufactured by the MOS (metal oxide semiconductor) process, and do not include the so-called high-speed timing function of a display on the device. The National part, however, uses an I^2L (integrated injection logic), with none of the speed limitations of MOS, so it does include the high-speed timing functions. This inclusion helps to reduce external parts count. (A discussion of just what these timing functions are follows in a later section of this article.)

As mentioned earlier, the Intel display controller must interface to a system through a DMA controller such as the Intel 8257. The Intel display controller incorporates two 80 character line buffers. While it is displaying a row of characters from one line buffer, it fills the second line buffer from the memory by "stealing" some memory cycles. It then uses the second line buffer for display and fills the first line buffer from the third row of characters, and so on. The timing for a 24 line by 80 character display is such that up to 25 percent of a system's memory cycles may be taken by the display controller action. The Intel part's line buffers store 7 bit characters, so the graphics achievable with this part are limited to what can be displayed with a 128 character set, augmented by character-set switching (using additional hardware).

A distinguishing feature of the Intel part is support for *visual attributes*. With only minimal external hardware, blocks of characters can be made to blink, be highlighted (higher than normal brightness), be reversed (black on white), be underlined, or have any combination of these four qualities. In addition, two more attribute signals are provided that could provide color selection on a color display.

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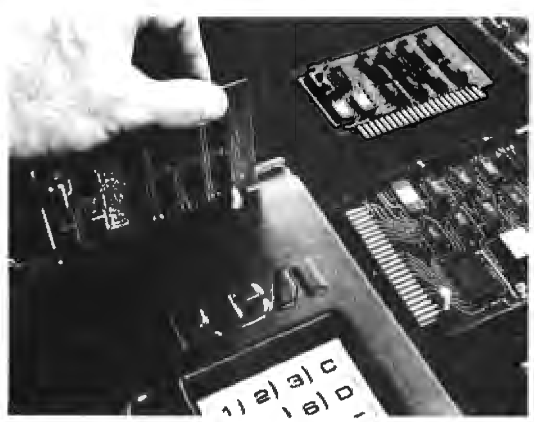

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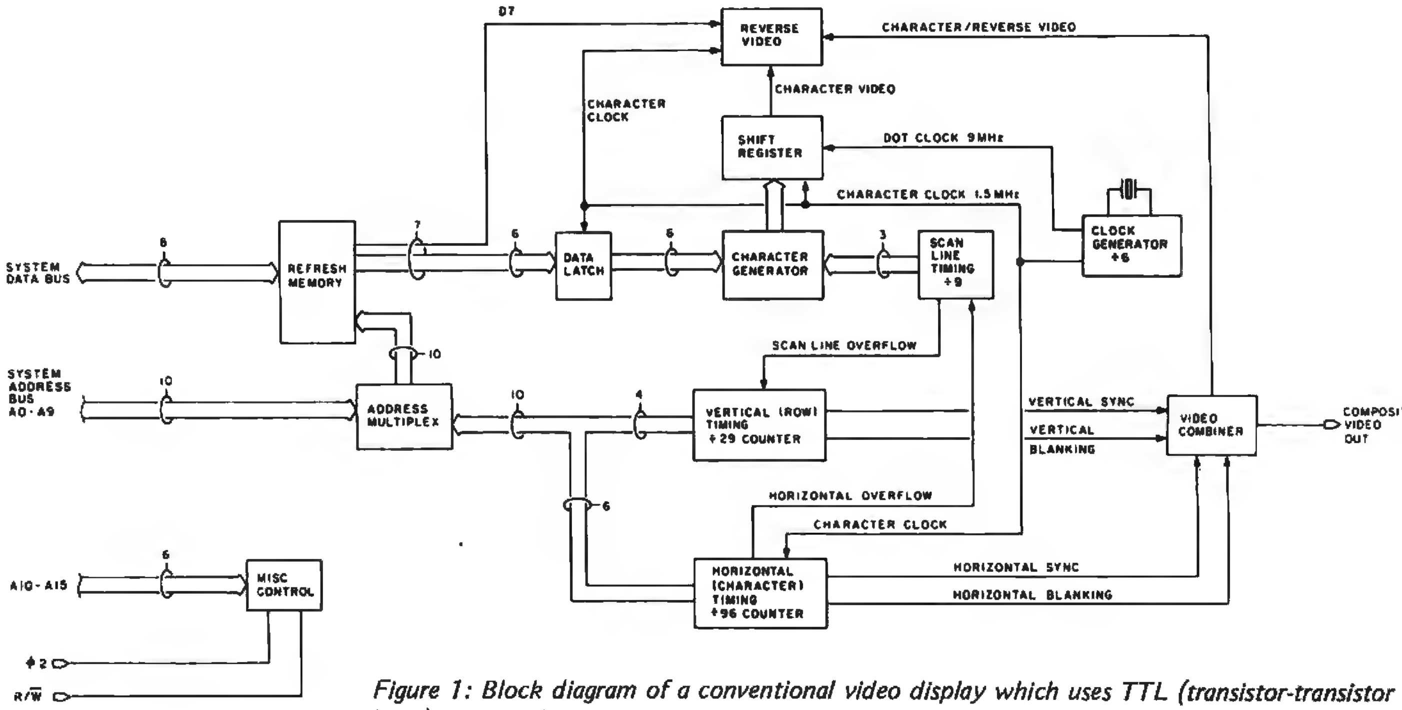

Figure 1: Block diagram of a conventional video display which uses TTL (transistor-transistor logic) integrated circuits.

A Conventional Display Design

To understand what the single integrated circuit video display controllers do, it is helpful to understand what functions a video display circuit must perform, and how those functions can be carried out with conventional TTL (transistor-transistor logic). Figure 1 shows the block diagram of such a display. A total of 32 packages (including the memory and character generator circuits) is required. The design is optimized for a 16 line, 64 character format. It uses the shared memory type of interface to the system. This interface scheme is simpler to implement, and faster for sytem updates, than the cursor control interface used in TV Typewriter designs, but it does suffer from a "snow" effect when the system updates the display.

A 9 MHz crystal oscillator provides the timing for the entire display. The 9 MHz signal is used to clock the shift register that feeds dots (or pixels) to the video combiner circuit, hence it is called the "dot clock." The character generator is a 5 dots horizontal by 7 dots vertical unit. The dot clock frequency is divided by 6 to allow for the 5 horizontal dots in each character, plus one blank dot space between characters. The dot clock divided by 6 is called the *character clock,* and it controls the transfer of characters between portions of the circuit.

The horizontal timing circuit is driven by the character clock. This circuit counts to 95, then resets itself to 0; therefore there are a total of 96 character intervals in each horizontal scan. The character clock rate of 1.5

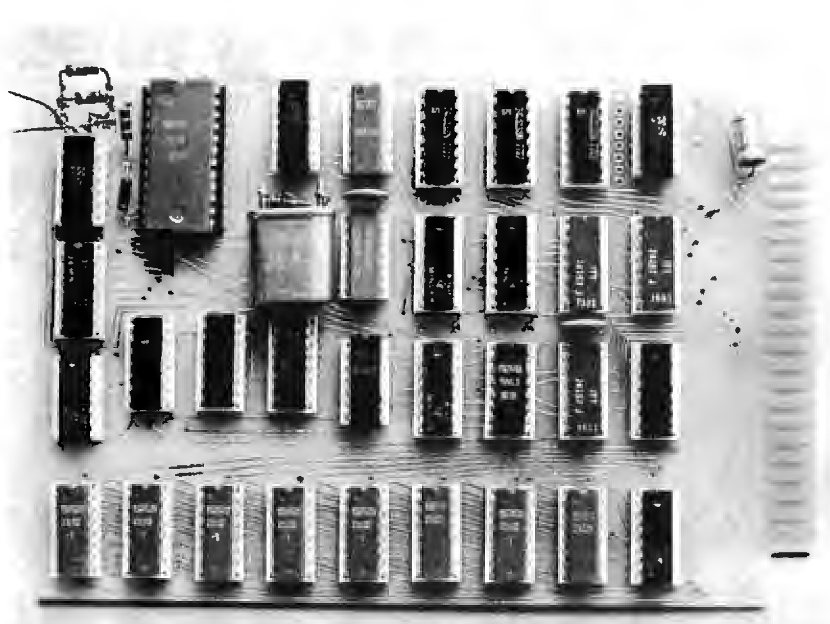

Photo 1: Video display circuit constructed from TTL (transistor-transistor logic) devices. This is the same TTL circuit discussed in the article text.

MHz (9 MHz divided by 6) yields a character time of 0.666 μs. 96 character intervals per horizontal scan yield a scan time of 63.94 μs, or a frequency of 15,640 Hz, close to the television standard. Of the 96 character intervals, 64 are displayed, and 32 are blanked.

At the end of each horizontal scan, another counter, the scan line counter, is incremented. It counts to 8, then resets itself to 0. Its output is connected to the character generator, to cause the character generator to output the correct line of dots for each scan line. Scan lines 0 and 8 are blank, because the character generator puts out no dots for these lines. There are, therefore, two blank scan lines between rows of characters. When the scan line counter resets to 0, the vertical (row) counter is incremented. The vertical counter counts to 28, then resets to 0. The first 16 counts are used to display character rows, and the remaining 13 are blanked. The 29 rows of nine scan lines each yield a total of 261 scan lines per frame, a vertical scan time of 16.69 ms (63.94 μs times 261), and a vertical frequency of 59.9 Hz, close enough to 60 Hz to minimize any shimmy problems in the display caused by power supply ripple or magnetic fields.

The addresses supplied to the refresh memory are produced by the horizontal (character) timing and the vertical (row) timing. The vertical address is incremented only when the scan line counter resets, so

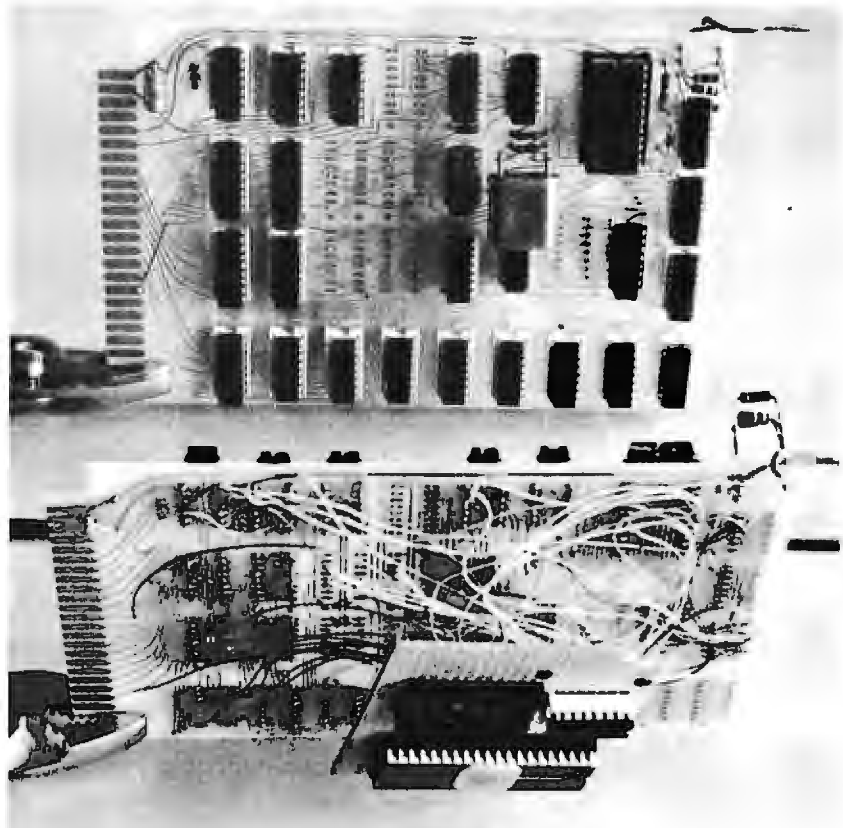

Photo 2: Printed circuit board from photo 1 after modification. Observe the wiring changes and "kluge board" attached to the back side of the board. The small kluge board contains the Motorola MC6845 video display processor, which has been grafted onto the original circuit. A mirror was used to show front and back sides simultaneously.

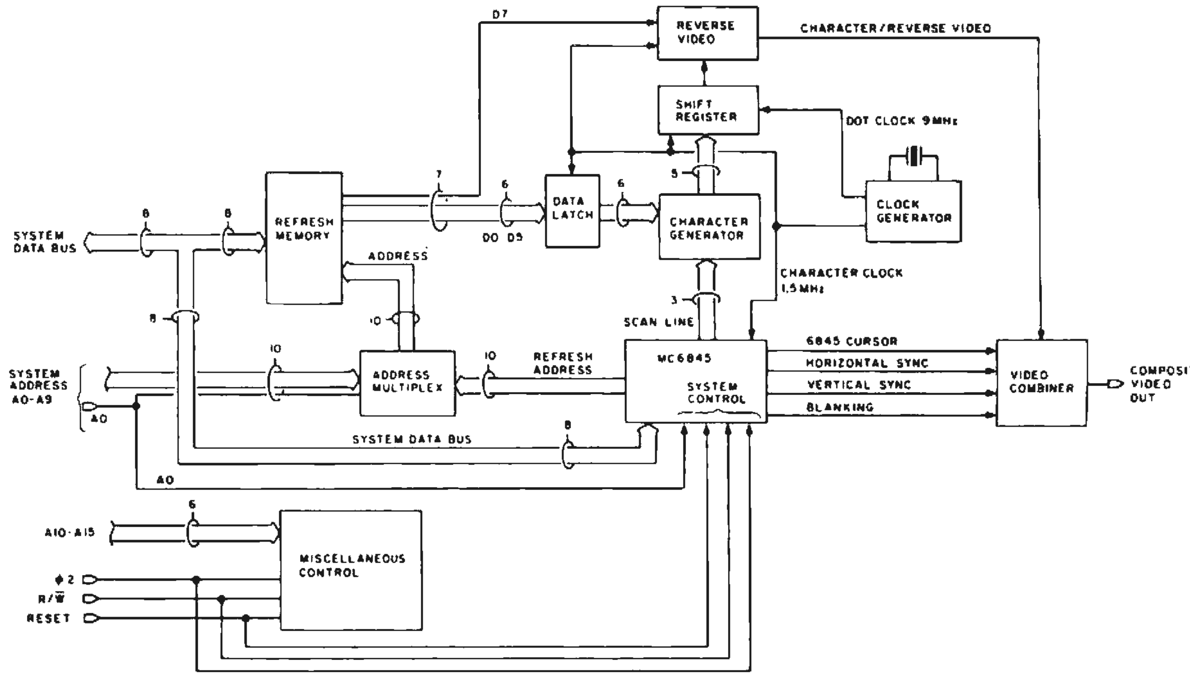

Figure 2: Block diagram of a video display utilizing the Motorola MC6845 video display controller.

that a given row of 64 characters of refresh memory is scanned nine times, in order to "paint" all seven scan lines of the characters, plus two blank lines. When the scan line counter resets, the vertical counter is incremented so that the next row of 64 characters may be scanned. In order to center the display, the vertical sync pulse is produced at about the 22nd character row, and the horizontal sync pulse at about the 80th character interval.

The circuit includes the capability of reversing (ie: converting to black on white) any character with bit 7 (the most significant bit) on. This can be used to highlight blocks of text, or generate a cursor.

Normally the refresh memory is connected to the vertical and horizontal timing circuits through a *multiplexer*, which can be thought of as a 10 pole, 2 position switch. When the processor wants to update the display, control circuitry switches the multiplexer so that the address the processor wants to update is supplied to the refresh memory instead of the address the timing circuits would be supplying. The processor reads or writes the location. The memory output is probably not correct for the display at that moment, so a segment of a different character is substituted for the correct one, producing the snow effect if extensive updates are being performed. The snow can be eliminated by allowing the processor to access the refresh memory only when the display is blanked, but I did not include circuitry for this in my design.

Using the Motorola MC6845 Display Controller

Figure 2 shows the block diagram of the display redrawn using the Motorola MC6845. The change is not striking. The 6845 has replaced only three blocks, namely, scan line timing, vertical (row) timing, and horizontal (character) timing. The circuit using the 6845 has five fewer packages. The 6845 occupies about the same amount of board space, consumes about the same amount of power, and costs more than the TTL packages it replaces. What have we gained by the replacement? For the person who is perfectly happy with the 16 by 64 TTL design, nothing. However, the advantage of the 6845 lies in its programmability. The characteristics of the display of which it is a part are easily changeable. This means that the same circuit can provide formats other than 16 by 64, such as 25 by 40, 14 by 72, and 12 by 80. The 6845 provides hardware scrolling, a blinking cursor (in addition to the selectable reverse video carried over from the all TTL circuit), support for a light pen, and three interlace options.

The programmability of the 6845 is in one way a slight disadvantage. An initialization program must be run by the system before the display will start up. The TTL version starts displaying immediately upon power-up, although the display will show at first whatever random characters the refresh memory contains at power-up.

Motorola's diagram of the 6845's internal

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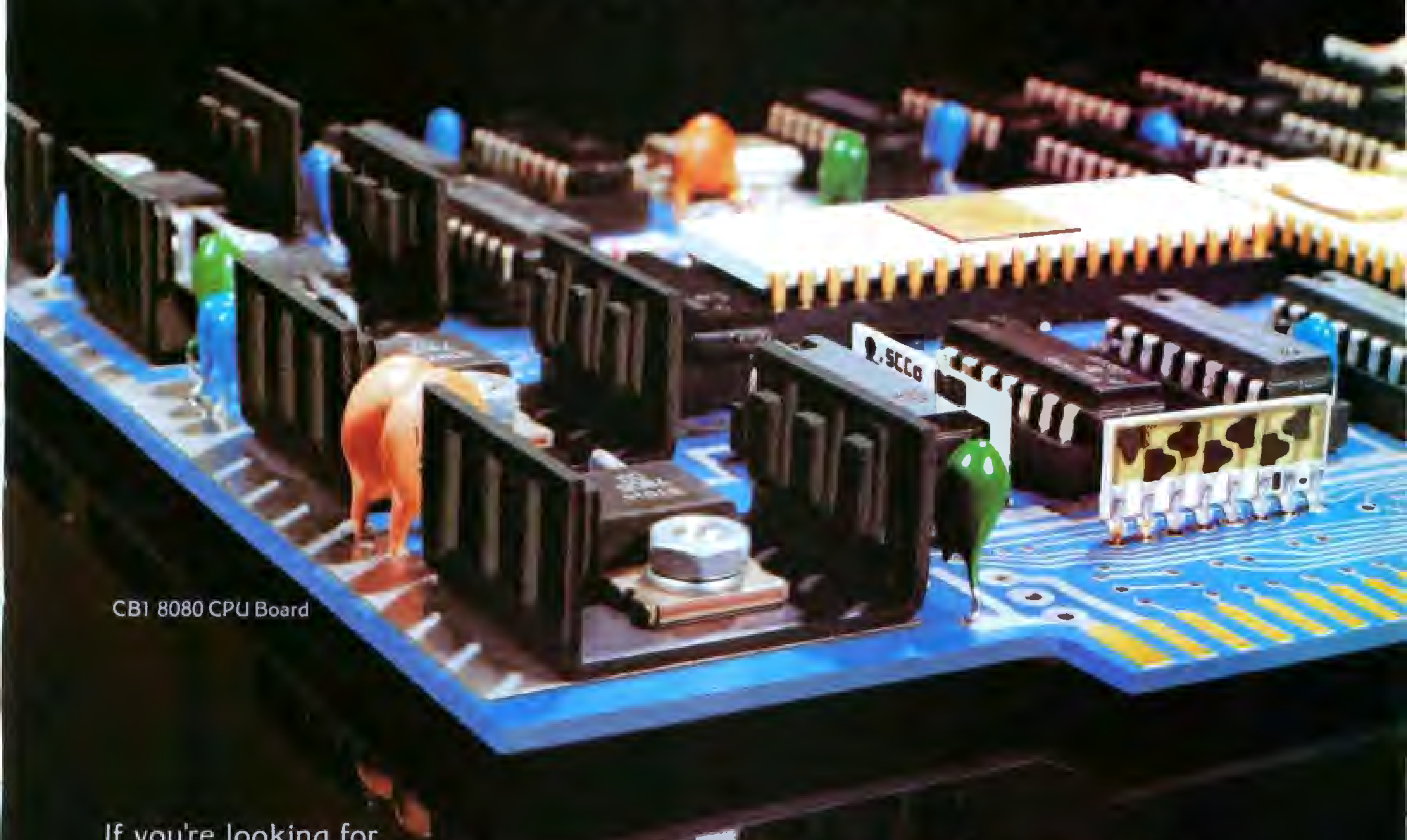

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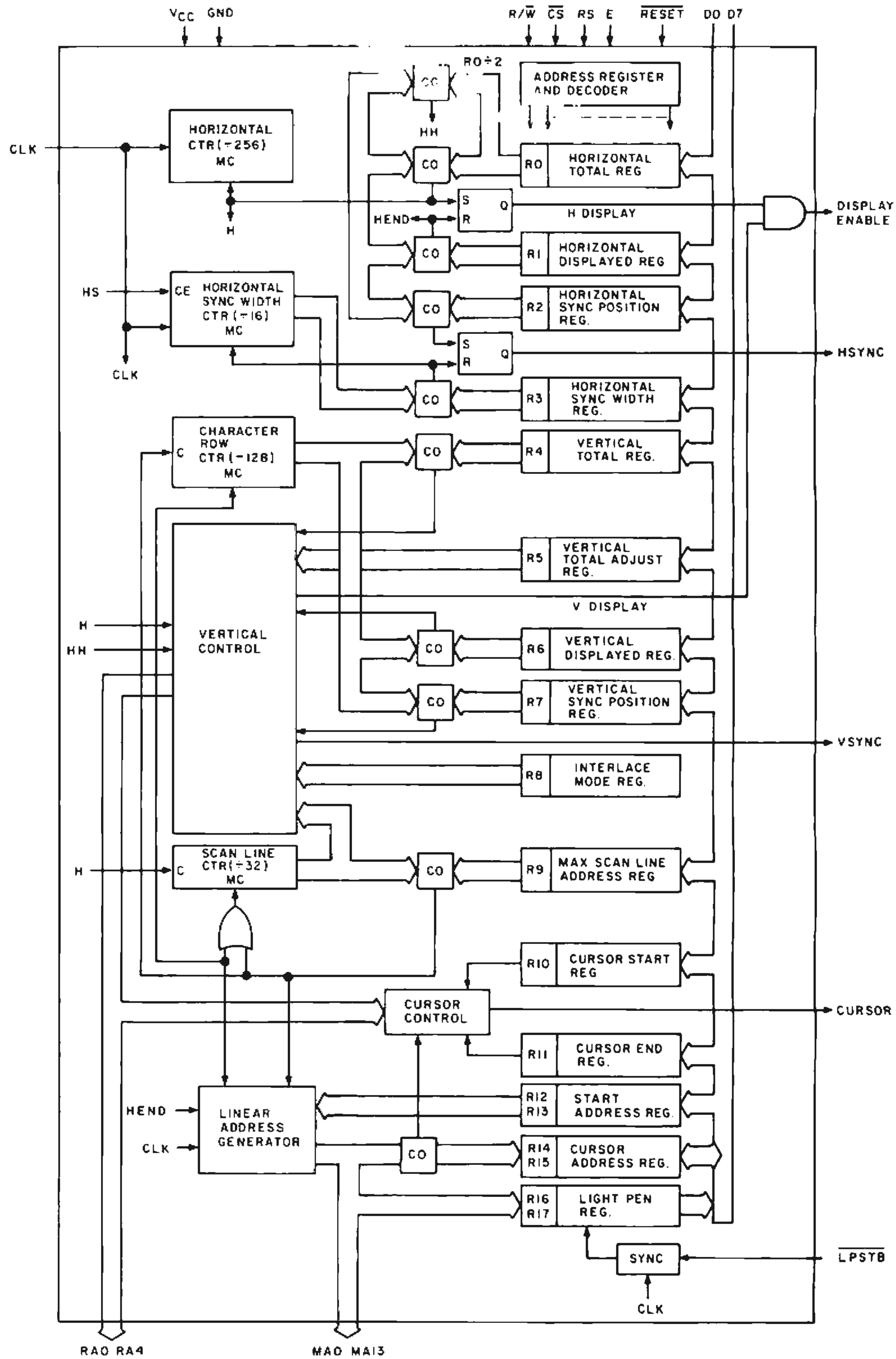

Figure 3: Functional block diagram of the Motorola MC6845 video display controller. Diagram used by permission of Motorola Semiconductor Products, Inc.

structure is shown in figure 3. The characteristics of the display are set by values stored in the 6845's internal registers by a program run on the system processor. Some of the registers are written only once, at system power-up, to establish the format of the display. Other registers are updated periodically as part of normal display usage.

In order for the system to access the 6845's internal registers, the device is connected to the system data bus, the system ϕ_2 (phase 2) and R/W (read/write) control lines, to an address decoder, and to address bus line 0. The display now responds to two sets of addresses — 1,024 addresses corresponding to the 1,024 screen positions, and to two additional addresses used to access the 6845's internal registers. I will call

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Listing 1: Initialization routine for MC6845 as coded for the 6800 microprocessor.

```
0200 5F              CRTINI   CLR  B                   ;  INIT REG #
0201 CE    0213               LDX       #TABLE         ;  INIT TABLE PTR
0204 F7    E800      CRTLP    STA  B    CRTC           ;  STORE REGISTER NUMBER
0207 A6    00                 LDA  A    0,X            ;  GET TABLE VALUE
0209 B7    E801               STA  A    CRTC+1         ;  STORE IN REGISTER
020C 08                       INX                      ;  NEXT TABLE VALUE
020D 5C                       INC  B                   ;  NEXT REGISTER NUMBER
020E C1    10                 CMP  B    #16            ;  LAST REGISTER?
0210 26    F2                 BNE       CRTLP          ;  REPEAT IF NOT LAST
0212 39                       RTS                      ;  RETURN TO CALLER
0213                 TABLE    FCB       $5E,$40,$4D,$08
0217                          FCB       $1C,$02,$10,$16
021B                          FCB       $00,$08,$40,$08
021F                          FCB       $00,$00,$00,$00
```

Listing 2: Initialization routine coded for the 6502 microprocessor.

```
0200 A2    00        CRTINI   LDX       #0             ;  INIT REG AND TAB PTR
0202 8E    00   E8   CRTLP    STX       CRTC           ;  STORE REGISTER NUMBER
0205 BD    11   02            LDA       TABLE,X        ;  GET TABLE VALUE
0208 8D    01   E8            STA       CRTC+1         ;  PUT VALUE IN REGISTER
020B E8                       INX                      ;  NEXT REGISTER
020C E0    10                 CPX       #16            ;  LAST?
020E D0    F2                 BNE       CRTLP          ;  REPEAT IF NOT
0210 60                       RTS                      ;  RETURN TO CALLER
0211                 TABLE     .BYTE    $5E,$40,$4D,$08
0215                           .BYTE    $1C,$02,$10,$16
0219                           .BYTE    $00,$08,$40,$08
021D                           .BYTE    $00,$00,$00,$00
```

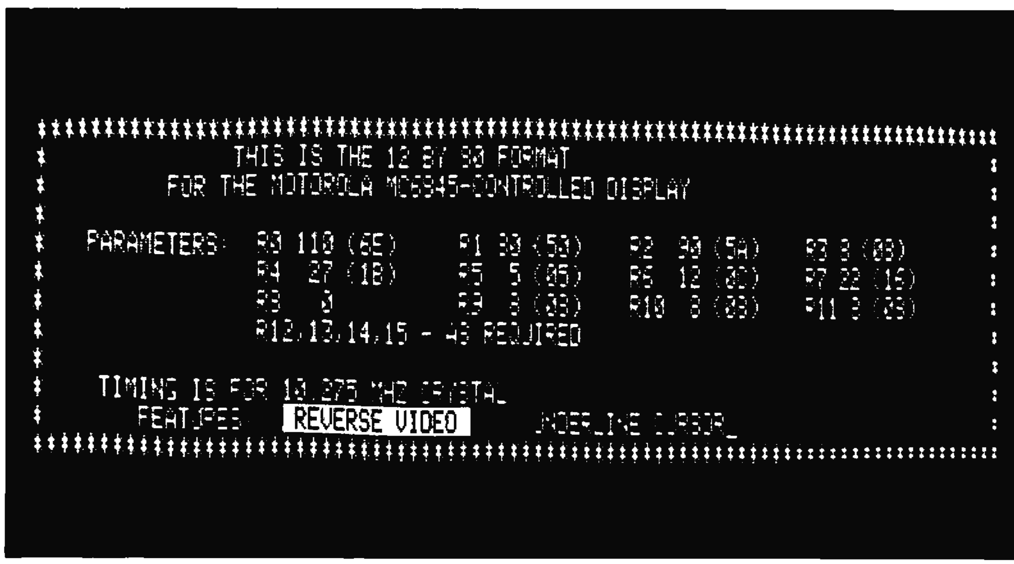


Photo 3: Display generated by MC6845 controlled circuit. The 12 line by 80 character format is shown. Parameters illustrated are values placed in 6845 registers by program executing on the main system processor. A 10.275 MHz crystal is used to correct for severe overscan in the author's monitor.

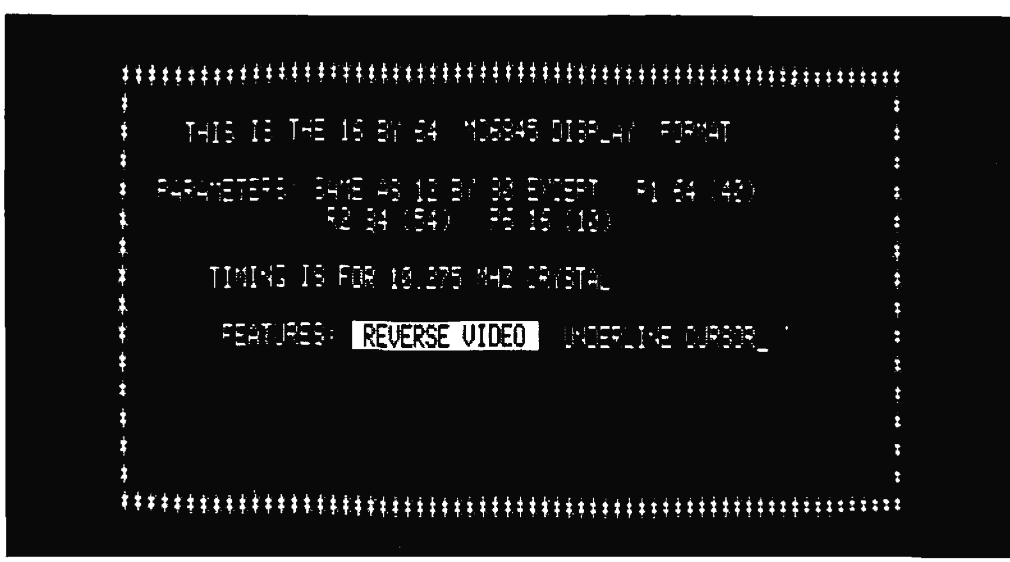


Photo 4: MC6845 circuit generated display using 16 line by 64 character format. Parameters shown and referenced are correct for 10.275 MHz crystal, which was left in place after demonstrating 12 by 80 format. See table 2 for parameters appropriate for 9.0 MHz crystal.

these latter addresses X and X+1; with the 6845's RS (register select) line connected to system address line 0 (the least significant bit), these will be consecutive addresses.

The first address, X, is the 6845's "pointer" register, which determines which register is accessed through address X+1. To write to a particular register, store the register number at X, and the desired value at X+1. A routine to initialize the 6845 coded for the 6800 is shown as listing 1, and a version for the 6502 as listing 2. The 6502 version is slightly shorter, because the 6502's X register can be used both as a table pointer and as the 6845 register number.

Table 2 summarizes the function of each register and the values to be programmed into each register for three formats: 16 lines by 64 characters, 25 by 40, and 12 by 80. The detailed function of each register and the calculation of the values for the 16 by 64 format are as shown in the following seventeen examples.

R0 Horizontal total. This register is programmed with one less than the total number of character intervals in a horizontal scan. A value of 94 provides for a total of 95 character intervals. This produces slightly better overall timing than the value of 96 character intervals used in the TTL circuit. The horizontal scan time is 95 X 0.666 μs = 63.27 μs, for a frequency of 15,800 Hz.

R1 Horizontal columns displayed. A value of 64, equal to the number of characters displayed, is used.

R2 Horizontal sync position. A value of 77 specifies that the horizontal sync pulse is to start at the 77th character position. This value centers the display on my particular monitor, but may be varied as needed for other monitors.

R3 Horizontal sync width. This is specified in number of character intervals. A value of 8 yields a sync pulse width of 5.33 μs, close to the television standard.

R4 Vertical total. This register is programmed with one less than the total number of character rows. A value of 28 specifies 29 character rows.

R5 Vertical total adjust. This register allows adding additional scan lines to the vertical display time to trim the vertical scan frequency, if required to bring it close to the power line frequency (to minimize display "shimmy"). A value of 2 is used here.

R6 Vertical rows displayed. This register is programmed with the number of character rows to be displayed, 16.

R7 Vertical sync position. A value of 22 specifies that the vertical sync pulse is to be produced at the 22nd character row, which centers the display on my monitor. Other monitors may require a slightly different value. The vertical sync pulse width is not programmable, as is the horizontal sync pulse width. It is fixed at 16 scan line times.

R8 Interlace mode. This register is programmed with 0, specifying no interlace (equivalent to the TTL circuit). Two other interlace modes are available, as mentioned previously, but these require a long persistence phosphor (P39) monitor.

R9 Maximum scan lines. This register

Register	Function	Value for 16 by 64	25 by 40	12 by 80
R0	horizontal total	94 (5E)	–	110 (6E)
R1	horizontal cols. displayed	64 (40)	40 (28)	80 (50)
R2	horizontal sync position	77 (4D)	66 (42)	90 (5A)
R3	horizontal sync width	8 (08)	–	–
R4	vertical total	28 (1C)	–	27 (1B)
R5	vertical total adjustment	2 (02)	–	5 (05)
R6	vertical rows displayed	16 (10)	25 (19)	12 (0C)
R7	vertical sync position	22 (16)	27 (1B)	22 (16)
R8	interlace mode	0 (0)	–	–
R9	maximum scan line	8 (08)	–	–
R10	cursor start	64 (40)	–	–
R11	cursor end	8 (08)	–	–
R12	refresh start address (high order)	0*	–	–
R13	refresh start address (low order)	0*	–	–
R14	cursor address (high order)	0*	–	–
R15	cursor address (low order)	0*	–	–
R16	light pen (high order)	**		
R17	light pen (low order)	**		

Table 2: Appropriate values to be stored in internal registers of MC6845 for several display formats. The decimal representation is given first, and the hexadecimal representation follows in parentheses. The values marked by one asterisk (*) may be updated during display usage. The positions marked by two asterisks (**) are for a light pen; this design does not provide for a light pen. The values given for the 12 line by 80 character format should be used with a 10.275 MHz crystal. The values for the 16 by 64 and 25 by 40 formats are specified for a 9.0 MHz crystal.

Value Stored in R10 (decimal)	Result
0	nonblinking reverse block
8	nonblinking underscore
32 or 40	no cursor
64	fast blinking reverse block
72	fast blinking underscore
96	slow blinking reverse block
102	slow blinking underscore

Table 3: Summary of cursor options for Motorola MC6845. To produce results shown in table, a value of 8 must also be stored in R11.

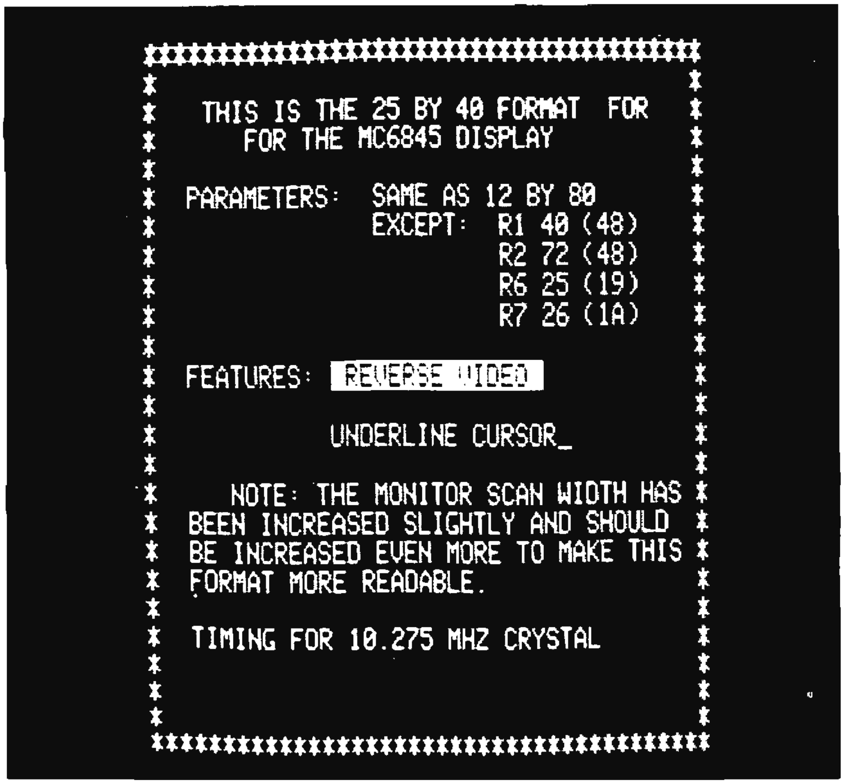


Photo 5: Display demonstrating 25 line by 40 character format, again produced by the MC6845 circuit. As before, see table 2 for 9.0 MHz crystal parameters.

is programmed with the maximum scan line number that is to be presented to the character generator, and is 1 less than the number of scan lines per character row. A value of 8 causes the counter to run from 0 to 8, then back to 0. This produces a total of nine scan lines per character row. Using this number along with the others specified above, the resultant vertical timing is: 29 rows (R4) X nine lines per row (R9) = 261 scan lines. 261 scan lines + two lines extra (R5) = 263. Now, 263 X 63.27 μs per scan line = 16.64 ms per vertical scan, or a frequency just under 60.1 Hz, again close to the power line frequency. (Other values could be used to adjust the vertical frequency to 50 Hz, the common power line frequency in other countries.)

R10 and R11 Cursor start and end. These registers specify the format of the cursor. The values of 64 for R10 and 8 for R11 generate a cursor which is a blinking reverse video block covering the entire character. For discussion of other cursor options see the section entitled "Cursor Generation."

The above registers are write only. Values may be stored in them, but not read back. These registers are generally written to only once (when the system is first powered up) to establish the characteristics of the display.

R12 and R13 Refresh start address. These registers are the high order six bits (R12) and low order eight bits (R13) of a 14 bit refresh address counter. For a nonscrolled display, these are initialized to 0. For a scrolled display, these registers will be updated periodically; since they, too, are write only, copies of them must be maintained by the processor. More information on the use of these registers is given in the section on scrolling.

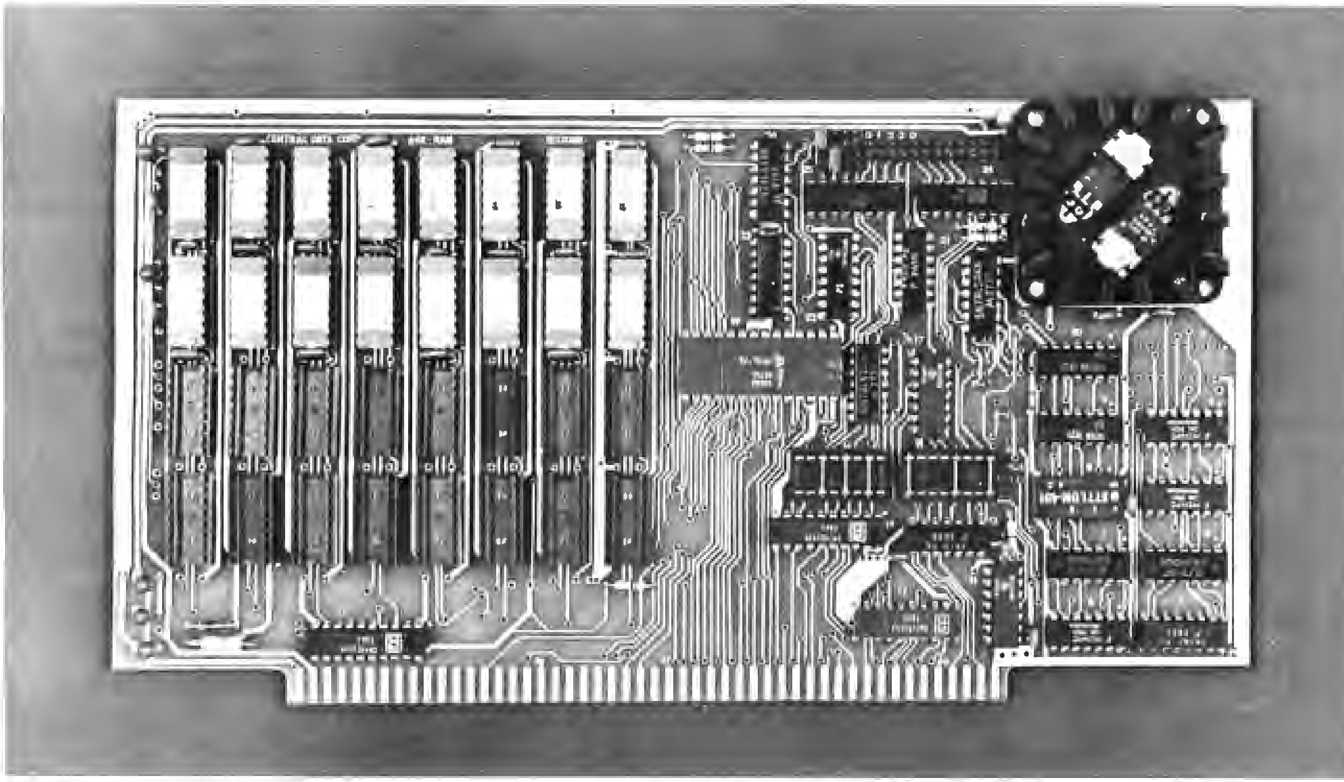
R14 and R15 Cursor location. These registers are the high order six bits (R14 and low order eight bits (R15) of the location at which the cursor is to be displayed. When the refresh address output by the 6845 equals the cursor address, a cursor output signal is activated, subject to the constraints placed on the cursor by values placed in R10 and R11. More information on cursor generation is in a later section of this article. R14 and R15 are in principle readable as well as writeable, but unless proper buffering is provided for the 6845, they cannot be read. The circuit presented in the next section does not have the proper buffering, so these registers are treated as if they were write only, and copies are maintained by the processor.

R16 and R17 Light pen. These read only registers capture the refresh memory address at the instant a pulse is received from an external light pen. The processor can thereby calculate where on the display screen the operator is pointing the light pen. I provide no circuitry to support this feature of the 6845.

Display Design Description

Figure 4 shows the schematic of the display using the Motorola MC6845. The MC6845 being a MOS device (limited in counting speed to about 3 MHz), the higher speed dot and character clock circuits are still TTL. These are the high-speed timing functions mentioned previously. They must be implemented with external TTL packages on the Intel and SMC parts as well. The National display controller includes the dot clock crystal oscillator and the character clock divider on the chip.

IC10 is a 9 MHz crystal oscillator. IC9 and IC7a divide this by 6 to produce the character clock. IC9 counts from 0 to 5; when it reaches 5, the output of IC7a goes low, conditioning IC9 to reset itself on the next clock pulse. Two variants of the character clock are used. The output of IC7a goes high when IC9 goes from 5 back to 0, and a rising edge clock pulse is needed for IC2, IC4, an IC5. A falling clock is needed for IC1 and the 6845. Furthermore, the clock supplied to IC1 must be high a minimum of 220 ns, and low a minimum of 160



32K Board Pictured Above

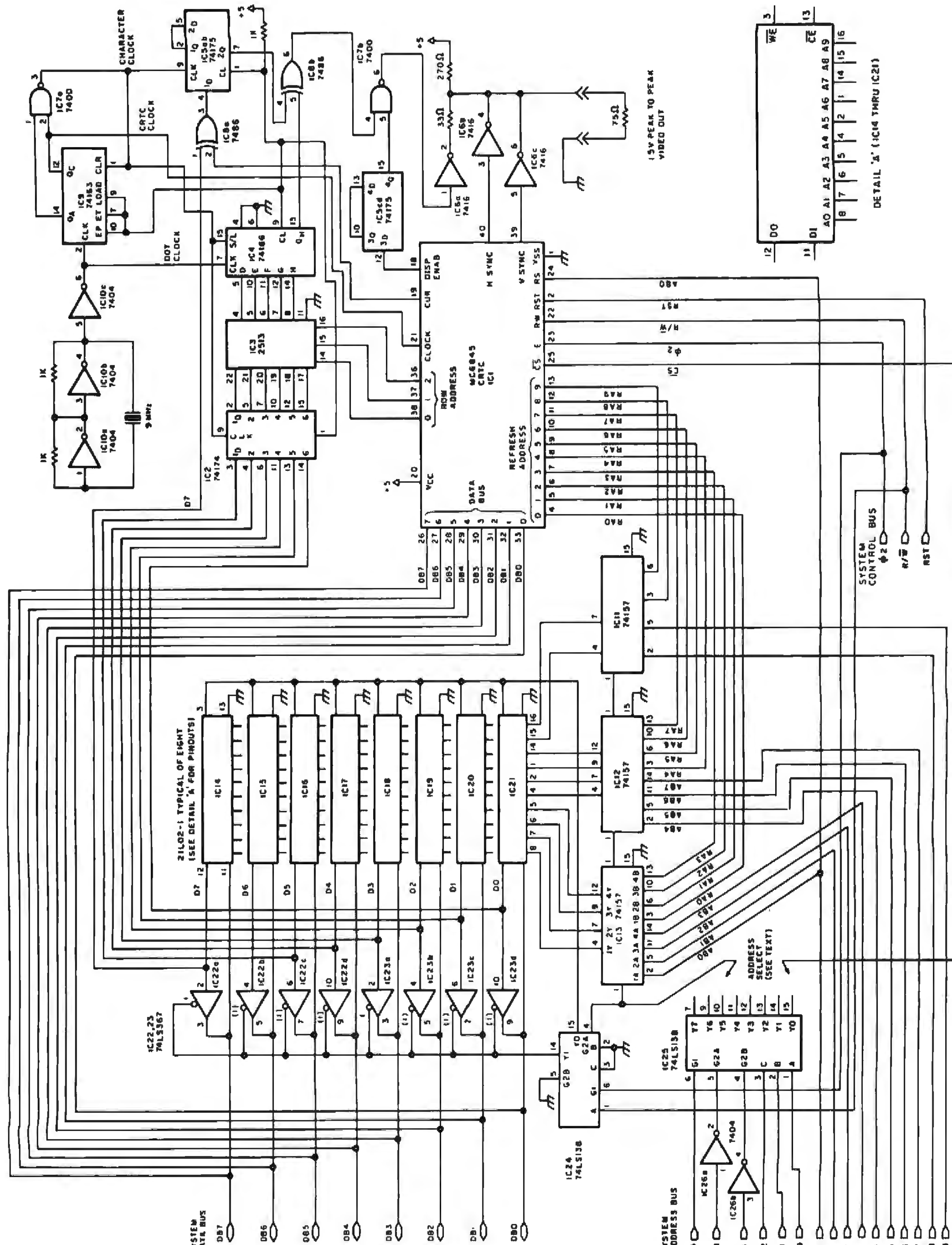


Figure 4: Schematic diagram of display circuit incorporating the MC6845 device. All integrated circuits except IC6 may be low power Schottky (LS) type.

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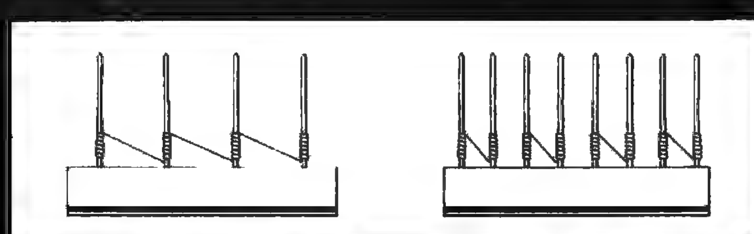

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IC2	74174	16	8		
IC3	2513	24	10	1	12
IC4	74166	16	8		
IC5	74175	16	8		
IC6	7416	14	7		
IC7	7400	14	7		
IC8	7486	14	7		
IC9	74163	16	8		
IC10	7404	14	7		
IC11	74157	16	8		
IC12	74157	16	8		
IC13	74157	16	8		
IC14	21L02-1	10	9		
IC15	21L02-1	10	9		
IC16	21L02-1	10	9		
IC17	21L02-1	10	9		
IC18	21L02-1	10	9		
IC19	21L02-1	10	9		
IC20	21L02-1	10	9		
IC21	21L02-1	10	9		
IC22	74LS367	14	7		
IC23	74LS367	14	7		
IC24	74LS138	16	8		
IC25	74LS138	16	8		
IC26	7404	14	7		

Table 4: A power pin table for the circuit in figure 4.

ns. The output of IC7a is of the wrong phase and is low for only 110 ns. Fortunately, the C output of IC9 is high for 220 ns (during counts 4 and 5), so it is used as the 6845 clock.

The 6845 presents the address of a character for refreshing the display to the memory. The memory then presents the character to the latch, IC2. The character in IC2 is then presented to the character generator, IC3. The dots for the specified scan line of the character are presented to the shift register, IC4, and shifted out at the dot clock rate to produce the video signal.

The 2 Character Pipeline

There is effectively a 2 character pipeline – one character being accessed from the refresh memory, and one character (actually one row of dots from a character) being accessed from the character generator. The two 6845 signals, *cursor* and *display enable*, must be delayed two character intervals by sections of IC5 to accommodate the pipeline effect. *Display enable* is low whenever the display is to be blanked. This includes the regions below, above, to the left, and to the right of the active display area. *Cursor* is high when the current refresh address matches the value programmed into the cursor address register pair (R14 and R15). Bit 7 of the character, the 6845 *cursor* signal, and the video signal from the shift register are combined in such a way that bit 7 being on causes reversal of the video for one character interval (changing white-on-black characters to black-on-white, or vice versa), and the 6845 *cursor* signal being on causes another reversal. Assuming the cursor has been so programmed, it can be distinguished from ordinary reversal because it will blink.

One timing consideration must be borne in mind when the MC6845 is used. The counter used in the all TTL circuit has negligible delay (20 ns) compared to the display character time (666 ns). The MC6845, being a metal oxide semiconductor device, is considerably slower, with a delay of as much as 160 ns. This delay time must be subtracted from the character time when specifying the refresh memory access time. The refresh memory integrated circuits specified in the design are "-1" suffix types (500 ns maximum access time) so the timing is satisfactory.

On the schematic diagram (figure 4), IC26 (74LS138) and IC27 (7404) are connected such that IC27 is enabled for the uppermost 8 K bytes of processor memory address space (hexadecimal E000 thru FFFF). Other connections of IC26's enable inputs (pins 4, 5, and 6) to the address lines, with or without sections of IC27, as required, can allow enabling for any 8 K memory address segment. Selection of a particular 1 K byte segment for the refresh memory is accomplished by connecting the refresh memory select line to a particular output of IC26. The CS (chip select) line from IC1, the 6845, is connected to another of the outputs of IC26. This allocates an entire 1 K byte segment to the 6845, whereas it needs only two addresses. More integrated circuits could be added to refine the decoding for the 6845 and eliminate the wasted address space.

Cursor Generation

The MC6845 provides several options for the generation of a cursor. Registers R10 and R11 control the format of the cursor, and R14 and R15 control its position. The low order five bits of R10 (bits 0 thru 4) specify the scan line on which the cursor is to start, and R11 specifies the scan line on which the cursor is to end. If R10 bits 0 thru 4 are all equal to 0, and R11 is 8, the cursor will occupy lines 0 thru 8, or the entire character. Using the circuitry presented earlier, the cursor becomes a block

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of reverse video. If the value 8 is stored in R10 bits 0 thru 4 (ie: bit 3 is on) and in R11, the cursor occupies only line 8. Hence it becomes an underscore. If values other than these are used, only a portion of the character is reversed. I have found that partial reversal makes characters difficult to read, so the only values I consider usable are (0, 8) and (8, 8).

Bits 5 and 6 of R10 control cursor blinking. If bit 5 is on and bit 6 is off, the cursor is not displayed at all. This can be used to blank the cursor to indicate the system is not accepting keyboard input. If bit 6 is on, the cursor will blink. If bit 5 is off, the blink rate is about four times per second. If bit 5 is on, the blink rate is about two times per second.

Scrolling

Scrolling is the management of a video display in the following way. New data is entered on the bottom line of the display. When the bottom line is full, the entire display is moved up one line. In the process, the top line, containing the oldest data, may be discarded, or if the display memory is larger than the portion displayed on the screen, the old display data may temporarily be kept. In the latter case, the display could be scrolled down as well as up, and the display screen could act as a moveable "window."

The data movement necessary to implement scrolling could be done by a processor program. In fact, it must be done by the processor in the case of the all TTL display design, for there is no provision for hardware scrolling in that design. A program loop to perform scrolling on a 1,024 character screen might take from 15 to 20 milliseconds on a 6502 or 6800 processor. If the source of data to the screen was a serial communications line operating at 1200 bits per second (assume the system is emulating a terminal), the time between characters is only about 8 ms, not long enough to perform a scrolling operation. (An interrupt-driven program could be written to handle both scrolling and receiving of characters from the line, but this would be complex).

The 6845 does provide scrolling because its refresh start address is programmable, and may be updated whenever necessary. Up to this point, I've used the term *scrolling* to mean "line scrolling" where data is moved around as complete lines. In this case, the refresh start address of the 6845 would be updated in increments of 64 (for the 64 character line length).

However, scrolling can be done by individual characters. If the refresh start address is incremented by one, each character in each line moves one position left, and the first character of each line moves to the last position of the previous line. Also, if the display memory is at least twice as large as the display screen, scrolling could be done by page, in which case the refresh start address would be updated by 1,024 each time (again assuming the 16 by 64 format). Since the 6845 can address up to 16 K (16,384) bytes, the refresh memory could contain up to 16 pages of data, and scrolling could be done by line or page.

The design I have presented here has a refresh memory the same size as the display screen. It uses scrolling to enter new data on the bottom line of the display, and the top line is discarded when it is displaced. An example of how such scrolling operations might be done is shown in figure 5. Figure 5a shows how the display would be initialized. The 6845 is initialized with a refresh start address of 64 (decimal). The 6845's refresh address counter runs to 1,023 at the end of the 15th line, then continues with 1,024 and up to 1,087 at the end of the 16th and last line. Since only ten of the 6845's 14 refresh address lines are connected to the refresh memory, a *wraparound* occurs the address 1,024 is equivalent (in

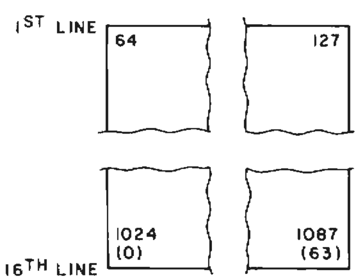

Figure 5a: Initialization for a scrolled display. Refresh addresses are shown. The differing value given in parentheses is that perceived by the refresh memory, due to wraparound.

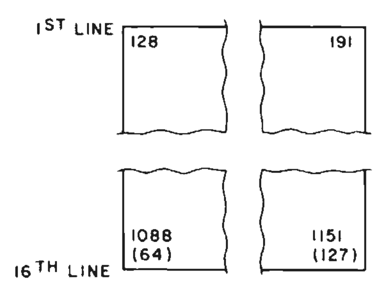

Figure 5b: Refresh addresses calculated after one scrolling operation.

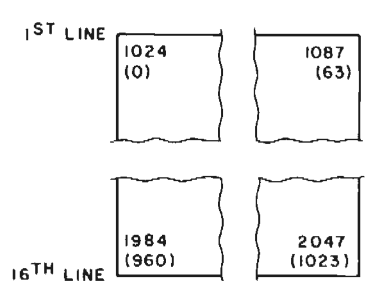

Figure 5c: Refresh addresses of last scrolling operation before the processor memory reference must be reset to 0.

the refresh memory's perception) to 0. Hence the last line of the display starts at a memory address of relative 0, from the processor's point of view. For example, if the display memory were located at processor hexadecimal addresses E000 thru E3FF, the last line of the display would start at E000.

The procedure to perform a scroll operation is as follows: increment the refresh start address by 64, update the cursor address, and prepare the processor to store new data at refresh memory locations 64 thru 127 (relative to the actual processor starting address; for the example given above, the addresses would be E040 thru E07F). Figure 5b shows the result of this scroll operation.

All addresses are incremented by 64 for each new line until the situation shown in figure 5c prevails. In order to perform another scroll operation, the processor memory address must be reset to relative 0 (E000 as above), but the 6845 refresh start address can continue to be incremented; it needn't be reset. It will eventually wrap around itself.

Note well that the cursor address register is a 14 bit register, as is the refresh start address register. All 14 bits of the cursor address must match a refresh address displayed on the screen for the cursor to be displayed. The range covered by the refresh address is determined by the refresh start address and the number of characters on the screen. If the cursor address is outside of this range, no cursor will be generated by the 6845.

Scrolling in the case of a 12 line by 80 character format (where neither of the dimensions is a power of 2) is more complicated. As shown in figure 6a, the 6845 is initialized with a refresh start address of 144, so that, at the beginning of the 12th line, the 6845 outputs the address 1024, which is equivalent to memory address 0. In figure 6b a single scroll operation has been performed. All values have been incremented by 80. So far, everything is just like the 16 by 64 case, except for the increment value. In figure 6c, the last "simple" scroll has occurred, and things get more complicated from this point. In figure 6d the result of another scroll operation is shown. Again, all values have been incremented by 80, but as can be seen, memory wraparound occurs within the display line. In the 16 by 64 case, wraparound always occurs between lines, and it is relatively easy for a processor program to deal with. In the 12 line by 80 character case, the processor program must be aware that wraparound can occur with a line, and it must act accordingly.

Device Availability

The SMC 5027 and the Intel 8275 (along with its associated 8257 controller) have been available for some time from computer hobbyist vendors. The 5027 was originally priced at about $50, but may be available for less than that now in view of increasing competition. The Intel 8275 and 8257 pair are available for under $100. The Motorola MC6845 is available from regular electronics distributors. It usually costs about $30. The National DP8350 is the most recently announced of the four parts, so its price and availability may still fluctuate.

There are other video display controllers besides the four I have covered in this article. There will probably be even more announced by the time it is published and prices can be expected to fall as competition heats up.■

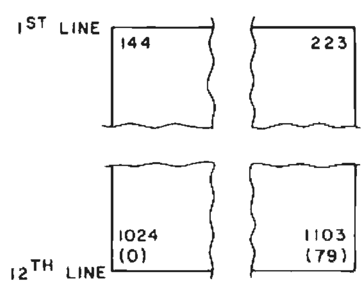

Figure 6a: Address initialization for a 12 line by 80 character display.

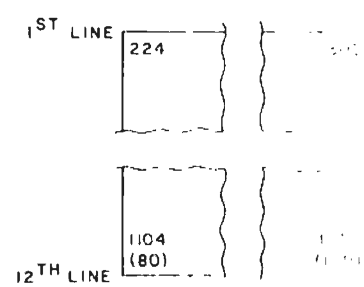

Figure 6b: Addresses for a 12 by 80 display following one scroll operation

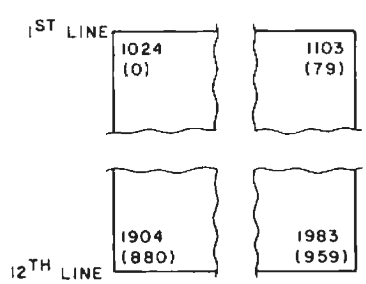

Figure 6c: The last scroll operation before memory wraparound occurs.

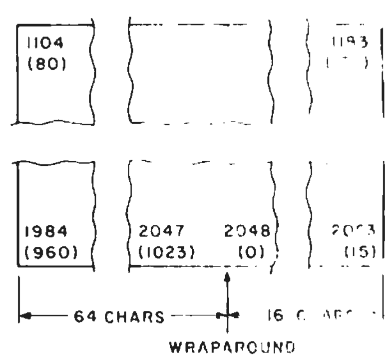

Figure 6d: Memory wraparound. All values have been incremented by 80, but wraparound occurs within the display line. In the 12 line by 80 character format, the processor program must take special action at this wraparound event.

Text continued from page 12:
have publications in which geographic coordinates for data base construction exist in both tabular and graphic form. Though somewhat tedious, tabular data can be keyed into the computer easily and saved in mass storage. If you have access to a graphics pad input device, you can quickly extract data directly from existing maps.

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An easier way to go about setting up a data base is to obtain a ready-made one. You can buy one from a commercial establishment or from an individual (expensive, in either case), or you might be able to get one free from a government agency or a university. There are so many different data bases in existence that it is best for you to first decide exactly what you need, then directly contact the agencies that would be most likely to have what you want.

Many observatories, including university observatories, have extensive data bases for astronomical uses, free for the asking. As far as government agencies are concerned, your best bets are with the National Oceanic and Atmospheric Administration (6010 Executive Blvd, Rockville MD 20852), the National Technical Information Service (Room 620, 425 Thirteenth St NW, Washington DC 20004), and the US Geological Survey (National Center, 12201 Sunrise Valley Dr, Reston VA 22092). These agencies have many kinds of data bases, covering all parts of the world. Depending upon what you need, there may or may not be a charge for the material.

One drawback to obtaining data bases from agencies such as these is that they may not be in a format that you can use directly. For example, you may find that the data you need is available only on standard 7 or 9 track computer tape, and you will have to find a way to read it and convert it into a format you can use.

Sample Mapping Programs

The field is so broad that it is impossible to discuss here all of the projections in common use. Therefore, I have selected a few of the simplest and most common map projections to serve as illustrations of the techniques involved. For each example discussed, a program listing is included, as well as a number of maps actually generated by the programs. Many readers will find immediate application for one or more of the sample projections, exactly as they are demonstrated. Others will want to make modifications, and still others will want to delve deeper into the subject. A visit to your local library will turn up useful books which explain map projections, their uses, and the mathematics required to carry them out.

In all of the examples which follow, it is assumed that the geographic coordinates (latitudes and longitudes) in the data base are in radians, and that they are being converted to rectangular X,Y map coordinates (measured usually in centimeters or inches). Standard trigonometric convention is used for the algebraic signs of the coordinates. In other words, for the geographic coordinates, north latitudes are positive; south latitudes are negative; east longitudes are positive; west longitudes are negative. It is further assumed that the origin (0,0) of the map coordinate system is at the center of the map, with the X axis positive to the right, and the Y axis positive toward the top. There may be some slight variation between this standard system and your own graphics device, but at most it would require only a simple translation or rotation of the coordinates.

Each of the examples is demonstrated as a subroutine, which is to be called once for each pair of coordinates in the data base. Before the first call is made to the subroutine, certain initial parameters must have already been defined, and these are noted in the remarks accompanying each subroutine.

For each call made, the main program supplies a pair of geographic coordinates from the data base, and the subroutine returns the rectangular map coordinates. Grid lines, when desired, may be created by generating sets of "artificial" geographic coordinates within loops in the main program, then calling the appropriate conversion routine to get the map coordinates to draw them with. Any labeling or annotation of the maps would also be carried out by the main program.

Listing 1: Subroutine to compute map coordinates for rectangular projection.

```
     REM  SUBROUTINE TO COMPUTE MAP COORDINATES FOR
     REM  RECTANGULAR PROJECTION.
     REM
     REM
     REM  THE FOLLOWING VARIABLES MUST BE DEFINED BEFORE
     REM  THIS SUBROUTINE IS CALLED:
     REM
     REM  L1 IS THE GEOGRAPHIC LONGITUDE AT THE
     REM     LEFT-HAND LIMIT OF THE MAP.
     REM
     REM  L2 IS THE GEOGRAPHIC LONGITUDE AT THE
     REM     RIGHT-HAND LIMIT OF THE MAP.  IF THE MAP
     REM     CROSSES THE 180-DEGREE MERIDIAN (I.E.,
     REM     L1>L2), THEN L2 MUST BE REDEFINED AS
     REM     L2 = L2 + 6.2831853.
     REM
     REM  P1 IS THE GEOGRAPHIC LATITUDE AT THE BOTTOM
     REM     LIMIT OF THE MAP.
     REM
     REM  P2 IS THE GEOGRAPHIC LATITUDE AT THE TOP LIMIT
     REM     OF THE MAP.
     REM
     REM  C1 IS THE GEOGRAPHIC LONGITUDE AT THE CENTER
     REM     OF THE MAP, WHERE C1 = (L1+L2)/2.0, AND
     REM     MUST HAVE BEEN COMPUTED AFTER L2 WAS
     REM     REDEFINED IF IT WAS NECESSARY TO DO SO.
     REM
     REM  C2 IS THE GEOGRAPHIC LATITUDE AT THE CENTER
     REM     OF THE MAP, WHERE C2 = (P1+P2)/2.0
 290 REM
 300 REM  F1 IS THE MAP SCALE FACTOR IN THE HORIZONTAL
 310 REM     (EAST-WEST) DIRECTION.  F1 = D1/(L2-L1),
 320 REM     WHERE D1 IS THE MAP LENGTH, IN CENTIMETERS
 330 REM     OR INCHES, IN THE EAST-WEST DIRECTION.
 340 REM
 350 REM  F2 IS THE MAP SCALE FACTOR IN THE VERTICAL
 360 REM     (NORTH-SOUTH) DIRECTION.  F2 = D2/(P2-P1),
 370 REM     WHERE D2 IS THE LENGTH IN CENTIMETERS OR
 380 REM     INCHES OF THE MAP IN THE NORTH-SOUTH
 390 REM     DIRECTION.
 400 REM
 410 REM  N  IS A FLAG TO INDICATE WHETHER THE MAP
 420 REM     CROSSES THE 180-DEGREE MERIDIAN (THAT IS,
 430 REM     WHETHER L1>L2 BEFORE L2 IS REDEFINED).
 440 REM     N=0 MEANS THAT THE MAP DOES NOT CROSS THE
 450 REM     180-DEGREE MERIDIAN.  N<>0 MEANS THAT THE
 460 REM     MAP DOES CROSS IT.
 470 REM
 480 REM  L  IS THE GEOGRAPHIC LONGITUDE (OBTAINED FROM
 490 REM     THE DATA BASE) OF THE POINT BEING CONVERTED.
 500 REM
 510 REM  P  IS THE GEOGRAPHIC LATITUDE (OBTAINED FROM
 520 REM     THE DATA BASE) OF THE POINT BEING CONVERTED.
 530 REM
 540 REM
 550 REM  THE FOLLOWING VARIABLES ARE COMPUTED BY THIS
 560 REM  SUBROUTINE:
 570 REM
```

Listing 1 continued on page 80

The flowchart in figure 1 has illustrated the principal features of the main program, and no attempt will be made here to detail it further, since there would be some variation dependent upon your own hardware. In any case, it will be quite straightforward and simple.

The remarks included in the listings fully explain the operation and use of each subroutine, so those aspects will not be repeated in detail in the text. In fact, the greatest part of each listing is composed of remarks, with the actual executable portion comprising only about ten to 20 statements in each case.

Rectangular Projections

This is probably the simplest projection in existence, and requires an absolute minimum of mathematics to generate. The meridians and parallels are simply laid out as equally spaced straight lines at right angles to each other. You can take a standard sheet of graph paper, for example, and let each space in the horizontal direction equal a degree of longitude, and each space in the vertical direction equal a degree of latitude. Plot a few geographic coordinates on the graph paper in this manner and you have a rectangular projection.

The computer, of course, can do the job faster, and the subroutine given in listing 1 will serve quite nicely. Notice that no trigonometry is required, and that the actual conversion requires only two statements. Consequently, this type of projection can be carried out very rapidly, even when a large data base is involved.

The rectangular projection is not a real "projection" in the true sense of the word, since it is arranged arbitrarily and there is no direct geometric relationship between it and the surface of the Earth. Nevertheless, for many purposes it works very well, especially if the latitudinal (north-south) extent of the area being mapped is not too great. It works best for areas near the equator, and becomes useless near the poles. (The meridians on the Earth converge at the poles, whereas they remain parallel to each other on the projection. The resultant distortion above about 50 or 60 degrees latitude is usually unacceptable.)

The accuracy of the projection can be significantly improved if the horizontal map scale factor, F1, is adjusted to compensate for the convergence of the meridians. We can do this in the main program by computing F2 first, then computing F1 by F1 = F2 X COS(C2). This does not eliminate the convergence problem, but it does reduce its effect.

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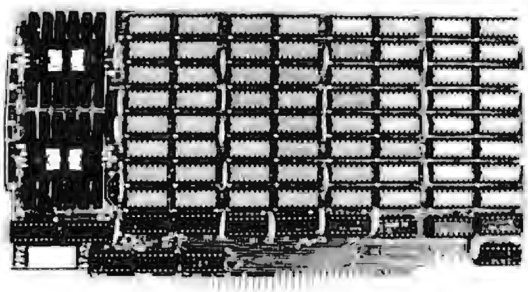

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This 8K board is available in two versions. The 8KS-B operates at 450ns for use with 8080 and 8080A microprocessor systems and Z-80 systems operating at 2MHz. The 8KS-Z operates at 250ns and is suitable for use with Z-80 systems operating at 4MHz. Both kits feature factory fresh 2102's (low power on 8KS-B) and includes sockets for all IC's. Support logic is low power Schottky to minimize power consumption. Address and data lines are fully buffered and 4K bank addressing is DIP switch selectable. Memory Protect/Unprotect, selectable wait states and battery backup are also designed into the board. Circuit boards are solder masked and silk-screened for ease of construction. These kits are the best memory value on the market! Available from stock . . . **8KS-B $125** (assembled and tested add $25.00)
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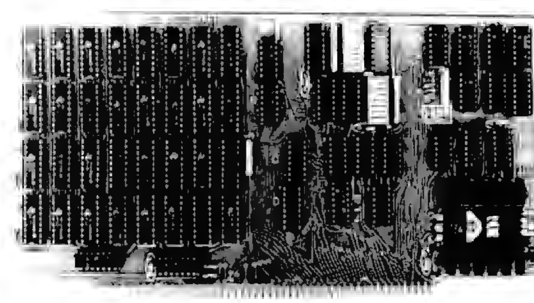

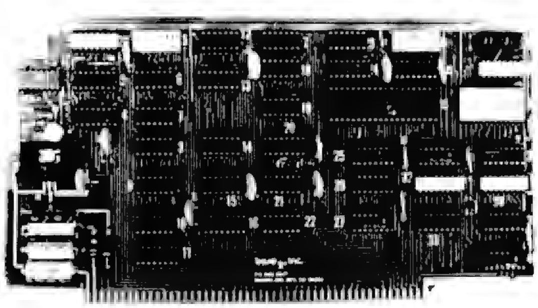

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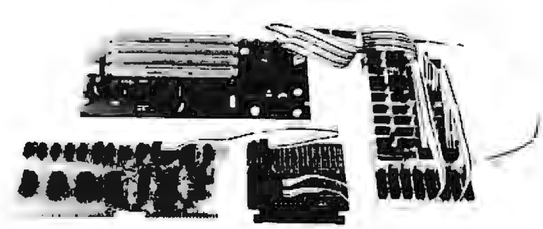

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Listing 1 continued from page 78:

```
4580    REM     S  IS THE OFF-SCALE FLAG.  S=0 MEANS ON-SCALE.
4590    REM        S=1 MEANS OFF-SCALE.
4600    REM
4610    REM     X  IS THE MAP X-COORDINATE, IN CENTIMETERS OR
4620    REM        INCHES.
4630    REM
4640    REM     Y  IS THE MAP Y-COORDINATE, IN CENTIMETERS OR
4650    REM        INCHES.
4660    REM
4670    REM
4680 LET S = 0
4690    REM     IF THE MAP CROSSES THE 180-DEGREE MERIDIAN,
4700    REM     AND THE LONGITUDE OF THE POINT FROM THE DATA
4710    REM     BASE IS NEGATIVE, REDEFINE THE LONGITUDE AS
4720    REM     A POSITIVE ANGLE.
4730 IF   N = 0  THEN 4780
4740 IF   L >= 0  THEN 4780
4750 LET L = L + 6.2831853
4760    REM     IF THE POINT IS OUTSIDE THE LIMITS OF THE MAP,
4770    REM     SET THE OFF-SCALE FLAG AND RETURN.
4780 IF   L < L1  THEN 4820
4790 IF   L > L2  THEN 4820
4800 IF   P < P1  THEN 4820
4810 IF   P <= P2  THEN 4860
4820 LET S = 1
4830 RETURN
4840    REM     COMPUTE THE MAP COORDINATES FROM THE
4850    REM     GEOGRAPHIC COORDINATES.
4860 LET X = (L - C1) * F1
4870 LET Y = (P - C2) * F2
4880 RETURN
4890 END
```

The map of the continental United States shown in figure 2 was generated with the rectangular projection routine. Even though the area being mapped does not meet the requirements for high accuracy (ie: it is far from the equator; it has a fairly large latitudinal extent; and in the case of this particular map, F1 was not corrected for convergence of the meridians), it is still entirely satisfactory for many purposes.

Another interesting thing about the map in figure 2 is that it is made up entirely of dots. In response to an article of mine which appeared in another magazine, I received about three thousand letters over a period of about four weeks. These were requests for technical data which required that the geographic coordinates for the center of the person's town be supplied. This resulted in a ready-made data base, and I became curious as to its distribution. It was a simple matter to have the computer examine the data base and draw a dot for each city represented (eliminating duplications), using a rectangular projection.

Notice that all dots are the same size, and

Figure 2: Rectangular projection of the continental United States. Dots represent locations of selected cities.

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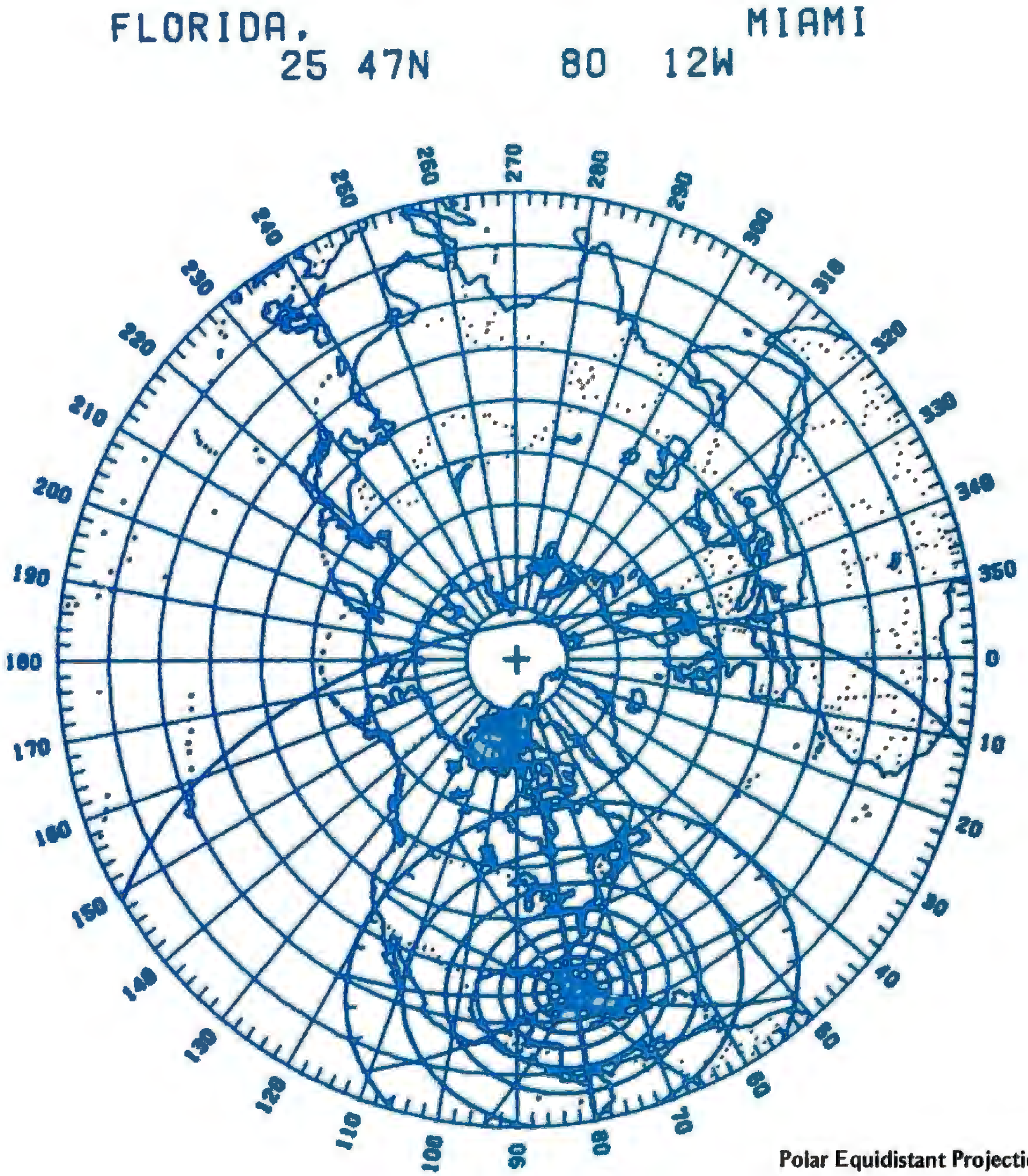

Figure 3: Polar equidistant projection of the northern hemisphere. This map is overlaid with OSCAR satellite tracking information for use by a ground station located at Miami FL.

0-6.7
NORTHERN
HEMISPHERE

that only one dot was drawn for each city, regardless of its population and regardless of how many letters were received from the city. No dot was drawn for any city (regardless of its size) unless at least one letter was received from it.

It took only a few minutes to set up the program to make the map, and only a few seconds for the computer to draw it. I then had an excellent graphical illustration of what I could only guess at by looking at the listing of the data base.

Polar Equidistant Projections

This is another rather simple projection, but one which has many important uses. Figures 3 and 4 show polar equidistant projections of the northern and southern hemispheres, respectively. The parallels are drawn as equally spaced concentric circles, and the meridians as equally spaced radii. As seen in listing 2, the polar form of the map coordinates can be represented directly from the geographic coordinates by (PI/2-P,L), where P and L are the latitude and longitude, respectively. (PI/2, of course, is the equivalent of 90° expressed in radians.) These in turn are directly converted to rectangular coordinates by the standard polar-to-rectangular conversion formulas. The entire process requires only three statements in the subroutine.

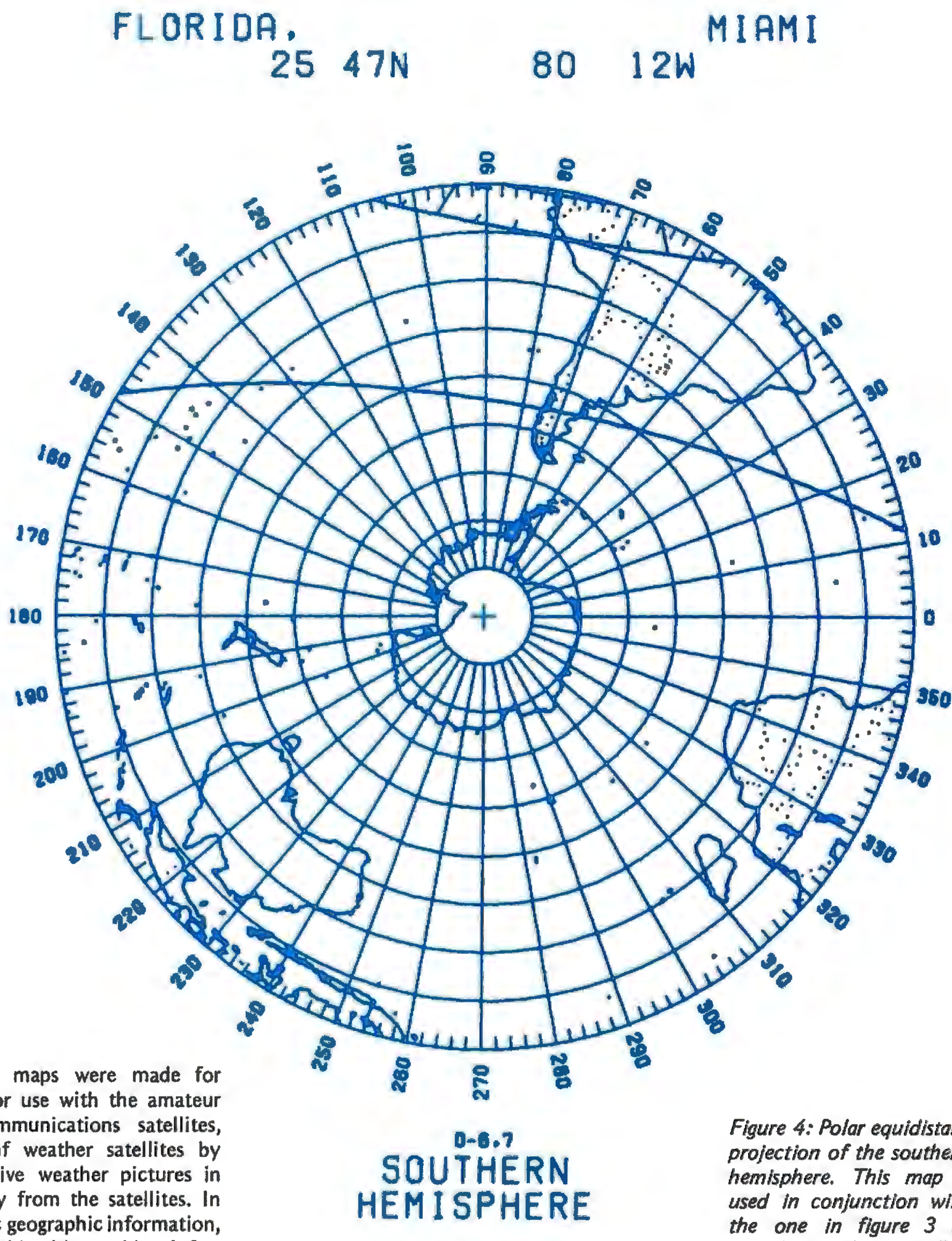

Figure 4: Polar equidistant projection of the southern hemisphere. This map is used in conjunction with the one in figure 3 to complete the satellite tracking coverage south of the equator.

These particular maps were made for satellite tracking, for use with the amateur radio OSCAR communications satellites, and for tracking of weather satellites by amateurs who receive weather pictures in their homes directly from the satellites. In addition to the basic geographic information, the maps are overlaid with tracking information based on the location at which the map is to be used (Miami FL, in this case). The set of interconnected concentric "circles" around Miami are elevation angle contour lines. The radial lines that connect them are azimuth angle contour lines.

The satellite's position over the surface of the Earth is plotted on the map, and if it falls anywhere within the interconnected "circles" it is within range of the ground station. The station antenna can then be pointed at the satellite, based on the information derived from the map. The radial lines give the antenna azimuth angle from true north in 30° increments (with additional 10° tick marks around the outer elevation contour). The concentric "circles" give the antenna elevation angle in 10° increments, starting with the outermost circle at 0° elevation (ie: the satellite is exactly on the horizon at this point). The elevation increases inward, with the innermost circle being 80°, and the dot at the center (the location of the ground station) being 90° (ie: directly overhead).

The far outside arc, which is not connected to the inner elevation circles, shows the maximum communications range through the satellite. In order for the ground station to see and access the satellite, the satellite's ground track must lie within the inner set of interconnected circles, but once it comes within that area the spacecraft will relay the signals to a far greater range. The distant unconnected circle shows what the maximum possible range is. When used for

Listing 2: Subroutine to compute map coordinates for polar equidistant projection.

```
3000   REM    SUBROUTINE TO COMPUTE MAP COORDINATES FOR
3010   REM    POLAR EQUIDISTANT PROJECTION.
3020   REM
3030   REM
3040   REM    THE FOLLOWING VARIABLES MUST BE DEFINED BEFORE
3050   REM    THIS SUBROUTINE IS CALLED:
3060   REM
3070   REM    P  IS THE GEOGRAPHIC LATITUDE (OBTAINED FROM
3080   REM       THE DATA BASE) OF THE POINT BEING CONVERTED.
3090   REM
3100   REM    L  IS THE GEOGRAPHIC LONGITUDE (OBTAINED FROM
3110   REM       THE DATA BASE) OF THE POINT BEING CONVERTED.
3120   REM
3130   REM    F  IS THE MAP SCALE FACTOR, EQUAL TO
3140   REM       D/3.1415927, WHERE D IS THE DIAMETER (IN
3150   REM       CENTIMETERS, INCHES, ETC.) OF THE FINISHED
3160   REM       MAP.
3170   REM
3180   REM    H  IS A FLAG TO INDICATE WHICH HEMISPHERE IS
3190   REM       BEING DRAWN.  H=0 MEANS NORTHERN HEMISPHERE.
3200   REM       H<>0 MEANS SOUTHERN HEMISPHERE.
3210   REM
3220   REM
3230   REM    THE FOLLOWING VARIABLES ARE COMPUTED BY THIS
3240   REM    SUBROUTINE:
3250   REM
3260   REM    S  IS THE OFF-SCALE FLAG.  S=0 MEANS ON-SCALE.
3270   REM       S=1 MEANS OFF SCALE.
3280   REM
3290   REM    R1 IS TEMPORARY STORAGE.
3300   REM
3310   REM    X  IS THE MAP X-COORDINATE IN CENTIMETERS OR
3320   REM       INCHES.
3330   REM
3340   REM    Y  IS THE MAP Y-COORDINATE IN CENTIMETERS OR
3350   REM       INCHES.
3360   REM
3370   REM
3380 LET S = 0
3390   REM    IF THE POINT FROM THE DATA BASE IS NOT IN THE
3400   REM    HEMISPHERE BEING DRAWN, SET THE OFF-SCALE FLAG
3410   REM    AND RETURN.
3420 IF  H = 0  THEN 3490
3430 IF  P > 0.0  THEN 3500
3440   REM    FOR A SOUTHERN HEMISPHERE MAP, CHANGE THE SIGN
3450   REM    OF THE LONGITUDE TO MAINTAIN THE PROPER MAP
3460   REM    ORIENTATION.
3470 LET L = -L
3480 GO TO 3540
3490 IF  P >= 0.0  THEN 3540
3500 LET S = 1
3510 RETURN
3520   REM    COMPUTE THE MAP COORDINATES FROM THE
3530   REM    GEOGRAPHIC COORDINATES.
3540 LET R1 = F * (1.5707963 - ABS(P))
3550 LET X = R1 * COS(L)
3560 LET Y = R1 * SIN(L)
3570 RETURN
3580 END
```

weather satellite tracking, this circle takes on a slightly different meaning. In that case, it shows the most distant land areas that the station can expect to receive pictures of.

In practice, a transparent plastic overlay showing the satellite's ground track is placed over the map to find the position at any given moment. Since the shape of the orbit doesn't change, only one ground track overlay is needed, and it is simply rotated on the map to match up with the point where the satellite crosses the equator on that particular pass.

A more elegant system, however, is to generate the map and tracking overlays on a video display. The satellite's current location can be displayed as a flashing dot whose position is constantly updated in a real-time mode.

Returning to the matter of the map itself, one realizes that the orientation of the map need never be changed, regardless of where the ground station is located. The subroutine shown in listing 2 generates the map from geographic coordinates, but this really needs to be done only once. A new data base can be made up of *map* coordinates, and every time a map is to be drawn the map coordinates can be fed directly to the graphics device without having to go through the conversion calculations.

On the other hand, the azimuth-elevation tracking overlays will change in position, size, and shape for every different ground station location and for every different satellite. A separate subroutine is required to generate sets of geographic coordinates to define the overlays, and that subroutine would in turn call the subroutine given in listing 2 in order to get the map coordinates with which to draw the overlays.

Although the maps shown in figures 3 and 4 stop at the equator, they can be extended further with no change in the program. In fact, it would be advantageous in this particular application to extend each of them another 20 or 30 degrees to provide some overlap. Extension much beyond 40 degrees, however, will result in excessive distortion.

As a final note about the satellite tracking maps, you may have noticed that the longitudes are labeled from 0 to 360 degrees. Not only that, they are positive *westward*. This convention used in satellite tracking is an exception to the standard rule stated earlier. But as far as we are concerned it makes no difference. It is simply the way the map is *labeled*. Our data base and conversion subroutine still use the standard convention to generate the map.

While we have concentrated on one specific application of the polar equidistant

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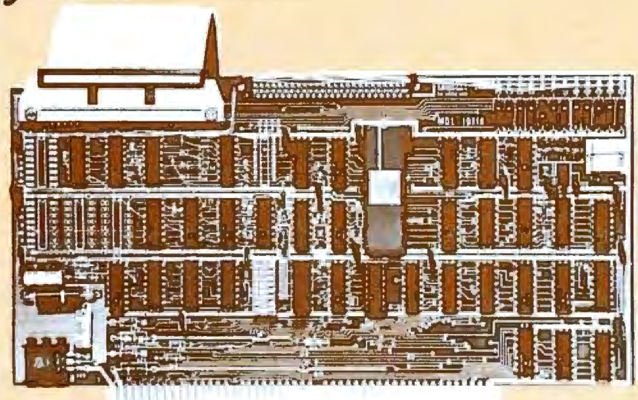

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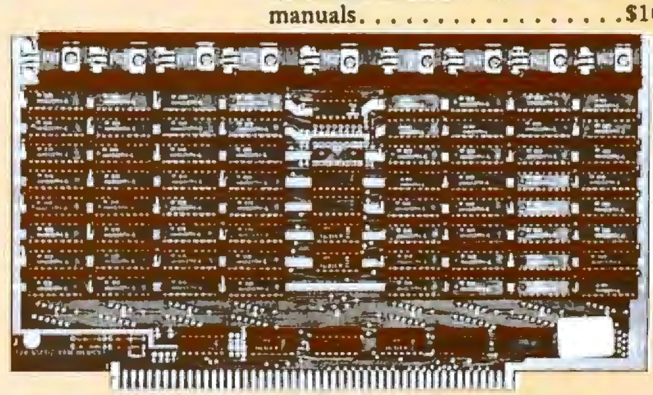

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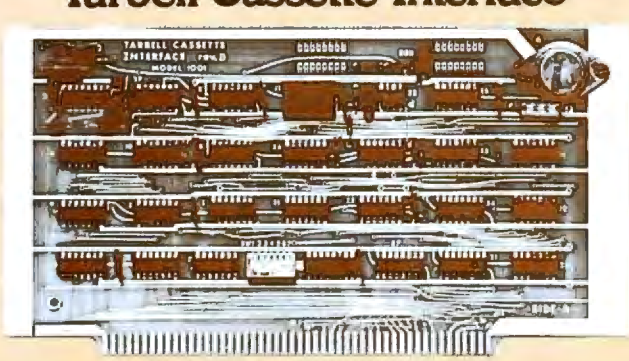

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```
1000 REM    SUBROUTINE TO COMPUTE MAP COORDINATES FOR
1010 REM    ORTHOGRAPHIC EQUATORIAL PROJECTION.
1020 REM
1030 REM
1040 REM    THE FOLLOWING VARIABLES MUST BE DEFINED BEFORE
1050 REM    THIS SUBROUTINE IS CALLED:
1060 REM
1070 REM    LO IS THE REFERENCE LONGITUDE (LONGITUDE AT
1080 REM       CENTER OF MAP).
1090 REM
1100 REM    P  IS THE GEOGRAPHIC LATITUDE (OBTAINED FROM
1110 REM       THE DATA BASE) OF THE POINT BEING CONVERTED.
1120 REM
1130 REM    L  IS THE GEOGRAPHIC LONGITUDE (OBTAINED FROM
1140 REM       THE DATA BASE) OF THE POINT BEING CONVERTED.
1150 REM
1160 REM    R  IS THE RADIUS OF THE FINISHED MAP, IN
1170 REM       CENTIMETERS, INCHES, ETC.
1180 REM
1190 REM
1200 REM    THE FOLLOWING VARIABLES ARE COMPUTED BY THIS
1210 REM    SUBROUTINE:
1220 REM
1230 REM    S  IS THE OFF-SCALE FLAG.  S=0 MEANS ON-SCALE.
1240 REM       S=1 MEANS OFF-SCALE.
1250 REM
1260 REM    R1 IS TEMPORARY STORAGE.
1270 REM
1280 REM    X  IS THE MAP X-COORDINATE, IN CENTIMETERS OR
1290 REM       INCHES.
1300 REM
1310 REM    Y  IS THE MAP Y-COORDINATE, IN CENTIMETERS OR
1320 REM       INCHES.
1330 REM
1340 REM
1350 LET S = 0
1360 REM    ROTATE THE GEOGRAPHIC LONGITUDE OF THE POINT
1370 REM    FROM THE DATA BASE TO REFERENCE IT TO THE MAP
1380 REM    CENTER LONGITUDE.
1390 LET L = L - LO
1400 REM    NORMALIZE THE ROTATED LONGITUDE BETWEEN -180
1410 REM    DEGREES AND +180 DEGREES (-PI AND +PI).
1420 IF  L <= 3.1415927  THEN 1450
1430 LET L = L - 6.2831853
1440 GO TO 1490
1450 IF  L >= -3.1415927  THEN 1490
1460 LET L = L + 6.2831853
1470 REM    IF OFF-SCALE (OUTSIDE THE RANGE FROM -PI/2 TO
1480 REM    +PI/2), SET FLAG AND RETURN.
1490 IF  L < -1.5707963  THEN 1510
1500 IF  L <= 1.5707963  THEN 1550
1510 LET S = 1
1520 RETURN
1530 REM    COMPUTE THE MAP COORDINATES FROM THE
1540 REM    GEOGRAPHIC COORDINATES.
1550 LET R1 = R * SIN(1.5707963 - ABS(P))
1560 LET X = R1 * SIN(L)
1570 LET Y = R * SIN(P)
1580 RETURN
1590 END
```

Listing 3: Subroutine to compute map coordinates for orthographic equatorial projection.

map (and a very important and useful application at that), one should remember that there are many other uses for it. Even if you have no interest in communications or weather satellites, you will probably sooner or later come across an application where it suits your needs perfectly.

Orthographic Equatorial Projections

Perspective projections are those which show the Earth exactly as it appears when viewed from some point in space. These are especially useful for generating images of the Earth for use in spaceship maneuvering, and for generating outline maps for overlay on weather satellite photos. In the orthographic equatorial projection, the point of view is at infinity, and level with the equator. As complex as this might sound, the math is actually very simple, and the entire procedure requires only about a half dozen statements in the conversion subroutine, which is given in listing 3.

Figures 5 and 6 show a pair of maps generated by the program — the former centered on 70° west longitude and the latter on 90° east longitude. These are quite spectacular to generate in rapid succession on a video display, simulating the rotation of the Earth or the passage of a spacecraft around the earth. Incrementing the center longitude by five or ten degrees between images gives a sufficiently smooth transition for most purposes, but the increment can be made as small as desired.

It is true that not all spacecraft orbit the Earth at the equator, and the point of view is somewhat closer than infinity. For games, however, the simplicity of the mathematics required for projection often outweighs other considerations.

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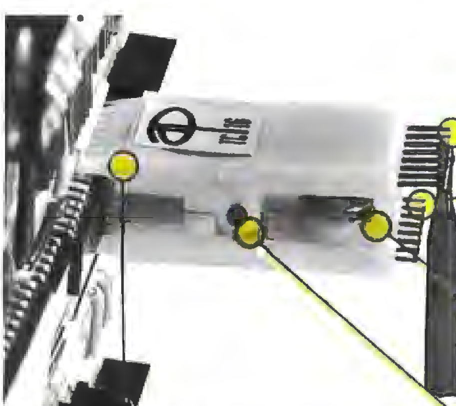

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Figure 5: Orthographic equatorial projection centered on 70° west longitude. This is a perspective view of the Earth, similar to that seen from a spacecraft in a high orbit above the equator.

If you need a more exact projection, pull out an old high school text on solid geometry or analytic trigonometry and you can come up with the formulas you need to generate a map projected from any altitude over any point on the Earth. You will need to go ahead and do this if you plan to generate map overlays for weather satellite photos, since some of the satellites are in very low orbits. TIROS-N, for example, is only about 854 km (531 miles) above the Earth's surface, and can see an area only about 6251 km (3884 miles) in diameter at any given moment. The picture image it transmits covers a significantly smaller area.

By the time you get to the height of a geosynchronous satellite (35,800 km or 22,250 miles), you see all but about 9 degrees around the edges of the Earth's disc. That's less than the last little sliver between the outer edge and the outermost meridian lines on the maps in figures 5 and 6. At the distance of the moon, you miss less than one degree, so the orthographic projection is virtually perfect at this distance. That's also why most maps of the moon are printed using an orthographic equatorial projection.

If you do write a subroutine to generate close-up perspective projections, you may find that in some cases the trouble is repaid with the advantage of needing to handle a considerably smaller portion of the data base at any given time. This is true because so much less of the Earth is visible in any one close-up projection. Depending upon exactly what you are doing, you may be able to partition the data base in such a manner that smaller hunks of it need to be accessed at a given time, cutting down on unnecessary input and output operations.

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Figure 6: Orthographic equatorial projection centered on 90° east longitude. Here, the same type of projection as used in figure 5 is employed, but the view has been rotated 160° to the east.

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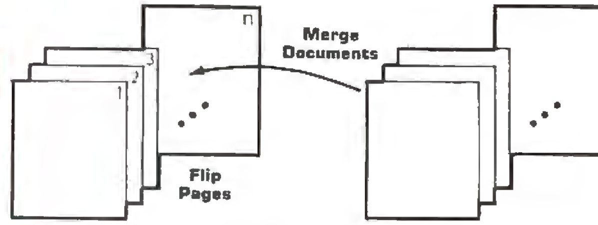

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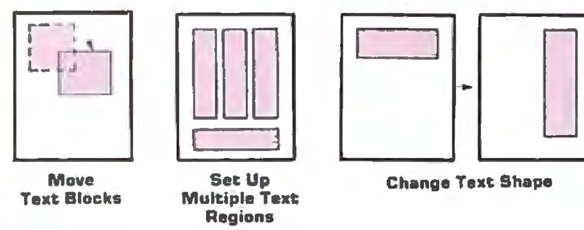

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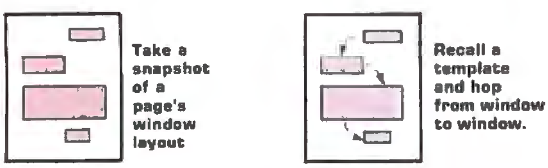

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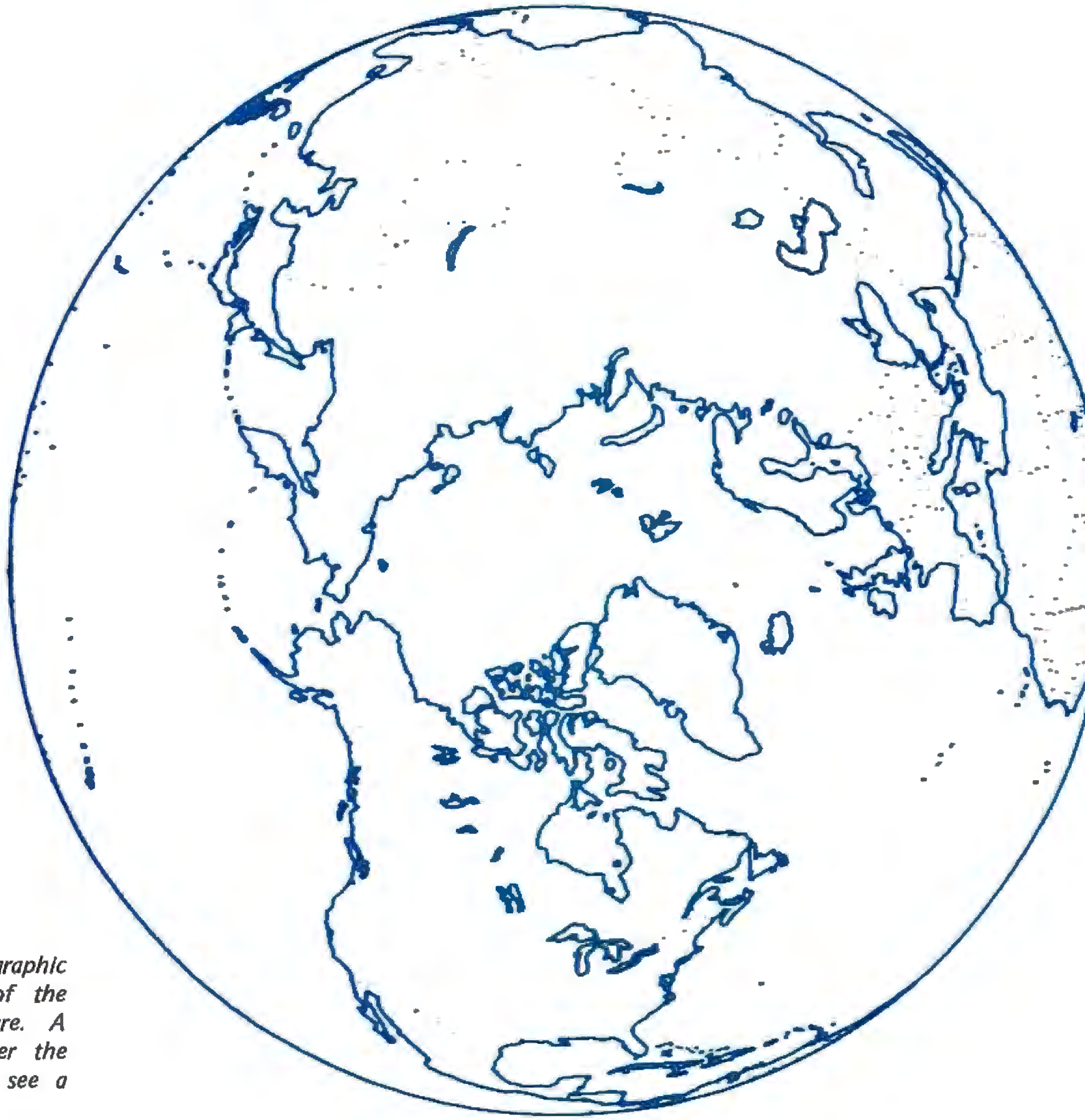

Figure 7: Orthographic polar projection of the northern hemisphere. A spacecraft high over the north pole would see a view similar to this.

```
2000    REM    SUBROUTINE TO COMPUTE MAP COORDINATES FOR
2010    REM    ORTHOGRAPHIC POLAR PROJECTION.
2020    REM
2030    REM
2040    REM    THE FOLLOWING VARIABLES MUST BE DEFINED BEFORE
2050    REM    THIS SUBROUTINE IS CALLED:
2060    REM
2070    REM    P  IS THE GEOGRAPHIC LATITUDE (OBTAINED FROM
2080    REM       THE DATA BASE) OF THE POINT BEING CONVERTED.
2090    REM
2100    REM    L  IS THE GEOGRAPHIC LONGITUDE (OBTAINED FROM
2110    REM       THE DATA BASE) OF THE POINT BEING CONVERTED.
2120    REM
2130    REM    R  IS THE RADIUS OF THE FINISHED MAP, IN
2140    REM       CENTIMETERS, INCHES, ETC.
2150    REM
2160    REM    H  IS A FLAG TO INDICATE WHICH HEMISPHERE IS
2170    REM       BEING DRAWN.  H=0 MEANS NORTHERN HEMISPHERE.
2180    REM       H><0 MEANS SOUTHERN HEMISPHERE.
2190    REM
2200    REM
2210    REM    THE FOLLOWING VARIABLES ARE COMPUTED BY THIS
2220    REM    SUBROUTINE:
2230    REM
2240    REM    S  IS THE OFF-SCALE FLAG.  S=0 MEANS ON-SCALE.
2250    REM       S=1 MEANS OFF-SCALE.
2260    REM
2270    REM    R1 IS TEMPORARY STORAGE.
2280    REM
```

Listing 4: Subroutine to compute map coordinates for orthographic polar projection.

Orthographic Polar Projections

This is another special case of the perspective projection where the point of projection is at infinity. This time, however, the viewpoint is located directly over the poles. As seen in figures 7 and 8, maps of this projection suffer from compression of geographic features near the equator, but this is a minor drawback considering the ease with which they are generated. Grid lines for the meridians and parallels were omitted from these two particular maps, so the distortion is really not so noticeable unless someone points it out to you. The differences near the equator will be apparent if you compare these maps to the polar equidistant maps in

Figure 8: Orthographic polar projection of the southern hemisphere. The projection is the same as in figure 7, but the vantage point has been shifted to a point above the south pole.

figures 3 and 4. Nevertheless, those maps are mathematical projections designed for specific purposes, and the orthographic polar maps are much more realistic for other purposes (the orbiting spaceships, for example).

The subroutine used to generate these maps is shown in listing 4, where only three statements are required for the conversion process. Although this sample routine does not provide for rotation of the map, this can be implemented by the inclusion of one additional statement. All you need to do is add the desired rotation angle to the geographic longitude (L) of the point being converted. (Some systems may also require that the resultant angle be normalized before it is used in the trigonometric function.)

Azimuthal Equidistant Projections

Here we come to one of the most interesting projections in common use. The azimuthal equidistant projection, also

Listing 4 continued:

```
2290    REM     X  IS THE MAP X-COORDINATE IN CENTIMETERS OR
2300    REM        INCHES.
2310    REM
2320    REM     Y  IS THE MAP Y-COORDINATE IN CENTIMETERS OR
2330    REM        INCHES.
2340    REM
2350    REM
2360 LET S = 0
2370    REM    IF THE POINT FROM THE DATA BASE IS NOT IN THE
2380    REM    HEMISPHERE BEING DRAWN, SET THE OFF-SCALE FLAG
2390    REM    AND RETURN.
2400 IF  H = 0  THEN 2470
2410 IF  P > 0.0  THEN 2480
2420    REM    FOR A SOUTHERN HEMISPHERE MAP, CHANGE THE SIGN
2430    REM    OF THE LONGITUDE TO MAINTAIN THE PROPER MAP
2440    REM    ORIENTATION.
2450 LET L = -L
2460 GO TO 2520
2470 IF  P >= 0.0  THEN 2520
2480 LET S = 1
2490 RETURN
2500    REM    COMPUTE THE MAP COORDINATES FROM THE
2510    REM    GEOGRAPHIC COORDINATES.
2520 LET R1 = R * COS(P)
2530 LET X = R1 * COS(L)
2540 LET Y = R1 * SIN(L)
2550 RETURN
2560 END
```

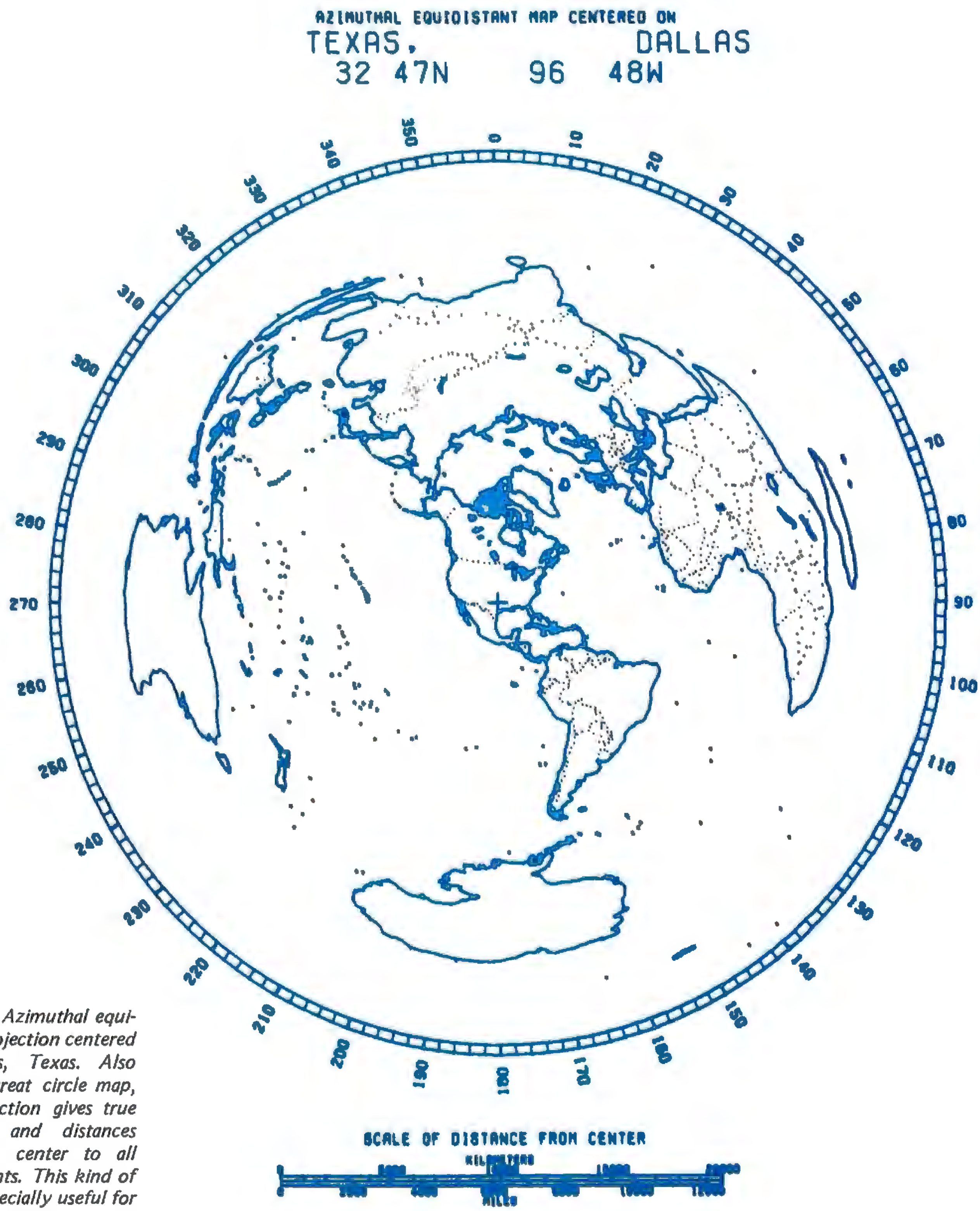

Figure 9: Azimuthal equidistant projection centered on Dallas, Texas. Also called a great circle map, this projection gives true azimuths and distances from the center to all other points. This kind of map is especially useful for showing great circle navigation routes and for determining the proper great circle bearings when aiming radio antennas.

referred to as a great circle map, is particularly useful in navigation and radio communication. Each such map is based on a chosen central location, and the land areas are mapped so that the azimuths to them from the center are true in all directions. This is accomplished by computing the great circle bearings and distances from the central location to each of the points in the data base, then scaling the distance to fit the map. This yields the polar form of the map coordinates which are then directly converted to rectangular map coordinates in the usual manner.

Since the shortest distance between any two points on the surface of the Earth is along the great circle path between them, ships and aircraft follow such paths as closely as possible. Radio signals are usually

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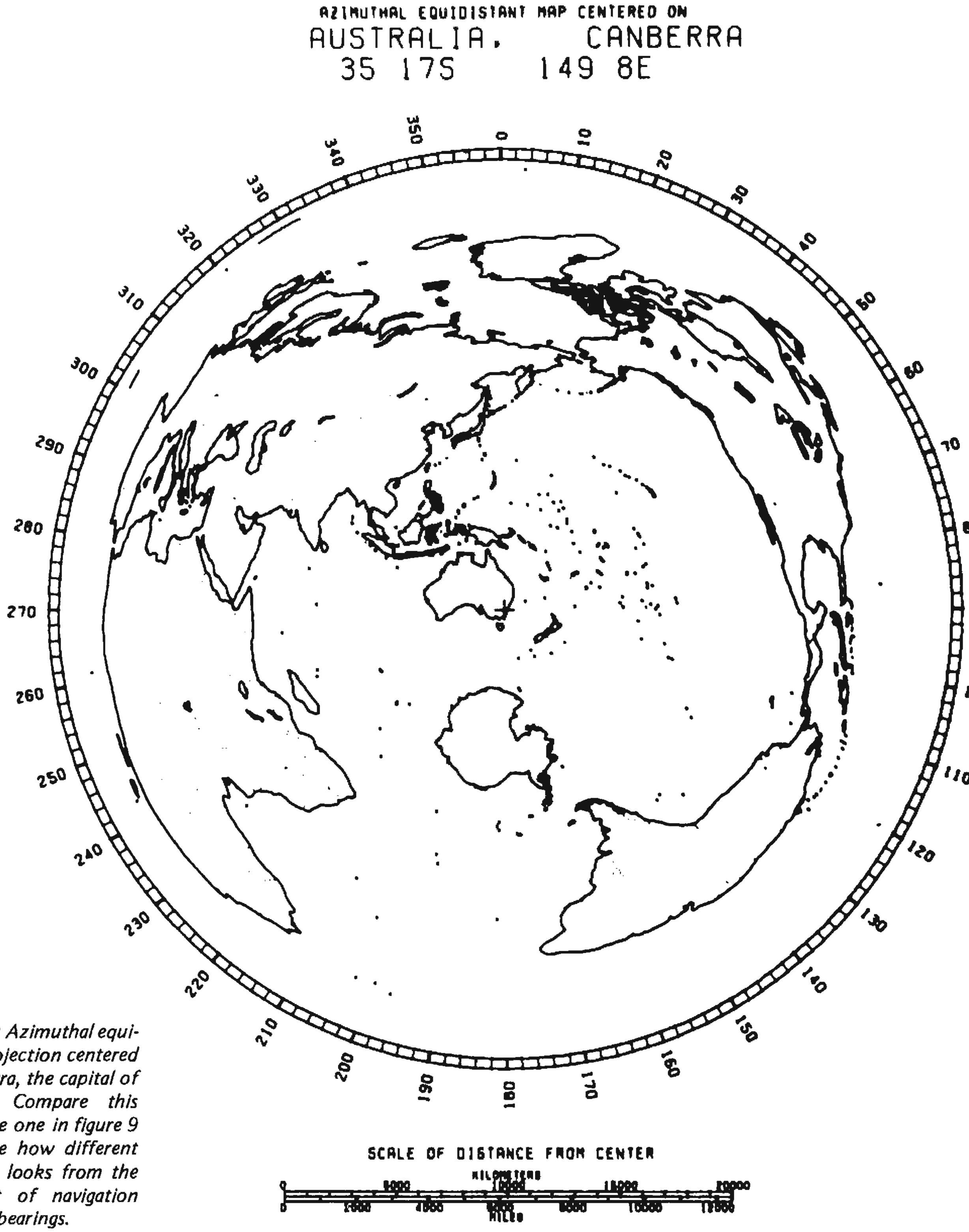

Figure 10: Azimuthal equidistant projection centered on Canberra, the capital of Australia. Compare this map to the one in figure 9 and notice how different the world looks from the standpoint of navigation and radio bearings.

strongest along the shortest path, so reception is best when the antenna is lined up with the correct great circle bearing. The azimuthal equidistant map is superb in these applications.

Figures 9 and 10 illustrate maps centered on Dallas TX, and Canberra, Australia, respectively. A navigator planning a flight from Dallas to Tokyo would draw a straight line from the center of the Dallas map, to Tokyo. This line indicates the shortest path between the two cities, and shows the intervening territory to be traversed. By extending the straight line on out to the bearing scale on the perimeter of the map, the initial departure bearing can be read directly.

Ham radio operators and shortwave listeners use these maps extensively. Suppose

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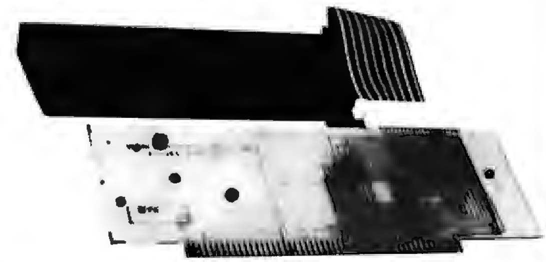

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Listing 5: Subroutine to compute map coordinates for azimuthal equidistant projection.

```
5000    REM    SUBROUTINE FOR COMPUTING MAP COORDINATES FOR
5010    REM    AZIMUTHAL EQUIDISTANT PROJECTION.
5020    REM
5030    REM
5040    REM    THE FOLLOWING FUNCTION MUST BE DEFINED BEFORE
5050    REM    THIS SUBROUTINE IS CALLED:
5060    REM
5070    REM    FNC( )  COMPUTES THE ARC COSINE OF THE
5080    REM            ARGUMENT.  THE FUNCTION MUST BE
5090    REM            NON-AMBIGUOUS; THAT IS, IT MUST
5100    REM            ATTACH THE CORRECT ALGEBRAIC SIGN
5110    REM            TO THE RESULT.
5120    REM
5130    REM
5140    REM    THE FOLLOWING VARIABLES MUST BE DEFINFD BEFORE
5150    REM    THIS SUBROUTINE IS CALLED:
5160    REM
5170    REM    A1 IS EQUAL TO SIN(A), WHERE A IS THE
5180    REM       GEOGRAPHIC LATITUDE OF THE LOCATION ON
5190    REM       WHICH THE MAP IS CENTERED.
5200    REM
5210    REM    A2 IS EQUAL TO COS(A), WHERE A IS AS DEFINED
5220    REM       ABOVE
5230    REM
5240    REM    L0 IS THE GEOGRAPHIC LONGITUDE OF THE LOCATION
5250    REM       ON WHICH THE MAP IS CENTERED.
5260    REM
5270    REM    P  IS THE GEOGRAPHIC LATITUDE (FROM THE DATA
5280    REM       BASE) OF THE POINT BEING PROCESSED.
5290    REM
5300    REM    L  IS THE GEOGRAPHIC LONGITUDE (FROM THE DATA
5310    REM       BASE) OF THE POINT BEING PROCESSED.
5320    REM
5330    REM    F  IS THE MAP SCALE FACTOR, EQUAL TO
5340    REM       R/3.1415927, WHERE R IS THE RADIUS OF THE
5350    REM       FINISHED MAP, IN CENTIMETERS OR INCHES.
5360    REM
5370    REM
5380    REM    THE FOLLOWING VARIABLES ARE COMPUTED BY THIS
5390    REM    SUBROUTINE:
5400    REM
5410    REM    L1 IS TEMPORARY STORAGE FOR THE DIFFERENCE
5420    REM       BETWEEN THE LONGITUDE OF THE POINT BEING
5430    REM       PROCESSED, AND THE LONGITUDE OF THE
5440    REM       LOCATION ON WHICH THE MAP IS CENTERED.
5450    REM
5460    REM    P1 IS TEMPORARY STORAGE FOR THE SINE OF THE
5470    REM       LATITUDE OF THE POINT BEING PROCESSED.
5480    REM
5490    REM    D  IS THE ANGULAR DISTANCE (ARC DISTANCE), IN
5500    REM       RADIANS, BETWEEN THE LOCATION ON WHICH THE
5510    REM       MAP IS CENTERED AND THE POINT BEING
5520    REM       PROCESSED.
5530    REM
5540    REM    D1 IS TEMPORARY STORAGE FOR THE COSINE OF D.
5550    REM
5560    REM    C  IS THE NORMALIZED ANGULAR COMPONENT OF THE
5570    REM       POLAR FROM OF THE MAP COORDINATES.
5580    REM
5590    REM    C1 IS THE COSINE OF THE VALUE OF C BEFORE C IS
5600    REM       NORMALIZED.
5610    REM
5620    REM    R1 IS THE RADIAL DISTANCE COMPONENT OF THE
5630    REM       POLAR FORM OF THE MAP COORDINATES.
5640    REM
5650    REM    X  IS THE MAP X-COORDINATE, IN CENTIMETERS OR
5660    REM       INCHES.
5670    REM
5680    REM    Y  IS THE MAP Y-COORDINATE, IN CENTIMETERS OR
5690    REM       INCHES.
5700    REM
5710    REM
5720 LET L1 = L - L0
5730    REM    NORMALIZE THE LONGITUDINAL DIFFERENCE BETWEEN
```

Listing 5 continued on page 100

that a ham in Canberra, the capital of Australia, hears a station in Venezuela that he would like to talk to. By using the map in figure 10, he can draw a line from the center, through Venezuela, out to the edge. The bearing read at the edge tells him where to set his antenna, and once done he not only receives the strongest possible signal from Venezuela, but he also assures that his own signal is transmitted along the shortest possible path to the other ham.

The distance scale at the bottom of these maps can be used to measure the distance between the center and any other location on the map. But it cannot be used between just any two locations: on this type of projection the distance scale is accurate only when measuring outward from the center.

The bearing scale, you will notice, is numbered from 0 to 360 degrees, clockwise from true north. This is the usual convention for all navigation and radio bearings. We label the map in this manner, but work with standard trigonometric convention in the program. More will be said about that later.

The program that generated the example maps is given in listing 5. Although slightly more involved than the previous map projections that we have looked at, it still requires only about a dozen statements to carry out the entire conversion process. One interesting feature is that there is no off-scale flag to worry about, because there is no such thing as an off-scale condition on an azimuthal equidistant map. The entire world is mapped, with no discontinuities, so every coordinate in the data base will find a home somewhere on the map.

The solution of the mathematics requires an inverse cosine function, which is not present in many BASIC interpreters. Rather than worry about what other implementations might be like, I just set it up to compute the inverse cosine by a user-defined function, FNC. It is up to the user to insert a properly defined function for this operation. *[Most BASIC interpreters have inverse tangent functions. Inverse cosine can be derived by* $cos^{-1}(X) = -tan^{-1}(X/\sqrt{1 - X^2}) + 1.5708$ *. . . .*RGAC*]*

Since many of the people who are interested in this type of map are also interested in printing out tables of great circle bearings and distances to other locations, I arranged the first part of the program to compute the angle in navigation/radio bearing convention before converting it to standard convention. The remarks beginning at line 5900 give additional details for extracting this information if you want it in tabular form.

One should be cautioned that the creation of azimuthal equidistant maps requires a fairly dense data base, because of

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Listing 5 continued from page 98:

```
5740   REM    -180 DEGREES AND +180 DEGREES (-PI AND +PI).
5750 IF  L1 >= -3.1415927  THEN 5780
5760 LET L1 = L1 + 6.2831853
5770 GO TO 5800
5780 IF  L1 <= 3.1415927  THEN 5800
5790 LET L1 = L1 - 6.2831853
5800 LET P1 = SIN(P)
5810 LET D1 = A1 * P1  +  A2 * COS(P) * COS(L1)
5820 LET D = FNC(D1)
5830 LET C1 = (P1 -A1*D1) / (A2 * SIN(D))
5840 LET C = FNC(C1)
5850   REM    NORMALIZE THE VALUE OF C, DEPENDING UPON THE
5860   REM    RELATIVE LONGITUDES OF THE POINT AT THE CENTER
5870   REM    OF THE MAP AND THE POINT BEING PROCESSED.
5880 IF  L1 >= 0.0  THEN 6020
5890 LET C = 6.2831853 - C
5900   REM    AT THIS POINT C IS IN THE RANGE FROM 0 TO
5910   REM    2*PI, MEASURED CLOCKWISE FROM TRUE NORTH.  IF
5920   REM    DESIRED, ONE CAN COMPUTE THE BEARING IN
5930   REM    DEGREES BY B = C * 57.2957795.  THE GREAT
5940   REM    CIRCLE DISTANCE ALONG THE SURFACE OF THE EARTH
5950   REM    CAN ALSO BE COMPUTED AT THIS POINT BY
5960   REM    K = D * 6378, WHERE K IS IN KILOMETERS, OR BY
5970   REM    M = D * 3963, WHERE M IS IN MILES.
5980   REM
5990   REM    NOW REVERSE THE DIRECTION OF MEASUREMENT OF C
6000   REM    AND ROTATE IT BY PI/2 (90 DEGREES).  THEN
6010   REM    NORMALIZE THE RESULT BETWEEN -PI AND +PI.
6020 LET C = 1.5707963 - C
6030 IF  C >= -3.1415927  THEN 6070
6040 LET C = C + 6.2831853
6050   REM    CONVERT THE ANGULAR DISTANCE TO THE MAP RADIAL
6060   REM    DISTANCE.
6070 LET R1 = D * F
6080   REM    R1 AND C NOW REPRESENT NORMALIZED POLAR
6090   REM    COORDINATES ON THE MAP, FROM WHICH THE
6100   REM    RECTANGULAR MAP COORDINATES ARE COMPUTED:
6110 LET X = R1 * COS(C)
6120 LET Y = R1 * SIN(C)
6130 RETURN
6140 END
```

the extreme elongation of graphical features near the edge of the map. The consequence of having widely separated data points will be an entirely unacceptable map with long straight and angular lines on the outer portions. This can be minimized somewhat by certain interpolation techniques, but none of these can entirely compensate for fundamental deficiencies in the data base.

Perhaps by this time some readers have realized that the polar equidistant maps that we looked at in figures 3 and 4 are actually just very special cases of the azimuthal equidistant map. Due only to their unique central locations, they happen to be more easily generated by the procedure in listing 2 than the one in listing 5, though either could do the job with just minor modification.

Celestial Maps

No examples of celestial maps have been included because the methods used to create them have already been covered in the discussion of the other types of maps. It is doubtful that you would want to generate a hard copy of a celestial map, since the projections used are pretty much standardized and there are plenty of nice printed maps available at nominal cost. The true value of computer generated celestial maps materializes in the creation of video displays for use adjacent to the telescope during astronomical observations.

One can set up a system to display selected areas of the heavens on a video display equipped with a red filter to preserve night vision. The area displayed can be specified at the keyboard, or it can be automatically designated according to the current pointing position of the telescope. The computer can be used to drive the telescope's tracking motors, and simultaneously update the video display as the field of vision moves across the night sky.

As mentioned earlier, ready-made data bases abound for astronomical applications. For all practical purposes, the format is the same as for geographical data bases. Celestial coordinates, however, are given in right ascension (measured in hours, minutes, and seconds) and declination (measured in degrees). Right ascension can also be represented in degrees of arc, where 15 degrees are equal to one hour of time. The format you use would depend upon the ultimate application.

In addition to the coordinates stored in the data base, it will be necessary to store a code indicating the type of object (star, nebula, galaxy, etc) as well as its visual magnitude (brightness). Then dots of varying size, or even distinctly different symbols, can be displayed to give a much more accurate representation of what the observer will see through the telescope. The process used for celestial mapping is very much like that demonstrated by the United States map in figure 2, in that the map is made up entirely of isolated dots or symbols with no lines connecting them.

Since the area of the sky presented on the video screen at any one time is comparatively small, most portions of the sky can be displayed with no noticeable distortion merely by using a simple rectangular projection. Areas within about 30 or 40 degrees of the celestial poles might be presented using a polar equidistant projection.

Homemade Projections

It has already been pointed out that the projections we examined are just the most common of the many projections actually in use. You may find that you have an application that requires a different approach, and you will probably find just what you want in any good text on cartography or map projections. But don't let that be the end of the line for you. There is nothing that says that you can't devise your own projections. If you want a projection that shows the surface of the Earth as viewed from an antimatter

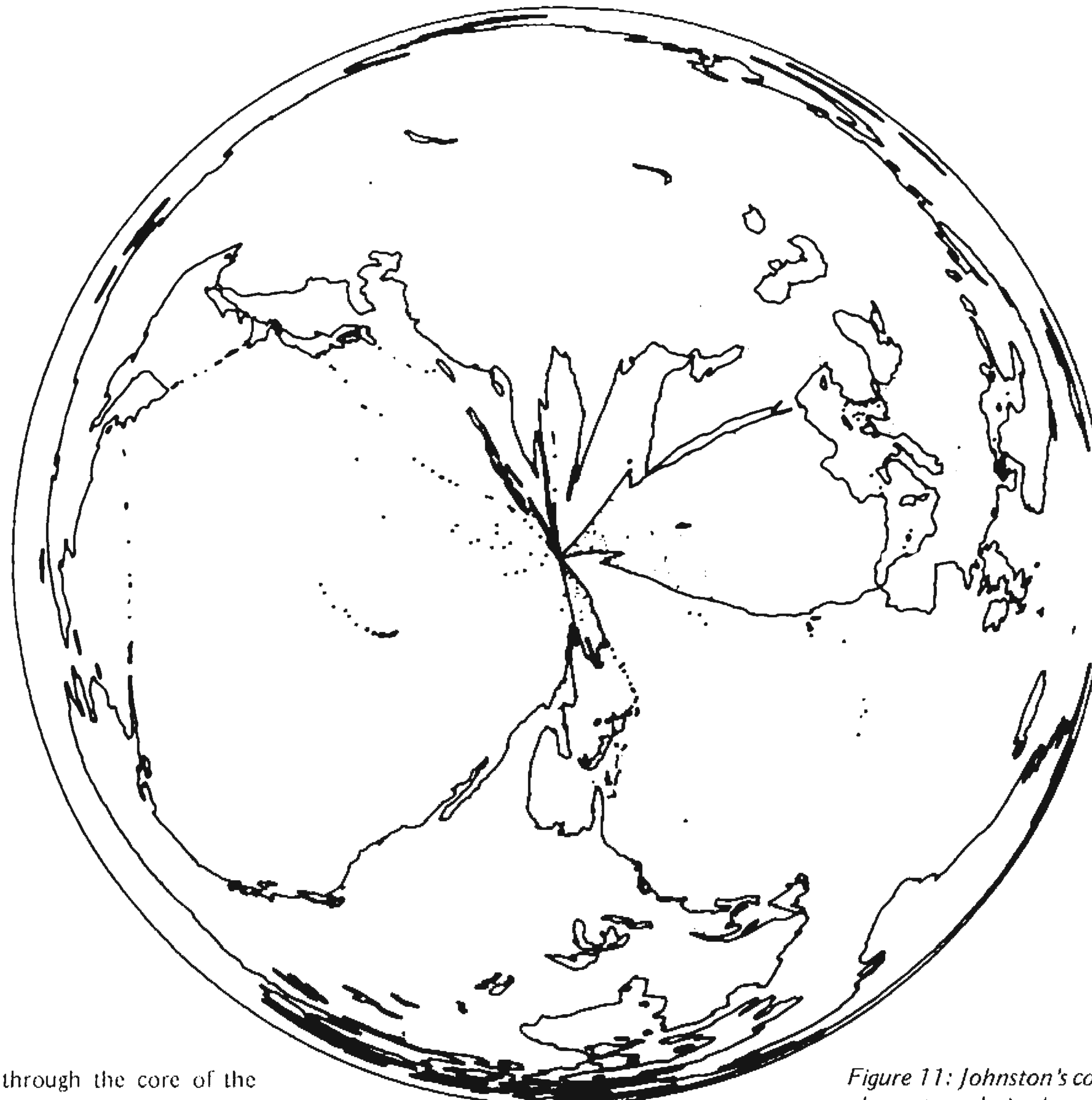

Figure 11: Johnston's complementary latitude polar projection of the northern hemisphere. This is a homemade projection invented by the author, for which the reader is invited to find a use.

spaceship traveling through the core of the Earth, it's a simple matter to set up one. When you're through, you can even name the projection after yourself.

To demonstrate the liberties one can take, I have included in figure 11 a projection of my own design. This I have called Johnston's Complementary Latitude Polar Projection of the Northern Hemisphere. The reader is left to find a use for it.

Summary

Some of the greatest theoretical contributions to the science of cartography were made as far back as 400 years ago. But producing each given map was a monumental task of manual computation, not to be taken lightly. What was possible in theory for hundreds of years has only become practical to carry out on any significant scale in the past 25 years, and for a time only by organizations with access to large scale computers.

Today, you and I can sit before our home computers, and with a few keystrokes we can command our machines to spew out maps of all descriptions. In mere seconds, we can have maps for satellite tracking, for antenna pointing, for Space War games, or for whatever purposes suit our fancy. The subroutines given in the accompanying listings can be used to generate a number of different types of very useful maps, and with little effort the reader can devise additional software to further expand the capability.

This article has barely scratched the surface of the field of computer generated maps. We have not, for example, addressed the subject of topographic mapping, or any of a host of other interesting aspects of computerized cartography. Commercial and government installations use techniques far more sophisticated than those demonstrated here. One can, however, derive an enormous amount of practical use and personal satisfaction from putting into operation the procedures that we have examined. If your imagination has no limits, then the power of your computer has no bounds.■

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```
                      NAM   DISASSEMBLER
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                      OPT   NOG
                      OPT   O
1800                  ORG   $1800
     A00C     XHI     EQU   $A00C
     A066     FLAG    EQU   $A066
     A067     CTR     EQU   $A067
     8004     KBD     EQU   $8004
     8008     PIAD    EQU   $8008
     E07E     PD1     EQU   $E07E
     E047     BADR    EQU   $E047
     A060     XTEM    EQU   $A060
     A062     PCTEM   EQU   $A062
     A064     YTEM    EQU   $A064
1800 20 16    START   BRA   SET
1802 00       PCR     FCB   0,$10,$16,0      Prompt test string -home, clear to end of
1806 00               FCB   0,'?,4           screen, "?"
1809 0D       CRLF    FCB   $D,$A,0,0,0,4    Carriage return & line feed string
180F 0D       PAGE    FCB   $D,$D,$D,'-      Page spacing string
1813 2D               FCB   '-,$D,$D,$D,4
1818 CE 8008  SET     LDX   #PIAD            Set up PIA for printer
181B 4F               CLR A
181C A7 01            STA A 1,X              Zero control reg
181E 43               COM A
181F A7 00            STA A 0,X              All data lines are outputs
1821 86 3F            LDA A #$3F
1823 A7 01            STA A 1,X              Idle pattern for ctl register
1825 CE 1802  PROM    LDX   #PCR             Prompt user
1828 BD E07E          JSR   PD1              Use Mikbug PDATA1 to do it
182B BD E047          JSR   BADR             Get hex starting adr. using Mikbug BADDR
182E FE A00C          LDX   XHI
1831 FF A062          STX   PCTEM            Put result in temp. pseudo pgm. counter
1834 86 3B    LCTR    LDA A #$3B             Init lines/page counter
1836 B7 A067          STA A CTR
1839 CE 1809  CONT    LDX   #CRLF            Print a CR/LF
183C BD 18DC          JSR   TTS
183F 7A A067          DEC   CTR              Bump line counter
1842 26 08            BNE   ADR              End of page?
1844 CE 180F          LDX   #PAGE            Yes
1847 BD 18DC          JSR   TTS              Page it and go reinit. counter
184A 20 E8            BRA   LCTR
184C CE A062  ADR     LDX   #PCTEM           Get adr of pseudo p.c in X reg
184F BD 18E7          JSR   TT4              Print pseudo p.c.
1952 FE A062          LDX   PCTEM            Get pseudo p.c. in X reg and print byte there
1855 BD 18E9          JSR   TT2              TT2 does an INX, so
1858 09               DEX                    put X back to pseudo p.c.
1859 BD 18EB          JSR   OUTS             Print a space
185C BD 1932          JSR   TABCK            Go look up byte (opcode) in table
185F 08               INX
1860 7F A066          CLR   FLAG             Check for immediate mode inst-if bit 4 of tag
1863 16               TAB                    is on, it is. (tag returns in A - tag code
                                             routine wants it in B with bit 4 off)
1864 C4 0F            AND B #$0F             Mask off bit 4 in B
186611                CBA                    and see if it was on.
1867 27 03            BEQ   FCODE            If not, leave flag=0
1869 7C A066          INC   FLAG             If so, set flag=1
186C 5D       FCODE   TST B                  Routine to interpret tag code
                                             Is tag=0?
186D 27 B6            BEQ   PROM             Yes, miss, illegal opcode, go get new start adr
```

Listing 1: Disassembler for the 6800 which resides in the upper 2 K byte portion of an 8 K byte memory which can operate on programs stored in the lower 6 K bytes.

Listing 1 continued on page 106

Processor	Disassembler
1. Fetch op code at address in program counter.	Fetch op code at address in pseudo-program counter.
2. Increment program counter.	Increment pseudoprogram counter.
3. Interpret op code.	Look up op code in table.
4. Fetch operand bytes, as necessary, incrementing program counter.	Fetch operand bytes, as necessary, incrementing pseudoprogram counter.
5. Execute instruction.	Print mnemonic operand.
6. Go to 1.	Go to 1.

Table 1: Comparison between the actual workings of the 6800 processor while operating on a program and the logical workings of the disassembler on the same text.

After spending two frustrating days trying to use MIKBUG to interface both a video display and a Teletype to the Southwest Technical Products SwTPC 6800 assembler (object code only), I wrote the disassembler in listing 1 to help me decipher the assembler. The disassembler and the program to be disassembled must be coresident in memory; the disassembler is located in the highest 2 K bytes of an 8 K byte memory, allowing it to operate on object programs up to 6 K bytes long. Temporary storage registers and the stack are located in the MIKBUG programmable memory area, hexadecimal addresses A000 thru A07F, and no page zero direct instructions are used.

The control port is a peripheral interface adapter (PIA) at hexadecimal 8004, configured for the SwTPC CT-1024/AC-30 television typewriter. MIKBUG input/output (IO) routines used are BADDR (E047) and PDATA 1 (E07E). The output port is a PIA at hexadecimal 8008, configured for the SwTPC PR-40 printer. The disassembler looks at object code in much the same way as the 6800 processor, but with one important difference: if the processor runs into an illegal op code, it runs amok; the disassembler just stops and requests a new starting address. Table 1 compares the physical operation of the processor with the logical operation of the disassembler.

Operation is easy: simply type a 4 digit hexadecimal starting address on the control port in response to the prompt "?". Disassembly and listing will begin at the specified address and continue until either an illegal op code is encountered or any key on the control port is pressed. For convenience, the disassembler also calculates and prints the effective address of all relative mode instructions.

Dirty tricks object code can make the disassembler stumble, but not fall, since it will request new input if it runs into obvious trouble. Things to watch out for are:

- Instructions which modify other instructions.

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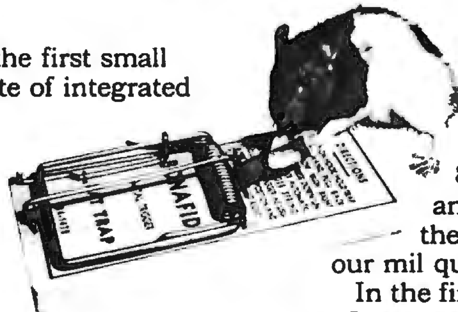

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Circle 171 on inquiry card.

Listing 1 continued from page 104:

```
186F 5A           DEC B          Is tag=1?
187Ø 27 4Ø        BEQ   RET      Yes, inherent instruction, go get next inst.
1872 5A           DEC B          Is tag=2?
1873 27 43        BEQ   REL      Yes, relative inst. Go process it.
1875 5A           DEC B          Is tag=3?
1876 27 3Ø        BEQ   B3       Yes, 3 byte inst. Go process it.
1878 5A           DEC B          Is tag=4?
1879 27 27        BEQ   PRTDS    Yes, 2 byte direct inst. Go process it.
187B 5A           DEC B          Is tag=5?
187C 27 1E        BEQ   PRTXS    Yes, 2 byte indexed inst. Print "X", space
187E C1 Ø6        CMP B =6       Is tag = B?
188Ø 2C 12        BGE   PRTBS    Yes, acc. B inst. Go print a "B"
1882 86 41        LDA A =A       No, acc. A inst. Print an "A", space
1884 8D 52        BSR   PCS
1886 5A     TST5  DEC B          Is tag=6 = B?
1887 27 13        BEQ   PRTXS    Yes, accumulator indexed inst. Print "X", space
1889 5A           DEC B          Is tag=7 or =C?
188A 27 16        BEQ   PRTDS    Yes, accumulator direct inst. Print "D", space
188C 5A           DEC B          Is tag=8 or=D?
188D 27 23        BEQ   RET      Yes, inherent accumulator inst. Go return
188F 5A           DEC B          Is tag=9 or=E?
189Ø 27 1C        BEQ   B2       Yes, 2 byte accumulator inst. Print operand
1892 2Ø 14        BRA   B3       Tag=A or F, 3 byte accumulator inst. Print operand
1894 86 42  PRTBS LDA A ='B      Print a "B" and a space
1896 8D 4Ø        BSR   PCS
1898 CØ Ø5        SUB B =S5      Set tag=tag-5
189A 2Ø EA        BRA   TST5     and go back into FCODE to finish up.
189C 86 58  PRTXS LDA A ='X      Print an "X" and a space
189E 8D 38        BSR   PCS
18AØ 2Ø ØC        BRA   B2       and print the operand byte
18A2 86 44  PRTDS LDA A ='D      Print a "D" and a space
18A4 8D 32        BSR   PCS
18A6 2Ø Ø6        BRA   B2       and print the operand byte
18A8 8D 7E  B3    BSR   FCK      Check to see if immediate mode, (prints - if so)
18AA 8D 3B        BSR   TT4      and print two byte operand
18AC 2Ø Ø4        BRA   RET      then return
18AE 8D 78  B2    BSR   FCK      Check to see if immed mode then
18BØ 8D 37        BSR   TT2      print one byte operand
18B2 FF AØ62 RET  STX   PCTEM    Save new pseudo p.c.
18B5 7E 1839      JMP   CONT     and loop back for next instruction to eat
18B8 8D 2F  REL   BSR   TT2      Relative mode, so print operand
18BA FF AØ62      STX   PCTEM    Save the new pseudo p.c. (inc. by TT2)
18BD Ø9           DEX            Put X reg. back to operand
18BE E6 ØØ        LDA B Ø,X      Get operand byte in B
18CØ Ø8           INX            X reg back to pseudo p.c. adr.
                                 Is the offset negative?
18C1 2B Ø6        BMI   SUB      Yes, go subtract it from pseudo p.c.
18C3 2B Ø8  ADD   INX            No, add one to pseudo p.c.
18C4 5A           DEC B          Added enough times?
18C5 26 FC        BNE   ADD      No, go increment again
18C7 2Ø Ø4        BRA   TADR     Yes, go print the effective adr.
18C9 Ø9     SUB   DEX            Offset is negative, so subtract one from
                                 pseudo p.c.
18CA 5C           INC B          Subtracted enough?
18CB 26 FC        BNE   SUB      No, go do it again
18CD FF AØ64 TADR STX   YTEM     Now print the effective adr.
18DØ CE AØ64      LDX   #YTEM
18D3 8D 12        BSR   TT4      4 hex chrs, 2 bytes
18D5 7E 1839      JMP   CONT     and go get the next instruction
18D8 8D 2C  PCS   BSR   TTY      Prints the ascii chr. in A and a space
18DA 2Ø ØF        BRA   OUTS
18DC A6 ØØ  TTS   LDA A Ø,X      Prints the character string pointed to
18DE 81 Ø4        CMP A #$4      by the X reg, until it finds EOT, then
18EØ 27 45        BEQ   T2       returns
18E2 8D 22        BSR   TTY
18E4 Ø8           INX            next chr in string, please
18E5 2Ø F5        BRA   TTS      and loop 'till EOT
18E7 8D Ø6  TT4   BSR   OUT2     Prints 4 hex characters pointed to by X reg
18E9 8D Ø4  TT2   BSR   OUT2     Prints 2 hex characters pointed to by X reg
18EB 86 2Ø  OUTS  LDA A #$2Ø     Prints a space
18ED 2Ø 17        BRA   TTY
18EF A6 ØØ  OUT2  LDA A Ø,X      Get byte into A
18F1 8D Ø5        BSR   OUTL     Print left half of byte
18F3 A6 ØØ        LDA A 0,X      Get right half and
18F5 Ø8           INX            point to next byte
18F6 2Ø Ø4        BRA   OUTR     Print right half
18F8 44     OUTL  LSR A          Make left half byte into
18F9 44           LSR A          right half byte
18FA 44           LSR A
18FB 44           LSR A
18FC 34 ØF  OUTR  AND A =$F      Convert hex ½ byte into ascii
18FE 8B 3Ø        ADD A =$3Ø     by adding 30
19ØØ 81 39        CMP A =$39     and testing to see if it's a hex letter
19Ø2 23 Ø2        BLS   TTY      No, go print the number
19Ø4 8B Ø7        ADD A =$7      Yes, change to ascii letter code
19Ø6 FF AØ6Ø TTY  STX   XTEM     and print it, or just plain print whatever's
19Ø9 CE 8ØØ8      LDX   =PIAD    in A, if you got here from somewhere other
19ØC A7 ØØ        STA A Ø,X      than OUTR. Stuff the chr. in A into the
19ØE 86 37        LDA A =$37     printer data reg. and pulse the CA2 line
191Ø A7 Ø1        STA A 1,X      low for a few μsec,
1912 86 3F        LDA A #$3F     then return CA2 to high
1914 A7 Ø1        STA A 1,X      to start the printer
1916 7D 8ØØ4 T1   TST   KBD      Look to see if user has hit a key
1919 2B Ø3        BMI   T3       Yes he did, so quit whatever is going on
```

Listing 1 continued on page 108

- Text strings, constant bytes or temporary storage locations embedded in blocks of executable code.
- Lookup tables, such as the one used in the disassembler.
- Instructions buried within other instructions, such as the CPX skip trick:

Entering at 0100 we see

```
0100    8C 86 20      LDX #$8620
0103    ...next...    (A is unchanged)
```

But entering at 0101 we see

```
0100    8C
0101    86 20         LDA A #$20
0103    ...next...    (A has $20 value)
```

(If one enters this routine at hexadecimal 0100, accumulator A is unchanged when NEXT is executed; entering at 0101 passes hexadecimal 20 to NEXT in accumulator A.)

No dirty tricks were incorporated in the disassembler program, so it happily disassembles itself starting at hexadecimal 1818, stopping when it reaches the top of the lookup table (see listing 2). Machines should work; people should think. It does take a considerable amount of thinking to find your way through somebody else's uncommented code, even using this program, but at least the clerical work can now be done by the machine.■

```
1818 CE  LDX #8008          1860 7F  CLR A066
181B 4F  CLR A              1863 16  TAB
181C A7  STA A X 01         1864 C4  AND B #0F
181E 43  COM A              1866 11  CBA
181F A7  STA A X 00         1867 27  BEQ 03 186C
1821 86  LDA A #3F          1869 7C  INC A066
1823 A7  STA A X 01         186C 5D  TST B
1825 CE  LDX #1902          186D 27  BEQ B6 1825
1828 BD  JSR E07E           186F 5A  DEC B
182B BD  JSR E047           1870 27  BEQ 40 18B2
182E FE  LDX A00C           1872 5A  DEC B
1831 FF  STX A062           1873 27  BEQ 43 18B8
1834 86  LDA A #1B          1875 5A  DEC B
1836 B7  STA A A067         1876 27  BEQ 30 18A8
1839 CE  LDX #1809          1878 5A  DEC B
183C BD  JSR 18DC           1879 27  BEQ 27 18A2
183F 7A  DEC A067           187B 5A  DEC B
1842 26  BNE 08 184C        187C 27  BEQ 1E 189C
1844 CE  LDX #180F          187E C1  CMP B #06
1847 BD  JSR 18DC           1880 2C  BGE 12 1894
184A 20  BRA E8 1834        1882 86  LDA A #41
184C CE  LDX #A062          1884 8D  BSR 52 18D8
184F BD  JSR 18E7           1886 5A  DEC B
1852 FE  LDX A062           1887 27  BEQ 13 189C
1855 BD  JSR 18E9           1889 5A  DEC B
1858 09  DEX                188A 27  BEQ 16 18A2
1859 BD  JSR 18EB           188C 5A  DEC B
185C BD  JSR 1932           188D 27  BEQ 23 18B2
185F 08  INX                188F 5A  DEC B
```

Listing 2: Sample output of the disassembler. This is a portion of the disassembler disassembled by itself.

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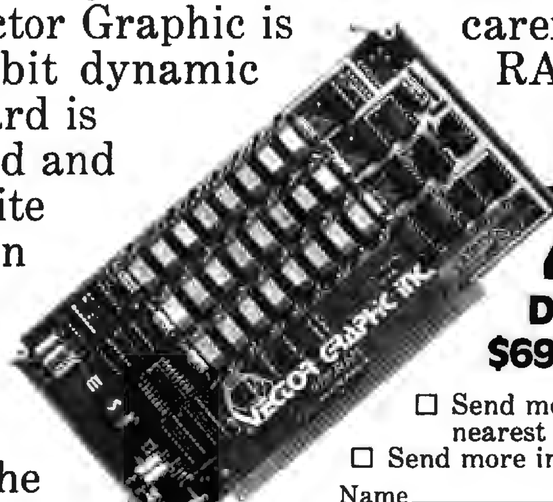

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Circle 383 on inquiry card.

Listing 1 continued from page 106:

```
191B 7E 1825         JMP   PROM      and ask for a new starting adress
191E 6D Ø1    T3     TST   1,X       No, he didn't, so look to see if the
192Ø 2A F4           BPL   T1        printer has finished, if not, wait in loop
1922 A6 ØØ           LDA A Ø,X       Printer done, so clear PIA flag
1924 FE AØ6Ø         LDX   XTEM      restore the index reg
1927 39       T2     RTS             and go back where ya came from
1928 7D AØ66  FCK    TST   FLAG      Look at the flag to see if an immediate inst,
192B 27 Ø4           BEQ   NIM       if not, do nothing but return
192D 86 23           LDA A #'#       If so,print a "#"
192F 8D D5           BSR   TTY
1931 39       NIM    RTS             and then return
1932 A6 ØØ    TABCK  LDA A Ø,X       Get possible opcode in A
1934 FF AØ62         STX   PCTEM     Save the pseudo p.c
1937 CE 195D         LDX   #TABL     Table starting adr in X reg
193A A1 ØØ    CK1    CMP A Ø,X       Compare opcode to table entry  Same?
193C 27 ØC           BEQ   HIT       Yes, found opcode, go print mnemonic
193E Ø8              INX             No, increment X to next location in
193F Ø8              INX             table
194Ø Ø8              INX
1941 Ø8              INX
1942 Ø8              INX
1943 8C 1D36         CPX   #TABEN    Look to see if the end of the table has
1946 26 F2           BNE   CK1       been reached, if not, go look again
1948 8D BC    MISS   BSR   TTY       Print the invalid opcode as ascii
194A Ø8       HIT    INX             Print mnemonic string until finding
194B A6 ØØ           LDA A Ø,X       tag byte, less than $1F
194D 81 1F           CMP A #$1F
194F 23 Ø4           BLS   DONE      Found tag code, go return
1951 8D B3           BSR   TTY       Not tag byte, so print it
1953 2Ø F5           BRA   HIT       and go get next byte in string
1955 8D 94    DONE   BSR   OUTS      Print a space
1957 A6 ØØ           LDA A Ø,X       Get the tag byte in A
1959 FE AØ62         LDX   PCTEM     Restore the pseudo p.c. to X reg
195C 39              RTS             and return tag to tag routine in acc  A
195D Ø1       TABL   FCB   $Ø1       Long, boring table starts here.
195E 4E              FCC   /NOP/     First byte is opcode, then three
1916 Ø1Ø6            FDB   $Ø1Ø6     ascii bytes containing the mnemonic,
1963 54              FCC   /TAP/     then the tag code.
1966 Ø1Ø7            FDB   $Ø1Ø7
1968 54              FCC   /TPA/
196B Ø1ØB            FDB   $Ø1Ø8
196D 49              FCC   /INX/
197Ø Ø1Ø9            FDB   $Ø1Ø9
```

Random Comments

SET	Set up PIA for lineprinter.		
PROM	Prompt user: Home up, clear end of file "?".		
LCTR	Line counter for pager.		
CONT	Continue loop reentry.		
ADR	Print address.		
FCODE	Interpret tag byte from table:		
	TST 5	Test tag codes greater than 5 loop reentry,	
	PRTBS	Print B, space;	
	PRTXS	Print X, space;	
	PRTDS	Print D, space;	
	B3	Print two bytes pointed to by X;	
	B2	Print one byte pointed to by X;	
	RET	Return – save new address, loop to continue.	
REL	Relative instruction:		
	ADD	Adder for REL;	Compute absolute target
	SUB	Subtractor for REL;	address.
	TADR	Printer for REL.	and print it.
PCS	Print ASCII character in a, space.		
TTS	Print ASCII character string pointed to by X register.		
TT4	Print 4 hexadecimal characters pointed to by X register:		
	TT2	Print similar to MIKBUG OUT4HS;	
	OUTS	Print a space;	
	OUT2	Print byte;	
	OUTL	Print left half of byte;	
	OUTR	Print right half of byte.	
TTY	Line printer print routine:		
	T1	Tests keyboard for any key pressed,	
	T3	Line printer done yet?;	
	T2	Yes.	
FCK	Flag check – looks to see if immediate mode instruction, if so print "#" if no, go:		
	NIM	FCK done.	
TABCK	Table check for op code in question:		
	CK1	Check it;	
	MISS	Not in table; print it as ASCII and give up;	
	HIT	In table, print mnemonic.	
TABL	Op code lookup table starts here.		

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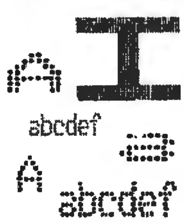

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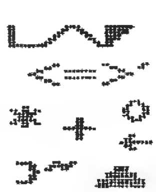

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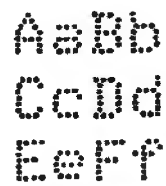

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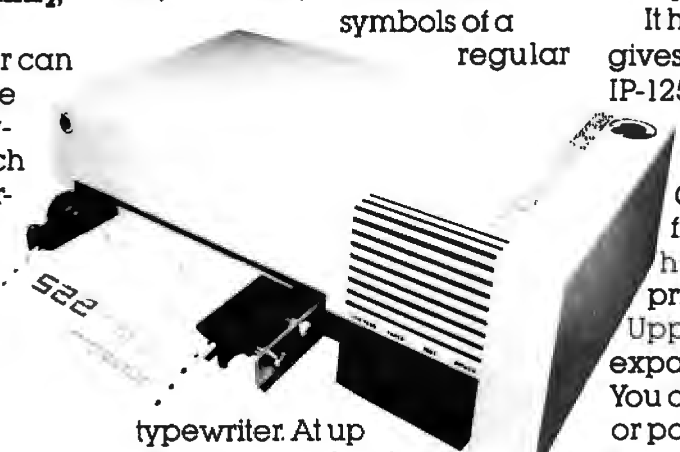

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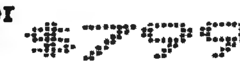

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Circle 177 on inquiry card.

Spacewar in Tiny BASIC

Navigating Through Integer BASIC

David J Beard
Sortiarii
RD 1 Box 648
Newmanston PA 17073

So you want to fly your own spaceship, but you're not up to doing six months worth of assembly language programming and the only high level language you've got is a *tiny* version limited to 4 function integer arithmetic? That rules out any kind of realistic navigation – or so it seems. All digital machines are limited to integer mathematics. Nearly any operation possible in machine code can be duplicated in a high level language, provided you have enough memory and the time to wait for the results. Armed with a little bit of knowledge, though, you can keep the convenience of your interpreter and have three-dimensional trigonometry, too. Here's how I did it.

My first objective in writing a spacewar game was to provide a realistic trainer for spaceflight rather than a flashy video display or a complex set of board game type rules. I feel strongly that a spacewar game ought to be three-dimensional. The third dimension is far more than a frill: it's the major difference between spaceflight and surface operations. I developed the scenario for my game in 1972 when I was working with a homebrew analog computer. In my version a single ship maneuvers in Cartesian space and is attacked by a series of homing torpedos that must be either destroyed or evaded. The game requires both aimed laser fire and navigation precise enough to permit evasion by narrow margins.

This article describes the trigonometry routines developed for the game. It assumes that you are familiar with high school physics and right angle trigonometry. These routines represent a compromise between precision and speed; they are neither quick nor simple, but then, neither is astrogation.

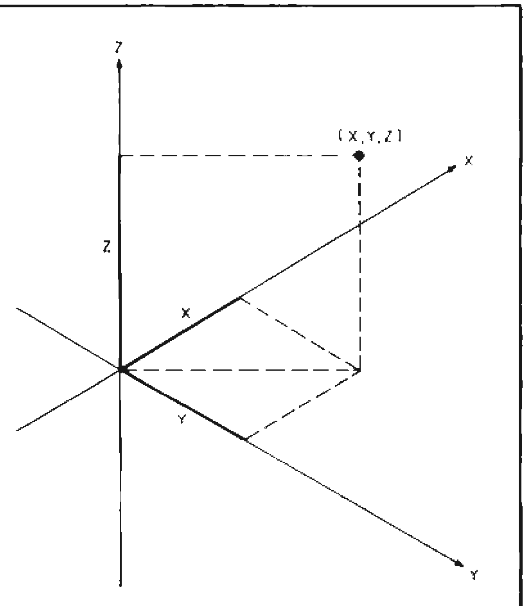

Figure 1: Cartesian coordinates for three-dimensional representation of position, velocity and acceleration.

Moving the Ship

The playing area for my game is a sphere of Cartesian space with a radius of 10,000 units. This provides about 4.2×10^{12} distinguishable positions, or the same number of vectors, each defined by a set of three integers X, Y, and Z as in figure 1. The ship's position, acceleration and velocity vectors can be represented by nine integers.

A convenient feature of this Cartesian representation is that motion along each axis can be calculated independently of the other axes. Also, I made the simplifying assumption that each turn in the game is one unit of time. This simplifies Newton's laws of motion considerably. The familiar:

$$\text{position}=S=S_0+VT+AT^2/2$$
$$\text{velocity}=V=V_0+AT$$

can be written as:

$$S=S+V+A/2$$
$$V=V+A$$

for each axis. Finding relative position and

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• **FIRMWARE:** On board firmware so that no software need be written or entered into your CPU system. The firmware can be shut off when not in use. Firmware residents at F0000. The firmware in and out of system is controlled from a switch on front panel.

• **3-ADDRESSABLE ROM LOCATIONS:** The EPROM Programmer has three sockets on front panel which are addressable to any location by dip switch. In addition each ROM location can be shut off or turned on by switches located on the front panel.

• **MONITOR:** A monitor is supplied within the firmware for performing several functions. Move memory, debug, verify, program from memory, program from TTY input, etc.

• **EASY CONNECTION:** The EPROM Programmer is attached with ease. For the TRS-80* users, the unit plugs into the rear of the keyboard or between the keyboard and expansion interface,. Included with the unit are two additional 40 pin edge connections for interfacing of other interfaces. For the S-100 users, a molded connection cable is supplied and it is inserted into one of the connectors on your mother board. Plug it in and it is ready to use.

• **FULLY BUFFERED:** add address and data lines are fully buffered.

• **OTHER FEATURES:** Other features include status lights for which ROM selected, switch enable for programming, pulse (burn) indicator firmware select-deselect switch, on, off and dip switches for the addressing of each ROM location.

*TRS-80 is a trademark of Tandy Corp

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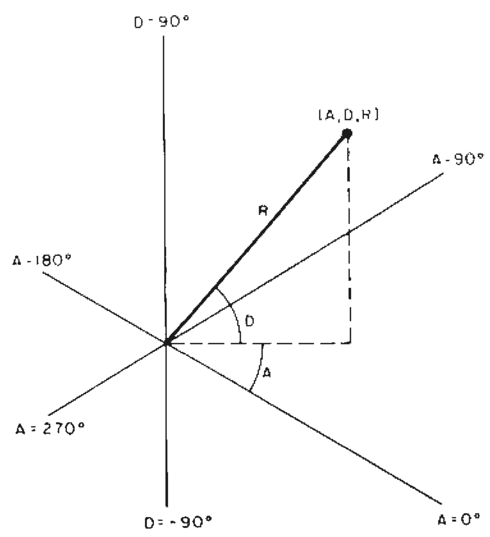

Figure 2: Spherical representation in three dimensions. Instead of the X, Y and Z axes as in Cartesian coordinates, spherical coordinates use azimuth, declination and radius.

velocity is also much simpler. Vector addition is just that addition:

$$S_{rel}=S_1-S_2$$
$$V_{rel}=V_1-V_2$$

for each axis.

Spherical Coordinates

Cartesian coordinates make it simple to model the laws of motion. A spaceship might possibly use a Cartesian system for navigation, but what about those homing torpedos? Any conceivable shipboard ranging and detection system tracking a foreign body should read out an angle and a range, not a set of grid points. Besides, entering your throttle settings in three axes is unnatural enough to deter any but the most hardened of spacewar addicts. The simplest solution is to keep track of all moving bodies in Cartesian coordinates and convert those coordinates to spherical form for display. Figure 2 shows a system of spherical coordinates. Each point or vector is defined by an azimuth ranging from 0 to 359 degrees (A), a declination ranging from −90 to 90 degrees (D), and a radius given in unit lengths (R). Instead of X,Y,Z we have A,D,R.

The ship's position and velocity are converted to spherical form for display. The thrust vector is input in spherical form and converted to Cartesian for computation. The direction of laser fire is kept in spherical form and compared to the spherical coordinates of the target at the next turn.

Next, we need routines to convert vectors in the form X,Y,Z to the form A,D,R and back again. The only trigonometric functions needed for those two conversions are the sine and the arctangent.

Listing 1 shows the S=sin (S) routine. S is an angle ranging from 0 to 90 degrees. The routine returns the sine of S in variable S in parts per thousand (1000 times the sin (S)). This routine makes use of the series:

$$\sin(S)=S-S^3/3!+S^5/5!-S^7/7!+\ldots$$

where S is in radians. Line 20 converts S from degrees to radians times 1000. Line 40 is the sine series in a form suitable for 16 bit integer mathematics. Beyond 45 degrees this series gave poor results. For values over 45 degrees line 10 transfers control to line 60. Lines 60 to 110 take the cosine of 90−S using the series:

$$\cos(S)=1-S^2/2!+S^4/4!-S^6/6!+\ldots$$

It's a good idea to test this routine by generating all 91 values and checking them against a table or calculator. The results should be within 2 or 3 parts per thousand.

```
10 IF S>45 GOTO 60
20 LET S=174*S/10
30 LET T=S/10
40 LET S=S-T*T/1000*T/6+T*T/1000*T/100*T/100*T/120
50 RETURN
60 LET S=90-S
70 LET S=174*S/10
80 LET T=S/10
90 LET S=1000-T*T/20+T*T/1000*T/100*T/24
100 LET S=S-T*T/1000*T/100*T/100*T/100*T/720
110 RETURN
```

Listing 1: BASIC routine for calculating the sine function. The sine is calculated in parts per thousand and the value of the sine is returned to the calling routine in variable S.

Listing 2 is a similar routine to calculate the arctangent of a ratio U expressed in parts per thousand (U times 1000). The series used here is:

$$\arctan(U)=U\ \ U^3/3+U^5/5-U^7/7+\ldots$$

It is not valid for U ⩾ 1. Line 10 is an adjustment to improve accuracy for values approaching 1. Notice that here the result S is in radians and must be converted to degrees immediately before exiting (line 50). Again, it's a good idea to test this routine for values of U between 0 and 999 before using it.

```
10 IF U>960 LET U=U+4
20 LET T=U/10
30 LET S=U-T*T/1000*T/3+T*T/1000*T/100*T/100*T/5
40 LET S=S-T*T/1000*T/100*T/100*T/100*T/100*T/7
50 LET S=S*10/174
60 RETURN
```

Listing 2: Routine for calculating the arctangent of U in parts per thousand. The result is returned to the calling routine in variable S.

A DEVELOPMENT TOOL FOR INTERACTIVE SOFTWARE

CIS COBOL is more than an efficient COBOL Compiler, it is a complete software development tool for business and office automation systems. It enables the programmer to write applications in a powerful subset of ANSI 74 standard COBOL and to take advantage of CIS COBOL language extensions such as interactive screen handling which are designed to fully exploit the special features of the microcomputer environment. Version 3 of CIS COBOL has many language additions but the compiler still requires only 20K bytes of memory and runs on 8080 and Z80 based microcomputers with 32K to 64K under the popular CP/M* operating system.

CIS COBOL is designed to support interactive applications. Areas of a CRT screen are mapped onto record descriptions in your CIS COBOL program and data is transferred using the ACCEPT and DISPLAY verbs providing full cursor manipulation and data entry facilities to the CRT operator. CIS COBOL language extensions enable the screen position at which the transfer is to start to be specified, protected fields to be defined and the CURSOR position to be detected and set by the program.

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CIS COBOL is supported by intelligent utility programs. When you take delivery of CIS COBOL Version 3 on 8 inch or 5 inch diskette you will receive in addition to the compiler and run time system the CONFIG program which enables you to configure CIS COBOL run time systems to drive many different types of "dumb" CRT terminal such as Lear Siegler ADM3A and Hazeltine 1500, plus the time saving FORMS program which allows you to create and edit screen images of business forms and then automatically generate the corresponding COBOL record descriptions to COPY into your CIS COBOL program.

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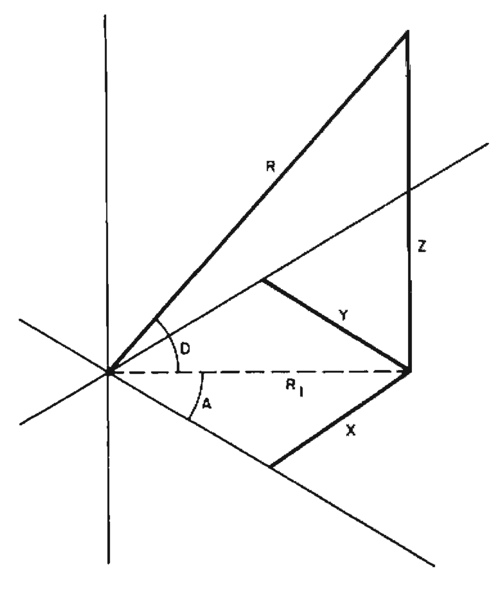

Figure 3: Measurements used for conversion between spherical and Cartesian coordinates. See text for full explanation.

Exact values of the tangent for angles in 1 degree increments should return the proper angle, but a tangent falling between these values does not necessarily return the closest angle.

Large Values

In order to prevent overflow and preserve even two digits of precision, it is necessary to make a special case of each decade. Listing 3, the S=arctan (T/U) routine, should serve as a worst case example of this process. This routine calculates the 3 digit ratio U and calls the arctangent routine shown in listing 2. The variable V is a flag set for angles over 45 degrees (line 30) and cleared otherwise (line 10). S is a temporary storage location used to swap T and U in these cases (lines 20, 40, 50, 60). Lines 70 to 100 represent the first decade. Note the trap at line 85 to prevent division by zero. The other decades are similar. Line 300 traps for values of U over 999, and line 320 tests the flag V and complements the angle S if T and U had been reversed.

```
10 LET V=0
20 IF U>=T GOTO 70
30 LET V=1
40 LET S=T
50 LET T=U
60 LET U=S
70 IF T>32 GOTO 110
80 LET T=T*1000
85 IF U=0 LET U=1
90 LET U=T/U
100 GOTO 300
110 IF U>327 GOTO 160
120 LET T=T*100
130 LET U=U/10
135 IF U=0 LET U=1
140 LET U=T/U
150 GOTO 300
160 IF T>3276 GOTO 210
170 LET T=T*10
180 LET U=U/100
185 IF U=0 LET U=1
190 LET U=T/U
200 GOTO 300
210 LET U=U/100
215 IF U=0 LET U=1
220 LET U=T/U*10
300 IF U>999 LET U=999
310 GOSUB (S=ARCTAN U)
320 IF V=1 LET S=90-S
330 RETURN
```

Listing 3: To guarantee that overflows do not occur during calculation, this routine makes sure that the range of numbers is broken down by decades. This also improves the accuracy of the approximation.

You will also need similar, but simpler, routines that return U=Usin(S) and U=U/sin(S). All of these routines can be shortened considerably if they do not need to accept the full range of 16 bit integers (as, for example, in a battleship type game on a 100 by 100 grid). The general process of writing these routines is similar to the manipulation of decimal places and the use of rough precalculations necessary if one were using a slide rule. It may be helpful to run through each decade of the routine on paper before beginning to program.

One More Detail

So far, all our routines work with first quadrant angles (positive declination and azimuth from 0 to 90 degrees). It is necessary to express each vector as its first quadrant equivalent before conversion, and restore the converted vector to its proper quadrant afterwards. Listing 4 is the Cartesian to spherical routine. In lines 10 to 120 the values X, Y, and Z are made positive and their original signs stored in the flags F, L, and G, respectively. The vector is now in the first quadrant and conversion can proceed. Refer to figure 3 during this discussion. Lines 130 to 160 calculate the azimuth, angle A. Lines 170 to 190 find the projected radius (R_1 in figure 3) and store it temporarily in variable R. Lines 200 to 220 find the declination, angle D. Lines 230 to 260 find the true radius. Note that line 230 complements S; the projected radius divided by the true radius, R_1/R, is the cosine of D or the sine of 90–D.

The vector A,D,R is now complete but must be restored to the proper quadrant. In line 270 the declination is simply given the same sign as Z. Line 280 exits if the azimuth is unchanged. Lines 290 to 310 apply the proper correction for azimuths between 270 and 360 degrees. Lines 320 to 340 deal with angles between 90 and 180 degrees, and line 350 corrects for the only remaining case.

The conversion from spherical to Cartesian requires a similar process of reduction to first quadrant and restoration, and uses the same three flags. Listing 5 shows only the actual spherical to Cartesian conversion. Lines 10 to 40 find Z. Lines 50 to 80 find the projected radius R_1 and store it temporarily in Y, again using the cosine or sine of the complement. Lines 90 to 110 find X, and lines 120 to 150 find Y.

Application

My version of this trigonometric package ran to 170 lines and almost 4 K bytes of program storage in a version of tiny BASIC that permits subscripted variables and FOR-NEXT loops. Even if your BASIC does not permit subscripted variables, it's a good idea to keep the temporary vectors A,D,R and X,Y,Z for the two conversion routines. If these are not written as subroutines, program length will get out of hand quickly. The flags F, L, and G can be replaced by a single variable holding the quadrant number. In a game involving two ships, one can be kept at the origin (X,Y,Z = 0,0,0), and only

```
10 LET F=0
20 LET L=0
30 LET G=0
40 IF X>-1 GOTO 70
50 LET X=-X
60 LET F=1
70 IF Y>-1 GOTO 100
80 LET Y=-Y
90 LET L=1
100 IF Z>-1 GOTO 130
110 LET Z=-Z
120 LET G=1
130 LET T=X
140 LET U=Y
150 GOSUB (S=ARCTAN T/U)
160 LET A=S
170 LET U=X
180 GOSUB (U=U/SIN S)
190 LET R=U
200 LET T=Z
210 GOSUB (S=ARCTAN T/U)
220 LET D=S
230 LET S=90-S
240 LET U=R
250 GOSUB (U=U/SIN S)
260 LET R=U
270 IF G=1 LET D=-D
280 IF F=0 IF L=0 RETURN
290 IF L=1 GOTO 320
300 IF F=1 LET A=360-A
310 RETURN
320 IF F=1 GOTO 350
330 LET A=180-A
340 RETURN
350 LET A=180+A
360 RETURN
```

Listing 4: BASIC program for converting from Cartesian to spherical coordinates.

```
10 LET S=D
20 LET U=R
30 GOSUB (U=U*SIN S)
40 LET Z=U
50 LET U=R
60 LET S=90-D
70 GOSUB (U=U*SIN S)
80 LET Y=U
90 LET S=A
100 GOSUB (U=U*SIN S)
110 LET X=U
120 LET U=Y
130 LET S=90-A
140 GOSUB (U=U*SIN S)
150 LET Y=U
```

Listing 5: Program for converting from spherical to Cartesian coordinates.

relative position and velocity for the other displayed. This saves nine more variables. However, it also eliminates a major challenge from the game. It's astonishing how far from your station you can wander while concentrating on combat, and how long it takes to turn around and get back. If you assume a fixed, forward firing weapon, you can use the same vector to represent both thrust and direction of fire. As a last resort, you can always go two-dimensional; this brings the number of variables used within limits (and greatly simplifies the conversion process).

Don't expect a great deal of accuracy from these routines. I got results within 1 degree and 1 percent for most cases, but certain values return much larger errors. As long as the Cartesian vectors are preserved from turn to turn, the errors do not accumulate and can be treated as quirks in the ship's ranging and detection system. Any attempt to rotate the coordinate system by converting to spherical coordinates, adding angular translations and converting back to Cartesian will quickly introduce large errors. Also remember that to keep the radius (R) from overflowing, X, Y, and Z must be limited to about ± 13,000.

If you plan to acquire a full BASIC for your system, you'd be well advised to wait for it before attempting a spacewar game. If, like me, you have to live with integer arithmetic for some time, a weekend's worth of work will give you a package of trigonometric capability that can serve as the nucleus for a wide variety of games and simulations.

Gravity wells and orbits can be handled nearly as easily as in a full BASIC; speed and position can be controlled accurately enough to make a docking maneuver painstakingly difficult. Another possibility is a version of lunar lander that includes the return to orbit. The software vacuum is likely to be with us for some time, but you can begin sharpening your skill as an astrogator now.■

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BYTE News ....

TI PERSONAL COMPUTER DELAY DUE TO HARDWARE PROBLEMS. Rumors abound that Texas Instruments has delayed introduction of their personal computer system because of problems encountered in the design of a new microprocessor circuit to be used in the system. The 9985 microprocessor is a 16 bit stripped down version of the 9940, which contains 2 K bytes of read only memory, 128 bytes of programmable memory, 32 bit I/O (input/output), 5 M Hz operation and timer/counter on one integrated circuit. Also, it has been reported that the FCC rejected the TI approach to the RF (radio frequency) modulator design. It is expected that TI will have solved these problems for the introduction of the system in June at the summer Consumer Electronics Show in Chicago.

RADIO SHACK HAS OVER 50 PERCENT OF PERSONAL COMPUTER BUSINESS. According to a report issued by Dataquest, a marketing research firm, Radio Shack sold approximately 100,000 TRS-80s, valued at $105 million dollars in 1978. This represented almost 10 percent of Tandy's business, and means that Radio Shack shipped over 50 percent of the total 1978 volume and 21 percent of the value of personal computer systems. Commodore was second, selling 25,000 PETs valued at $20 million, and Apple shipped 20,000 systems valued at $30 million. MITS/Pertec shipped 3000 units valued at $12 million, IMSAI shipped 5,000 valued at $18 million and all other personal computer makers shipped 35,000 units valued at $130 million. Dataquest adds to this the IBM and Hewlett-Packard table-top systems selling for less than $15,000. Thus IBM shipped 5,000 units valued at $95 million and Hewlett-Packard shipped 4,000 units valued at $80 million.

TANDY TO INTRODUCE NEW COMPUTER SYSTEM. Tandy has disclosed that it will soon introduce two, three and possibly four new computer systems in the second and third quarters of 1979.The systems will be designed to fit specific purposes. This is seen by industry experts as an attempt by Tandy to strengthen its market position in anticipation of Texas Instruments entering into the personal computer market. Tandy has had their TRS-80 in production for almost two years.

INTEL REPORTS 42 PERCENT INCREASE IN SALES FOR 1978. Intel, the pioneer in microprocessors, reported sales of just over $400 million dollars in 1978, compared to $282.5 million in 1977 — a 41.8 percent increase. In fact, sales in the last quarter increased over 61 percent as compared to the same period in 1977. Profits increased 39.7 percent; from $ 31.7 million to $44 million. Coincidentally, Zilog had sales of $18 million, and reportedly operated in the red for 1978.

MICROSOFT MOVING INTO 16 BIT SOFTWARE. Microsoft, a recognized leader in microprocessor software, plans to introduce a broad range of software for 16 bit processors, using the new Intel 8086 and Zilog Z-8000 microprocessors. Most of Microsoft's business is OEM (original equipment manufacturer). This indicates that several hardware manufacturers plan systems using these 16 bit processors. Microsoft will not desert the 8 bit area in which they plan to release a BASIC compiler and Pascal and APL interpreters.

INTEL PRESIDENT WORRIES ABOUT VLSI. Gordon Moore, Intel founder and president, was the keynote speaker at the recent International Solid States Circuit Conference. In his speech, he expressed great concern about the possibility that integrated circuit technology is too far ahead of applications. The industry is moving into the next generation of integrated circuits, called VLSI (very large scale integration) which feature devices with upwards of 400 K transistors, or 100 K gates. So far, the applications for such large devices have not developed. At the same meeting Dr Tom Longo, vice-president and chief technical officer at Fairchild Semiconductor, suggested that one possible application for VLSI might be the 64 bit microprocessor.

MICRODISKS ARE COMING. Microdisk is the name given to the new 8 inch hard disk drive, which is now being developed by several disk manufacturers. It is expected that at least four manufacturers will show these new disks at the NCC (National Computer Conference) show next month. These drives will fit into the same space as an 8 inch floppy disk, provide upwards of 20 M bytes unformatted storage, and use Winchester technology for high speed access. It is anticipated that the first production microdisks should be available late 1979, with full production not expected until mid 1980. Expected selling price in OEM quantities is $1500. This will probably translate to $3000 retail for a complete system including controller and power supply. At present 14 inch hard disks with 10 M byte storage are available at an end user cost of $7000 to $10,000.

16 BIT MICROPROCESSOR SCENE GROWING. Zilog began shipping Z-8000 samples in March, and Motorola expects to start sampling their 68000 this month. Production quantities should be available in the fall. Meanwhile, Intel has heated up competition by cutting the 8086 price by 23 percent; from $82.50 to $65.20 (4 MHz) and from $99 to $76.25 (5 MHz) in 500 quantity lots. The 8086 has been in production for almost a year; a very substantial lead time. However, the Zilog Z-8000 and the Motorola 68000 in particular are more powerful than the 8086, and Intel's price reduction probably represents a marketing strategy.

HP NOW PRIMARILY A COMPUTER COMPANY. Hewlett-Packard, which until now has been primarily a manufacturer of electronic instruments (voltmeters, frequency generators, etc), has disclosed that their computer business is now larger than their instrument business, and is growing at a faster rate. It is rumored that Hewlett-Packard will soon introduce a personal computer system.

COMMODORE REPORTS 8.6 PERCENT INCREASE FOR 1978. Commodore's 1978 Annual Report states that sales increased from $46 million to $50 million and that income rose from $1.5 million to $4 million, a 165 percent increase. There is little doubt that the PET and KIM accounted for the major portion of this increase. Like Tandy, Commodore does not break down its sales figures: however, industry experts estimate that over 25,000 PETs were sold in 1978. The Annual Report shows pictures of a PET with a standard keyboard, numeric pad and outboard tape recorder. Further, they promise a "new generation of PET computers" but do not say when.

IEEE AND ANSI WORKING ON PASCAL STANDARD. The IEEE (Institute of Electrical and Electronic Engineers) and ANSI (American National Standards Institute) have formed a joint committee to coordinate development of a Pascal standard. It is expected that the development of the standard will take several months.

PERKINS-ELMER LEAVES FLOPPY BUSINESS. Perkins-Elmer is the second major floppy disk manufacturer to leave the business within the last year. The Wangco division supplied drives to personal computer systems makers such as Cromemco, Heath Co and Intelligent Systems Corp. Although Wangco operated in the black and was growing, its profits were not apparently fulfilling Perkins-Elmer's expectations.

APL INTERPRETER AVAILABLE. The first APL interpreter for a microprocessor has been introduced by Vanguard Systems Corp, San Antonio TX. It is designed to run on a Z-80 computer system. As yet no data is available on how it compares to IBM APL. Several companies, including Microsoft and Scientific Time Sharing, have been promising a microprocessor APL package, but Vanguard is the first to reach the market.

LOW COST VOICE OUTPUT FOR COMPUTERS. If you are looking for a low cost, high quality voice output for your computer system, why not try interfacing the Texas Instruments Speak and Spell game to your system. This is done by interfacing some parallel ports to the keyboard connections of Speak and Spell. A short software driver routine for the interface was published in the January issue of the *Ottawa Computer Group Newsletter* (Box 132218, Kanata Ontario Canada).

MICROSOFT PASCAL. We have heard that Microsoft is going to announce a Pascal package. The Microsoft version is supposed to be compatible with UCSD, ANSI, and ISO Pascal. The initial implementations of Pascal will be on the 8080, 8086, Z-80, Z-8000, and LSI-11. Additional implementations will be produced as the demand arises. The 8080, 8086, and Z-80 versions will be CP/M compatible. The rumored price for Microsoft Pascal is $1,000.

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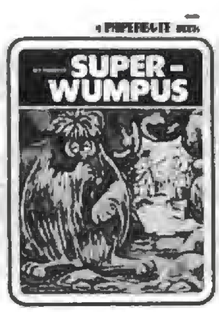
NEW

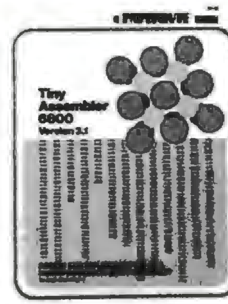
ISBN 0-931718-11-2
Editor: Christopher P. Morgan
Pages: approx. 128
Price: **$10.00**

SUPERWUMPUS is an exciting computer game incorporating the original structure of the WUMPUS game along with added features to make it even more fascinating. The original game was described in the book **What To Do After You Hit Return,** published by the People's Computer Company. Programmed in both 6800 assembly language and BASIC, SUPERWUMPUS is not only addictively fun, but also provides a splendid tutorial on setting up unusual data structures (the tunnel and cave system of SUPERWUMPUS forms a dodecahedron). This is a **PAPERBYTE™** book.



ISBN 0-931718-03-1
Author: Jack Emmerichs
Pages: 56
Price: **$6.00**

TINY ASSEMBLER 6800, Version 3.1 is an enhancement of Jack Emmerichs' successful Tiny Assembler. The original version (3.0) was described first in the April and May 1977 issues of BYTE magazine, and later in the **PAPERBYTE™** book **TINY ASSEMBLER 6800 Version 3.0.**



In September 1977, BYTE magazine published an article entitled, "Expanding The Tiny Assembler". This provided a detailed description of the enhancements incorporated into Version 3.1, such as the addition of a "begin" statement, a "virtual symbol table", and a larger subset of the Motorola 6800 assembly language.

All the above articles, plus an updated version of the user's guide, the source, object and PAPERBYTE™ bar code formats of both Version 3.0 and 3.1 make this book the most complete documentation possible for Jack Emmerichs' Tiny Assembler.

ISBN 0-931718-08-2
Author: Jack Emmerichs
Pages: 80
Price: **$9.00**

A walk through this book brings you into **Ciarcia's Circuit Cellar** for a detailed look at the marvelous projects which let you do useful things with your microcomputer. A collection of more than a year's worth of the popular series in BYTE magazine, **Ciarcia's Circuit Cellar** includes the six winners of BYTE's On-going Monitor Box (BOMB) award, voted by the readers themselves as the best articles of the month: **Control the World** (September 1977), **Memory Mapped IO** (November 1977), **Program Your Next EROM in BASIC** (March 1978), **Tune In and Turn On** (April 1978), **Talk To Me** (June 1978), and **Let Your Fingers Do the Talking** (August 1978).

Each article is a complete tutorial giving all the details needed to construct each project. Using amusing anecdotes to introduce the articles and an easy-going style, Steve presents each project so that even a neophyte need not be afraid to try it.

NEW

ISBN 0-931718-07-4
Author: Steve Ciarcia
Pages: approx. 128
Price: **$8.00**

is right now!

BASEX, a new compact, compiled language for microcomputers, has many of the best features of BASIC and the 8080 assembly language—and it can be run on any of the 8080 style microprocessors: 8080, Z-80, or 8085. This is a **PAPERBYTE™** book.

Subroutines in the **BASEX** operating system typically execute programs up to five times faster than equivalent programs in a BASIC interpreter—while requiring about half the memory space. In addition, **BASEX** has most of the powerful features of good BASIC interpreters including array variables. text strings, arithmetic operations on signed 16 bit integers, and versatile IO communication functions. And since the two languages, BASEX and BASIC, are so similar, it is possible to easily translate programs using integer arithmetic data from BASIC into BASEX.

The author, Paul Warme, has also included a BASEX Loader program which is capable of relocating programs anywhere in memory.

NEW

ISBN 0-931718-05-8
Author: Paul Warme
Pages: 88
Price: **$8.00**

PROGRAMMING TECHNIQUES is a series of **BYTE BOOKS** concerned with the art and science of computer programming. It is a collection of the best articles from BYTE magazine and new material collected just for this series. Each volume of the series provides the personal computer user with background information to write and maintain programs effectively.

The first volume in the Programming Techniques series is entitled **PROGRAM DESIGN.** It discusses in detail the theory of program design. The purpose of the book is to provide the personal computer user with the techniques needed to design efficient, effective, maintainable programs. Included is information concerning structured program design, modular programming techniques, program logic design, and examples of some of the more common traps the casual as well as the experienced programmer may fall into. In addition, details on various aspects of the actual program functions, such as hashed tables and binary tree processing, are included.

ISBN 0-931718-12-0
Editor: Blaise W. Liffick
Pages: 96
Price: **$6.00**

SIMULATION is the second volume in the Programming Techniques series. The chapters deal with various aspects of specific types of simulation. Both theoretical and practical applications are included. Particularly stressed is simulation of motion, including wave motion and flying objects. The realm of artificial intelligence is explored, along with simulating robot motion with the microcomputer. Finally, tips on how to simulate electronic circuits on the computer are detailed.

ISBN 0-931718-13-9
Editor: Blaise W. Liffick
Pages: approx. 80
Price: **$6.00**
Publication: Winter 1979

RA6800ML: AN M6800 RELOCATABLE MACRO ASSEMBLER is a two pass assembler for the Motorola 6800 microprocessor. It is designed to run on a minimum system of 16 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (such as Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

The Assembler can produce a program listing, a sorted Symbol Table listing and relocatable object code. The object code is loaded and linked with other assembled modules using the **Linking Loader LINK68.** (Refer to **PAPERBYTE™** publication **LINK68: AN M6800 LINKING LOADER** for details.)

There is a complete description of the 6800 Assembly language and its components, including outlines of the instruction and address formats, pseudo instructions and macro facilities. Each major routine of the Assembler is described in detail, complete with flow charts and a cross reference showing all calling and called-by routines, pointers, flags, and temporary variables.

In addition, details on interfacing and using the Assembler, error messages generated by the Assembler, the Assembler and sample IO driver source code listings, and **PAPERBYTE™** bar code representation of the Assembler's relocatable object file are all included.

This book provides the necessary background for coding programs in the 6800 assembly language, and for understanding the innermost operations of the Assembler.

ISBN 0-931718-10-4
Author: Jack E. Hemenway
Pages: 184
Price: **$25.00**

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LINK68: AN M6800 LINKING LOADER is a one pass linking loader which allows separately translated relocatable object modules to be loaded and linked together to form a single executable load module, and to relocate modules in memory. It produces a load map and a load module in Motorola MIKBUG loader format. The Linking Loader requires 2 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (for instance, Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

It was the express purpose of the authors of this book to provide everything necessary for the user to easily learn about the system. In addition to the source code and **PAPERBYTE™** bar code listings, there is a detailed description of the major routines of the Linking Loader, including flow charts. While implementing the system, the user has an opportunity to learn about the nature of linking loader design as well as simply acquiring a useful software tool.

ISBN 0-931718-09-0
Authors: Robert D. Grappel
& Jack E. Hemenway
Pages: 72
Price: **$8.00**
Winter 1979

TRACER: A 6800 DEBUGGING PROGRAM is for the programmer looking for good debugging software. TRACER features single step execution using dynamic break points, register examination and modification, and memory examination and modification. This book includes a reprint of "Jack and the Machine Debug" (from the December 1977 issue of BYTE magazine), **TRACER** program notes, complete assembly and source listing in 6800 assembly language, object program listing, and machine readable **PAPERBYTE™** bar codes of the object code.

ISBN 0-931718-02-3
Authors: Robert D. Grappel
& Jack E. Hemenway
Pages: 24
Price: **$6.00**

MONDEB: AN ADVANCED M6800 MONITOR-DEBUGGER has all the general features of Motorola's MIKBUG monitor as well as numerous other capabilities. Ease of use was a prime design consideration. The other goal was to achieve minimum memory requirements while retaining maximum versatility. The result is an extremely versatile program. The size of the entire MONDEB is less than 3 K.

Some of the command capabilities of MONDEB include displaying and setting the contents of registers, setting interrupts for debugging, testing a programmable memory range for bad memory locations, changing the display and input base of numbers, displaying the contents of memory, searching for a specified string, copying a range of bytes from one location in memory to another, and defining the location to which control will transfer upon receipt of an interrupt. This is a **PAPERBYTE™** book.

ISBN 0-931718-06-6
Author: Don Peters
Pages: 88
Price: **$5.00**

BAR CODE LOADER. The purpose of this pamphlet is to present the decoding algorithm which was designed by Ken Budnick of Micro-Scan Associates at the request of BYTE Publications, Inc., for the **PAPERBYTE™** bar code representation of executable code. The text of this pamphlet was written by Ken, and contains the general algorithm description in flow chart form plus detailed assemblies of program code for 6800, 6502 and 8080 processors. Individuals with computers based on these processors can use the software directly. Individuals with other processors can use the provided functional specifications and detail examples to create equivalent programs.

ISBN 0-931718-01-5
Author: Ken Budnick
Pages: 32
Price: **$2.00**

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Text continued from page 6

The parts for a simple 110 VAC lamp controller with one channel and a 10 A rating consist of:

One Sigma Instruments Model 221A-3-5D Hybrid Relay	$12.80
One AC Line Cord (surplus store)	$ 1.00
One AC Socket (local hardware store)	$ 1.35
One plug for my computer's parallel interface (DB-15)	$ 2.00
One aluminum minibox	$ 2.98
Miscellaneous interconnect wire	0.00
Total for one channel	$20.13

In an evening I had this relay wired to my computer, and ready for use in some applications. The most obvious home oriented application is, of course, the control of lamps in real time, assuming you have a real time clock and an appropriate operating system in your computer. At a high level, the simplest open loop lamp control procedure can now be implemented:

```
DO FOREVER
   BEGIN
      Wait Until 6;
      Turn On Lamp;
      Wait Until 11;
      Turn Off Lamp
   END;
```

Here I have used "DO FOREVER" to mean that the block will be repeated indefinitely with no ending condition in the program itself, although it is always possible to pull the plug or reset the computer with manual intervention. This is a procedure which is reiterated day in and day out as a background task of the computer system, with a real time executive which can monitor time. What is the advantage over a simple mechanical timer? It is, of course, the equivalent of that timer, but you have gained the ability to combine the relay control with the more sophisticated logic of a program.

With this simple amount of hardware, it is now possible to write programs which do much more than the mechanical timer. For example, if you want to give your house a lived-in look on the basis of lights, you can now add some randomization. Let's define a function, RANDOM(X), which returns a random number ranging from 0 to X, as do many standard compilers and interpreters. We can extend this procedure, using randomization of the starting and stopping times. In this next example, we add a second period in which the lamp is on:

```
DO FOREVER
   BEGIN
      Wait Until (6 + RANDOM(2));
      Turn On Lamp;
      Wait Until (8 + RANDOM(1));
      Turn Off Lamp;
      Wait Until (9 + RANDOM(1));
      Turn On Lamp;
      Wait Until (11 + RANDOM(3))
   END;
```

Our program has no inputs now, other than time synchronization with the computer's real time clock. The effect is that of having two periods with random starting and stopping times during the evening. Combine this with several other channels for different rooms of the house, and you have unique and random night lighting control for times when the house is vacant due to business or family trips. Of course, no computer (as yet) can collect piled up mail or clear snow from the driveway, but with a simple evening's effort of wiring up several relays in a control box, this sort of program can be left running when you go away.

In this example, I wanted to use this relay for lamp control. But, with a little imagination, you can control much more than lamps. The solid-state relays can turn on and off virtually any load within the current limitations of the device (10 A in this example) at the zero point of the AC waveform. This could include: turning on your coffeemaker in the morning (assuming that you primed it with water and grounds the night before); turning on a hot plate (of less than 1000 W) under a tea kettle in the morning; responding to a voice input microphone for the particular room you are in by recognizing the words *on* and *off* (all using techniques discussed in past BYTE issues). There is no reason why other appliances, such as the motor of my attic fan, could not be controlled in the same way.

The point is, the act of creating hardware for such brute force things as turning AC lines on and off has been reduced to wiring, and is now an easily solved problem. Just as we all experiment with software, we can now very simply experiment with software that controls significant hardware outside the computer system. All it takes is the willingness to spend some time wiring the particular details needed to make your system's output port talk to the real world. Hardware is not hard to control, once you've got a complete computer system with real time clock and parallel output data ports. ■

Event Queue

In order to gain optimum coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications Inc, 70 Main St, Peterborough NH 03458. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

May 1-3, 1979 Southwestern Computer Conference, Myriad Convention Center, Oklahoma City OK This conference, sponsored by the Oklahoma State University Technical Institute in cooperation with the Data Processing Management Association and the Association for Systems Management, will include 150 exhibit booths and 60 seminar presentations Contact E Z Million, OSU Technical Institute, 900 N Portland, Oklahoma City OK 73107

May 7-11, Data Base Concepts and Design, Kansas City KS Sponsored by the American Management Association, this course will feature practical information, workshops and case studies to help the participant understand structure, concepts, design, software and management Contact American Management Associations, 135 W 50th St New York NY 10020, (212) 586 8100

May 11-13, The West Coast Computer Faire, San Francisco Civic Auditorium This is a conference and exposition on personal computers for home business, and industry. Contact Computer Faire, POB 1579, Palo Alto CA 94302, (415) 851 7075

May 14-16, Implementing Cryptography, The New York Sheraton, New York NY This seminar will present current techniques that protect transmitted and stored data, authenticate messages and system users, and generate electronic digital signatures Contact Ketron Inc, Valley Forge Executive Mall, # 10, 530 E Swedesford Rd, Wayne PA 19087

May 15-17 Micro/Expo '79, Centre International de Paris, Paris FRANCE Contact Sybex Inc, 2020 Milvia St, Berkeley CA 94704

May 15-17, First Education Computer Fair, Detroit Plaza Hotel, Detroit MI This fair will be held in conjunction with 1979 Association for Educational Data Systems 17th Annual Convention The theme of the fair will be the use of microprocessors in education Contact Bruce G Alcock Riverdale Country School, W 253 St and Fieldston Rd, Bronx NY 10471

May 15-18, 1979 Association for Educational Data Systems 17th Annual Convention, Detroit Plaza Hotel, Detroit MI The convention program will focus on computer applications, computer resources, computer related curriculum, application development methodologies and futures Exhibits, user group meetings and vendor sessions will also be offered Contact Arthur W Daniels Jr, 31202 Dorchester, Madison Heights MI 48071

May 17-18, Microcomputers in Education and Training, Arlington VA Contact Society for Applied Learning Technology 50 Culpeper St, Warrenton VA 22186

May 21-23, Distributed Data Processing, Logan Airport Hilton, Boston MA A detailed perspective of the decisions to be made in planning, implementing and maintaining distributed data processing systems Contact American Management Associations, 135 W 50th St, New York NY 10020

May 21-24, Eighth Annual Incremental Motion Control Symposium, Ramada Inn, Urbana IL Contact Dr B C Kuo, POB 2772, Station A, Champaign IL 61820

May 21-25, Systems Analysis Workshop, Chicago IL This workshop will teach systems analysts and others needing systems analysis skills to use a practical set of tools and techniques to evaluate user requests and document requirements for new data processing systems Contact Brandon Systems Institute, 4720 Montgomery Ln, Bethesda MD 20014

May 21-25, Structured Programming and Software Engineering, The George Washington University, Washington DC This course is designed for experienced program architects, designers and managers It will provide up-to-date technical knowledge of logical expression, analysis and invention for performing and managing software architecture, design and production Presentations will cover principles and applications in structured programming and software engineering Design workshops with analysis and review sessions will provide actual practice in problem solving. Contact George Washington University, Con-

tinuing Engineering Education, Washington DC 20052.

May 23-24, The Clemson Conference on Small Computers: Application for Business, Industry, Education, Medicine, Clemson University, Clemson SC. This conference will be of interest to individuals interested in small computers who have a wait and see attitude. Persons who are already involved with small systems will find the conference interesting and beneficial. There will be discussions on a wide variety of applications, tutorials on small systems and exhibits of equipment. Contact William J Barnett, Associate Professor, College of Engineering, Clemson University, Clemson SC 29631.

May 24-26, Computers in Critical Care and Pulmonary Medicine, Yale University School of Medicine, Norwalk CT. The purpose of this meeting is to bring together computer scientists, biomedical engineers and physicians who are interested in the application of computer technology to the diagnosis and treatment of critically ill patients. The program will consist of one day devoted to respiratory monitoring and two days devoted to the presentation of papers pertaining to the application of computer technology to the monitoring of critically ill patients. Contact S Nair MD, Norwalk Hospital and Yale University School of Medicine, Norwalk CT 06856.

June 3-6, 1979 International Summer Consumer Electronics Show, McCormick Place, Chicago IL. This show serves as the marketplace for the entire consumer electronics industry. Contact Consumer Electronics Show, 2 Illinois Ctr, Suite 1607, 233 N Michigan Av, Chicago IL 60601.

June 4-7, 1979 National Computer Conference, New York Coliseum, New York NY. NCC '79 will feature a premier showcase of the state of the art in computing and data processing. Leading organizations, large and small, will show the latest equipment and services in approximately 1500 booths. More than 100 program sessions are planned, emphasizing the four major areas of management, applications, science and technology, and social implications. In conjunction with NCC '79, the Personal Computing Festival of commercial exhibits, application demonstrations, and technical sessions on microcomputer systems and applications will be held at the Americana Hotel. Contact NCC '79, c/o American Federation of Information Processing Societies Inc, 210 Summit Av, Montvale NJ 07645.

June 6-8, Twelfth Annual Association of Small College Computer Users in Education Conference, Denison University, Granville OH. Sessions will include the presentation of papers and demonstrations of the educational use of microcomputers, computer text book surveys, discussions with authors of computer texts, administrative uses of computers in small colleges, and a tutorial on microprocessors. Contact Douglas Hughes, Computer Ctr, Denison University, Granville OH 43055, (614) 587-0810.

June 6-8, Eighth Annual Conference of the MUMPS Users Group, Marriott Hotel, Atlanta GA. Papers will be presented on all aspects of MUMPS development, implementation, and use. Contact Judith Faulkner, Program Committee, Department of Psychiatry, Clinical Sciences Ctr, 600 Highland Av, Madison WI 53792.

June 6-8, Computer Contract Negotiation, New York NY. This three day course is designed to give participants sound answers to the complex ramifications of preparing and negotiating computer contracts. Contact Brandon Consulting Group Inc, 505 Park Av, New York NY 10022.

June 19-21, International Microcomputers/Minicomputers/Microprocessors '79, Palais des Expositions, Geneva SWITZERLAND. Focusing on the changing state of the art in mini/microcomputers and microprocessors, the 1979 conference program will probe advances in systems and equipment, with emphasis on practical applications and uses of minicomputers and microcomputers as well as the techniques important to their development.

June 20-22, The 1979 Symposium of the Wilmington Section of the Instrument Society of America, University of Delaware, Newark DE. The symposium theme, "Measurement Technology for the 80's," is being programmed by three of ISA's divisions: Process Measurement and Control, Analysis Instrumentation, and Water and Waste Water Industries. Contact A H Straightiff, E I Du Pont de Nemours and Co Inc, (302) 366-3810.

June 27-29, Machine Processing of Remotely Sensed Data, Purdue University, W Lafayette IN. The symposium will focus upon the theory, implementation and novel applications of machine processing of remotely sensed data. Contact Purdue University, Laboratory for Applications of Remote Sensing, 1220 Potter Dr, W Lafayette IN 47906.

July 9-20, Computing Systems Reliability, University of California, Santa Cruz CA. Contact Institute in Computer Science, University of California Extension, Santa Cruz CA 95064. ■

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Nybbles

TMS-9900 Monitor

Jeremy O Jones
Alan Jones
Dept of Computer Science
Trinity College Dublin
Dublin 2–IRELAND

Everyone has their own idea of what a good monitor should and should not do. Our TMS-9900 monitor is aimed at a small Texas Instruments 9900 system (without disks) with a terminal (64 by 32 character screen size) for I/O (input/output). It has been designed so that programs (which may be cross assembled elsewhere) can be debugged efficiently. To this end, the monitor contains an instant assembler, a disassembler, and comprehensive user program tracing facilities. The instant assembler allows modifications in code to be made quickly, since calculating op codes is difficult because the op code fields are not aligned on nybble boundaries.

The monitor occupies slightly less than 256 bytes of memory and has been assembled to occupy hexadecimal locations F400 thru FFFE. The monitor allows the user to examine and change memory locations; disassemble instructions; assemble mnemonics; perform memory searches; move blocks of memory; set breakpoints; trace program operation; and other functions.■

The Nybbles Library is an inexpensive means for BYTE readers to share some interesting but specialized forms of software. These programs are written by readers with small computers and printer facilities, and are therefore designed for particular systems. The algorithms and programming techniques in these programs can be directly used by readers with similar equipment, or can serve as an inspiration for improvisation on computers of different characteristics.

Potential authors of such programs should send us a self-addressed stamped envelope, with a request for a copy of our Guidelines for Nybbles Authors. *Payment for Nybbles items is based on sales and length of the item. Rates are set at the time of acceptance.*

This month the "TMS-9900 Monitor" (# 106) has been added to the Nybbles Library. To order your personal copy, at $3.00 postpaid, fill out the coupon below.

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The Intel 8275 CRT Controller

Chris Tennant
119 S Kaspar
Arlington Hts IL 60005

About the Author

Chris Tennant is an electrical engineering graduate of the University of Illinois. His specific areas of interest are communications and computer systems. As a hobby, Chris has been building the Z-80 S-100 microcomputer partially shown in the pictures.

Chris works in the University's Psychology department as an electronic technician of the Cognitive Psychophysiology Lab. Brain wave experiments are run, and PDP-11 minicomputers abound in this environment. Along with a fellow senior technician he has designed and built digital and analog devices to interface the computers to the test subjects. Microprocessor projects are both in progress and on the drawing board.

The Intel 8275 is a programmable video display controller manufactured by Intel Corporation. It is sealed in a 40 pin dual in line package. The device is presently expensive, but it replaces more costly circuitry of a greater size and complexity.

The 8275 has full color capability, a light pen option, many display modes, and simplicity in both hardware and software. This article's focus is on the ability and overall value of an 8275 based video terminal. Since value is a relative judgment, frequent comparisons will be made between an 8275 based terminal and other kinds of terminals presently available.

Video terminals can be divided into two groups:

- *Dedicated memory terminals.* These are prevalent in microprocessor systems. A typical terminal contains 1 K or 2 K bytes of memory for screen data. The memory is used almost continuously for screen refresh, and hence is dedicated to the terminal. The processor may have both read and write access to the video memory. Dedicated memory terminals include bit mapped terminals. Every dot location on a bit mapped display is addressable. Many bit mapped terminals allow read access as well as write access.
- *Direct memory access terminals.* This kind of terminal is connected to a processor bus. The video memory actually resides in processor memory. It is not dedicated memory, so the information must be transferred from the processor to the screen for each screen refresh. Usually processor operation is suspended for refresh, resulting in lower processor throughput.

For the most part, this article considers the use of an 8275 and a microprocessor

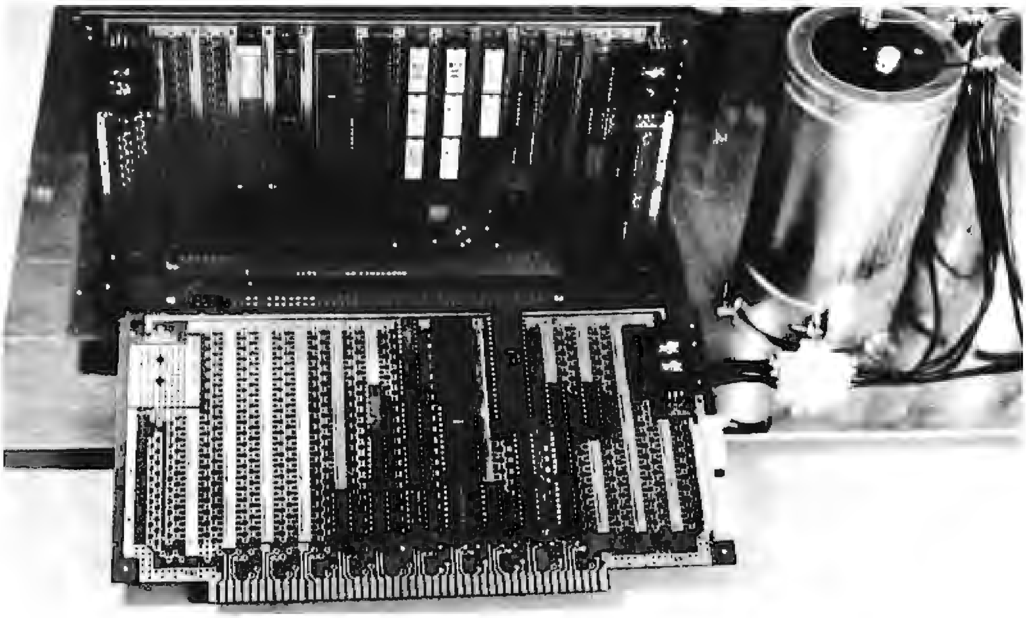

Photo 1: The author's 2 board video controller using the Intel 8275 video display controller.

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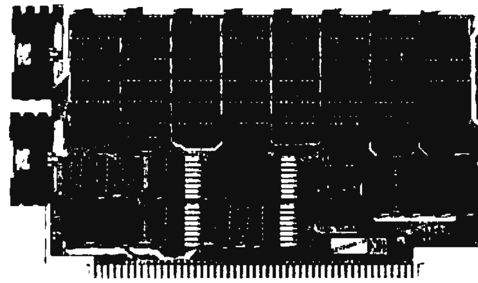

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Econoram XII-24™	24K X 8	S-100	8K boundaries	static	**$479**	**$539**	**$649**
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Econoram VI™	12K X 8	H8	static	2 MHz	1-8K, 1-4K	**$200**	**$270**	N/A
Econoram VII™	24K X 8	S-100	static	4 MHz	2-4K, 2-8K	**$445**	**$485**	**$605**
Econoram IX™	32K X 8	Dig Grp	static	4 MHz	2-4K, 1-8K, 1-16K	**$649**	N/A	N/A
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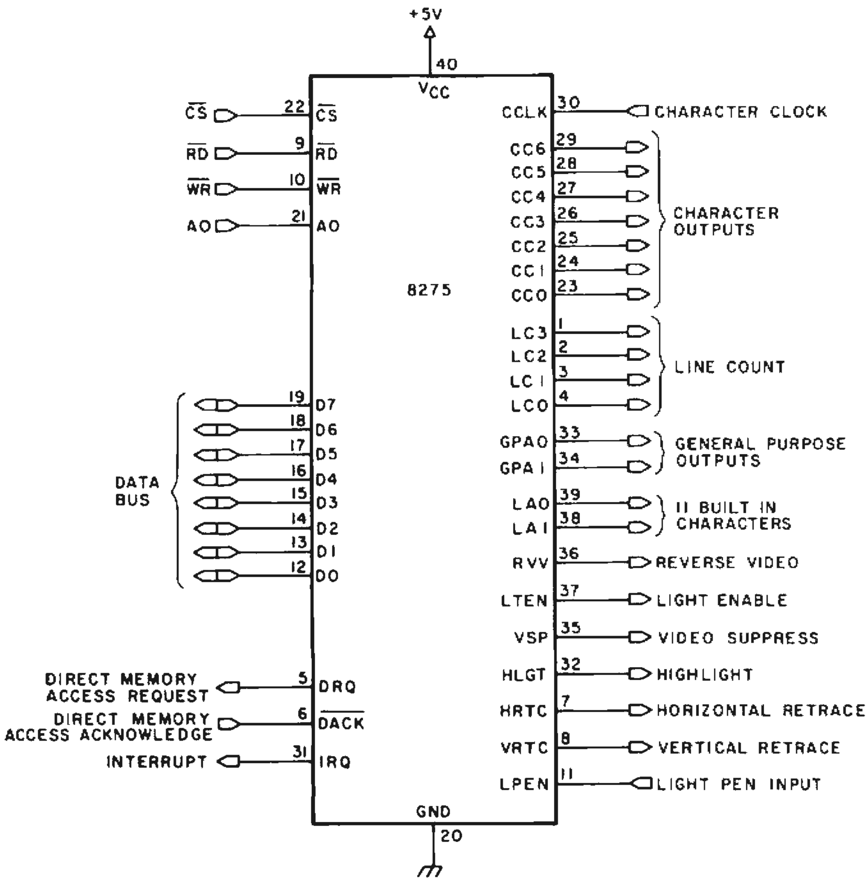

Figure 1: A functional block diagram of the Intel 8275 video controller integrated circuit.

system as a terminal. Hence, this terminal is intended to be connected to a large computer. The hobbyist, on the other hand, often uses a microprocessor as a stand alone computer. For the hobbyist, processor time is more important than for the user of a microprocessor based terminal connected to a larger computer. Therefore, the potential homebrewer reading this article would understandably be skeptical of the 8275 because it can rob up to 25 percent or more of the processor's time. But after all things are considered, I believe that even the experimenter will be tempted by the features of the 8275 as I was.

An example of how the 8275 can be uniquely applied to a real life situation will help to orient the reader toward its abilities. A power generating plant could employ an 8275 based terminal in its main control room. Many tables of data might be kept in the computer defining the status of various generators, the power load of various points in the city and graphs of previous days and weeks' status.

The operator, using an 8275 based terminal, could flip between the pages of information. The operator could watch statistics change dynamically. Headings of tables would be underlined. Important statistics would be printed as reverse video characters, yellow alert information would be highlighted, and disaster information would be highlighted and blinking. This way, the operator can find the necessary information at a glance. If one is looking for all disaster and yellow alert data, one can spot it immediately, at a time when seconds count. If one is looking for other kinds of information, it can also be found quickly because it, too, has its own kind of signature. Dedicated memory terminals and bit map terminals would all be too slow for this application involving emergency situations. Once the operator has the needed information, he or she can initiate corrective measures through the same terminal.

What follows is an introductory explanation of 8275 operation. Its merits and weaknesses are judged by comparing it to scrolling terminals, dedicated memory terminals and bit mapped (also dedicated memory) terminals. Finally, the frequent uses of terminals in general are measured against the 8275's abilities. I hope to show that the 8275 meets most of these needs better than the other terminals.

Device Description

The 8275 video controller requires two peripheral items in order to operate: a microprocessor and a direct memory access device. The microprocessor initializes the 8275 during power-up. It also shares its memory with the 8275. Figure 1 is a functional block diagram of the 8275. The lefthand signal lines interface to the system bus. The processor communicates with the 8275 via the bidirectional data bus and standard handshaking. The single address line, A0, indicates that this device occupies two locations in memory or I/O (input/output) space. The 8275 communicates with the direct memory access controller via the direct memory access request output and direct memory access acknowledge input. The interrupt output is used to coordinate direct memory access activity.

The video control lines are described below.

- *Character Clock* input. The character clock tells the 8275 how fast characters are to be output to the screen. It also clocks the several internal counters which provide the screen timing. Direct memory access timing is based on the character clock as well.

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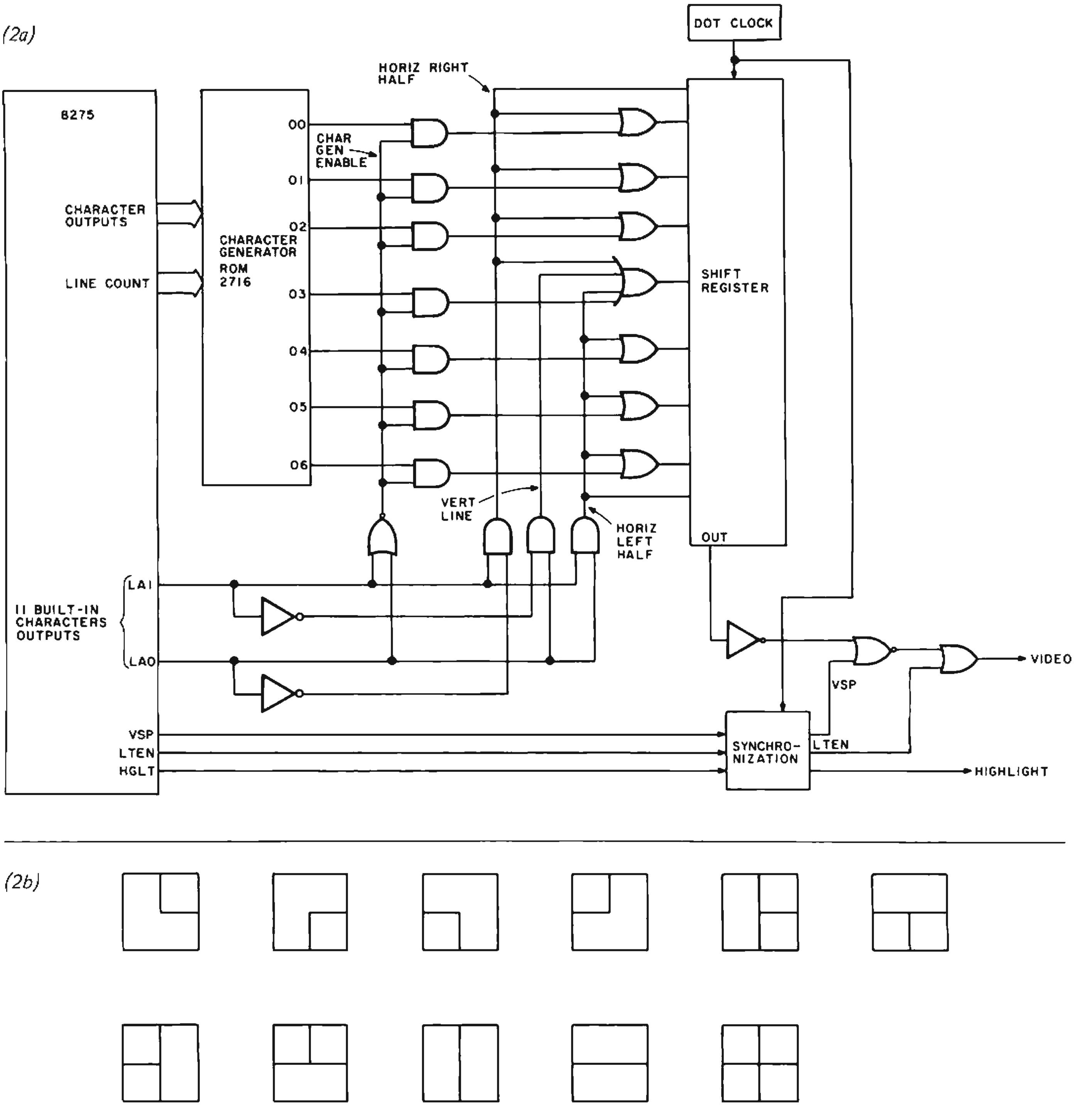

Figure 2: A description of the circuitry needed for generating built-in characters. The resulting characters that are output are shown in figure 2b.

- *Line Count* outputs. These four outputs inform the character generator which scan line the screen is tracing. At the top of a character row, the line count is 0. After the next retrace, the line count is 1, and so forth. The line count tells the character generator which row of dots to output. The line count is programmable from one to 16 scan lines per character.

- *Character* outputs. These seven bits of output determine which one of 128 possible characters is to be displayed. They typically output the ASCII code representations of the characters.

- *Two Built in Characters* outputs. These signals are used to provide 11 characters without the use of a character generator. The use of these outputs may add needless complexity to the video circuitry. Figure 2a shows the circuitry needed to provide the characters in figure 2b. These characters are used for drawing boxes around fields on the screen. A lower chip count and several hours of building time are sacrificed for these 11 characters. It is recommended that the characters be put in the character generator read only memory. The 2708 programmable read only memory makes a good 128 by 8 by 8 character generator. I chose a programmable read only memory because I could not find a character generator I liked on the market.

- *Two General Purpose* outputs. These two bits can be individually programmed to change logic levels at predetermined points on the screen. Their function is left to the designer.

- *Reverse Video* output. This bit tells the video circuitry that the negative image of the character is to be displayed. A white character on a black background is therefore displayed as a black character on a white background.

- *Light Enable* output. When this output is high, an override of the character generator occurs and only white dots are sent to the screen. This output is used for the underline function and to display the cursor.

- *Video Suppress* output. This output has the opposite function of light enable. It blanks the screen. It also provides blinking characters, invisible retrace and "end of line" blanking (which will be explained later).

- *Highlight* output. Characters of two intensities are possible because of this output.

- *Horizontal Retrace* output. Raster timing is generated internally. This output synchronizes the video monitor's horizontal oscillator with the 8275.

- *Vertical Retrace* output. This output synchronizes the monitor's vertical oscillator with the 8275. The duration of both kinds of retrace is programmable.

Number	Type	+5 V	GND	−5 V	+12 V
IC1	8275	40	20		
IC2	8212	24	12		
IC3	74LS165	16	8		
IC4	74169	16	8		
IC5	7404	14	7		
IC6	7400	14	7		
IC7	7486	14	7		
IC8	7402	14	7		
IC9	7432	14	7		
IC10	7416	14	7		
IC11	7408	14	7		
IC12	7414	14	7		
IC13	74174	16	8		
IC14	74157	16	8		
IC15	74157	16	8		
IC16	74157	16	8		
IC17	7400	14	7		
IC18	74126	14	7		
IC19	2102	10	9		
IC20	2102	10	9		
IC21	2102	10	9		
IC22	2102	10	9		
IC23	2102	10	9		
IC24	2102	10	9		
IC25	2102	10	9		
IC26	2102	10	9		
IC27	2708	24	12	21	19
IC28	7400	14	7		
IC29	74426	14	7		
IC30	74426	14	7		
IC31	74426	14	7		
IC32	74426	14	7		
IC33	7405	14	7		
IC34	7421	14	7		
IC35	7486	14	7		
IC36	74139	16	8		

Table 1: Power pin assignments for the circuits in figures 3 thru 6.

- *Light Pen* input. A positive edge on this input latches the present row and column positions. One possible light pen circuit is shown in figure 3. The light pen is a phototransistor. It is connected to a differentiator (the resistor/capacitor network) and a comparator. The comparator detects a positive spike caused by the electron beam intensifying the phosphor on the screen. A Schmitt gate gives the video controller a clean, sharp edge. The controller now has the row and

Text continued on page 139

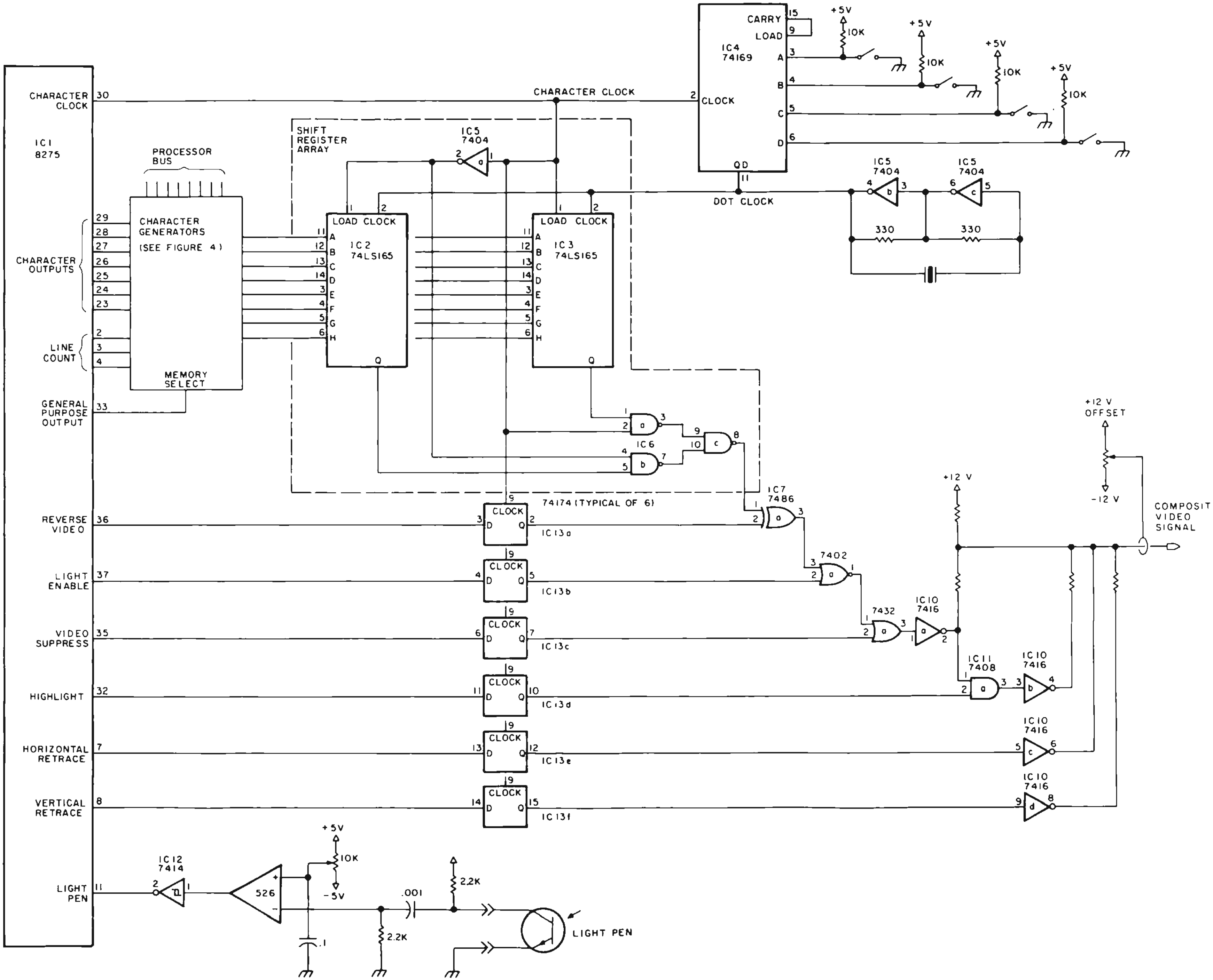

Figure 3: A possible configuration of the 8275 to produce a composite video signal. The number of dots which make up a character is determined by the dot clock.

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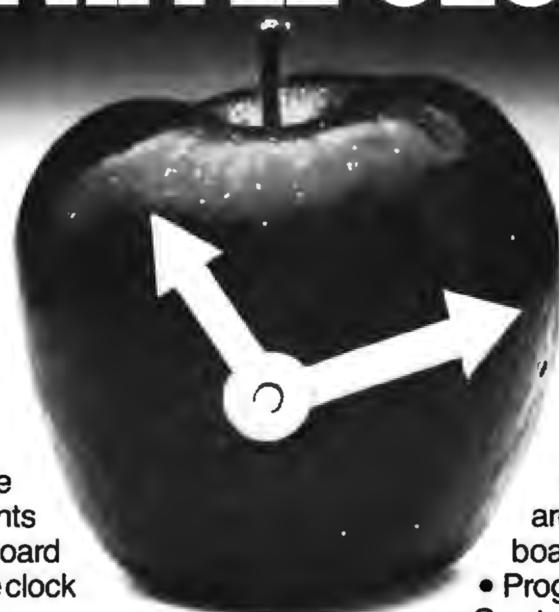

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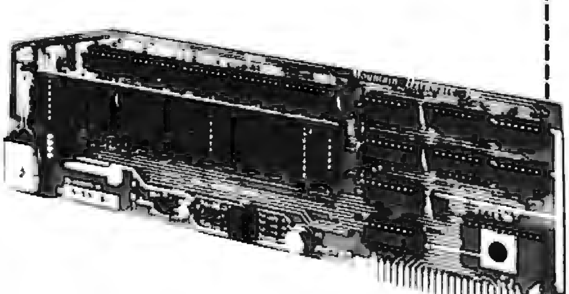

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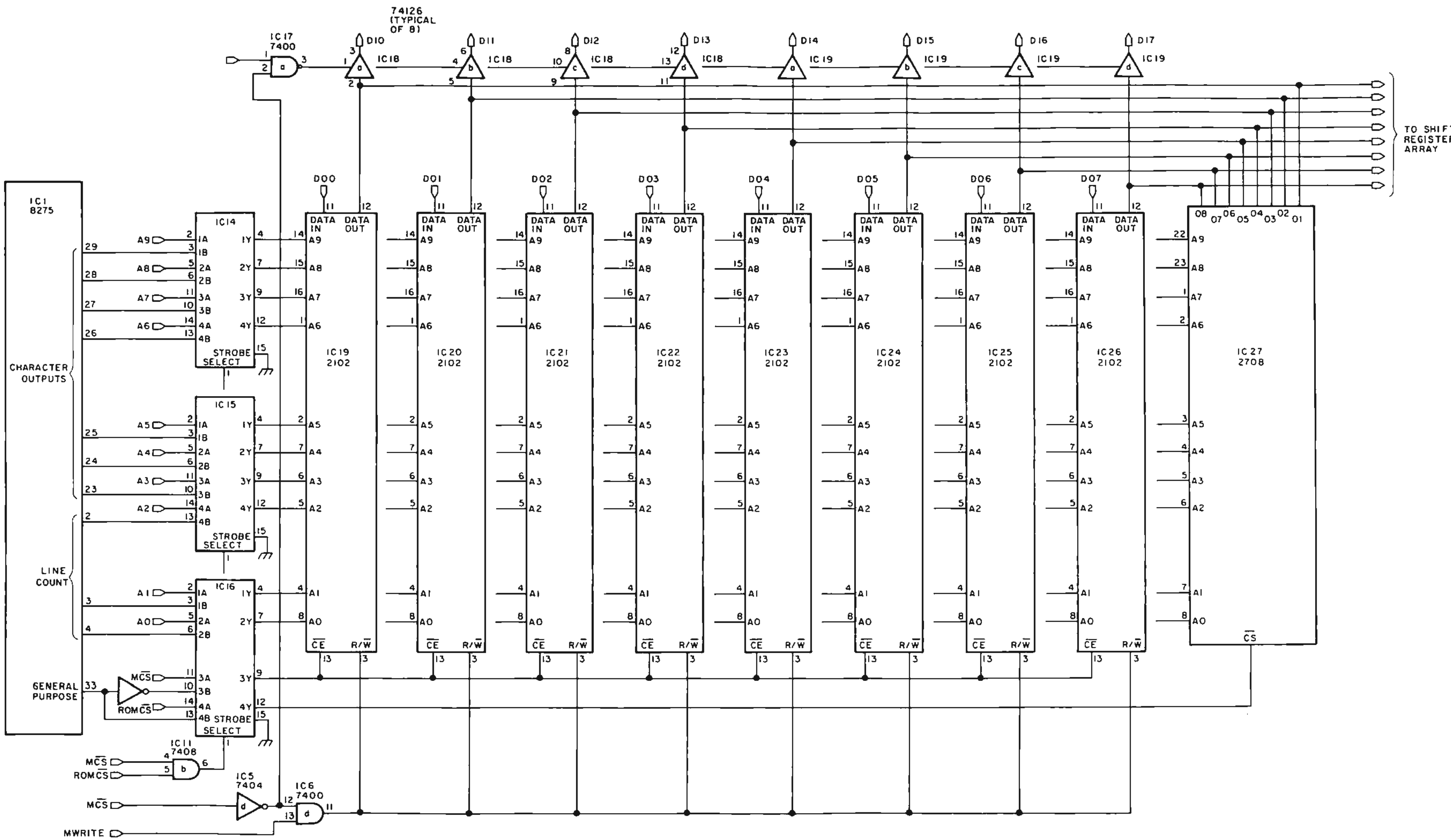

Figure 4: Adding the character generator circuitry to the 8275 video controller. This particular configuration has 128 predefined characters and 128 programmable characters.

Text continued from page 135:
column positions latched in its internal registers.

It is good to know that the two *General Purpose*, the *Reverse Video*, and the *Highlight* outputs all operate identically. Their functions can be changed at the will of the designer. Any three of the outputs could be used to represent the primary colors. Then either additional chroma circuitry or direct connection to the electron guns' amplifiers could turn the output bits into actual colors. This feature could be very important to experimenters who may someday upgrade their systems to have color video.

Video Display Circuitry

Since this article is primarily concerned with the 8275's operation, discussion of the circuit will be limited mostly to the composite video output circuitry. The purpose of this section is to further acquaint the reader with the 8275. Figure 3 shows one configuration for producing a composite video signal. A dot clock is divided down to provide the character clock. If the dot clock is divided by n, there are exactly n dots per character horizontally. The character clock is connected to the 8275, but it must also connect to two other points. It controls the loading of the shift register, and it clocks several bits through flip flops. The shift register turns the parallel dot data from the character generator to serial form for the video display. The six bits (*Reverse Video, Light Enable, Video Suppress, Highlight, Horizontal Retrace and Vertical Retrace)* are delayed by one clock by passing them through the flip flops to synchronize them with the slow speed of the character generator. They are then gated with the character data through some logic gates to produce the composite video output signal.

My character generator (figure 4) has 128 fixed characters and 128 programmable characters. The programmable characters are interfaced to the processor bus in such a way that the processor has priority of access over the 8275. The video controller selects one of the 128 character groups with a *General Purpose* output. Note that up to 512 characters are possible if both *General Purpose* outputs are used. The simplest character generator would have no interface to the processor bus and would consist of a single character generator.

Figure 3 gives the reader an idea of the complexity of the output circuit. Each box represents one integrated circuit (if a simple character generator is assumed), except for the six flip flops, which are all contained

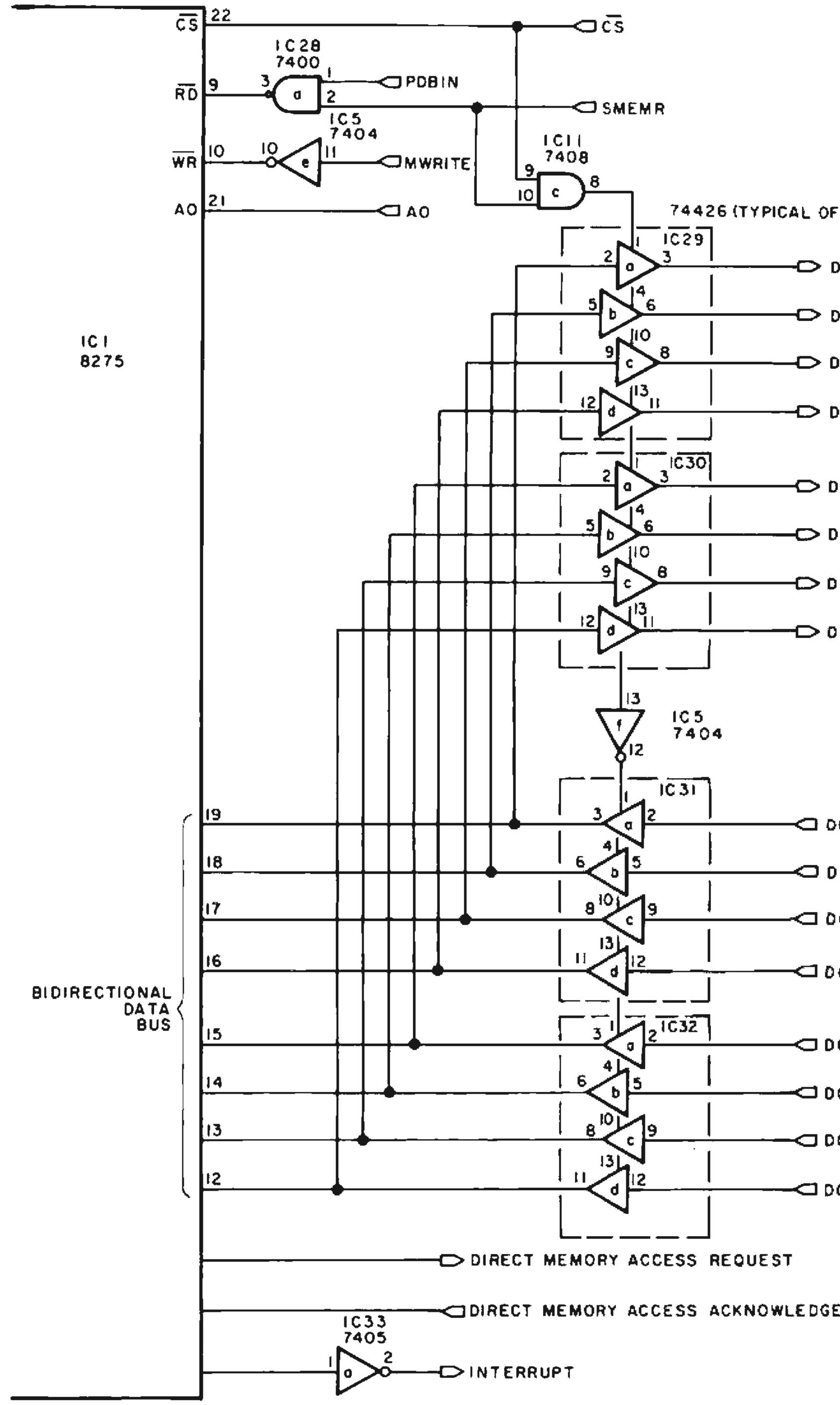

Figure 5: This circuitry will interface the video controller to the computer's bus.

in a single chip. A total of about a dozen chips is required to realize the output logic. With a crystal and some resistors and capacitors, the output circuit is complete.

Screen Format

The screen format of the 8275 is programmer definable. Characters can be displayed either single or double spaced. The

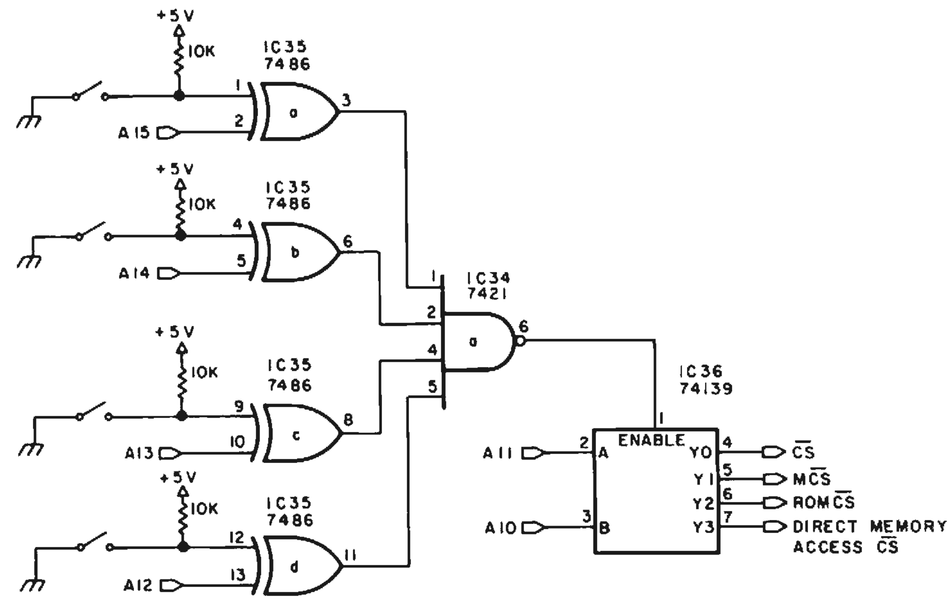

Figure 6: The address decoding circuitry is added to the character generator circuitry of figure 4 to complete the video controller.

height of each character is programmable from 1 to 16 raster scan lines. The number of characters in a row is programmable from 1 to 80. The number of rows from top to bottom is programmable from 1 to 64. Unfortunately, the monitor's timing is not infinitely flexible. Some screen formats would be impossible for a monitor to synchronize with. For example, a screen format of two characters horizontally by two characters vertically would not be possible. A horizontal or vertical retrace signal would come from the 8275 long before the monitor's beam was at the end of the screen. Another limitation may be the bandwidth of the monitor. If the monitor has a low bandwidth, the characters may become smeared and difficult to read if there are too many characters in a horizontal row. The parameters also depend on the character clock going into the 8275.

In spite of all this confusion, there is a range of screen and character formats which is acceptable to the monitor, and one of them must be chosen before data can be displayed.

The screen format parameters are loaded into the 8275 after power-up, but can also be changed dynamically. This means that different screen and character formats can be used to represent different kinds of information. For example, a tightly packed screen of 4 K characters might be used for graphics, a medium packed screen of 2 K to 3 K characters might display text, and a loosely packed 1 K character screen might be a table of contents or other directive data. The user could tell at a glance what kind of information he is looking at just by the screen format. Only six bytes are required to reprogram the 8275's screen and character format.

Controller Circuitry

Building a direct memory access circuit requires special care. The device is master of the bus at one moment, a normal peripheral the next; a situation which requires some signal reversing. Furthermore, when it is the bus master, it can do some odd things to the timing.

The Intel 8257 direct memory access controller will set up a memory address and do a normal memory read by making $\overline{\text{MEMRD}}$ low. Then, the I/O write ($\overline{\text{IOWR}}$) will go low to strobe the data to the I/O device (the video controller in this case). The signal $\overline{\text{DACK}}$ informs the video controller that it alone is intended to receive the data. If the designer is not careful, other I/O devices may be accidentally addressed. Each direct memory access cycle puts a new address on the bus. The cycling of addresses and the strobing of $\overline{\text{IOWR}}$ will eventually access all I/O devices unless disabling of I/O devices is designed into the system. The job is more complex when dealing with S-100 signals.

My direct memory access controller has evolved its way out of S-100 compatibility. Stubbornly using Intel's direct memory access controller meant altering boards and the bus. Some nonstandard things needed to be done. Indeed, my devices are not even I/O mapped as the 8275 assumes. Rather than raking over the details of my circuit, I recommend the reader check on other direct memory access devices, such as the Zilog Z-80 DM-8. It has separate cycles for reading

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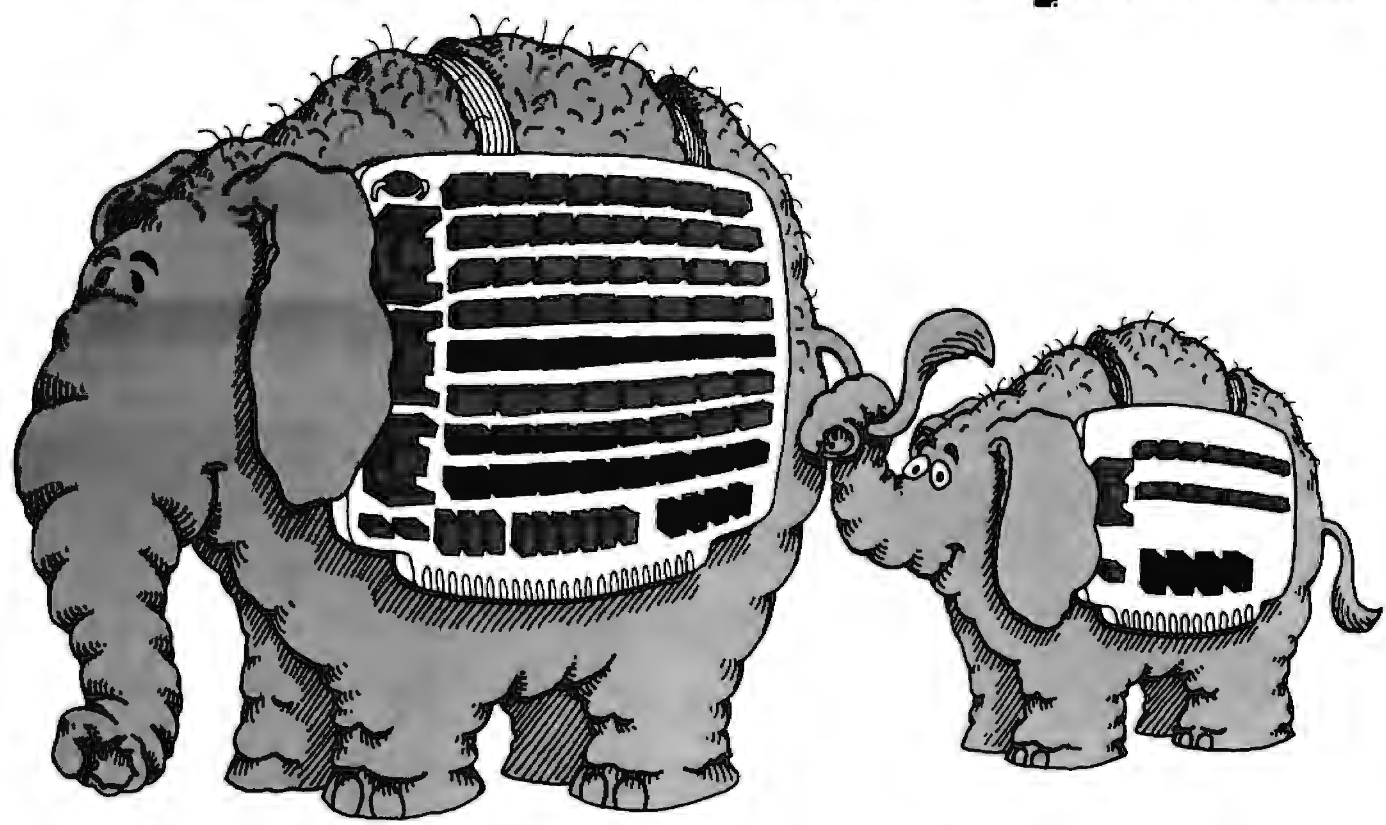

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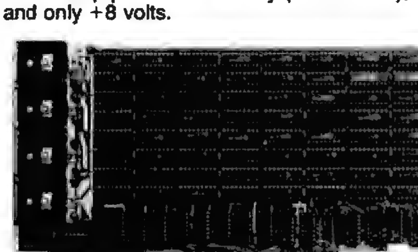

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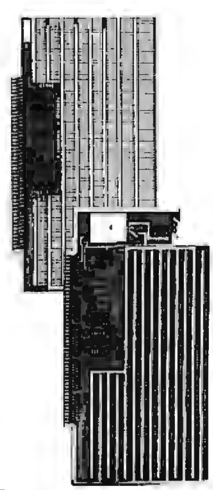

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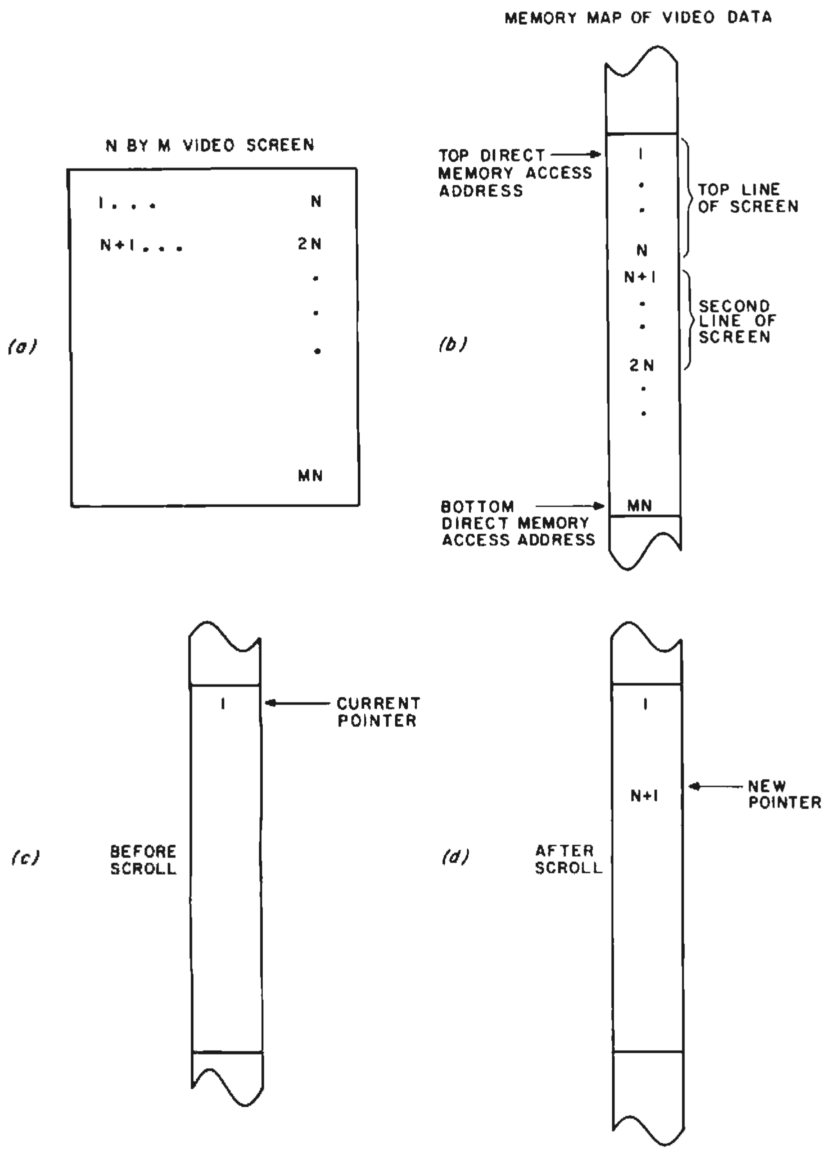

Figure 7: An example of scrolling and using direct memory access. The screen (7a) resides in processor memory (figure 7b). Scrolling takes place when the current direct memory access pointer is moved as shown in figures 7c and 7d.

memory and writing to a peripheral. It also allows memory mapped I/O. Of the two direct memory access devices mentioned, it alone can be considered S-100 compatible.

Direct Memory Access

Characters which are to be displayed on a video screen are transferred by direct memory accessing from processor memory. The direct memory access process also retrieves the special attributes such as reverse video, highlight, underline, blink, and two general purpose signals. A series of direct memory access transfers occur for each character line to be displayed. After the entire screen has been written, vertical retrace occurs, and the direct memory access is repeated. The microprocessor must wait while the transfer takes place. This may interfere with as much as 25 percent of the processor's time. This figure does not take "cycle stealing" into account. (Cycle stealing is a condition where the processor allows the direct memory access controller to take control of the system bus while the processor is doing internal work.) The processor is not using the bus anyway, so the direct memory access controller steals that clock cycle or cycles. For an 8080A, the timing diagrams seem to indicate that no cycle stealing takes place. The processor-direct memory access handshaking is too slow. This will be true for either controller mentioned earlier. My 25 percent figure assumes a full 2 K screen with no cycle stealing, and using the Intel controller at a 2 MHz clock frequency. The screen is refreshed at a rate of 60 Hz.

A strong argument against the 8275 is that it cuts into processor time while merely displaying a static picture. Other terminals for microprocessors, such as those with dedicated video memory, can operate without disrupting processor operation at all. The only time the processor uses up with respect to video is the time it takes to change the screen.

Opponents of the 8275 point out the direct memory access problem as its greatest weakness. But using direct memory access also has its advantages. The reader can weigh the advantages of the 8275 against this overhead disadvantage. I find that, for my purposes, the flexibility and display power offered is worth the loss of processor throughput. Furthermore, as will be seen, the overhead can be reduced.

With direct memory access capabilities, the processor memory is shared with video memory but without timing conflicts. Dedicated memory video terminals, on the other hand, give the processor priority in memory operations. If the terminal is writing characters when the processor takes over its memory, the screen becomes undefined, and a "scratch" mark results. Scrolling, page changing and other operations which require around 2,000 reads and 2,000 writes (for a typical 2 K screen) can produce temporary havoc on the screen. A dynamically changing screen can be annoying to look at. Video memory for the 8275 can be read from or written into at any time without scratch marks because only one device operates at a time – either the controller or the processor.

The direct memory access controller is programmable to work on any section of memory. It can, in fact, be programmed to change source locations at any time. This means that page changes of the video screen can be made by changing the accessed address; a task which requires half a dozen writes. This compares with 2,000 reads and 2,000 writes of a block transfer in dedicated memory terminals.

With direct memory access, scrolling is automatic. The interrupt output of the 8275 is used to tell the processor that the bottom of the screen has been reached. At this time the processor can effect a scroll by changing the current pointer in the controller (figure 7). Without any actual character manipulation, the characters on the screen are made to move up by one row. The top row swings around to the bottom. This new bottom row can then be erased. The same locations in memory are used before and after the scroll. Both scrolling up and scrolling down are possible.

A different kind of scrolling is also possible. In this method, the addressed memory space actually does change. If the programmer is dealing with 10 K bytes of text, it could be scrolled one line at a time by moving the direct memory access space down by 80 (for an 80 character per line screen format – see figure 8). The current direct memory access pointer is always at the top of the address space. This is just another form of page changing with most of the screen being common to both pages.

The 8275 is an intelligent controller. As it accesses the data, it examines the incoming characters for special command bytes. When the most significant bit is a one, the controller knows this is a special command. One command outputs one of the 11 built-in characters. Another special command sets or resets six bits corresponding to reverse video, underline, blink,

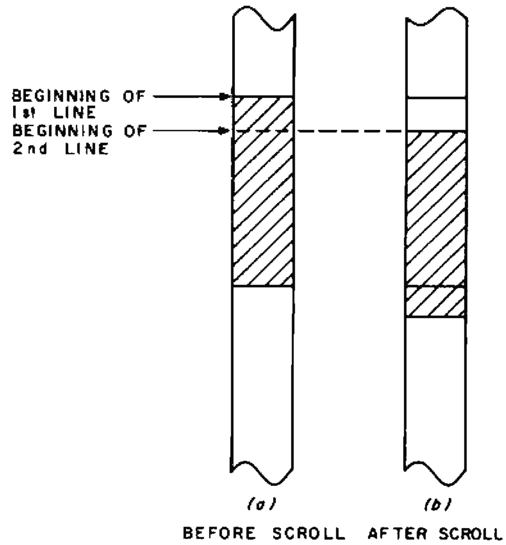

Figure 8: A simplified memory map showing scrolling by moving the pointers to different memory areas which are accessed by the video controller.

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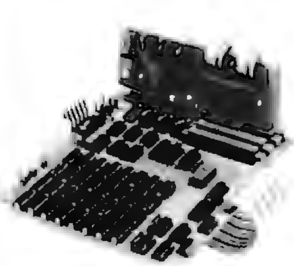

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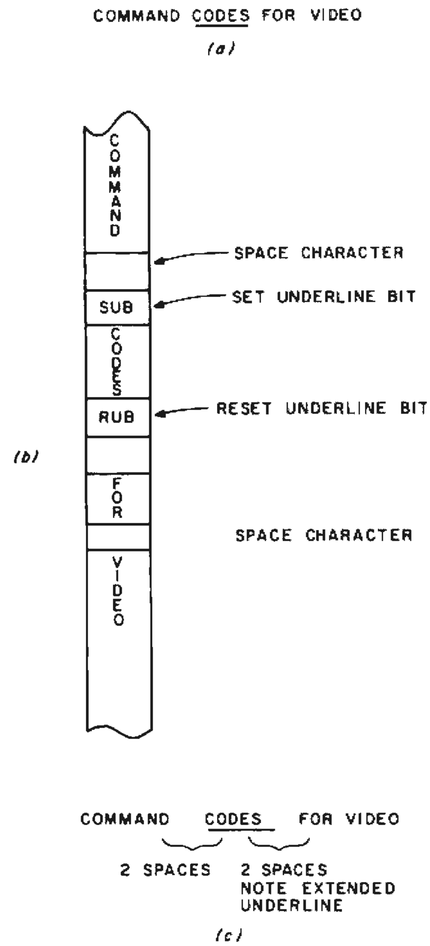

Figure 9: An example of using "invisible" special commands with the video controller. The output shown in figure 9a is what is desired. We wish to underline the five letters in the word "codes". Figure 9b shows a memory map with the special codes inserted in the text. The set underline bit command will command the controller to underline all output until the bit is reset. The reset underline bit command stops the underlining procedure. If the codes were not invisible, the output would probably look like figure 9c. Since the special command codes cannot be converted into printable ASCII characters, spaces are output on the screen. Note the extended underline. This occurs because the reset underline bit command is printed before the bit is actually reset. This visible code mode is not advisable for high quality output.

highlight, and general purpose.

In order to underline five consecutive characters on the screen as in figure 9a for example, the five characters must be preceded by a special command which sets the underline bit (figure 9b). Every character following the command is underlined for the remainder of the screen unless another special command resets the underline bit. Such a command would follow the 5 character word to terminate the underline. Note in figure 9a that the special code does not occupy a character position on the screen. This happens with the 8275 even though the special codes are accessed just like the displayed data. The codes are "invisible." The 8275 can be programmed for either visible or invisible special command codes. Figure 9c is an example of a visible command code.

A different kind of command is end of line. When the 8275 reads this one byte command, it blanks the remainder of the current line by enabling the video suppress output. Thus, after a scroll, the new bottom line need not be erased but only headed by an end of line command. For an 80 character per line format, one write effectively clears the bottom line instead of 80 writes.

The end of screen command is similar to end of line except that the remainder of the screen is blanked instead of just one line. Thus, a clear screen operation consists of one write instead of 2,000. The end of screen command would be placed at the top lefthand corner of the screen.

It has been shown that emulating a simple scrolling terminal is easy with the direct memory access controller and the 8275 video controller. When using a scrolling terminal, one notices the large amount of unused screen space that frequently exists. If the 8275 controller were to access 2,000 characters when, say, only 200 characters were being displayed, the 8275 would be wastefully cutting into processor time. The stop direct memory access commands answer this problem. A short line of print is followed by an end of line, stop direct memory access command, which blanks the remainder of the line and discontinues memory transfer until it is needed for the next line. Variable line lengths are stored in memory, each followed by end of line, stop direct memory access. The end of line, stop direct memory access command allows text to be both stored in compact form and displayed easily. Both kinds of scrolling discussed as well as page changing are simply achieved. The only difference is that variable line lengths are involved.

The last line of nonblank characters can be followed by end of screen, stop direct memory access, which blanks all subsequent lines and terminates the transfer operation. The stop direct memory access commands reduce overhead considerably. The processor experiences not 25 percent delay, but frequently as low as 0 to 10 percent delay due to direct memory access operation. In this way, the direct memory access overhead argument is no longer as strong. Furthermore, much processor time is actually saved by the memory access — page changes, scrolling, and line and screen blanking are all faster, requiring fewer reads and writes. They take less software than most dedicated memory terminals. Also, visual continuity is maintained because no scratches ever appear on the screen during reads and writes.

Interesting results can be obtained by changing some of the device parameters. If the direct memory access controller is programmed to transfer 4 K bytes of memory, but the video controller is only programmed for a 2 K byte screen, the following results occur.

The first scan displays the first 2 K bytes of addressed memory. The vertical retrace occurs and the screen is redrawn. This time, the second 2 K bytes of addressed memory is displayed. Upon the third frame, the first

2 K bytes is once again displayed. A double exposure of the two images effectively occurs. Since each frame is 1/60 second, the refresh of each image is 1/30 second. The human eye senses flicker below approximately 24 frames per second, so no flicker is noticeable. If each frame contained a graph on identical axes, the double exposure would be the superposition of the two graphs. The graphs could be plotted by loading programmable characters into the character generator and displaying them in the proper positions on the screen.

Double exposures would double the memory requirement but have no effect on the data transfer overhead. The video display is still refreshed at the same rate but with alternating images. Triple exposures can also be made. The addressed memory size is three times the screen size. Some flicker would exist since each image is refreshed every 1/20 second.

Superposition of screens cannot be done with ordinary dedicated memory systems. Bit mapped displays can, however, superimpose any number of images without experiencing screen flicker. This can be done by ORing the images together into the same bit map. If involved graphics are intended for a video terminal, the bit map displays are preferred to an 8275 based display.

Interlacing

Ordinary television sets and monitors will interlace the picture if the incoming signal has interlace timing. An interlaced picture has twice as much vertical resolution as a noninterlaced picture. For ordinary television, there are 525 scan lines in an interlaced picture but only 262 lines in a noninterlaced picture. Like so many video terminals, the 8275 unfortunately does not provide interlace timing.

Cost

This topic is a bit unpleasant to the average hobbyist. As of midMarch, 1978, the 8275 was a $100 integrated circuit. If this device is like many others, its price could drop significantly before too long. The direct memory access controller is presently about $28 (it has two spare channels left over for the user's floppy disk and digital cassette too). A character generator runs for $8 to $18. My 2 board system was under $225. All things considered, this is not very expensive when one thinks about the price of terminals with half the features of this one.

A smart way to build this circuit (or anything else that uses expensive components) is to construct the boards first, begin testing the transistor-transistor logic, and last of all buy the 8275. This way, you give the price a chance to come down.

Conclusions

An 8275 based terminal offers the user a large number of features. The useful lifetime of such a terminal is long because of its flexibility. It can bend to meet a wide variety of requirements. Features which are not immediately taken advantage of are always available at a later time.

Features include outputs for reverse video, underlining, blinking, highlighting and general purposes (user defined). A light pen can be used and a cursor is provided. 11 built-in characters are a mixed blessing because of the work involved in decoding them. The character height (line count), the screen format, the retrace timing, the direct memory access burst timing, and the type of cursor to be displayed are programmable.

Upgrading the system is easy because of its programmability. Hence, color can be added without major complications. The controller easily becomes a dual controller for two video monitors.

More and more "minimal systems" that are not so minimal in their power are coming into being. Greater need is arising for a video interface that is small. 10 chip computers with video are possible, and larger single board computers promise great performance for their size when they use the 8275. The price paid for all the features of the 8275 is in direct memory access overhead. The processor is halted for a portion of the time while the screen is refreshed. The end of line, stop direct memory access and end of screen, stop direct memory access commands reduce this overhead, dependent on how full the screen is. The double space mode cuts the overhead in half.

Direct memory access also increases the speed of some operations. Page changing and scrolling are two examples that take almost no processor time. To the user, they appear to be instantaneous operations. Visual continuity is maintained while the processor works in video memory. None of the "scratch" marks characteristic of dedicated memory terminals appear.

Feature for feature, terminals using the 8275 surpass dedicated memory terminals. In text environments with only light graphics requirements, its speed and special attributes make it more attractive than bit-mapped terminals. For many users, a video terminal based on the 8275 video display controller is the optimum choice.■

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Smart Memory, Part 2

Randy C Smith
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Walnut Creek CA 94598

In part 1 the principal processes of an associative memory and processor were described. These include:

- Selection — activating the desired memory words in parallel via their content (addressing by content).
- Alteration — updating all selected words in parallel, with multiwrite.
- Arbitration (Responder Resolution) — methods for reading content serially from potentially more than one responding word.

The second and concluding part of this article reiterates these themes through the use of successive *black box* logic diagrams. No attempt is made to specify exact devices (as in a schematic), since the idea is to illustrate a general architecture. Once the conceptual components are understood (and this is only one of many forms for associative memories) the personal computer enthusiast can experiment with methods for further logic reduction through the use of large scale integration circuits, addition of circuitry for random access or multidimensional addressing, or even the application of more hardware processing power at each memory node.

This concludes our content addressable design discussion. For information about REM, which is a 4 K byte associative memory board for the S-100 bus, contact Semionics at 41 Tunnel Rd Berkeley CA 94705.

See figures following on pages 152 thru 160.

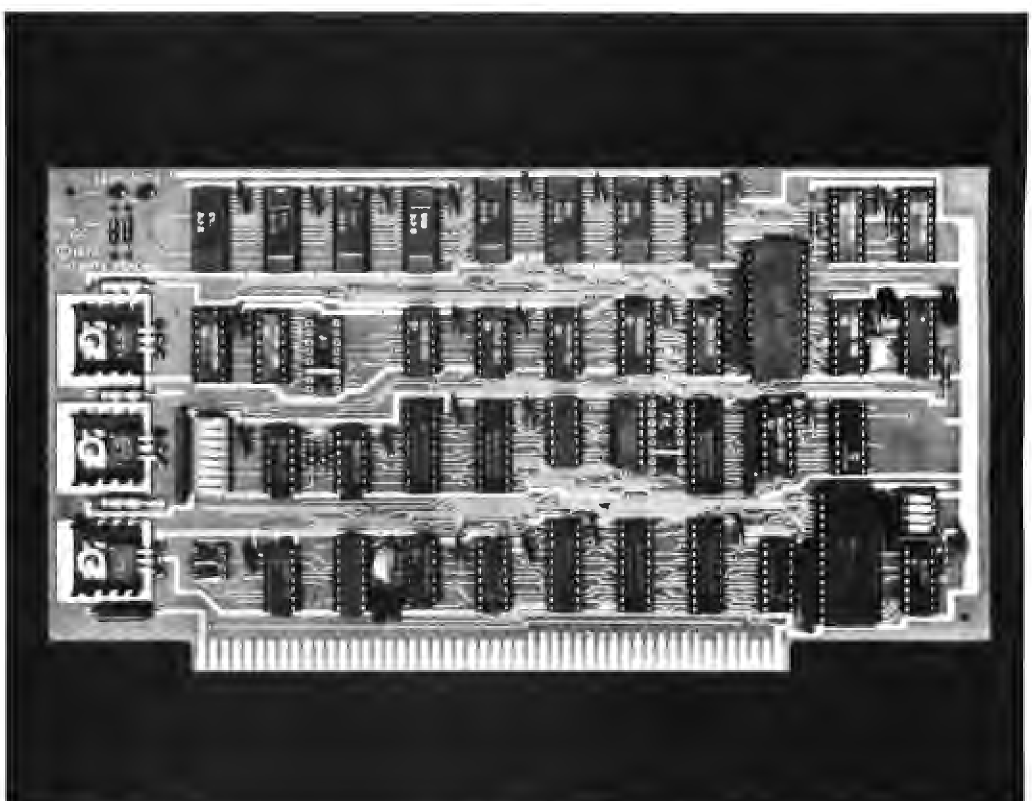

Photo 2: Content addressable memory board for the S-100 bus. The 4 K byte memory board is manufactured by Semionics Associates.

About the Author:

Randy Smith is employed by Semionics Associates as the design engineer for the REM S-100 board and is the coinventor of REM. His personal interests include artificial intelligence research, especially language comprehension.

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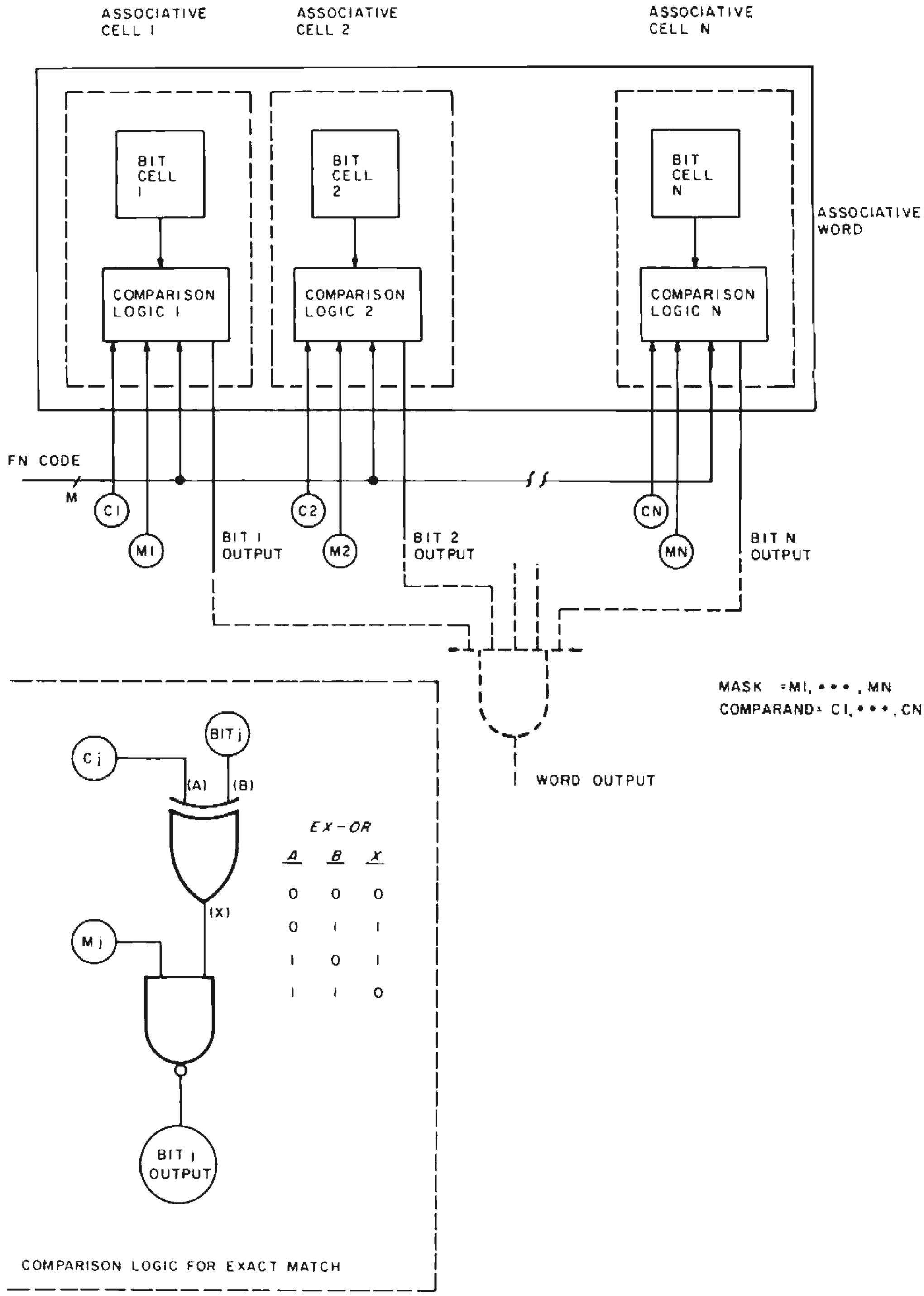


Note: The numbering of figures, photos and tables is continued from part 1 in April 1979 BYTE, page 54.

Figure 4: Word parallel associative memory. Each cell of the word contains logic to compare its contents with the respective bit of the comparand broadcast from the central processor. The type of comparison selected by the FNCODE is generally only exact match (=) for this architecture. The result of the comparison for each bit is placed on the output line, and the separate bit results are combined by external logic into the result for the entire word. For exact match, the output lines need merely be ANDed. If the outputs are open collector, this can be implemented without a gate by tying the outputs together through an appropriate pull-up resistor. An N bit mask is applied to the associative cells so comparison on only part of the word (where the mask = 1) is possible. The inset shows how the comparison logic box could be implemented for exact match. The word read and write logic is omitted for simplicity.

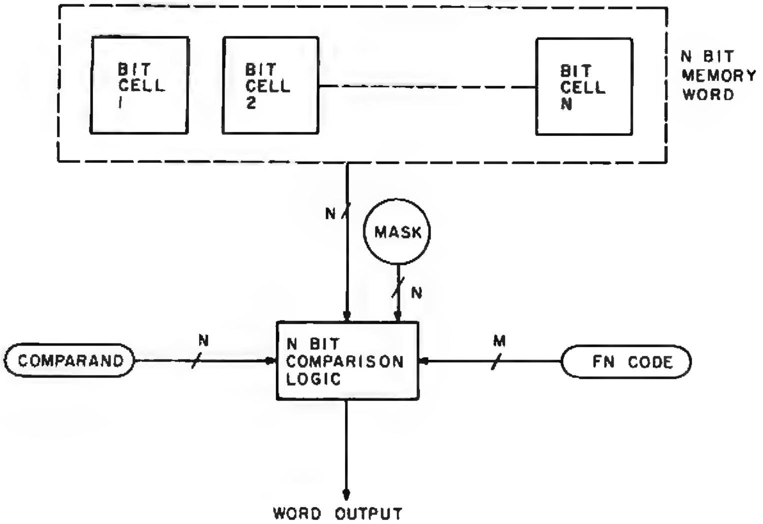


Figure 5: Word parallel associative memory with external word logic for comparisons. By placing the comparison logic external to the memory word, the need for special memory cells is removed, and the memory word may be an ordinary, available, and cheap random access type. The N bit comparison logic can be built in the form of available integrated circuit comparators. Magnitude comparisons like word > comparand (>), or word < comparand (<), etc. are now readily included with exact match in the associative function set.

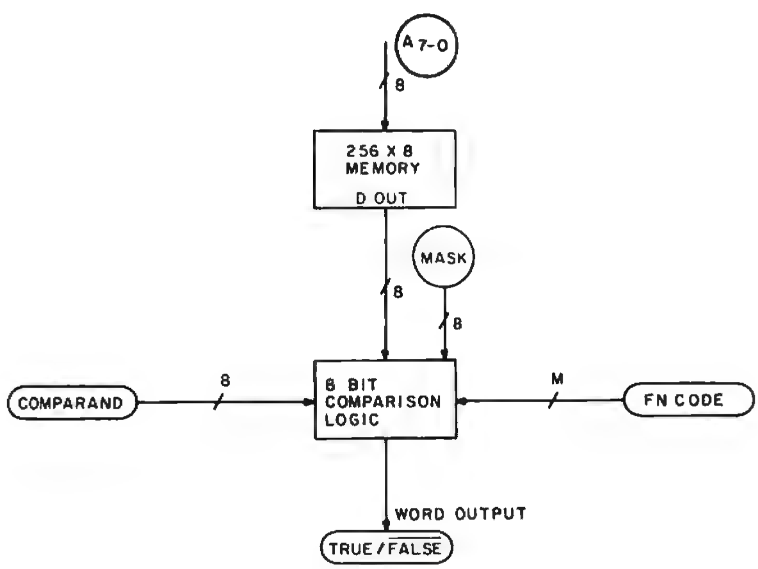


Figure 6: Block oriented comparison logic: byte serial, block parallel. A further savings in associative logic can be realized by sharing the logic over a block of memory words. By choosing the block size judiciously, it is possible to use existing programmable memory circuits. Information in the block will be considered as a unit (eg: a personnel record for one individual) and all blocks (rather than all words) in the system will be treated in parallel. For the rest of this article, the figures will illustrate conceptual architectures for a microcomputer add-in associative memory subsystem. Therefore, the word size will be eight bits. The block size is chosen as 256 words by eight bits so it can hold enough related character information. For textual information, one ASCII character will occupy one byte. Since our processor can send only one byte of comparand to the memory at a time, eight bits of low address (A_7 thru A_0) will select the one of 256 bytes of all blocks to be compared. This offset address can be kept conveniently in an 8 bit register and incremented or changed when necessary.

CLK	$\overline{PR}$	J	$\overline{K}$	Q
X	L	X	X	H
↑	H	L	H	Q_0
↑	H	L	L	L

Table 2: Partial function table of a J-$\overline{K}$ flip flop.

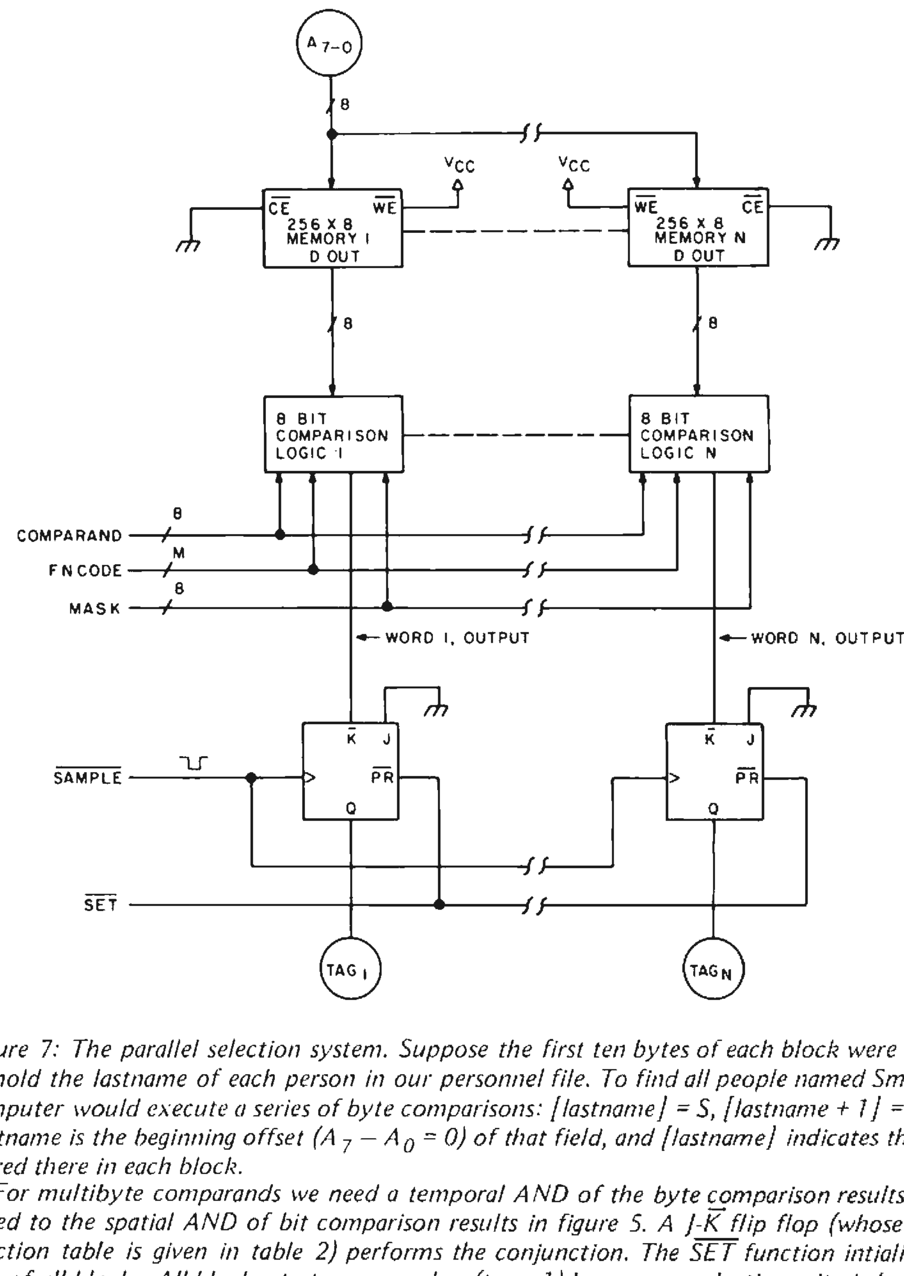


Figure 7: The parallel selection system. Suppose the first ten bytes of each block were defined to hold the lastname of each person in our personnel file. To find all people named Smith, the computer would execute a series of byte comparisons: [lastname] = S, [lastname + 1] = M, etc. Lastname is the beginning offset ($A_7 - A_0 = 0$) of that field, and [lastname] indicates the value stored there in each block.

For multibyte comparands we need a temporal AND of the byte comparison results, as opposed to the spatial AND of bit comparison results in figure 5. A J-$\overline{K}$ flip flop (whose partial function table is given in table 2) performs the conjunction. The $\overline{SET}$ function intializes the tags of all blocks. All blocks start as responders (tag = 1) because no selection criteria have been imposed. Subsequent restrictions cause those blocks that do not meet all specifications to turn their tags off — and they remain discarded until a new $\overline{SET}$ command is issued.

Therefore, at the end of the comparison or selection process, that subset of blocks whose tags are still on have met all the requirements. The $\overline{SAMPLE}$ line clocks the flip flops only during an associative compare function, and at the time when the comparison logic result becomes valid. All blocks respond to the comparison simultaneously, and as shown at this level of the design, can only read out their data for comparison purposes.

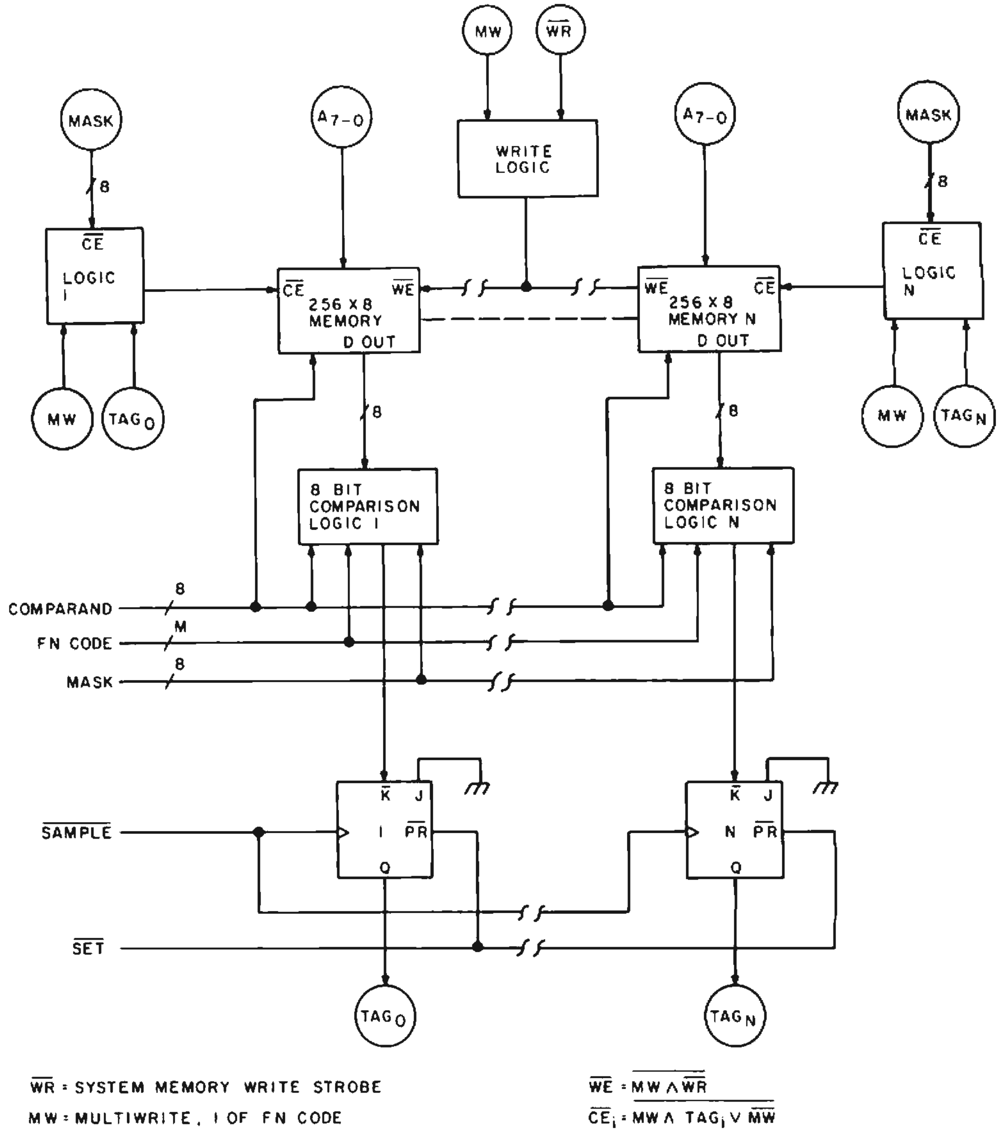


Figure 8: Parallel processing in place: the multiwrite function. New logic black boxes have been added to the CE (chip enable) and the WE (write enable) inputs of our memory blocks to turn them into CAPPS (content addressable parallel processors), which Foster (see bibliography, part 1) has defined as associative memories with parallel write ability. Without recourse to address, we can change the contents of any previously selected blocks, whose tags are 1. When the multiwrite responders command is executed, only the chip enables of those blocks whose tags are on are activated. The write enable is also activated during multiwrite. The value of the addressed byte in all selected blocks is changed to the contents of the comparand bus. The tags are unaffected (no SAMPLE signal is present). Without knowing the addresses of the blocks in our selected subset, we are able to change their contents in place. Notice this change can be common data (mark all engineers in our file for a \$100 bonus) or specific (show 550 parts on hand for stock item #36574).

Access Type	Address A_{15} thru A_{12}	A_{11} thru A_8	A_7 thru A_0	Resulting Access Type
MEM WRITE	Hole other	FNCODE <address>	OFFSET	1 of 16 associative functions. Random access memory write.
MEM READ	<16 bit address>			Random access memory read; any memory in hole space must be read only.

Derivation of Associative Commands

A_{15} thru A_{12}	A_{11} thru A_8	A_7 thru A_0
HOLE	FNCODE	OFFSET

(Address during an associative command.)

Table 3: A clarification of the random access and associative operation definitions.

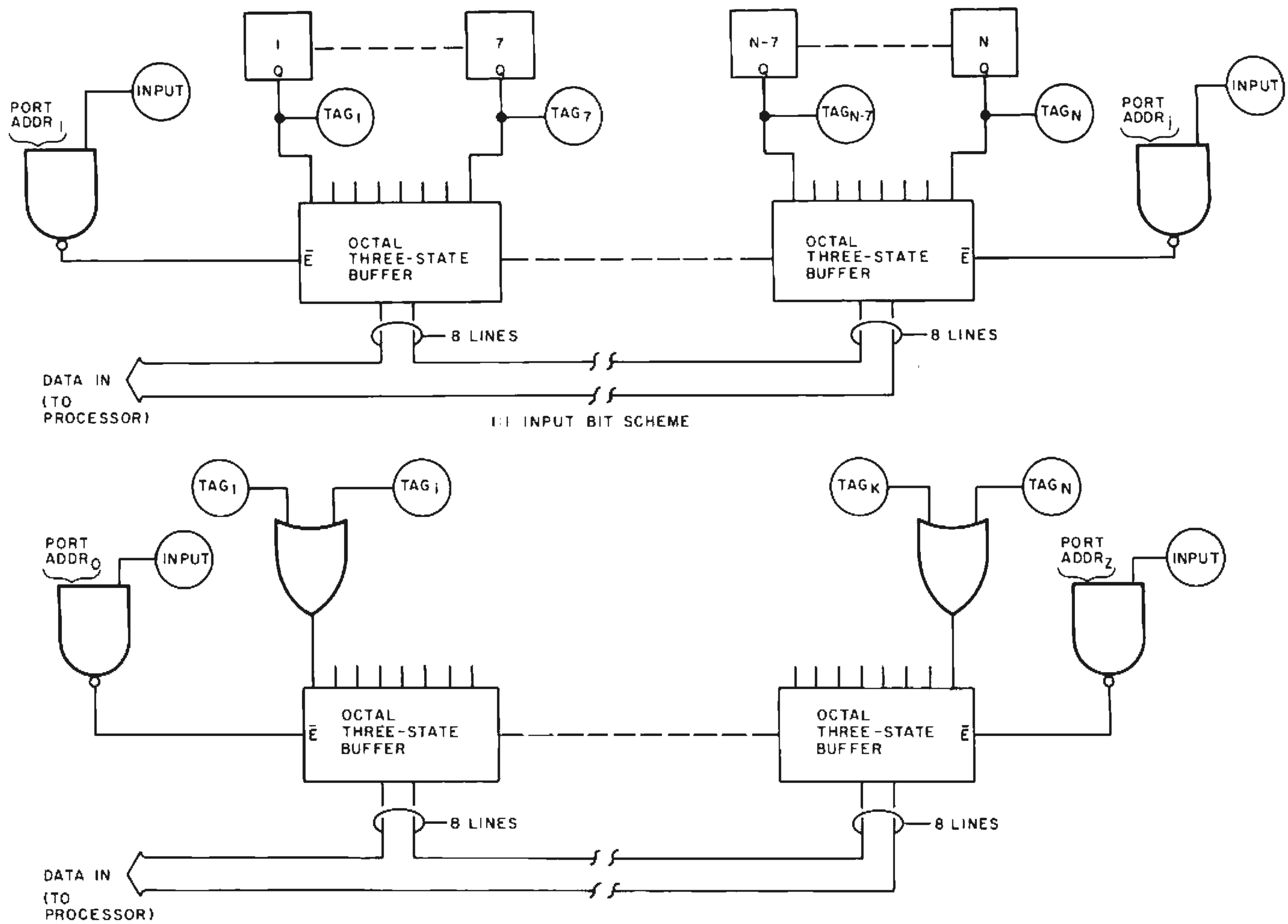
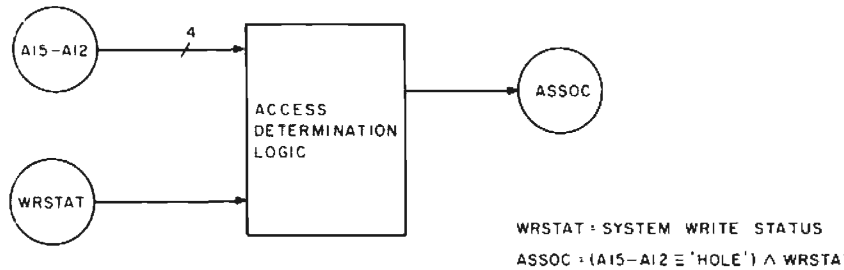
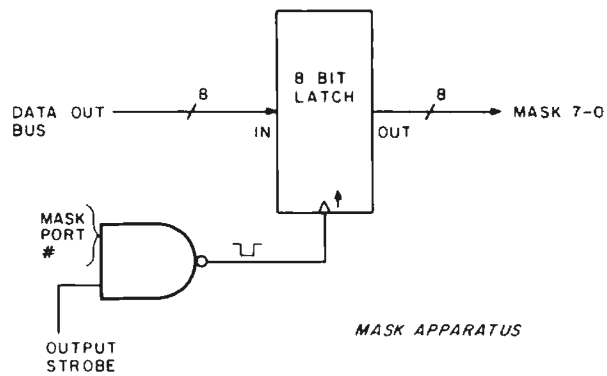


Figure 9: Nonassociative read responder techniques. In part 1 an associative technique was described to read the contents of responders (without addresses) when there were more than one. It consists of a daisy chain connecting all the tags in the memory into a priority list. During an associative read, only the highest priority responder (the first responder) could place its contents on the bus to the processor. A companion function, next, to turn off the first responder, and the query function to determine if there are any more responders, completed the description of necessary hardware. Implementing these priority chains would require at least three more different logic gates per memory word and, although fast (and address free), the design becomes rather bulky.

When a random access address structure is placed on the memory words (as it usually is to facilitate loading and unloading of the memory), a nonassociative technique for reading responders is available. The responders may be read serially by taking advantage of their address structure. The tags of all blocks from least to highest in address may be sent in batches to the central processor through input ports. The processor can then scan the tags in sequence for the next (or first) responder, and quickly derive the responding block's address in preparation for a random access read. The tag input ports could also be arranged hierarchically, to speed search in cases where there are likely to be few responding words. Alternatively, all responders could first multiwrite a 1 into a reserved flag bit in their memory block. Groups of tags could be ORed and the results for many groups sent to the processor through input ports. Finding a 1 in any bit of the input word tells the processor the group of blocks to search. A random access, serial scan of the flag bit for each block in that group determines exactly which one (or more) responded. A random access read then fetches the information desired. The query function, here, simply entails reading and testing the input words.



DETERMINATION OF ASSOCIATIVE ACCESS REQUEST



MASK APPARATUS

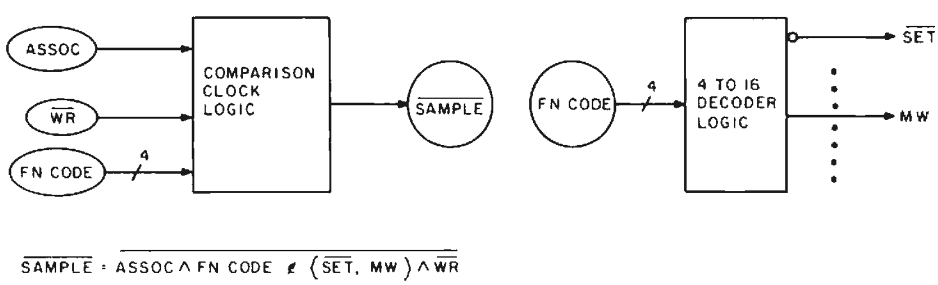


Figure 10: Accessing the add-in associative memory. Only eight address bits (A_7 thru A_0) are used for associative memory accesses. Therefore, eight bits (A_{15} thru A_8) are left to specify whether a memory access represents an associative access, and, if so, which function is involved. Let A_{11} thru A_8 be the FNCODE (one of 16 functions) during an associative instruction. Comparison and multiwrite instructions need data supplied by the central processor. For these operations, the processor must execute a memory write. If the nonassociative (random access) technique for reading responders is used, all associative functions may be initiated by a processor memory write cycle. To distinguish between random access and associative operations, a 4 K byte "hole" is defined at some arbitrary 4 K boundary of address space. In general, a memory write to the hole indicates an associative function specified by A_{11} thru A_8. A read of any byte in the hole is considered normal random access (although memory, if present, must be read only). Table 3 clarifies the definition of random access and associative operations. Figure 10 also illustrates the derivation of the mask and other signals used in previous diagrams. The mask, for example, can be implemented by a simple 8 bit output port. ■

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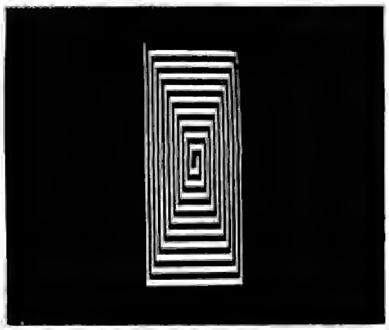
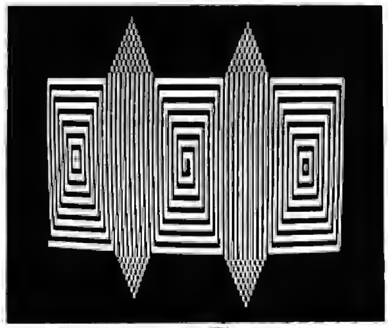
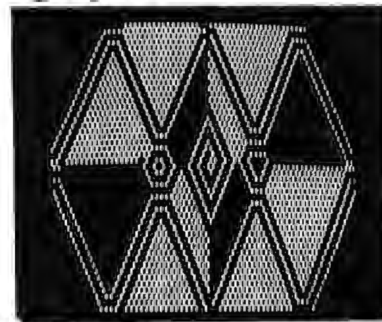

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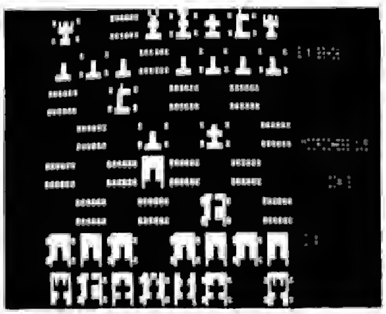
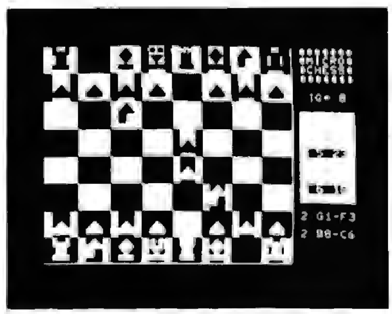
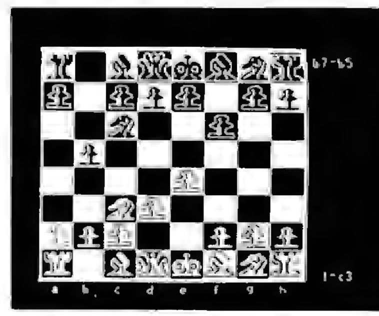

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Simultaneous Input and Output for Your 8080

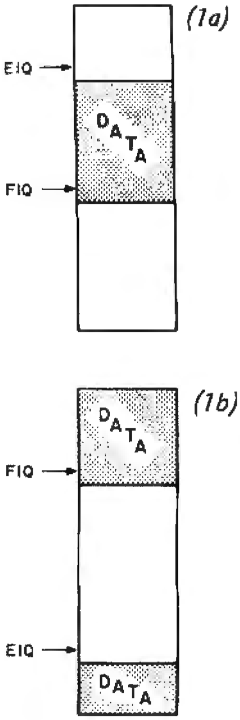

Figure 1: The "wrap-around" queue. The queue is a method for storing data in the form of a list: the first item into the list becomes the first out of the list, in the same manner as a waiting line of people at a supermarket checkout counter. Figure 1a shows the data for an input queue in memory with two pointers, FIQ (front of input queue) and EIQ (end of input queue). When an item is added to the end of the queue, EIQ is incremented by 1. In removing an item from the queue, FIQ is incremented by one. Note that the queue is "upside-down" here; that is, the end of the queue is on top. When the top of the array in memory is reached, EIQ is altered so it points to the bottom of the array, thus "wrapping" the queue around the array as in figure 1b. Notice also that pointer EIQ points to the location that is one beyond the end of the queue. This enables the program to detect an empty or full array when EIQ = FIQ.

The process of I/O (input/output) in assembly language on a typical microcomputer system is rather crude. You input the status register and perform a logical AND with a mask consisting of one bit. If the result is not zero, you know the bit was on and the I/O device was therefore ready. In that case, you either input or output the data register, as appropriate. Otherwise, you loop back to input the status register again. On the 8080, it goes like this:

```
                Input

ILOOP:   IN     ISTAT
         ANI    IREADY
         JZ     ILOOP
         IN     IDATA

                Output

OLOOP:   IN     OSTAT
         ANI    OREADY
         JZ     OLOOP
         OUT    ODATA
```

where the quantities ISTAT, IDATA, OSTAT, ODATA, IREADY, and OREADY are what is called, in the world of big computers, "installation-dependent" (that is, they differ from one person's 8080 to another). The first four of these might be given by:

```
ISTAT    EQU  3
IDATA    EQU  2
OSTAT    EQU  3
ODATA    EQU  2
```

describing a single channel for both input and output involving two ports, with port numbers 3 and 2. The other two might be given as:

```
IREADY  EQU  1
OREADY  EQU  2
```

to denote that the rightmost bit of the status register is the input-ready flag and the second bit from the right in this register is the output-ready flag. (Your dealer must supply you with these values, or show you how to find what they are, when you buy your system.) You can also make these into subroutines by adding a return as follows:

```
INPUT:   IN     ISTAT
         ANI    IREADY
         JZ     INPUT
         IN     IDATA
         RET

OUTPUT:  IN     OSTAT
         ANI    OREADY
         JZ     OUTPUT
         OUT    ODATA
         RET
```

This allows you to CALL INPUT to bring a newly input character into register A, or to CALL OUTPUT whenever you have a new character in register A that you want to put out.

The trouble with this kind of I/O is that it is not simultaneous. When you are doing input, that is all you are doing; when you are doing output, that is all you are doing. Meanwhile, your system is sitting uselessly in a loop, which it is performing several thousands of times, or sometimes (particularly in the case of input) several *millions* of times. What you need in order to increase the efficiency of your system, if you have 190 bytes of read only memory and 65 bytes of programmable memory to spare, is a simultaneous I/O package which allows you to do input, processing, and output, all at the same time.

The basic idea of simultaneous I/O is that of the *queue*. Any queue can be considered by analogy to a waiting line for a bus. (The story, told to this author second or third hand, is that in England people line up for buses in lines that look like spirals or, more

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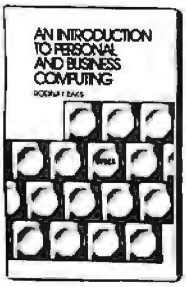

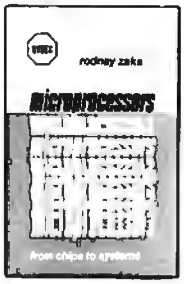

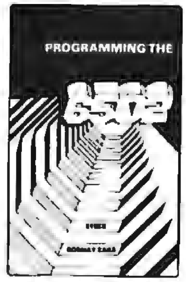

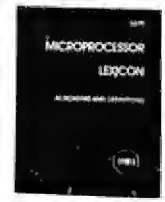

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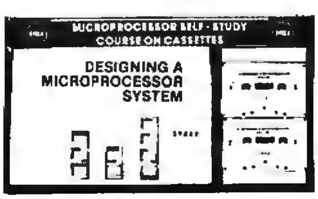

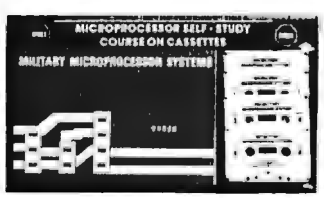

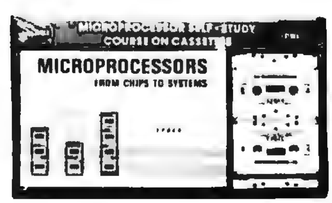

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informally, like the tail of a pig — a shape that is in turn called *queue* in French, presumably because it looks vaguely like the letter Q.) Consider the characters waiting for the bus as ASCII characters, rather than as local town characters, and consider the bus *not* as a bus in the technical sense, but (for output) as the actual output device — the teletypewriter video display terminal, Selectric terminal, or whatever. When your routine wants to output a character, this character goes on the end of the queue. It then has to wait for a while until the characters in front of it, which were entered earlier, get on the bus — that is, until they are actually output — before it can be output.

The analogy with the bus is not a perfect one, because a real bus, when it comes along, takes everybody waiting for it all at once. A waiting line in a supermarket at the checkout counter would be a better analogy, because characters, like shoppers, leave the queue one at a time, as well as entering it one at a time.

For input, there is another queue, but this time the input device feeds new characters onto the *end* of the waiting line, and they come off the front — that is, board the bus — when they are actually used by the program which is asking for input. Several characters might be typed before they were actually used by the program, presumably because it is doing something else, such as a long computation. For output, the use of the queue is more common, because programs typically produce output characters much faster than they can actually be put out; these characters enter the queue and are then output from it, one at a time,

```
IP:     PUSH H       ; SAVE HL REGISTER
        LHLD FIQ     ; FRONT OF INPUT Q TO HL
        LDA EIQ      ; END OF INPUT Q (LO) TO A
        CMP L        ; COMPARE FIQ(LO):EIQ(LO)
        JNZ IP3      ; IF UNEQUAL, Q NONEMPTY
IP2:    CALL OPOLL   ; Q EMPTY. TIGHT LOOP
        CALL IPOLL   ; (KEEP POLLING I AND O)
        JNC IP2      ; (UNTIL IN CHAR. RECEIVED)
IP3:    MOV A,M      ; FIRST IN Q CHAR. TO A
        PUSH PSW     ; SAVE THIS CHARACTER
        INX H        ; UPDATE FRONT OF INPUT Q
        MVI A,TIQ    ; WRAPAROUND TEST (COMPARE
        CMP L        ;  FIQ(LO) AND TOP OF IN Q
        JNZ IP4      ;  (LO) -- IF =, RESET TO
        MVI L,BIQ    ;  BOTTOM OF IN Q (LO)
IP4:    SHLD FIQ     ; PUT FIQ BACK IN MEMORY
        POP PSW      ; RESTORE INPUT CHARACTER
        POP H        ; RESTORE HL REGISTER
        RET          ; OUT OF THIS ROUTINE
```

Listing 1: Subroutine IP, written in 8080 assembler language and called when the user's program wants an input character. IP returns that character in the A register.

while the computer goes on to whatever it has to do next.

Before we discuss how a queue like this is actually implemented, let us digress a bit and answer one fundamental question: how are we to handle three programs going simultaneously — an input program, an output program, and something else which is reading input and writing output? There are two ways, one being the use of interrupts, the other making use of a technique called *polling*. We shall use polling, mainly because it does not require any special hardware (not all 8080 systems have a priority interrupt control unit) and also allows the user who might not have written his own monitor to use simultaneous I/O without interfering with any interrupt conventions which his monitor might have established.

Polling, in this case, assumes that the functions of watching the input device and the output device to see if they are ready, and taking appropriate action when they are ready, are *subroutines* of the user's program. We shall call them IPOLL and OPOLL. They are *not* to be confused with the ordinary I/O subroutines which supply input to the user's program and accept output from it; we shall call these IP and OP. To summarize the functions of our four routines:

(1) IP is called when the user's program wants an input character, and IP returns with that character in register A.
(2) OP is called when the user's program has a character to be output, and this character must be in register A when OP is called.
(3) IPOLL is called every so often (in a sense to be described more precisely below) to check whether the user has keyed in a new character that has to be placed on the end of the input queue.
(4) OPOLL is called every so often to check whether the output device has completed its processing of the previous character to be output; if it has, the next one is sent out.

IPOLL and OPOLL are called both from IP and OP and from the user's program. When they are called from IP and OP, they employ an additional feature, not discussed above. IPOLL returns with the carry set if a new character is placed on the input queue, and clear otherwise. OPOLL returns with the carry set if a new character was removed from the output queue and put out, and clear otherwise. This information is used by IP and OP, but it is not needed by the user program. In fact, for the user program, there is no need to distinguish between the func-

tions of calling IPOLL and calling OPOLL. It is enough to have a single subroutine, POLL, whose only function is to call IPOLL and OPOLL and then return; the subroutine POLL can then be called by the user program.

How often must the user program call the subroutine POLL? The answer is that the user program must be so organized that there is never a significant amount of real time during which POLL is not called. (How to ensure this will be described below.) The reason, of course, is that if this is not so, we could have the bad luck to push an input key during such a period of real time, and then, since POLL was not called, that input character will never be placed on the input queue and will therefore never be seen by the user's program. (Remember Murphy's law: if anything can go wrong, it will.)

On output, the situation is not that bad, but if there were a significant amount of time during which POLL was not called, the output device would effectively be stopped during that period of time. If this were a recurrent phenomenon, you would see the output device starting and stopping in jerks, like a car that loses power.

The easiest way to call POLL often enough from the user's program is to call POLL once in every loop and at least once in every subroutine. (If there is a subroutine call instruction in a loop, we do not need to call POLL explicitly in that loop, since POLL will be called by the called subroutine.) Or, for a more explicitly stated method, call POLL just before every return instruction and at every labeled instruction to which there is a backward jump. (That is, if the label is ALPHA, then somewhere *later* in the program there must be a jump to ALPHA.)

```
OP:     PUSH PSW    ; SAVE A-REGISTER
        PUSH H      ; SAVE HL-REGISTER
        LHLD EOQ    ; END OF OUTPUT Q
        MOV M,A     ; PUT CHAR. ON END OF Q
        INX H       ; UPDATE END OF OUTPUT Q
        MVI A,TOQ   ; WRAPAROUND TEST (COMPARE
        CMP L       ;  EOQ(LO) AND TOP OF OUT Q
        JNZ OP2     ;  (LO) -- IF =, RESET TO
        MVI L,BOQ   ;  BOTTOM OF OUT Q (LO))
OP2:    LDA FOQ     ; FRONT OF OUTPUT Q (LO)
        CMP L       ;  TO A -- IF = EOQ (LO)
        JNZ OP4     ;  AFTER INCR., Q FULL
OP3:    CALL IPOLL  ; Q FULL. TIGHT LOOP
        CALL OPOLL  ; (KEEP POLLING I AND O)
        JNC OP3     ; (UNTIL SMALLER OUT Q)
OP4:    SHLD EOQ    ; PUT EOQ BACK IN MEMORY
        CALL OPOLL  ; MAKE SURE OPOLL AND IPOLL
        CALL IPOLL  ;  ARE CALLED AT LEAST ONCE
        POP H       ; RESTORE HL-REGISTER
        POP PSW     ; RESTORE A-REGISTER
        RET         ; OUT OF THIS ROUTINE
```

Listing 2: Subroutine OP, called when the user's program has a character to be output. This character must be in the A register when OP is called.

This insures that POLL will be called often enough. *[In a system with a real time clock, calling POLL from the interrupt handler for the clock every few milliseconds will accomplish the same end . . . .* **CH***]*

We now discuss the way in which we implement a queue in memory, namely as a "wraparound array." We start with an array IQ (input queue) of characters, together with two 16 bit pointers, or variables whose values are addresses, called FIQ (front of input queue) and EIQ (end of input queue). Figure 1 shows a typical configuration of the input queue. The shaded area shows the characters that are actually in the queue; the unshaded area shows the rest of the array in memory. To take a character off the front of the queue, assuming that FIQ is in register pair HL (which we can bring about by doing LHLD FIQ), we get the character to which FIQ points (by doing MOV A,M) and then increase FIQ by one (by doing INX H). To put a character on the end of the queue, assuming that EIQ is in the HL register pair (by means of LHLD EIQ), we move it to memory at the place where EIQ points (by doing MOV M,A – assuming that the new character is in the A register) and then increase EIQ by one (by doing INX H). Note that, in a sense, the queue is "upside-down" – the end of the queue is on top. If it were "right-side-up" we would have to decrease FIQ and EIQ by one in the above processes (by doing DCX H), rather than increasing them by one. Of course, after either decreasing or increasing, we must put FIQ (or, respectively, EIQ) back in memory (by doing SHLD FIQ or SHLD EIQ).

Of course, we cannot keep increasing FIQ and EIQ forever. Eventually, in figure 1a, EIQ will get to the top of the array in memory. When this happens, we alter it to point to the *bottom* of this array (this is the "wraparound" feature). After a while, the situation looks like figure 1b. Here again, the shaded area represents the characters actually in the queue. The first one is where FIQ points, the next one is right above that, and so on up to the top of the array; then we start at the bottom of the array, and so on up to where EIQ points. We are treating the array as if it were cyclical, and, in fact, on big computers, this setup is often known as a "circular array" or a "ring buffer."

We note that FIQ points to the first character in the queue, but EIQ does *not* point to the last character in the queue – it points to the position one beyond the last character. To see why this is so, suppose the queue has exactly one character in it. We do not want FIQ and EIQ to be the same, because we want that to happen only when the queue is empty – when there are *no* characters in it – or else when it is entirely full

(since these are the two cases in which special action has to be taken). By adopting the convention illustrated in figure 1, both of these conditions can be sensed by testing for FIQ = EIQ. Of course, the entire setup of figure 1 has to be duplicated for the output queue OQ and its two associated pointers FOQ and EOQ.

Let us make the simplifying assumption that each queue is entirely within one 256 byte page (from hexadecimal addresses xx00 through xxFF for some hexadecimal value of xx). This means that we can compare register pair HL with the address of the top of a queue by simply comparing register L with the low-order eight bits of this address. On equality, we set register L only (register H does not change) to the low-order eight bits of the address of the bottom of the queue. Here the top and the bottom refer to the array in memory, and are distinct from the front and the end as discussed above.

What happens when our queues get full? First of all, let us discuss how big we want the queues to be. The two queues and the four addresses FIQ, EIQ, FOQ, and EOQ must of course be in programmable memory, while the four routines IP, OP, IPOLL, and OPOLL can be in read only memory. So to a certain extent it depends on how much programmable memory is available in your system. An input queue of n characters allows you to type n characters ahead of where the program is at any given moment; an output queue of n characters allows your program to put out n more characters than have actually been output yet by the output device at any given moment. While the device is outputting these n characters, your system can be doing something else simultaneously. There is no reason for the input and the output queues to be the same size, and in a typical application you might be using 10 characters in the input queue and 55 characters in the output queue. A bit of experimentation here will satisfy you as to what is comfortable for your application.

When the output queue gets full, it means that the capacity of the queue for temporarily saving output characters has been used up. In that case we simply go back to what we used to do before we had simultaneous I/O — that is, wait for a character to be actually put out before we do anything else. Whenever the user's program puts a new character into the output queue, we perform our incrementation, as discussed above, and then check to see if the output queue is full (FOQ = EOQ). In that case, we go into a loop, calling IPOLL and OPOLL until OPOLL returns with the carry set. This indicates that OPOLL sensed output ready and put out a character — an operation that reduces the size of the output queue. The result is that, when we *enter* the output routine OP, the output queue will never be full, and, if FOQ = EOQ, we know that the output queue is not full but empty.

When the input queue becomes full, we are typing too fast. Any further characters which we type will not be read by the user's program. The only thing we can do in this case is to give the user a warning that this has happened, so that he will retype the characters involved. Fortunately we can do this easily, with most output devices, by putting out a control-G (hexadecimal 07, or on some output devices 87) which will either ring a bell or put out a high-pitched beep. A variation on this system, which we use, involves putting out the control-G when the output queue is *almost* full (let us say, seven or fewer spaces remaining) so that the last few characters do not have to be retyped; the user simply stops typing for a while and waits for a decent interval.

A minor technical point: We cannot sound the bell simply by calling OP. Recall that calling OP simply puts a character on the output queue; it may be a second or longer before that character is actually put out. When we type a character that has to be retyped, however, we need an immediate indication of this fact. We therefore use a single-byte input alarm counter IAC which is normally zero. To specify a bell as above, we simply increment IAC

```
IPOLL:    IN ISTAT     ; GET STATUS BITS (IN)
          ANI IREADY   ; READY BIT ZERO MEANS
          RZ           ;  NOTHING TYPED - OUT
          PUSH H       ; SOMETHING TYPED - SAVE
          IN IDATA     ;  HL REG. AND INPUT IT
          LHLD EIQ     ; END OF INPUT Q TO HL
          MOV M,A      ; PUT CHAR. ON END OF Q
          INX H        ; UPDATE END OF INPUT Q
          MVI A,TIQ    ; WRAPAROUND TEST (COMPARE
          CMP L        ;  EIQ(LO) AND TOP OF IN Q
          JNZ IPOLL2   ;  (LO) -- IF =, RESET TO
          MVI L,BIQ    ;  BOTTOM OF IN Q (LO))
IPOLL2:   LDA FIQ      ; FRONT OF INPUT Q (LO)
          SUB L        ;  TO A -- IF = EIQ (LO)
          JZ IPOLL3    ;  AFTER INCR., Q FULL
          SHLD EIQ     ; NOT FULL. RESTORE EIQ
IPOLL3:   JNC IPOLL4   ; IF FIQ-EIQ IS NEGATIVE,
          ADI LIQ      ;  ADD SIZE OF INPUT Q
IPOLL4:   CPI IFUDGE   ; TEST IN Q WITHIN FUDGE
          JNC IPOLL7   ;  FACTOR (7) OF BEING
          LXI H,IAC    ;  FULL. IF SO, BUMP INPUT
          INR M        ;  ALARM COUNTER BY 1
IPOLL7:   POP H        ; RESTORE HL REGISTER
          STC          ; SET CARRY (CHAR. THERE)
          RET          ; OUT OF THIS ROUTINE
```

Listing 3: Subroutine IPOLL, called periodically to check whether the user has keyed in a new character that has to be placed at the end of the input queue.

```
OPOLL:    IN OSTAT     ; GET STATUS BITS (OUT)
          ANI OREADY   ; READY BIT ZERO MEANS
          RZ           ;  PORT STILL BUSY - OUT
          LDA IAC      ; GET INPUT ALARM COUNTER
          DCR A        ; AND DECREASE IT BY 1
          JM OPOLL1    ; IF WAS ZERO, NO ALARM
          STA IAC      ; STORE DECREASED VALUE
          MVI A,CTRLG  ; CONTROL-G (BELL) TO A
          OUT ODATA    ; OUTPUT (TYPING TOO FAST,
          RET          ;  ALARM) AND EXIT
OPOLL1:   PUSH H       ; SAVE HL REGISTER
          LHLD FOQ     ; FRONT OF OUTPUT Q TO HL
          LDA EOQ      ; END OF OUT Q (LO) TO A
          CMP L        ; COMPARE FOQ(LO):EOQ(LO)
          JZ OPOLL7    ; IF EQUAL, NOTHING IN Q
          MOV A,M      ; GET FIRST THING IN Q
          OUT ODATA    ;  AND PUT IT OUT
          INX H        ; UPDATE FRONT OF OUTPUT Q
          MVI A,TOQ    ; WRAPAROUND TEST (COMPARE
          CMP L        ;  FOQ (LO) AND TOP OF OUT
          JNZ OPOLL5   ;  Q(LO) -- IF =, RESET TO
          MVI L,BOQ    ;  BOTTOM OF OUT Q (LO))
OPOLL5:   SHLD FOQ     ; PUT FOQ BACK IN MEMORY
OPOLL7:   POP H        ; RESTORE HL REGISTER
          STC          ; SET CARRY (WORK DONE)
          RET          ; OUT OF THIS ROUTINE
```

Listing 4: Subroutine OPOLL, called periodically to check whether the output device has completed its processing of the previous character to be output. If it has, the next character is sent out.

```
FIQ: DS 2              ; FRONT OF INPUT Q (2 BYTES)
EIQ: DS 2              ; END OF INPUT Q (2 BYTES)
FOQ: DS 2              ; FRONT OF OUTPUT Q (2 BYTES)
EOQ: DS 2              ; END OF OUTPUT Q (2 BYTES)
IAC: DS 1              ; INPUT ALARM COUNTER (1 BYTE)
LIQ EQU 36             ; LENGTH OF INPUT Q
LOQ EQU 36             ; LENGTH OF OUTPUT Q
IQ:  DS LIQ            ; INPUT Q (SINGLE PAGE)
OQ:  DS LOQ            ; OUTPUT Q (SINGLE PAGE)
BIQ EQU IQ MOD 256     ; BOTTOM OF INPUT Q (LO)
BOQ EQU OQ MOD 256     ; BOTTOM OF OUTPUT Q (LO)
TIQ EQU BIQ+LIQ        ; TOP OF INPUT Q (LO)
TOQ EQU BOQ+LOQ        ; TOP OF OUTPUT Q (LO)
ISTAT EQU 3            ; INPUT STATUS PORT
OSTAT EQU 3            ; OUTPUT STATUS PORT
IDATA EQU 2            ; INPUT DATA PORT
ODATA EQU 2            ; OUTPUT DATA PORT
IREADY EQU 2           ; MASK FOR INPUT READY
OREADY EQU 1           ; MASK FOR OUTPUT READY
CTRLG EQU 7            ; CONTROL-G (SOMETIMES 87H)
IFUDGE EQU 7           ; INPUT FUDGE FACTOR
```

Listing 5: Suggested data definitions.

```
INIT: LXI H,IQ     ; BOTTOM OF INPUT Q IS
      SHLD FIQ     ;  INITIAL VALUE OF FRONT
      SHLD EIQ     ;  AND END OF INPUT Q
      LXI H,OQ     ; BOTTOM OF OUTPUT Q IS
      SHLD FOQ     ;  INITIAL VALUE OF FRONT
      SHLD EOQ     ;  AND END OF OUTPUT Q
      XRA A        ; ZERO IS INITIAL VALUE
      STA IAC      ;  OF INPUT ALARM COUNTER
```

Listing 6: Initialization of the system.

by one, and then OPOLL checks IAC before it does anything else (if the output device is ready) and outputs a bell if IAC does not equal 0, decrementing IAC by one as it does so.

The complete code for IP, OP, IPOLL, and OPOLL is given in listings 1 through 4, with the data definitions given in listing 5 and the initialization given in listing 6. To summarize the steps needed in order to use the system:

(1) Include in your program (kept in either read only memory or programmable memory) the subroutines given in listings 1, 2, 3, and 4.

(2) Include as part of the initialization of your main program the initialization steps given in listing 6.

(3) Include as part of your data (kept in programmable memory) the data definitions of listing 5.

(4) In your program, whenever you need an input character, write CALL IP to put a new character into the A register; whenever you have a character to put out, put it in the A register and then CALL OP.

(5) Have a subroutine POLL in your program, as follows:

```
POLL: PUSH PSW
      CALL IPOLL
      CALL OPOLL
      POP PSW
      RET
```

and have your program call POLL once in each loop and just before each subroutine return.

As soon as you have gotten this much working, it will be possible for you to tinker with this system a bit further. Some suggested ways of doing this are as follows:

(1) The sizes of the input and output queues can be altered. Make sure to alter the *entire* data structure of listing 5 to insure that all the routines of listings 1, 2, 3 and 4 operate on the same version of the data structure.

(2) There is a section of code in IP that almost duplicates a similar section of code in IPOLL. With a little ingenuity, this can be made into a subroutine called by both IP and IPOLL. (Hint: the first instruction is INX H, and JNZ can be replaced by RNZ.) The same thing happens with OP and OPOLL.

(3) The input alarm logic can be further changed. For example, two kinds of alarms could be given: a single bell when the input queue is almost full, and a long string of bells (say, ten of them) when the queue is actually full.■

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As text is typed and the end of a line is reached, a partially completed word is shifted to the beginning of the following line. Whenever text is inserted or deleted, existing text is pushed down or pulled up in a wrap around fashion. Everything appears on the video display as it occurs, which eliminates guesswork. Text may be reviewed at will by variable speed scrolling both in the forward and reverse directions. By using the search or search and replace functions, any string of characters may be located and/or replaced with any other string of characters as desired.

Numerous combinations of line length, page length, line spacing and page spacing permit automatic formatting of any form. Character spacing, bold face, multicolumn and bidirectional printing are included in the Diablo versions. Multiple columns with right and left justified margins may be printed in a single pass.

Wide screen video

Versions are available for Imsai VIO video users with the huge 80x24 character screen. These versions put almost twice as many characters on the screen!!!

CP/M versions

Digital Research's CP/M, as well as its derivatives, including IMDOS and CDOS, and Helios PTDOS versions are also available. There are several NEC Spinwriter print packages. A utility program that converts The Electric Pencil to CP/M to Pencil files, called **CONVERT**, is only $35.

Features

- CP/M, IMDOS *and* HELIOS compatible
- Supports four disk drives
- Dynamic print formatting
- DIABLO and NEC printer packages
- Multi-column formatting in one pass
- Print value chaining
- Page-at-a-time scrolling
- Bidirectional multispeed scrolling controls
- Subsystem with print value scoreboard
- Automatic word and record number tally
- Cassette backup for additional storage
- Full margin control
- End-of-page control
- Non-printing text commenting
- Line and paragraph indentation
- Centering
- Underlining
- Bold face

Upgrading policy

Any version of The Electric Pencil may be upgraded at any time by simply returning the *original* disk or cassette and the price difference between versions, plus $15 to Michael Shrayer Software. Only the originally purchased cassette or diskette will be accepted for upgrading under this policy.

mss

MICHAEL SHRAYER SOFTWARE, INC.
1253 Vista Superba Drive
Glendale, CA. 91205
(213) 956-1593

Have we got a version for you?

The Electric Pencil II operates with any 8080/Z80 based microcomputer that supports a CP/M disk system and uses an Imsai VIO, Processor Tech. VDM-1, Polymorphic VTI, Solid State Music VB-1B or Vector Graphic video interface. REX versions also available. Specify when using CP/M that has been modified for Micropolis or North Star disk systems as follows: for North star add suffix A to version number; for Micropolis add suffix B, e.g., SS-IIA, DV-II B.

Vers.	Video	Printer	Price
SS-II	SOL	TTY or similar	$225.
SP-II	VTI	TTY or similar	225.
SV-II	VDM	TTY or similar	225.
SR-II	REX	TTY or similar	250.
SI-II	VIO	TTY or similar	250.
DS-II	SOL	Diablo 1610/20	275.
DP-II	VTI	Diablo 1610/20	275.
DV-II	VDM	Diablo 1610/20	275.
DR-II	REX	Diablo 1610/20	300.
DI-II	VIO	Diablo 1610/20	300.
NS-II	SOL	NEC Spinwriter	275.
NP-II	VTI	NEC Spinwriter	275.
NV-II	VDM	NEC Spinwriter	275.
NR-II	REX	NEC Spinwriter	300.
NI-II	VIO	NEC Spinwriter	300.
SSH	SOL	Helios/TTY	250.
DSH	SOL	Helios/Diablo	300.

Attention: TRS-80 Users!

The Electric Pencil has been designed to work with both Level I (16K system) and Level II models of the TRS-80, and with virtually any printer you choose. Two versions, one for use with cassette, and one for use with disk, are available on cassette. The TRS-80 disk version is easily transferred to disk and is fully interactive with the READ, WRITE, DIR, and KILL routines of TRSDOS 2.1.

Version	Storage	Price
TRC	Cassette	$100.
TRD	Disk	$150.

<u>Demand</u> a demo from your dealer!

Circle 319 on inquiry card.

BYTE's Bits

Computer Chess Report

The ninth annual North American Computer Chess Champsionship held at the convention of the Association for Computing Machinery December 1978 produced a new champion program. The Belle system, developed at Bell Laboratories by Ken Thompson, emerged with four wins in the Swiss System Tournament and with top honors.

Belle was seeded fourth in the tournament, and faced defending champion program Chess 4.7, the perennial favorite written by David Slate and Larry Atkin of Northwestern University, in the second round. This match was generally thought to be the finest game of the entire event. Only the programs "knew" what was going on; neither Robert Byrne nor David Levy, both highly skilled chessmasters, could even tell which program was winning.

A complete table of tournament results is reproduced here. The table contains blank entries because the 4 round Swiss System does not have each program play against every other program. A clear winner is produced, but the relative ranking of contestants finishing in the middle of the pack is indeterminate. The seeding of entries, performed by Dr Monroe Newborn, was fairly accurate; only three game results were contrary to that predicted by the seeding.

Two programs in the event were written for microprocessors. Sargon, for the Z-80, and Mike, for the 6800, competed against programs executing on impressively large computers. Much jest was made over the fact that Sargon, running on a Wave Mate Jupiter computer, defeated the program Awit, which was running on a huge Amdahl 470 system.

Awit had its problems, many of which were caused by attempts to run the program on several different machines during the tournament. The saddest hard luck entry, however, was the Brute Force program. It was plagued with system crashes, program bugs (it couldn't handle *en passant* pawn captures made in just a particular way), and malfunctioning "patches" to the program bugs. Brute Force lost its second round game in three different ways.

A speed chess tournament pitting human chess players against Chess 4.7 was held as an adjunct to the main event. The machine won two "5-minute" games from Mark Diesen, one of the fast rising young stars of American chess. Robert Byrne beat the machine twice, but in "10-minute" games. The programmers were honored to have had the program play a speed game against Edward Lasker, at 93 years of age the grand old man of chess. The computer was not awed; it won the game.

Chess Endgame Research and Developments

Ken Thompson, the programmer of Belle, has written other programs which specialize in playing chess endgames. One program plays the endgame of King and Queen versus King and Rook. In late December 1978, Walter Browne (see "Grandmaster Walter Browne versus Chess 4.6," January 1979 BYTE, page 110) played this endgame against the machine.

Browne played White, having the material advantage. The computer, playing a previously unknown defensive method, tenaciously defended its "theoretically lost" position. According to the rules of chess, Browne had to capture the Rook within 50 moves after the start of the exercise, or the game would be declared drawn.

The initial position was chosen to be the worst possible position for the computer's Black pieces. It is highly significant that despite his best efforts,

	Chess 4.7	Duchess	Chaos	Belle	Blitz	Ostrich	Black Knight	Awit	Sargon	Mike	BS6676	Brute Force
1. Chess 4.7		1		0		1	1					
2. Duchess	0		½		½			1				
3. Chaos		½		0		1			1			
4. Belle	1		1		1					1		
5. Blitz		½		0				1			1	
6. Ostrich	0		0				1					1
7. Black Knight	0					0				½		1
8. Awit		0			0				0		1	
9. Sargon			0					1		½		1
10. Mike				0			½		½		½	
11. BS6676					0			0		½		1
12. Brute Force						0	0		0		0	

Table 1: Cross table giving results of games in the 1978 North American Computer Chess Championship.

Browne was only able to capture the Rook exactly on move 50. This enabled Browne to quickly win the game and a $100 wager he had riding on it, but he was not able to find the win in 31 moves predicted by the program.

In his chess programs Thompson uses a Digital Equipment Corp PDP-11 which has been outfitted with two special purpose hardware devices. One generates possible moves, and the other evaluates positions.■

Land Identification and Information Management System

The San Diego County Department of Transportation has recently formed a task force whose objective is to formally define a proposed LIMS (Land Identification and Information Management System).

The collection, analysis and display of land related information, particularly in map form, is a significant part of everyday county operations, not only in San Diego or California, but nationwide. In the United States, county governments are the geographic and political units for land information and record keeping. Most land use recording and mapping systems today are unorganized and uncoordinated, having evolved from antiquated systems which have changed little since the days when America was still expanding westward. The current systems used in processing, storage, and subsequent use of this data pertaining to land use, acquisition, assessment, and development are proving to be costly and inefficient.

San Diego County's LIMS Task Force is proposing to develop a land identification system which will combine these efforts into a single, comprehensive and cost-effective system. High-speed, high capacity computer technology which will permit increased data storage, rapid access to this data, and automated display and/or printout of the desired map-formulated products is now available. The system would provide a central repository of all geographically oriented information in the county and a singular comprehensive file of land related data.

San Diego County is approaching the data input problem in a way that is significantly different from previously proposed or developed automated mapping systems. The innovative method of data input envisioned for the LIMS project will utilize inputs based on engineering calculations, in lieu of digitized inputs. This process will produce end results which represent real world geographic values instead of digitized map data.

The study will examine the inefficiencies of the current land records keeping system, prepare new system design parameters, evaluate alternative systems, and recommend a final design with organizational, funding, and implementation plans. When implemented, LIMS should serve such other county departments as the planning, assessment, records, and registry of voters departments. Additional users are expected to be the municipalities within the county, state and federal agencies located in the county, and land related businesses in the private sector.

For further information on the LIMS Project in San Diego County, contact Kenneth L Pyle, LIMS Task Force Director, at (714) 565-5297.■

A Call For Educational Material

The Florida Educational Computing Project, which is supported by the state of Florida, has recently approved a project for the evaluation and implementation of a microcomputer based instructional computing system. As a member of the evaluation committee, I am writing to you so we may contact those readers who have education oriented software developed for microcomputers.

We are looking for both computer aided instruction type material and administrative support programs (eg: film library inventory/control, word processing, statistical analysis, etc.). At this time we do not have the funds to purchase any software, and would therefore be willing to certify the return or destruction of any program material loaned to us.

Because of the variety of computers these programs may run on, we would prefer those which are not too dependent on a particular hardware configuration or operating system (if one is required). However, we would like to hear about any programs running on 6502, 6800, 8080, 8085, or Z-80 machines.

The outcome of this project will be a catalog listing all the acceptable software packages we receive, their evaluation, and their source of distribution. This catalog will be available to all educational institutions in the state of Florida and to any other interested educational systems. Naturally we would like to share with those who contribute software for evaluation, possibly starting an exchange program among the participants.

Any help we receive would not only be greatly appreciated, but would accelerate the exposure, use, and knowledge of microcomputers in general. We feel that the microcomputer, because of its relative small size, low cost, and dedicated one-on-one responsiveness, will prove to be a powerful learning tool for the student and a valuable timesaving aid to the educator.

We hope, with the cooperation of your magazine and your readers, that our efforts will show that the microcomputer is "an idea whose time has come" in the field of education.

Those who have software they wish to submit for evaluation and inclusion in our catalog, or questions concerning our project may contact Dr Nelson J Towle, Sarasota County Schools, 2409 Hatton St, Sarasota FL 33577, (305 953-5000 extension 322.■

Queuing Theory, The Science of Wait Control

Part 2: System Types

Len Gorney
Box 96 R D 1
Clarks Summit PA 18411

In part 1 we discussed the computer implementation of *row* and *circular* queues. Now, let us take a look at the structure of queues in the real world and see if they can be fitted to our previous programs. In the following discussion, the word *queue* refers to the waiting line in the system. The word *facility* refers to the service facility area located at the head of the queue.

System Types

There are four general types of queuing structures. The first, and simplest, is the single queue single facility system (figure 3). In this structure, there is one waiting line and one service area to be studied. A 1 pump gas station with one entrance is a real world example of this system.

We can extend this system to the single queue multifacility system (see figure 4). In this structure, customers line up in a single waiting line and are serviced at the first of a series of facilities. Upon departure from the first facility, the customers immediately enter another queue to await their turn at the second service facility. This insertion and deletion continues until the customer is eventually deleted from the last facility and consequently the entire system. This structure is not unlike a cafeteria where you first line up for a sandwich, then line up for dessert, then for a drink, and finally, for the cash register.

Another basic queue structure is a multiqueue single facility system (see figure 5). This is the type of structure you see at a typical supermarket checkout counter area. Customers arrive at the queue with their purchases and choose one of many waiting lines. Each service facility offers the same service, that is, checking out the purchases, but each line holds different customers.

The multiqueue, multifacility system in figure 6 is a combination of the previously mentioned structures. A number of initial queues feed into a series of facilities. When a customer enters a particular queue, that customer travels from each facility within that subsystem until the eventual deletion from the system. Once a customer is entered into a subsystem, that customer causes that subsystem to behave as does the single queue multifacility queue system.

Any waiting line can be fitted to one of the four queue structures just mentioned. Try it the next time you're waiting in a line.

After we are able to define the type of queue we have, the problem of analyzing the structure and arriving at answers most important in queuing problems is our next step. At this time we won't concern ourselves with the difference between a single server or a multiserver queue. The former represents a grocery store checkout counter arrangement where customers enter any line (usually the shortest or the fastest moving). The latter fits into the situation at a barbershop. One long line feeds into

Figure 3: A single queue single facility system with one waiting line and one service area.

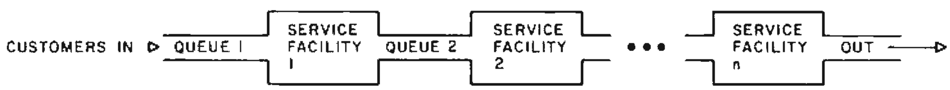

Figure 4: Single queue multifacility system, in which the customer waits in a queue to use a facility, then waits in another queue for the second facility, and so on until all service facilities have been used.

Note: The numbering of the figures and listings is continued from part 1 in April 1979 BYTE, page 132.

a large service area where a number of barbers (ie: the servers) wait for you to come to them.

Let's imagine a 1 pump gas station. At the start of the day, the operator (ie: server) opens the pump and waits for the first customer of the day to arrive. After some period of time, the first customer arrives and immediately drives up to the pump for service. This lucky first customer has no waiting time since the facility (at the head of the queue) is open and free of previous customers. The customer requires some period of time for service, and upon completion of this servicing time leaves the system. The operator sits back and waits for the next customer to arrive.

The second customer arrives, is immediately served, and leaves the system. If the only time a customer spends in a queue is the time required for service, no queue forms. What we need for a queue to form is to have customers arrive while there is a customer being serviced. Then a line will form with waiting customers. The queue will form based entirely upon the service requirements of the customer at the service area.

Randomness

A pure queuing problem requires that customer arrival and service times be different. In other words, while a customer is being serviced, other customers enter the system at random intervals during the simulation period to form a queue.

Formally speaking, the randomness of these arrivals follows a *Poisson distribution* and exponential interarrival times. Basically, this means that an arrival has an equal chance of arriving at the tail of the queue at any time during the simulation period of the problem. Typical nonqueue structures do not exhibit this random criterion. For example, a movie theater line is not a good queue problem because arrivals usually bunch up in a period 10 to 15 minutes before the new show starts. Therefore, during the simulation period, randomness is a key ingredient. Randomness causes the queue to lengthen and decrease based only on the service requirements of each customer.

Usually a customer must wait in a line at any business establishment before receiving the desired service. How the businessman treats these waiting customers is of prime importance as to the success or failure of most businesses. A typical customer will take one of the following actions when faced with a waiting line. The first action is to just wait in the line until service arrives. Once in line, that customer will remain in line until the end. The businessman has little worry over this customer because this customer will eventually be serviced and some profit will be realized.

A second alternative open to a waiting customer is for that customer to jockey from line to line. How many times have you seen this customer arrive at one queue, wait for a short period of time, move to another queue, wait again, then move again, and so on. This situation exists in the multiqueue system as is evidenced in a bank or large supermarket with many service facilities available for customer use.

The definition of a queue requires that arrivals to the queue be random.

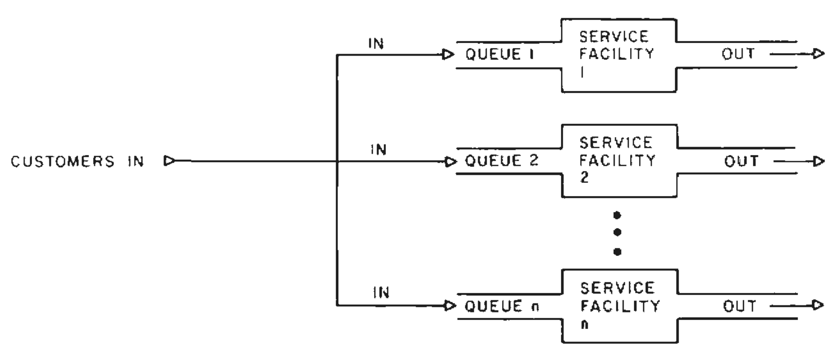

Figure 5: Multiqueue single facility system. An example of such a system is the supermarket checkout area. The checkout area has several service facilities, each with a corresponding queue, that all offer the same service.

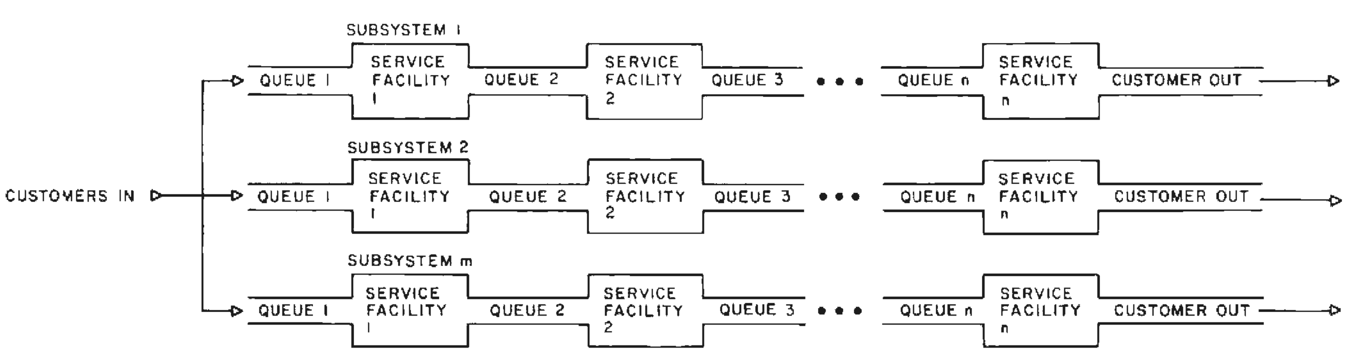

Figure 6: Multiqueue, multifacility system. This system has a number of initial queues feeding into a series of facilities. A customer entering a particular queue stays within that particular subsystem until leaving the system.

The previous two actions should cause little concern. The customer remains in the system and will eventually be served, thereby yielding the business some profit. However, what happens when the customer leaves the system after entering or refuses to enter the system initially?

If a customer has entered the system and leaves before being serviced, that customer has reneged. This situation occurs quite often when the waiting lines are moving at a rate far too slow for the customers within the lines. The customer and possible profits are lost to the businessman when a customer's action takes him or her on this route.

The last, and most damaging to the businessman, is the situation where a customer doesn't initially enter the system. When a customer sees a long and slow moving line, that customer usually balks. This customer is surely lost because he doesn't even give the businessman a chance at the very outset.

Since time is money, the important questions relating to queuing systems must be solved with relation to the time involved in waiting and servicing customers.

What is the maximum amount of time a customer waits in a line? What is the average amount of time all the customers are expected to wait in line before being served and deleted? What is the maximum amount of service time for any one customer during a typical period of time? Any measurement involving customer waiting time and customer service time is vital to the success or failure of a business.

A Queuing Problem

The program shown in listing 3 is that of a typical queuing problem utilizing the circular queue as the queuing structure. What we may have here is a hypothetical 1 pump gas station. The system will therefore be described as a single queue single facility structure.

Past experience gives us some of the input parameters required for the problem solution. For example, our queue is dimensioned to ten locations, so only ten cars can fit in our service area. This parameter can be adjusted using input parameter questions at the beginning of the program. In addition to the queue length, the program asks for the minimum and maximum typical service times. The arrivals per unit time determine how many customers are arriving each minute during the simulation. The simulation is halted after the first parameter value is reached, namely, the amount of time to run the model.

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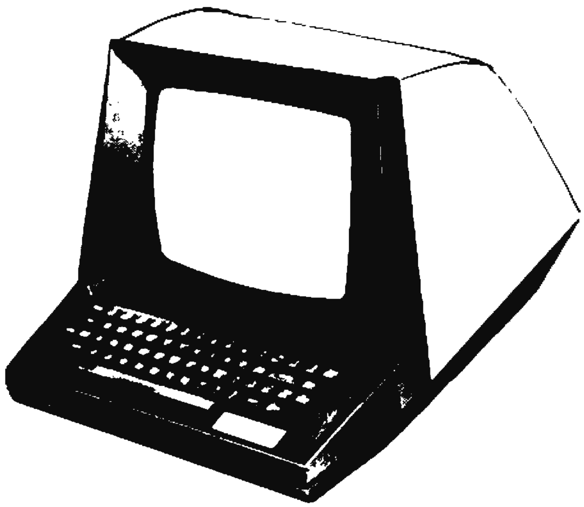

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SPECIFICATIONS

DISPLAY

SCREEN CAPACITY, CHARACTERS	2000
CHARACTERS PER LINE	80
NUMBER OF LINES	25
SCREEN	P4 phosphor (white)
TUBE SIZE(DIAGONAL)	12 inches (30.4 cm)
VIEWING AREA	54 square inches (137.1 cm)
CHARACTER SIZE	0.20" high x .08" wide (5.08 mm high x 2.03 mm wide)
REFRESH RATE	60 Hz (50 Hz available)
SCAN METHOD	Raster
CHARACTER GENERATION	5 x 7 character in an 8 x 10 dot matrix
CURSOR	Blinking block

MEMORY

TYPE	Random Access Memory
CAPACITY	2000 characters

OPERATOR CONTROLS

POWER ON/OFF SWITCH	On rear of unit
BRIGHTNESS CONTROL	On rear of unit

POWER REQUIREMENTS

Model 501 – 115 volts, 60 Hz, 100 watts nominal
Model 502 – 230 volts, 50 Hz, 100 watts nominal

INTERFACE

DATA FORMAT	
DATA BITS	7 serial, asynchronous
DATA BIT 8	1, 0 or deleted
PARITY	Odd, even or deleted with error displayed as DLE
STOP BITS	1 or 2
DATA TRANSFER RATE	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 BAUD

STANDARD FEATURES

INVERSE VIDEO	Operator or software selectable
TRANSMIT MODES	Half or full duplex (switch selectable)
DATA ENTRY	Top or bottom line
END OF LINE BELL	Switch selectable
CURSOR POSITIONING	X–Y
CURSOR ADDRESS	Load and read
DISPLAYABLE CHARACTERS	126 (including space)
CURSOR CONTROLS	Up, down, left, right, home, return
AUTOMATIC ROLL-UP	Switch selectable
AUTO CARRIAGE RETURN AND LINE FEED	Switch selectable
MONITOR MODE	Special "Monitor" Mode allows display of control codes (first two columns) of ASCII Code Chart).

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Listing 3: BASIC program that simulates a single queue single facility system such as a 1 pump gas station. The program incorporates several functions discussed in part 1.

```
1000 DIM Q(10)
1010 PRINT "MINUTES TO RUN SIMULATION=";
1020 INPUT M
1030 PRINT "MAXIMUM ARRIVALS/UNIT TIME=";
1040 INPUT A2
1050 PRINT "MINIMUM SERVICE TIME=";
1060 INPUT S2
1070 PRINT "MAXIMUM SERVICE TIME=";
1080 INPUT S3
1090 PRINT "QUEUE LENGTH=";
1100 INPUT H2
1110 PRINT "INPUT 1 FOR RUNNING OUTPUT, ELSE INPUT 0";
1120 INPUT P
1130 C = 0
1140 C2  =  0
1150 C3  =  0
1160 C4  =  0
1170 M2  =  0
1180 M3  =  0
1190 S4  =  0
1200 H  =  H2
1210 T  =  H2
1220 FOR J2 = 1 TO H2
1230 Q(J2)  =  -9
1240 NEXT J2
1250 Q(T) = 0
1260 T = T - 1
1270 GOSUB 1610
1280 FOR J = 1 TO M
1290 FOR J2 = 1 TO H2
1300 IF Q(J2) = -9 THEN 1330
1310 C = C + 1
1320 Q (J2) = Q (J2) + 1
1330 NEXT J2
1340 C2 = C2 + C
1350 IF C <= C3 THEN 1370
1360 C3 = C
1370 C = 0
1380 IF P = 0 THEN 1410
1390 PRINT " PICTURE OF QUEUE AFTER "; J; " MINUTES"
1400 GOSUB 1680
1410 IF Q(H) < M3 THEN 1520
1420 M2 = M2 + M3
1430 C4 = C4 + 1
1440 S4  = S4  + S
1450 IF P = 0 THEN 1470
1460 GOSUB 1730
1470 GOSUB 2110
1480 GOSUB 1610
1490 IF P = 0 THEN 1520
1500 PRINT "PICTURE OF QUEUE AFTER DELETE"
1510 GOSUB 1680
1520 A3 = 1
1530 A = INT (RND (1) * A2)
1540 IF A3 > A THEN 1580
1550 GOSUB 1900
1560 A3 = A3 + 1
1570 GOTO 1540
1580 NEXT J
1590 GOSUB 1730
1600 STOP
1610 S = INT (RND (1)*10) + (S3-9)
1620 IF Q (H) = -9 THEN 1640
1630 Q (H) = 0
1640 M3 = Q (H) + S
1650 IF P = 0 THEN 1670
1660 PRINT "REQUIRED SERVICE TIME="; S
1670 RETURN
1680 FOR J2 = 1 TO H2
1690 PRINT Q (J2);
1700 NEXT J2
1710 PRINT "TAIL="; T;" HEAD="; H
1720 RETURN
1730 PRINT C4;" FULLY SERVED CUSTOMERS IN "; J;" MINUTES"
1740 PRINT "MAXIMUM CUSTOMERS QUEUED="; C3
1750 M5 = M2/C4
1760 PRINT "AVERAGE WAIT TIME ="; M5
1770 S5 = S4/C4
1780 PRINT "AVERAGE SERVICE TIME="; S5
1790 C5 = C2/J
1800 PRINT "AVERAGE NUMBER OF QUEUED CUSTOMERS="; C5
1810 RETURN
1850 REM
1860 REM    I N S E R T I O N   R O U T I N E
1870 REM
1880 REM CHECK TAIL AND HEAD POINTER VALUES
1890 REM
1900       IF H  =  T  GOTO 1970
1910       IF H  <  T  GOTO 2030
1920       IF T  >=  1 GOTO 2030
1930       IF H = H2 GOTO 2080
1931 REM
1932 REM  INSERT ITEM AT Q (H)
1933 REM  SINCE QUEUE IS EMPTY
1934 REM
1940       Q (H2) = 0
1950       T = H2-1
1960       GOTO 2050
1970       IF T <> 0 GOTO 2000
1971 REM
1972 REM  RESET POINTERS TO HEAD OF QUEUE
1973 REM
1980       H = H2
1990       T = H2
1991 REM
1992 REM  CHECK IF Q (T) EMPTY FOR POSSIBLE INSERT
1993 REM
2000       IF Q (T) <> -9 GOTO 2080
2010       H = H2
2020       T = H2
2021 REM
2022 REM  NORMAL TAIL INSERTION
2023 REM
2030       Q (T) = 0
2040       T = T -1
2050       IF P = 0 THEN 2070
2060       PRINT "ARRIVAL"
2070       RETURN
2080       IF P = 0 THEN 2100
2090       PRINT "OVERFLOW"
2100       RETURN
2101 REM
2102 REM      D E L E T I O N   R O U T I N E
2103 REM
2104 REM  CHECK POINTER VALUES FOR POSSIBLE DELETE
2105 REM
2110       IF H = T GOTO 2150
2120       IF H > 0 GOTO 2190
2130       H = H2
2140       GOTO 2180
2150       IF H <> 0 GOTO 2180
2160       H  =  H2
2170       T = H2
2171 REM
2172 REM  DELETE FROM Q (H) IF Q (H) HAS AN ITEM
2173 REM  ELSE, QUEUE IS EMPTY, I. E. UNDERFLOW
2174 REM
2180       IF Q (H) = -9 GOTO 2240
2190       Q (H) = -9
2200       H = H -1
2201 REM
2202 REM  RESET POINTERS FOR NEXT DELETE
2203 REM
2210       IF H <> 0 GOTO 2260
2220       H = H2
2230       RETURN
2240       IF P = 0 THEN 2260
2250       PRINT "UNDERFLOW"
2260       RETURN
2270 END
```

Conclusion

For the serious reader, the list of reference material includes those texts which place a good emphasis on queuing theory. After digesting the ideas in this article, plunge into these texts. Now I can return to my reading queue and get to those lines of books and articles waiting on my bookshelf. I'm sure that somewhere out there is a line waiting for you! ■

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Desk Top Wonders

Digits

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Digits is a number guessing game written for the Texas Instruments SR-52 programmable calculator featuring cyclic permutation, nested loops and various space saving devices. Hal Snyder teaches mathematics at Roosevelt University in Chicago.

Listing 1: The Digits program, written for the Texas Instruments SR-52. The object of the game is to guess a number generated randomly by the calculator in the fewest number of guesses possible.

```
Program Listing             Commentary

000  LBL A'                 ; number of digits
002  4 STO 00 rtn

007  LBL E'                 ; truncate
009  ( STO - .5 )
015  EE INV EE rtn

019  LBL D'                 ; 10^10
021  10 INV log rtn

026  LBL +                  ; count matching
028  A'                     ; digits
029  LBL cos
031  9 SUM 00
035  ( IND RCL 00 -
041  9 INV SUM 00
046  IND RCL 00 )
051  INV ifzro π            ; if match, clear
054  IND STO 00             ; guess digit,
058  1 SUM 19               ; increment count
062  LBL π
064  dsz cos rtn

067  LBL B                  ; respond to guess
069  prt fix 0
072  ÷ A' INV log
076  LBL sin
078  x 10 =
082  - E' IND STO 00 =
089  dsz sin                ; fraction in display
091  0 STO 19
095  SBR +                  ; tens digit in
097  10 PROD 19             ; response
102  A' dsz x
105  LBL x                  ; cycle
107  RCL 00 +               ; save outer loop
111  A' RCL 01 (            ; index
116  LBL 1'
118  IND EXC 00
122  INV ifzro 2'           ; leave zeroed digit
125  IND EXC 00             ; in place
129  LBL 2'
131  dsz 1'
133  + A' 0 )
137  IND STO 00
141  SBR +
143  0 = STO 00             ; retrieve outer
148  dsz x                  ; loop index
150  RCL 19 INV fix
155  prt pap HLT

158  LBL E                  ; pick a number
160  fix 0 A'
163  LBL SUM                ; generate random number
165  RCL 00 + 9             ; by taking
170  + STO 01               ; (R99 x 7^9) mod 10^10
174  7 y^x 9 x RCL 99
181  ÷ D' - E' =
186  x D' ÷ STO 99
192  9 INV log =            ; get leading digit
196  E' x (
199  IND STO 01 -
204  07 ) =                 ; is it in range?
208  ifpos SUM
210  dsz SUM
212  INV fix CLR HLT        ; cleanup

216  LBL D                  ; seed for random
218  EXC 99 HLT             ; note EXC is used
```

Instructions:

1. Enter program.
2. Start random number sequence by keying in a positive integer and pressing D.
3. For a new game, press E. In the initial configuration, the SR-52 selects four digits, all between 1 and 6, such as 2361 or 5335, then displays 0 (this takes about 120 seconds).
4. Key in your guess and press B. After a few moments (see below for approximate timing), SR-52 responds with a 2 digit number xy, where x (tens) is the number of digits in your guess which are in the right position, and y (ones) is the number of correct digits in the wrong position. For example, if the SR-52 had chosen 5335 and your guess was 5351, the response would be 21.
5. Repeat step 4 as many times as needed to determine the hidden number completely. If not using a TI PC-100 printer, you should keep a written record of guesses and responses. The object of the game is to use as few guesses as possible. Step 3 starts a new game.
6. Variation: the program is initially set for 4 digit numbers. For any other number (2 to 9) of places, set location 002 to the desired number, say by keying *GTO A' LRN* number *LRN.*
7. Variation: the program initially uses digits 1 thru 6. To use digits 1 thru r, enter r+1 in locations 204 thru 205, with leading 0 if r+1 is a 1 digit number. To use digits 1 thru 7, key *GTO 204 LRN 08 LRN.*

Digits Versus Codebreaker

The game described above is similar to Codebreaker (copyright 1976, Texas Instruments), which comes in the TI game library for the SR-52. Digits, however, permits repeated occurrences of a digit in the hidden number, and can be easily modified (steps 6 and 7 above) for different versions of the game.

The Program

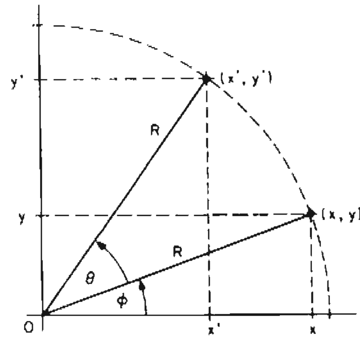
The Digits program is shown in listing 1. Frequently used subroutines are placed at the front for improved speed. Subroutine

E' shows one way to do truncation on the SR-52. A quick way to get powers of 10 is illustrated in D'. The "cycle" routine (locations 105 thru 149) cyclically permutes the digits of the guess entered with the following modification: any digits in the guess which were previously matched in the answer will have been set to 0, and these digits will not be moved. (Thus, 1234 becomes 4123, but 1034 becomes 4013.) The outer loop (105 thru 149) contains an inner loop (114 thru 132), and the program listing shows how the outer index is saved on the SR-52 operations stack when the inner loop is executing.

The random number formula (see listing commentary) is the one used in the TI basic library. Key D can be used between games to examine or restart the random sequence since it exchanges display contents with the random number in memory.

Response time depends on the width of the numbers used. As a rule, if you are using numbers with p decimal positions, the time in seconds from guess entered to response displayed will be $5/3\ (p^2+p)$, which means it will take about 20 and 35 seconds for 3 and 4 digit numbers respectively, all the way up to 150 seconds for 9 digit numbers.■

Figure 1: Diagram illustrating rotation of the vector x, y in Cartesian coordinates. The final position of the vector endpoint is x', y'. Two different "black boxes," or subroutines, are used to solve various trigonometric problems by means of the CORDIC algorithm. Black Box 1 (BB 1) calculates x' and y' given the displacement angle θ. Black Box 2 (BB 2) calculates the displacement angle θ necessary to rotate the vector to a given y'. These two routines enable the programmer to calculate a variety of trigonometric functions quickly and efficiently.



Trigonometry in Two Easy Black Boxes

About the Author

John A Ball is a radio astronomer at the Center for Astrophysics, Cambridge MA. He has written a book entitled Algorithms for RPN Calculators *published by Wiley.*

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If your computer can add, subtract, multiply, divide, calculate square roots, sines, cosines, tangents, arc sines, arc cosines, and arc tangents, then you are prepared to solve any trigonometry problem. However, if your computer lacks some of these trig functions, then this article will be helpful, as it shows how to use CORDIC techniques to program two "black boxes" (alias subroutines or processors) to perform trigonometric functions. As a bonus, you will find that some complex and important problems are easier with the two black boxes than with conventional trig functions.

Coordinate Rotations

Suppose we have a black box (call it BB 1 for "black box number one") that performs rotations in Cartesian coordinates. Given x, y, and θ, BB 1 calculates x' and y' where:

$$\begin{aligned} x' &= x\cos\theta - y\sin\theta \\ &= (x - y\tan\theta)\cos\theta \\ y' &= y\cos\theta + x\sin\theta \\ &= (y + x\tan\theta)\cos\theta \end{aligned} \qquad (Eq\ 1)$$

These are the standard equations for a rotation. They can be derived from figure 1. The sign convention on the angle θ in these equations is such that the point (or vector) x, y rotates counterclockwise through an angle θ in a stationary coordinate system, or alternatively, the coordinate system rotates clockwise through an angle θ and the point is stationary. Interchanging the plus and minus signs in equations 1 gives the opposite sign convention for θ.

Many trigonometric problems are solvable using BB 1. The special case $y = 0$, $x = R$, for example, gives:

$$\begin{aligned} x' &= R\cos\theta \\ y' &= R\sin\theta \end{aligned} \qquad (Eq\ 2)$$

These are the equations for converting polar to rectangular coordinates. The special case $y = 0$, $x = 1$ gives:

$$\begin{aligned} x' &= \cos\theta \\ y' &= \sin\theta \end{aligned} \qquad (Eq\ 3)$$

BB 1 will calculate sines and cosines, and from these the other trigonometric functions are easy.

Now suppose we have a second black box, BB 2, which rotates the given coordinates x and y through whatever angle is

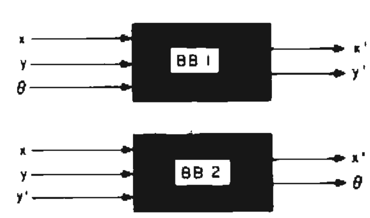

Figure 2: Functional diagram of Black Box 1 and Black Box 2 showing inputs and the outputs which can be calculated from them.

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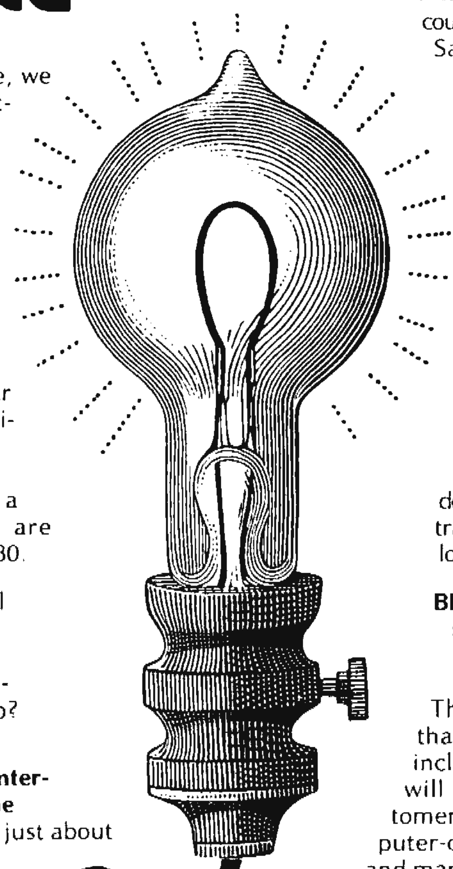

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necessary to give a specified y'. So BB 2 also satisfies equations 1 but x, y, and y' are the given quantities and BB 2 calculates x' and θ as shown in figure 2. Equations 1 can be rewritten as:

$$\begin{aligned} x' &= \pm\sqrt{x^2 + y^2 - y'^2} \\ \theta &= \sin^{-1}(y'/R) - \phi \end{aligned} \qquad (Eq\ 4)$$

where

$$\begin{aligned} R &= \sqrt{x^2 + y^2} \\ \phi &= \tan^{-1}(y/x) \\ x &= R\cos\phi \\ y &= R\sin\phi \end{aligned} \qquad (Eq\ 5)$$

That is, R and ϕ are the polar coordinates corresponding to x and y as shown in figure 1. Some combinations of x, y, and y' are impossible: if $|y'| > R$, then BB 2 will award you a demerit and write an uncomplimentary error message.

Two distinct solutions exist for x' and θ. These solutions differ in the sign of x', and θ is replaced by $180° - \theta - 2\phi$. BB 2 gives the solution first encountered while rotating. Alternatively, a version of BB 2 could be written to give both solutions.

BB 2 is also a powerful trigonometric problem solver. The special case $y' = 0$, for example, gives:

$$\begin{aligned} x' &= \pm R \\ \theta &= -\phi \text{ or } 180° - \phi \end{aligned} \qquad (Eq\ 6)$$

This case gives rectangular to polar coordinate conversion. Also, since $\phi = \tan^{-1}(y/x)$, this case gives a four quadrant arc tangent. The special case $y = 0$ gives:

$$\begin{aligned} x' &= \pm\sqrt{x^2 - y'^2} \\ &= x\cos\theta \\ \theta &= \sin^{-1}(y'/x) \end{aligned} \qquad (Eq\ 7)$$

This case gives an arc sine and the solution to a right triangle. And the special case $x = 0$ gives:

$$\begin{aligned} x' &= \pm\sqrt{y^2 - y'^2} \\ &= -y\sin\theta \\ \theta &= \cos^{-1}(y'/y) \end{aligned} \qquad (Eq\ 8)$$

This case gives an arc cosine and the solution to a right triangle.

Together with add, subtract, multiply, divide, and maybe a square root, BB 1 and BB 2 can be used to solve any solvable problem in plane or spherical trigonometry.

Many problems are simplified by being written directly in terms of coordinate rotations or rectangular to polar to rectangular coordinate conversions. Examples are conversions of coordinate systems in positional astronomy and problems in complex numbers, especially complex impedances in electronics.

CORDIC Techniques

Volder (1959) developed the original CORDIC (COordinate Rotation DIgital Computer) technique for use in a special purpose computer which solved, among other problems, for the distance and heading between two points specified by their latitudes and longitudes on the earth. Meggitt (1962) and Walther (1971) described generalizations of the CORDIC technique called pseudo-multiplications and pseudo-divisions. (See the end of this article for bibliographic information about this reference and the other references cited.) Hewlett-Packard and other calculators use CORDIC techniques internally to calculate trigonometric functions [see Cochran (1972) and Egbert (1977)].

CORDIC techniques allow one to program (or to "solder" together) BB 1 and BB 2 using only adds, subtracts, and shifts inside the loops. Outside the loops one also needs one or two multiplications or divisions in a base 2 machine, or one or two multiplications or divisions and a square root in a base 10 machine. As a rough general rule, CORDIC techniques are faster and easier in a computer that has no floating point hardware and no multiply/divide hardware, but does have multibit shifts. If a multibit shift must be built up from single bit shifts or from a multiply, then series expansions to get trigonometric functions are sometimes preferable. These statements are usually also true in a base 10 machine with "digit" substituted for "bit." If you are really in a hurry, a CORDIC rotator can be made in hardware, as Volder (1959) describes.

With the second half of equations 1 in mind, suppose we want to perform coordinate rotations quickly and easily. The $\cos\theta$ factor multiplying the parentheses is a scale factor for both x' and y'. As a special case, consider rotating through an angle θ_n satisfying:

$$\theta_n = \tan^{-1}(b^{-n}) \qquad (Eq\ 9)$$

where b is the radix or the base of the number system in the computer (usually $b = 2$ or 10) and n is an integer. For these special angles, the rotation in equations 1 simplifies to shifts (multiplying by $\tan\theta_n$ is equivalent to a right shift by n places) and add and subtract, except for the scale factor $\cos\theta_n$. Since θ_n becomes arbitrarily small for arbitrarily large n, any angle θ can be represented as a sum of θ_n.

$$\theta = \sum_n R_n\theta_n \qquad \text{(Eq 10)}$$

where each R_n is an integer, and $|R_n| < b$. In base 2, for example:

$$\theta_n \cong 45^\circ, 26.565^\circ, 14.036^\circ, 7.125^\circ, 3.576^\circ, \ldots \qquad \text{(Eq 11)}$$

and in base 10:

$$\theta_n \cong 45^\circ, 5.7106^\circ, 0.5729^\circ, 0.05730^\circ, 0.005730^\circ, \ldots \qquad \text{(Eq 12)}$$

The set R_n represents θ in what is called the arc tangent radix.

Given θ and b, the set R_n is unique only with some additional conditions. In bases other than 2, we usually specify $R_n \geqslant 0$ and also $\theta \geqslant 0$, which are not restrictions, since $0 \leqslant \theta < 360^\circ$ represents all possible angles. In base 2 we can specify $R_n = \pm 1$ (never 0) provided we begin with a 90° initial rotation, and provided $180^\circ < \theta < 180^\circ$. Rotating by 90° is, of course, trivial. These R_n in base 2 have the following advantage: The scale factor $\cos(R_n\theta_n)$ is independent of R_n, so the product

$$K = \prod_n (\cos\theta_n)^{-1} \cong 1.64676 \qquad \text{(Eq 13)}$$

which is the scale factor for the total θ rotation, is a constant independent of R_n and θ. K depends only slightly on the number of bits in a word, which is the range of n in equation 13.

In any base other than 2, K is a function of R_n and we need to calculate K for each θ. Fortunately this calculation can be done also using only adds and shifts inside the loop and a square root outside the loop. To see this, write:

$$K = \prod_n \left(\frac{1}{\cos\theta_n}\right)^{R_n} = \prod_n \left(\sqrt{1 + \tan^2\theta_n}\right)^{R_n} \qquad \text{(Eq 14)}$$

$$K^2 = \prod_n (1 + b^{-2n})^{R_n}$$

Multiplying by b^{-2n} is equivalent to a right shift by $2n$ places.

This scheme for finding K works well for BB 1 because the square root can wait until outside the loop; but BB 2 is somewhat more difficult. In BB 2 we need to know K at each step of the loop in order to compare the current y' with the desired y' (unless it is 0). Except for the needed square root, we could use equations 14 to keep a correctly scaled version of the desired y' to compare with the current y' at each step. The need for a square root can be eliminated by stepping through angles of $2\theta_n$. The correct factor for K therefore becomes $(\cos\theta_n)^{-2}$. Rotating by $2\theta_n$ at each step is twice as much work as rotating by θ_n, but any other scheme involves still more work. BB 2 takes about twice as much time in the loop as BB 1, but needs no square root.

As pointed out by Walther (1971) and Rheinstein (1977), the CORDIC approach can also be used to calculate hyperbolic functions, and, from these, logarithmic and exponential functions. In my experience, however, the conventional approach using series expansions for logs and exponentials is almost always preferable.

CORDIC techniques produce arbitrarily precise answers if the effective word length is arbitrarily long. If digits lost by shifting are rounded rather than truncated, then the precision will usually be no worse than ±2 or ±3 in the least significant digit, as discussed by Meggitt (1962).

Test Programs in BASIC

Listing 1 is a CORDIC version of BB 1 and BB 2 written in BASIC. The point of using BASIC is that this listing is simultaneously an algorithm (or flowchart) and a test to verify that the algorithm works. The program in BASIC has no practical value, but should be translated into assembly language (or even hardware) to make useful subroutines.

Statements 10 thru 60 are initialization. B is the base of the computer's number system (a special version for B = 2 is discussed below). M is the number of digits in a word and also the number of places in the arc tangent radix representation of angles. The array A is θ_n (see equation 12). The value of A should be precalculated and assembled into the program as a permanent reference array. The D array is unnecessary in a working program. Instead, think of D(J)* as an operator that produces a right shift by 2J digits. This is important because D(J)* is *used* not as a multiply, but as a shift in the loops.

The units in this program are degrees. To

```
  5 REM BB1, BB2, AND R->P
  6 REM ADAPTED FROM RHEINSTEIN IN BYIE 2-8, 142 (AUGUST 1977)

 10 LET B = 10
 20 LET M = 6
 25 DIM A(M), D(M)
 30 FOR J = 0 TO M
 40  LET D(J) = B↑(-2*J)
 50  LET A(J) = ATN(B↑(-J))*180/3.14159
 60 NEXT J

 70 PRINT "TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ";
 80 INPUT Z
 85 PRINT
 90 IF Z = 1 GOTO 120
100 IF Z = 2 GOTO 300
105 IF Z = 3 GOTO 500
110 GOTO 70

120 PRINT "TYPE X, Y, THETA ";
130 INPUT X, Y, T
132 IF T >= 0 GOTO 135
133 LET T = T+360
134 GOTO 132
135 PRINT
155 LET K = 1
170 FOR J = 0 TO M
175  LET T1 = T
180  LET T = T-A(J)
190  IF T < 0 GOTO 250
210  LET Y1 = Y
220  LET Y = Y+X
230  LET X = X-D(J)*Y1
235  LET K = K+D(J)*K
240  GOTO 175
250  LET T = T1
255  LET Y = Y*B
260 NEXT J
265 LET K = SQR(K)
280 PRINT "X' = "; X/K; ", Y' = "; Y/K/B↑(M+1)
290 GOTO 70

300 PRINT "TYPE X, Y, Y' ";
310 INPUT X, Y, Y3
315 PRINT
340 LET T = 0
345 LET K = Y3
350 FOR J = 0 TO M
370  LET Y1 = Y
372  LET X1 = X
374  LET Y2 = Y+X
376  LET X2 = X-D(J)*Y
380  LET Y = Y2+X2
382  LET K1 = K
384  LET K = K+D(J)*K
390  IF (Y-K)*(Y1-K1) <= 0 GOTO 430
400  LET X = X2-D(J)*Y2
402  IF X*X1 > 0 GOTO 410
404  IF (Y1-K1)*X > 0 GOTO 430
410  LET T = T+A(J)+A(J)
420  GOTO 370
430  LET Y = Y1
435  LET X = X1/B
436  LET K = K1
440 NEXT J
442 IF ABS(Y/K-1) < B↑(-M+1) GOTO 445
443 PRINT "ERROR! DELTA Y = "; (Y/K-1)*Y3
445 LET K = K/Y3
450 PRINT "X' = "; X/K*B↑(M+1); ", THETA = "; T
460 GOTO 70

500 PRINT "TYPE X, Y ";
510 INPUT X, Y
515 PRINT
540 LET T = 0
545 LET K = 1
550 FOR J = 0 TO M
570  LET Y1 = Y
580  LET Y = Y-X
590  IF Y*Y1 <= 0 GOTO 630
600  LET X = X+D(J)*Y1
610  LET T = T+A(J)
615  LET K = K+D(J)*K
620  GOTO 570
630  LET Y = Y1*B
640 NEXT J
645 LET K = SQR(K)
646 IF X > 0 GOTO 650
647 LET X = -X
648 LET T = T+180
650 PRINT "R = "; X/K; ", PHI = "; T
660 GOTO 70

999 END
```

Listing 1: A CORDIC version of Black Box 1, Black Box 2, and a rectangular to polar conversion routine written in BASIC for the decimal number system. This listing is intended as a "flowchart" of the CORDIC algorithm to show how it works. Readers should convert it to assembly or machine language to make it fast enough to be practical.

```
  5 REM BB1, BB2, R->P
  6 REM ADAPTED FROM RHEINSTEIN IN BYTE 2-8, 142 (AUGUST 1977)
  8 REM BINARY VERSION, B = 2

 12 LET K = 1.64676
 20 LET M = 22
 25 DIM A(M), D(M)
 27 LET A(0) = 90
 30 FOR J = 1 TO M
 40  LET D(J) = 2↑(1-J)
 50  LET A(J) = ATN(D(J))*180/3.14159
 60 NEXT J

 70 PRINT "TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ";
 80 INPUT Z
 85 PRINT
 90 IF Z = 1 GOTO 120
100 IF Z = 2 GOTO 300
105 IF Z = 3 GOTO 500
110 GOTO 70

120 PRINT "TYPE X, Y, THETA ";
130 INPUT X, Y, T
131 IF T-180 < 0 GOTO 134
132 LET T = T-360
133 GOTO 131
134 IF T+180 > 0 GOTO 137
135 LET T = T+360
136 GOTO 134
137 PRINT
170 FOR J = 0 TO M
175  LET I = SGN(T)
176  LET I = I+1-ABS(I)
177  REM I = SGN(T) WON'T DO BECAUSE SGN(0) = 0
180  LET T = T-I*A(J)
210  LET Y1 = Y
212  IF J > 0 GOTO 220
213  LET Y = I*X
214  LET X = -I*Y1
215  GOTO 260
220  LET Y = Y+I*D(J)*X
230  LET X = X-I*D(J)*Y1
260 NEXT J
280 PRINT "X' = "; X/K; ", Y' = "; Y/K
290 GOTO 70

300 PRINT "TYPE X, Y, Y' ";
310 INPUT X, Y, Y3
315 PRINT
340 LET T = 0
345 LET K1 = Y3
350 FOR J = 1 TO M
372  LET I = SGN((K1-Y)*X)
373  LET I = I+1-ABS(I)
380  LET Y1 = Y+I*D(J)*X
400  LET X = X-I*D(J)*Y
402  LET Y = Y1+I*D(J)*X
404  LET X = X-I*D(J)*Y1
410  LET T = T+I*(A(J)+A(J))
415  LET K1 = K1+D(J)*D(J)*K1
440 NEXT J
442 IF ABS(Y/K1-1) < 2↑(-M+3) GOTO 445
443 PRINT "ERROR! DELTA Y = "; (Y/K1-1)*Y3
445 LET K1 = K1/Y3
450 PRINT "X' = "; X/K1; ", THETA = "; T
460 GOTO 70

500 PRINT "TYPE X, Y ";
510 INPUT X, Y
515 PRINT
540 LET T = 0
550 FOR J = 0 TO M
570  LET Y1 = Y
572  LET I = SGN(Y)
573  LET I = I+1-ABS(I)
574  IF J > 0 GOTO 580
575  LET Y = -I*X
576  LET X = I*Y1
577  GOTO 610
580  LET Y = Y-I*D(J)*X
600  LET X = X+I*D(J)*Y1
610  LET T = T+I*A(J)
640 NEXT J
650 PRINT "R = "; X/K; ", PHI = "; T
660 GOTO 70

999 END
```

Listing 2: A CORDIC version of Black Box 1, Black Box 2, and a rectangular to polar conversion routine written in BASIC for the binary number system.

change to radians, drop the *180/3.14159 in line 50 and replace 360 by 2π in line 133 and 180 by π in line 648.

Statements 70 thru 110 allow the operator to select BB 1, BB 2, or R→P discussed below.

BB 1

Statements 120 thru 290 are BB 1. The operator types X, Y, and THETA (alias T). Lines 132 thru 134 make T positive. This version can rotate only positively; negative angles are handled by going all the way around. Two nested loops are necessary: a J loop from lines 170 thru 260, which corresponds to the n sum in equation 10, and an inner loop from 175 to 240, which rotates and also determines R_n by the subtraction in 180 and the test in 190. Statements 210 thru 230 implement equation 1 for $\theta = \theta_n$ but with two twists: first, $\cos\theta$ is ignored until outside the loops, as mentioned above; second, the Y value is actually YB^J (see line 255). This eliminates a shift which would otherwise be in line 220. So we trade a multidigit shift in the inner loop for a single digit shift in the J loop (line 255) and a multidigit shift outside the loops (in the print statement 280). This idea is described by Egbert (1977). The inner loop also calculates K, as in equations 14. Line 235 is another shift and add (not a multiply) and the square root is outside the loop in line 265. Dividing by K in line 280 gives X′ and Y′ correctly scaled. Note that X, Y, and T are all written over.

BB 2

Statements 300 thru 460 are BB 2. The angle T starts from 0 in line 340 and K is initialized to Y3 (the desired y') in line 345 rather than to unity as in line 155. The J loop extends from lines 350 thru 440 and the inner loop from lines 370 thru 420. Lines 370 thru 384 and lines 400 and 410 implement the double angle rotation described above. The trick of moving one of the shifts outside the inner loop, as described in BB 1, is used here also, but with the roles of X and Y interchanged (see line 435).

The obscure part of this program is probably the three IF statements (lines 390, 402, and 404) used to determine when to exit from the inner loop. Only one subtraction per cycle is needed in line 390 because the expression Y1-K1 for one cycle is the same as Y-K for the preceding cycle. The multiply is not needed. Instead, the point of 390 is

to determine whether the sign of Y-K differs from the sign of Y1-K1 and, if so, to go to line 430. These signs differ only if the last rotation has carried past the proper stopping point. K and K1 in line 390 are the desired y' scaled by the same factors as Y and Y1. The subtractions would be meaningless if the scale factors were different.

Even if the signs of Y-K and Y1-K1 in line 390 are the same, the rotation might still have carried past the proper stopping point. This occurs if Y1-K1 is positive and X has changed from positive (X1) to negative, or if Y1-K1 is negative and X has changed from negative (X1) to positive. These two cases correspond to rotating through 90° or 270° and are tested for in lines 402 and 404. The multiplications in 402 and 404 again need not be done, and the subtraction in 404 has already been done in 390. An alternative would be to perform the addition in line 410 and then test T.

Statement 442 tests whether the desired y' has been achieved. If not, the desired y' is too large ($|y'| > R$) and your reward is in 443. K needed to scale X′ is calculated in line 445, this time without a square root. However, there is a problem: Y3 (the desired y') must not be 0. This version of BB 1 cannot work with the desired $y' = 0$.

R→P

The special case $y' = 0$ in BB 2 is the very useful rectangular to polar (R→P) coordinate converter. Although the preceding general purpose BB 2 will not handle $y' = 0$, a special program for $y' = 0$ is actually easier and faster than BB 2. Statements 500 thru 660 are R→P. No new tricks are needed: R→P is quite similar to BB 1. The IF statement in line 590 determines whether or not the sign of Y has changed. The reversed signs in lines 580 and 600 change the sign of the angle to give ϕ rather than θ as the answer (see equations 6). Statements 646 thru 648 are necessary because X can be negative.

Base 2 is Special

A binary version with $R_n = \pm 1$, as shown in listing 2, allows some simplifications but also presents some problems. For BB 1 and R→P, K is the constant in line 12. With no inner loop, just a J loop, no advantage comes from shifting only X or only Y. So D(J)* is an operator causing a right shift by J-1 bits.

This binary version of BB 1 can rotate either positively or negatively, but only up to 180°; hence the reason for lines 131 thru 136. I is the direction to rotate and is equal to the sign of T (see line 175); so multiplying by I in lines 180, 213, 214, 220, and 230 is really just selecting whether to add or subtract. The special case for J = 0 in lines 213 through 215 is a preliminary 90° rotation, as mentioned above.

In BB 2, J can start at 1 rather than 0 (line 350) because each rotation step is double the normal angle. The direction to rotate is positive if K1-Y has the same sign as X and negative if these signs differ (see line 372). As before, K1 is the desired y' with the same scale factor as Y.

Most of the rest of this program is the same as the previous version in listing 1.

Examples

This section contains two examples of problems solved using BB 1 and BB 2. I use the following notation:

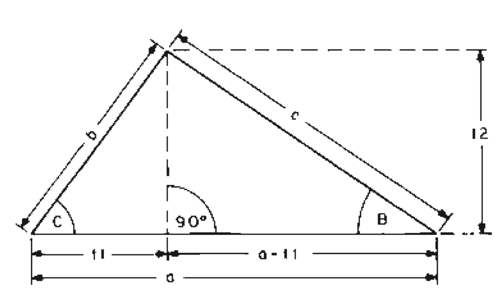
$$\begin{array}{l} \text{Call BB 1 } (x, y, \theta; x', y') \\ \text{Call BB 2 } (x, y, y'; x', \theta) \\ \text{Call R}\rightarrow\text{P } (x, y; R, \phi) \end{array} \qquad \textit{(Eq 15)}$$

In each case above, the given quantities precede and the answers follow the semicolon (see figure 2). When using the actual programs, remember that the given quantities often are written over.

Consider first a plane triangle. Given two sides and the included angle, find the other side and two angles (see figure 3). This problem is known as *SAS* for *side-angle-side: A*, *B*, and *C* are angles; *a*, *b*, and *c* are the oppo-

Figure 3: The side-angle-side problem in plane trigonometry (given a, b, C; *find* A, B, c*) can be solved as follows:*

*Call BB1 (*b, *0,* C; t*1*, t*2)*	t*1 and* t*2 are the rectangular coordinates corresponding to a vector of length* b *at an angle* C *(equation 2 in the text).*
*Call R→P (*a − t*1*, t*2;* c, B*)*	a − t*1 and* t*2 are the rectangular coordinates corresponding to a vector of length* c *at an angle* B.
A = *180°* − B − C	*the sum of the interior angles of a triangle is 180°.*



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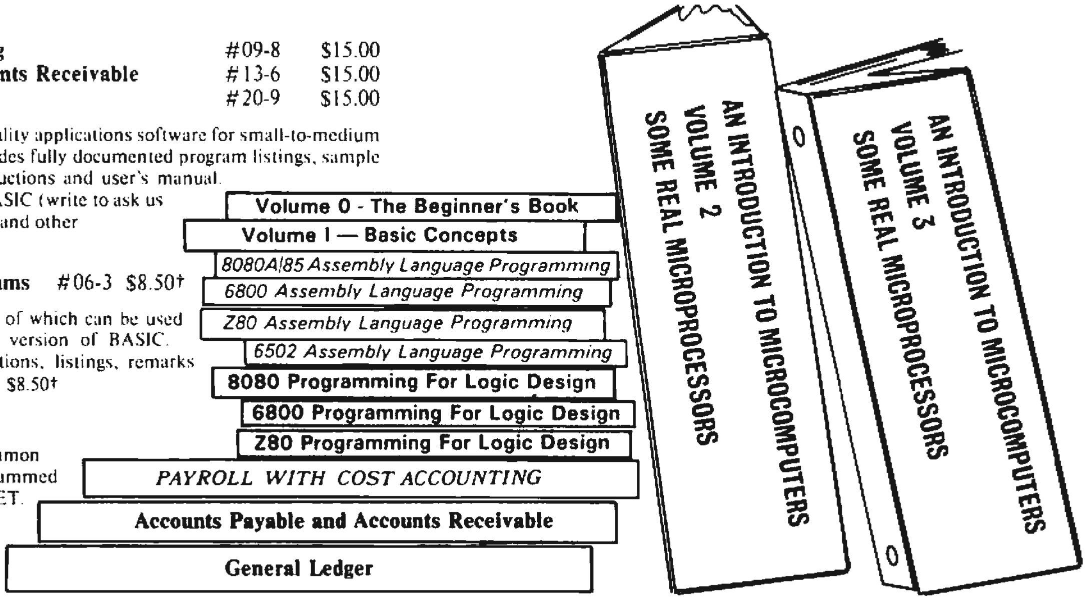

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site sides. Given a, b, C; find A, B, c. The solution can be written as:

$$\begin{aligned}&\text{Call BB 1 } (b, 0, C; t1, t2)\\ &\text{Call R}\to\text{P } (a - t1, t2; c, B) \qquad \textit{(Eq 16)}\\ &A = 180^\circ - B - C\end{aligned}$$

The ts are intermediate answers. As a test case: a = 50, b = 70.71, C = 105°; get A = 30°, B = 45°, and c = 96.59. This test case is in listing 3. The derivation of this algorithm is left as an exercise for the reader; start from the equations in any trigonometry book.

As a somewhat more difficult example, consider the problem Volder (1959) originally solved: given the latitudes and longitudes of two points on the earth, find the great circle distance between them and the initial heading. This problem comes up, for example, in long-distance ham radio in determining where to point the antenna beam. Given the longitude λ_1 (west longitudes are +) and latitude ϕ_1 (north latitudes are +) of station 1 (home) and the longitude λ_2 and latitude ϕ_2 of station 2, the algorithm below calculates A, the initial heading or pointing angle (north reference clockwise azimuth) from station 1 toward station 2, and D, the great circle distance between stations.

$$\begin{aligned}&\text{Call BB 1 } (1, 0, \phi_2; C2, S2)\\ &\text{Call BB 1 } (C2, 0, \lambda_1 - \lambda_2; t1, t2)\\ &\text{Call BB 1 } (t1, S2, -\phi_1; t3, t4) \qquad \textit{(Eq 17)}\\ &\text{Call R}\to\text{P } (t4, t2; t5, A)\\ &\text{Call R}\to\text{P } (t3, t5; t6, d)\end{aligned}$$

As a test, $t6$ = 1. The angle d is the distance D in angular units. If d is in degrees, multiply by 60 to get D in nautical miles; by 69.1 to get statute miles; or by 111.2 to get kilometers. This algorithm is approximate because it assumes a spherical earth. As a test case: λ_1 = 71.05°, ϕ_1 = 42.367° (Boston), λ_2 = 70.667°, ϕ_2 = −33.417° (Santiago de Chile on the west coast of South America); get A = 179.7° (slightly *east* of south) and D = 5237 statute miles. This test case is shown in listing 4.

The derivation of this algorithm is also left as an exercise for the reader. [As a hint: two approaches are possible. One approach begins with figure 6 in Smart (1962) and uses spherical trigonometry. Another approach, mentioned by Volder (1959), uses rotation matrices and views the problem in terms of coordinate transformations. Calculator algorithms for this and some similar problems are in Ball (1978), appendix A.7.] ■

```
RUN
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 1
TYPE X, Y, THETA ? 70.71? 0? 105
X' = -18.3009 , Y' =  68.3011
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 3
TYPE X, Y ? 68.3009? 68.3011
R =  96.5922 , PHI =  45.0001
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ?
STOP @ 80
PRINT 180-45.0001-105   29.9999
```

Listing 3: Test case solution to a side angle side triangle problem.

```
PRINT 71.05-70.667   .383
RUN
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 1
TYPE X, Y, THETA ? 1? 0? -33.417
X' =  .834679 , Y' = -.550739
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 1
TYPE X, Y, THETA ? .834679? 0? .383
X' =  .83466 , Y' =  5.57898E-3
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 1
TYPE X, Y, THETA ? .83466? -.550739? -42.367
X' =  .245545 , Y' = -.969374
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 3
TYPE X, Y ? -.969374? 5.57898E-3
R =  .96939 , PHI =  179.67
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ? 3
TYPE X, Y ? .245545? .96939
R =  1 , PHI =  75.7858
TYPE 1 FOR BB1, 2 FOR BB2, OR 3 FOR R->P ?
STOP @ 80
PRINT 75.7858*69.1   5236.8
```

Listing 4: A test case for the algorithm that gives great circle distance and heading between points on the earth.

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Keeping these possibilities in mind, let us examine the problem of developing a program to enable the computer to play tic-tac-toe with the user.

The game of tic-tac-toe at first appears to be a trivial game. New players quickly learn that a game played rationally by both sides must end in a draw. But being unbeatable does not mean you have mastered the game. The skilled player sets traps in the form of forks so that there are two ways to complete a row of three, only one of which can be blocked by the opponent. There are 15,120 different sequences for the first five moves alone, counting rotations and reflections, but these may be reduced to a manageable number of possibilities. There are only three basic opening moves: center, side, and corner. The corner opening is strongest; only by taking the center can the second player avoid an immediate trap. With a side opening or with a center opening, the second player has four choices to avoid an immediate trap. For the side opening game, these safe choices are the three adjacent cells or the opposite side. For the center opening game, the safe choices are the four corners.

There are a number of tic-tac-toe programs already available, so why write another one? Many of these programs play a very passive game, and some even allow the user to win. If the user can win, it follows that the computer response was a mistake. Actually, the computer response may be a mistake even if it does *not* allow a user win (it may fail to take advantage of an opportunity to set a trap). I have designed an aggressive program that allows no user wins, and that takes every possible opportunity to set a trap. The user has to play a perfect game to get even a draw.

System Considerations

It is assumed that either a printer or a video terminal is to be used for input and output. The user's responses to program questions may be entered as Y or N (for yes or no), and user moves during the game may be entered as single digits 1 thru 9. Each digit represents one of the nine cells of the playing board (see figure 1a). The printer or video terminal allows a 2-D display of the tic-tac-toe playing board, including the positions of all computer and user moves.

Program Planning

There are several possible ways of programming a tic-tac-toe game. One way is to identify all possible board configurations (as is done in the game of Hexapawn) and then to make the proper response for each configuration. For tic-tac-toe, this would involve an unreasonable number of possibilities. Another approach is to check the center cell, take it if it has not been taken, and otherwise take a corner cell, etc. This leads to a passive and irrational game. The algorithm used in my program is as follows:

1. Randomly select a center, side, or corner opening move.
2. Check the user's response to be sure it is a legal move before entering it onto the board.
3. Based upon the user's response, select a sequence of forcing moves so that the user must next make a predetermined move or lose the game.
4. If possible, set a trap (fork).
5. For variety, randomly select alternate strategies for setting traps.
6. After either a computer win or a draw game, print an appropriate message (remember that it is not possible for the user to win).

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There are a number of special cases that complicate things. The program must correctly handle *all* possibilities.

Implementation

The program first checks to see if the operator needs instructions for playing the game. If so, they are printed out, including a tic-tac-toe board with the number of each cell indicated. Note that the board array (B), which holds the contents of all nine board cells, is not a string array; instead, the number which corresponds to the desired ASCII character is stored and then converted to an ASCII character at board display time.

Program initialization is necessary to insure that the first and all subsequent games start off correctly. The initial computer move is selected by using the RND function,

Text continued on page 202

Listing 1: Tic-tac-toe program written in BASIC.

```
10  PRINT " *** RATIONAL TIC-TAC-TOE ***"
20  REM
30  REM    A PROGRAM BY D D HINRICHS IN TDL 8 K BASIC
40  REM                              APRIL 1977
50  PRINT
60  INPUT "DO YOU WANT INSTRUCTIONS (Y OR N)  " ; A$
70  IF A$ = "N" THEN 230                    : REM SKIP INSTRUCTIONS
80  N = 48
85  FOR I = 1 TO 9
90  B(I) = N + I                            : REM SET EACH BOARD CELL TO ITS NO.
100 NEXT I
110 PRINT
120 PRINT "THIS PROGRAM PLAYS AN AGGRESSIVE GAME OF TIC-TAC-TOE.  IF"
130 PRINT "YOU MAKE ANY MISTAKE, THE COMPUTER WILL WIN.  IF YOU PLAY"
140 PRINT "A PERFECT GAME, YOU WILL GET A DRAW.  THE PLAYING BOARD IS"
145 PRINT "DISPLAYED AS FOLLOWS:"
150 GOSUB 1780                              : REM DISPLAY PLAYING BOARD
160 PRINT
170 PRINT "TO MAKE YOUR MOVE, ENTER THE DIGIT (1 - 9) THAT REPRESENTS"
180 PRINT "THE BOARD CELL YOU WISH TO OCCUPY, THEN ENTER A CARRIAGE"
190 PRINT "RETURN.  THE COMPUTER WILL THEN CALCULATE ITS RESPONSE AND"
195 PRINT "DISPLAY THE UPDATED BOARD.  AT THE START, THE COMPUTER WILL"
200 PRINT "RANDOMLY CHOOSE A CENTER, CORNER, OR SIDE OPENING MOVE."
205 PRINT
210 PRINT "COMPUTER MOVES ARE:              X"
220 PRINT "YOUR MOVES ARE:                  O"
230 F = RND(-1)
250 DATA 4,6,8,2,3,7,0,9,0,0,  7,3,1,4,9,3,7,6,9,4
260 DATA 2,8,6,4,1,9,0,7,0,0,  1,9,3,7,2,7,3,8,9,2
270 DATA 9,1,8,2,7,3,7,1,2,9,  8,2,1,9,6,4,0,3,0,0
280 DATA 9,1,6,3,4,1,9,7,4,3,  6,4,2,8,7,3,0,1,0,0
290 DATA 5,8,7,3,6,4,0,9,0,0,  5,8,6,4,1,9,0,7,0,0
300 DATA 1,3,5,9,8,5,8,3,1,7,  1,3,7,4,6,0,9,0,8,0
310 DATA 3,1,5,7,8,5,8,3,1,7,  1,3,5,8,9,0,0,0,0,0
320 DATA 1,5,7,4,6,3,6,5,7,4,  3,1,5,8,7,0,0,0,0,0
330 DATA 4,7,5,6,9,5,9,7,4,3,  9,5,7,8,4,7,4,9,5,8
340 DATA 5,9,2,8,3,3,2,9,5,6,  5,9,3,2,7,2,3,5,8,9
350 DATA 2,3,5,8,9,9,5,3,2,6,  3,2,5,9,7,7,4,5,3,9
360 DATA 7,4,3,5,2,3,2,7,4,5
440 REM
450 REM  ENTRY POINT TO INITIALIZE FOR A NEW GAME
455 RESTORE                                 : REM  RESET DATA POINTER TO START
460 E = 0
465 F = INT(RND(1)*2)                       : REM  SET FLAG TO 0 OR 1
470 G = 1
475 H = 0
480 C1 = 10
490 C2 = 10
500 N = 0
510 FOR I = 1 TO 9
520 B(I) = 32                               : REM  SET BOARD CELLS TO BLANKS
530 NEXT I
550 REM  INITIAL COMPUTER MOVE IS 0, 1, OR 2  (0 THEN CHANGED TO 5)
570 C = INT(RND(1)*3)                       : REM  SELECT INITIAL MOVE
580 IF C = 0 THEN C = 5                     : REM  CENTER OPENING GAME
590 U = 10 - C                              : REM  PUT COMPUTER MOVE IN CELL,
600 GOSUB 2100                              : REM  DISPLAY BOARD, ACCEPT 1ST USER MOVE
630 IF C = 5 THEN 1720                      : REM  CENTER OPENING GAME
640 IF C = 2 THEN 1320                      : REM  SIDE OPENING GAME
650 IF U = 5 THEN 940                       : REM  CORNER GAME, 1ST USER MOVE 5
670 R = 10 * U + 140                        : REM  FIND RESPONSES FOR CORNER GAME
680 IF U  >  5 THEN R = R - 10
700 E = 1                        : REM  REENTRY POINT FOR 5-UNIT RESPONSES
720 IF F = 1 THEN R = R + 5
740 F = 1                        : REM  REENTRY POINT FOR 7-UNIT RESPONSES
742 IF R = 0 GOTO 770
745 FOR I = 1 TO R
750 READ C                       : REM  INCREMENT DATA POINTER TO 1ST RESPONSE
760 NEXT I
```

Listing 1 continued on page 200

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Listing 1 continued from page 198:

```
770 REM  REENTRY POINT FOR LOOP TO SELECT COMPUTER RESPONSES
780 F = F - 1
790 F = F * F                    : REM  FLIP FLAG (0 TO 1 OR 1 TO 0)
800 READ C                       : REM  SELECT COMPUTER RESPONSE FROM LIBRARY
810 C2 = C1
820 C1 = C                       : REM  UPDATE PREVIOUS COMPUTER RESPONSE
830 N = N + 1                    : REM  INCREMENT RESPONSE NO.
840 IF C = 0 OR C = U THEN 770   : REM  IF SPACER OR MATCH, TRY AGAIN
850 B(C) = 88                    : REM  PUT COMPUTER MOVE IN CELL
860 IF C2 = 0 OR C = H THEN 1160           : REM DRAW GAME
870 IF F = 1 THEN 2070                     : REM COMPUTER WINS
880 IF E = 0 THEN 900
890 IF N = 5 THEN 2070                     : REM  COMPUTER WINS
900 GOSUB 1780                   : REM  DISPLAY UPDATED BOARD
910 GOSUB 1980                   : REM  ACCEPT NEXT USER MOVE
920 GOTO 770                     : REM  LOOP TO SELECT NEXT RESPONSE
930 REM
940 REM  CORNER OPENING GAME, FIRST USER MOVE WAS 5
950 U = 1                        : REM  PUT COMPUTER MOVE (9) IN CELL,
960 GOSUB 2100                   : REM  DISPLAY BOARD, ACCEPT 2ND USER MOVE
970 IF U = 3 OR U = 7 THEN 1220  : REM  SECOND USER MOVE IS 3 OR 7
980 IF U = 4 OR U = 8 THEN G = 0 : REM  SECOND USER MOVE IS 4 OR 8
990 GOSUB 2100                   : REM  CALC RESPONSE, DISPLAY, 3RD MOVE
1030 C = 7
1040 IF G = 0 THEN C = 3         : REM  SET UP TRIAL COMPUTER MOVES
1050 IF C < > U THEN 2060        : REM  TRIAL CORRECT, COMPUTER WINS
1060 GOSUB 2100          : REM OTHERWISE, CALC RESPONSE, DISPLAY, 4TH MOVE
1090 IF G = 0 THEN 1130
1095 C = 2
1100 IF B(2) < > 32 THEN C = 6   : REM  SET UP TRIAL COMPUTER MOVES
1110 IF B(C) = 32 THEN 2060      : REM  TRIAL CORRECT, COMPUTER WINS
1120 GOTO 1150
1130 C = 4
1135 IF B(4) < > 32 THEN C = 8   : REM  SET UP TRIAL COMPUTER MOVES
1140 IF B(C) = 32 THEN 2060      : REM  TRIAL CORRECT, COMPUTER WINS
1150 C = 10 - U                  : REM  CALC FINAL MOVE FOR DRAW GAME
1155 B(C) = 88                   : REM  PUT COMPUTER MOVE IN CELL
1160 GOSUB 1780                  : REM  DISPLAY BOARD FOR DRAW GAME
1163 PRINT
1167 PRINT "CONGRATULATIONS - YOU GOT A DRAW THAT GAME"
1170 INPUT "DO YOU WANT TO PLAY ANOTHER GAME (Y OR N)"; A$
1180 IF A$ = "Y" THEN 450        : REM  GO TO START NEW GAME
1190 PRINT
1195 PRINT "SO LONG UNTIL NEXT TIME THEN"
1200 STOP
1210 REM  CORNER OPENING GAME, 1ST USER MOVE 5, 2ND USER MOVE 3 OR 7
1220 C0 = 2
1230 IF U = 3 THEN C0 = 4        : REM  SET UP TRIAL COMPUTER MOVES
1240 GOSUB 2100          : REM  CALC RESPONSE, DISPLAY, ACCEPT 3RD USER MOVE
1250 C = C0
1260 IF U = C THEN C = C + 4     : REM  ADJUST TRIAL COMPUTER MOVES
1270 GOTO 2060           : REM  COMPUTER WINS WITH ADJUSTED TRIAL MOVE
1310 REM
1320 REM  SIDE OPENING GAME REENTRY POINT
1330 IF U = 8 THEN 1420          : REM  SKIP IF FIRST USER MOVE IS 8
1340 R = 10 * U + 60             : REM  FIND RESPONSES FOR SIDE GAME
1350 IF U = 1 THEN R = 80
1360 IF INT(U/2) = U/2 THEN 700  : REM  RETURN TO SELECT RESPONSES
1370 IF U > 6 THEN E = 1
1380 GOTO 740                              : REM  RETURN TO SELECT RESPONSES
1400 REM
1410 REM  SIDE OPENING GAME, FIRST USER MOVE IS 8
1420 B(9) = 88                             : REM  COMPUTER RESPONSE IS 9
1430 GOSUB 1780                            : REM  DISPLAY UPDATED BOARD
1440 GOSUB 1980                            : REM  ACCEPT SECOND USER MOVE
1450 IF U < 4 THEN 1560
1460 IF U > 5 THEN 1630
1470 B(3) = 88                             : REM  COMPUTER RESPONSE IS 3
1480 GOSUB 1780                            : REM  DISPLAY UPDATED BOARD
1490 GOSUB 1980                            : REM  ACCEPT THIRD USER MOVE
1500 C = 1
1510 IF U = 1 THEN C = 6                   : REM  COMPUTER RESPONSE IS 1 OR 6
1520 GOTO 2060                             : REM  COMPUTER WINS
1540 REM
1550 REM  SIDE OPENING GAME, 1ST USER MOVE IS 8, 2ND USER MOVE IS 3 OR 1
1560 F = 0
1565 H = 6
1570 IF U < > 1 THEN 1600                  : REM  SET UP LAST 5 REPONSES
1580 F = 1
1590 H = 4
1600 R = 140                               : REM  SET RESPONSE ENTRY POINT
1610 GOTO 700                              : REM  RETURN TO SELECT RESPONSES
1620 REM
1630 REM  SIDE OPENING GAME, 1ST USER MOVE IS 8, 2ND USER MOVE IS 6 OR 7
1640 B(1) = 88                             : REM  COMPUTER RESPONSE IS 1
```

Listing 1 continued on page 202

1	2	3
4	5	6
7	8	9

Figure 1a: Cell numbers for the tic-tac-toe board.

```
     I   I
  O  I X I X
 ----+---+----
     I X I O
 ----+---+----
     I O I X
     I   I
```

Figure 1b: A typical printout of a tic-tac-toe board.

Text continued from page 198:

which calculates a random (actually pseudorandom) number between 0 and 1. This number is then multiplied by 3, and only the integer part saved to form a random 0, 1, or 2. Then 0 (later changed to 5), designates a center opening game, 1 a corner opening game and 2 a side opening game. Variable F (flag), which selects alternate computer strategies, is also randomly set to 0 or 1.

In this program, the response library is entered with DATA statements. The program's opening move and the initial user response are used to determine where to start reading in the response library. The library contains sequences of digits which represent the program's forcing moves. For 13 of the 24 possible combinations of opening move and user move, there are two possible winning strategies for the program, one of which is selected depending upon the status of variable F. Thus, even with the same opening move and the same initial user move, the program's responses may vary. Each of these winning strategies, which results in a fork, has five digits. These digits are selected sequentially for the program's responses. If the selected response is the same as the user's move, the user has blocked that row and the next digit is selected by using a loop. The digits in the even numbered positions and the fifth (last) digit represent winning responses, and control is diverted to a win routine which prints the board and the computer winning message.

Two more of the 24 possible combinations have only one strategy for a sure program win, but the program responses are handled in the same manner.

Six of the 24 possible combinations do not have a forced win strategy. These are handled by a 7 digit string of forcing moves that may end in a draw. These 7 digit strings have a 0 spacer inserted before the seventh digit to trigger diversion to the draw routine. The latter prints the board and a draw message after the seventh digit has been selected. A separate test causes a jump to the next digit if a zero spacer is detected as a program response.

That leaves three cases that require spe-

Listing 1 continued from page 200:

```
1650 GOSUB 1780                          : REM  DISPLAY UPDATED BOARD
1660 GOSUB 1980                          : REM  ACCEPT THIRD USER MOVE
1670 C = 3
1680 IF U = 3 THEN C = 5                 : REM  COMPUTER RESPONSE IS 3 OR 5
1690 GOTO 2060                           : REM  COMPUTER WINS
1700 REM
1710 REM  CENTER OPENING GAME REENTRY POINT
1720 R = U * 10 - 10                     : REM  FIND RESPONSES FOR CENTER GAME
1730 IF U > 5 THEN R = R - 10
1740 IF INT(U/2) = U/2 THEN 700          : REM  RETURN TO SELECT RESPONSES
1750 GOTO 740                            : REM  RETURN TO SELECT RESPONSES
1760 REM
1770 REM  DISPLAY SUBROUTINE TO PRINT UPDATED PLAYING BOARD
1780 PRINT
1790 PRINT TAB(4) "I   I"
1800 PRINT TAB(2) CHR$(B(1)) ; " I " ; CHR$(B(2)) ; " I " ; CHR$(B(3))
1810 PRINT "----+---+----"
1820 PRINT TAB(2) CHR$(B(4)) ; " I " ; CHR$(B(5)) ; " I " ; CHR$(B(6))
1830 PRINT "----+---+----"
1840 PRINT TAB(2) CHR$(B(7)) ; " I " ; CHR$(B(8)) ; " I " ; CHR$(B(9))
1850 PRINT TAB(4) "I   I"
1860 RETURN
1960 REM
1970 REM  SUBROUTINE TO ACCEPT AND CHECK NEW USER MOVE
1980 INPUT "YOUR MOVE IS " ; U
1990 IF  U < 1 OR U > 9 THEN 2030
2000 IF INT(U) < > U THEN 2030
2010 IF B(U) < > 32 THEN 2030
2020 B(U) = 79
2025 RETURN
2030 PRINT "YOUR MOVE IS ILLEGAL.  TRY AGAIN"
2040 GOTO 1980
2050 REM
2055 REM  ROUTINE FOR WHEN THE COMPUTER WINS THE GAME
2060 B(C) = 88                           : REM  PUT COMPUTER MOVE IN PROPER CELL
2070 GOSUB 1780                          : REM  DISPLAY BOARD FOR WINNING GAME
2075 PRINT
2080 PRINT " ***** I WON *****"
2090 GOTO 1170                           : REM  NEW GAME?
2100 REM
2110 REM  SUBROUTINE FOR COMBINED CALC, ENTERING, BOARD DISPLAY, USER MOVE
2120 C = 10 - U
2130 B(C) = 88
2140 GOSUB 1780
2150 GOSUB 1980
2160 RETURN
2170 END
```

cial handling. One is similar to the six cases of the preceding paragraph except that the last move is not a forcing move. To avoid a false win-test on the sixth (even) digit, zeros are inserted as spacers before the sixth and also before the seventh response digits.

The last two cases are more difficult, and somewhat similar. In each case it would be possible to use a series of forcing moves ending in a draw if the user simply blocked each potential row of three as it occurred. In each case, it is also possible to forego a first response forcing move, and instead to set a trap if the nonforced user move is not correct. I used the latter method in this program. This requires checking the second user move and then making the correct response to that move. A number of extra program steps are required to do this, but the program now plays a rational game.

Other Systems?

Some BASICs may not have some of the features used in this program, such as logical operators, ASCII code to character conversion, string variables, prompting INPUT statements, or PRINT TAB. These operations can normally be duplicated in other BASICs by slight program changes. If you would like a copy of this program in its Hewlett-Packard HP-67 programmable calculator form, send me two blank magnetic cards and a stamped, self-addressed envelope, and I will send it to you along with the slightly different instructions.

Conclusions

This game program exercise demonstrates the programming requirements for even a fairly simple problem:

1. Thoroughly evaluate the problem, to be sure that all possibilities are allowed for.
2. Consider the limitations and special features of the system to be used.
3. Decide exactly what you want to program to do, and then program to do it in a logical, straightforward manner.
4. Plan for ease of input and clarity of output.
5. Document so that others (and yourself at a later date) can readily understand the program.

In programming for this game, you may have found some pointers on logic and program planning. In any case, the completed program may be used to demonstrate system operation while entertaining your family and friends.■

Clubs and Newsletters

The Birmingham Microprocessor Group Computer Club

The Birmingham Microprocessor Group Computer Club meets on the fourth Sunday of each month. Meeting time is 2 PM at the Park Memorial Branch of the public library, 1814 11th Av S, Birmingham. The rear entrance to the building should be used. Membership dues are $6 per year which includes their newsletter. For more information, write POB 8072, Birmingham AL 35218

New Apple Computer Club in North Carolina

A new Apple computer club, the Carolina Apple Core, has been founded in the Durham-Raleigh-Chapel Hill NC area. The meeting format consists of monthly meetings on the third Tuesday of each month at different locations. Annual dues are $5 with a monthly newsletter and software library developing. At least two Apple computers with dual disk drives will be attendant at each meeting Dynamic programs featuring Apple captions are scheduled monthly, with seminars on Apple topics scheduled at other times during the month for the novice or the professional. The club is interested in exchanging information and software with other clubs. Contact Carolina Apple Core, 5212 Inglewood Ln, Raleigh NC 27609.

MUMPS Users Group

In an attempt to reach a larger MUMPS area, the MUMPS Users Group has switched to a controlled circulation magazine format The intention is to publish the magazine quarterly with each issue featuring a major MUMPS applications package, a number of unique applications, facts on new implementations, information on the annual meeting and on available MUMPS tutorials, and whatever items prove of interest to the readers. For more information about the MUMPS Users Group, write to POB 208, Bedford MA 01730

Triangle Amateur Computer Club

The TACC (Triangle Amateur Computer Club) in Raleigh NC is dedicated to the advancement of interest in amateur or personal computers Membership is open to all who support these ideas. The club meets on the last Sunday of the month at 2 PM in the Dreyfus Auditorium, Research Triangle Institute, Research Triangle Park NC For further information about the club, write POB 17523, Raleigh NC 27514.

Apple Users Group in Boston Area

The Boston area now has its own Apple Computer Users Group. NEAT (New England Apple Tree) supports a regular newsletter containing the latest information in the world of Apple, programming tips and techniques, program listings, reviews, tutorials, and more. Monthly meetings are held the third Wednesday of each month in the Mitre Corp cafeteria, Rt 3, Bedford MA, for software exchange, information sharing, and guest speakers. They also have available software for the Apple Annual dues are $6. For further information, contact Mitch Kapor, 31 Birch Rd, Watertown MA 02172.

Boston Computer Society Membership Increases 281%

According to the latest issue of The Boston Computer Society newsletter, the *BCS Update*, their club's membership has increased from 80 to 225 members in a five month period. Congratulations! The club has a wide range of interests, ideas and interesting people. New computers and programs are displayed at meetings, rumors and facts are exchanged, free magazines and information are available, and guest speakers keep members up to date with new systems and applications. Additionally, the club fosters a PET user group. For meeting information, write to The Boston Computer Society, 17 Chestnut St, Boston MA 02108.

Attention French Computer Enthusiasts

A new club called Microtel-club for the hobbyists in microcomputer and telecommunication areas has been formed in France Their intentions are to develop the interest of the French population in these technical areas, to give the members the chance to use and compare microcomputers, to support the most interesting projects of its users, and to promote the exchanges between them. More than ten Microtel-clubs exist in France In Paris the club owns six microcomputers, many training kits, a library, and three laboratories with electronic equipment. The club is open every day and a newsletter is published twice a month A new Microtel-club will be formed in Palo Alto CA to develop exchanges between France and the United States The membership cost is $35 per year For further information, write Microtel-club Administration, 9 rue Huysmans, 75006 Paris FRANCE 0 544 70 23.

Newsletter for ProcessorTechnology Computers

Proteus/News, formerly *Solus News*, is an independent newsletter for owners and users of Processor Technology Corporation computers. A sampling of the content of this one page newsletter includes: a "Review of PTDOS 1 5", "An Introduction to Programming in Pascal", a book review of *45 BASIC Programs* by Didactix; "Development of the SLAC Pascal Compiler"; description of the SLAC Pascal Solus/Cuter utilities; and other features The bimonthly subscription rate is $12 per year. Contact *Proteus*, 1690 Woodside Rd, Suite 219, Redwood City CA 94061

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The 8080 Etc compatible users group has expanded its services to both the personal computer user and commercial firms. Free access to over 85 types of business, medical, accounting, research, and hobby software programs is offered to members who have a communications modem Acoustic couplers or the IDS card for the S-100 bus are recommended and they must be set at the transmission rate of 300 bps The system can be accessed by dialing (209) 638-6392 and typing the following passwords: Hello-w101, 8080 Etc The users group also publishes a quarterly journal of group activities and general debugging notes and always has need for tidbits and notes from members or interested people. For a free list of program titles, send a self addressed stamped envelope and include the type of system and specific components, along with any questions to Membership, The 8080 Etc, POB 894, Fresno CA 93714.

Microcomputer Business Users Group

BUG (The Microcomputer Business Users Group) is an association of business men and women and data processing professionals who meet monthly to educate themselves about the methods of achieving solutions to business problems with microcomputers. The primary emphasis is upon education related to application software, although system software and hardware get some attention Vendors are invited to speak and are encouraged to give educational talks. The group is geared towards end users and vendors or prospective vendors of software The BUG newsletter keeps members informed about activities, happenings, forthcoming speakers, hearsay information and previous meetings. Meetings are held 7 PM on the first Tuesday of each month at Baruch College, 46 E 26 St, New York NY (3rd floor computer library) Contact The Microcomputer Business Users Group, 161 W 75 St, New York NY 10023

Chicago TRS-80 Users Group

TRS-80 users in Chicago will be pleased to know of the existence of the Chicago TRS-80 Users Group (Chicatruc). The group meets the third Wednesday of every month and a monthly newsletter is available to members who have paid the $9 membership fee. Contact Emmanuel B Garcia Jr and Associates, 3950 N Lake Shore Dr, Apt 2310, Chicago IL 60613

BYTE's Bugs

FFT BASIC Problem

Some users have experienced problems in running the BASIC program from "Fast Fourier Transforms on Your Home Computer" by William D Stanley (December 1978 BYTE, page 14). The difficulties are caused by differences in the behavior of BASIC interpreters when they encounter additional statements on the same line following an IF-THEN statement

Many BASIC systems act in this manner. in cases where the condition tested by the IF is false, program flow proceeds to the next line of the program, skipping over additional statements on the same line as the IF-THEN (following the colon or backslash). However, some BASICs will execute statements on the same line as the IF-THEN, even if the condition is false.

If you have the second type of BASIC interpreter, the following program line must be inserted for the program to run correctly.

```
1075 IF C > X4 THEN 1090
```

[Thanks to Dana Tremblay, 178 County St, Apt 6, Attleboro MA 02703, for pointing out this problem.] ■

APL and the Greatest Common Divisor

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I read the article "Pascal versus BASIC: An Exercise" in August 1978 BYTE, page 168. Upon examining the Pascal, BASIC and FORTRAN listings on page 172 for the greatest common divisor between two integers, I was curious about how an APL program would compare. I submit my APL version in listing 1 (several example runs are shown in listing 2). A detailed step by step analysis of the APL program is given which shows some of the power inherent in the APL language.

Analysis of Program

The explanation is given for the function `GCD 6 8 14`. The greatest common divisor among a series of integers as contained in vector *V* is necessarily less than or equal in magnitude to the smallest one of the integers. The smallest integer is easily selected in APL using the floor reduction `⌊/V`, which in our example would result in selecting the number 6. One could proceed by dividing all of the elements of *V* by this smallest integer and testing each division for a remainder of 0. This again is easily implemented using `∧/((⌊/V)|V)=0` , wherein, for our example, the 6 residue of vector 6 8 14 given by `6| 6 8 14` returns the vector 0 2 2. When this vector is logically equated to 0 the vector 1 0 0 results. The logical AND reduction of this vector `∧/1 0 0` returns the number 0. One could next subtract 1 from the smallest element, 6, and repeat, whereupon one would find that `∧/(5|6 8 14)=0` also returns the number 0. Obviously, the first integer in the decreasing series of integers thus obtained that returns the number 1 will be the greatest common divisor.

In our example `⍳6` gives the vector 1 2 3 4 5 6. Thus if we reverse this vector, we have the desired elements for successive divisors. This is done in APL for our example using the vector reversal `⌽⍳6`. This gives the vector 6 5 4 3 2 1.

The outer product in APL is called out by the two symbols " `∘.` ", precisely the operation needed here since the outer product will take each of the elements on the left and apply it in turn to the primitive function on the right. Thus in our example, `6 5 4 3 2 1 ∘.| 6 8 14` returns the matrix:

```
0  2  2
1  3  4
2  0  2
0  2  2
0  0  0
0  0  0.
```

When this matrix is logically compared to 0 we obtain:

```
1  0  0
0  0  0
0  1  0
1  0  0
1  1  1
1  1  1.
```

The AND reduction, `∧/` , applies to the rows of a matrix. Hence we will return in our example the vector 0 0 0 0 1 1 when applied to the last matrix above. The position of the first 1 that occurs in this vector will reference the position in the vector of divisors `(⌽⍳⌊/V)` . If this position index is appended as a subscript, `(⌽⍳⌊/V)[ . .index . . ]`, the greatest common divisor will be displayed. The first occurrence of 1 in the vector for our example is obtained by the dyadic use of the index operator iota on the vector 0 0 0 0 1 1 ⍳ 1, which returns a 5. The fifth element of vector 6 5 4 3 2 1 is 2, which is the greatest common divisor of 6 8 14.■

```
      ∇ GCD V
[1]   'GCD= ',⍕(⌽⍳⌊/V)[(∧/((⌽⍳⌊/V)∘.|V)=0)⍳1]∇
```

Listing 1

```
      GCD 391 238 1887 1003
GCD= 17

      GCD 637 735 343 49 6468
GCD= 49

      GCD 6 8 14
GCD= 2
```

Listing 2

APL Aids Instructors

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Fortunately, I did not know that APL was unsuitable for computer aided instruction, so I started using it four years ago. It works fine. Professor Gerhold's "Teaching with a Microcomputer" (December 1978 BYTE, page 124) falls far short of convincing me that I should learn another special purpose language just to handle computer aided instruction.

Professor Gerhold found the interpretation of responses to simple yes-no questions formidable in BASIC. None of my programs ask that kind of question as part of the instruction, but rather as the start up routine. Here's how I handle it:

```
[10] →SK×ι'N'=1↑⍞,⎕←
'WANT YOUR MISSION ORDERS?'
```

I don't try to handle variants of expression because I find that beginning students, told to answer yes or no, do it. I haven't protected against expressions like yesterday, yetti, or you blasted idiot, because I've never seen inexperienced students answer that way. Semisophisticated students may try to spoof the system with things like that, but as far as I am concerned, they are welcome to whatever they get.

When I present a question calling for a word or two as response, I use a function that tests for the presence of key letters in specified order. Thus, a judicious selection of key letters makes the function tolerant of some misspelling and typographical errors. The function checks the list of alternatives and responds differently depending on whether the response matches the first or one of the subsequent alternatives.

Professor Gerhold believes that such a function would be too slow. I find no basis for that belief. On a Sigma-9 in a timesharing environment with 30 users, the function has no discernable impact on terminal response time. Under those conditions the response time does not exceed the carriage return time and so is perceived as immediate. If a dedicated microprocessor can't match that, I am going to be disappointed.

Aside from permitting me to work in a familiar and powerful language, using APL for computer aided instruction allows me to use functions already developed. For example, when I need to plot histograms, I simply copy the histogram function from my statistical workspace. This came in handy in the writing of my StarTrek game in which I had to figure a confidence interval for the mean, in order to spread the phaser enough to have a reasonable chance of hitting the Klingon.

A third advantage of APL is that it lets me write complex programs very easily.■

The Problem of Software Piracy Revisited: A Proposal

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One of the greatest problems facing individuals who own computers is to legally acquire inexpensive, high quality software. The fact that it is often possible to acquire such software for free illegally is one of the reasons we have the problem, for if a paying market existed, some extremely useful programs would be written for it. (There are rumors that Bell Labs LSI-11 UNIX may never be released: if it costs hundreds of

Circle 179 on inquiry card.

thousands of dollars to develop a system which can then be stolen and sold for \$10, there is scarcely a reason to market it at \$500 to \$1000, prices that would yield a good profit on an "honest" market.)

Most illicit copying is done casually and in a spirit of friendly (nonprofit) cooperation between fellow users. I believe that the following suggestion, if adopted by sellers of major software products, would drastically reduce the risk of such copying.

Let P be the price the seller has currently put on one unit of his or her product. (P would be related to the seller's estimate of what the traffic could bear if no illicit copying were possible.) When customers buy the product, they have the option of naming (on the sales form) any person who is already a registered purchaser of the software. The person so named would then receive an rP dollar "software bounty" from the seller, where r is a number between 0 and 1 announced by the seller when the product is introduced. (It might take some experience to decide the best value for r. My opinion is that some value greater than 0.5 would be optimum for the seller. The price P could be changed with time, but a fixed r would help consumers maintain confidence in the bounty.)

The rP software bounty would have many effects. Suppose Tom buys the product. If he can convince Jan to buy, Tom can recover a substantial portion of his expense (assuming that r is reasonably large). But why would Jan name Tom on the sales form? Presumably because Tom has promised Jan some fraction of the bounty; that is their affair. If Tom is an enterprising individual (and if the product is much in demand) then he might be able to recover his entire purchase cost and possibly make more.

Of course, Jan and all the others that Tom has won bounties on may be doing the same thing. This is a secondary effect of the scheme. It turns present marketing realities upside down: the software bounty would reward those who purchase early, and leave procrastinators with the risk that there may be no bounties left to win when they get around to buying.

Notice that although the arrangements between customers and prospective customers may be quite complicated and novel, the situation would be simple for the seller. He or she must keep a mailing list of registered purchasers—also necessary for sending out software updates and maintenance fixes. If n units are eventually sold, the seller will receive at least nP - (n-1)rP for his efforts. (If P changes with time, the result is only slightly more complicated.)

The software bounty scheme will not stifle those whose moral fiber is not merely weak, but nonexistent. An outright criminal who copies the product and sells it at a low price could make a lot of money. Two features of the plan might tend to discourage this, however. The person receiving the bounty must be named by the new purchaser on a bona fide sales form. Thus anyone buying a bootlegged product would know that he was doing so and would know that he could not obtain any bounties of his own; in fact, he would have to undertake equivalent criminal activity if he wished to make any money from disseminating the product. Secondly, outright bootlegging directly damages legitimate bounty hunters and is therefore more likely to be reported than under present marketing strategies.■

*A creative suggestion, to be sure. But if to purchase a score of a great symphony one had to pay the same amount as the original composer's stipend, very few people would have ever heard a number of masterpieces. A commission sales arrangement is exactly how such works of art are sold by a myriad of dealers — and there is no reason why software works of art cannot be sold on a similar basis. . . .*CH

Machine Language Puzzler

An Added Attraction

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Using any instructions in the Intel 8080 instruction set *except* ADD, ADI, ADC, ACI, and DAD, write a program that adds two 8 bit binary numbers. Assume that the addend and augend have been preloaded into the B and C registers, respectively. The sum should be located in the accumulator when the addition is completed, and then the processor should be halted. The program should have a minimum number of instructions and should execute with the greatest possible speed. Puzzle a bit on this problem and when you figure out how to do it, turn to page 217.■

Technical Forum

Periodic Answers

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I would like to comment on the question BYTE posed in reference to Jef Raskin's article "Unlimited Precision Division" (February 1979 BYTE, page 156). The question concerned decimal expansion of 99991/99989.

By using several tricks from *An Introduction to Number Theory* by Harold Stark, in conjunction with an HP-25 calculation to do 10 digit arithmetic, I found that the period of the decimal expansion of 99991/99989 is 99988.

The theorem states that for any pair of numbers m and n which have no factors in common except 1, and which have no common factors with 10, the rational number m/n has a purely periodic decimal expansion and the length of the period is ord_n (10). The function ord_n (10) is defined as follows (paraphrasing Stark):

> if 10^b leaves a remainder of 1 when divided by n, and b is the smallest positive integer for which this occurs, then ord_n (10) =b. For example, ord_{99} (10) =2 since 10^2 leaves a remainder of 1 when divided by 99. Therefore, by Stark's theorem, 1/99 has period 2 in its decimal expansion.

Stark also gives some hints which reduce the amount of work in finding the smallest working value of b. For the case n=99989, there are 11 candidates for b, of which only b=99988 works.

During all stages of the calculation, one cares only about the remainders after division by 99989, so a calculator that can handle 10 decimal digits is adequate.

Thanks for suggesting an interesting puzzle! ■

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A Hard Way to Hard Copy

Suppose you have glued a light emitting diode (LED) on each key of your typewriter, then connected those LEDs to the outputs of a decoder, then connected the decoder to the output ports of your favorite microcomputer. Each time a character is displayed on the output LED light, you push the key and the character is printed. You must not forget some auxiliary function indicators for things like space, new line, etc. I think it is the most economical way to obtain a good printout from a microcomputer or a personal computer. In my opinion the achievable speed is nearly two characters per second.

The cost of such an adaptation should be less than $25, assuming bargain basement LEDs and a typewriter you already own. It could be possible to extend the function by adding a touch contact on each key.

I have only one reservation: in a few years it might be more common to own a microcomputer than a typewriter.■

Other Early Computers

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Keith Reid-Green's article "A Short History of Computing" (July 1978 BYTE, page 84) neglected to mention a number of very significant machines. On reading the article one gets the impression that prior to this decade no computers were built outside the USA, and that any machine within the USA was in all probability built by IBM. Of course in a short article one cannot hope that a complete history will be presented, but I do not feel that the author presented a correct view of the development of computers.

Since my own knowledge of the history of computing is limited to mainly British machines, I too will no doubt leave out many machines that others would include. The following are some of the machines that I feel should have been mentioned:

- Konrad Zuse's electromagnetic computers built in Germany before and during World War II.

- The code breaking computers (COLOSSI) built in Bletchley Park England, during World War II.
- The Manchester University Mark 1 (1948) and the Cambridge EDSAC (1949). The Mark 1 was the first stored program computer. The first program written for it was to determine the highest proper factor of 2^{18}. It succeeded in solving this problem in a 52 minute run on June 21 1948. It used as memory the electrostatic Williams Tube which was later used under license by IBM for the 701 and 702 computers. The EDSAC machine introduced the concept of subroutines.
- Two transistorized computers were built at Manchester in 1953 and 1955. These machines led to the MV950 computer which was used commercially, six being built and used for a period of five years.
- The Atlas computer (1962). This was designed at Manchester by a team led by Prof Kilburn who was part of the team that built the Mark 1 and also wrote the program mentioned above. When Atlas was finished it was said to be the most powerful computer in the world and it introduced concepts such as paging and virtual storage. This machine was also sold to a number of users and one was still in full time use up to a couple of years ago. The machine made such an impression that even today the power of a computer is often quoted as so many Atlases.
- No mention was made of the Burroughs machines with their unique architecture.
- What ever became of DEC?

If any one is interested in a fuller account of the development of computing machines, there are several books that should be read. They are:

- *History of Manchester Computers* by S Lavington, published by the National Computing Center, Manchester England and distributed in the USA by The Hayden Book Company Inc, 50 Essex St, Rochelle Park NJ. This book describes the development and construction of all the computers built at Manchester University.
- *The Origins of Digital Computers: Selected Papers*, second edition B Randell (ed), published by Springer-Verlag, New York, 1975. This book contains many reprinted and some unpublished papers on the development of early digital computers.■

Compare New Processors Carefully

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I would like to compliment you on the article "A Microprocessor for the Revolution: The 6809, Part 1: Design Philosophy" by Terry Ritter and Joel Boney (January 1979 BYTE, page 14). Although most of us will never be in a position to design an LSI microprocessor, an article on design philosophy is quite appropriate. The same considerations faced by the microprocessor designer are faced by the system designer trying to choose the best microprocessor for his system, and the user (including the hobbyist) trying to choose the best system for his application.

Ritter and Boney do an excellent job of presenting the criteria to be used in judging a microprocessor, but their conclusions — that the 6809 is "the best 8 bit machine so far made by humans" and "definitely superior to the 8 bit competition" —are by no means beyond question. Their attitude can perhaps be excused by the fact that they are the proud fathers of a new "baby", but it has been said with considerable justification that there is no "best" microprocessor for all applications. It is unlikely that when the 6809 becomes available the situation will be any different. For example, Synertek's upgrade of the 6502, the 6516, could prove superior to the 6809 in many applications.

It is true, but perhaps not immediately obvious, that increasing the number of address modes available on a microprocessor does not necessarily make it more useful. The autoincrement and autodecrement modes, in particular, are powerful and appropriate on a 16 bit machine like the PDP-11, but they can actually decrease the power of an 8 bit machine by introducing two types of inefficiencies.

First, because an exotic instruction set requires a complex architecture, it increases both the die size (and cost) of the device and the overhead (instruction decode, internal transfers, and thus execution time) required to perform a given operation. Second, it necessitates the use of page prefixes or 2 byte op codes, because a single byte instruction does not have enough bits to describe all combinations of operations that can be performed. Thus, many 6809 instructions require four bytes to specify.

By contrast, the 6516's instruction set is more compact and includes only 8 bit op codes. Does this mean that it is less powerful than the 6809? Not necessarily. Ritter and Boney indicated that loads and stores were by far the most prevalent operations encountered in their static analysis of 6800 source code. The following example illustrates how the 6516 would handle a load autoincrement instruction for which it does not have a specific address mode. Similar sequences would be used for accumulator offset and PC (program counter) relative modes, and of course both the 6502 and 6516 have true indexed modes which operate much faster than the 6809's constant offset modes:

```
6809: LDAA ,Y+    ;load accumulator with con-
                  ;tents of location addressed
                  ;by Y, then autoincrement Y
                  ;requires two bytes and six
                  ;cycles.

6516: LAY         ;load accumulator with con-
                  ;tents of location addressed
                  ;by Y.
      INY         ;increment Y.
                  ;requires two bytes and four
                  ;cycles total.
```

In addition to requiring the same amount of memory and executing 50 percent faster, the unbundled 6516 approach is more flexible. Suppose the programmer wishes to use the same instruction but the index register is decremented after use. The 6516 code would be LAY, DEY but since the 6809 does not support postdecrement mode, a longer and slower sequence of instructions (four bytes and nine cycles) must be used.

For the most complex address modes (eg: LDAA [,–X]) the 6809 does have an advantage in memory and speed. Therefore, the user must determine if his application requires a large enough proportion of such operations to make the

6809 the most effective choice, remembering that *all* operations using the common address modes (direct and extended) require the same or fewer bytes of code and at least one less cycle of execution time on the 6516.

The next most frequent operations in Ritter and Boney's static analysis, after loads and stores, were subroutine calls and returns. A comparison of the two processors' capabilities in that area follows:

Type of Addressing	6809 Byte	6809 Cycles	6516 Byte	6516 Cycles
extended	3	8	3	5
rel, 8 bit	2	7	2	4
rel,16 bit	3	9	3	6
indirect	3	14	3	7
system	1/2	19/20	1	6/7
RTS	1	5	1	4
RTI	1	6/15	1	5
Other	all indexed modes available		address must be calculated	

As mentioned in the article, the use of software interrupts for breakpoints and operating system calls is a good programming practice. The 6809 provides three software interrupt instructions; two require two bytes and all save all registers on the stack. The 6516 has six BRK instructions; all 1 byte instructions. They save no registers for flexibility and speed, but only one byte and ten additional cycles are required, if necessary, to save all registers.

Authors Ritter and Boney indicated that a major effort was made to "clean up the 6800 instruction set and make it more consistent," and cite the instruction TFR R1, R2 as an example. It is not clear to me that remembering 42 combinations like TFR A,B, TFR X,Y is any easier than remembering 42 mnemonics of the form TAB, TBA, and TXY, and the 6809 user will pay a heavy price for such consistency. The TFR instruction requires two bytes and seven cycles for each register transferred, as opposed to one byte and one cycle on the 6516. Moreover, if the programmer insists on using a TFR type format, a 6516 assembler could certainly be written to accept it.

Another advantage of the 6516 is the 16 bit data handling capability. Aside from the ADDD, SUBD, and CMPD instructions, the 6809 has no facilities for computing with 16 bit data. All 6516

Technical Forum is a feature intended as an interactive dialog on the technology of personal computing. The subject matter is open-ended, and the intent is to foster discussion and communication among readers of BYTE. We ask that all correspondents supply their full names and addresses to be printed with their commentaries.

arithmetic and logical instructions (ADD, ADC, SUB, SBC, CMP, ORA, AND, EOR) operate on both 8 and 16 bit data. The 6516 can operate on two bytes in memory as a 16 bit quantity, using a single rotate, shift, increment, or decrement instruction. Equally important, the 6516's index registers can be used as 8 bit quantities for true indexing and counting applications, and data from memory can be added directly to the index registers for fast address calculations. Finally, the 6516 has a direct-page-indirect address mode which allows many pointers to be maintained entirely in memory without involving the index registers at all.

In short, I am not convinced that the 6809 is "definitely superior" and would suggest that careful consideration be given to the merits of all processors before such claims are made for any one of them. ■

Puzzling Rotation

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Listing 1.

```
10  PRINT
20  Y=0: X=INT((1/7)*1E+06)
30  FOR K=1 TO 7
40  Y=Y+X
50  PRINT Y
60  PRINT
70  NEXT K
80  END
```

The program in listing 1 is more a puzzle than a useful routine. The only practical application I can foresee would be to entice some computer hobbyist with more mathematical ability than I, to explain why the resulting numbers have the same digits in the same order. Does the same digit rotation occur for similar operations in other number bases?

Line 20 starts with a 6 digit integer formed from the first six digits of the reciprocal of that magic number, seven. This number is repeatedly added to itself to form a column of 6 digit numbers with curious properties.

I won't show these results here. You will have to try it on your computer. If your version of BASIC insists, you might have to enter 1E+06 in line 20 as 1000000. ■

Solution to Machine Language Puzzler (*See page 209*)

Addition can be performed without an ADD instruction by subtracting the *two's complement* of the addend from the augend. Specifically:

X + Y = X - (-Y) = X - Y*

where Y* is the two's complement of Y. A simple approach is as follows (assume that X is in register C, and that Y is in register B):

```
MOV A, B
CMA
INR A
MOV B, A
MOV A, C
SUB B
CMC
HLT
```

A shorter solution is not quite as obvious:

```
MOV A, B
CMA
SUB C
CMA
HLT
```
■

Circle 91 on inquiry card.

Circle 386 on inquiry card.

The Hobby Unwrap

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The Hobby Wrap Model BW-630 wire wrap gun, manufactured by the OK Tool Company, 3455 Conner St, Bronx NY 10475, is a useful tool for experimenters. One feature I missed, though, is the ability to unwrap wrong connections. The Hobby Wrap is powered by a DC motor run on two C cells. If the batteries are installed *backwards*, the motor runs in the *reverse* direction. It can then unwrap wire wrap connections. But removing the batteries and replacing them backwards is a very inefficient way to do unwrapping. Some better method of reversing battery polarity is required.

A double pole double throw (DPDT) switch can be used to change the polarity of the motor connections. The Hobby Wrap is dismantled by removing the two bolts and the metal ring around the battery compartment. I have found that a Radio Shack 275-407 (or equivalent) DPDT subminiature slide switch can be mounted in a cutout made in the thin plastic square at the

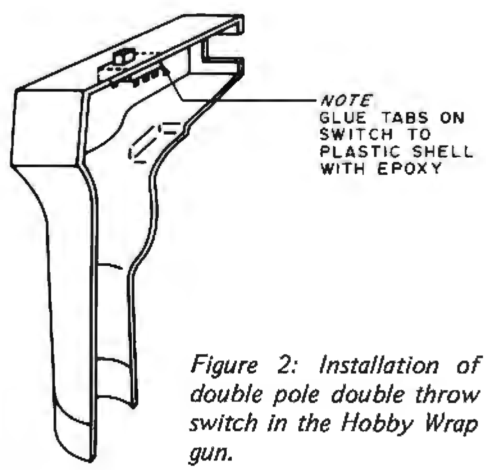
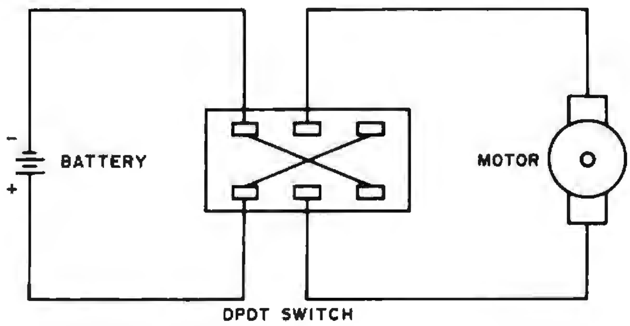


Figure 2: Installation of double pole double throw switch in the Hobby Wrap gun.

Circle 86 on inquiry card.

Figure 1: A modification to the Hobby Wrap Model BW-630 wire wrap gun manufactured by the OK Tool Company. A double pole double throw switch is used to reverse the direction of motor rotation, enabling the user to unwrap wire wrap connections.



rear of the top side of the tool. The switch should be mounted in the *left* half of the case (when viewed from the rear of the gun). This allows the right half to be removed completely without upsetting the battery connections. The slide switch is glued in position with epoxy, because mounting holes would be difficult to drill. The whole modification takes less than two hours.

Step by Step Instructions

1. Remove *right* half of case (two bolts and ring).
2. Remove motor (pop off rubber belt and gently remove motor from drive shaft).
3. Unsolder wires connecting the motor with the battery connectors.
4. Solder wires (30 gauge wire wrap) diagonally across the switch as shown in figure 1.
5. Solder two wires from the motor to the middle two contacts on the switch, and two wires from the battery connectors to one of the outer pairs of contacts on the switch.
6. Trim out the thin section of plastic on the *left* half of the case (figure 2) and glue the switch into this slot with epoxy.
7. Remount the motor, route the wires past the bolt hole, replace the right half of the case in its original position, and label the switch positions.

You now have an unwrapping tool whenever you need it. To unwrap, slide the switch to the unwrap position, place the tool over the wire wrap post as in wrapping, and press more firmly than usual while giving the motor a brief burst. The wrap should come right off.■

Circle 70 on inquiry card.

Programming Quickies

SwTPC 6800 Display Routine

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The SwTPC 6800 computer requires the use of the MIKBUG M function to load and display the contents of memory. The program in listing 1 allows immediate display or loading of X number of bytes, and is much easier on the programmer than the MIKBUG subroutines. I hope this program will be of some service to readers.■

Listing 1: 6800 program for displaying and reading X number of bytes.

```
                  *        CHANGE ALLOWS USER TTY INPUT OF MANY BYTES
                  *        AT ONCE. USE MIKBUG "G" FUNCTION TO JUMP TO
                  *        $0100, THEN TYPE IN THE FIRST ADDRESS . CHANGE
                  *        WILL DISPLAY THAT ADDRESS AND ITS DATA . . .
                  *
                  ****     DISPLAY MODE ****
                  *        ENTER A SPACE TO SHOW NEXT BYTE IF IN DISPLAY
                  *        MODE, OR TO ENTER NEXT BYTE IF IN LOAD MODE.
                  *
                  *        ENTER ";" INSTEAD OF SPACE TO SWITCH FROM
                  *        DISPLAY TO LOAD MODE OR VICE VERSA. IN EITHER
                  *        MODE, ENTERING A CARRIAGE RETURN STARTS A
                  *        NEW LINE.
                  ****     EXIT FROM THE PROGRAM ****
                  *        THE USER MAY EXIT AT ANY TIME FROM DISPLAY
                  *        MODE BY INPUTTING ANY CHARACTER EXCEPT ";",
                  *        SPACE, OR THE CARRIAGE RETURN . . .
                  *        EXIT FROM THE LOAD MODE BY TYPING IN AN ILLEGAL
                  *        BYTE. ALSO CAN GO BACK TO CHANGE ENTRY POINT,
                  *        FROM LOAD MODE, BY TYPING IN AN ILLEGAL USER
                  *        RESPONSE AFTER BYTE ENTRY
         E047     BADDR    EQU  $E047
         E055     BYTE     EQU  $E055
         E1AC     INCH     EQU  $E1AC
         E0CC     OUTS     EQU  $E0CC
         E1D1     OUTCH    EQU  $E1D1
         E0BF     OUT2H    EQU  $E0BF
         E0CA     OUT2HS   EQU  $E0CA
         E0C8     OUT4HS   EQU  $E0C8
         E07E     PDATA1   EQU  $E07E
                  *
                  *
A00C                 ORG $A00C
A00C     00       XHI      FCB  00
A00D     00       XLOW     FCB  00
                  *
1000                 ORG $1000
         1000     CHANGE   EQU  *        BEGIN WITH USER INPUT ADDRESS
1000     CE  1061          LDX  #STRING
1003     BD  E07E          JSR  PDATA1
1006     BD  E047          JSR  BADDR
1009     8D  46   CHA51    BSR  ADD0     PRINT CURRENT ADDRESS
100B     BD  E0BF CHA31    JSR  OUT2H    PRINT CURRENT DATA
100E     FF  A00C          STX  XHI
1011     BD  E1AC          JSR  INCH     GET USER RESPONSE
1014     81  20            CMPA #$20
1016     27  F3            BEQ  CHA31    IF RESPONSE " " THEN PRINT NEXT
                                         DATA BYTE
1018     81  0D            CMPA #$0D
101A     27  ED            BEQ  CHA51    IF RESPONSE CR THEN START NEW
                                         LINE
101C     81  3B            CMPA #';
101E     27  01            BEQ  CHA71    IF RESPONSE ";" THEN ENTER LOAD
                                         MODE
1020     3F                SWI           IF RESPONSE WAS NONE OF ABOVE,
                                         RETURN
                  *
1021     BD  E055 CHA71    JSR  BYTE     WAIT FOR USER INPUT OF TWO HEX
                                         CHAR
1024     09                DEX
1025     A7  00            STAA X        STORE IN LOCATION POINTED TO BY
                                         X 1
```

Listing 1, continued:

```
1027   BD  E1AC  CHA75   JSR   INCH      WAIT FOR USER DIRECTIVE
102A   81  20            CMPA #$20
102C   27  0A            BEQ   CHA81     ON SPACE INPUT PREP FOR LOAD
                                         ANOTHER BYTE
102E   81  3B            CMPA #';
1030   27  0D            BEQ   CHA91     TRANSFER BACK INTO DISPLAY MODE
1032   81  0D            CMPA #$0D
1034   27  0F            BEQ   CHA95     ON CARRIAGE RETURN PRINT NEW
                                         ADDRESS
1036   20  C8            BRA CHANGE      IF NONE OF ABOVE, GET NEW
                                         ADDRESS TO START
                         •
1038   08        CHA81   INX
1039   08                INX
103A   FF  A00C          STX   XHI
103D   20  E2            BRA   CHA71
103F   08        CHA91   INX
1040   FF  A00C          STX   XHI
1043   20  C4            BRA   CHA51
1045   8D  0A    CHA95   BSR   ADD0
1047   BD  E0BF          JSR   OUT2H
104A   09                DEX
104B   09                DEX
104C   FF  A00C          STX   XHI
104F   20  D6            BRA   CHA75
                         •
     1051        ADD0    EQU   •
1051   CE  1061          LDX   #STRING   PRINT "@",CR AND LF
1054   BD  E07E          JSR   PDATA1
1057   CE  A00C          LDX   #XHI
105A   BD  E0C8          JSR   OUT4HS
105D   FE  A00C          LDX   XHI
1060   39                RTS
                         •
1061   0D        STRING  FCB   $D,$A,0,0,'@,4
1062   0A
1063   00
1064   00
1065   40
1066   04
                 END

TOTAL ERRORS    0
```

6800 Register Display

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The program in listing 1 solves a major point of frustration for users of the 6800 processor with the MIKBUG operating system. With such systems, the user must insert the software interrupt (SWI, #$3F) instruction into the code and stop the program execution at that point every time a register display is desired. A software interrupt causes MIKBUG to gain control after outputting the contents of the registers. Note that after using the software interrupt, the user must reset the program counter and other registers and run the program again. There is no practical way to single step through a program or to have lights which allow one to view registers during execution of a program.

DISPL solves this problem when called as a subroutine. It prints all register contents at the point of call and then returns control to the calling program with all registers restored.

Slight modifications will allow DISPL to do elaborate and useful functions. Including a small supervisor routine in the DISPL routine will allow conditional register printing, or conditional software interrupt. Conditional printing is useful when the user desires to display the registers just the first ten times through a loop, or perhaps just after the 100th time through a loop. This is implemented with just a simple counter and branch if greater than. Conditional software interrupt is extremely useful when the user knows that at a certain place in a program, a particular register should not exceed a given value.

Obviously there are many variations on the sorts of small supervisor routines which can be added on to this basic program. Most are easy to implement. The idea for DISPL was derived from certain functions available with the Motorola Exorcisor system. Unfortunately, no listings of those system programs were available to me, so I wrote the basic idea.■

Listing 1: 6800 register display program. Use of references to MIKBUG makes this program fully position independent.

```
                                      NAM   DISPL
A  0200                               ORG   $200
                  E0CA  A  OUT2HS     EQU   $E0CA     PRINT 2 CHAR FROM X
                  E0C8  A  OUT4HS     EQU   $E0C8     PRINT 4 CHAR FROM X
                  E1D1  A  PRINT      EQU   $E1D1     PRINT A CHAR FROM A
A  0200           00    A  SAVCC      FCB   0         SAVE CONDITION CODES
A  0201           00    A  SAVBR      FCB   0         SAVE B REGISTER
A  0202           00    A  SAVAR      FCB   0         SAVE A REGISTER
A  0203           0000  A  SAVX       FDB   0         SAVE X REGISTER
A  0205           0000  A  SAVPC      FDB   0         SAVE PROGRAM COUNTER
A  0207     07             DISPLY     TPA             TRANSFER CC TO A REGISTER
A  0208     07                        TPA
A  0209     B7    0200  A             STAA  SAVCC
A  020C     32                        PULA            STORE IN . . .
A  020D     B7    0202  A             STAA  SAVAR     SAVCC SAVAR SAVBR SAVX
A  0210     F7    0201  A             STAB  SAVBR     CC    A     B     X
A  0213     FF    0203  A             STX   SAVX
A  0216     30                        TSX             STACK HOLDS PC ON ENTRY
A  0217     A6    00    A             LDAA  0,X
A  0219     B7    0205  A             STAA  SAVPC
A  021C     A6    01    A             LDAA  1,X
A  021E     B7    0206  A             STAA  SAVPC+1   STORE PREVIOUS PC IN SAVPC
A  0221     CE    0200  A             LDX   #SAVCC
A  0224     BD    E0CA  A             JSR   OUT2HS
A  0227     BD    E0CA  A             JSR   OUT2HS
A  022A     BD    E0CA  A             JSR   OUT2HS
A  022D     BD    E0C8  A             JSR   OUT4HS
A  0230     BD    E0C8  A             JSR   OUT4HS    OUTPUT CC,B,A,X,P
A  0233     86    0D    A             LDAA  #$D
A  0235     BD    E1D1  A             JSR   PRINT
A  0238     86    0A    A             LDAA  #$A       CR,LF OUT
A  023A     BD    E1D1  A             JSR   PRINT
A  023D     B6    0202  A             LDAA  SAVAR
A  0240     F6    0201  A             LDAB  SAVBR
A  0243     FE    0203  A             LDX   SAVX
A  0246     36                        PSHA            RESTORE ALL REGISTERS
A  0247     B6    0200  A             LDAA  SAVCC
A  024A     06                        TAP
A  024B     32                        PULA
A  024C     39                        RTS
                                      END
TOTAL ERRORS 00000
```

Text continued from page 8:
siderations already discussed in the forum published with your comment. Remember, all programming languages are equivalent (eg: to a Turing machine), so there are no programs that will run in Pascal that won't run in BASIC.

I don't mean to defend BASIC. It's slow and archaic. But it (and FORTRAN) have lasted much longer than *any* of the block structured languages: ALGOL, PL/1, SIMULA, etc. (By "last," I mean that it is still in popular use.) How long will Pascal last? The ideas behind block structured languages are great, but they have yet to be implemented in an optimal form.

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Several comments. You are considering the cost of a system from the ground up. Many people already have systems with large amounts of memory, and therefore the Pascal system addition is only $200. If you own a small business, the cost of buying a complete Pascal system versus a smaller system using BASIC is probably less once programming time is considered. Also, Pascal is now running on the Apple II computer. The Apple cuts off the cost of a terminal and brings you down to an 1800 dollar computer . . . RGAC

PASCAL COMMUNICATION REQUESTED

We are busy with the implementation of a high level language compiler and would like to get in touch with other groups who pursue similar goals Here is a short summary of our project.

The language at which we are aiming has the full expressional power of Pascal and will run on a p-code interpreter for a virtual machine. As our language will have special features to support the compiler writer's task, we have chosen the name COSY-Pascal to distinguish our Pascal from the strictly defined language. We have planned additional features for the following compiler subtasks. syntax definition, attribute propagation, and definition table options. Design criterions for the extensions were economy of memory usage, user convenience and simplicity of implementation.

Based on recursive descent LL(1) techniques, syntactic rules may be formulated in Backnus-Naur Form. The grammar is compiled almost as is, and will be interpreted at runtime.

As with attributed grammars, variables may be associated with every nonterminal of the grammar, such that the variables of the dynamically last nonterminals are accessible to the programmer. Error messages produced by other errors will be suppressed by the system.

Presently we want to implement a strongly simplified version of Pascal. Most of the interpreter (6502 processor) and some support routines are implemented, but they are not yet intensively tested. A detailed specification of most of Pascal has been worked out and will be discussed.

We hope to have some simple programs compiled and running soon.

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IMPROVING STATISTIC ACCURACY

Alan B Forsyth's article "Elements of Statistical Computation" (January 1979 BYTE, page 182) pointed out how numerical errors can accumulate when computing means and standard deviations. Readers interested in more information about this topic should consult the December 1978 issue of *PPC Journal*, the monthly publication of the Personal Programmers Club for Hewlett-Packard programmable calculator users.

The article, "More Accurate Statistics," discusses in detail a method for accumulating sums of data to compute means and standard deviations. The recurrence formulas, which can be used to store or delete data using the new method, are given, as well as the formulas which show how to compute other statistical parameters associated with the line of best fit for a group of data and the correlation coefficient. An HP-67/97 program is given which shows how to implement the new technique, and numerical examples are discussed. The method given can be programmed on any calculator or computer.

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SOME INSIGHTS ON INFORMATION

Thank you for publishing the fine article by Andrew Filo, on the biology of robots "Designing a Robot from Nature," (February and March 1979 BYTE) His article "turned on a little light." One light turned on in my head per day, or even per week, makes it all worth while.

He reports that frog skin was moved from back to stomach, and from stomach to back. Irritating the stomach then caused the frog to scratch his back, and irritating his back caused the frog to scratch his stomach.

I say Aha Packet-switching. Headers, with source address.

The telegram, the telephone call, or the computer packet all come with a source address; a necessity if the information comes in on a port that has multiple users

Aha #2) I have always wondered how there could be as many nerves in my spine as there are sensors below. If things are party-lined, there don't have to be as many wires.

Aha #3) Our sensors, for the most part, have very low data rates. Normally we are not irritated on many parts of our skin at once. Thre is plenty of time for many sensors to share a trunk in a party-line architecture. We are, I think, confused by an over-abundance of signals at once. By stimulating large areas of skin at one time, you know that something is happening, but you may not be able to separate the points.

Aha #4) Think acupuncture. I have a doctor who, though educated on the US mainland, is Chinese. Dr Lam has studied acupuncture, and practices it, in conjunction with normal medicine. My wife had cramps in her stomach area. They persisted. Dr Lam couldn't localize the trouble because a large area of muscles were fighting. He got out his needle and spun it into her foot, in a spot which he says is related to the stomach area. Within five minutes the muscles had relaxed. The remaining pain was isolated in a small area. He could feel this area, and he diagnosed the pain as gall-bladder. A subsequent operation proved him right: many large gall-stones, one of which had plugged up the duct. What had the doctor done? He had biased (pushed the break button) the nerve from the stomach area to the brain, by getting at the nerve from another port. The brain didn't know the foot-signal from any other signal on the same trunk. The brain decided that there was no longer any pain in the stomach.

Aha #5) This suggests that there are many party-lines in higher animals (and I am a computer man: I have no idea how high) and each of these goes to may diverse sensors.

Aha #6) Today airplanes are using high-bandwidth coax from a string of sensors to the controls. They're on the right track.

Give us enough time, and mix together enough scientists and engineers, give us the help of magazines like BYTE, and we may figure ourselves out yet.

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PASCAL UNEXPANDABLE

Your position in favor of UCSD Pascal is valid only from the perspective of the buyer of a complete computer system who wants the manufacturer to supply all of the operating system software. This buyer is willing to accept the limitations of the software in order that he may take advantage of its being off the shelf. The trend towards bundled packaging of Pascal, as well as other major operating systems and languages, places the buyer of such a product in the position where he or she initially gets a very good deal on a powerful system, but is then unable to expand that initial hardware and software without buying a whole new system. Of course, no such expansion need be contemplated by the majority of customers. But some people may prefer that their initial investment in a system be of continuing value as future additions are made. Although less elegant than UCSD Pascal, there are other software packages one can start with which allow users to implement their own expansions, such as the IPS system described in your January issue. Thus, while valid from the perspective of certain users, your position should be qualified to reflect the limitations of that perspective.

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*As a user of UCSD Pascal for several months now, I have yet to find an impenetrable wall—a fundamental function that was not in the system. To be sure, there are implementation dependent aspects which I find less than perfect. An implicit file name search over all volumes mounted in the system would be a convenience and a slightly larger maximum size for procedure blocks would be most useful. But the system is fundamentally well thought out, and complete as a basis for much productive programming....***CH**

APL NOT DESIRED

Periodically I see APL programs in BYTE. I would like to discourage as much as possible all usage of APL.

When I was an undergraduate at Rice University, I had occasion to use APL quite a bit—first as the language I cut my programming teeth on, then as a graphics language, and finally, tutoring other students who were cutting their programming teeth. I saw these students acquire the same bad habits which I had learned from the language, and have just as hard a time breaking these habits as I did.

APL can be wonderful fun when you first use it, and it has some marvelously powerful constructions which allow you to do many things very concisely. Graphics is a good example. But this same conciseness and the lack of control structures encourage students to have competitions for one-liners. Everyday some poor soul would be elated about a new, completely obtuse line of APL which would generate the first n prime numbers, or some such foolishness. This was fine, as long as these one-liners remained the property of the programmer. But have you ever tried to decipher another person's APL programs? It is literally easier to read an assembler program than a foreign APL program. Even commercial APL software is written obtusely.

I spent a good portion of a week trying to decipher a workspace of graphics routines written by a well-known and well-respected manufacturer, and finally gave up. I've also found that I have a hard time understanding programs that I myself have written more than a month ago in APL. I've found that I no longer need APL, because I have a programmable calculator, and it is my belief that APL would never have existed had Hewlett-Packard come out with the HP-65 before IBM decided that FORTRAN was not all that the engineer needed.

Please let me encourage you not to spoil any of your good articles with an obtuse, unreadable, inefficient one-liner in APL. If APL persists, and our civilization perishes, APL will one day be dug up by a future archaeologist, who will try to decipher it, and find it more unreadable than Linear B.

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GENEALOGICAL INFORMATION

Help! I am a genealogist with a PDP-10, expanded memory and disk and paper tape storage. Where can I find programs for the genealogist to use?

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*Could any readers help trace some promising programs?...***RGAC**

FAST FOURIER TRANSFORMS ON YOUR HOME COMPUTER

I was pleased to see the article by Stanley and Peterson on the fast Fourier transform, "Fast Fourier Transforms on Your Home Computer" (BYTE December 1978, page 14). Aside from having many useful applications, this technique is complex enough to provide some fun and surprises when just playing with it. I would like to share some observations and prejudices which have arisen out of my personal experience with the FFT (fast Fourier transform).

Although the Fourier transform sometimes gives unexpected results and may be used to couch propositions in a very elegant fashion, it may not always be the best approach to use. Every operation in frequency space has an equivalent operation in real space; therefore any procedure utilizing the Fourier transform may, in fact, be performed without it. Sometimes results which appear to be profound become just common sense when approached in this way.

I think that authors should emphasize strongly (as did Stanley and Peterson) that the FFT is not an approximation, but just a faster way to compute the DFT (discrete Fourier transform). Approximations occur only in the sense that the DFT is used to approximate the continuous transform of a continuous (or analytic) function. These approximations arise from two sources, a finite sampling interval and a finite total sampling time. By their very nature, computers cannot calculate a continuous Fourier transform, and we are always forced to use the DFT.

I personally would like to see the "sampling theorem" banned. At best its invocation obscures a perfectly clear concept, and at worst it is a tautology. The useful content of the theorem is contained in the observation that two points are needed to specify a sine wave of a given frequency. Used in this way, the theorem is misleading when it implies that we can safely discard parts of a signal (above a given frequency) because they "contain no information." I think it is more correct to say that the lost parts of the signal contain information that we do not want, cannot get, or do not need. In one sense "information" is a concept that we bring to a signal, not a property of the signal itself. In another sense, all frequencies contain some information, and a portion of that information is always lost during the sampling process.

The sampling theorem is meaningless if, in the literal sense, a signal really contains no information above a given frequency (ie: all Fourier amplitudes are 0). It is then obvious that a knowledge of all amplitudes below this frequency is equivalent to knowing the signal.

For a number of reasons the high frequency part of the DFT differs from the continuous transform we would like it to approximate. It turns out that the DFT is equivalent to sampling a segmental linear function, that is, to a linear interpolation between data points. High frequency components (ie: near the limit decreed by the sampling rate) may be better approximated by multiplying the transform by a low pass filter function. The shape of a given filter corresponds to a particular method of interpolating between data points, and conversely any interpolation scheme yields its own filter function.

Some other references which I have found very useful are:

- Cooley, J W, P Lewis, and P D Welsh, "The Fast Fourier Transform and its Applications," *IEEE Transactions on Education 12*, 1969, page 27.
- Higgins, R J, "Fast Fourier Transform: An Introduction with some Minicomputer Experiments," *American Journal of Physics 44*, 1976, page 766.
- Bice, P K, "Speed Up the Fast Fourier Transform," *Electronic Design 9*, 1970, page 66.

I would be interested in any response to these comments.

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Book Reviews

Practical Microcomputer Programming: The INTEL 8080
by W J Weller, A V Shatzel, and H Y Nice
Northern Technology Books
Evanston IL 1976
306 pages hardcover, 6½ by 9¼ inches
$21.95

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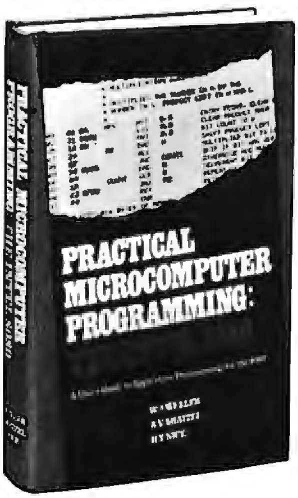


There was my new computer running correctly, lights twinkling alluringly, and there was my first serious problem: how was I to introduce keyboard written code into the thing? I was (that was three years ago) a green novice suddenly required to create a program in machine language, and the available literature helped not at all. The assembly manuals were written in language that a child could follow, but the applications manuals were written in the runes of the software priesthood, all abbreviation and ellipsis. How I wished for a book to bridge the gap!

Well, here it is. In fact it has existed since the end of 1976, but without the fanfare it deserves. It introduces 8080 machine language and assembly language programming to the novice. The authors know that there is a difference between novice and ninny. They never talk down. They merely talk in clear English, in sentences with recognizable nouns and verbs, and they spell out words fully. They move fast, but they have time for colorful illustrations and allusions. They introduce binary operations with a passing reference to Paul Revere's lantern ("One if by land . . . .") and with the case of "If the shade is up don't come in. My husband is home." Examples abound in the form of short assembly language programs. These are always cogent and often related to actual problems that confront the typical home computer owner, such as how to read a keyboard. What's more, the book is a pleasure to handle: hardcover, sewn in signatures (so that it can lie on the desk open at any page), printed in clear book type on creamy matte paper.

The first chapters focus on binary operations, the Intel mnemonics, the elemental operations that they instigate, and the conventions of assembly language programming. On every page the authors spot and clear up the small ambiguities of technical jargon that can block understanding. For example, the Intel instruction MOV A,B only copies the contents of B register into A register and nothing gets transported bodily. Throughout, they use the word *copy* in preference to *move*. They point out the fact that the zero flag in the status register reads zero when the result of an operation is nonzero and is one when the result is zero. And they explain that there is a difference between carry and overflow in the status register even though, as they point out, "the Intel literature has used them interchangeably and in some places erroneously."

They go on, chapter by chapter, to shed light on binary arithmetic; multiplication and division in binary; the use of the stack pointer; the use of subroutines, arrays, and tables; how to convert between binary and decimal (and why the instruction DAA is not often used); a detailed explanation of input/output (I/O) and communication with a terminal; analog I/O; interrupt driven processes; and the debugging of programs. With this kind of introduction, the reader is then quite able to benefit from the many books and manuals that are directed toward the professional.

The reader will learn best by actually trying the little programs that accompany the text, but in doing so should be prepared for some snags. The source listings frequently contain pseudoinstructions that are peculiar to the cross assembler used by the authors: ZAR, LLA, JEQ, and about a dozen others. These can be translated even by a beginner (with the help of the index) into conventional Intel instructions, but one wishes it were not necessary. The cross assembler was written by the authors for a Computer Automation LSI-2 machine. The home computerist might wish they had used one of the resident assemblers commonly available to home users, but evidently the book is aimed not only at the hobbyist but also at the college classroom, where the big equipment is more likely to be available. Almost a third of the book is devoted to a complete source listing of the cross assembler.

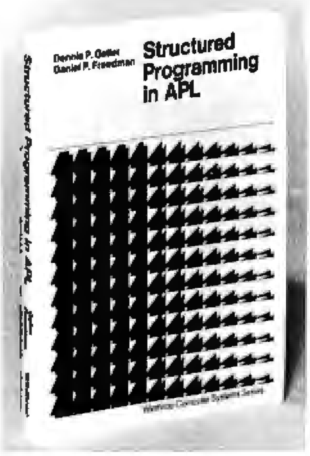
Another substantial source listing, found in Appendix A, is the authors' "Hexadecimal Debug" program, and you may well want to put it into operation in your own system. It's nifty. Debug is an 880 byte program that enables the user to inspect and alter the contents of memory, to inspect and alter the registers, and to set breakpoints, all in unusually convenient ways. Remember, however, to mark all the odd pseudo-operation codes and replace them. You may also have to replace subroutine labels that duplicate the designations of registers A, B, D and H, if your assembler gets confused by such duplication, as mine does. Line 254 contains a misprint: the printed instruction is CPI ' ', whereas it should read CPI '.'; perhaps the period got lost when the dot matrix printout was reproduced.■

Structured Programming in APL
by Dennis P Geller and Daniel P Freedman
Winthrop Publishers Inc, 1976
Englewood Cliffs NJ $9.95

Structured programming began with two insights: one embodied in a formal proof that any possible program logic could be expressed in terms of a conditional branch and a conditional loop, and the other, Dijkstra's observation that the quality of programmers' work is a decreasing function of the number of GOTOs in their code. From these two insights has sprung a revolution in programming style among those who have accepted them, and angry arguments from those who haven't, and who feel put upon by those who insist on eliminating GOTOs altogether.

This book simply shows how to use APL in such a way that only structured programs result, and makes virtually no mention of the term structured programming outside its title. It is written as an introductory textbook, interweaving lessons on APL functions and operators among chapters on IF statements and DO loops, other features of APL such as terminal use, workspace management and debugging aids, and apt quotations from Lewis Carroll's *The Hunting of the Snark*.

Coverage is thorough, and the level is elementary. Anyone who absorbs all the material of this book will need only study and practice on a variety of applications in order to be a competent programmer, something that cannot be said of most language manuals which define the language but do not show the right manner of using it. The chapter on documentation is especially valuable, and would make an excellent addition to every APL public library system.



Another useful feature of the book is the careful demonstration of the program development process, especially after the program is working and various features are being incorporated into the design, many in exercises for the student. Included in program development is provision for error checking of input, with various indicators of error or prompts to try again. This is an area in which APL excels if the programmer knows how to do it and takes the trouble.

Functions can check their arguments and user inputs for type, size, range and other errors before performing any operations that could adversely affect data or otherwise cause trouble, and a general utility function to do this is provided that accepts as its arguments a condition to be checked and a message to print when the condition holds.

The method used to diagram program structure is one that enforces the discipline of structured programming. It permits the nesting of loops and decisions, but does not have provision for going from one point in the program to any other. Once a program has been laid out in this manner, it is a trivial task to code the branch statements; and thus correct structure, though not efficiency, is assured. This is one of the sore points among nonstructured programmers. It is, of course, not mentioned in the text, except for a note in the preface expressing the hope that students will learn from the text to write working (ie: correct) programs here, whether or not they may learn to write more compact, faster or more aesthetic programs later.

The foreword claims that students using the material of this book learn more, faster, at lower cost in human and machine time than those using other approaches. I have no way of directly testing this myself, but I can say that it would not surprise me if it were true. This is the only APL textbook that is a programming textbook first and a language manual second; this is rare in any programming language. The only book I can compare it with is *APL: An Interactive Approach*, by Gilman and Rose, on the basis that both teach the language to the user, on line, giving examples and experiments to try. Gilman and Rose go more deeply into the language, but neglect programming style and technique; they are not writing for novice programmers as Geller and Freedman are. If you are confident of your style, read Gilman and Rose. If you are just starting, or don't know much about structure, design and documentation, *Structured Programming in APL* is the one for you. Better yet, read both.

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The Cheap Video Cookbook
by Don Lancaster
Howard W Sams and Co
Indianapolis IN, 1978
$5.95

Don Lancaster stays on the sequel bandwagon with his new "cookbook." This time, the recipe is for a 7 integrated circuit design called TVT 6 5/8. This $20 circuit, along with software and module customizing, allows a wide variety of alphanumeric (such as 24 lines by 80 characters) or graphic (256 by 256) displays on standard television sets. A little extra software gives you multiple cursors, scrolling, and full editing features.

The book's first chapter introduces the concept of "cheap video," and has a brief explanation of its two novel tricks: SCAN and upstream tap. Chapter 2 covers various software routines needed for a good display, each routine building on the last. The reader is encouraged to write improved versions. Routines covered include cursors, scrolling, graphics loaders, memory repacking (for 40 or 80 character lines), and the all-important (to "cheap video") SCAN "microinstruction." Upstream taps, data-to-video conversion, bandwidth reduction, sync circuitry, and other hardware, as well as television modifications, are in chapter 3. Construction details in chapter four describe the main circuit and several "personality" modules. The fifth chapter addresses transparency, or how to do other things such as run BASIC, when the computer is not working with the display.

The TVT 6 5/8 is designed around a 6502 microcomputer (KIM), but with mainly software changes a 6800 system should work just fine. Other processors, such as the Z-80, 8080, 1802, and 2650 should be usable, but would require more work. Although the TVT 6 5/8 is built from only seven integrated circuits, and the circuit itself only costs approximately $20, there is more to it than first meets the eye.

The author makes a few important assumptions. It is assumed that you already own a microcomputer (KIM in this case) that has sufficient programmable memory (up to 8 K bytes for 256 by 256 black and white graphics) to store the display. There must also be enough memory left over to run any cursor, loader, or other applications software. You must be willing and able to modify your microcomputer's memory to add a clever trick called an "upstream tap." Finally, you mustn't mind giving up 5 percent (for a single 32 or 40 character line display) to 50 percent (for 16 by 80 alphanumeric displays) to 50 to 95 percent (256 by 256 graphics) of the processor's time so that it can control the display. As far as the television is concerned, you may have to adjust the horizontal hold and/or defeat the sound trap for a really good 24 by 80 display. Still, you get only a 5 by 7 dot matrix (it uses less bandwidth than a 7 by 9 matrix) and, if you aren't careful, the display may still flicker. Cheap video is cheap because the memory (the single largest expense for a video display) is assumed to be available at no cost, and the processor is assumed to be available between 5 and 95 percent of the time to provide display timing.

Whether you stick with the older all-hardware interface using counters and gates and registers, or try your hand at this approach of letting the processor do most of the dirty work, or even if you just are curious about how video displays work, this is a good reference book. It has several hints and tricks for reducing bandwidth requirements, for generating suitable video and sync signals, and for making more general (module programmed) circuits which easily can be changed to provide different display formats. It even has complete schematics, printed circuit board patterns, and "nuts and bolts" instructions on how to build your own TVT 6 5/8. Proofreading was lax in the schematics section, though, so you have to be on your toes and understand basic electronics to catch and correct the many discrepancies in component types and values, as well as to follow the few unexplained circuit changes made from schematic to schematic.

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Microcomputer-Based Design
by John B Peatman
McGraw-Hill, New York
540 pages, 6½ by 9½ inches
$24.50

Microcomputer-Based Design by John B Peatman is a combination text and reference book aimed at engineers who wish to learn how to design systems using microprocessor. It is written not in a dull, dry tone, but rather in a light style. The minimum required background for this text is a rudimentary knowledge of logic (ie: transistor-transistor logic gates and flip flops) and the basic concepts of computer programming. The book develops hardware and software design skills upward from that point to a practical and useful level. A key feature of this book is the logical, lucid presentation of arguments present in the many illustrated design decisions.

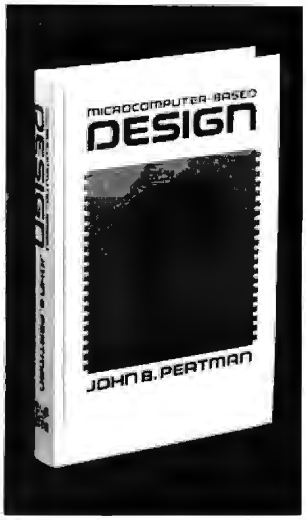
Microcomputer-Based Design is divided into seven chapters and six appendices. The chapters are fairly complete, in-depth entities and each contains a set of practical design problems and additional references. The references may be difficult to find for readers without access to an engineering library since many of the references are articles in engineering journals or manufacturers' application notes.

Chapter one is an overview of microcomputer applications focusing primarily on the distribution of "intelligence" to instruments and tools.

Chapter two, "Microcomputer Registers and Data Manipulation", includes a brief discussion of numbering systems and the various, commonly encountered modes of addressing. This is followed by a good presentation of machine language instructions, assembly language, and assembly language programming techniques.

Chapter three considers computer hardware organization. Several different philosophies of commercially available microprocessor families are described. The characteristics of various logic families are considered with an eye towards interconnection compatibility. Bus structures and their electronic implementation are described in some detail. Flags, interrupts, direct memory access control and programmable timers are also described with examples.

Chapter four reviews the various characteristics of memory components and systems. Included are sections on the implementation of main power failure battery



backup systems and floppy disks.

Chapter five examines peripherals. There are sections on IO control and handshaking, timing and buffering. There are also discussions of specific common microcomputer peripherals: keyboards, phototransducers, circuit testers, analog to digital and digital to analog converters, pressure transducers, optical displays, relay drivers, synchromotors and printers. Finally, there are sections on universal asynchronous receiver-transmitters (UARTs), line drivers, the HPIB-IEEE 488 bus and self-test hardware.

Chapter six describes the various options that exist in hardware and software development packages from prototyping boards to disk based operating systems. There is also a brief discussion of high level languages for microcomputers.

Chapter seven describes in detail the algorithms for solutions to several common microcomputer software problems. Algorithms are described to read and to parse a functional keyboard input, self-test routines and number system conversion and manipulations. Real time programming constraints are also considered.

The set of appendices describes the characteristics of specific microcomputers. Each appendix covers the architecture and organization of a particular processor integrated circuit. The rest of the integrated circuit set (memory, IO, etc) is also briefly covered. Appendices are included on the 4004, F8, 8080, 6800, COSMAC, and PPS-8 processors. It is refreshing to see that these appendices are more than just a reprinting of the manufacturers' specification sheets.

On the negative side, there is a disturbing absence of discussion of any of the higher performance integrated circuits that were certainly available when this book was written. There is also inadequate treatment given to bit slice and microprogramming techniques. Software development by emulation is also omitted. The balance is, however, overwhelmingly positive. This is a text which starts off quietly, never grows dull, and yet contains a great deal of substance. There are sections on using esoteric devices like first in first out stacks (FIFOs) that I have previously never seen in a design text.

Microcomputer-Based Design is a welcome development. I recommend this book to advanced experimenters, undergraduate engineering students and practicing engineers.

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A Mini-Disassembler for the 2650

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Software development in machine language is a difficult task. A substantial part of the frustration can be traced to the difficulties of debugging a program when one must work from a printout that has no flow, no mnemonics, and bears little resemblance to any real world logic system. A disassembler can save the programmer countless headaches by correcting these deficiencies. This particular disassembler was constructed to aid in the development of software for a dedicated controller for an amateur radio repeater.

The basic requirements for our disassembler are that it use a small amount of memory (this version uses less than 750 bytes of memory, satisfying our definition of small), and that it provide a readable listing that includes mnemonics. The only restriction of this version is that it will print a maximum of only hexadecimal FF addresses (eg: hexadecimal 0400 to 04FF) without being restarted.

Using the Disassembler

The disassembler is employed in a straightforward manner:

1. Load the program from the listing.
2. Using the Signetics PIPBUG monitor, GOTO the initial address of the disassembler.
3. Input a 4 digit address for the program to be listed (include leading zeroes).
4. Input a 2 digit stop address.

Text continued on page 236

Listing 1: A 2650 disassembler. Technically, this listing is a disassembled assembly listing of a disassembler. The program is designed to take Signetics 2650 machine language code and transform it into an assembler-like listing.

Address	Hexadecimal Code			Operator	Operand
0440	76	40		PPU	
0442	77	02		PPL	
0444	06	FD		LODI	2
0446	3F	02	24	BSTA	3
0449	01			LODZ	1
044A	CE	64	00	STRA	2
044D	DA	77		BIRR	2
044F	06	FE		LODI	2
0451	0E	63	FF	LODA	2
0454	C1			STRZ	1
0455	3F	02	69	BSTA	3
0458	DA	77		BIRR	2
045A	3F	03	5B	BSTA	3
045D	04	02		LODI	0
045F	CC	04	FC	STRA	0
0462	0D	84	FD	LODA	1
0465	06	F8		LODI	2
0467	04	03		LODI	0
0469	07	DB		LODI	3
046B	CC	04	FB	STRA	0
046E	0E	63	F3	LODA	2
0471	E1			COMZ	1
0472	98	0E		BCFR	0
0474	CF	04	F9	STRA	3
0477	04	09		LODI	0
0479	CC	04	FA	STRA	0
047C	3F	05	E4	BSTA	3
047F	1F	04	D0	BCTA	3
0482	87	03		ADDI	3
0484	DA	68		BIRR	2
0486	04	01		LODI	0
0488	CC	04	FC	STRA	0
048B	04	0C		LODI	0
048D	CC	04	FA	STRA	0
0490	06	FC		LODI	2
0492	0E	63	F7	LODA	2
0495	E1			COMZ	1
0496	98	09		BCFR	0
0498	CF	04	F9	STRA	3
049B	3F	05	E4	BSTA	3
049E	1F	04	D0	BCTA	3
04A1	87	03		ADDI	3
04A3	DA	6D		BIRR	2
04A5	F5	10		TMII	1
04A7	18	03		BCTR	0
04A9	1F	05	15	BCTA	3
04AC	F5	08		TMII	1
04AE	1C	05	00	BCTA	0
04B1	07	AB		LODI	3
04B3	04	14		LODI	0
04B5	06	02		LODI	2
04B7	E1			COMZ	1
04B8	99	09		BCFR	1
04BA	CF	04	F9	STRA	3
04BD	3F	05	28	BSTA	3
04C0	1F	05	D2	BCTA	3
04C3	84	04		ADDI	0
04C5	87	0C		ADDI	3
04C7	FA	6E		BDRR	2
04C9	84	17		ADDI	0
04CB	D8	68		BIRR	0
04CD	1F	00	00	BCTA	3
04D0	3F	00	8A	BSTA	3
04D3	0C	04	FE	LODA	0
04D6	E4	01		COMI	0
04D8	1E	00	00	BCTA	2
04DB	0D	04	FF	LODA	1
04DE	E1			COMZ	1

Listing 1 continued:

```
04DF    9E 00 00    BCFA    2
04E2    1F 04 4F    BCTA    3
04E5    00          LODZ    0
04E6    00          LODZ    0
04E7    00          LODZ    0
04E8    00          LODZ    0
04E9    00          LODZ    0
04EA    00          LODZ    0
04EB    12 13       SPU
04ED    74 75       CPU
04EF    76 77       PPU
04F1    84 85       TPU
04F3    40          HLT
04F4    92          LPU
04F5    93          LPL
04F6    C0          NOP
04F7    00          LODZ    0
04F8    30          RDCZ    0
04F9    EA 09       PPL
04FB    03          LODZ    3
04FC    01          LODZ    2
04FD    04 FE       LODI    0
04FF    12
*
0500    04 20       LODI    0
0502    07 93       LODI    3
0504    E1          COMZ    1
0505    99 06       BCFR    1
0507    CF 04 F9    STRA    3
050A    1F 05 28    BCTA    3
050D    87 03       ADDI    3
050F    84 1F       ADDI    0
0511    D8 71       BIRR    0
0513    1B 72       BCTR    3
0515    04 10       LODI    0
0517    07 7B       LODI    3
0519    E1          COMZ    1
051A    99 06       BCFR    1
051C    CF 04 F9    STRA    3
051F    1F 05 28    BCTA    3
0522    87 03       ADDI    3
0524    84 1F       ADDI    0
0526    D8 71       BIRR    0
0528    F5 0C       TMII    1
052A    C0          NOP
052B    98 0F       BCFR    0
052D    04 03       LODI    0
052F    CC 04 FC    STRA    0
0532    CC 04 F7    STRA    0
0535    04 06       LODI    0
0537    CC 04 FA    STRA    0
053A    1B 37       BCTR    3
053C    F5 08       TMII    1
053E    98 0F       BCFR    0
0540    04 02       LODI    0
0542    CC 04 FC    STRA    0
0545    CC 04 F7    STRA    0
0548    04 09       LODI    0
054A    CC 04 FA    STRA    0
054D    1B 24       BCTR    3
054F    F5 04       TMII    1
0551    98 11       BCFR    0
0553    04 02       LODI    0
0555    CC 04 FC    STRA    0
0558    04 01       LODI    0
055A    CC 04 F7    STRA    0
055D    04 09       LODI    0
055F    CC 04 FA    STRA    0
0562    1B 0F       BCTR    3
0564    04 01       LODI    0
0566    CC 04 FC    STRA    0
0569    04 00       LODI    0
056B    CC 04 F7    STRA    0
056E    04 0C       LODI    0
0570    CC 04 FA    STRA    0
0573    3F 05 8A    BSTA    3
0576    04 01       LODI    0
0578    CC 04 FB    STRA    0
057B    07 77       LODI    3
057D    0C 04 F7    LODA    0
0580    83          ADDZ    3
0581    CC 04 F9    STRA    0
0584    3F 06 02    BSTA    3
0587    1F 05 D2    BCTA    3
```

Listing 1 continued on page 236

Text continued from page 233:

The Listing Format

Example: 0765 04 20 00 LODI 0

Address
First Byte (op code)
Second Byte (if used)
Third Byte (if used)
Mnemonics
R/V

Listing 1 continued:

Address	Hexadecimal Code			Operator	Operand
058A	06	0C		LODI	2
058C	0E	65	9B	LODA	2
058F	E1			COMZ	1
0590	98	05		BCFR	0
0592	04	01		LODI	0
0594	CC	04	FC	STRA	0
0597	FA	73		BDRR	2
0599	1F	05	A9	BCTA	3
059C	14			RTCI	0
059D	15			RTCI	1
059E	16			RTCI	2
059F	17			RTCI	3
05A0	34			RTEI	0
05A1	35			RTEI	1
05A2	36			RTEI	2
05A3	37			RTEI	3
05A4	94			DARI	0
05A5	95			DARI	1
05A6	96			DARI	2
05A7	97			DARI	3
05A8	00			LODZ	0
05A9	F5	03		TMII	1
05AB	98	07		BCFR	0
05AD	04	33		LODI	0
05AF	CC	04	F8	STRA	0
05B2	1B	1B		BCTR	3
05B4	F5	02		TMII	1
05B6	98	07		BCFR	0
05B8	04	32		LODI	0
05BA	CC	04	F8	STRA	0
05BD	1B	10		BCTR	3
05BF	F5	01		TMII	1
05C1	98	07		BCFR	0
05C3	04	31		LODI	0
05C5	CC	04	F8	STRA	0
05C8	1B	05		BCTR	3
05CA	04	30		LODI	0
05CC	CC	04	F8	STRA	0
05CF	1F	05	E4	BCTA	3
05D2	C0			NOP	
05D3	07	01		LODI	3
05D5	3F	03	5D	BSTA	3
05D8	0C	04	F8	LODA	0
05DB	3F	02	B4	BSTA	3
05DE	3F	00	8A	BSTA	3
05E1	1F	04	D3	BCTA	3
05E4	0E	04	FC	LODA	2
05E7	0D	84	FD	LODA	1
05EA	3F	02	69	BSTA	3
05ED	07	01		LODI	3
05EF	3F	03	5D	BSTA	3
05F2	0D	04	FE	LODA	1
05F5	85	01		ADDI	1
05F7	CD	04	FE	STRA	1
05FA	FA	6B		BDRR	2
05FC	0F	04	FA	LODA	3
05FF,	3F	03	5D	BSTA	3
*					
0602	0E	04	FB	LODA	2
0605	0D	04	F9	LODA	1
0608	0D	25	9B	LODA	1
060B	3F	02	B4	BSTA	3
060E	FA	78		BDRR	2
0610	07	01		LODI	3
0612	17			RTCI	3
*					

Listing 1 continued:

0613	–5A	–49	–52	–41	–4C	–4F	–44	–45	–4F	–52	–41	–4E	–44	–49	–4F	–52
0623	–41	–44	–44	–53	–55	–42	–53	–54	–52	–43	–4F	–4D	–42	–43	–54	–42
0633	–53	–54	–42	–52	–4E	–42	–53	–4E	–42	–43	–46	–42	–53	–46	–42	–49
0643	–52	–42	–44	–52	–00	–00	–00	–52	–54	–43	–52	–44	–43	–52	–54	–45
0653	–52	–52	–52	–52	–44	–45	–52	–44	–44	–00	–00	–00	–00	–00	–00	–44
0663	–41	–52	–57	–52	–43	–00	–00	–00	–52	–52	–4C	–57	–52	–45	–57	–52
0673	–44	–54	–4D	–49	–00	–00	–55	–53	–50	–4C	–43	–50	–55	–43	–50	–4C
0683	–50	–50	–55	–50	–50	–4C	–54	–50	–55	–54	–50	–4C	–48	–4C	–54	–4C
0693	–50	–55	–4C	–50	–4C	–4E	–4F	–50	–0E	–0E	–0C	–8E	–0C	–8B	–4B	–2D

•

In any command dealing with registers, the R/V column represents the register number. In all other cases the R/V column represents the V (value or condition) field.

The total memory used in this listing is from hexadecimal 0440 to 069A. Areas 04EB to 04F2 and 04F3 to 04F6 are used as tables of unique codes. 04F7 to 04FF is a scratch pad storage area (eg: STOP, START addresses). The area from hexadecimal 059C to 05A7 contains a table of op codes that are one byte long but which have a format of two bytes. Hexadecimal 0613 to 069A is used for storage of ASCII characters which are used for mnemonics.

Storage Area Definitions

04F7 = Address mode 00=Z, 01=I, 02=R, 03=A
04F8 = R/V of op code
04F9 = Indexing for mnemonics print
04FA = Number of spaces between data and mnemonic
04FB = Number of letters in mnemonic
04FC = Number of bytes in command
04FD = High order start address
04FE = Low order start address
04FF = Stop address

This is not a refined program by any means: with some work it could reside in less memory and perhaps be more efficient. Its only intent is to be a development tool, and it does this well. It has helped make software development for our controller more like higher level language programming.■

Aids for Hand Assembling Programs

BRAVEC

The program takes a 16 bit number ORigin and adds two to it. The new number then is subtracted from another 16 bit number, DEstination. The difference, which may be positive or negative, in two's complement, is stored in POINTL. The difference is also examined to determine if it is larger than +127 (if positive) or smaller than −127 (if negative). If this is the case, FF is loaded into POINTH; otherwise 00 is loaded. POINTH and POINTL are then displayed by transferring control to the (KIM) operating system.

Listing 1: Program description for BRAVEC. This description should be the first step taken when writing a program.

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Resident assembler programs and interpreters for high level languages are available increasingly for microcomputer systems based on the more popular microprocessors. Nevertheless, many operators of small microcomputer systems are unable to use such programs because their systems are not large enough to support them. Unless they are lucky enough to have access to a timesharing service or to some larger computer which supports a cross assembler, their only way of developing a usable object program is to assemble it by hand.

While the mere idea of such an endeavor might horrify any programmer who is used to working with large machines, the hand assembly of shorter programs for 8 bit microprocessors actually is not very difficult. It has been my experience that the assembly of programs can be greatly simplified and the likelihood of errors can be reduced by using some simple aids in the assembly process.

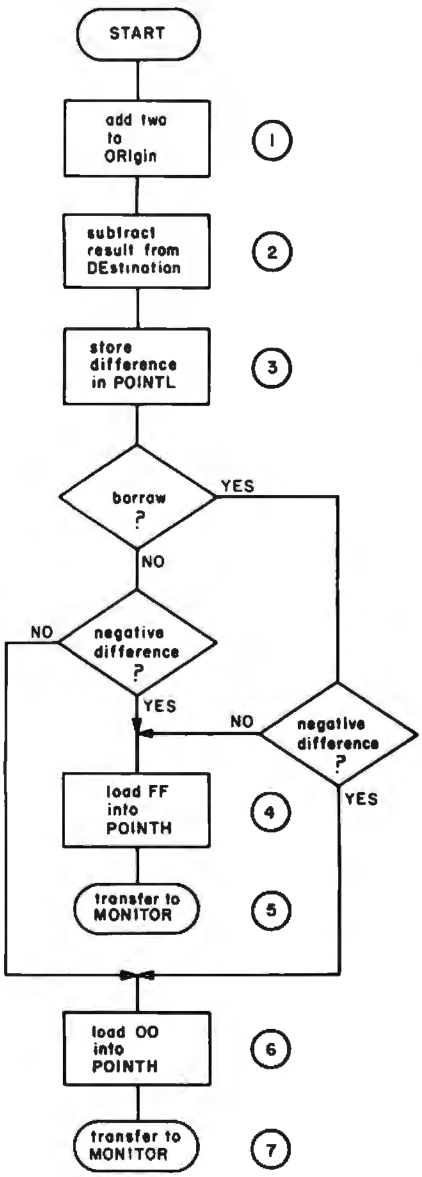
One of these aids is in the form of hardware and consists of a special program assembly form. The software aids are several short utility routines which run even on the smallest microcomputer systems. Development of the assembly method described in this article is based on experience gained from working with programmable calculators of the keyboard language type. Matt Biever of the Pro-Log Corporation has long been advocating some of the techniques that I am using. The article's assembly method is used for program development for a KIM-1 microcomputer. It can be adapted easily for other microcomputer systems as long as they use an 8 bit processor. The assembly method will be demonstrated with a sample program.

Before writing a program, it is a good idea to put down in writing what the program is supposed to do. Such a program description, as shown in listing 1, might state any limitations on the magnitude of variables used or might indicate what happens if these limitations are exceeded.

The next step is to develop a concept of the program in the form of a flowchart as in figure 1. While the symbols used in such charts are standardized, the chart's degree of detail is a matter of personal preference. From program descriptions and flowcharts, one can determine how many memory locations or registers will be necessary to store data and temporary results. These locations should be written in the program register table as shown in table 1. This table also contains the addresses of subroutines or registers of the monitoring system that are called by the program, or of PIA registers that will be addressed. The table is similar to the symbol table printed by the computer during the machine assembly of a program.

After a program description is developed the actual writing of the program can begin. The programmer, who writes a symbolic listing for machine assembly, arranges a program in the form of lines. Each line is successively numbered, contains one mnemonic for an operation (unless it is an "all comment" line) and later will be punched into one punch card for computer entry. Because the operation described by the mnemonic can have a length of one, two or three bytes, each line eventually results in one, two or three machine instructions. Therefore, there exists no simple relation between the line number and the address at which the machine code is stored in the computer memory. For the hand assembly of programs, it is advantageous to use a different format for the program listing in which there is a one to one relationship between program line and memory location. The writing of the symbolic program and the assembly into machine code is greatly simplified by the use of a special program assembly

Figure 1: Flowchart of the program described in listing 1. The circled numbers refer to the comment numbers in listing 2.



Use	Label	Location
ORigin	ORLO ORHI	0000 01
DEstination	DELO DEHI	02 03
"open cell"	POINTL POINTH	FA from listing of FB KIM monitor
Transfer to KIM monitor	START	1C4F from listing of KIM monitor

Table 1: Program register table for program BRAVEC. This table contains all descriptions of all memory locations used by the program.

form. The form I developed for our KIM-1 system is shown in listing 2. (Similar forms are available from the Pro-Log Corporation; order Nr CF-1.) Each line of the coding form corresponds to one memory location with the least significant hexadecimal digit of the address preprinted in the ADD column. The form can be used with any computer system that uses a hexadecimal machine code. For octal notation, a different layout is advantageous.

The programmer starts writing a program by adding the other digits of the program starting address in the ADD and Page

Listing 2: Program listing of BRAVEC using the author's hand assembly form for the KIM-1. This form can be used with any hexadecimal based microprocessor.

Program: BRAVEC

Page 1 **of** 2 **Date: Programmer:**

Page	ADD	OPC	Label	MNE	Mode	Operand	N	Comment
00	0Ø		ORLO					
	1		ORHI					DATA
	2		DELO					REGISTERS
	3		DEHI					
	4	18		CLC				1
	5	A9		LDA	#	2		
	6	02						
	7	65		ADC	Z	ORLO		
	8	00						
	9	90		BCC		NELO		
	A	02						
	B	E6		INC	Z	ORHI		
	C	01						
	D	85	NELO	STA	Z	ORLO		
	E	00						
	F	38		SEC				2
	1Ø	A5		LDA	Z	DELO		
	1	02						
	2	E5		SBC	Z	ORLO		
	3	00						
	4	85		STA	Z	POINTL		3
	5	FA						
	6	A5		LDA	Z	DEHI		2
	7	03						
	8	E5		SBC	Z	ORHI		
	9	01						
	A	A5		LDA	Z	POINTL		
	B	FA						
	C	90		BCC		NEG		
	D	09						
	E	10		BPL		OUT		
	F	09						

VA-BECC Program Assembly Form

columns. It should be noted that the Page column refers to memory pages while the Page-of heading indicates pages of coding forms. The program is written by entering the mnemonic of the first instruction into the MNE column of line 0. Many of the instructions of a microprocessor can occur in more than one addressing mode. During machine assembly, the assembler program deducts the addressing mode from the format of the operand or the definition of a symbol. When hand assembling a program it is advantageous to specify the addressing mode in the Mode column. Immediate

Listing 2 continued:

Program: BRAVEC
Page 2 **of** 2 **Date:** **Programmer:**

Page	ADD	OPC	Label	MNE	Mode	Operand	N	Comment
	2Ø	A9	FLAG	LDA	#	$FF		4
	1	FF						
	2	85		STA	Z	POINTH		
	3	FB						
	4	4C		JMP	ABS	START		5
	5	4F						
	6	1C						
	7	10	NEG	BPL		FLAG		
	8	F7						
	9	A9	OUT	LDA	#	00		6
	A	00						
	B	85		STA	Z	POINTH		
	C	FB						
	D	4C		JMP	ABS	START		7
	E	4F						
	F	1C						
	Ø							
	1							
	2							
	3							
	4							
	5							
	6							
	7							
	8							
	9							
	A							
	B							
	C							
	D							
	E							
	F							

VA-BECC Program Assembly Form

mode addressing is commonly indicated by the symbol #. For other addressing modes, suitable abbreviations of the column headings in the programmer's reference card should be used. For operations which have only one addressing mode, the Mode column is left empty. The addressing mode determines how many address bytes will have to follow the op code byte. After filling in the Mode column, the programmer should cross out the appropriate number of lines in the MNE column. This reserves the corresponding memory locations for the address or operand part of the instruction.

The Label column will carry an entry for two conditions only:

- If the line contains the start of a subroutine.
- If the line is the destination of a conditional or unconditional jump or branch instruction.

While assembly programs sometimes put certain limitations on the choice of labels, any suitable word or letter and number combination can be used as a label for hand assembly. However, it makes sense to pick a word or abbreviation that indicates what the subroutine or branch destination is doing in the program, (ie: "WAITLOOP," "COUNT," or simply "LOOP 7").

The next column to fill in is the one with the heading Operand. When writing programs for machine assembly, the programmer enters a symbolic label in this field and leaves it up to the assembly program to figure out what to do with it. When writing for hand assembly, the programmer can make the task easier by being a bit more specific. The operand can be one of the following things:

1. In the immediate addressing mode, it is simply the number that is to be entered by the operation. Rather than give this number a symbolic name which is defined somewhere in a symbol table, it is much easier to enter it directly in the Operand column. One has to be careful to remember which number system is being used. A number without a prefix indicates decimal notation. The prefix % indicates binary notation. A bit mask for bit 2 and 0, for example, would have the operand % 0000 0101. If the number is in hexadecimal form, the prefix $ would normally be used, but in this case it is much simpler to enter the hexadecimal number directly in the OPC column of the following line.

2. With a jump or branch instruction, the operand symbol indicates the destination of the operation. The operand of such an operation must have a counterpart in the label column somewhere in the program. The only exception is when the program calls subroutines that are stored in read only memory (as I do frequently with subroutines of the KIM monitoring system). In this case, the operand symbol has to have a counterpart in the stored program.

3. With any other memory referenced instruction, the operand must symbolize a memory location. I have found it useful to think of these locations as registers even though, unlike the registers of the processor, they are physically located somewhere in memory. As a matter of fact, their location, if possible, is in page zero of the memory to take advantage of the shorter addressing mode. For registers used in stock subroutines, I have assigned locations which begin at the upper end of page zero and work their way downward. They are listed in a master register list and care has been taken that subroutines that are likely to be used in the

same program do not occupy the same register addresses. The symbolic names for registers that will be used in the main program are noted in a program register table (table 1) with the addresses to be assigned later. The symbols again should be words or abbreviations which indicate the meaning of the data contained in the register, such as STARLO to mean starting address, low order byte.

The column N of the program assembly form can be used to indicate the number of cycles it takes to execute the instruction. This is necessary, for example, to determine the time of timing loops. In most cases, however, this column will be left empty.

Finally, the Comment column should be used to explain the function of the operation listed in the current line and sometimes some following lines. While this information may not be needed by the programmer, it is tremendous help for any other person trying to understand what the program is doing. If the program has been flowcharted first, which is highly recommended for all but the shortest programs, the comment can simply be a number which refers to an equally numbered symbol on the flowchart.

In this way the programmer works down the lines of the program assembly form. Every time a 0 is encountered in the ADD column, (s) he adds the most significant bit. If that addition makes the ADD column is also advanced. Eventually the program will be completed and the hand assembly can begin. Like the computer, I do this in a number of passes.

The first pass is the easiest one. Using a listing of the instruction set, or the programmer reference chart, the mnemonic and the entry in the Mode column is used to look up the op code of the instruction, which is entered into the OPC column of the line. A frequent error during this operation is to mistake an 8 for a B or vice versa, and I double check op codes with these sumbols. The programmer's reference cards supplied by the manufacturers, although they fit nicely into a shirt pocket, were apparently not intended for use by programmers over 40 years of age. The listing of the instruction set in the data sheets or system manuals is usually printed in a more reasonable letter size.

The second step is to assign absolute addresses to the symbols of the program register list. First, all registers and their addresses used in stock subroutines to be called by the program are transferred from the master register list to the program register list. Then absolute addresses are assigned to all other registers listed, making sure that no duplication occurs. Registers which contain the low and high order bytes of numbers, or registers which contain successive bytes if multiple precision operations are used, have to be arranged in such a way that their absolute addresses are adjacent in increasing order (STARLO = B3, STARHI = B4).

With the completed program register list one can go over the program again. For each memory referenced instruction other than branch and jump instructions, the program register list will contain an absolute address for the symbol in the operand column. This hexadecimal number is now entered into the OPC column of the following line. For registers located outside of page zero (such as the registers in PIAs) the address will be entered in two lines and care has to be taken to enter the low order byte first, followed by the high order byte. During this pass I also check all lines with a # in the Mode column and, if necessary, convert the binary or decimal operand into hexadecimal notation which is entered in the OPC column of the following line.

With this step completed, the OPC column should show a hexadecimal number in most lines. The next step is to pass over the program listing another time.

Any line with an open OPC column where the mnemonic indicates a branch instruction will require that the branch vector for the relative addressing mode be calculated. For short forward branches this poses no problem because the offset can easily be counted off (beginning at the second line following the one which contains the branch instruction, and continuing to the line which has the corresponding symbol in the label column). For longer branches and especially backwards branches, if memory pages are crossed it is very easy to make a mistake and miss by one count in either direction. I have found it advantageous to let the microcomputer perform this operation because, after all, it is much better in hexadecimal calculations than any programmer.

The example program BRAVEC receives the origin and destination of a branch and calculates the branch vector in two's complement notation. A flag is set if the relative addressing range is exceeded. The program is loaded from cassette tape beginning at memory location 0000. Loading begins here because this location in the KIM-1 system can be addressed easily by pressing the space bar of the connected terminal. The first four locations are actually data registers into which the low and high order bytes of origin and destination of the branch are entered.

When the program is executed beginning at location 0004, it displays or prints the branch vector in two's complement as the low order byte of the address field. The high order byte of this field normally shows 00, while FF indicates that the reach of the relative addressing mode has been exceeded.

While the program, as listed, is written for the 6502 microprocessor, only instructions that have an equivalent in the instruction set for the 6800 were used. The program, therefore, can be converted easily. However, the registers POINTHI and POINTLO, which are displayed as an address in the LED display of the KIM-1 microcomputer, are specific for this system. For other computers the user will have to find another way of displaying the result of the calculation.

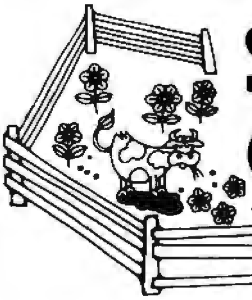
After all branch vectors have been calculated in this fashion and entered in the appropriate lines, the only open spaces in the OPC column should be the address parts of jump instructions. For jumps within the main program, it is easy to find the line with a matching entry in the label column and to enter the address of this line into the OPC columns of the lines following the one containing the jump instruction. For subroutines called from read only memory, the address has to be *looked up in the* subroutine listing.

Stock subroutines which have been written on some other occasion and which can be loaded from magnetic or paper tape frequently can be used. Normally such subroutines will be tacked on after the last memory location occupied by the main program. The KIM-1 system has a relocating loading routine for loading from magnetic tape. If this feature is not available, some area in the memory should be set aside into which the subroutines are loaded. A move program then can be executed to pull up the subroutine. For the 6502 processor I use a program called MOVBLO which requires only 14 program steps due to one very convenient addressing mode of this processor.

Unless one is very pressed for memory space, it is a good idea to have all subroutines start in lines with a 0 as the least significant digit because it is easier to keep track of the starting address after relocation. In order to be relocatable, a subroutine may not contain any absolute jump instructions and only relative addressing within the subroutine is permitted.

After the last addresses for the stock subroutines have been entered in the program assembly form, the hand assembly is completed. I have never clocked the operation, but by following the methods described, it goes much faster than one would expect. With all op codes being listed in a single column it is much easier to enter them into the machine, either from a hexadecimal keyboard or from the keyboard of a terminal. This is another occasion in which operator errors can easily occur and I proofread all programs after entry. This operation is again greatly simplified by the use of the assembly form which shows address and op code in adjacent columns.

The assembly method and the assembly aids described have been in use for several months and have been found to greatly reduce the likelihood of assembly errors. Unfortunately, this method does not protect from programming errors and the debugging of the program still is a time consuming but necessary step to follow the assembly of a program.■



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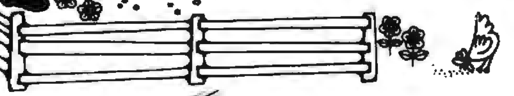

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☐ Most of us, in our rush to apply the computer in trying to solve our real world problems, jump to find the right language or the proper algorithm. Perhaps a preparatory step could help us toward realizing the most direct, creative, and efficient solution. Ackoff's book is a lesson in creative problem solving (Part One) with examples in the application of this art (Part Two). It is an enlightening book. 214 pp. $13.95 Hardcover.

Z-80 INSTRUCTION HANDBOOK
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☐ Moving over to a more powerful processor? Learn the full capabilities of the Z-80 instruction set quickly with this new Scelbi publication. It is a practical reference, using the original Zilog mnemonics, and is meant to serve as a guide for the novice, intermediate, or experienced programmer. 117 pp. $4.95

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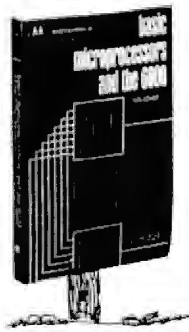
☐ This new edition reviews all areas of computer language translation and goes on to cover the syntex of complex languages and their compilation. The text is designed to educate the users of high level languages to a position where they can understand, diagnose or implement a compiler. Lee accomplishes this end with a lively and graphic style. 470 pp. $19.95.

BASIC WITH STYLE: PROGRAMMING PROVERBS
by Henry Ledgard

☐ Programmers can and should write programs that work the first time. This statement may sound idealistic to those accustomed to long hours of debugging. Yet it is the theme of this book. It contains a unique collection of "proverbs" or rules and guidelines for writing more accurate error-free programs. Newly rewritten, the book now emphasizes structural programming and all examples are in BASIC. 134 pp. $5.95.



BASIC MICROPROCESSORS AND THE 6800
by Ron Bishop

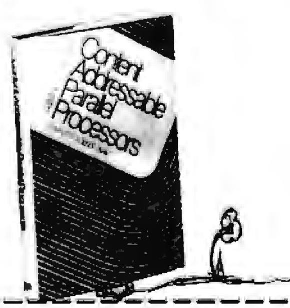
☐ This book is for people who would like to know more about microcomputers, and who do not have a technical background. Building on a foundation of basics, Ron Bishop explains the essential microcomputer parts and programming concepts. The text centers around the Motorola M6800 processor and explores in detail its instruction set, addressing modes and use. A very comprehensive introduction. 262 pp. $11.95.

9900 FAMILY SYSTEMS DESIGN AND DATA BOOK
by Texas Instruments

☐ This is a comprehensive design manual/data book for Texas Instruments' family of 16-bit microprocessor products. Nine chapters cover basic decisions in system design, hardware design, software design, the 9900 instruction set, program development, and application examples. Here is a complete information package (1000+ pages) on TI's powerful new processor. $9.95.

SOURCE BOOK FOR PROGRAMMABLE CALCULATORS
by Texas Instruments

☐ TI has put together over 60 example problems for solution on their TI58 and TI59 programmable calculators. Each example contains a description of the problem, the calculator program, guides for using the program, example solutions and references for further investigation. The problems cover topics in: number theory, algebra and trig, calculus, statistics, business,economics, biology, engineering, and physics. 416 pp. $16.50.

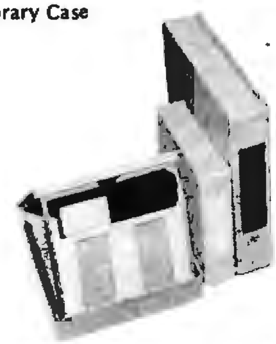


CONTENT ADDRESSABLE PARALLEL PROCESSORS
by Caxton C. Foster

☐ Content addressable memory arrays and parallel processing of all memory elements simultaneously are techniques which offer the advantages of speed and ease of programming as the cost of logic and memory elements continues to decrease. This book by Caxton C. Foster covers the theory, structure, and capabilities of CAPP machines; the known algorithms for parallel processing; applications of CAPP's; a survey of papers on distributed parallel processing; and descriptions of real CAPP machines. It is a comprehensive text, and a good introduction to the subject. 233 pp. $13.95.

What's New?

Minidisk Library Case



The Minikas-ette/10 is a minidisk sized version of the Kas-ette/10 Diskette Library Case. The cases safeguard recorded data by protecting against contaminants such as dust and debris, and offer temperature and humidity control for storage or shipping. Durably constructed of extra strong polyprolene, the library cases are finished in a beige leather type texture. Additional features include: flexible fan tabs which provide a firm vertical hold while allowing for easy media access and replacement, and the pop-up easel design places media within convenient view and reach of user. Both library cases are available from The Minicomputer Supplies Company, 963 Holmdel Keyport Rd, Holmdel NJ 07733.■

Circle 644 on inquiry card.

New Electric Wire Wrapping Tool

This new EW-8 electric wire wrapping tool from OK Machine and Tool Corp is interchangeable with its previous model EW-7D and incorporates a number of improvements at no increase in price. Rated to accept bits for wire sizes 22-30 AWG, the Model EW-8 features a reinforced Lexan housing, radio frequency (RF) interference reducing circuitry, and a high reliability motor and indexing mechanism. The tool is double insulated and weighs 14 ounces. It is available with accessory tool VIT-1 which permits easy resetting of indexing position in 45 degree increments.

The EW-8 is priced at $85.11 and the VIT-1 costs $15. Contact OK Machine and Tool Corp, 3455 Conner St, Bronx NY 10475.■

Circle 645 on inquiry card.

Where Do New Products Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by promoters of new products. If in our judgment the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

Printer Controller Supports Centronics and Dataproducts Printers

The DEC PDP-11 Line Printer Controller (DLP 11), designed to support either Centronics or Dataproducts type printers, operates on any Digital Equipment Corporation PDP-11 computer without software or hardware modification.

The DLP 11 comes complete with all necessary cabling and connectors to interface directly to the printer used. In order to simplify installation and testing, a self-test mode is provided. Low power requirement is another feature of the controller, which incorporates low power Schottky transistor-transistor logic.

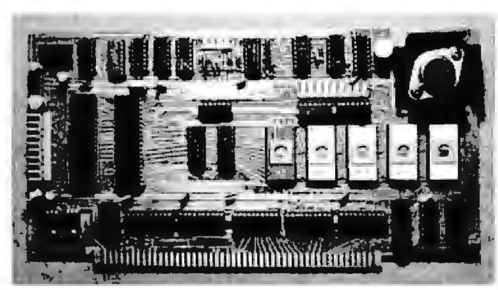
Priced at $750 in single quantities, the DLP 11 is available from DataSystems Corp, 8716 Production Av, San Diego CA 92121.■

Circle 646 on inquiry card.

An S-100 Compatible 6802/09

Micro Data Systems has announced the MD-690A, a new processor board which adds three features to those found on their MD-690. These features are: 6809 compatibility, 10 K bytes programmable read only memory, RS-232 interface provision and S-100 bus compatibility.

The MD-690A gives the user more monitor flexibility and the option of upgrading the board to accommodate the 6809 processor by Motorola. It comes complete with MONBUG, a 1K byte programmable read only memory monitor program which is software compatible with the standard Motorola MIKBUG monitor and designed to interface with most memory mapped video and graphics cards for fast input and output (IO). The board can accommodate up to 10 K bytes of 2716 erasable read only memory which may be used for 8 K byte BASIC or other firmware.



The price for the board with the 2400 bps cassette interface, 1 K byte monitor and 1 K bytes of programmable memory is $198 in kit form and $258 assembled and tested. Complete documentation including assembly and troubleshooting instructions and a comprehensive user's guide are provided. For further information write to Micro Data Systems, POB 36051, Los Angeles CA 90036.■

Circle 647 on inquiry card.

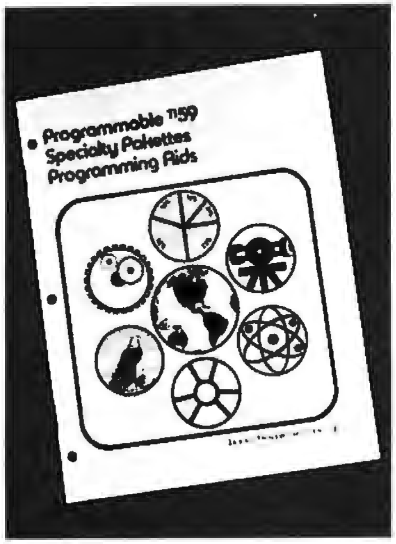
Multikeyed Indexed Sequential File Control

The keyed indexed sequential search (KISS) system enables multikey access to a user's disk files. KISS provides user selected variability of key and data lengths. The KISS system includes an indexed sequential file manager (ISFM) and a direct access file manager (DAFM). The absolute maximum number of disk accesses to retrieve any record under control of KISS is three. The system is implemented in assembler language and is designed to operate on the 8080/8085 and Z-80 based systems.

KISS is distributed as a relocatable object module on user specified formatted floppy disk. Configurations are available for IMSAI (DOS-A) and ISIS-II using PL/M, FORTRAN, assembler, and Extended BASIC. The 3 section illustrated user guide, which includes technical concept, user interface control, and file control code examples for various languages, is included in the price of $485. The user guide can be purchased separately for $22.50 plus $2.50 for postage and handling. Contact Morrow Computer and Electronic Design Inc, 315 Wilhagan Rd, Nashville TN 37217.■

Circle 544 on inquiry card.

Specialized Programming Aids for TI-59 Handheld Calculator



Specialized computer programming aids are now available from Texas Instruments for use with the TI programmable 59 handheld calculator. These aids offer easier conversion of ASCII and EBCDIC codes, routines for debugging and analyzing TMS 9900 and Intel 8080 processor programs, and a number of general programmer aids covering base conversions and logical and arithmetic operations.

The Programmer's Aid Pakette is a 64 page booklet providing detailed documentation for six full length programs: EBCDIC code converter, ASCII code converter, ASCII and EBCDIC encoder, TMS 9900 disassembler, Intel 8080 disassembler and TI programmer simulator. All require a TI-59 with attached PC-100A thermal printer, plus blank TI-59 magnetic program cards, into which the user keys the code lists for automatic entry into the calculator. The booklet format includes program listings which are keyed into the user's own magnetic cards; no additional programming is required.

Pakettes are also available on securities, statistical testing, civil engineering, electronic engineering, blackbody radiation, oil/gas/energy, astrology and TI-59/PC-100A printer utilities.

All pakettes are priced at $10 with a $1.50 handling charge plus state and local taxes. For further information write to Texas Instruments Inc, Service Facility, POB 53, Lubbock TX 79408.■

Circle 545 on inquiry card.

BYTE's Bits

About the March 1979 Cover

In the flurry of January's snowstorms, we neglected to put in an "About The Cover" text elaborating more than the title of Robert Tinney's March cover painting *Through The Trapdoor.* One or two readers took us to task for this omission, perhaps because it was not as obvious to them as to us. The lettering on the wooden block puzzle as assembled (if you could do so) spells out the word *plaintext,* in two lines. As the plaintext is cranked through the black box of a trapdoor algorithm, it becomes a jumbled form known as ciphertext. Here we symbolize the trapdoor by a hole in a sheet of translucent material, and the trapdoor jumbles the puzzle parts as they fall through the hole.

This of course brings up a challenge. Who will be the first reader with skills at woodcrafts to rationalize the design of such a woodblock in order to create a real puzzle? The actual pieces should be close to those imagined in this picture, but certainly not identical since there is no way to assemble the pieces shown into a cube which spells "plain" and "text" along two rows.■

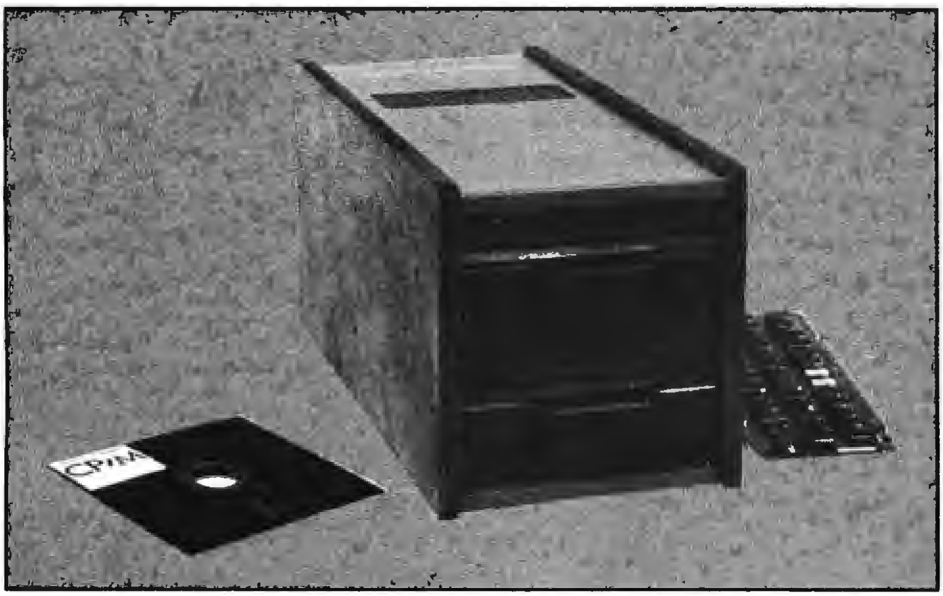
Double Density Floppy Disk Storage System

This new double density floppy disk storage system, the Delta-1, has been introduced by Meca, POB 696, 7026 Old Woman's Spring Rd, Yucca Valley CA 92284. The Delta-1 provides up to 200 K bytes of storage on a single 5¼ inch drive. Included with the Delta-1 disk system is the MFM S-100 disk controller which supports up to three SA-400 disk drives. Individuals who now own a Meca Alpha-1 tape system can use the MFM disk controller to combine the Alpha-1 and Delta-1 into a fully integrated tape and disk storage system. North Star owners may take advantage of the availability of the MFM disk controller card to double disk storage space from 90 K to 180 K bytes. The price for the controller card alone is $199.

Available software includes a CP/M disk operating system with editor, assembler, debugger and BASIC-E for $98. Microsoft Extended Disk BASIC is offered for $195. Several applications programs are available which operate with both the Delta-1 and Alpha-1. An introductory price of $699 includes the minifloppy single-sided disk drive, MFM disk controller, power supply, connectors and cable, complete documentation, and Meca disk operating system.■

Circle 603 on inquiry card.

Dual and Single Drive Expandable Floppy Disk Systems



A new family of expandable floppy disk systems, called EXP, is available from Micromation Inc, 524 Union St, San Francisco CA 94133. EXP is a complete floppy system using standard 8 inch disks and a write protect and front panel activity light as standard. The system uses drives supplied by Memorex. Each drive offers a full 265 K bytes of storage in IBM 3740 soft sectored format.

EXP is fully supported by software. Users are offered CP/M as one option. BASIC, FORTRAN, or complete business application and word processing packages are also offered.

EXP is a complete, fully assembled and tested floppy disk storage system. The total system includes drives, S-100 controller, power supply, and wood and metal enclosure. The EXP-1 single drive system is priced at $1195 and the EXP-2 dual drive system is $1895, and an optional double density controller (for $300) permits doubling the actual density of data on each disk.■

Circle 604 on inquiry card.

Floppy Disk System from Charles River Data Systems

Charles River Data is offering its MF-11 LSI-11 floppy disk system with the DEC LSI-11/2 and associated Digital Equipment Corp (DEC) plug-in memory. The MF 11/2 is functionally identical in performance characteristics to the PDP 11VOS but uses only 10½ inches of panel height and is available at a lower price. The 10½ inch enclosure holds the DEC processor, two Shugart floppy disk drives with controller, power supply, slides for rack mounting, and the DEC H9270 back panel. An 8 quad slot backplane is also available.

The controller and interface card provides total software and media compatibility between the DEC processor and the floppy disk system, which allows use with any of the PDP 11VO3 software packages. It also provides bootstrap loader, self-test and IBM 3740 formatter. Contact Charles River Data Systems Inc, 4 Tech Cir, Natick MA 01760.■

Circle 605 on inquiry card.

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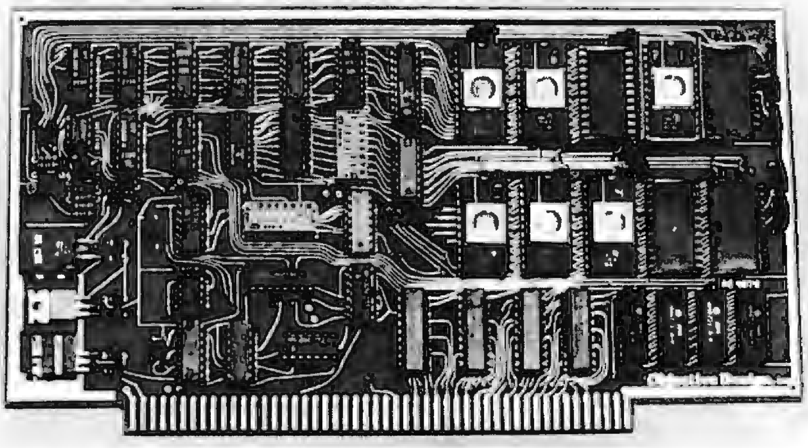
S-100 Card Holds and Programs 2716, 2708 Programmable Read Only Memories

A maximum of eight TMS 2716 or 2708 16 K or 8 K bytes programmable read only memories are held on this new programming and storage board called the Databank. The board will also program memories by means of two special sockets. One of these sockets provides a connection to an external programming station while the other socket allows the programming of memories on the Databank. Each of the eight memories may be individually switched into or out of the system address space. The entire board can be disabled and enabled by I/O (input/output) commands.

In addition to the programmable read only memories, the Databank will hold 1 K or 2 K bytes of 2114 programmable memory. The memory will operate as bus memory or can be substituted by software command for any of the programmable read only memories. A memory in the programming socket also has this substitution ability. All programming voltages are provided by the Databank board circuitry.

The board is available in kit form at the following prices: DB00 (without programmable memory) $199.95; DB08 (1 K byte programmable memory) $219.95; DB16 (2 K byte programmable memory) $239.95 with shipping charges of $5 in the US and Canada and $25 overseas. For further information, contact Objective Design Inc, POB 20325, Tallahassee FL 32304.■

Circle 531 on inquiry card.



Associative Computer Memory Available from Semionics Associates

Content addressable or associative computer memory is available from Semionics Associates, 41 Tunnel Rd, Berkeley CA 94705. Called REM (recognition memory), it differs from conventional memory by eliminating serial searching. An item may be accessed simply by being named. REM can be written into and read from like ordinary memory, but has parallel processing functions, including six types of recognize and multiwrite. The recognition operations replace serial searching, while multiwrite allows the processor to write into multiple locations with a single instruction. Individual bit masking may be applied to all of the operations, including ordinary (location accessed) read and write. A data processing system with these functions is known as a CAPP (content addressable parallel processor). Ideal for pattern recognition and information retrieval applications, it is also capable of performing parallel arithmetic operations.

Semionics' first product is an add-in recognition memory for microcomputers having the S-100 bus. Called REM S-100, the board converts the microcomputer to a CAPP by adding new instructions to the instruction set of the processor. The board is organized to make these additional instructions possible without any alteration to the processor.

Recognition memory is organized in 8 bit words and 256 word REM records. It is a static memory with an access time of 200 ns for a single memory location, and recognize or multiwrite time, for all REM records of 4 μs. This time does not increase with size of memory. In a system with multiple REM boards, all of these are accessed in parallel during a recognize or multiwrite operation.

The REM S-100 add-in recognition memory board has a capacity of 8 K bytes and is priced at $525.■

Circle 533 on inquiry card.

Two New Boards for S-100 Systems

This 8 K byte read only memory and programmable memory board is ideal for S-100 systems which require both types of memory. It will replace two boards in most systems, reducing cost, inventory, and motherboard slots. The independent addressing and wait state control make the board as flexible as two separate boards. The control and I/O board has 12 inputs and four high current outputs. The Triac control allows direct computer control of AC equipment. Counters are valuable for process control or counting instruments and the built-in timer gives the computer a dual count per minute (or second) capability.

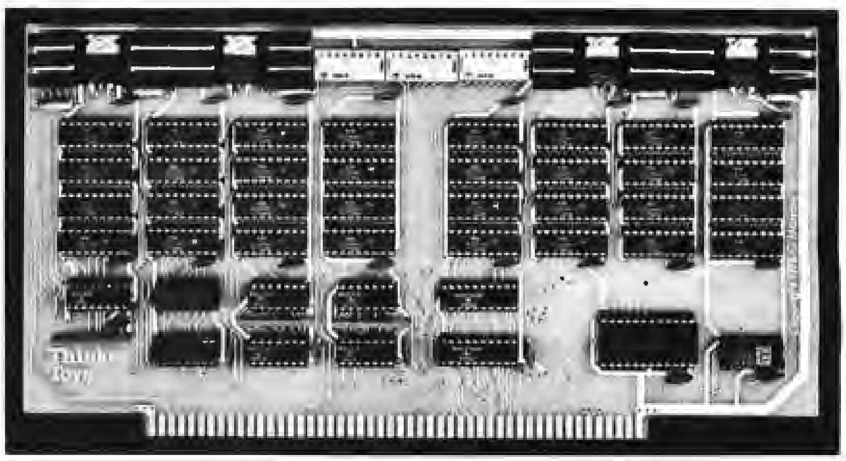
Assembled and tested, the boards sell for $195 each. OEM quantity discounts are available. For more information, contact Tri Mark Engineering, 12402 W Kingsgate, Knoxville TN 37922.■

Circle 532 on inquiry card.

Low Price 16 K Byte Static Memory Board

This 16 K byte static memory board, designated SupeRam 16, has been designed for S-100 microcomputer systems. SupeRam is a complete kit featuring four independently addressable and write-protectable 4 K byte blocks. The compact control design uses only 11 integrated circuits. All signals are fully buffered, including address and data lines. SupeRam 16 K byte is priced at $299 and available from Thinker Toys, 1201 10th St, Berkeley CA 94710.■

Circle 534 on inquiry card.



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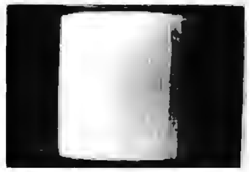
PROCESSING SYSTEM



GRAY LEVELS

OUR VP1 VIDEO SYSTEM CONSISTS OF THE FOLLOWING KITS:

- CCD 202C SOLID STATE VIDEO CAMERA KIT ASSEMBLED & TESTED $499.00
- VP-1 COMPUTER/VIDEO INTERFACE SYSTEM (3 BOARDS) ASSEMBLED & TESTED $999.00
- ASSEMBLED 8K MEMORY BOARD (OPTIONAL)................ $235.00

THIS VIDEO COMPUTER KIT CAN WORK WITH THE GE, REDICON, OR ANY OTHER 128 x 128 SENSOR CAMERA

THIS REMARKABLE VP-1 COMPUTER/INTERFACE KIT HAS THE FOLLOWING:

FEATURES
- IT PRODUCES COMPOSITE VIDEO OUTPUT IN A 128 x 128 MATRIX FROM A DIRECT MONITOR CONNECTION USING 8K OF MEMORY
- THE SYSTEM USES A STANDARD S 100 BUSS
- WILL NOT TIE UP COMPUTER SOFTWARE WHEN NOT ADDRESSED
- IT DISPLAYS CONTINUOUSLY WHEN NOT ADDRESSED
- IT MAY PRODUCE PSEUDO COLOR AND/OR GRAPHICS (UP TO 16 GREY LEVELS, 4 BIT BINARY)

THE CAMERA WILL TAKE BETWEEN 15 AND 100 FRAMES/SECOND. THE CAMERA CONNECTS TO THE PROCESSOR WITH SEVEN LINES. THIS INCLUDES VIDEO AND TIMING SIGNALS

APPLICATIONS
- CONTINUOUS SURVEILLANCE
- INSPECTION OF MOVING PARTS WITH PROPER STROBING
- VISUAL GRAPHIC INPUT TO A COMPUTER
- CHARACTER OR PATTERN RECOGNITION
- PICTURES MAY BE TAKEN DIRECTLY FROM A TV WITHOUT ELECTRICAL CONNECTIONS
- THE INTERFACE KIT MAY BE USED SEPARATELY AS A 128 x 128 16 LEVEL GRAPHIC DISPLAY

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(OV PROTECT)

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4001	18	4019	37	4050 -	35	74C74 -	45
4002	18	4020	90	4053 -	1.10	74C83 -	1 15
4006 -	95	4021 -	90	4055 -	1.25	74C86	40
4007	18	4022 -	90	4066 -	.70	74C93	75
4009	37	4023	18	4069 -	.45	74C151	1 40
4010 -	37	4024 -	75	4071 -	18	74C160	1 05
4011 -	18	4025	18	4072 -	.21	74C161	1 05
4012	18	4027 -	37	4076 -	.97	74C174	1 05
4013 -	29	4028	80	4516 -	.96	74C175	1 05
4014 -	75	4029	95	4520	70	74C192	1 20
4015 -	75	4030 -	33	74C00 -	22	74C193	1 20
4016 -	29	4035 -	97	74C02 -	22	74C901	48
4017	1 05	4042	65	74C08 -	22	74C902	48
4018 -	90	4049	35	74C23 -	65	74C914	1.70

1488 RS232 INTERFACE	$1 40	UPD410 1 4K STAT RAM	[illegible]
1489 RS232 INTERFACE	1 25	4116-3	[illegible]
[illegible] TRI STATE STAT [illegible]	[illegible]	5280/2107B 4K DYN RAM	3 40
2513 CHARAC GEN [illegible]	6 75	TMS 4050	[illegible]
[illegible] 32 BIT SR	[illegible]	5204 4K PROM	[illegible]
[illegible] STATIC SHIFT REG	1 95	82S23	1 95
2708 8K EPROM [illegible]	12 95	82S129	[illegible]
[illegible] DYN S R	[illegible]	AY5 1013 UART	5 25
2518 [illegible]	[illegible]	TR1 602B	[illegible]
2102 1 (450 ns)	[illegible]	8700C [illegible] 8 BIT AD CONVERT	[illegible]
21L02 (450 ns)	1 25	PT 1482 B PSAT	[illegible]
[illegible]	[illegible]	8080A	[illegible]
[illegible]	1 95	8212	[illegible]
2101 1 256 x 4 STATIC	2 49	8214	[illegible]
2111 1 256 x 4 STATIC	2 49	8224	[illegible]
2112 1 256 x 4 STATIC	2 75	8251	4 90
2114 4K STAT RAM (450 ns)	8 90	8255	5 90
2117 16K DYN RAM	[illegible]		

8130 2 95 | 8T380 [illegible] | 8834 2 25
8131 2 95 | 8830 2 95 | 8837 2 25
8838 2 25

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2.000 MHz
4 000 MHz
5 000 MHz
6.000 MHz
8 000 MHz
10 000 MHz
20.000 MHz

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50 cond. - 90/per foot

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FCS 8024 4 digit C.C 6" display	$5.95	DL 747 C.A. 6"	$1.25
FND 503 C.C. 5"	$ 85	HP3400 .8"CC	$1.95
FND 510 C.A 5"	$ 85	HP3405 .8"CA	$1.95
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2N2646 UJT	$ 45
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CCD 202C 100x100 Image Sensor ... $145.00

VERIPAX PC BOARD............... $4.00
This board is a 1/16" single sided paper epoxy board, 4½"x6½" DRILLED and ETCHED which will hold up to 21 single 14 pin IC's or 8,16 or LSI DIP IC's with busses for power supply connector.

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RED, YELLOW, GREEN, or AMBER LARGE LED's 2" .... 6/$1.00
TIL-118 OPTO-ISOLATOR ...... $ 75
MCT-6 OPTO ISOLATOR .... $ 80
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MCM 6571A 7 x 9 character gen $ 10.75

UNIVERSAL 4Kx8 MEMORY BOARD KIT $69.95
32-2102-1 fully buffered, 16 address lines, on board decoding for any 4 of 64 pages, standard 44 pin buss, may be used with F 8 & KIM

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200	07	20	35	1 15	4 25	6.50
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600	11	30	70	1 80	8 50	12 50
800	15	35	90	2 30	10 50	16.50
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320T - 5, 12, 15 or 24	$ 1 10	79 MG	$ 1 35

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2N6233-NPN SWITCHING POWER	$ 1.95
MRF-8004 a CB RF Transistor NPN	$ .75
2N3772 NPN Si TO 3	$ 1.00
2N1546 PNP GE TO-3	$ .75
2N4908 PNP Si TO 3	$ 1 00
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2N3137 NPN SI RF	$ .55
2N3919 NPN Si TO 3 RF	$ 1 50
2N1420 NPN SI TO 5	3/$ 1.00
2N3767 NPN Si TO 66	$ 70
2N2222 NPN Si TO-18	5/$ 1 00
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2N3638 PNP Si TO 5	5/$ 1 00
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TTL IC SERIES

7400 -	15	7446 -	[illegible]	74151 -	.61
7401 -	15	7447 -	[illegible]	74153 -	.61
7402	15	7448 -	[illegible]	74154 -	.94
7403 -	15	7450	18	74156 -	[illegible]
7404 -	18	7472 -	.28	74157 -	[illegible]
7405 -	18	7473 -	.28	74158 -	.65
7406 -	.27	7474 -	.28	74161 -	[illegible]
7407	24	7475 -	.45	74162 -	[illegible]
7408	18	7476 -	.30	74163 -	[illegible]
7409	18	7480 -	.31	74164	.85
7410 -	.15	7483 -	.68	74165 -	[illegible]
7411 -	.18	7485 -	.87	74173 -	1 20
7412 -	18	7486 -	.28	74174 -	[illegible]
7413 -	[illegible]	7489 -	1.25	74175 -	[illegible]
7414 -	.60	7490 -	.47	74176 -	.75
7416	22	7491 -	[illegible]	74177 -	.75
7417 -	.25	7492 -	.43	74180 -	[illegible]
7420	18	7493 -	.43	74181 -	[illegible]
7425	.30	7494 -	.67	74190 -	1.00
7426 -	22	7495 -	[illegible]	74191 -	[illegible]
7427	.28	7496 -	[illegible]	74192 -	[illegible]
7430	18	7497 -	[illegible]	74193 -	[illegible]
7432	.22	74107 -	.28	74194 -	[illegible]
7437 -	22	74121 -	.28	74195 -	[illegible]
7438 -	.22	74122 -	.40	74196 -	[illegible]
7440	15	74123 -	45	74197 -	[illegible]
7441 -	.70	74125 -	40	74279 -	[illegible]
7442 -	.45	74126 -	40	74298 -	[illegible]
7445	[illegible]	74145 -	[illegible]	74365 -	.67
		74148 -	1 10	74393 -	1.75
		74150 -	1 00	74[illegible] -	1.[illegible]

DATA CASSETTES 1/2 HR $ 95

14 pin headers 3/$1.00

MM 5387AA new clock chip which will directly drive LED's 12/24 hrs, 1 supply & alarm $5.95

NO 30 WIRE WRAP WIRE SINGLE STRAND 100' $1 40

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MTA 106 SPDT	$ .95
MTA 206 DPDT	$ 1 70
MTA 206 P-DPDT CENTER OFF	$ 1.85
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PRV	2A	6A	25A
100			1.30
200	.75	1.25	2 00
400	.95	1.50	3.00
600	1.20	1 75	4.00

DIP SOCKETS
8 PIN .17 24 PIN .35
14 PIN .20 28 PIN .40
16 PIN .22 40 PIN .60
18 PIN .25

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Si 1010 G 10 WATTS	$ 7.80
Si 1020 G 20 WATTS	$16.70
Si 1050 G 50 WATTS	$28.50

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.47UF 35V 5/$1 00	10UF 10V $ 25
.68UF 35V 5/$1.00	22UF 25V $ 40
1UF 35V 5/$1.00	15UF 35V 3/$1 00
2 2UF 20V 5/$1.00	30UF 6V 5/$1.00
3 3UF 20V 4/$1.00	33UF 20V $ 40
4.7UF 15V 5/$1.00	47UF 20V $.35
	68UF 15V $ 50

74LS SERIES

74LS00 -	.31	74LS138 -	[illegible]
74LS02 -	.31	74LS139 -	[illegible]
74LS03 -	.31	74LS151 -	[illegible]
74LS04	.34	74LS153 -	[illegible]
74LS05 -	.34	74LS155 -	[illegible]
74LS08 -	.34	74LS156 -	[illegible]
74LS09 -	.34	74LS157 -	[illegible]
74LS10 -	.31	74LS160 -	1.21
74LS11 -	.31	74LS161 -	1.21
74LS13 -	[illegible]	74LS162 -	1.21
74LS14 -	1.[illegible]	74LS163 -	1.21
74LS15	.31	74LS164 -	1.34
74LS20 -	.31	74LS165 -	1.43
74LS21 -	.31	74LS166 -	1.43
74LS22	.31	74LS170 -	[illegible]
74LS26 -	[illegible]	74LS173 -	[illegible]
74LS27	[illegible]	74LS174 -	1.36
74LS28	[illegible]	74LS175 -	1.36
74LS30 -	.31	74LS181 -	2.81
74LS32	[illegible]	74LS190 -	1.48
74LS37	.31	74LS191 -	1 48
74LS38	.37	74LS192 -	1 19
74LS40 -	.31	74LS193 -	1 48
74LS42	[illegible]	74LS195 -	[illegible]
74LS51 -	.34	74LS196 -	[illegible]
74LS54	.34	74LS197 -	[illegible]
74LS73 -	.47	74LS241 -	[illegible]
74LS74	[illegible]	74LS257 -	1 19
74LS75 -	.47	74LS258 -	1 19
74LS86	.47	74LS260 -	[illegible]
74LS90 -	[illegible]	74LS365 -	.40
74LS92	.47	74LS366 -	.55
74LS93	[illegible]	74LS367 -	[illegible]
74LS109	[illegible]	74LS368 -	[illegible]
74LS112 -	.47	74LS373 -	[illegible]
74LS113 -	.47	74LS386 -	[illegible]
74LS114 -	[illegible]	74LS390 -	[illegible]
74LS124 -	1.35	74LS393 -	[illegible]
74LS136 -	[illegible]	74LS395 -	[illegible]
74LS138 -	[illegible]	74LS398	[illegible]
74LS132 -	[illegible]	74LS670 -	2 70

LINEAR CIRCUITS

LM 101 -	75
LM 301/748	25
LM307 -	30
LM 308 -	75
LM 311 -	75
LM 318 -	1 20
LM 324 -	70
LM 339 -	1 10
LM 358 -	70
LM 370 -	1 15
LM 377 -	1 60
LM 380 -	95
LM 387 -	1 25
LM386 -	80
LM 387	1 25
LM 537	2 50
LM 553	- 2 50
LM 555 -	40
LM 556 -	85
NE540L	- 2 75
560	- 2 00
565 -	95
566 -	1 10
567	1 10
703 -	90
733	75
709 -	25
710 -	35
711CH -	40
741C or V -	29
747 -	50
LM 1310 -	2 50
1456 -	95
1458 -	50
3900 -	40
8038CC -	3 90
781 -	1 95
LF356H -	1.20

TRIACS / SCR'S

PRV	TRIACS 1A	TRIACS 10A	TRIACS 25A	SCR'S 1.5A	SCR'S 6A	SCR'S 35A
100	.40	.70	1.30	.40	.50	1.20
200	.70	1.10	1.75	.60	.70	1.60
400	1.10	1.60	2.60	1.00	1.20	2.20
600	1.70	2.30	3.60		1.50	3.00

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Circle 340 on inquiry card.

MIT Offers Video Tape Course in Semiconductor Devices

A course in semiconductor devices by Professor Clifton Fonstad is being offered by Massachusetts Institute of Technology in the form of tutored video instruction. The course consists of 38 1 hour MIT classes plus problem sets, quizzes and solutions.

Starting with a basic presentation of the energy band viewpoint, this course deals with the physics, modeling, fabrication and application of semiconductor devices. Silicon devices are emphasized in the context of integrated circuits. Physical models for devices are developed to a point sufficient for viewers to understand the design and use of semiconductor devices. The course begins with a presentation of much of the required physics, so that students with a wide diversity of backgrounds should be able to use the course effectively.

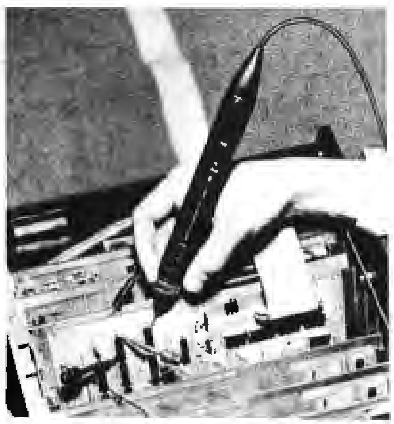
The video tapes are delivered in four shipments of nine to ten tapes each. They may be kept up to six weeks, or the course may be accelerated by requesting earlier shipment of the next course and returning tapes of the completed section.

The fee for participating in TVI is \$900 plus \$150 per noncredit student. There is no additional charge if the number of students exceeds 25. Contact Dr John T. Lynch, director, Tutored Video Instruction, Room 9-267, Massachusetts Institute of Technology, Cambridge MA 02139.■

Circle 608 on inquiry card.

Logic Probe for TTL and CMOS Testing from Heath

Heath Company has released the IT-7410/ST-7410 Logic Probes which are designed for in circuit testing of TTL (transistor-transistor logic) and CMOS integrated circuits. Features include switch selection of threshold levels for either TTL or CMOS circuitry and lamps that turn on when the input voltage crosses the appropriate level. A memory circuit is incorporated in the design of the unit to turn on a light emitting diode when either threshold level is crossed.



The new probes provide true logic level detection at high frequencies (no AC coupled) and detection of pulses as short as 10 ns. Upper frequency limits are 100 MHz (TTL or CMOS at 5 VDC squarewave) and 80 MHz (CMOS at 15 VDC squarewave). Power for the Logic Probe is drawn from the circuit under test via two spring loaded, insulated clips. A ground lead is provided for high frequency operation. Probe overload protection is 50 VDC continuous and 175 VDC for 5 seconds.

The IT-7410 is the kit version and is priced at \$39.95 and the ST-7410 is the assembled version and sells for \$64.95. For more information about the Logic Probes, write to the Heath Company, Dept. 350-690, Benton Harbor MI 49022.■

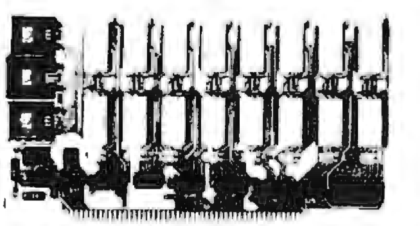
Circle 609 on inquiry card.

Speak to Me in MICR

This kit of magnetic ink character recognition letters makes it possible to personalize your own shirts, tote bags, jeans, director's chair covers, and other canvas or cotton items with a household iron. The software applications kit is designed to help the authors of such phrases as APL polisher, computer simulation, loose circuits, terminal case, and bubble logic, communicate creatively even when away from the computer. Each kit contains 118 letters, 40 numbers and 44 computer widgets with complete instructions for application. The kit is \$3.95 or \$7 for two (add 10% for postage). Contact Martha Herman, 114 W 17th St, New York NY 10011. Specify blue or white type when ordering.■

Circle 658 on inquiry card.

16K EPROM CARD-S 100 BUSS



$59.95 KIT

OUR BEST SELLING KIT!

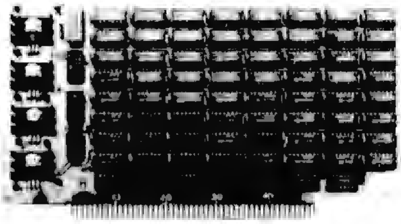
USES 2708's!

Thousands of personal and business systems around the world use this board with complete satisfaction. Puts 16K of software on line at **ALL TIMES!** Kit features a top quality soldermasked and silk-screened PC board and first run parts and sockets. All parts (except 2708's) are included. Any number of EPROM locations may be disabled to avoid any memory conflicts. Fully buffered and has WAIT STATE capabilities.

OUR 450NS 2708'S ARE $8.95 EA. WITH PURCHASE OF KIT

ASSEMBLED AND FULLY TESTED ADD $25

8K LOW POWER RAM KIT-S 100 BUSS
250 NS SALE!



ADD $5 FOR 250NS!

$129 KIT

(450 NS RAMS!)

Thousands of computer systems rely on this rugged, work horse, RAM board. Designed for error-free, NO HASSLE, systems use.

KIT FEATURES:

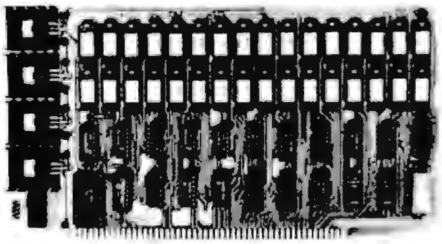
1. Doubled sided PC Board with solder mask and silk screen layout. Gold plated contact fingers.
2. All sockets included.
3. Fully buffered on all address and data lines.
4. Phantom is jumper selectable to pin 67.
5. FOUR 7805 regulators are provided on card.

Blank PC Board w/Documentation **$29.95**
Low Profile Socket Set...**13.50**
Support IC's (TTL & Regulators) **$9.75**
Bypass CAP's (Disc & Tantalums) **$4.50**

ASSEMBLED AND FULLY BURNED IN ADD $30

16K STATIC RAM KIT-S 100 BUSS

$295 KIT



FULLY STATIC, AT DYNAMIC PRICES

WHY THE 2114 RAM CHIP?

We feel the 2114 will be the next industry standard RAM chip (like the 2102 was) This means price, availability, and quality will all be good! Next, the 2114 is FULLY STATIC! We feel this is the ONLY way to go on the S-100 Buss! We've all heard the HORROR stories about some Dynamic Ram Boards having trouble with DMA and FLOPPY DISC DRIVES Who needs these kinds of problems? And finally, even among other 4K Static RAM's the 2114 stands out! Not all 4K static Rams are created equal! Some of the other 4K's have **clocked** chip enable lines and various timing windows **just as critical** as Dynamic RAM's Some of our competitor's 16K boards use these "tricky" devices But not us! The 2114 is the ONLY logical choice for a trouble-free, straightforward design

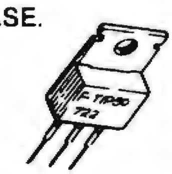
KIT FEATURES:

1. Addressable as four separate 4K Blocks.
2. ON BOARD BANK SELECT circuitry (Cromemco Standard!) Allows up to 512K on line!
3. Uses 2114 (450NS) 4K Static Rams
4. ON BOARD SELECTABLE WAIT STATES
5. Double sided PC Board, with solder mask and silk screened layout. Gold plated contact fingers.
6. All address and data lines fully buffered
7. Kit includes ALL parts and sockets
8. PHANTOM is jumpered to PIN 67
9. LOW POWER: under 2 amps TYPICAL from the +8 Volt Buss
10. Blank PC Board can be populated as any multiple of 4K.

BLANK PC BOARD W/DATA—**$33**
LOW PROFILE SOCKET SET—**$12**
SUPPORT IC'S & CAPS—**$19.95**
ASSEMBLED & TESTED—**ADD $30**
2114 RAM'S—**8 FOR $69.95**

COMPLEMENTARY POWER TRANSISTORS

SILICON NPN AND PNP. TO-220 CASE.
VCEO - 40V PD - 30 WATTS
FOR AUDIO POWER AMPS, ETC



TIP29 - NPN
TIP30 - PNP

YOUR CHOICE
3 FOR $1

16K DYNAMIC RAM CHIP

16K X 1 Bits 16 Pin Package Same as Mostek 4116-4 250 NS access 410 NS cycle time. Our best price yet for this state of the art RAM 32K and 64K RAM boards using this chip are readily available. These are new, fully guaranteed devices by a major mfg **VERY LIMITED STOCK!**

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NOT ASSOCIATED WITH DIGITAL RESEARCH OF CALIFORNIA, THE SUPPLIERS OF CPM SOFTWARE.

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450 NS!

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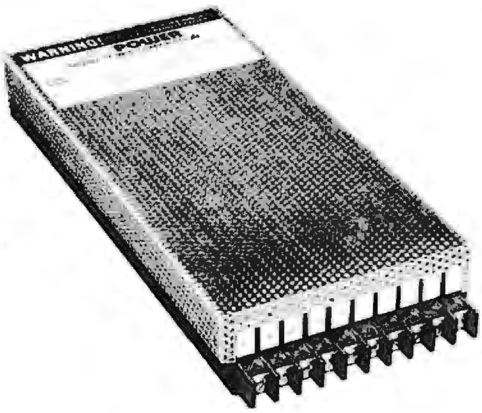
Circle 92 on inquiry card.

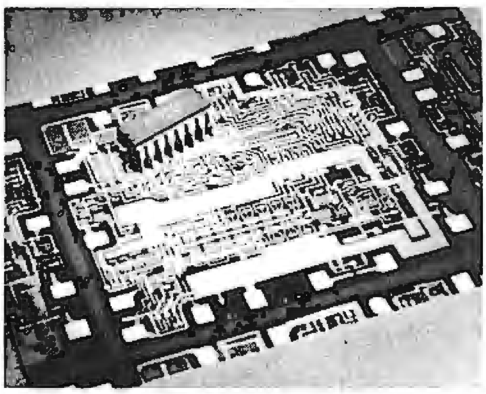
Switching Power Supplies With Power Fail Signal



Circle 559 on inquiry card.

This new series of switching power supplies has been designed for small computers utilizing nonvolatile memories. The DS151 series features a power fail signal as standard feature. Should a power failure of one half cycle occur, the TTL compatible power fail signal warns the computer (for example with an interrupt) that primary AC power has been lost allowing the program in the system to store the state of the machine in nonvolatile memory before DC power fails several milliseconds later. This power failure warning feature thus allows for "fail safe" operation when power is interrupted. Three models are presently available: 5 V at 30 A, 12 V at 12 A, or 15 V at 10 A. All are regulated to within plus or minus 0.1%. The power supplies will operate within a wide input voltage range from 100 to 130 VAC. The power fail series is priced at $194 in production quantities (1000) and $289 for prototype quantities. Contact Digital Power Corp, 2060 The Alameda, San Jose CA 95126.■

High Speed Monolithic 8 Bit Digital to Analog Converter



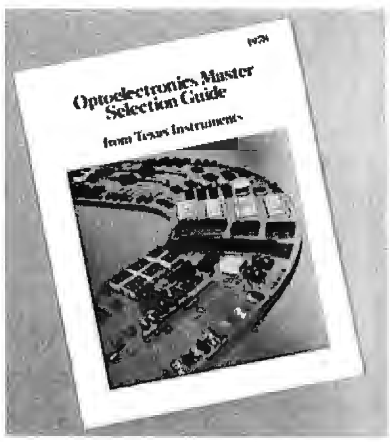
A 10 ns settling time enables Motorola's new state of the art MC-10318 to convert digital information into analog signals in high speed instrumentation, digital displays, storage oscilloscopes, radar processing and television broadcast applications.

Accurate to 8 bits (±½ least significant bit), and monotonic over a 0 to 70° C (32° to 158° F) temperature range, the new digital to analog converter can operate in systems with data rates above 25 MHz. Inputs are compatible with MECL 10,000 logic, for direct interfacing with high speed processing systems. Operating from a standard −5.2 V power supply, the integrated circuits complementary outputs can produce 51 mA full scale over a compliance range from −1.3 V to +2.5 V, while dissipation is typically less than 500 mW. Maximum nonlinearity is ±0.19 percent of full scale.

The 16 pin ceramic dual-in-line package device is priced at $26 in quantities of 100 thru 999. For further information, contact Motorola Semiconductor Products Inc, POB 20912, Phoenix, AZ 85036.■

Circle 561 on inquiry card.

Guide to Texas Instruments Line of Optoelectronic Devices



A publication entitled *Optoelectronics Master Selection Guide* is available free from Texas Instruments Inc, POB 5012, M/S 308, Dallas TX 75222. CL-346 is a 56 page product selection guide and catalog designed to provide designers with a reference to TI's line of optoelectronic devices.

This publication covers infrared emitters and detectors, light emitting diodes, optocouplers, arrays and assemblies, single digit displays, multidigit displays, hermetic displays, and electro-optical components. Packaging information and key features of all TI opto-products are included. Basic features and descriptions are presented in short form to help in the selection of the proper devices. A complete cross-reference guide and an alphanumeric index of all devices in the guide are included.■

Circle 562 on inquiry card.

Floppy Disk Read Amplifier From Motorola

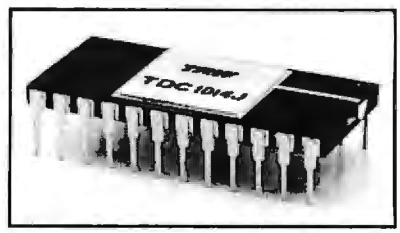
Motorola's new MC3470 floppy disk read amplifier combines linear and digital functions ordinarily requiring several integrated circuits to accurately extract digital information from magnetic floppy disk read heads. The disk signal, which may be noisy and exhibit a number of waveform variations, is processed by the integrated circuit to produce a standardized logic output.

Accepting a differential input from the magnetic head, in the presence of common-mode noise, the signal is amplified, routed through an external RC (resistor capacitor) filter network, and then sharpened by an active differentiator. Peaks are detected by a comparator, which drives a digital time domain filter consisting of pulse generators, a oneshot multivibrator and a D type flip flop. The resulting digital output exhibits none of the amplitude variations and jitter present in the input, and can drive standard logic forms with a guaranteed maximum peak shift of 3.5 percent.

The MC3470 floppy disk read amplifier is available in an 18 pin plastic dual-in-line package at the 100 piece price of $5.95. For more information, contact Motorola Semiconductor Products Inc, POB 20912, Phoenix AZ 85036.■

Circle 560 on inquiry card.

Video Speed Analog to Digital Converter



This new analog to digital converter integrated circuit, the TDC 1014J, features 6 bit resolution and a 30 MHz sample rate. Packaged in a 24 pin dual-in-line package, the device provides video speed data conversion without the need for an external sample and hold circuit.

The TDC 1014J requires only a single convert command to digitize an analog waveform between 0 and −1 V. Included in the circuit are 63 strobed comparators, encoding logic, and a 6 bit data latch with TTL outputs. Output mode controls provide either straight binary or two's complement data.

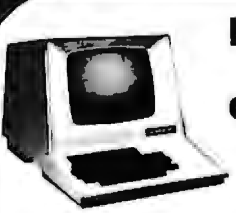
The TDC 1014J is priced at $186 in quantities of 100. Contact TRW LSI Products, POB 1125, Redondo Beach CA 90278.■

Circle 563 on inquiry card.

California Digital

Post Office Box 3097 B • Torrance, California 90503

Hazeltine 1400



cost effective
CRT TERMINAL
$735 plus shipping

The Hazeltine 1400 Vidio Display Terminal is designed to optimize interactive real-time operations. The interface is capable of either local or remote connection through an EIA RS232-C interface at baud rates that are switch selectable up to 9600 baud.

- All 128 ASCII Codes
- 64 Displayable Characters
- 24 Lines; 12 inch Screen
- 80 Characters per Line
- Self Diagnostic Test

Immediate Delivery

S-100 Mother Board

Quiet Buss
$29.95
8803-18
18 slot
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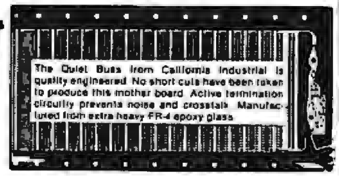

The Quiet Buss from California Industrial is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy FR-4 epoxy glass.

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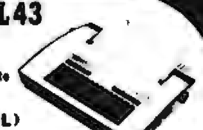
Even if we have to give them away, we're going to ship more 43's in 1979 than the aggregate of all our competitors.



Model 43AAA (TTL)

EACH	3	10	25
$925.	875.	850.	825.

RS-232 Interface "K" Add $75.00 plus shipping

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$449.50

$29.95 BOX of 10 DISKETTES

Verbatim. APPLE/TRS-80 Mini - Soft sector

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your choice
DB25P male plug & hood
or
DB25S female
$3.95

Qty.	fe.	male	hd.
10	3.45	2.45	1.15
25	3.15	2.25	1.05
100	2.85	1.90	.95
500	2.25	1.60	.85
1K	1.97	1.37	.73

Edge Connectors

GOLD 100 PIN IMSAI/ALTAIR

Imsai solder .125x.250	$4.95	3/$10.00
Imsai w/w .125 centers	$4.95	3/$13.00
Altair soldertail .140 row	$5.95	3/$15.00
SPECIALS		
22/44 Kim eyelet .156"	$1.95	3/$5.00
25/50 solder tab .156"	$1.09	3/$2.00
36/72 wide post w/w .156	$1.95	3/$5.00

UNIVAC KEYBOARD

$24.88

The famous Sperry Univac 1710 Hollerith keyboard assembly is now available from California Industrial for only $24.88. The ideal computer input device for accountants and mathematicians. The numeric keys are placed on the lower three rows to resemble a ten key adding machine. This format allows one handed numeric data entry. Original cost was $380. Used but guaranteed in excellent condition. Complete with documentation.

World Power TRS-80 Interface

MSIOa I/O Modual......	$129.95
MCCa master control...	$149.95
RSBa S-100 interface....	$289.95
EPR80a Eprom prog....	$159.95
EPR100a Eprom prog. . .	$159.95

Data sheet available upon request

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Mullen $34.95
Facilitates design and troubleshooting of all S-100 microsystems. Includes logic probe along with high-low and pulse LED display.
Also available, the Mullin CB-1 controller board $88.

S-100 PROTOTYPE BOARD

$19.98

GP100-Maximum design versatility along with standard address decoding and buffering for S100 systems. Room for 32 uncommitted 16 pin IC's. 5 bus buffer & decoding chips. 1 DIP address select switch, a 5 volt regulator and more.
WW100-Wire wrap breadboard, similar to the GP100. Allows wire wrap of all sizes of sockets in any sizes of sockets in any combination. An extra regulator position for multiple voltage applications.

MEMORY

TRS-80 APPLE II $65
16k memory (8) 4116's

• As you may be aware, publishers require advertisers to submit their ad copy 60 to 90 days prior to "press" date. That much lead time in a volatile market place, such as memory circuits, makes it extremely difficult to project future cost and availability.
To obtain the best pricing on memory we have made volume commitments to our suppliers, which in turn affords us the opportunity to sell these circuits at the most competitive prices. Please contact us if you if you have a demand for volume state of the art memory products.

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4045 1Kx4 450	8.95	8.50	8.00	*	*
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EPROMS		1-15	16-63	64+
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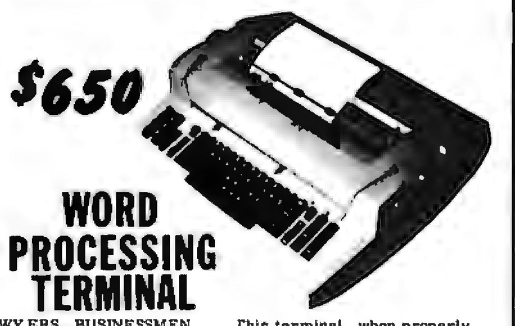
2716	16K	19.95	*	*
2532	32K	*	*	*

Attention TRS-80 Owners



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WORD PROCESSING TERMINAL

LAWYERS, BUSINESSMEN..... This terminal, when properly interfaced to your computer, allows you the flexibility of generating computerized error free correspondence. Gives your clients and business associates the impression that each letter was personally typed for the recipient. Compose your correspondence and "Fill-in" forms on your computer, edit on your screen and when your text is letter perfect instruct your computer to print an error free copy on your terminal.
The heart of this terminal is the durable IBM Selectric Typewriter. If maintenance is ever required, the World Wide network of IBM service centers is at your disposal. The terminal is functional as a regular office typewriter when not performing computer work.
Over the next several months 150 of these terminals will be removed from service, returned to the manufacturer, inspected and brought into perfect condition. Last Spring we offered for sale two-hundred Diablo printers. Within three weeks every unit was sold. Don't pass this opportunity to purchase a word processing terminal at an excellent price.
Selectric Terminal $650 (FOB Los Angeles). Shipping to the East coast aprox. $35. Combined TRS-80 interface and power supply available. Documentation will be supplied to those individuals who want to do their own custom interfacing.
Sorry, but credit cards will not be accepted on this purchase.

Thumbwheel switch

Ten position **BCD**
$1.39 ea.

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your choice **$.98**

10	50	100	1k
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Rocker JBT	DPDT
Rotary	3P-4-Pos.
Rotary	3P-6-Pos.
Push B (N.O.)	$.39ea. 4/$1

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.01 disc	.06	.05	.04

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KYNAR WIRE WRAP
50ft. $.98

500	1,000	11,000
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Battery wire wrapping tool
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Circle 39 on inquiry card.

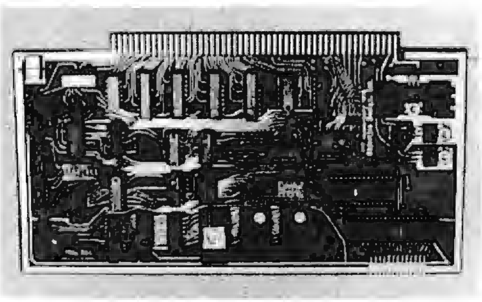
New Video Product Line from Environmental Interfaces

Environmental Interfaces' new video product line digitizes video data from standard EIA or NTSC TV cameras, deposits the data in the computer memory via the S-100 bus, and uses the digital data to reconstruct a picture on a monitor. The data is digitized into 16 gray levels with a maximum resolution of 512 pixels per line by 256 lines.

The Real Time Video Digitizer (RT) digitizes the picture in 1/60 second and deposits it in the main memory as a single operation using direct memory access. The Gray Level/Graphics Monitor Interface (MI) displays pictures in 16 gray levels or displays graphics in black and white. The MI uses block direct memory access control between computer main memory (requiring an additional interface) to develop the video signals for the monitor. In combination, the RT and MI can simultaneously deposit a picture in computer memory and display it, providing flicker-free digitized motion pictures or a frozen image. The Programmable Video Digitizer (PVD) digitizes the image in a line bypass fashion under software control. Resolution of the PVD is completely variable up to 512 pixels per line by 256 lines. If the RT or MI is used, horizontal resolution must be 64, 128, 256, or 512 pixels per line, and vertical resolution must be 64, 128, or 256 lines. Resolution is varied by DIP switches.

The RT, PVD and MI each consist of two printed circuit boards which plug into the S-100 bus, utilizing one slot for each board. A combined RT and MI is available which consists of three boards. The prices are as follows: PVD, \$495; RT, \$595; MI, \$595; and the RT and MI, \$850. For further information write to Environmental Interfaces, 23414 Greenlawn Av, Cleveland OH 44122.■

Circle 535 on inquiry card.



Call Me Tuesday at Four!

A combination of crystal derived real time clock, hardware interrupts, and programmable read only memory software come together in the Timeminder, an S-100 compatible board by Objective Design Inc, POB 20325, Tallahassee FL 32304. Timeminder software will maintain a list of user requested wake up calls and alert the indicated routines at appointed times. Intervals range from ms to days. User calls can also be based on the Timeminder time of year calendar. Wake up requests are then given as time and date. Because this is an interrupt driven device, the computer is always available for non-timed activities while waiting for the next alarm. Timed interrupts may also be applied to control of time critical hardware and software.

Timeminder software is held in on board programmable read only memory, with scratchpad programmable memory also available on the card. The interrupts and the required CALL instruction vectors are all generated on board. Additional interrupts are free for general system use.

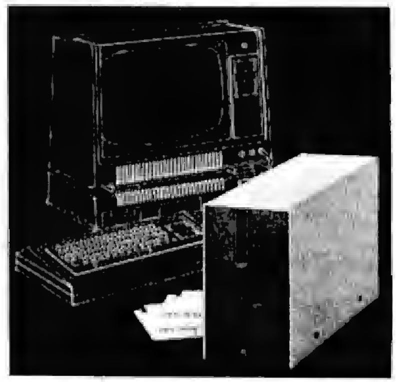
The Timeminder in kit form, which includes one programmable read only memory, is \$224.95 with shipping charges of \$5 to Canada and \$20 for other foreign countries.■

Circle 536 on inquiry card.

PerCom Manufactures Add-On Disk Drive for Radio Shack TRS-80

PerCom has recently announced an add-on 5 inch floppy disk drive for the Radio Shack TRS-80 computer. The PerCom unit, which includes the drive, drive power supply, and enclosure, is identical in all important respects to the TRS-80 Mini Disk System. The drive itself is the Shugart SA-400. The data transfer rate is 125 thousand bits per second, and access time is a fraction of a second. The drive power supply features overload current limiting and thermal protection.

Interfacing of disk drives to the TRS-80 computer is accomplished with the Radio Shack TRS-80 Expansion Interface, which accommodates up to four drives (and other peripherals), and includes controller electronics and a four drive cable. Operating software for all drives is obtained by the user with the



purchase of the first drive from Radio Shack.

The PerCom unit sells for \$399. For further information, contact PerCom Data Company Inc, 4021 Windsor, Garland TX 75042.■

Circle 537 on inquiry card.

Buffered APL/ASCII Video Terminal

Offering protected formats, video enhancements and APL overstrike and ASCII underscore, the Datamedia Elite 3045A is a microprocessor based, fully buffered, APL/ASCII video terminal. It features: character interactive, line or page mode communications; 103 and 202 modem compatibility and switch selectable EIA and optional 20 mA current loop interfaces; underscore in APL or ASCII mode; formatted data entry with protect capability; direct connect through RS-232C or 20 mA current loop or remote connection compatible with Bell 103 or 202 modems; cursor addressability and remote position sensing; ten user function keys; multiple level video display capability; no memory address space required to support screen enhancements; detached keyboard to provide expanded applications flexibility; and 15 data

transmission rates, up to 9600 bps, selectable from keyboard.

The Elite 3045A is priced at \$1995. Contact Datamedia Corp, 7300 N Crescent Blvd, Pennsauken NJ 08110.■

Circle 538 on inquiry card.

TRS-80 Owners—

Read this and save over $100.00

Introducing the Vista V80 Mini Disk System

- **23% MORE STORAGE CAPACITY** — Increases your usable storage capacity 23% from 55,000 to 67,800 bytes on drive one.
- **FASTER DRIVE** — Electronically equal to the TRS-80 Mini-Disk System, but up to 8 times faster (Track-to-track access in 5ms for the V80 versus 40ms for TRS-80).
- **DOES NOT VOID TRS-80 WARRANTY** — V80 also has 90-day warranty.
- **HERE'S WHAT YOU GET:** Minifloppy disk drive/Power Supply/Regulator board/Compact case
- **DOUBLE DENSITY FOR DOUBLE STORAGE** — The V80 will work with the Vista double-density expansion unit when available.
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Santa Ana, CA 92705
(714) 751-9201
TWX 910-595-1565

DEC LA 36 Compatible Acoustic Coupler

Designated A242A/36, this new acoustic coupler designed with TTL is made specifically for Digital Equipment Corporation's LA 36 teleprinter terminal. The A242A/36 offers full duplex 103/113 operation at up to 450 bps. The A242A/36 features positive handset lock, direct microphone handset coupling and direct connection to terminal via permanently attached J4 cable.

To increase accuracy of transmitted and received data, the unit features built-in quartz crystal controlled circuitry, double flange seals, special circuitry for reduction of sidetone effects, and special rubber feet for extra vibration isolation.

The A242A/36 is housed in a compact, lightweight case and is priced at $265. For further information contact Anderson Jacobson Inc, 521 Charcot Av, San Jose CA 95131.■

Circle 539 on inquiry card.

Turnkey Video Interface Board

The CRT-1000 is a complete 16 line by 64 character video interface. It includes a 1 K by 6 bit programmable memory, a 64 by 7 by 5 row scan character generator, and a video processor, in addition to the supplementary logic. It accepts TTL data levels in ANSI standard ASCII and provides a composite video output which can be directly connected to any standard video monitor.

Power required by the CRT-1000 is 5 V at approximately 350 mA. Video and synchronous levels (positive or negative) are switch selectable. Synchronous timing is crystal controlled; however, the dot frequency (character width) may be adjusted to accommodate different video screen widths and scan rates.

The CRT-1000 responds to a large group of cursor control commands, including: erase page and home cursor, home cursor, erase to end of line and return cursor, return cursor, cursor left, cursor right, cursor up and cursor down. An erase line function which does not affect the cursor position is provided. When the cursor reaches the bottom line of the display and a line feed code is activated, the entire display is shifted up one line. Additionally, a roll screen command is available which causes the bottom line to be replaced by what was previously at the top of the screen instead of a blank line as in line feed.

The CRT-1000 measures 3.5 by 5 inches (8.89 by 12.7 cm). The price is $119.95. For further information contact Nucleonic Products Company, POB 1454, Canoga Park CA 91304.■

Circle 540 on inquiry card.

Acoustic Coupler for Personal Computer Use

This acoustically coupled modem assembly set has been developed specifically for the personal computer market. According to the manufacturer, the modem can be assembled in less than 15 minutes with a screwdriver and a pair of pliers. No soldering is required. Since all components are tested, calibrated and burnt in, test equipment is unnecessary.

The coupler will operate in both originate and answer modes, with full and half duplex capability. An RS232C/20 mA interface is standard. No special telephone lines are required, and the device is fully compatible with telephone company 300BPS equipment (103/113 series).

The price is $169.95 and the company offers a 20 day, money back guarantee. An additional 120 day warranty on parts and labor is also provided. For further information, contact Dynamic Devices, 1087 Mississippi St, San Francisco CA 94107.■

Circle 541 on inquiry card.

LDM 404B Synchronous Limited Distance Modem

The Model LDM 404B limited distance modem is designed for full duplex synchronous communication at 4800 bps out to 50 miles. LDM 404B operates over 4 wire voice grade 3002 lines (conditioned or unconditioned), T Carrier and most other carrier systems. The transmitter uses quaternary amplitude modulation followed by frequency translation to a narrow band centered in the voice channel. The receiver uses delay equalization with digital filtering techniques. The alignment is performed with a built-in tuning meter and it has a self-checking capability. Installation requires no special tools or test equipment. The LDM 404B is available as a stand-alone unit or in a rack mounted version. For more information, contact Gandalf Data Inc, 1019 S Noel, Wheeling IL 60090.■

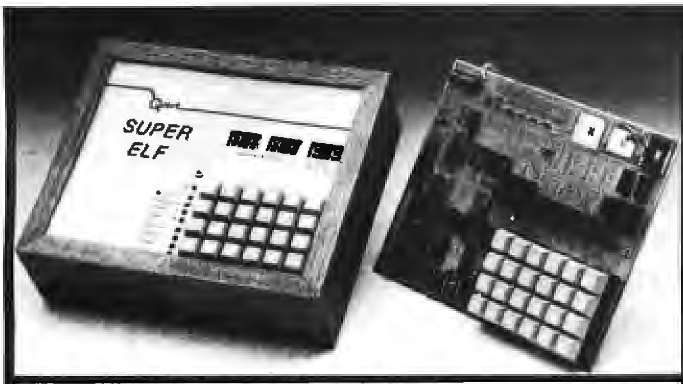
Circle 542 on inquiry card.

Light Pen for Commodore PET 2001

A self-contained light pen which plugs directly into the Commodore PET 2001 user port has been announced by the 3G Company Inc, 37a Williams Canyon Rd, Gaston OR 97119. This light pen makes it possible to bypass the PET's keyboard and interact directly with the information displayed on the video screen. The light pen adds versatility to most graphics programs. It also adds unique capabilities for application programs aimed at the noncomputer oriented person.

The light pen is complete and ready to plug into the PET. A sample program and programming instructions come with the pen. The entire package sells for $24.95.■

Circle 543 on inquiry card.



RCA Cosmac Super Elf Computer $106.95

Compare features before you decide to buy any other computer. There is no other computer on the market today that has all the desirable benefits of the Super Elf for so little money. The Super Elf is a small single board computer that does many big things. It is an excellent computer for training and for learning programming with its machine language and yet it is easily expanded with additional memory, Tiny Basic, ASCII Keyboards, video character generation, etc.

The Super Elf includes a ROM monitor for program loading, editing and execution with SINGLE STEP for program debugging which is not included in others at the same price. With SINGLE STEP you can see the microprocessor chip operating with the unique Quest address and data bus displays before, during and after executing instructions. Also, CPU mode and instruction cycle are decoded and displayed on eight LED indicator lamps.

An RCA 1861 video graphics chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a speaker system included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

A 24 key HEX keyboard includes 16 HEX keys plus load, reset, run, wait, input, memory protect, monitor select and single step. Large, on board displays provide output and optional high and low address. There is a 44 pin standard connector for PC cards and a 50 pin connector for the Quest Super Expansion Board. Power supply and sockets for all IC's are included in the price plus a detailed 127 pg. instruction manual which now includes over 40 pgs. of software info. including a series of lessons to help get you started and a music program and graphics target game.

Many schools and universities are using the Super Elf as a course of study. OEM's use it for training and research and development.

Remember, other computers only offer Super Elf features at additional cost or not at all. Compare before you buy. Super Elf Kit $106.95, High address option $8.95, Low address option $9.95. Custom Cabinet with drilled and labelled plexiglass front panel $24.95. NiCad Battery Memory Saver Kit $6.95. All kits and options also come completely assembled and tested.

Questdata, a 12 page monthly software publication for 1802 computer users is available by subscription for $12.00 per year.

Tiny Basic for ANY 1802 System

Cassette $10.00. On ROM $38.00. Super Elf owners, 30% off. Object code listing with manual $5.00. Object list, manual and paper tape $10.00. Original ELF Kit Board $14.95.

Super Expansion Board with Cassette Interface $89.95

This is truly an astounding value! This board has been designed to allow you to decide how you want it optioned. The Super Expansion Board comes with 4K of low power RAM fully addressable anywhere in 64K with built-in memory protect and a cassette interface. Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the Super Elf. The board includes slots for up to 6K of EPROM (2708, 2758, 2716 or TI 2716) and is fully socketed. EPROM can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/editor and error checking multi file cassette read/write software, (relocatible cassette file) another exclusive from Quest. It includes register save and readout, block move capability and video graphics driver with blinking cursor. Break points can be used with the register save feature to isolate program bugs quickly, then follow with single step. The Super Monitor is written with subroutines allowing users to take advantage of monitor functions simply by calling them up.

Improvements and revisions are easily done with the monitor. If you have the Super Expansion Board and Super Monitor the monitor is up and running at the push of a button.

Other on board options include Parallel Input and Output Ports with full handshake. They allow easy connection of an ASCII keyboard to the input port. RS 232 and 20 ma Current Loop for teletype or other device are on board and if you need more memory there are two S-100 slots for static RAM or video boards. A Godbout 8K RAM board is available for $135.00. Also a 1K Super Monitor version 2 with video driver for full capability display with Tiny Basic and a video interface board. Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50. A 50 pin connector set with ribbon cable is available at $12.50 for easy connection between the Super Elf and the Super Expansion Board.

The Power Supply Kit for the Super Expansion Board is a 5 amp supply with multiple positive and negative voltages $29.95. Add $4.00 for shipping. Prepunched frame $5.00. Case $10.00. Add $1.50 for shipping.

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7402N 17
7404N 19
7409N 23
7410N 17
7414N 63
7420N 17
7422N 1 39
7430N 20
7442N 50
7445N .69
7447N 60
7448N 89
7450N 17
7474N 29
7475N 49
7485N 88
7489N 2 00
7490N 43
7492N 43
7493N 43
7495N 69
74100N 90
74107N 29
74121N 34
74123N .59
74125N 39
74145N 69
74150N 85
74151N 69
74154N 1 00
74157N 69
74161N 87
74162N 87
74163N 87
74174N 86
74175N 90
74190N 1 15
74192N 87
74193N 85
74221N 1 55
74298N 1 65
74365N 66
74366N 66
74367N 66

74LS00 TTL
74LS00N 25
74LS02N 25
74LS04N 25
74LS05N 25
74LS08N 25
74LS10N 25
74LS13N 40
74LS14N 90
74LS20N 25
74LS22N 25
74LS28N 41
74LS30N 25
74LS33N 39
74LS38N 30
74LS74N 70
74LS75N 47
74LS90N 51
74LS93N 51
74LS95N 1 89
74LS107N 35
74LS112N 35
74LS113N 35
74LS132N 72
74LS136N 35
74LS151N 67
74LS155N 67
74LS157N 67
74LS162N 91
74LS163N 91
74LS174N 95
74LS190N 1 05
74LS221N 1 95
74LS258N 67
74LS367N 1 35

LINEAR
CA3045 90
CA3046 67
CA3081 1 80
CA3082 1 90
CA3089 2 95
LM301AN/AH 35
LM305H 87
LM307N 35
LM308N 89
LM309H 1 15
LM309K 1 50
LM311H/N 90
LM317T K 2 02
LM318 1 35
LM320K-5 1.20
LM323K-5 6 95
LM320K-12 1 35
LM320K-15 1 35
LM320T-5 1 60
LM320T-8 1 60
LM320T-12 1 50
LM320T-15 1 60
LM324N 1 15
LM339N 1 55
LM340K-5 1 35
LM340K-8 1 35
LM340K-12 1 35
LM340K-15 1 35
LM340K-24 1 35
LM340T-5 1 25
LM340T-8 1 25
LM340T-12 1 25
LM340T-15 1 25
LM340T-18 1 25
LM340T-24 1 25
LM343H 4 50
LM350 7 50
LM370 1 15
LM377 3 00
LM379 5.00
LM380N 1.00
LM381 1.60
LM382 1 60
LM703H 40
LM709H 28
LM723H/N 50
LM733N 67
LM741CH 35
LM741N 28
LM747H/N 62
LM748N 35
LM1303N 82
LM1304 1 10
LM1305 1 27
LM1307 2 00
LM1310 2 75
LM1458 47
LM1800 1.75
LM1812 7 50
LM1889 3 00
LM2111 1 75
LM2902 1 50
LM3900N 60
LM3905 1 75
LM3909N .61
MC1458V .50
NE540L 2 89
NE550N 65
NE555V 43
NE556A 79
NE565A 1 00
NE566V 1 50
NE567V 1 20
NE570B 5.00
NE571B 5.00
78L05 60
78L08 60
79L05 70
78M05 85
75108 1 75
75491CN 50
75492CN 55
75494CN 89

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9400CJV/F 7 40
ICL7103 9.50
ICL7107 14 25

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CD4000 18
CD4001 21
CD4002 .21
CD4006 1 10
CD4007 21
CD4008 21
CD4009 .39
CD4010 39
CD4011 21
CD4012 21
CD4013 38
CD4014 88
CD4015 .86
CD4016 38
CD4017 .94
CD4018 .94
CD4019 21
CD4020 1 02
CD4021 1 02
CD4022 86
CD4023 21
CD4024 75
CD4025 21
CD4026 1 51
CD4027 38
CD4028 79
CD4029 1 02
CD4030 21
CD4035 1.02
CD4040 1 02
CD4042 71
CD4043 63
CD4044 63
CD4046 1 67
CD4049 38
CD4050 38
CD4051 1 13
CD4060 1 42
CD4066 .71
CD4068 .40
CD4069 .40
CD4070 .40
CD4071 .21
CD4072 21
CD4073 21
CD4075 21
CD4076 1 75
CD4078 40
CD4081 .21
CD4082 21
CD4116 .47
CD4490 5 50
CD4507 1.00
CD4508 4.25
CD4510 1.02
CD4511 .94
CD4515 2.52
CD4516 1 10
CD4518 1.02
CD4520 1 02
CD4527 1 51
CD4528 .79
CD4553 3.50
CD4566 2 25
CD4583 4.50
CD4585 1 10
CD40192 3.00
74C00 28
74C04 33
74C10 28
74C14 2 10
74C20 28
74C30 28
74C48 1 95
74C74 75
74C76 1 40
74C90 1 15
74C93 1 40
74C154 3 00
74C160 1 44
74C175 1 35
74C192 1 65
74C221 2 00
74C905 3.00
74C908 75
74C914 1 95
74C922 5 50
74C923 5 50
74C925 6.95
74C926 6.95
74C927 6 95

INTERFACE
8095 65
8096 .65
8097 65
8098 65
8T09 1.25
8T10 4 50
8T13 3 00
8T20 5 50
8T23 3 10
8T24 3 50
8T25 3 20
8T26 1 69
8T28 2 75
8T97 1 80
8T98 1 69

MOS/MEMORY RAM
2101-1 3 95
2102-1 95
2102AL 4 1 60
21L02 1 1 10
21F02 1 25
2104A 4 4 95
2107B 4 95
2111-1 3 75
2112-2 3 95
2114L 3 7 90
4116 10 95
2513B 6 30
MM5262 40
MM5280 3 00
MM5320 9 95
MM5330 5 94
PD411D-3 4 00
PD411D-4 5 00
P5101L 13 95
4200A 9 95
82S25 2 90
91L02A 1 50
HD0165-5 6 95
MM57100 4 50
GIAY38500-1 9 95
MCM6571A 9 95
9368 3 50
4100 10 00
416 16 00

CLOCKS
MM5309 3 00
MM5311 3.60
MM5312 4 80
MM5313 3 60
MM5314 3 90
MM5315 4.00
MM5316 5 00
MM5318 3 60
MM5369 2 10
MM5841 14 45
MM5865 7 95
CT7001 5 80
CT7002 8 95
CT7010 8 95
CT7015 7 75
MM5375AA/N 3 90
MM5375AB/N 4 90
7205 10 50
7207 7 50
7208 15.95
7209 4 95
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DS0056CN 3 75
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MICROPROCESSOR
6800 17 50
6802 24 95
8080A with data 8 95
8085 27 00
Z80A 19 75
8212 2 90
8214 8 00
8216 2 90
8224 2 90
8228 5 35
8251 8 50
8253 10 00
8255 9 25
8257 19 50
8259 19 50
1802CP plus 13 95
1802DP plus 17 95
1861P 11 50
CDP1802CD 19 95
CDP18020 25 00
CDP1861 12 95
6820 9 95
6850 12 95
6502 12 50

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Solder Tin Low Profile PIN	1 UP	PIN	1 UP
8	15	22	30
14	16	24	35
16	20	28	42
18	27	36	58
20	29	40	57

3 level wire wrap gold 14 pin 25
2 level 14 pin ww 20

WIRE WRAP LEVEL 3

PIN		PIN	
14	25	24	86
16	33	28	1 00
18	57	40	1 23

UART/FIFO
AY5-1013 5 50
AY5-1014 7 50
3341 6 95

PROM
1702A 3 95
N82S23 2 95
N82S123 3 50
N82S126 3 75
N82S129 3 75
N82S131 3 75
N82S136 8 75
N82S137 8 75
2708 10 50
DM8577 2 90
8223 2 90
2716T1 29 50
2716 Intel 48 00

CRYSTALS
1 MHz 4 50
2 MHz 4 50
4 MHz 4 25
5 MHz 4 25
10 MHz 4 25
18 MHz 3 90
20 MHz 3 50
32 MHz 3 90
32768 MHz 4 00
1 8432 MHz 4.50
3 5795 MHz 1 20
2 0100 MHz 1 85
2 097152 MHz 4 50
2 4576 MHz 4 50
3 2768 MHz 4 50
5 0688 MHz 4 50
5 185 MHz 4 50
5 7143 MHz 4 50
6 5536 MHz 4 50
14.31818 MHz 4 25
18 432 MHz 4 50
22 1184 MHz 4 50

CONNECTORS
44 pin edge 2 75
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AY5-2376 $12 50
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	1	10
Red	.55	47
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Keyer 8043 14 50 comp w-spec clock

TRANSISTORS
2N1893 40
2N2222A 18
2N2369 30
2N2904A 20
2N2907A 25
2N3053 40
2N3638 25
2N3643 25
2N3904 18
2N3906 18
2N3055 69
2N4400 25
2N4401 75
2N4402 20
TIP31 60
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DL747/750 CA CC 600 1 95
DL750 CC 600 1 95
FND359 CC 357 70
FND500/507 CC/CA 500 1.35
FND503/510 CC/CA 500 90
FND800/807 CC/CA 800 2 20
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7520 Clairex photocells 39
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5500		25V	2 50
5800		40V	3 00
6100		40V	3 00
6100		50V	3 00
7700		50V	2 50
8000		55V	2 50
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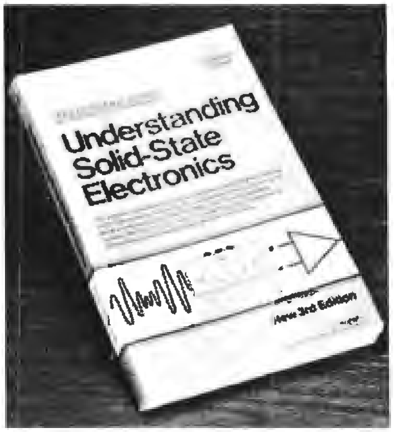
TI Publishes Third Edition of Understanding Solid-State Electronics

A new and updated edition of *Understanding Solid-State Electronics*, 270 pages, is available from the Texas Instruments Learning Center Library, POB 3640, MS 84, Dallas TX 75285. The softback is priced at $3.95.

This third edition covers today's semiconductor technologies and products and reviews earlier electronic devices and integrated circuits to provide the reader with a basic understanding of solid-state electronics. Written in nontechnical language, *Understanding Solid-State Electronics* is a self-teaching textbook complete with quizzes and glossaries.

New additions include comprehensive discussions on MOS (metallic oxide semiconductors) and LSI (large scale integrated circuits); how an MOS transistor works, how it compares to a bipolar transistor and how MOS transistors have made microprocessors and microcomputers possible. New details are also provided on linear integrated circuits; the techniques used to fabricate them and how they are used.



The book explains how diodes, transistors, thyristors and integrated circuits are made; how they work; and how they are used in systems. Other topics covered are: what electricity does in systems; how circuits make decisions; and how semiconductors relate to systems.■

Circle 526 on inquiry card.

Directory of PET Related Products

A comprehensive hardware and software reference service for users of the Commodore PET computer has been announced by Channel Data Systems, 5960 Mandarin Av, Goleta CA 93017. The *Channel Data Book* is a user oriented directory of PET related products including: software, hardware and peripherals, literature and periodicals of special interest to PET users, listings of user groups and distributors, and cross references by product type and supplier. The *Channel Data Book* provides dividers and color coding to organize programs, articles, and newsletters of specific interest to each user.

The book includes a 3 ring binder and updated supplements with instructions for filing new and revised material. The *Channel Data Book* is priced at $19.95, which includes an update service through calendar year 1979.■

Circle 529 on inquiry card.

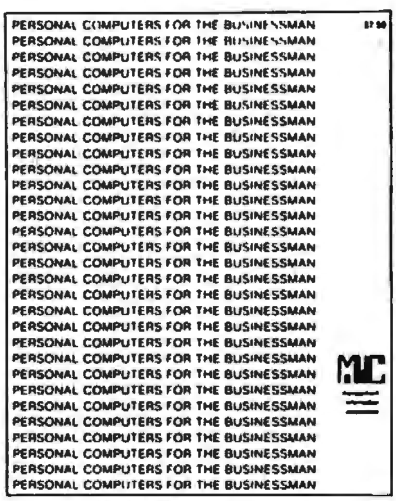
1978/1979 Catalog from Cramer Electronics

This comprehensive catalog from Cramer Electronics lists the components, systems, peripherals, instruments and tools that are available at local Cramer stocking centers. Listed in the *1978-79 Cramer Buyer's Guide* are products made by such companies as Allen-Bradley, Amphenol, Bournes, Erie, Fairchild, General Electric, ITT Cannon, Mostek, Motorola, RCA, Sprague, Texas Instruments and about 80 more manufacturers. Cramer offers components in over 50 product categories covering all active and passive areas plus a wide range of accessories. For a copy of this catalog, write to Cramer Electronics, 85 Wells Av, Newton MA 02159.■

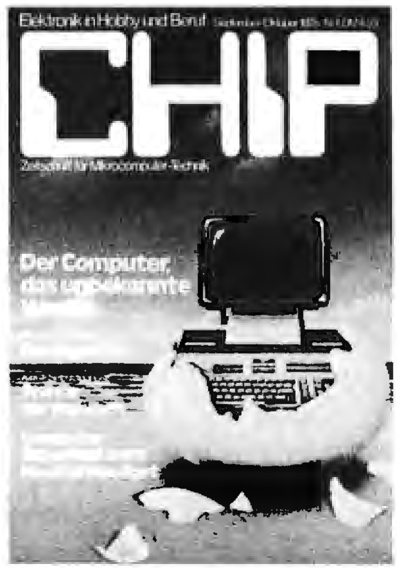
Circle 527 on inquiry card.

How to Find the Personal Computer You Want

A 24 page publication entitled *Personal Computers for the Businessman* explains what a personal computer is and how it differs from a minicomputer. It also describes a shopping strategy to follow when the decision is made to purchase a system. A major part of the report is an overview of the best known manufacturers currently in the personal computer market. The configuration of each system is given as well as the price range. There is also a list of manufacturers and suppliers in the back of the publication. The purchase price of the report is $7.50. For further information contact Management Information Corp, 140 Barclay Ctr, Cherry Hill NJ 08034.■



Circle 528 on inquiry card.



New Microcomputer Magazine from Germany

Chip is a new German language magazine for microcomputer users interested in computer construction, programming and application. Published every other month, this appealing publication has at least 65 pages of editorial material dealing with software and hardware, ready-for-use devices, instructions for circuit construction, programming, and stories in words and pictures. Every issue is complete with book reviews, training methods and instructions, and a forum for exchanging experiences and opinions. The cost for six issues of *Chip* is DM 24.00. For more information, write to Vogel-Verlag, Max-Planck-Str, 7/9, Postfach 6740, D-8700 Wurzburg 1, GERMANY.■

Circle 530 on inquiry card.

SAL-11 Structured Assembly Language

The SAL-11 Structured Assembly Language software is a MACRO-11 preprocessor which operates on DEC LSI-11s and PDP-11s under RT-11. SAL-11 is a midlevel language suitable for systems and applications programming which requires the advantages of assembly language.

SAL-11 facilitates the use of structured programming techniques; provides a standard interface between FORTRAN and MACRO-11 modules; provides string handling capabilities; handles recursive and reentrant modules; and provides commands for stack manipulation, register saving and restoring, and for passing parameters and control between modules.

The structured programming facilities provided by SAL-11 include the classic control structures for conditional execution, iterative execution, case statements, program block definition and environment setup.

Included in the $515 binary license fee is a copy of the user's guide and 1 year warranty which includes technical assistance and maintenance support. For more information contact GEJAC Inc, 3322 Stanford St, Hyattsville MD 20783.■

Circle 546 on inquiry card.

Play 4 Person Contract Bridge Against the Computer

Bridge Challenger, for 8 K byte PETs, 16 K byte Level II TRS-80s and 16 K byte Apples, lets you and the dummy play 4 person contract bridge against the computer. The program will deal hands at random or according to your criteria for high card points, and you can save hands on cassette and reload them for later play. You can review tricks, rotate hands east-west, shuffle only the defense hands, or replay hands when the cards are known. Bridge Challenger is priced at $14.95 and is available from Personal Software, POB 136, Cambridge MA 02138.■

Circle 548 on inquiry card.

Structured Programming for the TRS-80

SLIC (structured language for interactive computation) is a high level language interpreter offered by RTG Data Systems, 309 Santa Monica Blvd, Suite 312, Santa Monica CA 90401. SLIC features a complete set of control statements for structured programming; modular programming using functions with arguments; dynamic variable allocation for efficient memory usage; device independent input and output (IO) using unit numbers (byte, record and variable IO are all provided); programs that can read and write cassette data files; character, integer and real variables; one- and two-dimensional arrays; keyword compression; 28 built-in functions; cassette motor control and many more features.

Sample SLIC program listings are included. SLIC is available on TRS-80 cassette and requires a 16 K Level I machine. The price is $50 and the user's manual may be ordered separately for $10.■

Circle 549 on inquiry card.

Game Series Available for Apple II

The Intelligent Game Series #1 is available for the Apple II computer. The three software packages include: Battleship and 3-dimensional Tic Tac Toe; Hangman and Concentration; and Casino Royale (includes 1 arm bandit, crap game, blackjack and roulette). All three packages feature Apple II low and high resolution graphics with instructions included. Each program package costs $12 and individual program listings can be obtained for $3 per program. For more information contact Stuart Frager, POB 13331, Baltimore MD 21203.■

Circle 547 on inquiry card.

Zilog BASIC Interpreter Supports Z-80 Based Microcomputers

Zilog's extended BASIC interpreter supports the firm's MCZ series of microcomputers introduced to date (the MCZ-1/05, MCZ-1/60 and MCZ-1/90) and its new line of development systems (the 4 MHz ZDS-1/40 and 2.5 MHz ZDS-1/25).

Programs can be interactively entered, edited, run and debugged completely within the BASIC interpreter subsystem. Zilog's BASIC allows the user to manipulate real, integer and string data with full file capabilities, including both string and record random access. BASIC includes two mathematics packages: a binary package with seven significant digits, and a binary coded decimal data version with 13 significant digits.

The interpreter interfaces with the RIO operating system of Zilog's microcomputers, which use the Z-80 processor. Programs can be interfaced with PLZ or assembly language procedures and can be chained to other BASIC programs.

For more information contact Zilog, 10460 Bubb Rd, Cupertino CA 95014.■

Circle 550 on inquiry card.

Compiler for 6500 Microcomputer Family

A systems implementation language called CSL/65 has been developed by Computer Applications Corporation (COMPAS) for the 6500 microcomputer family offered by Rockwell, Synertek and MOS Technology. The language resembles PL/1 and ALGOL in general form, but has been specifically designed for microcomputer users. Versions are currently available for the Rockwell System 65 development system and any PDP-11 using the RT-11 operating system.

CSL/65 is a midlevel language designed to combine the power and flexibility of assembler language with the structuring potential of a high level language. All language features are aimed at improving the productivity of the systems programmer by simplifying the development of programs normally written in assembler. CSL/65 produces assembler code rather than object code. This allows the programmer to enhance or optimize at the assembler level if necessary as well as enabling the programmer to drop into assembler whenever necessary. CSL/65 output is then passed to the assembler, which is part of the System 65 monitor, or to the MINmic assembler, which is available from COMPAS for the PDP-11.

The price for either the System 65 or PDP-11 versions of CSL/65 is $1000. The MINmic 1165 assembler (required for PDP-11 users) is $900. For further information contact Computer Applications Corp, 413 Kellog, Ames IA 50010.■

Circle 551 on inquiry card.

BASIC for Fairchild F8 Features Floating Point

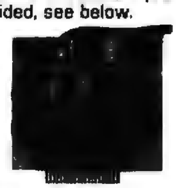
Micro Business Systems Inc has announced a full BASIC interpreter for use with Fairchild's F8 processor. Called MBS-BASIC, the new product features 9 digit precision and floating point arithmetic.

Including all standard arithmetic operations and relations, MBS-BASIC is competitive in speed and efficiency with the 8080 and Z-80 BASIC interpreters. MBS-BASIC version 1.0 has a license fee of $179.95. The MBS-BASIC interpreter is distributed on ASR33 compatible paper tape and is provided with documentation. Contact Micro Business Systems Inc, POB 8255, JFK Sta, Boston MA 02114.■

Circle 552 on inquiry card.

TRS-80 E.S. SERIAL I/O

• Can input into basic • Can use LLIST and LPRINT to output, or output continuously • RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line • Requires +5, -12 VDC • Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010 C. No connectors provided, see below.

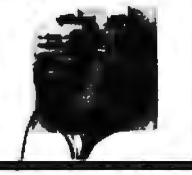


EIA/RS-232 connector Part No DB25P $6.00, with 8', 8 conductor cable $10.95 Part No DB25P8.

3' ribbon cable with attached connectors to fit TRS-80 and our serial board $19.95 Part No 3CAB40.

MODEM ✲

• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output-serial • Connect 8 Ω speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board only $7.60 Part No. 109, with parts $27.50 Part No. 109A



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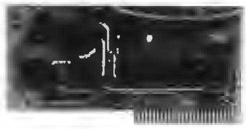
APPLE II ✲ SERIAL I/O INTERFACE



Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

8K EPROM PIICEON

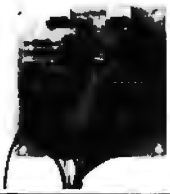
Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers. • S-100 bus compatible • Room for 8K bytes of EPROM non-volatile memory (2708's). • Onboard PROM programming • Address relocation of each 4K of memory to any 4K boundary within 64K • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software available • Solder mask both sides • Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.

T.V. TYPEWRITER

• Stand alone TVT • 32 char/line, 16 lines, modifications for 64 char/line included • Parallel ASCII (TTL) input • Video output • 1K on board memory • Output for computer controlled curser • Auto scroll • Non-destructive curser • Curser inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, and -12 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper case only • Board only $39.00 Part No. 106, with parts $145.00 Part No. 106A

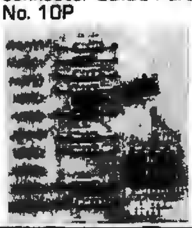
TAPE ✲ INTERFACE

• Play and record Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board only $7.60 Part No. 111, with parts $27.50 Part No. 111A



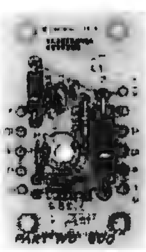
RS-232/TTL ✲ INTERFACE

• Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires -12 and +12 volts • All connections go to a 10 pin gold plated edge connector • Board only $4.50 Part No. 232, with parts $7.00 Part No. 232A 10 Pin edge connector $3.00 Part No. 10P



RS-232/TTY ✲ INTERFACE

• Converts RS-232 to 20mA current loop, and 20mA current loop to RS-232 • Two separate circuits • Requires +12 and -12 volts • Board only $4.50 Part No. 600, with parts $7.00 Part No. 600A

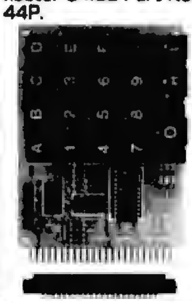


UART & BAUD RATE GENERATOR ✲

• Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. • All connections go to a 44 pin gold plated edge connector • Board only $12.00 Part No. 101, with parts $35.00 Part No. 101A, 44 pin edge connector $4.00 Part No. 44P

HEX ENCODED KEYBOARD E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX-3A. 44 pin edge connector $4.00 Part No. 44P.



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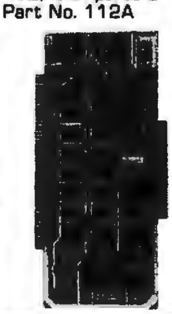
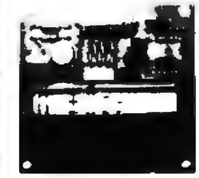


T.V. INTERFACE

• Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple • Power required is 12 volts AC C.T., or +5 volts DC • Board only $7.60 part No. 107, with parts $13.50 Part No. 107A



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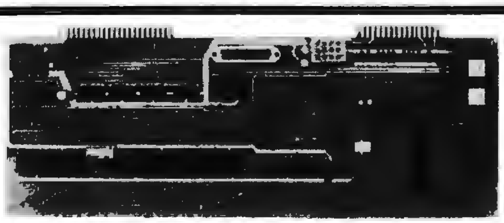

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This bidirectional board is a direct replacement for the board inside the Trendata 1000 terminal. The on board connector provides RS-232 serial in and out. Sold only as an assembled and tested unit for $330.00. Part No. TA 1000C

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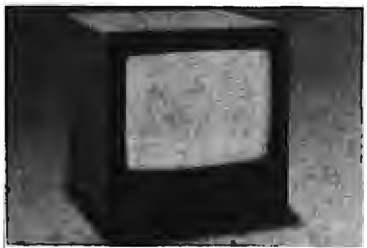

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- Cabinets • XFMRS • Heat Sinks • Printers • Components

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Circle 391 on inquiry card.

HICKOK LX303 $74.95

HICKOK LX303

74^{95}*

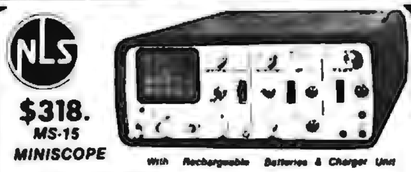
• 5%, 3½ digit 19 Range DVM. ½" LCD displays runs 200 hrs on 1 battery. 10 Meg Ohm input. 1 yr. guarantee, made in U.S.A., test leads included.

Available Accessories

RC-3 115V AC Adapter	$7.50
CC-3 Deluxe Padded Vinyl Carrying Case	$7.50
VP-10 X10 DCV Probe Adapter/ Protector 10Kv	$14.95
VP-40 40Kv DC Probe	$35.00
CS-1 10 Amp Current Shunt	$14.95

***FREE**

Just for Asking.
FREE BATTERY with your meter.



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MS-15
MINISCOPE

With Rechargeable Batteries & Charger Unit

- 15 megahertz bandwidth.
- External and internal trigger.
- Time base — 1 microsec. to 0.5 Sec/div - 21 settings ±3%
- Battery or line operation
- Automatic & line sync modes
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• MS-215 Dual Trace Version of MS-15 **$435.**

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Controlled Soldering Station

THREAD-TOGETHER MODULAR DESIGN FOR QUICK, ON-LINE HEATER OR TIP CHANGE

- Available in 3 preset temperatures, 600°F, 700°F or 800°F for any application
- Closed loop, non-magnetic control
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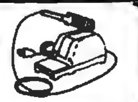
- Designed for use on sensitive components



COMPLETE STATION AND REPLACEABLE HEATER SELECTION GUIDE

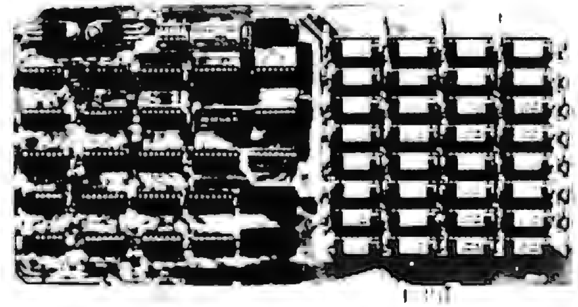
Temperature	Complete Station	Controlled Heater No
600°F	50T6	#76
700°F	50T7	#77
800°F	50T8	#78

Controlled Heaters: $14.95 Each. Tips: $2.25 Each. Adapter: $1.30 Each

List $59.50 OUR PRICE $52.50

SD EXPANDORAM

The Ultimate S-100 Memory



The EXPANDORAM is available in versions from 16K up to 64K, so for a minimum investment you can have a memory system that will grow with your needs. This is a dynamic memory with the invisable on-board refresh, and IT WORKS!

- Bank Selectable
- Phantom
- Power 8VDC, ±16VDC, 5 Watts
- Lowest Cost Per Bit
- Uses Popular 4116 RAMS
- PC Board is doubled solder masked and has silk-screen parts layout.
- Extensive documentation clearly written
- Complete Kit includes all Sockets for 64K
- Memory access time: 375ns, Cycle time: 500ns.
- No wait states required.
- 16K boundries and Protection via Dip Switches
- Designed to work with Z-80, 8080, 8085 CPU's.

EXPANDO 64 KIT (4116)

16K	$245.00
32K	$310.00
48K	$375.00
64K	$440.00

Vector

8803 MOTHER BOARD FOR S100 BUS MICRO-COMPUTERS

Price: $29.50

Vector Plugboards

8800V

Universal Microcomputer/processor plugboard use with S 100 bus. Complete with heat sink & hardware 5.3 x 10 x 1/16

1-4	5-9	10-24
$19.95	$17.95	$15.96

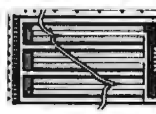
8801-1

Same as 8800V except plain less power buses & heat sink

1-4	5-9	10-24
$14.95	$13.46	$11.96

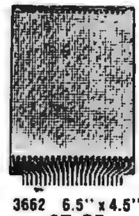
3682 9.6" x 4.5" $10.97
3682-2 6.5" x 4.5" $9.81

Hi-Density Dual-In-Line Plugboard for Wire Wrap with Power & Grd Bus Epoxy Glass 1/16" 44 pin con. spaced .156



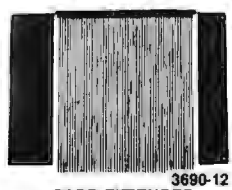
3677 9.6" x 4.5" **$10.90**
3677-2 6.5" x 4.5" **$9.74**

Gen. Purpose D.I.P. Boards with Bus Pattern for Solder or Wire Wrap. Epoxy Glass 1/16" 44 pin con spaced .156



3662 6.5" x 4.5" **$7.65**
3662-2 9.6" x 4.5" **$11.45**

P pattern plugboards for IC's Epoxy Glass 1/16" 44 pin con spaced .156



3690-12
CARD EXTENDER
Card Extender has 100 contacts 50 per side on .125 centers-Attached connector-is compatible with S-100 Bus Systems. $25.83
3690 6.5" 22/44 pin .156 ctrs. Extenders $13.17

1/16 Vector BOARD

.042 dia holes on 0.1 spacing for IC's

Phenolic PART NO.	SIZE	PRICE 1-9	10-19
64P44XXXP	4.5x6.5"	$1.56	$1.40
169P44XXXP	4.5x17"	$3.69	$3.32
Epoxy Glass			
64P44	4.5x6.5"	$1.79	$1.61
84P44	4.5x8.5"	$2.21	$1.99
169P44	4.5x17"	$4.52	$4.07
169P84	8.5x17"	$8.03	$7.23

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MEMORY EXPANSION KITS
4116's RAMS
(16Kx1 200ns)

8 for $69.00

2708

8K 450 ns
EPROM
FACTORY PRIME
$12.00 EA.
25 + Call For Price

WOW 14 & 16 PIN GOLD 3 LEVEL WIRE WRAP SOCKETS

14 - G3 100 for $30.00
16-G3 100 for $30.00
50 of each for $32.00

Sockets are End & Side stackable, closed entry

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$56.95 with tube

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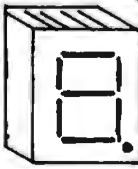
Common Cathode
FND 510
Common Anode
½" 7 seg LED
59¢
10/4^{50}



Vector

WRAP POST for .042 dia. holes (all boards on this page)

T44/C pkg 100	$2.34
T44/M pkg 1000	$14.35
A-13 hand installing tool	$2.94

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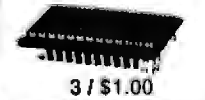
24 PIN DIP PLUGS WITH COVERS



3 / $1.00
40 / $10.00

HICKOK LX303 $74.95

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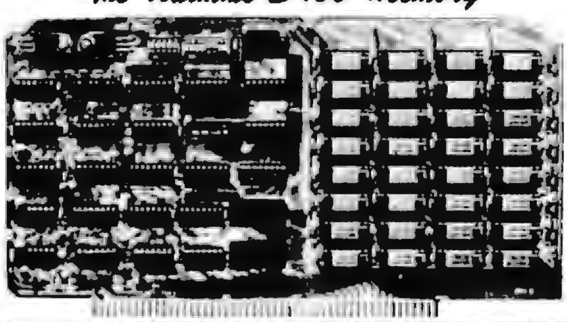
The Ultimate S-100 Memory



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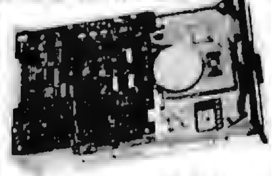
EXPANDO 64 KIT (4116)

16K	$245.00
32K	$310.00
48K	$375.00
64K	$440.00

DISC DRIVES



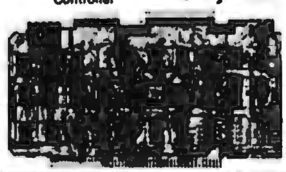
Sugart SA400 5¼"
$295.00

GSI/Siemens *FDD100-8 8"
$395.00
*equivalent to Sugart 801

Siemens FDD 200-8 8" double-sided double density
$599.00

DISC CONTROLLER
SD "VERSAFLOPPY" Kit

The Versatile Floppy Disk Controller — **Only $159.00**



FEATURES IBM 3740 Soft Sectored Compatible. S-100 BUS Compatible for Z-80 or 8080 Controls up to 4 Drives (single or double sided) Directly controls the following drives
1. Shugart SA400/450 Mini Floppy
2. Shugart SA800/850 Standard Floppy
3. PERSCI 70 and 277
4. MFE 700/750
5. CDC 9404/9406
6. GSI/Siemans FDD100-8

34 Pin Connector for Mini Floppy 50 Pin Connector for Standard Floppy Operates with modified CP/M operating system and C-Basic Compiler The new "Versafloppy" from S D Computer Products provides complete control for many of the available Floppy Disk Drives, Both Mini and Full Size FD1771B-1 Single Density Controller Chip Listings for Control Software are included in price

CONTINENTAL SPECIALTIES CORPORATION

100MHz 8-Digit Counter

- 20 Hz-100 MHz Range
- 6" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable - completely self-contained
- Size - 1.75" x 7.38" x 5.63"
- Four power sources, i.e. batteries, 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply.

~~$134.95~~ **Sale $120.00**

ACCESSORIES FOR MAX 100:
Mobile Charter Eliminater use power from car battery. Model 100—CLA $3.95
Charger/Eliminator use 110 VAC Model 100 — CAI $9.95

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SALE

LOGIC MONITOR 1

Trace signals through all types of digital circuits. Unit clips over any DIP IC up to 16 pins. Each of its 16 contacts connects to a single-bit level detector that drives a high-intensity, numbered LED readout activated when the applied voltage exceeds a fixed 2 V threshold. Logic "1" turns LED on; logic "0" keeps LED off. A power-seeking gate network automatically locates supply leads and feeds them to the LM-1's internal circuitry. Saves minutes, even hours in design, troubleshooting, debugging of equipment. **Voltage Threshold:** 2 V ± 0.2 V. **Input Impedance:** 100,000 ohms. **Input Voltage Range:** 4-15 V max. across any two or more inputs. **Current Drain:** 200 mA at 10 V. *Size:* 4" l. x 2" w. x 1.75" d. when open. *Weight:* 3 ozs.

CSC Model LM-1 Logic Monitor—Complete.
List Price $54.95

CONTINENTAL SPECIALTIES CORPORATION

Logic Probes and Digital Pulsers

SALE

SALE

LOGIC PROBES

CSC logic probes are the ultimate tool for breadboard design and testing These hand-held units provide an instant overview of circuit conditions Simple to use, just clip power leads to circuit's power supply, set logic family switch to TTL/DTL or CMOS/HTL. Touch probe to test node Trace logic levels and pulses through digital circuits. Even stretch and latch for easy pulse detection Instant recognition of high, low or invalid levels, open circuits and nodes. Simple, dual-level detector LEDs tell it quickly, correctly. HI (Logic "1"); LO (Logic "0") Also incorporates blinking pulse detector e g , HI and LO LEDs blink on or off, tracking "1" or "0" states at square wave frequencies up to 1.5 MHz. Pulse LED blinks on for ½ second during pulse transition. Choice of three models to meet individual requirements; budget, project and speed of logic circuits.

MODEL LP-1
Hand-held logic probe provides instant reading of logic levels for TTL, DTL, HTL or CMOS **Input Impedance:** 100,000 ohms. **Minimum Detectable Pulse:** 50 ns **Maximum Input Signal (Frequency):** 10 MHz. **Pulse Detector (LED):** High speed train or single event **Pulse Memory:** Pulse or level transition detected and stored

CSC Model LP-1 Logic Probe—Net Each ...... ~~$44.95~~ **$42.70**

MODEL LP-2
Economy version of Model LP-1 Safer than a voltmeter More accurate than a scope. **Input Impedance:** 300,000 ohms **Minimum Detectable Pulse:** 300 ns. **Maximum Input Signal (Frequency):** 1.5 MHz **Pulse Detector (LED):** High speed train or single event **Pulse Memory:** None

CSC Model LP-2 Logic Probe—Net Each ~~$24.95~~ **$23.70**

MODEL LP-3
High speed logic probe Captures pulses as short as 10 ns Input Impedance: 500,000 ohms **Minimum Detectable Pulse:** 10 ns **Maximum Input Signal (Frequency):** 50 MHz **Pulse Detector (LED):** High speed train or single event **Pulse Memory:** Pulse or level transition detected and stored

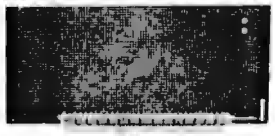
CSC Model LP-3 Logic Probe—Net Each ~~$69.95~~ **$66.45**

DIGITAL PULSER
The ultimate in speed and ease of operation. Simply connect clip leads to positive and negative power, then touch DP-1's probe to a circuit node, automatic polarity sensor detects circuit's high or low condition Depress the pushbutton and trigger an opposite polarity pulse into the circuit Fast troubleshooting includes injecting signals at key points in TTL, DTL, CMOS or other popular circuits Test with single pulse or 100 pulses per second via built-in dual control push-button, button selects single shot or continuous modes. LED indicator monitors operating modes by flashing once for single pulse or continuously for a pulse train Completely automatic, pencil-size tab/field pulse generator for any family of digital circuits. **Output:** Tri-state **Polarity:** Pulse-sensing auto-polarity **Sync and Source:** 100 mA **Pulse Train:** 100 pps **LED Indicator:** Flashes for single pulse, stays lit for pulse train

CSC Model DP-1 Digital Pulser—Net Each ~~$74.95~~ **$71.20**

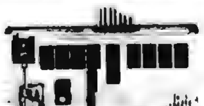
4607
DEC LSI-11, PDP8, PDP11, Heath H-11, P Pattern Epoxy Glass, Plug Board 8 43"x5 187", Dual 36 pin DEC/HEATH Connectors

1-4	5-9	10-24
10.95	17.96	15.96



8801-1
Plain no etched circuitry except contacts Produces maximum flexibility.

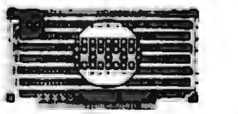
1-4	5-9	10-24
14.95	13.46	11.96



8802-1
Pad per 2 holes Two-holE pads allow tack soldering of socket, plus second hole for component leads

1-4	5-9	10-24
21.95	19.76	17.56

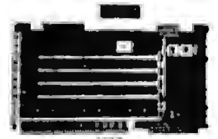
Vector



8804
"ANY DIP" has full power and ground planes back to back. Board accommodates 3, 4, 6, 9" Dips

1-4	5-9	10-24
21.95	19.76	17.56

Vector



4608
is form and size compatible with INTEL SBL80 Series and NATIONAL BLC 80 Series microcomputer boards. Power and Ground buses on both sides.

1-4	5-9	10-24
45.00	40.50	36.00

4608-1
Same as 4608, except plain less power buses

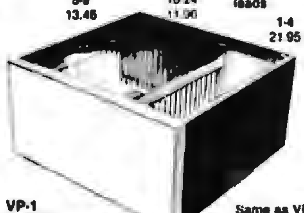
104	5-9	10-24
34.00	30.60	27.20

VECTOR-PAK ASSEMBLED MICROCOMPUTER CASES

Adjustable packaging system for S-100 bus microcomputers, compatible with Altair 8800 and IMSAI 8080 size cards.

- Smart looking, deluxe cases unmarred by unsightly screws or fasteners.
- Finished in dark blue textured vinyl.
- Instantly accessible interiors with slip out covers.
- Removable recessed rear and front panels.
- Fully adjustable interior mounting systems for any card or card spacing within size limitations. No cutting or drilling necessary.
- Perforated bottom cover for cooler operation.

DESCRIPTION
Assembled case with perforated bottom cover Installed mounting struts for card guides and receptacles or mother board Cards top loaded, spanning front to back Card guide (12 pair) and chassis plate supplied uninstalled

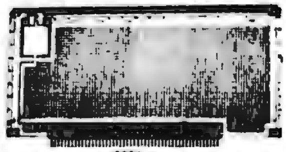


VP-2

Vector

VP-1
$163.00
Shipping Weight 25 lbs.

VP-2
$159.00
Same as VP1 except cards oriented side to side



8801
Individual tinned square pads surround most holes ideal for mounting components by ' tack soldering Top of board pod free for mounting I/O connectors

1-4	5-9	10-24
19.95	17.95	15.96

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S-100 BUS EDGE CONNECTORS

S100-WWG 50/100 Cont 125 ctrs 3 LEVEL WIRE WRAP .025" sq posts on 250 spaced rows GOLD PLATED

1-4	5-9	10-24
$4.00	$3.75	$3.50

S100ALT 50/100 Cont 125 ctrs DIP SOLDER TAIL on 140 spaced rows for ALTAIR motherboards GOLD plated

1-4	5-9	10-24
$4.00	$3.75	$3.50

S100-STG 50/100 Cont 125 ctrs DIP SOLDER TAIL on 250 spaced rows for VECTOR and MASI motherboards GOLD plated

1-4	5-9	10-24
$3.50	$3.25	$3.00

S100SE 50/100 Cont 125 ctrs PIERCED SOLDER EYELET tails GOLD

1-4	5-9	10-24
$5.00	$4.50	$4.25

S-100-CRM 50/100 Cont 125 ctrs 250 spaced rows SMALL DIP SOLDER TAIL PINS for CROMEMCO motherboard

1-4	5-9	10-24
$6.25	$6.00	$5.75

OTHER POPULAR EDGE CONNECTORS

All Edge Card Connectors are GOLD PLATED (not Gold Flash) Bodies are non brittle, Solvent res., G.E Valox. Contacts are Bifurcated; Phos/Bronze: GOLD over Nickel.

ABBREVIATIONS: SE = Solder Eyelet WW = 3 Level Wire Wrap ST = Solder Tail

.100" Contact Center Connectors

PART NO.	TYPICAL APPLICATION	PRICE 1-4	5-9	10-24
D1326-1SE	Imsai M10, SIO	2.10	1.85	1 75
D2244-1WW	Vector Plugboards	4.00	3.80	3 60
D2550-1SE	Imsai P10, Intel Multibuss	3.00	2.80	2.60
D2550-1ST	Imsai P10, Intel Multibuss	3.00	2.80	2 60
D3060-1WW	Intel Multibuss	4.00	3.80	3.60
D3672-1SE	Vector Plugboards	5.00	4 80	4 60
D3672-1ST	Vector Plugboards	4.00	3 75	3 50
D3672-1WW	Vector Plugboards	4.80	4.60	4.30
D4080-1SE	PET	4.80	4 50	4 30
D4080-1ST	PET	4.90	4.60	4.25
D4080-1WW	PET	5.00	4.65	4.35
D4386-1SE	Cos. ELF	5.00	4.75	4 50
D4386-1ST	Cos. ELF	5.10	4.85	4.60
D4386-1WW	Cos ELF	4.95	4.70	4.45
D50100-1WW	Cos. ELF	4.80	4.60	4 30

.125" Contact Center Connectors

PART NO.	TYPICAL APPLICATION	PRICE 1-4	5-9	10-24
D4080-2WW	Vector 4350	5.20	5.00	4.60
S100-STG	S-100, Imsai, Vector Motherboards	3.50	3.25	3.00
S100-WWG	S-100 Wire Wrap	4.00	3.75	3.50
S100-ALT	S-100 Altair	4.00	3.75	3.50
S100-CRM	S-100 CROMEMCO	6.25	6.00	5.75

.156 Contact Centers Connectors

PART NO.	TYPICAL APPLICATION	PRICE 1-4	5-9	10-24
S6X-5SE	Pet, NSC CLK Modules	1.30	1.10	1.00
D612-5SE	Pet, NSC CLK Modules	1.35	1.15	1 05
D1020-5SE		2.00	1.80	1.60
D1224-5SE	Pet	2.15	1.95	1 75
D1224-5ST	Pet	2.15	1 95	1.75
D1530-5SE	Vector Plugboards, GRI Keybrds	2.25	2.05	1 85
D1530-5ST	Vector Plugboards, GRI Keybrds	2.25	2.05	1 85
D1836-5SE		2.40	2.20	2.00
D2244-5SE	Vector, Kim, etc.	2.20	2.00	1.80
D2244-5ST	Vector, Kim, etc.	2.20	2.00	1.80
D2244-5WW	Vector, Kim, etc.	2.40	2.20	2.00
D3672-5SE	Vector Plugboards	3 50	3.30	3.10
D3672-5ST	Vector Plugboards	3.50	3.30	3.10
D3672-5WW	Vector Plugboards	4.00	3.80	3.60
D4386-5ST	Mot 6800, Intel Multibuss	5.00	4.75	4 50
D4386-5WW	Mot 6800, Intel Multibuss, NSC pacer	5.00	4.75	4.50
CG-1	Imsai Style Card Guides	5/1.00 or 100/10.00		

RS232 & "D" TYPE CONNECTORS

P = Plug-Male S = Socket-Female C = Cover-Hood

PART NO.	DESCRIPTION	PRICE 1-4	5-9	10-24
DE-9P	9 Pin Male	1 45	1.35	1 25
DE-9S	9 Pin Female	2 00	1.90	1.80
DE-9C	2 pc. Grey Hood	1.25	1 15	1.05
DA15P	15 Pin Male	2 00	1.90	1.80
DA15S	15 Pin Female	2 80	2.60	2 40
DA15C	15 Pc. Grey Hood	1 50	1 40	1.30
DB-25P	25 pin Male	2.25	2.15	2.05
DB-25S	25 pin Female	3.25	3.05	2.75
DB51212-1	1 pc. Grey Hood	1.30	1.20	1.10
DB1226-1A	2 pc. Black Hood	1.40	1.30	1.20
DB110963-3	2 pc. Grey Hood	1.40	1.30	1.20
DC37P	37 Pin Male	3.70	3.50	3.35
DC37S	37 Pin Female	5 00	4.75	4.40
DC37C	2 pc. Grey Hood	1.95	1.85	1.75
DD50P	50 pin Male	4.40	4 30	4 10
DD50S	50 pin Female	4.90	4 70	4 50
DD50C	1 pc Grey Hood	2.30	2.20	2.10
D20418-S	Hardware Set	75	70	65

Connector for CENTRONICS 700 SERIES:
Amhoenol 57-30360 for back of Centronics 700 Series printers 1-4—$9.00 5-up—$7 50

DIP PLUGS

Part #	No. of Pins	PRICE 1-24	25-99	100-499	Part #	No. of Pins	PRICE 1-24	25-99	100-499
P08P02	8	.41	.36	.29	P22P02	22	75	67	.63
P14P02	14	.48	42	34	P24P02	24	79	71	.66
P16P02	16	.55	.47	38	P28P02	28	1 10	.93	81
P18P02	18	.67	57	.46	P40P02	40	1 25	1 07	94

GOLD SOLDERTAIL STANDARD

	1-24	25-49	50-99		1-24	25-49	50-99
8STG	30	27	.24	22STG	70	.63	57
14SG	35	32	29	24STG	70	.63	57
16STG	.38	35	.32	28STG	1.10	1.00	.90
18STG	52	.47	.43	40STG	1.75	1 55	1 45
20STG	60	56	.52				

TIN SOLDERTAIL · LOW PROFILE

	1-24	25-49	50-99		1-24	25-49	50-99
8CS2	.25	16	.15	22CS2	.37	36	35
14CS2	25	.18	.16	24CS2	.38	37	36
16CS2	25	.20	18	28CS2	.45	44	43
18CS2	29	28	27	40CS2	.63	62	61
20CS2	34	.32	.30				

3 LEVEL GOLD WIRE WRAP SOCKETS

Sockets purchased in multiples of 50 per type may be combined for best price.

	1-24	25-49	50-99	100-249	250-999	1K-5K
8 pin*	41	.38	35	.31	.27	23
14 pin*	39	.38	36	.32	29	27
16 pin*	43	.42	39	.35	32	30
18 pin	63	.58	54	.47	42	36
20 pin	80	.75	70	.63	58	53
22 pin*	.90	.85	80	.70	61	.57
24 pin	90	.84	.78	.68	.63	.58
28 pin	1 10	1.00	90	.84	.76	71
40 pin	1 50	1.40	1 30	1.20	1.04	89

All sockets are GOLD 3 level closed entry. *End and side stacable 2 level Tail, Low Profile, Tin Sockets and Dip Plugs available. CALL FOR QUOTATION

unbeatable GREAT JUMPERS

FLAT RIBBON CABLE ASSEMBLIES AT AFFORDABLE PRICES

- Choice of 3 types of end connectors molded on and factory tested.
- Daisy chain and single-end also available.
- 5 popular sizes to choose from: 20, 26, 34, 40 and 50 contacts, each with line-by-line probe access holes.
- Choice of 2 cable types and 5 lengths.

FLAT RIBBON CABLE

Stranded, 28 AWG with laminated PVC insulation

"Electric Pink" cable has red stripe on one edge for orientation. Used only on double end and daisy chain assemblies.

"Rainbow" cable is coded in standard 10-color sequence on front. Serpentine striping on back aids in identifying wire number and wire group during tear down separation for discrete wire terminations. Used only on single end jumpers.

CARD-EDGE JUMPERS

No Contacts	DOUBLE END Electric Pink 6"	SINGLE END Rainbow 36"	DAISY CHAIN (3 connectors) Electric Pink 6"
20	924052 06 R $5 69	924062 36 R $4 11	924082 06 R $8 42
26	924053 06 R $6 46	924063 36 R $4 88	924083 06 R $9 54
34	924054 06 R $7 96	924064 36 R $6 15	924094 06 R $11 74
40	924055 06 R $9 29	924065 36 R $7 20	924095 06 R $13 70
50	924056 06 R $10 10	924066 36 R $8 21	924096 06 R $14 86

PCB JUMPERS

No Contacts	DOUBLE END Electric Pink 6"	SINGLE END Rainbow 36"
20	924032 06 R $2 57	924042 36 R $2 55
26	924033 06 R $3 32	924043 36 R $3 31
34	924034 06 R $3 95	924044 36 R $4 13
40	924035 06 R $4 57	924045 36 R $4 84
50	924036 06 R $5 67	924046 36 R $5 97

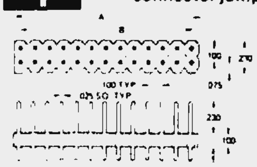
SOCKET JUMPERS

No Contacts	DOUBLE END JUMPER ASSEMBLIES Electric Pink Cable 6"	18"	36"	SINGLE END Rainbow 36"	DAISY CHAIN (3 connectors) Electric Pink 6"
20	924002 06 R $3 70	924002 18 R $ 4 16	924002 36 R $ 4 85	924012 36 R $3 12	924072 06 R $ 5 44
26	924003 06 R $4 78	924003 18 R $ 5 38	924003 36 R $ 6 28	924013 36 R $4 04	924073 06 R $ 7 02
34	924004 06 R $6 25	924004 18 R $ 7 05	924004 36 R $ 8 25	924014 36 R $5 30	924074 06 R $ 9 18
40	924005 06 R $7 33	924005 18 R $ 8 27	924005 36 R $ 9 68	924015 36 R $6 22	924075 06 R $10 76
50	924006 06 R $9 15	924006 18 R $10 31	924006 36 R $12 05	924016 36 R $7 73	924076 06 R $13 43

double-row JUMPER HEADERS

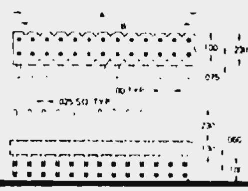
Ideal mates for "GREAT JUMPERS"

- Solder to PC boards for instant plug-in access via socket-connector jumpers
- .025" square posts are molded into plastic header strip on a .10" x .10" matrix
- Choice of straight or right angle configurations



STRAIGHT

No. Posts	Dim. "A"	Dim. "B"	Part Number	Price 2 sets
20	1 0	0 9	923862 R	$ .98
26	1 3	1 2	923863 R	$ 1.28
34	1 7	1.6	923864 R	$ 1.64
40	2 0	1 9	923865 R	$ 1.94
50	2 5	2 4	923866 R	$ 2.36

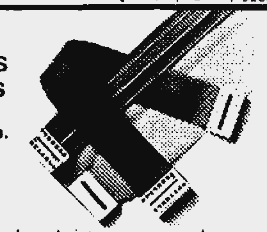


RIGHT-ANGLE

No. Posts	Dim "A"	Dim. "B"	Part Number	Price 2 sets
20	1 0	0 9	923872 R	$ 1 20
26	1 3	1 2	923873 R	$ 1.52
34	1 7	1 6	973874 R	$ 1.96
40	2 0	1 9	923875 R	$ 2.30
50	2 5	2 4	923876 R	$ 2.82

DIP JUMPERS

FLAT RIBBON CABLE ASSEMBLIES WITH DIP CONNECTORS



- Available with 14, 16, 24 and 40 contacts.
- Mate with standard IC sockets.
- Fully assembled and tested.
- Integral molded-on strain relief.
- Line-by-line probeability.

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All assemblies use rainbow cable. Standard lengths are 6, 12, 18, 24 and 36 inches.

WOW

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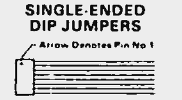
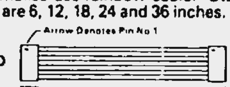


No Contacts	Length 36"
14	924102 36 R $2 33
16	924112 36 R $2 59
24	924122 36 R $4 00
40	924132 36 R $6 71

DOUBLE-ENDED DIP JUMPERS



No. Contacts	Length 6"	Length 12"	Length 18"	Length 24"	Length 36"
14	924106 6 R $2 41	924106 12-R $2 61	924106 18 R $2 82	924106 24 R $3 02	924106 36 R $3 43
16	924116 6 R $2 65	924116 12-R $2 88	924116 18 R $3 11	924116 24 R $3 34	924116 36 R $3 80
24	924126 6 R $4 15	924126 12 R $4 50	924126 18 R $4 85	924126 24 R $5 20	924126 36 R $5 90
40	924136 6 R $6 93	924136 12-R $7 52	924136 18 R $8 11	924136 24-R $8 70	924136 36 R $9 88

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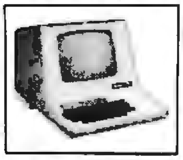

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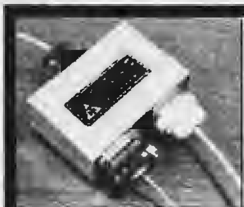

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7	1.66	5.63	10.37/K	8.91/K
7½	1 73	5.89	10.91/K	9.33/K
8	1 78	6.15	11.44/K	9.79/K
8½	1 82	6 41	11.97/K	10.19/K
9	1 87	6.76	12.51/K	10.62/K
9½	1.92	6.93	13.04/K	11.05/K
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12"	1 33	1 44	2 24	2.33	2 55	3.92
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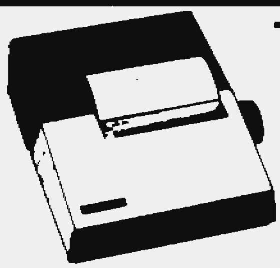

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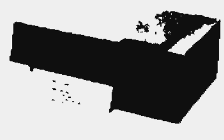
(90 day manufacturer's warranty)

TRS-80 Interface Cable for Black Box Printer w/[illegible] connectors $48.00
[illegible] used with expansion module, [illegible] amp power supply required.

Power Supply for TRS—80/Black Box Printer — $49.00

Integral Data Systems



Check the impressive features on Integral's IP-125 Impact Printer

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• Microprocessor controller • Serial RS232C interface • Parallel TTL level interface • Full upper and lower case ASCII character set (96 characters) • Full 8½ inch wide paper • Line length of 80 columns at 10 characters per inch • Impact printing • 7x7 dot matrix • Ordinary paper roll, fanfold, or sheet • Serial baud rate to 1200 bits per second • Multiple line buffer of 256 characters • Instantaneous print rate to 100 characters per second • Multiple copies without adjustment • Reinking ribbon mechanism • Front panel operator controls • Attractive table top console

IP-125 Integral Data System IP-125 Friction Feed Printer
- 96 upper & lower case ASCII character set
- Enhanced character control
- Serial RS232C Interface (std. factory wiring)
- Parallel TTL Interface (factory wired on req.)
- 80 column line
- 256 byte multiline buffer

$799

IP-225 Integral Data System IP-225 Tractor Feed Printer
- All standard features of IP-125
- Tractor feed paper drive
- Forms Control Option (P1250)

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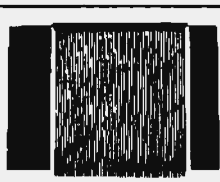

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Card Extender has 100 contacts 50 per side on .125 centers. Attached connector is compatible with S-100 Bus Systems — $26.00
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Same as 8800V except plain, less power buses & heat sink

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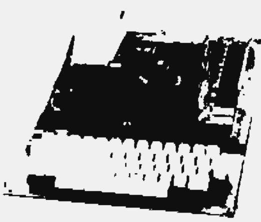

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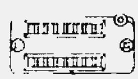

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Assembled & Tested:

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Includes: CPU/Keyboard, Power Supply, Video Monitor, Cassette Recorder, Manual, and Game Cassette.

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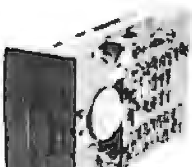
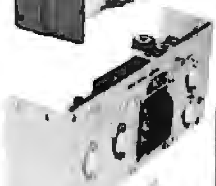
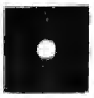


8" Siemens FDD120-8 Drive All Siemen's options included in this drive which can be configured hard or soft and single or double density. (Others give only stripped unit) $425.00



"Power One" Model CP206 Floppy Power Unit. For two drives going full-out, and possably more on less severe service. 2.8A@24V, 2.5A@5V, 0.5A@–5V. Beautiful quality. $99.00



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Cable Kits 10' with 50 cond. cable and connectors and also Molex connectors and power cable: For one drive: $27.50 For two drives: $33.95, and for three drives: $38.95

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10 Megabyte SUPER DISK!!!

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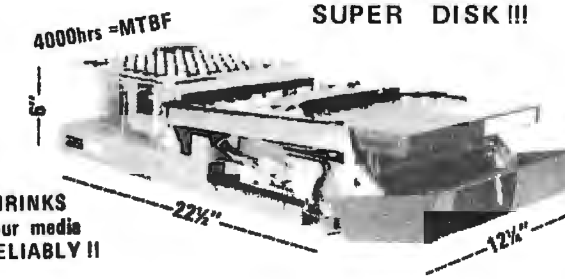

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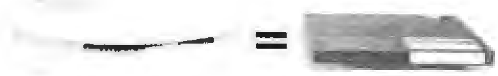

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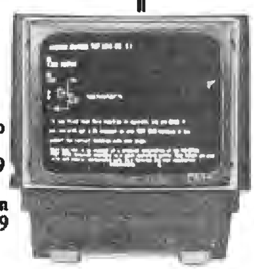

Used Sylvania 12" Video Monitors. Composite video 15mhz, 115vac, 50/60hz New Tube. As shown $109 OEM style without case: $99, Anti-glare tube option add $12. Specify p4 or p39

ESAT200B (Bi-Lingual) 80X24 Communicating Terminal
Scrolling, Full Cursor, Bell, 8X8 matrix, 256 addressable characters 110-19,200 baud, etc, etc ...... This terminal has been purchased by many agencies, universities & companies. Fully stand-alone, It is the only dual font terminal of any kind for less than $2500. Supplied complete and fully guaranteed: (many graphics applications)
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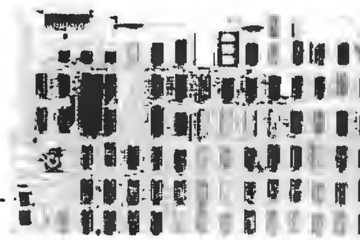

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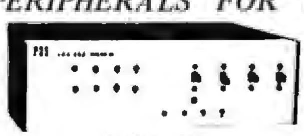
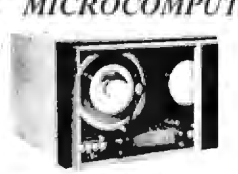
PRINTER TERMINALS



MODEMS



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- Model 5541 (IBM Correspondence code) $695.00
- Model 5550 (corres. code, built-in cassette drive) $1195.00
- Model 5560 (ASCII code, built-in cassette drive) $1295.00

•**IBM SELECTRIC 725 TYPEWRITER I/O** w/solenoids switches & magnet driver PCB (from GTE/IS terminal) plus instructions for 8080 printer-driver interface hardware & software.
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- –POS 103/202 MODEM (Auto-Answer, Auto-Dial). $399.95

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•**CONVERT 15" IBM OFFICE SELECTRIC TO I/O TYPEWRITER:** Kit includes assembled solenoids, switches, wire harness, magnet driver PCB plus instructions for installation and mCPU interface $200.00

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•**FORMS TRACTORS**, Moore Variable width "Form A-Liner" for print terminals:
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- b) Model K81 for QUME or DIABLO Hytype I or II printers (new): $90.00

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- –LAMBDA No. LMEE5 w/OV protect: +5V reg. @ 25A (35 lb.). $59.95

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Trans-Check $29.95 ea.

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DB25S-4-S	4 ft	2-DP25S	$17.95 ea.

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DJ14-1	1 ft.	1-14 Pin	$1.59 ea.
DJ16-1	1 ft.	1-16 Pin	1.79 ea.
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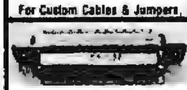
DJ14-1-14	1 ft.	2-14 Pin	2.79 ea.
DJ16-1-16	1 ft.	2-16 Pin	3.19 ea.
DJ24-1-24	1 ft.	2-24 Pin	4.95 ea.

For Custom Cables & Jumpers, See JAMECO 1979 Catalog for Pricing

CONNECTORS
25 Pin-D Subminiature



DB25P (as pictured)	PLUG (Meets RS232)		$2.95
DB25S	SOCKET (Meets RS232)		$3.50
DB51226-1	Cable Cover for DB25P or DB25S		$1.75

PRINTED CIRCUIT EDGE-CARD

.156 Spacing-Tin-Double Read-Out — Bifurcated Contacts — Fits .054 to .070 P.C. Cards

15/30	PINS (Solder Eyelet)		$1.95
18/36	PINS (Solder Eyelet)		$2.49
22/44	PINS (Solder Eyelet)		$2.95
50/100 (.100 Spacing)	PINS (Wire Wrap)		$6.95
50/100 (.125 Spacing)	PINS (Wire Wrap)	R681-1	$6.95

Solar Cells 2x2cm

- 0.4 volts
- 100mA
- 41 MW

Can be added in series for higher voltage or parallel for higher current.

#SC 2x2 $1.95 ea. or 3/$5.00

the 3rd Hand

MAKES CIRCUIT ASSEMBLY A BREEZE!
Lets you work with both hands. Sturdy Aluminum Construction. **$9.95 ea.**

- Clamp "3rd Hand" on edge of bench, table or work-board. Insert circuit board, position components.
- Flip circuit board to flat position for soldering and clipping.

- Bright .300 ht. comm. cathode display
- Uses MM5314 clock chip
- Switches for hours, minutes and hold modes
- Hrs. easily viewable to 20 ft.
- Simulated walnut case
- 115 VAC operation
- 12 or 24 hr. operation
- Incl. all components, case & wall transformer
- Size: 6¾" x 3-1/8" x 1¾"

JE701

6-Digit Clock Kit $19.95

REMOTE CONTROL TRANSMITTER & RECEIVER

$19.95

INSTRUMENT/CLOCK CASE

This case is an injection molded unit that is ideal for uses such as DVM, COUNTER, or CLOCK cases. It has dimensions of 4½" in length by 4" in width by 1-9/16" in height. It comes complete with a red bezel.

PART NO: IN-CC $3.49 each

MICROPROCESSOR COMPONENTS

8080A/8080A SUPPORT DEVICES		
8080A	CPU	$ 9.95
8212	8-Bit Input/Output	3.25
8214	Priority Interrupt Control	5.95
8216	Bi-Directional Bus Driver	3.49
8224	Clock Generator/Driver	3.95
8226	Bus Driver	3.49
8228	System Controller/Bus Driver	5.95
8238	System Controller	5.95
8251	Prog. Comm. I/O (USART)	7.95
8253	Prog. Interval Timer	14.95
8255	Prog. Periph. I/O (PPI)	9.95
8257	Prog. DMA Control	19.95
8259	Prog. Interrupt Control	19.95
6800/6800 SUPPORT DEVICES		
MC6800	MPU	$14.95
MC6802CP	MPU with Clock and Ram	24.95
MC6810API	128X8 Static Ram	5.95
MC6821	Periph. Inter. Adapt (MC6820)	7.49
MC6828	Priority Interrupt Controller	12.95
MC6830L8	1024X8 Bit ROM (MC68A30-8)	14.95
MC6850	Asynchronous Comm. Adapter	7.95
MC6852	Synchronous Serial Data Adapt.	9.95
MC6860	0-600 bps Digital MODEM	12.95
MC6862	2400 bps Modulator	14.95
MC6880A	Quad 3-State Bus. Trans. (MC8T26)	2.25
MICROPROCESSOR CHIPS—MISCELLANEOUS		
Z80(780C)	CPU	$19.95
Z80A(780-1)	CPU	24.95
CDP1802	CPU	19.95
2650	MPU	19.95
8035	8-Bit MPU w/clock, RAM, I/O lines	19.95
P8085	CPU	19.95
TMS9900JL	16-Bit MPU w/hardware, multiply & divide	49.95
SHIFT REGISTERS		
MM500H	Dual 25 Bit Dynamic	$.50
MM503H	Dual 50 Bit Dynamic	.50
MM504H	Dual 16 Bit Static	.50
MM506H	Dual 100 Bit Static	.50
MM510H	Dual 64 Bit Accumulator	.50
MM5016H	500/512 Bit Dynamic	.89
2504T	1024 Dynamic	3.95
2518	Hex 32 Bit Static	4.95
2522	Dual 132 Bit Static	2.95
2524	512 Static	.99
2525	1024 Dynamic	2.95
2527	Dual 256 Bit Static	2.95
2528	Dual 250 Static	4.00
2529	Dual 240 Bit Static	4.00
2532	Quad 80 Bit Static	2.95
2533	1024 Static	2.95
3341	Fifo	6.95
74LS670	4X4 Register File (TriState)	1.95
UART'S		
A-Y-5-1013	30K BAUD	5.95

MICROPROCESSOR MANUALS			
M-Z80	User Manual		$7.50
M-CDP1802	User Manual		7.50
M-2650	User Manual		5.00
ROM'S			
2513(2140)	Character Generator(upper case)		$9.95
2513(3021)	Character Generator(lower case)		9.95
2516	Character Generator		10.95
MM5230N	2048-Bit Read Only Memory		1.95
RAM'S			
1101	256X1	Static	$1.49
1103	1024X1	Dynamic	.99
2101(8101)	256X4	Static	3.95
2102	1024X1	Static	1.75
21L02	1024X1	Static	1.95
2111(8111)	256X4	Static	3.95
2112	256X4	Static MOS	4.95
2114	1024X4	Static 450ns	9.95
2114L	1024X4	Static 450ns low power	10.95
2114-3	1024X4	Static 300ns	10.95
2114L-3	1024X4	Static 300ns low power	11.95
5101	256X4	Static	7.95
5280/2107	4096X1	Dynamic	4.95
7489	16X4	Static	1.75
74S200	256X1	Static Tristate	4.95
93421	256X1	Static	2.95
UPD414 (MK4027)	4K	Dynamic 16 pin	4.95
UPD416 (MK4116)	16K	Dynamic 16 pin	14.95
TMS4044-45NL	4K	Static	14.95
TMS4045	1024X4	Static	14.95
2117	16,384X1	Dynamic 350ns (house marked)	9.95
MM5262	2KX1	Dynamic	4/1.00
PROM'S			
1702A	2048	FAMOS	$5.95
TMS2516 (2716)	16K*	EPROM(Intel 2716) *Requires single +5V power supply	49.95
TMS2532	4KX8	EPROM	89.95
2708	8K	EPROM	10.95
2716 T I	16K**	EPROM **Requires 3 voltages, —5V, +5V, +12V	29.95
5203	2048	FAMOS	14.95
6301-1(7611)	1024	Tristate Bipolar	3.49
6330-1(7602)	256	Open C Bipolar	2.95
82S23	32X8	Open Collector	3.95
82S115	4096	Bipolar	19.95
82S123	32X8	Tristate	3.95
74186	512	TTL Open Collector	9.95
74188	256	TTL Open Collector	3.95
74S287	1024	Static	2.95

CSC CONTINENTAL SPECIALTIES PROTO BOARDS

Proto Board 203

A total ready-to-use power breadboard ... 24 14 ... All metal construction. 9¾" L x 6¾" W x 2¾" H

PB 203 **$75.00**

Model Number	L x W x H (Inches)	Price
PB-6	6.0 x 4.5 x 1.4	$15.95
PB-100	6.0 x 4.5 x 1.4	$19.95
PB-101	6.0 x 4.5 x 1.4	$22.95

Proto Board 203A

All the features of the PB 203 plus additional power supply flexibility, provides 1% Regulated 5VDC supply ... +15VDC and −15 VDC 0.5A supplies, each with internally and independently adjustable output voltage. Ripple and noise of + and −15V supplies 10mV at 0.25A

PB 203A **$124.95**

Model Number	L x W x H (Inches)	Price
PB-102	7.0 x 4.5 x 1.4	$26.95
PB-103	9.0 x 6.0 x 1.4	$44.95
PB-104	9.8 x 8.0 x 1.4	$54.95

B&K PRECISION 3½-Digit Portable DMM

- Overload Protected
- .3" high LED Display
- Battery or AC operation
- Auto Zeroing
- 1mv .1Va .01 ohm resolution
- Overange reading
- 10 meg input impedence
- DC Accuracy 1% typical

Ranges: DC Voltage - 0-1000V
AC Voltage 0-1000V
Freq. Response 50-400 HZ
DC/AC Current 0-100mA
Resistance 0-10 meg ohm
Size 6.4" x 4.4" x 2"

Model 2800 $99.95
Comes with test leads, operating manual and spare fuse

Accessories:

AC Adapter BC-28	$9.00
Rechargeable Batteries BP-26	20.00
Carrying Case LC-28	7.50

CSC 100 MHz 8-Digit Counter

CONTINENTAL SPECIALTIES CORPORATION

- 20 Hz-100 MHz Range
- .6" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable — completely self-contained
- Size — 1.75" x 7.38" x 5.63"
- Four power souces, i.e. batteries, 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply

MAX-100 $134.95

ACCESSORIES FOR MAX 100:
Mobile Charger Eliminator — use power from car battery — Model 100 — CLA $3.95
Charger/Eliminator — use 110 V AC — Model 100 — CAI $9.95

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JE200 5V-1 AMP POWER SUPPLY

- Uses LM309K
- Heat sink provided
- PC Board construction
- Provides a solid 1 amp @ 5 volts
- Can supply up to ±5V, ±9V and ±12V with JE205 Adapter
- Includes components, hardware & instructions
- Size: 3½"x5"x2"H

JE200 $14.95

JE205 ADAPTER BOARD
— Adapts to JE200 — ±5V, ±9V and ±12V

- DC/DC converter w/ +5V input
- Toriodal hi-speed switching XMFR
- Short circ. protection
- PC Brd. construction
- Piggy-back to JE200 board
- Size: 3½"x2"x9/16"h

JE205 $12.95

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$139.95 Kit Only

The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

Data Transmission Method	Frequency-Shift Keying, full-duplex (half-duplex selectable)
Maximum Data Rate	300 Baud
Data Format	Asynchronous Serial (return to mark level required between each character)
Receive Channel Frequencies	2025 Hz for space, 2225 Hz for mark
Transmit Channel Frequencies	Switch selectable: Low (normal) = 1070 space, 1270 mark, High = 025 space, 2225 mark
Receive Sensitivity	−46 dbm acoustically coupled
Transmit Level	−15 dbm nominal. Adjustable from −6 dbm to −20 dbm
Receive Frequency Tolerance	Frequency tolerance automatically adjusts to allow for operation between 1800 Hz and 2400 Hz
Digital Data Interface	EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar)
Power Requirements	120 VAC, single phase, 10 Watts
Physical	All components mount on a single 5" by 8" printed circuit board. All components included

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align

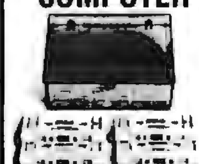
TRS-80 16K Conversion Kit

Expand your 4K TRS-80 System to 16K. Kit comes complete with:

- 8 each UPD416-1 (16K Dynamic Rams) 250NS
- Documentation for conversion

TRS-16K $99.95

COMPUTER CASSETTES



- 6 EACH 15 MINUTE HIGH QUALITY C-15 CASSETTES
- PLASTIC CASE INCLUDED 12 CASSETTE CAPACITY
- ADDITIONAL CASSETTES AVAILABLE #C-15-$2.50 ea

CAS-6 $14.95
(Case and 6 Cassettes)

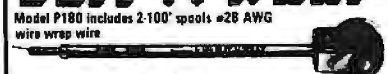
SUP 'R' MOD II
UHF Channel 33 TV Interface Unit Kit

Wide Band B/W or Color System
★ Converts TV to Video Display for home computers, CCTV camera, Apple II, works with Cromeco Dazzler, SOL-20, TRS-80, Challenger, etc.
MOD II is pretuned to Channel 33 (UHF).
★ Includes coaxial cable and antenna transformer.

MOD II $29.95 Kit

SLIT-N-WRAP

Model P180 includes 2-100' spools #28 AWG wire wrap wire



Supplies insulated wire from spool to wrap-posts without prestripping and precutting using "daisy chain" method.

Model P180 Tool $24.50

P180A Replacement Bit	$12.95
W28-2 Replacement wire (3 spool pkg.)	$2.75 ea.

Specify color: A-green B-red C-clear D-Blue

IDEAL FOR TRS 80 — CASSETTE CONTROLLER

"Plug/Jack interface to any computer system requiring remote control of cassette functions"

The CC100 controls cassette motor functions, monitors tape location with its internal speaker and requires no power. Eliminates the plugging and unplugging of cables during computer loading operation from cassette.

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63-Key Unencoded Keyboard

This is a 63-key, terminal keyboard newly manufactured by a large computer manufacturer. It is unencoded with SPST keys, unattached to any kind of PC board. A very solid molded plastic 13 x 4" base suits most application. IN STOCK **$29.95/each**

Hexadecimal Unencoded Keypad

19-key pad includes 1-10 keys, ABCDEF and 2 optional keys and a shift key. **$10.95/each**

Circle 200 on inquiry card.

Circle 30 on inquiry card.

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Satisfaction Guaranteed

EDGE CARD CONNECTORS: GOLD PLATED. (Not Gold Flash)
BODY: Non brittle, Solvent res., G.E. Valox.
CONTACTS: Bifurcated, Phos/Bronze, Gold over Nickel.
ABBREVIATIONS: S/T Solder Tail, S/E Sold. Eyelet:
W/W Wire Wrap 3; SW/W Short W/Wrap;

PART #	Description	Row Sp.	1-4	5-9	10-24
5010	50/100 S/T ALTAIR	140	3.75	3.50	3.30
5020	50/100 S/T IMSAI	250	3.95	3.75	3.50
5030	50/100 W/W IMSAI	250	4.10	3.90	3.70
5040	50/100 S/E ALT/IMSAI	140	5.00	4.50	4.25
5050	50/100 S/T CROMEMCO	.250	6.25	6.00	5.75
1450	IMSAI CARD GUIDES		0.16	0.14	0.12
.100" Contact Center Connectors					
1020	13/26 S/E Imsai MIO:	140	2.10	1.85	1.75
1040	25/50 S/E	140	2.95	2.75	2.50
1050	25/50 S/T	140	3.00	2.80	2.60
1060	36/72 W/W Vector	.200	4.80	4.60	4.30
1065	36/72 S/T Vector	.200	4.00	3.75	3.50
1070	40/80 S/E PET	140	4.80	4.50	4.30
1075	40/80 W/W PET	200	5.00	4.65	4.35
1080	40/80 S/T PET	140	4.90	4.60	4.25
1085	43/85 S/E Cos.ELF	140	5.00	4.75	4.50
1090	43/86 S/T Cos.ELF	.140	5.10	4.85	4.60
1093	43/86 S/T Cos.ELF	.200	4.95	4.70	4.45
1095	43/86 W/W Cos.ELF	.200	5.50	5.20	4.90
POLARIZING KEYS: For Above			0.10	0.10	0.10
.156" Contact Center Connectors.					
1550	6/- S/E PET,Etc	.140	1.30	1.10	0.90
1560	6/12 S/T PET:NSC.	140	1.35	1.15	0.95
1575	12/24 S/E PET	.140	2.15	1.95	1.75
1580	12/24 S/T PET	.140	2.10	1.90	1.70
1590	15/30 S/E GRI Keybd.	.140	2.25	2.05	1.85
1620	18/36 S/E	.140	2.40	2.20	2.00
1650	22/44 S/E KIM,VECTOR	140	2.20	2.00	1.80
1660	22/44 S/T KIM,VECTOR	140	2.00	1.80	1.70
1670	22/44 W/W KIM,VECTOR	.200	2.40	2.20	2.00
1690	36/72 W/W	.200	3.90	3.75	3.50
1710	36/72 S/E	.140	3.50	3.30	3.10
1720	36/72 S/T	.200	3.30	3.10	2.90
1730	43/86 S/T Mot. 6800	.140	4.40	4.15	3.90
1740	43/86 S/T Mot. 6800	.200	4.35	4.10	3.85
1750	43/86 W/W Mot. 6800	.200	4.45	4.25	4.10
POLARIZING KEYS: For Above			0.10	0.10	0.10

RS232 & 'D' TYPE SUBMINIATURE CONNECTORS:

QUANTITY		1-4	5-9	10-24
DE9P Male		1.45	1.35	1.25
DE9S Female		1.93	1.80	1.70
DE110963-1	2pc. Grey Hood	1.20	1.10	1.00
DA15P Male		1.95	1.80	1.70
DA15S Female		2.80	2.60	2.40
DA51211-1	1pc. Grey Hood	1.25	1.15	1.10
DA110963-2	2pc. Grey Hood	1.22	1.10	1.05
DB25P Male		2.20	2.10	1.90
DB25S Female		3.20	3.00	2.70
DB51212-1	1pc. Grey Hood	1.30	1.20	1.10
DB51226-1A	2pc. Black Hood	1.40	1.30	1.20
DB110963-3	2pc. Grey Hood	1.35	1.25	1.15
DC37P Male		3.70	3.50	3.35
DC37S Female		4.90	4.70	4.40
DC110963-4	2pc. Grey Hood	1.95	1.85	1.75
DD50P Male		4.40	4.30	4.10
DD50S Female		4.90	4.70	4.50
DD51216-1	1pc. Grey Hood	2.30	2.10	1.90
DD110963-5	2pc. Grey Hood	2.40	2.20	2.00
D20418-2 Hardware Sets		0.75	0.70	0.65

I.C. SOCKETS, GOLD. WIRE WRAP 3 TURN.
14 pin $0.36 ea.
16 pin 0.38 ea

I.C. SOCKETS. Dip Solder. Tin.
14 pin $0.15 ea
16 pin 0.17 ea

8080 PRIME
$8.00 ea

2708 EPROMS PRIME
$14.00 ea.

CONNECTORS FOR CENTRONICS 700 SERIES:
Amhpenol 57-30360 For Back of Centronics '700' Series:
Price. $9.00ea. 5 pcs. $7.50ea.

WHISPER FANS: Excellent for Computer cabinet cooling. Extremely quiet.
Dim. 4-3/4" x 1-1/2" thick. U.L. Listed.

1-4	5-9	10-24
$22.00	$19.00	$18.00

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- 72 KEY KEYBOARD

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FUTURE PRODUCTS: 80 CHARACTER VIDEO BOARD,
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CB-1 8080 Processor Board. 2K of PROM 256 BYTE RAM power on/reset Vector Jump Parallel port with status. Kit..............$125.95 PCBD............$28.95

MB-6A Basic 8KX8 ram uses 2102 type rams, S-100 buss. Kit 450 NSEC .. $123.95. PCBD $24.95

MB-7 16KX8, Static RAM uses µP410 Protection, fully buffered KIT $299 95

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MB-9 4KX8 RAM/PROM Board uses 2112 RAMS or 82S129 PROM kit without RAMS or PROMS $72 00

IO-2 S-100 8 bit parallel /IO port, ²⁄₃ of boards is for kludging. Kit .. .$46.00 PCBD $26.95

IO-4 Two serial I/O ports with full handshaking 20/60 ma current loop. Two parallel I/O ports. Kit, $130.00 PCBD .$26.95

VB-1B 64 x 16 video board, upper lower case Greek, composite and parallel video with software, S-100. Kit .. . $125.00 PCBD $26.95

Altair Compatible Mother Board, 11 x 11½ x ⅛"
Board only ....$39.95. With 15 connectors $94.95

Extended Board full size. Board only $ 9.49
With connector $13.45

SP-1 Synthesizer Board S-100
PCBD. . $42.95 KIT $135 95

82S23	$1.50	PRIME SUPPORT	
82S123	1.50	8080A	$ 9.95
82S126	1.95	8212	3.25
82S129	1.95	8214	6.50
82S130	3.95	8224	3.49
82S131	3.95	2114 (450 NS) Low PWR	7.25
MM16330	1.50	2114 (250 NS) Low PWR	7.99
IM5600	1.50	2102A-2L	1.60
IM5603	1.95	2102A-4L	1.25
IM5604	3.95	2708 450 NSEC	8.95
IM5610	1.50	1702A-6	3.50
IM5623	1.95	4116 (Apple RAM)	.12.95
IM5624	3.95		8/89.95

WMC inc. **WAMECO INC.**

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remic 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not inclulded).
PCBD .$42.95

FPB-1 Front Panel, IMSAI size, hex displays. Byte. or instruction single step
PCBD $47.50

MEM-1 8KX8 fully buffered, S-100, uses 2102 type rams PCBD $25.95

QM-12 MOTHER BOARD, 13 slot, terminated, S-100 board only $34.95

CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD $26.95

RTC-1 Realtime clock board Two independent interrupts. Software programmable PCBD $25.95

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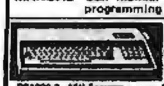

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XR1488P	1.31	XR2207N	5.26	XR2242CP	1.60	XR4558CP	.75
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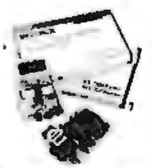

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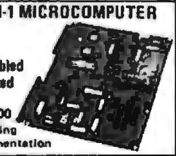

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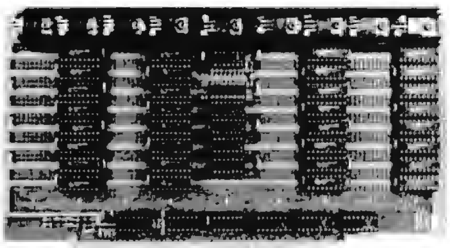

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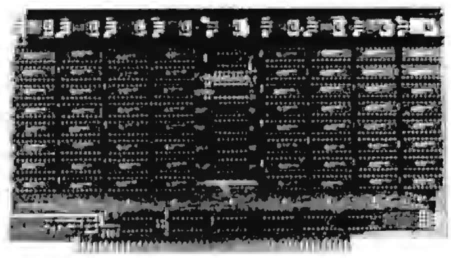
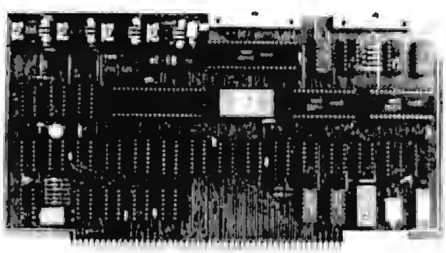
32K →





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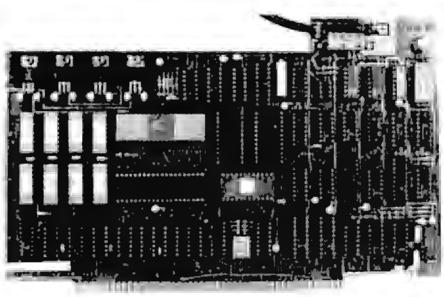

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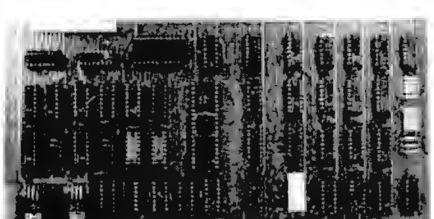

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WANTED: Maintenance manual or schematic information for Frieden Flexowriter model 2301A or similar unit. Will pay $5. for schematic or $25 for manual. William A Brown, 79 Salem Hl Rd, Howell NJ 07731, (201) 364-6532.

GAMES FOR SALE: Programs on cassette for Level I TRS-80. Star Trek (so compact it runs on 4 K) $10. Ping-Pong (4 K) $5. Lunar Lander (4 K) $5. Add $5 for cassette and shipping. M Feeley, 150-15 Ave, Iberville Quebec CANADA, J2X 1A3.

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FOR SALE: H11 (LSI processor) with arithmetic chip and 16 K. Manuals and softwear. New cost (kit) $1,850. Would like $1,600. Also H10A; new cost (kit) $350, but have had trouble. Will sell for $200, with manuals. James L Achord, 2500 North State St, Jackson MS 39216.

FOR SALE: TI Microterminal for use with TM990 series microcomputers. $75. 12 inch modified line isolated video processor. $60. Quality keyboard case. $25. Miscellaneous character generators, 2102s, 1702As. K Zandler, 481 N Armistead St, Alexandria, VA 22312, (703) 664-6460 during day.

HELP: Need Memorex Model 1240 terminal service manual. Also print cartridge and print cartridge drive belt. Johannes Oelke, 8852 Rock Forest Dr, St Louis MO 63123, (314) 421-5055 (Mon thru Fri) or (314) 843-5609 evening.

WANTED: New or used dumb video display or PET. Also a modem for either. Jonathan Guttenburg, 125 E 72 St, New York NY 10021.

FOR SALE: Heath H8, 16 K, serial I/O (input/output), video display terminal, and all Heath software. Working great. Bargain at $1000. Jeff Lambros, 7 Parkshore Cir, Sacramento CA 95831, (916) 422-7802.

FOR SALE: KIM-1, TVT-6 and an ASCII Keyboard wired with software for use as an ASCII controlled video terminal. Complete documentation. Plus *First Book of KIM, Cheap Video Cookbook, KIM-1 User Notes, Microchess* and other utility and game programs on cassette. Will pay shipping. $250. John Dobiac, QTRS 770-2, Ft Ritchie, MD 21719, (301) 241-4744.

FOR SALE: Heath H9 video terminal. Up and running, all documentation included. $425. Dr Bauman, 509 Wolcott Rd, Wolcott CT 06716 (203) 879-3865.

WANTED: Information on the IBM Cardatype typewriter, type 866 and 868 or on the IBM electric typewriter Model 11C. I would like manuals, parts, or other data to help me convert this machine to a printer for a 6800 microcomputer. John Kluth, 1060 DeLeone Dr, Kent OH 44240.

WANTED: Operations manual and schematic for a Dumont Labs type 350-R oscilloscope. Will pay any reasonable price for copies. James Brown, 15 New Ocean St, Lynn MA 01902.

FOR SALE: TMS-9900 16 bit Techinco starter system with monitor, Assembler, 1.5 K power, manuals. $450. Datel Selectric terminal with full ASCII I/O (input/output) RS-232, extensive manual $700. Power Supply ± 5 V ± 12 V common ground at 1.3 A regulated and protected S50. David Lynn, 1913 Kingsland Av, Orlando FL 32808, (305) 293-4074 after 6 pm.

WANTED: Back issues of *Software-Practice and Experience, Computer Graphics, Computer Journal, SIAM journals;* other computer journals excluding ACM. William G Hutchison Jr, Princton Arms N 191, Cranbury NJ 08512, (609) 443-6631.

EMPLOYMENT WANTED: Graduated December 1978 from Central Michigan University with a Bachelor of Independent Study degree in Electronic Sound Synthesis (minor in Computer Science). Also hold Associate degree in Industrial Electronics. Seeking employment in electronic sound synthesis but will consider other areas. I have an excellent background in microcomputers. Steven Petersen, 3111 Bird Av NE, Grand Rapids MI 49505, (616) 361-6083.

FOR SALE: Heath H10 reader/punch assembled and tested. Never bought rest of Heath system. $280. Also Scientific Devices digital capacitance meter, factory built, $60. Jeff Duntemann, 6208 N Campbell Av, Chicago IL 60659, (312) 764-5069 evenings, 648-1668 days.

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FOR SALE: Paratronix model 100A logic analyzer, new, assembled and working, $165 (factory price: $229 kit, $295 assembled). I bought a Paratronix 150. C J Drost, Cornell University, College of Vet Med, Ithaca NY 14853, at office: (607) 256-2121, or at home (607) 272-2458.

FOR SALE: Heathkit owners; assembled 12 K programmable memory board for H8. $180. (Godbout Econoram VI). Darrell Mears, 201 Prospect St, Blacksburg VA 24060.

FOR SALE OR TRADE: Integrand S-100 rack mountable mainframe. Includes 11 slot motherboard, five connectors in place, 15 A power supply, and fan. Never been used. First check or money order for $220, or I will trade it for a KIM-1 like new with power supply and all manuals. David Minuk, 467 E College St, Murfreesboro TN 37130, (615) 890-1701.

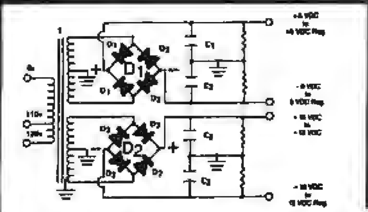
WANTED: Operating manual, service manual, and used disk packs for an IBM 2311 disk drive. Also any information pertaining to a source for the above or use of the 2311 in a hobby computer. Mike Braun, 200 N Adams, Mt Pleasent IA 52641 (319) 385-2000.

WANTED: Technical data on a Foto-Mem Inc video display terminal. Has Ball Brothers video display model TV-12C 7-012-0100, micro switch keyboard SW-10255 and auxiliary keypad SW-10112. Display 80 characters, 24 lines. Fred Ordway, POB 5946, Bethesda MD 20014.

FOR SALE: Digital Group 10 K Z-80 system with two Phi-Decks 64 character-video, Javelin monitor, keyboard, power supplies. No cabinets. Fully functional. $1,500. or best offer. Grant Youngman, 3731 Bramblevine Cir, Lithonia, GA, 30058 at office (404) 586-8727, or at home: (404) 981-6640.

MEMORY: Static 16 K byte memory board for S-100 computer made by Vandenberg Data Products, uses UPD410 circuits addressed in 4 K blocks. Assembled, works perfectly. $200. Steve Goldband, 58 Inwood Pl, Buffalo NY 14209. (716) 886-1020.

FOR SALE OR TRADE: BYTE magazine 16 issues Volume 1 thru Dec 76, excellent condition. $125, or swap for KIM-1, Heath ETS3400, ELF II, TI-58, or in part for challenger 1P, AIM 65, TI-59. After 5 PM and weekends. Ralph Reinke, 3007 Heron Ave, Wausau WI 54401, (715) 842-0196.



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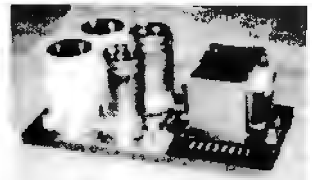

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Video Out in Front

Voting on the February 1979 BOMB card was rather close. The first and second place winners placed 8.75 and 8.46 points above the standard deviation. The third and fourth place articles were 7.38 and 7.09 points above the standard deviation.

In first place was Timothy Loos for his short hardware article entitled "Use a Television Set as a Video Monitor." In second place was John Giacomo for his "Stepping Motor Primer." These authors will receive $100 and $50 respectively.

Placing third was "A Microprocessor for the Revolution," by Terry Ritter and Joel Boney followed closely by Steve Ciarcia's "Build a Computer Controlled Security System."

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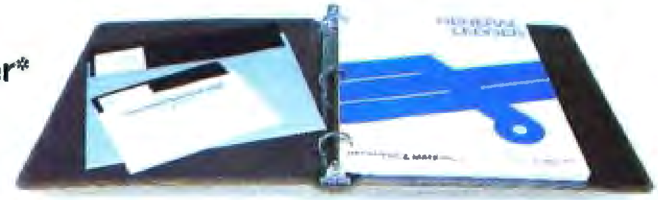

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