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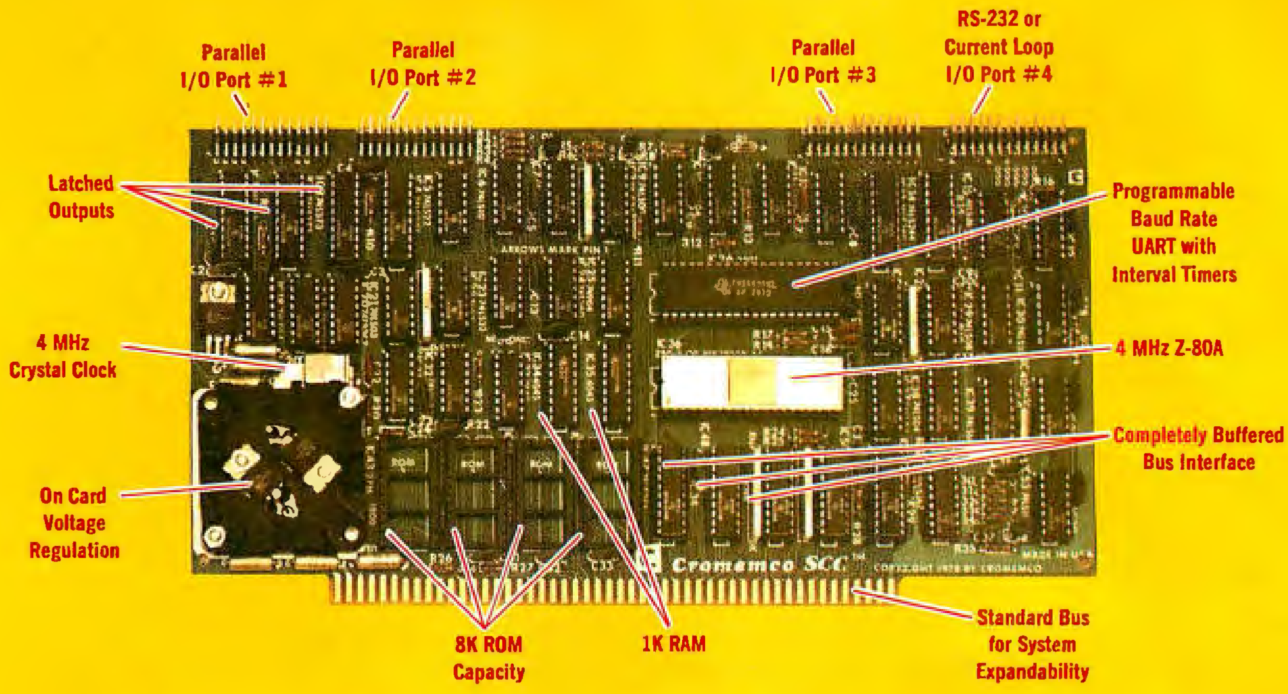

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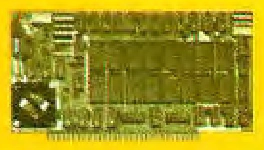

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Circle 1 on inquiry card.

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Volume 5, Number 6

In The Queue


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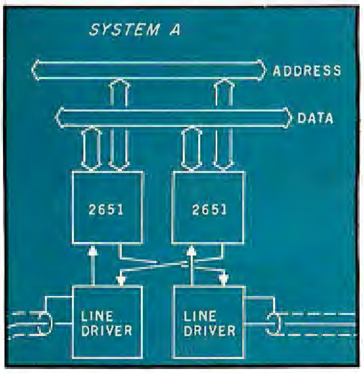

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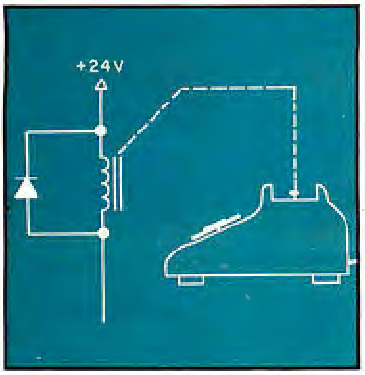

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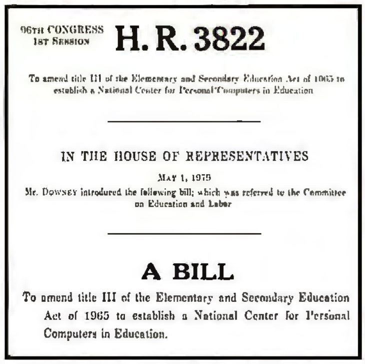
96TH CONGRESS 1ST SESSION **H. R. 3822**

To amend title III of the Elementary and Secondary Education Act of 1965 to establish a National Center for Personal Computers in Education

IN THE HOUSE OF REPRESENTATIVES

MAY 1, 1979

Mr. DOWNEY introduced the following bill; which was referred to the Committee on Education and Labor

A BILL

To amend title III of the Elementary and Secondary Education Act of 1965 to establish a National Center for Personal Computers in Education.

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ON THE COVER

On this month's cover, Robert Tinney has created a visual fantasy on a communications theme. Imagine a network of personal computers where each person's computer is a node. Each node can display some information about the network. The fantasy cover painting shows several such personal computers in a matrix of translucent network connections. A few message packets are in transit down gossamer conduits, and each computer shows a view of the network from that node's vantage point.

As noted in this month's editorial, the real-world equivalent of this fantasy is the telephone network with low-speed modem equipment. While 300 bps is not the data communications equivalent of the bandwidth of a light beam, it is a good start which exists today. The nodes we know about via modems and telephones consist of our personalized directories of public access and private computer systems.

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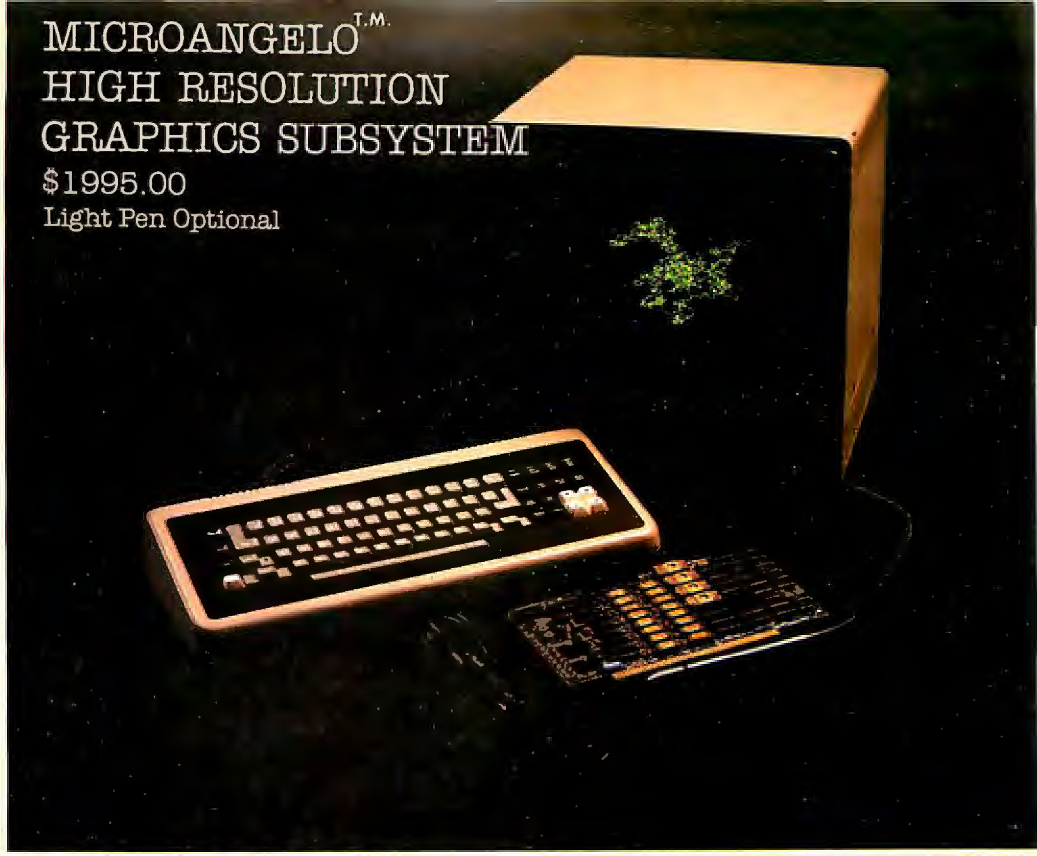

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Editorial

The Grass Roots Electronic Post Office

or, How Electronic (and Private) Mail Is Already Here

by Carl Helmers

How many of our readers could agree with the following propositions about ways in which they live?

I never use a telephone.	( ) Agree	( ) Disagree
I never talk with anyone.	( ) Agree	( ) Disagree

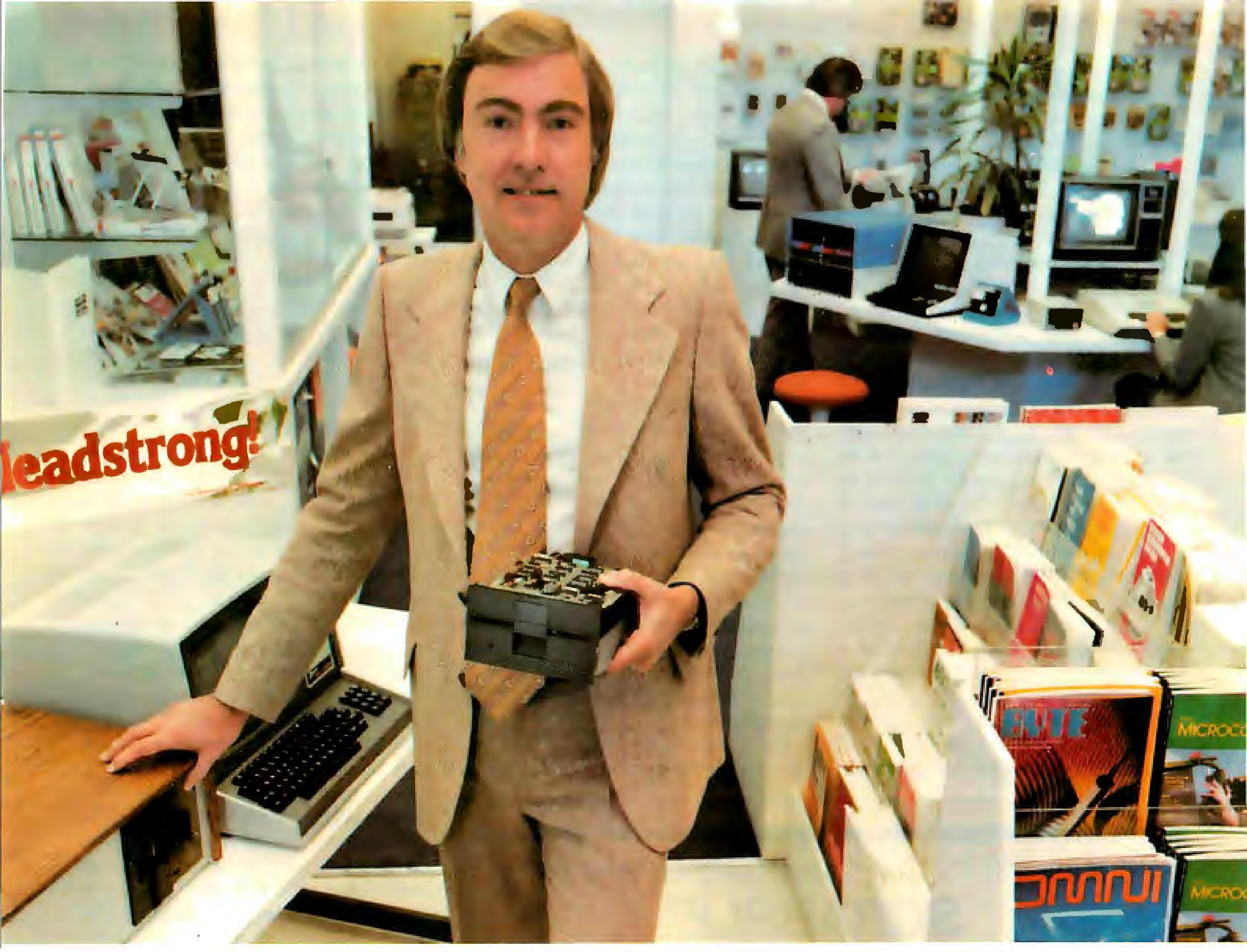
Most readers would disagree with both propositions, since they use telephones and talk to one another—as do most people in our society. One would be tempted to compare the first proposition with the second by noting that telephone use is simply talking augmented by technology. Talking does not require any technology, whereas using a telephone does. However, both are means of communication (ie: sending and receiving messages). Talking and telephone use both require what is perhaps our oldest technology: verbal reasoning within a commonly defined language.

Communications is the theme of this issue of BYTE and our emphasis is on extensions to the scale of this technology. We are talking about telephone networks with personal computers attached. The medium is the telephone network, and computers are the tools. We offer a number of articles this month covering areas as diverse as the technology of modems to their use in new forms of electronic-publication services for personal-computer users. In future months, readers will see more articles on communications applications of small computers.

The personal computer heralds the beginning of an age of personal data communications, encouraged by recent changes in telephone rules which allow "foreign" attachments to be connected with the telephone network. An unplanned side effect of these rule changes is that a personal computer can be one of those foreign attachments, in addition to the various forms of non-Bell domestic telephones and phone-answering machines.

We now see the ability for a personal-computer owner to send a message to another via the telephone network at any time of the day or night. The receiving computer will most likely have a floppy disk for storage and a printer for hard-copy output. If a letter takes a week to arrive at its destination or may be forever lost, why even bother with "first class" mail? A slightly more expensive electronic system already exists through data communications. These facts guarantee the existence of the completely unofficial, unplanned "Grass Roots Electronic Post Office."

For one of our readers with a personal computer to open his or her own box in the Grass Roots Electronic Post Office there is an initiation fee of sorts, namely the price of some standard or custom software and Federal Communications Commission (FCC) approved and registered modem-phone connection to the typical small computer. The auto-answer/auto-dial modem is the enabling technology for the personal computer in this application. The key to the user's mailbox is the software running in the computer. The address is provided by the telephone network as the usual phone number. A common language is provided by 8-bit asynchronous serial communications at 300 bits per second (bps).



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The network has existed since the phone companies made direct-dialing telephones practically universal in recent years. The telephone companies have solved all the problems of sending messages by the best routes, addressing the recipients of the messages, and running the needed lines. They provide a universally switched bandwidth adequate for 300 bps (30 characters per second) with simple Bell 103-style modems. With these specifications a three-minute phone call transmits 5400 characters of information. This is approximately equivalent to three 1920-character (24-by-80) terminal screens full of information, or a page and a half of formatted printed text. To send such a message from New Hampshire to a friend of mine in Santa Clara, California, would cost about $0.60 at the current rates, if done at night or on the weekend. This is not an excessive premium over the cost of a $0.15 first-class letter which might get there within a week.

Thus any two people who have a personal computer and a Bell 103-compatible modem can send electronic messages back and forth. Such messages can be on an "instant" basis with the two parties actively at a terminal. Or such messages can be sent on a "store-and-forward" basis, in which case no active human intervention is needed at either end at transmission time; messages are created as text files with addressee information. Then, at the optimal time of day from a telephone-rate point of view, these text files are sent to the appropriate recipients with similar computers.

The purposes of such communications are as varied as the purposes of any communication. The communication can be made totally private, if desired, by use of an automatic encryption technique, or the communication can be as open as the normal telephone call. As more and more people obtain this type of equipment, especially the auto-answer/auto-dial type of modem, there is the need for directories of people with active data nodes on the phone network.

Most everyone keeps a personal directory of telephone numbers in a more or less organized fashion. With a personal computer, such a directory can be kept on a floppy disk. Using an auto-dial modem which can disconnect its carrier after dialing, automatic dialing of voice calls is possible. A natural extension is to maintain a personal directory of modem communications contacts along with the mode of operation used.

Just as a telephone-company directory goes far beyond an individual's list of friends and contacts, we may see modem manufacturers, independent publishers, or computer clubs publishing directories. Each entry would consist of the telephone number and any equipment information needed for random access. The widespread publication of general access information for private computers really defines the Grass Roots Electronic Post Office as a social phenomenon larger than its origins with individuals and small groups.

One thing we do not need as users, however, is the United States Postal Service (USPS) intervention. Today the system works through the wonders of our existing AT&T network. But then, private-letter express companies worked very well before the government postal monopoly was given legal protection in the nineteenth century. Occasional challenges of the private express statutes and USPS inefficiency are made. Companies making the challenge have shown excellent profitability prior to being closed down by the government-enforced postal monopoly. If these companies were allowed to exist and expand, we might have a little improvement (lower prices, better service) in first-class mail delivery.

In spite of heavy regulation, telephone companies work very well. After many decades of government-sanctioned limitations on competition, telephone companies are now facing new rivalries from many sources. Alternative long-distance voice and data-communications techniques now exist over microwave and satellite links. Competition is growing in alternative telephone set designs. The fact that modems can be connected to the telephone network at all is part of this recent regulatory reform.

Running counter to this liberalizing trend is the U S Postal Service's recently expressed desires to "provide" electronic mail. A political reaction from the U S Postal Service and its

allies in Congress could adversely affect the future of a Grass Roots Electronic Post Office. Based on the past effectiveness of the Postal Service, the results could well be disastrous. In a confrontation between the FCC and the Postal Service during 1979, the FCC came out as a defender of electronic media from interference.

Assuming that political problems are not sufficient to hinder the growing private use of data-communications techniques, what technical problems might be present? The technical basis of raw communication was set many years ago with the definition of the Bell 103 modem standard. Perhaps the most significant remaining problem is the definition of "generally accepted" protocols for two-user interactions of various kinds. (Multiple-person, conference call interactions are the exception in telephone usage.)

Protocols of this sort often grow out of practice in the art. A parallel example from a related communications field is the protocol used by citizen band (CB) radio correspondents. It is derived from common usage, and has evolved in time as a subset of the English language. But it is a protocol with defined meanings and semantics taken from common English. One fairly standard communication protocol already exists in the form of "computerized community bulletin-board systems" (CCBBS) begun by Ward Christensen and Randy Suess of the CACHE computer club in Chicago, Illinois. Many similar systems now exist as the software percolates around the country.

We can expect operating protocols for computers attached to the phone network to be as varied as the different styles of operating systems. We hope to find a generally accepted protocol for some key items. For example, the characters used to invoke a "Help" system usage aid may reduce through practice to one or more alternatives. This is somewhat akin to CB common usages like "10-4 good buddy" meaning "yes." It will be interesting to see what develops in this area.

But whatever the command practices that evolve, an underlying standard is provided by the American Standard Code for Information Interchange (ASCII) standard, as recently extended. Every personal computer made in the United States uses some adaptation of the ASCII standard for character information. And, in ASCII, certain codes have predefined semantic meanings such as "acknowledge," "negative acknowledge," "carriage return," "line feed," etc. These predefined meanings can be used to some advantage; they represent a history of conventions that antedate widespread personal computer usage. There is no real need to reinvent a wheel which grew out of facing these problems of computer-to-computer communications.

In summary, while there are some nagging problems, the Grass Roots Electronic Post Office is alive and well. It exists in the hardware and software of personal-computer users who have modems as part of their systems. As a means of sending messages and using the telephone network more effectively by individuals or businesses, it has grown out of the simple availability of the hardware. It is not yet formally recognized enough to have its own directory publications. But wherever there exist two friends with modems there is a high likelihood of communication being used. The future for communications by personal computer looks bright.■

Notes by Carl Helmers

Many of our readers will want to explore further this idea of personal use of data communications. An excellent source of information is found in the manuals provided by D C Hayes Associates Inc that accompany its communications products. This company markets an S-100-compatible modem and an Apple-compatible product which is called Micromodem II. These comments are based on the manual for the Micromodem II, written by Donald J Hyde.

The content of the Micromodem II Owner's Manual *is an example of some of the best documentation available. We find an 81-page booklet which is well illustrated with technical drawings and examples. It begins with the expected details of installation and use of the Micromodem's built-in programs. It then progresses to a complete discussion of elementary modem programming, illustrated by examples. We find out how to dial the telephone, hang up the telephone, answer the telephone, transmit data and receive data—all from examples given in BASIC. (D C Hayes promises to release information on use of the Micromodem with Apple Pascal, but as of this writing it has not been received. In a phone conversation in mid-March, we found that the Pascal software for Micromodem II is complete but not 100% debugged. Readers can expect to see the Pascal software available soon.)*

Under other headings, we find advanced programming techniques such as manipulation of hardware defaults, turning off the carrier so that another phone on the same line can be used for voice purposes, waiting for the Nth ring, etc. Inspirational programs are provided in a chapter of that name in order to give examples of applications such as repertoire dialing, and even a computerized wakeup call-generator.

A tutorial chapter is devoted to background information on the phone network, Bell 103 modems, data rates, ringing, and dialing. Although the source listing for the read-only memory (ROM) programs is not given in the manual (it should have been), there should be enough documentation to manipulate the hardware through these routines. And if worse came to worst, one could always disassemble the ROM programs. (Apple Pascal users should note, however, that present PROMs are useless due to references made to the Apple firmware replaced by the Pascal systems software.)

So, if readers are looking for some information on the technical details to support this concept for the Grass Roots Electronic Post Office, we highly recommend perusal of this D C Hayes manual. Another source of similiar information is Ronald G Parsons' article "An Answer/Originate Modem," found on pages 24 thru 40 of this issue of BYTE.

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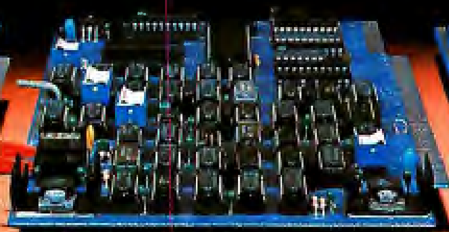
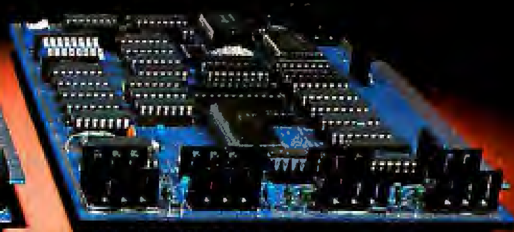

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It generates both U.S. and European TV rates and meets the new IEEE S-100 standard. Other features include keyboard input, black on white or white on black, one level of grey, underline, strike thru, blinking char., blank-out char., and programmable cursor. Software includes a CP/M compatible driver and a powerful terminal simulator.

VB3 is available in several configurations. Retail prices start at $375 kit, $440 assembled.

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Letters

Review of Some Excellent Marketing and Pointers for Companies Marketing Computers

I read Carl Helmers' editorial in the January 1980 BYTE ("The Era of Off-the-Shelf Personal Computers Has Arrived," page 6), and I thought your readers might, in turn, be interested in my recent experience in approaching the purchase of a personal computer. First of all, let me mention that I am a consulting engineer in optics and instrumentation and must, therefore, own most of my own tools (computers). Before I give some words about my experiences in the hunt for a satisfactory personal computer, may I give some technical background about one major area of my work and the requirements I have for the personal machine?

Lenses and mirrors are part of the optics I design. The design of combinations of these to satisfy some client requirement is a complex and often laborious calculating task. Tracing a single light ray through one lens or mirror surface in accordance with the rigorous physical-mathematical rules takes as many as 350 steps of file manipulation and arithmetic or higher mathematical calculations. To complete a design may take thousands of these ray-surface calculations. Worse yet, most optical designs are compromises against focusing errors (aberrations), and the computer must seek to improve the given lens design by reducing these errors using matrix calculations. Often, the matrices are as large as 40 by 40, or even bigger. Because matrices of this size are often not completely soluble, least-squares reduction of residual aberrations (by damping the matrix) is now the popular method of computing optimal lens designs. So, the matrix has to be resolved several times—called "iterations toward the optimum solution."

So, the outcome of all of this is my requirement that the personal computer be strongly oriented toward number crunching. Also, the matrix inversion (solution) may depend on maintaining a large number of significant digits in each number. Thus, we arrive at one of my major complaints against personal-computer advertising: there is almost no reference to the *number of digits* available in single-precision computing. Let me now go ahead and list some of my complaints about personal-computer advertising and promotional literature from the manufacturers:

1) Lack of description—number of digits in single precision.
2) Limited number of math functions available.
3) Lack of description—speed of typical calculation.
4) Frequent absence of full list of required hardware components. What is needed to be fully up and running—controllers, interconnecting special cables, etc.
5) Pricing for complete package—ready to plug in and use for calculations.

As an engineer, I need to know these facts to determine if the machine is the one I should buy.

As if in answer to my questions, Hewlett-Packard (HP) recently released technical information about the HP-85 personal computer. Almost every question I might think of which bears on my decision to purchase was answered in their technical data sheet. Of course, there are some things about the HP-85 which are less than satisfactory, but, and this is very important, when I finally got to see the machine and run it for a few minutes, there were no surprises! Just about everything I expected from the brochure was found, including some of the not-so-good items. I was thus able to make up a point-score on the machine and make my decision without a lot of unknowns.

Well, where does this lead to? I suggest that the following be recommended to personal computer manufacturers:

1) There are many, many potential buyers who need to know things about a machine that are not now mentioned in the literature or ads.
   a) What are the components necessary to get a ready-to-run package? What price?
   b) How fast does the machine accomplish a typical task (some kind of benchmark test)?

Circle 5 on inquiry card.

Circle 6 on inquiry card. →

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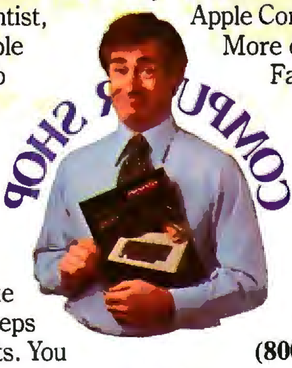

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c) What are the number of digits available in single precision? What math functions?

2) Take a look at the HP data sheets to see what kind of information attracts the engineers, and what is needed. Issue a similar data sheet for your machine, as a complete system ready to plug in and run.

I realize that ANSI BASIC describes pretty well a lot of the things I mentioned. However, there seems to be a wide difference between individual BASICs in important details. These should be admitted and exposed.

Many of my friends and acquaintances have purchased small personal computers. One thing which disturbs them is the lack of a firm support commitment and a method of getting repairs and maintenance. I have heard it said more than once that the additional cost for a solid and efficient maintenance setup would not be objectionable.

Finally, there are many, too many, advertisments for peripherals that fail to mention that additional controllers or interfacing boards are needed. Sometimes, when these are mentioned, no price is given. The result: one cannot determine just what it takes to get plugged in and running. Not everyone is aware of the intricacies of interconnection and interfacing and controlling. BYTE can help here by occasionally redefining some of the more-or-less standard terms, components, and abbreviations as related to how they combine to form a complete ready-to-run computer, even if it is a particular configuration—and by reminding advertisers to do the same.

If you suppose that we (number crunchers) are in a minority, just think of the many TI-59 and HP-67/97 users and their clubs. We'd like to move up into the bigger machines, too.

Bennett Sherman
90-59 56th Ave
Elmhurst NY 11373

Another Way to Computerize a Home

Steve Ciarcia's article "Computerize a Home" (January 1980 BYTE, page 28), which deals with utilizing the BSR X-10 Home Control System more fully by adding computer control, blazes a trail of interest to many. And his tracking of the amazing drop in system cost provided by the BSR technology is very graphic.

Readers of BYTE should be aware that some of the BSR command units do not include the microphone circuitry needed to accept the acoustic signals from the remote controller or Steve's interface. The command unit Model X10-014311, probably sold primarily as part of the $89 starter system, does *not* have the microphone. If you plan to implement Steve's approach, you must use the Model X10-014301.

On page 34, Steve listed and evaluated the principal interface methods available between the X-10 and the computer. I think this area might deserve further review, especially in the light of the figure and caption on page 40. The principal options are:

1) Directly synthesize the command console waveform and impress it directly onto the AC line.
2) Brute-force contact closure—attaching computer-controlled relays or switches in parallel with the existing switches of the command unit.
3) Synthesize the waveform from the ultrasonic controller and let the computer "talk" to the command console.
4) In addition, synthesize an electrical waveform and inject it into the command console, bypassing the acoustic elements.

Rather than dismiss option 1 and ignore option 4, one might want to evaluate the choices on more substantive grounds, which might include the capabilities of the experimenter. Radio Shack sold a novice-level, carrier-current intercom kit for years which dealt with

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the "hostile" 110 VAC environment Steve worries about.

I opted for option 1, for two reasons: simplicity and cost. The hardware actually requires fewer discrete parts than Steve's design and eliminates all but two integrated circuits, an opto-isolator, and a 555 timer. Even more interestingly, I used the computer, not special hardware, to generate the waveforms. For these off/on-type waveforms, the computer is in its glory. Both the actual cost of parts and the time required to implement the hardware were less than one-half of Steve's cost. Futher, I don't have to tie up or share a $50 command console.

I didn't explore option 4, but the trade-off between the cost of the acoustic transducer and opening the command unit probably favors option 3 for a transducer costs under $10.

In developing my software, I followed the structured programming approach because of two things I had in mind. I didn't want to dedicate a $1200 Apple II computer to the menial task of controlling a dozen light circuits, and I didn't want to reload and reinitialize the home-control program after each time I wanted to use the machine for something else. Because of this, my program is strictly modular and can be run in two modes: the *interrupt* mode where the home-control program runs continuously in background leaving the foreground available continuously for other uses (a very elementary time-share system), or in the *alternate* mode where home-control execution can be halted temporarily to make the machine available for other uses. Following this use, the home-control program will "play catch-up" in case any event times occurred while it was off-line.

To accomplish the above, I partitioned the modules of the program into two portions: that portion required to be in the computer's memory for program operation (the event-controlling program) and that portion required to interface with the human operator and allow changes, etc (the driver program). The event-controlling program (including the machine-language waveform-generator routine) occupies less than 3 K bytes of memory and is located at the high end of memory (with HIMEM set below it). With HIMEM set below it, the computer can be used normally; the BASIC commands RUN, LOAD, SAVE, NEW, etc can be used without erasing or corrupting the event-controlling program. The driver program is loaded when necessary to make changes.

Anyone interested in more details on this approach should send a stamped, self-addressed envelope to me at the address below. I do believe implementing this approach is one step further along the path toward an economical, utilitarian use for a home computer.

Jim Fulton
1106 Sandpiper
Corona Del Mar CA 92625

Protecting the Stack

The article by Michael McQuade in the February 1980 BYTE ("A Fast, Multibyte Binary to Binary-Coded-Decimal Conversion Routine," page 106) presents a good multiprecision binary-to-BCD routine. It presents well-structured code that also illustrates a very important subtlety; the published code will not work reliably in an interruptible operating system.

Decrementing the stack pointer is a dangerous way to maintain a "top of stack" value, because an interrupt can occur before or between the decrements and mash the contents of the stack. Pushing the data just popped is foolproof, takes 1 byte instead of 2, and one less cycle. So the two pairs of decrement-stack-pointer (DCX SP) instructions found in locations 0015 and 0016, and in locations 0023 and 0024 in listing 1 on page 110, should be changed to two single PUSH H instructions.

Thousands of programs do not maintain the integrity of the stack and so will not always work with the newer, interruptible operating systems. Unless the programmer knows what he or she is looking for, the problem can be impossible to find.

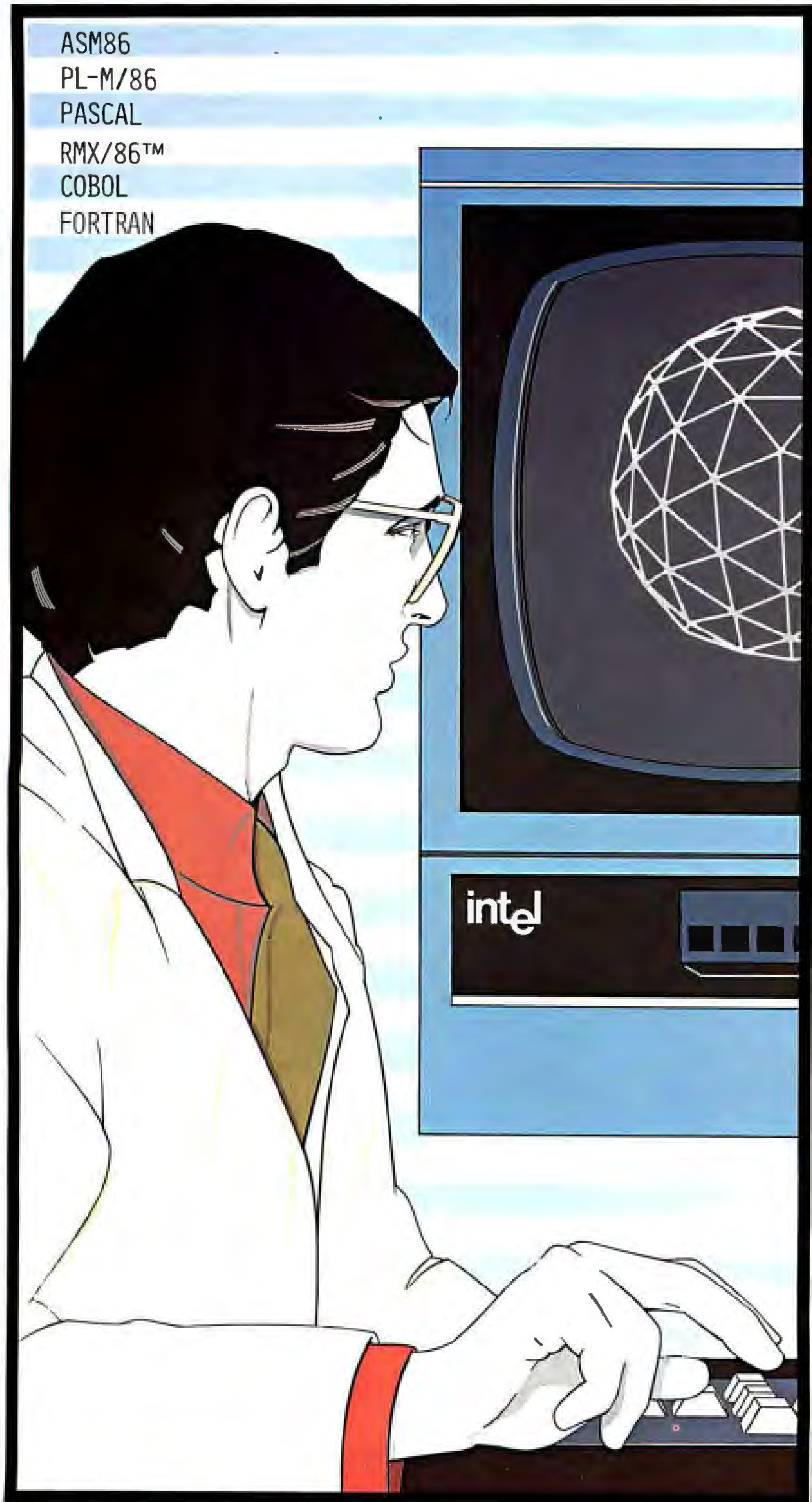
Gregg Hauser
196 Arguello Blvd
San Francisco CA 94118

A Microengine Arrives

I've bought and received a Western Digital Pascal Microengine. I had been waiting for it for a while and had enough time to fabricate the connectors necessary to interface my terminal and disk drives. So, I was prepared for the processor system when it arrived. My initial try at starting the system was both disappointing and heartening. It was disappointing because after pushing the reset button on the Microengine, I never received the greeting on the terminal that I expected. It was heartening because from the sound of the disk drive, it was likely that the processor and the disk were working correctly. I felt relief that the cabling that I'd produced and the "Shugart-compatible" drives that I'd purchased were okay.

The next day, the problem with the terminal was straightened out by a call to the terminal manufacturer. The fellow I spoke to sounded a bit chagrined when he had to admit the peculiarities of the

Tools to solve the



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software crisis.

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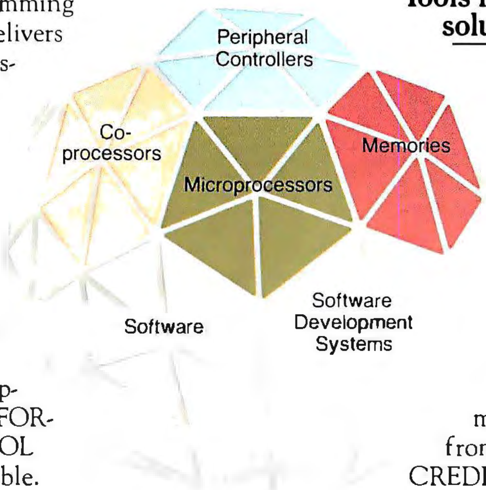

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RS-232 interface on the terminal I was trying to use. That night, after making some changes to my cabling, I had my system up and running. I was pleased that the various parts of the system all managed to "talk" to each other with what I considered to be a relatively small amount of trouble. Perhaps there really is hope for standardization.

I would like to correspond with other users of the Microengine to exchange information on the system and its use.

Shirley Kawamoto
172 Highland Ave
Winchester MA 01890

Numerical Precision in UCSD Pascal

Since the only versions of Pascal that I have seen for garden-variety computers have six-digit (maybe seven-digit) precision, checkbook balancing with Pascal is useful only for the poor, starving computer aficionados who have at most $9999.99. What about the rest of us who haven't bought a computer (and all those peripherals) yet?

Why are the popular Pascal compilers limited to six digits? I am *very* new to the computer field and particularly interested in Pascal. I teach mathematics, and Pascal seems to offer quite a bit. For some of my work, I like lots of digits as in Cromemco BASIC. I know that there's a trade-off between speed and significant digits, but only six digits?

Will the six-digit limitation always be present? If so, how can a business use Pascal, a language which many are claiming is the wave of the future?

Martin Berman
494 Forest Ave
Teaneck NJ 07666

The Pascal compilers in question all seem to be the ones included in the UCSD Pascal system. The definition of the pseudocode (ie: p-code) interpreter for the UCSD system is what determines the precision available. The six-digit precision is the maximum available when numbers are stored in a reasonable format in only 4 bytes. There are some nonstandard extensions in UCSD Pascal that give you up to some arbitrary number **N** *decimal digits precision in fixed-point format; these are called long integers. I believe the maximum value of* **N** *is thirty-six digits. This particular extension was intended for use in business programs....***CH**

Let's Hear a Good Word for Compilers

I have read with great interest the article by Mr James Lewis comparing BASIC and assembly language speeds on the TRS-80 ("TRS-80 Performance, Evaluation by Program Timing," March 1980 BYTE, page 84). The problem, as he clearly points out, is that it takes a large amount of human time to use assembly language efficiently.

The availability of FORTRAN for microcomputers now allows another, far superior, alternative. Since FORTRAN, like assembly language and unlike BASIC, is compiled, it should produce fast code. Assuming an inefficient compiler, producing code four times slower than that obtained by careful assembly-language coding, the program would still have run in under one and a half hours, over four times faster than the fastest BASIC run.

I strongly feel that anyone needing fast-executing code should always think of FORTRAN before rushing to assembly language.

Mohamed el Lozy MD
Harvard University
School of Public Health
Dept of Nutrition
665 Huntington Ave
Boston MA 02115

*The advantages of compilation are not exclusive to FORTRAN. Any high-level language, including BASIC, may be compiled. For example, a BASIC compiler is now being sold by Microsoft for Z80 systems....***RSS**

Domesticating Computers: Some Wishes Expressed

The editorial in the January 1980 BYTE on the state-of-the-art home computer omits home operations and management, although four articles in the same issue illustrate the importance of this topic. To be fair, computerized home management is next year's state of the art, and I hope that my "wishes" expressed in this letter soon become reality.

Steve Ciarcia's article on adapting the BSR X-10 system ("Computerize a Home," page 28) demonstrated that it soon will be possible to control the electrical appliances and the lighting in a home. And John H Gibson's design of a computer-controlled light dimmer is, perhaps coincidentally, a homebrew design of an X-10 light switch/dimmer. Edward Joyce showed how easy it is for a computer to dial over telephone lines. I hope that someone develops a commercial product soon, based on this idea.

Taking a different view, Theron Wierenga designed a furnace watchdog to show how a computer can monitor the outside world.

To convert these homebrew ideas into off-the-shelf computer products, both hardware and software problems must be solved. (And, as is so often the case, the hardware will be developed long before the software.)

The ideal version of the BSR X-10 would be able to *measure* the outside world, by sensors that communicate over ordinary home wiring, unlike Theron Wierenga's homebrew version. (My apologies, Theron, if I'm wrong about your design.) The sensors could be "polled," or signaled by the control unit to indicate the temperature, pressure, etc, or could initiate a signal independently (eg: in response to a change in conditions). And, of course, the sensors would be individually addressable. I doubt that BSR is working on such sensors because they would be of little use for a manually controlled system, and they have given no indication that they are working on a computerized version of the X-10.

The ideal computer will also require a programmable real-time clock. Also, if we are serious about energy conservation, we might want to shut down part or even all of the computer for a few hours of the day. Perhaps this on/off capability can be made part of the programmable timer.

Even if all this hardware were available for our off-the-shelf computer, it would make little sense to devote a machine with considerable capacity to just one application program. Ideally, we would like to monitor and control several outside systems while still using the machine for game playing, word processing, or whatever. This requirement implies a multiprogramming operating system, a feature generally confined today to large computer systems. We would also like the real-time clock to be able to interrupt all other programs at regular intervals and initiate a polling program to sample the outside systems. Alternatively, the operating system gives every program in the system, including the polling program, a chance to execute at least once a second. So our operating system could include "time slicing." Finally, since we can never be certain of the starting address in memory of a program in a multiprogramming system, all software should be relocatable.

I think that the software requirements will prove challenging to software homebrewers, of which there aren't enough.

Philip Burton
3333 Cowper St
Palo Alto CA 94306

A Problem with Radio-Frequency Interference

We have a Nano computer and an FM radio receiver and they don't get along! When the computer is operational, it will function as a process controller for our solar-heating system. It is connected to sixteen low-voltage heat sensors located throughout the house. This wiring was positioned as the house was built and is therefore unmovable. All the wires terminate in our "computer room," which also houses the FM receiver. None of the sensor wires are closer than two feet to the FM antenna or its (coaxial) cable.

When the Nano computer is on, we get whistling, buzzing, and hissing on one station (90.9 MHz), which is 75 miles away. Putting the receiver in monophonic mode, as opposed to stereophonic, eliminates the interference, as does moving the Nano (less sensor wires) into another room. Because none of the closer stations are affected, it is clear that the strength of the FM signal is a factor. Unplugging the sensor wires from the Nano reduces the interference significantly, but not completely.

We have tried (at the suggestion of several acquaintances who are electronics/computer-engineer people) a low-frequency filter on the FM antenna, a power-line filter, switching plugs and

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circuits, and grounding a wire screen and putting it between the computer and receiver. The maximum separation possible between the two is about 5 feet. None of these things have had any noticeable effect. Oddly enough, sometimes the interference all but disappears for no apparent reason.

It is imperative that this interference be permanently eliminated because we cannot relocate any of the equipment. We would appreciate any help BYTE readers can give us.

Mr and Mrs J M Johnston
1116 E Deep Run Rd
Westminster MD 21157

A North Star Alternative

I liked Carl Helmers' January 1980 editorial ("The Era of Off-the-Shelf Personal Computers Has Arrived," page 6), but I feel that it would have been better and more dramatic if he had included more examples and less emphasis on the Apple II Pascal system. I went through the same issue of BYTE and built the following system on paper:

Horizon 2-Q with 32 K user memory 720 K bytes disk storage two serial input/output ports one parallel port North Star disk-operating system, monitor, and North Star BASIC	$2560
North Star 32 K-byte memory card	$ 520
North Star UCSD Pascal system	$ 78
Anadex DP-8000 printer	$ 795
Interface cables	$ 70
CP/M operating system in North Star format	$ 145
CBASIC-2 for North Star	$ 110
MicroSoft MACRO-80, COBOL-80, and FORTRAN-80	$1025
Freight	$ 70
TOTAL	$5373

The sources for these items include Avionics Enterprises (AEI), American Square Computer, Logon Incorporated, and LifeBoat Associates. I did not include a modem because I did not see the Hayes S-100 modem advertised this month. If I remember correctly, it sells for about $400, bringing to $5773 the total price of my paper system.

So, for less than $6000 I have synthesized a hypothetical example to complement Mr Helmers' Apple II example. The Horizon 2 example will execute UCSD Pascal approximately twice as fast as the Apple II, and with the above additions provides FORTRAN, COBOL, two BASICs, two assemblers, and compatibility with all of the excellent software designed for use with CP/M. In addition, the Anadex printer will produce listings and output at twice the speed of the Integral Data 440 when the former is used in the bidirectional mode.

I provide this example (I have both an Apple and a North Star) to point out that some alternatives exist.

Robert Rennard
2281 Cobble Stone Ct
Dayton OH 45431

More (Transcendental) Pi in the Sky

Regarding the letter "Pi in the Sky" (February 1980 BYTE, page 16), I have found Mr Sprenkle's approximation to π of 1/(113/355) to be useful for the old mechanical "four-bangers" as well as the modern four-function calculators, but its accuracy generally leaves much to be desired in modern computers. My preference is the function:

PI = 4*ATN(1)

for all scientific work. For whether you have six- or sixteen-decimal digit capability, this value of π will be accurate to the full capacity of your machine, and it is no more difficult to remember than 1/(113/355).

Rex H Shudde
27105 Arriba Way
Carmel CA 93923

*Alas, this is not always the case. Several years ago, I was obtaining inaccurate trigonometric calculations from some FORTRAN programs that used double-precision variables. The FORTRAN compiler was the product of a prominent minicomputer manufacturer, which shall remain anonymous. After much attempted debugging, the minicomputer firm revealed that the writers of the compiler had put in an incorrect value for π, and therefore all of the double-precision trigonometric functions were inherently inaccurate. Sigh....*RSS

Information Wanted

I would to like contact anyone who has determined the nature of the incompatibility between the Cromemco ZPU board and the IMSAI VIO-C video interface board—when both are installed in an IMSAI I-8080 mainframe.

Also, I'm trying to locate a firm or a person who really knows how to repair an IMSAI DIO disk-interface board.

Jack Williams
902 Anderson Dr
Fredericksburg VA 22401

Circle 14 on inquiry card. →

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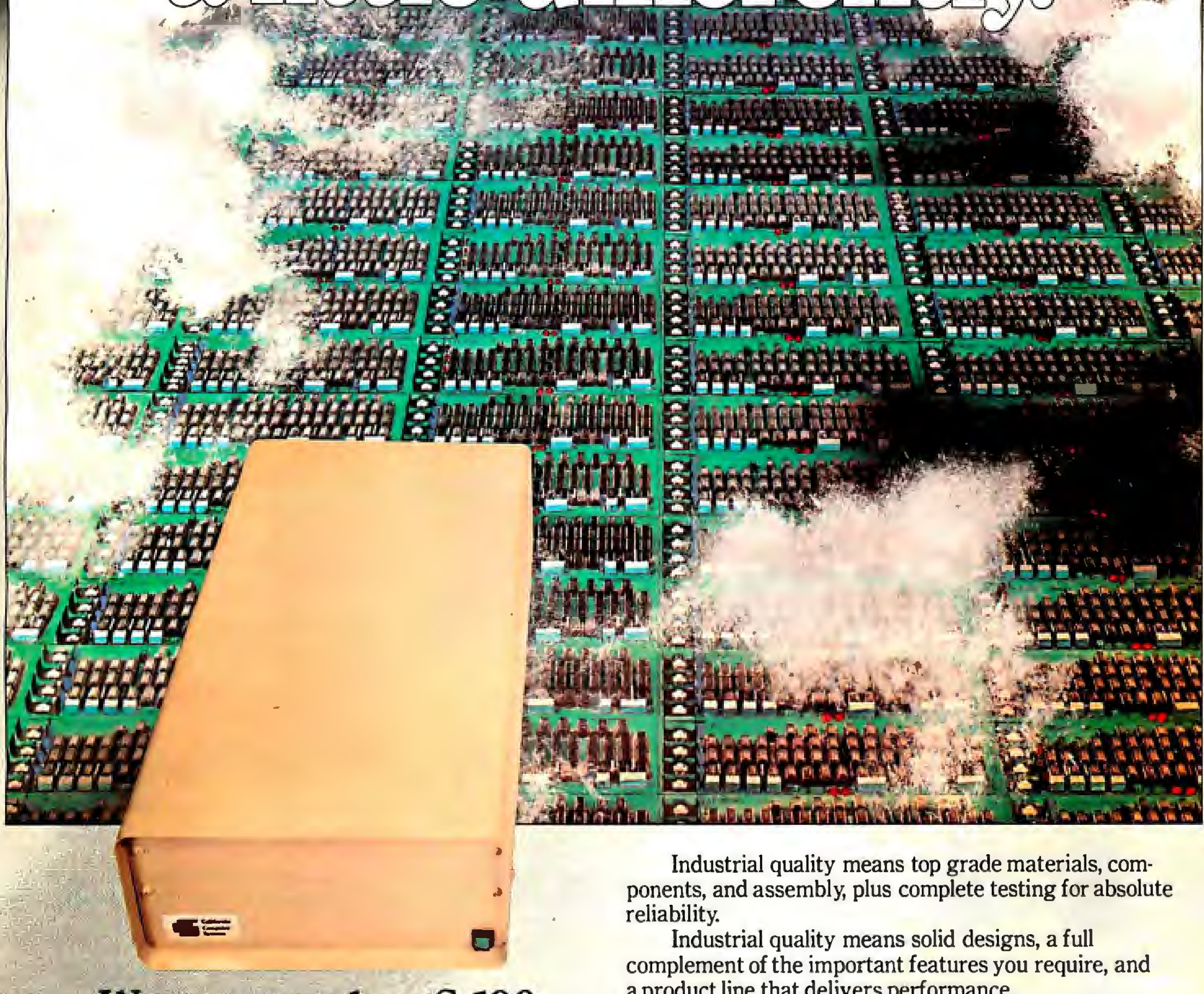

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Recursive Decisions?

In his article "What Computers Cannot Do" (January 1980 BYTE, page 100), T G Lewis asserts: "If the DECIDE program *itself* is put into GR, a paradox is created for GR." Following this he shows that *if* a particular outcome (HALT NOT FOUND) results, this would lead to a contradiction and so DECIDE could not exist. His hypotheses 7 thru 10 seem to hinge on the nonexistence of a DECIDE program, which in turn depends on HALT NOT FOUND occurring on input of DECIDE into DECIDE. However, HALT NOT FOUND was only one of two possible outcomes. Finally, either I missed it or Mr Lewis did not state why HALT NOT FOUND *must* result from feeding DECIDE into DECIDE.

John S Wallingford
Chairman, Dept of Physical Science
Pembroke State University
Pembroke NC 28372

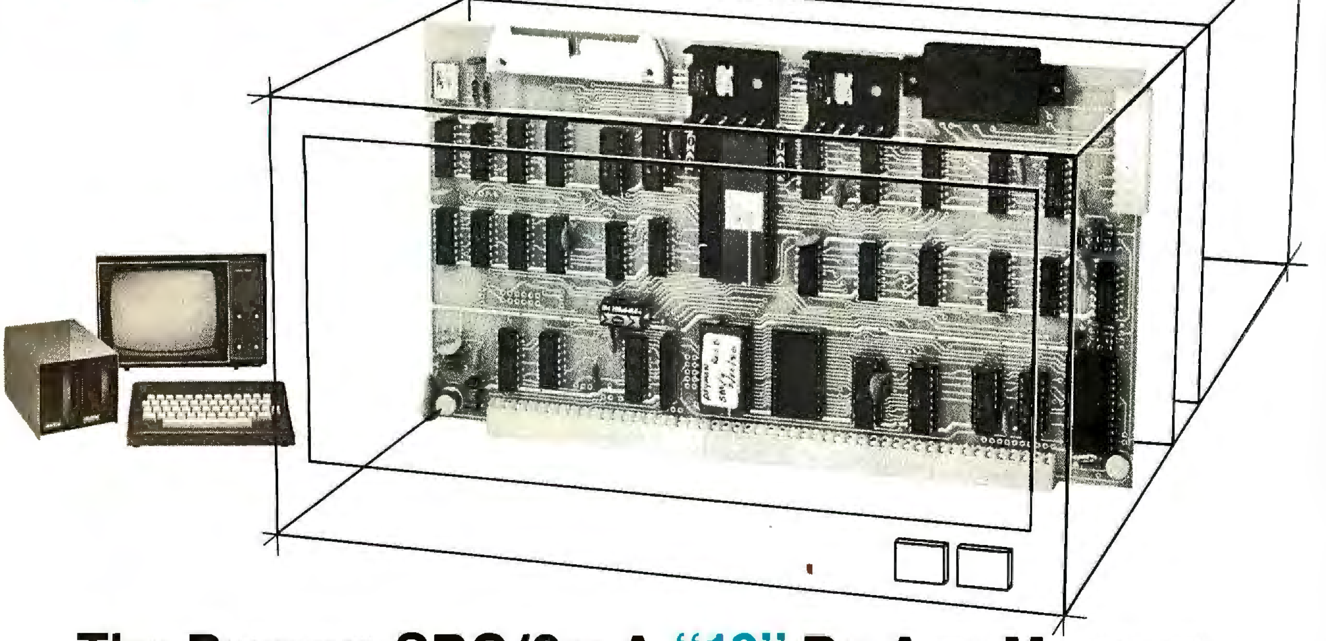
Undocumented Feature of Apple Writer

Apple Computer Company has recently introduced a text editor named Apple Writer, which I developed. Apple Writer has an undocumented feature that may save the user some time, money, and difficulty. The hidden feature is a software serial interface that connects to a printer by way of the Apple II game-paddle input/output (I/O) socket. To enable this serial interface, the user types "SERIAL" from the Apple Writer print menu. The program will then display the hardware protocol and available data rates.

At present, this interface is one of a very few ways to use a Qume printer (among others) with the Apple II. Because only three wires are required, cost and complexity are low. However, some technical skill is required to make the electrical connections, and electrical compatibility between the printer and the Apple II must be determined. If these precautions are not taken, damage to the Apple II and/or the printer may result. It is for these reasons that Apple Computer chose not to document the feature.

I have used the serial interface on two printers (IDS and Qume) with no problems. It appears that most serial-interface-equipped printers will accept the signals available from the Apple II.

Paul Lutus
291 N Gold Canyon Dr
Kerby OR 97531 ■



An Answer/Originate Modem

Ronald G Parsons
9001 Laurel Grove Dr
Austin TX 78758

One of the few and nearly universal methods of exchanging data between diverse microprocessors is by means of data transmission over switched telephone facilities. Most other means of data exchange such as floppy disk or cassette tape are specific to one or a few microcomputers. But data transmission over phone lines is nearly independent of the microprocessors involved and the method or speed of the mass data storage used by either processor.

To transmit data at reasonable speeds over a telephone line, a *modem* is used to convert digital signals to an analog form for transmission over the telephone network. "Modem" is a hybrid of the words modulator and demodulator. A modem must be used because the telephone network was designed for analog voice transmission and not for digital data. The telephone network has an audio bandwidth of approximately 3000 Hz, so the modem must condition the signals to fit within this bandwidth.

Since communication usually involves data transmission in both directions, a convention has been established so that two sets of data traveling in opposite directions do not interfere with each other. The Bell 103 type of modem uses designated audio frequencies for binary 0 and 1. One of the pair of communicating entities is arbitrarily designated as the originating end and the other the answering end. As the words imply, the originating end usually originates the telephone call and the answering end usually answers, but this is not necessary. All that is necessary is for one of the pair to agree to call itself the answerer and the other the originator.

The originating end transmits a binary 0 (sometimes called a space) as a tone of 1070 Hz and a binary 1 (sometimes called a mark) as a tone of 1270 Hz. The originating end also *receives* spaces and marks as tones of 2025 Hz and 2225 Hz, respectively. The answering end has the transmit and receive frequencies interchanged. The Bell 103 modem translates serial data from voltage levels to these audio tones capable of being transmitted over standard telephone lines at a data rate from 0 to 300 bps.

> The telephone network was designed for analog voice transmission, not digital data.

A data bit is usually translated first by a terminal or microcomputer to standard voltage levels defined by an Electronic Industries Association (EIA) standard known as RS-232C. This standard defines a space as a voltage level between +5 V and +15 V and a mark as a voltage level between −5 V and −15 V. Voltages between −5 V and +5 V have undefined meaning. These signals are capable of being transmitted over wire cable for distances of several hundred feet at speeds up to several thousand bits per second.

The modem described in this article uses RS-232C levels between the processor or terminal and the telephone line; it connects to the telephone line through a device called a data access arrangement (DAA). This device has two common types: the CBS data coupler, which uses RS-232C levels to interface with the modem; and the simpler CBT data coupler, which uses contact closures (ie: switches or relays) for the modem interface. The CBT type is used in this design for simplicity. Motorola's *Application Note AN-747* entitled "Low-Speed-Modem System Design using the MC6860" discusses the interface to either coupler.

The most complicated and troublesome parts of a modem are usually the filters used to separate and purify the transmitted and received audio tones. It is not uncommon for filters for the transmit and receive frequencies each to contain several operational amplifiers and many precision resistors and capacitors. The filters used in this design, however, are available as "miniModem" building blocks from Cermetek Microelectronics, 660 National Ave, Mountain View CA 94043. They require no adjustments and few external components.

Two filters are used. One, the CH1262, is a switchable, dual-channel, transmit filter and line hybrid. The center frequency of the filter is

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The compact unit communicates via its acoustic coupler over standard telephone lines with any computer system, using standard RS 232 telecommunications (used on most mainframes). No special programming is needed.

To operate, just dial your computer or computer operator. Place your telephone handset into the acoustic coupler and you're ready to go! Just key in a line (up to 80 characters), review on the 16-character display via scroll keys, then transmit. The speed of computer response is easily set for your own viewing pace.

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	INS., SHIPPING And Handling Charge	$3.50	______
TOTAL	(Mass. Residents add 5% Sales tax.)		______

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chosen to be 1170 Hz or 2125 Hz by changing the DC voltage on the channel-select pins. The other, the CH1267, is a switchable, dual-channel, receive filter and limiter. It is necessary for us to be able to switch the center frequencies of the filters so the modem can be used as an originate or an answer modem.

The functions of modulation, demodulation, and control are performed by a Motorola MC6860 metal-oxide semiconductor/large-scale integration (MOS/LSI) modem chip. After conversion to transistor-transistor logic (TTL) levels, the modulator section of the 6860 converts serial digital data into analog frequencies. It does this by digitally synthesizing a sine wave at one of the space and mark frequencies. This signal is filtered and amplified by the transmit filter. The demodulator section of the 6860 detects the presence of a mark or space frequency and presents a digital 0 or 1 output to the terminal or computer. The receive-signal input to the 6860 must be a 50% duty-cycle, TTL signal that is filtered and limited (ie: amplified and clipped).

Several supervisory control functions are provided by the 6860. The 6860 places the modem into answer mode (if a ring indication is detected) or into originate mode (if a handset-off-hook condition is detected). If the data terminal is ready, the detection of the ring creates an answer phone signal to the DAA. A mode-signal output from the 6860 is used to control the switchable filters to ensure that the correct set of signal pairs are used. A clear-to-send (CTS) signal is also created to indicate to the terminal or computer the establishment of a communication link.

Constructing the Modem

Figure 1 shows the schematic diagram for the modem. The signals from the terminal or computer to and from the modem are first converted from RS-232C levels to TTL levels by the 1488 and 1489A integrated circuits. The request-to-send (RTS) signal is not used by the 6860, but is used by the support circuitry to control pulse dialing and setting the answer/originate mode. The 1458 dual operational amplifier is used to convert the TTL-level mode signal, as possibly modified by the test/normal switch, to a +12 V or −12 V signal sent to switch the filters between originate and answer. The 301A operational amplifier is used to limit the received signal. The 3.9 V zener diode causes the output of the operational amplifier to be TTL compatible and the TTL gate helps square up the limited signal. The 200 k-ohm variable resistor on the CH1262 is used to set the transmit level to 0 dBm (ie: 1 mW at 600 ohms or 0.7 V RMS).

If the modem is powered up with the ready-to-send line active (ie: at +5 V to +12 V), the modem is in originate mode and the answer-phone signal from the 6860 commands the DAA telephone interface to take the phone line off hook. The telephone may then be dialed by pulsing the ready-to-send line off and on under software control. An assembly-language program for an 8080 to do automatic dialing is shown in listing 1.

If the modem is powered up and the ready-to-send line is off (ie: −5 V to −12 V), the modem will wait for a ring indication from the DAA

Text continued on page 34

Circle 18 on inquiry card. →

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Number	Type	+5 V	GND	−12 V	+12 V
IC1	1488		7	1	14
IC2	1489A	14	7		
IC3	6860	12	1		
IC4	7407	14	7		
IC5	LM301			4	7
IC6	1458			4	8
IC7	7486	14	7		
IC8	7404	14	7		
IC9	7400	14	7		
IC10	CH1262		5	13	12
IC11	CH1267		18	9	7

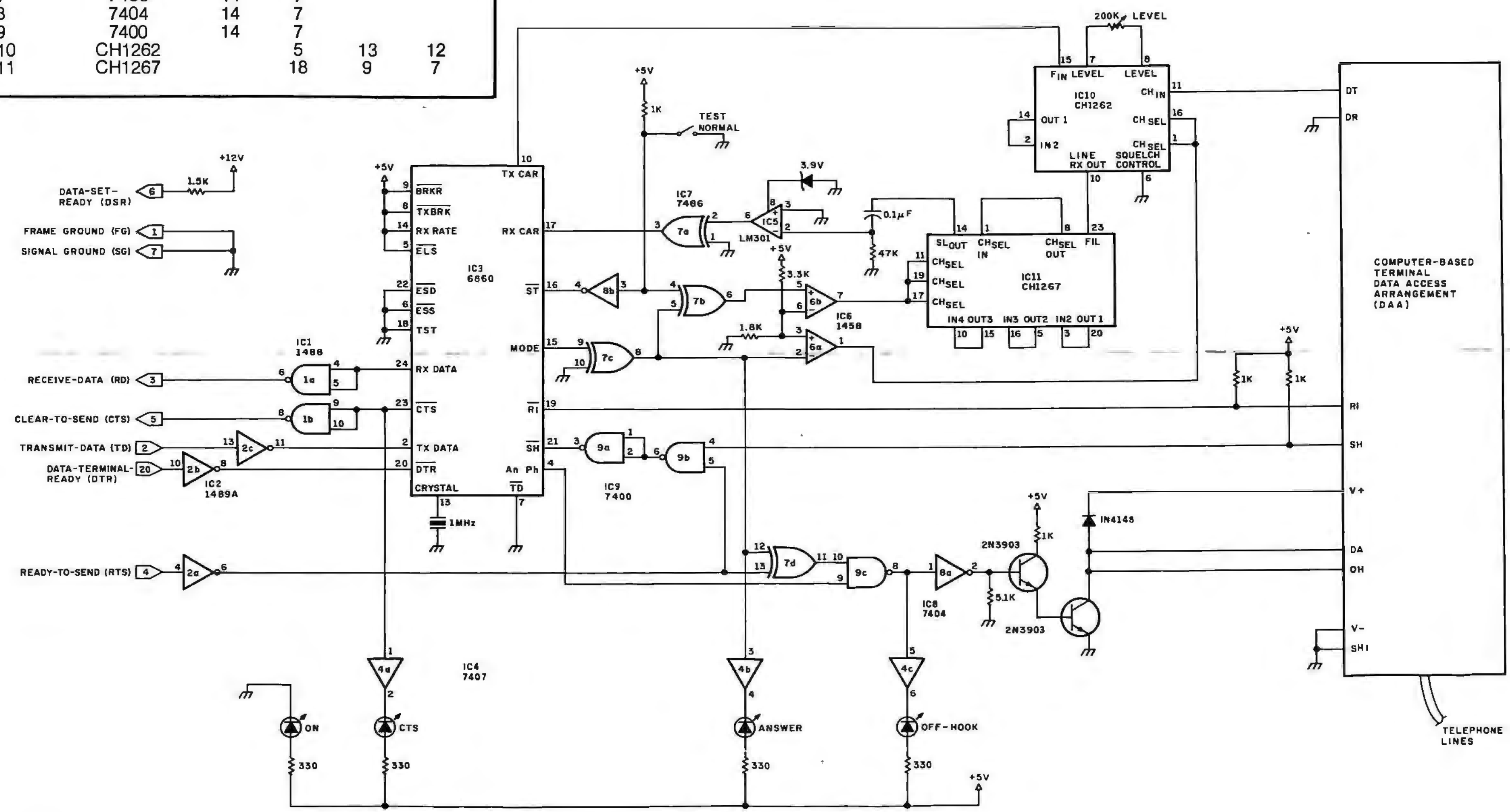

Figure 1: *Schematic diagram of the answer/ originate modem. IC1 and IC2 convert the modem RS-232C signal to a digital transistor-transistor logic (TTL) level and back. IC3 is the Motorola 6860 modem integrated circuit. IC10 and IC11 are the transmit and receive filters, respectively, used to interface the modem and the telephone line.*

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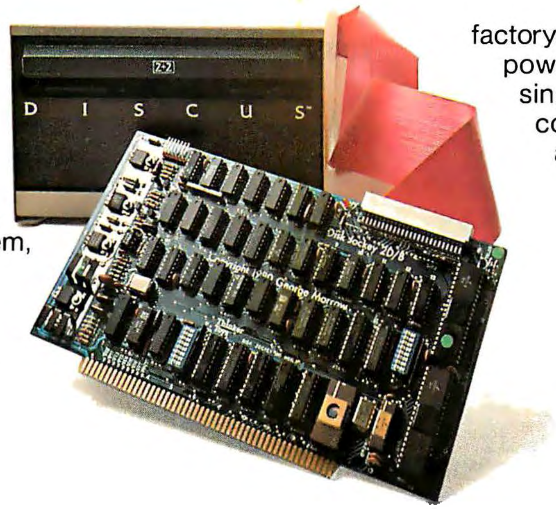

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Circle 19 on inquiry card.

Listing 1: *DIAL routine to perform automatic dialing by the computer. This listing, which is designed to run as part of a CP/M-based 8080 or Z80 system, performs automatic dialing of a telephone number with the command DIAL <phone number>. If a modem answers, this program causes its computer to act as a "dumb" terminal for the computer connected to the answering modem.*

```
                    ; Auto-dial program
                    ; Syntax:  DIAL <phone-number>[:<signon-character>]
                    ;    <signon-character> sent when CTS is asserted.
                    ;
0005 =              BDOS     EQU     5       ;BDOS entry point
E00C =              TERM     EQU     0E00CH  ;Terminal simulation subroutine
0020 =              SCTS     EQU     32      ;serial CTS
0010 =              SRTS     EQU     16      ;serial RTS
00F8 =              SERST    EQU     0F8H    ;serial status port
                    ;
0100                         ORG     100H
                    ;
0100 31FFCB         START:   LXI     SP,0CBFFH
0103 CDA101                  CALL    OFFHOOK
0106 0E64                    MVI     C,100   ;wait 2 seconds for dialtone
0108 CD5C01                  CALL    DELAY
010B 0E64                    MVI     C,100
010D CD5C01                  CALL    DELAY
0110 218100                  LXI     H,81H   ;use default buffer area
0113 7E             NEXT:    MOV     A,M     ;get digit
0114 23                      INX     H
0115 B7                      ORA     A
0116 CA3301                  JZ      TERMINAL
0119 FE3A                    CPI     ':'     ;signon-character?
011B CA2901                  JZ      GETSIGNON
011E F5                      PUSH    PSW
011F CD5301                  CALL    SOUT    ;echo number
0122 F1                      POP     PSW
0123 CD6A01                  CALL    DIGIT
0126 C31301                  JMP     NEXT
                    ;
                    GETSIGNON:
0129 7E                      MOV     A,M
012A B7                      ORA     A
012B C23001                  JNZ     NOTCR
012E 3E0D                    MVI     A,13    ;CR if character zero
                    NOTCR:
0130 32AC01                  STA     SIGNON
                    ;
                    TERMINAL:
0133 DBF8                    IN      SERST
0135 E620                    ANI     SCTS
0137 C23301                  JNZ     TERMINAL        ;wait for clear-to-send
013A CD4A01                  CALL    SETIO   ;set I/O parameters for serial port
013D 3AAC01                  LDA     SIGNON
0140 B7                      ORA     A
0141 C45301                  CNZ     SOUT
0144 CD0CE0         TRANS:   CALL    TERM
0147 C34401                  JMP     TRANS
                    ;
014A 3E01           SETIO:   MVI     A,1     ;set Sol/SOLOS I/O parameters serial
C806 =              IPORT:   EQU     0C806H
C807 =              OPORT:   EQU     0C807H
014C 3206C8                  STA     IPORT
014F 3207C8                  STA     OPORT
0152 C9                      RET
```

Listing 1 continued on page 32

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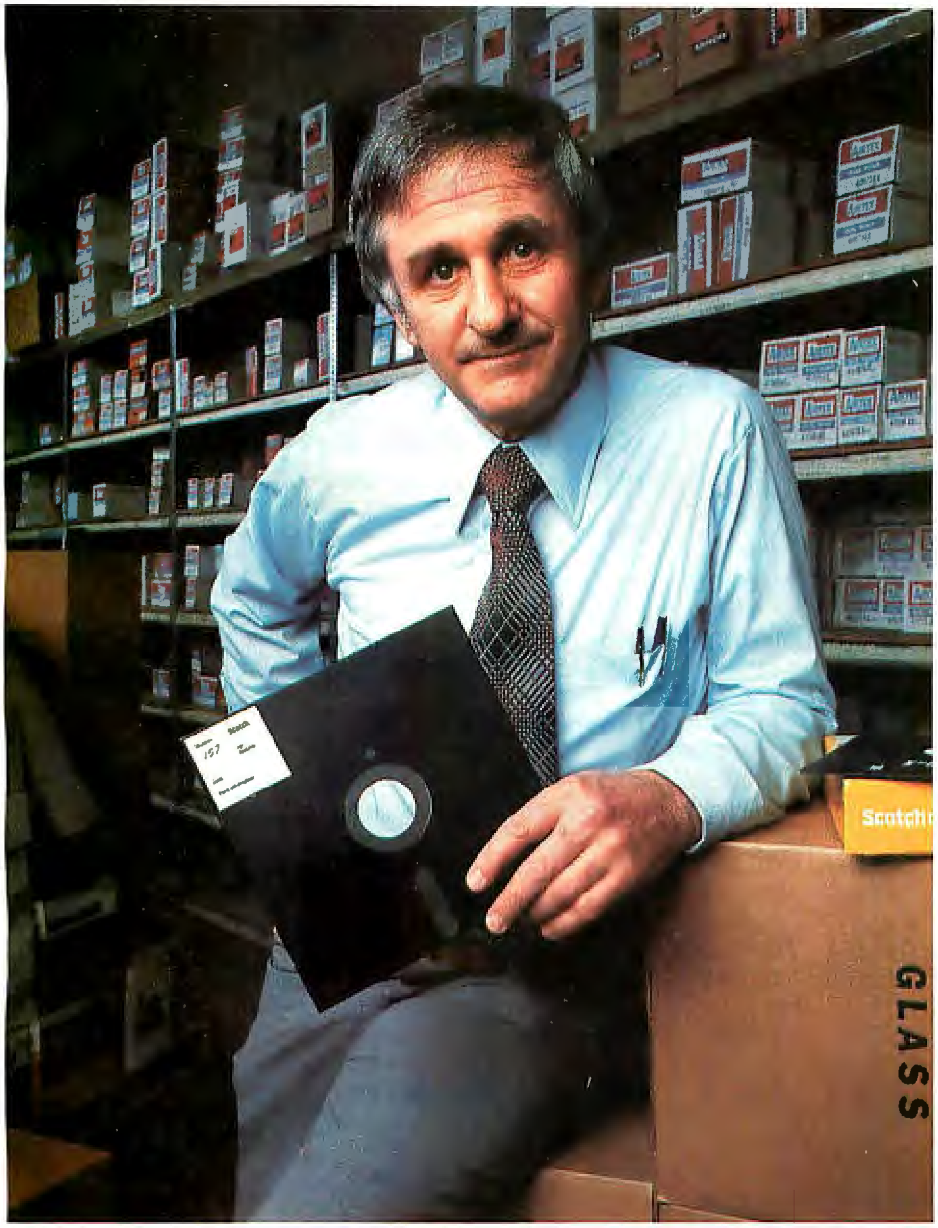

Don Stone, President,
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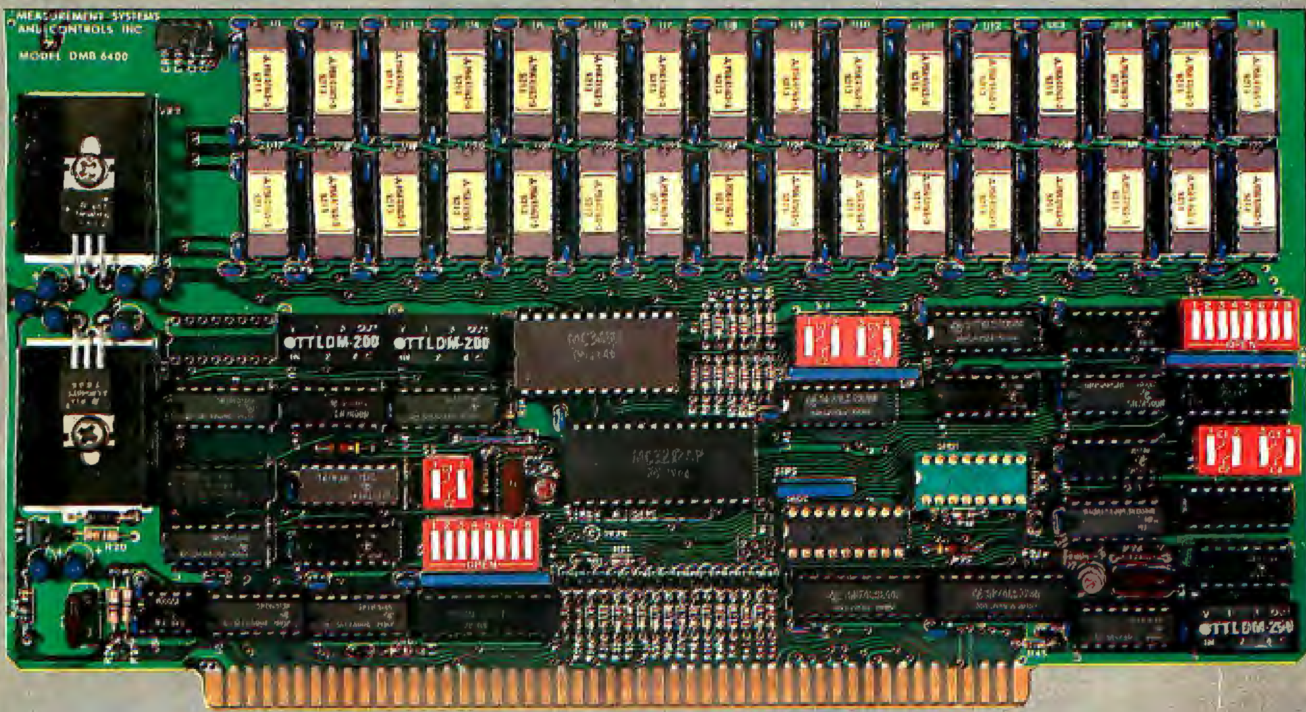
3M

Circle 20 on inquiry card.

Listing 1 continued:

```
                 ;
0153 5F          SOUT:   MOV     E,A        ;write character to console
0154 0E02                MVI     C,2
0156 E5                  PUSH    H
0157 CD0500              CALL    BDOS
015A E1                  POP     H
015B C9                  RET
                 ;
015C 115403      DELAY:  LXI     D,852      ; .01 times (C) seconds
                 ;Adjust DE for different clock periods
015F 0D                  DCR     C
0160 F8                  RM
0161 1B          DELA1:  DCX     D
0162 7A                  MOV     A,D
0163 B3                  ORA     E
0164 C26101              JNZ     DELA1
0167 C35C01              JMP     DELAY
                 ;
016A FE2D        DIGIT:  CPI     '-'        ;Call with ASCII digit in A
016C C8                  RZ                 ;skip '-'
016D FE20                CPI     ' '
016F C8                  RZ                 ;skip blanks
0170 FE30                CPI     '0'
0172 DAA601              JC      DIGERR
0175 FE3A                CPI     '9'+1
0177 D2A601              JNC     DIGERR     ;not an ASCII digit
017A E60F                ANI     0FH        ;subtract ASCII Bias
017C C28101              JNZ     NOTZERO
017F C60A                ADI     10         ;zero is ten
                 NOTZERO:
0181 47                  MOV     B,A
                 PULSE:  ;each digit is onhook for 60 ms and offhook for 40 ms
0182 0E06                MVI     C,6
0184 CD9C01              CALL    ONHOOK
0187 CD5C01              CALL    DELAY
018A 0E04                MVI     C,4
018C CDA101              CALL    OFFHOOK
018F CD5C01              CALL    DELAY
0192 05                  DCR     B
0193 C28201              JNZ     PULSE
0196 0E64                MVI     C,100
0198 CD5C01              CALL    DELAY      ;inter-digit delay
019B C9                  RET
                 ;
019C 3E00        ONHOOK: MVI     A,0        ;put line on-hook
019E D3F8                OUT     SERST
01A0 C9                  RET
                 ;
                 OFFHOOK:                   ;take line off-hook
01A1 3E10                MVI     A,SRTS
01A3 D3F8                OUT     SERST
01A5 C9                  RET
                 ;
                 DIGERR:         ;not a digit - go on-hook and reboot
01A6 CD9C01              CALL    ONHOOK
01A9 C30000              JMP     0          ;boot
                 ;
01AC 00          SIGNON  DB      0          ;store for sign-on character
```



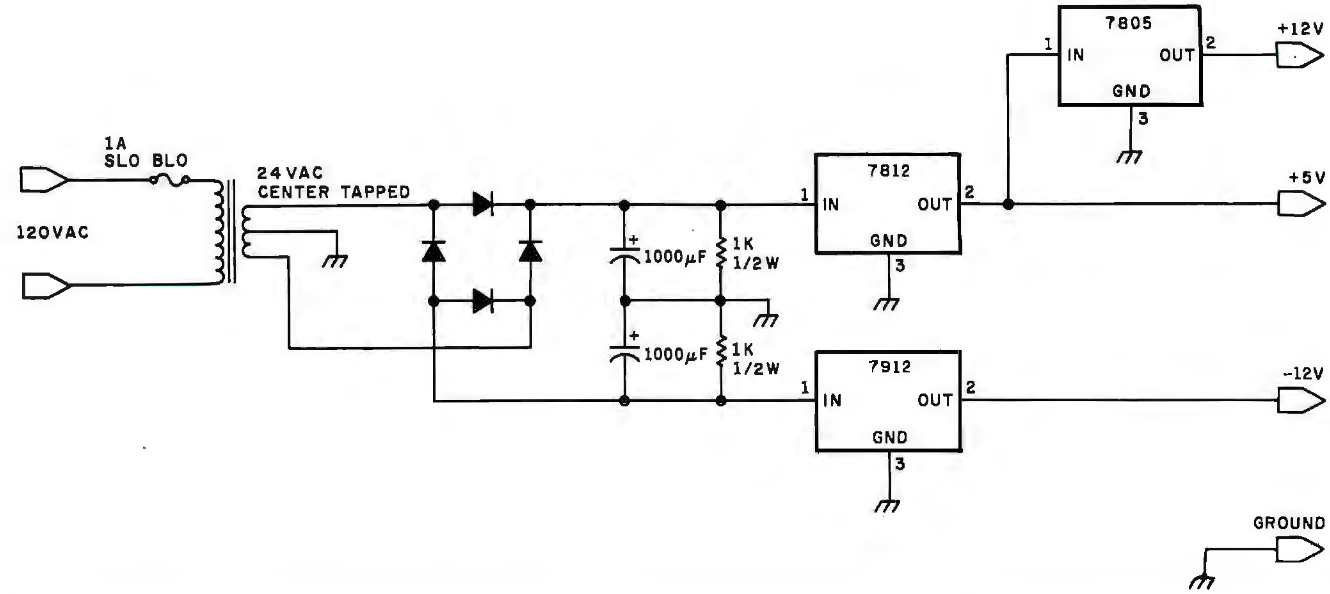


Figure 2: *Schematic diagram of the optional power supply. This regulated power supply can be eliminated if the required voltages are available from a nearby computer or terminal.*

Text continued from page 26:
telephone interface. On receipt of the ring, the 6860 will bring the answer-phone line high and begin sending the transmit carrier, which is at 2225 Hz. If the modem on the other end of the line responds with its carrier, which is at 1270 Hz, the 6860 will turn clear-to-send on about a half second later. The terminal or computer can detect this and initiate whatever procedure is necessary to communicate with the originator.

Figure 1 shows four light-emitting diodes (LEDs) that can be used by the operator to monitor the operation of the modem. The functions displayed are power-on, clear-to-send, mode (with the LED on in answer mode), and off-hook.

A power-supply schematic is shown in figure 2; it supplies +5 V, +12 V, and −12 V, regulated. These voltages may be obtained from the terminal or computer if they are available. I chose to make the modem an independent device: it was wire-wrapped on a small perforated board and enclosed in a cabinet.

Modem Software

Listing 1 shows a CP/M-based, assembly-language program for an 8080 processor to perform automatic dialing to an answer modem and to initiate communication. The CP/M syntax of the program is:

DIAL <phone number>

or

DIAL <phone number>:
<logon character>

The phone number may contain blanks and hyphens that are ignored. If an invalid character is found in the phone number, the program hangs up the telephone and rebootstraps

Text continued on page 40

Listing 2: *Remote-access computer routine. This is the software needed by the computer that is connected to the answering modem of figure 1. This routine allows its computer to be controlled by a remote terminal, with the connections made by two modems and a telephone line. This routine runs on a CP/M system.*

```
                 ; Remote Access to CP/M
                 ;   using a Sol and SOLOS
                 ;
BFE0 =           IOCODE  EQU    0BFE0H  ;Temporary storage for I/O code
C01C =           AOUT    EQU    0C01CH  ;Write to logical output unit (A)
C022 =           AINP    EQU    0C022H  ;Read logical input unit (A)
C800 =           UIPRT   EQU    0C800H  ;User defined input routine address
C802 =           UOPRT   EQU    0C802H  ;User defined output routine address
C806 =           IPORT   EQU    0C806H  ;Standard input unit number
C807 =           OPORT   EQU    0C807H  ;Standard output unit number
00F8 =           SERST   EQU    0F8H    ;Serial status port
00D4 =           DCCMD   EQU    0D4H    ;Tarbell command port
                 ;
0100                     ORG    100H
                 ;
0100 31FFCB      START   LXI    SP,0CBFFH
0103 3E00                MVI    A,0
0105 D3F8                OUT    SERST   ;set modem for answer - RTS off
0107 3E06                MVI    A,6     ;turn disk motor off
0109 D3D4                OUT    DCCMD
010B DBF8        NOTCTS  IN     SERST   ;CTS?
010D E620                ANI    20H     ;wait for modem to answer and get response
010F C20B01              JNZ    NOTCTS  ;no
0112 3E05                MVI    A,5     ;turn disk motor on
0114 D3D4                OUT    DCCMD
0116 CD4001              CALL   DELAY   ;wait one second
0119 3E03                MVI    A,3     ;set up SOLOS for
                                        ;  user defined I/O routines
011B 3206C8              STA    IPORT
011E 3207C8              STA    OPORT
0121 21E0BF              LXI    H,IOCODE        ;store user defined I/O addresses
0124 2202C8              SHLD   UOPRT
0127 21EBBF              LXI    H,IOCODE+XIPRT-XOPRT
012A 2200C8              SHLD   UIPRT
                 ; Transfer I/O code to IOCODE
012D 21E0BF              LXI    H,IOCODE
0130 0E11                MVI    C,XEND-XOPRT
0132 114A01              LXI    D,XOPRT
                 TRANLOOP:
0135 1A                  LDAX   D
0136 77                  MOV    M,A
0137 0D                  DCR    C
0138 23                  INX    H
0139 13                  INX    D
013A C23501              JNZ    TRANLOOP
013D C30000              JMP    0       ;boot
                 ;
0140 =           DELAY   EQU    $
0140 110000              LXI    D,0
0143 1B          DLOP1   DCX    D
0144 7A                  MOV    A,D
0145 B3                  ORA    E
0146 C24301              JNZ    DLOP1
0149 C9                  RET
                 ;
                 ;Relocatable user defined I/O routines
                 ;
                 ;Output routine - output to serial and screen
014A 3E01        XOPRT   MVI    A,1
014C CD1CC0              CALL   AOUT    ;put on serial
014F 3E00                MVI    A,0
```

Listing 2 continued on page 38

Listing 2 continued:

```
0151 CD1CC0               CALL    AOUT     ;put on screen
0154 C9                   RET
                 ;
                 ;Input routine - input from serial port
0155 3E01        XIPRT    MVI     A,1
0157 CD22C0               CALL    AINP     ;get serial
015A C9                   RET
                 ;
015B 00          XEND:    DB      0
                 ;
```

Listing 3: *Remote-user routine. This routine allows a remote user to communicate with the operator of the host computer tied to the answering modem.*

```
                 ; Write to operator
                 ;Syntax:  WTO <message text>
0100                      ORG     100H
0100 210000               LXI     H,0
0103 2B          BELOOP:  DCX     H
0104 7D                   MOV     A,L
0105 B4                   ORA     H
0106 D3FC                 OUT     0FCH     ;sound alarm port
0108 C20301               JNZ     BELOOP
010B C9                   RET              ;return to CP/M
                 ;
```

Listing 4: *Remote-user routine. This routine allows a remote user to communicate with the host computer's operator; it also allows the operator to send a reply to the remote terminal.*

```
                 ; Write to operator with reply
                 ;Syntax:  WTOR <message text>
                 ;
0100                      ORG     100H
                 ;
C019 =           SOUT     EQU     0C019H
C01C =           AOUT     EQU     0C01CH
C022 =           AINP     EQU     0C022H
                 ;
0100 210000      START:   LXI     H,0
                 BELLOOP:
0103 2B                   DCX     H
0104 7D                   MOV     A,L
0105 B4                   ORA     H
0106 D3FC                 OUT     0FCH     ;sound alarm port
0108 C20301               JNZ     BELLOOP
                 REPLOOP:
010B 3E00                 MVI     A,0
010D CD22C0               CALL    AINP     ;get keyboard character
0110 CA0B01               JZ      REPLOOP
0113 FE0D                 CPI     13       ;done?
0115 C8                   RZ               ;return to CP/M
0116 47                   MOV     B,A
0117 CD19C0               CALL    SOUT     ;send to standard output port
                                           ;  may be user defined port
                                           ;  such as serial and display
011A C30B01               JMP     REPLOOP
                 ;
```

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Text continued from page 34:

CP/M. If a colon follows the phone number, the next character is sent in ASCII form to the answering modem after the clear-to-send signal is received from the answering modem. Such a logon character is often required by timesharing services. After communication is established and any logon character is sent, the program calls a terminal-simulation subroutine (TERM) that will listen for a character which was the serial line, display it on the CP/M display, and send a character of input to the CP/M console. The serial status port and bit configuration is that of a Processor Technology Sol. The subroutine SETIO must configure CP/M to send output to the serial port and receive input from the serial port. The subroutine shown is also for the Sol.

Listing 2 shows a program that will configure the operating system to be remotely accessed. The program, after starting, will wait for the telephone to ring and the modem to answer. If the caller is an originating modem, the program will configure CP/M to use the terminal on the other end of the telephone line as the display console. All data output to the remote terminal and input to CP/M from the remote terminal is echoed to the local display.

Listings 3 and 4 show small programs that can be used by the remote user to communicate with the local operator. The programs can be used only to send a message or to send a message and get a reply from the local operator. These programs are thus named Write To Operator (WTO) and Write To Operator and Reply (WTOR).

Conclusion

Once the modem is constructed and tested, a protocol is still needed to establish two-way communications between processors. Commercial timesharing services set this protocol for their customers. Personal computer users do not have a standard file and message exchange protocol, but groups such as PCNET in the San Francisco Bay area (280 Polaris Ave, Mountain View CA 94303) are working on the problem. The PCNET protocol is based on the use of modems similar to the type described in this article.■

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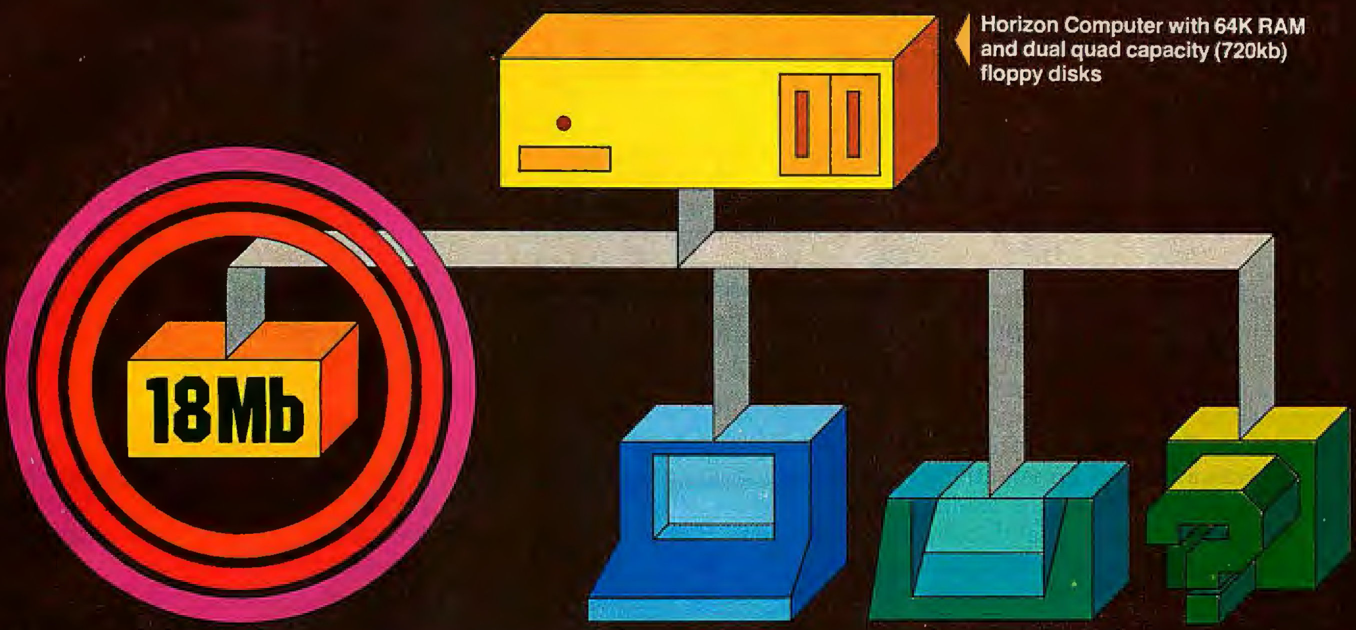

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I/O Expansion for the TRS-80

Part 2: Serial Ports

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POB 582
Glastonbury CT 06033

Last month in Part 1, I discussed the attachment of parallel input and output ports to the Radio Shack TRS-80 computer. This was basically a response to the many inquiries I have had on TRS-80 interfacing. As usual, it was a general presentation, intended to first enlighten the reader with interfacing concepts and then tender a few alternative circuits for construction. While TRS-80 owners benefit most directly, many computers have similar bus structure and can just as easily accommodate parallel input/output (I/O) expansion.

The presentation this month of a serial interface for the TRS-80 required a little more thought. Parallel ports are strictly hardware devices which in their simplest form only require execution of a single assembly-language or BASIC instruction to function efficiently. A serial interface, on the other hand, needs a software program to direct its operation. The many registers and buffers involved in the serial communication process must be synchronized by the execution of a *serial-driver* routine stored in memory. Any design for a serial port has to take into account the capabilities and memory location of this routine. Even the most splendid hardware circuit would be a failure if the software driver interfered with other computer functions.

To eliminate any potential problems that might occur, I decided to make my design completely software-compatible with existing TRS-80 serial-driver routines. This does not necessarily minimize circuit complexity by any means, but it greatly enhances potential user acceptance.

I was equally concerned with the power requirements and physical

This RS-232C interface design is compatible with existing TRS-80 serial-interface control software.

configuration. Radio Shack sells a serial-interface board for the TRS-80, but it cannot be operated independently and requires integral attachment to the expansion interface

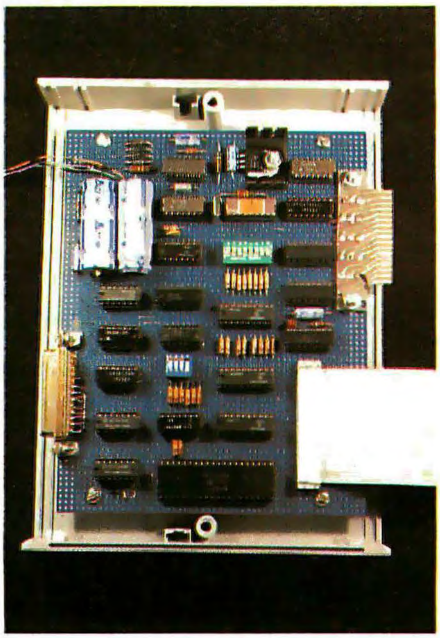

Photo 1: *Prototype of the COMM-80 interface. The ribbon cable at the lower right connects to the expansion-bus port (either the expansion connector on the keyboard/processor unit or connector J2 on the expansion interface). The edge connector at the upper right is for the Centronics-compatible, parallel printer port. The RS-232C DB-25S connector is at the lower left.*

module. The expansion interface and one serial port add $400 to the cost of the basic computer. Also, with its present hardwired addressing, the TRS-80 can support only one serial port and one parallel printer port.

Depending upon the intended application, you may not need the extra functions (eg: disk controller and memory expansion) provided in the expansion interface. The $300 outlay for the expansion interface is an extraordinary expense if you merely intend to attach a modem and use the TRS-80 as a terminal on a timesharing network, such as the Source or MicroNet. Rather than duplicate what I consider to be a restrictive hardware configuration, I have attempted to present a cost-effective communications interface that gives more flexibility in use and has a better price/performance ratio.

The COMM-80 Communications Interface

The approach I decided to take was to combine elements from Part 1 of this article with this one, and produce a stand-alone serial/parallel interface which could plug directly into the expansion-bus connector (the keyboard-unit expansion connector or connector J2 on the expansion interface). Designated the COMM-80, the unit includes a 50 to 19,200 bit per second (bps) RS-232C serial port, a full 8-bit-in/8-bit-out parallel printer port, an auxiliary expansion-port edge connector, and switch-selectable addressing which allows a single TRS-80 to simultaneously connect up to sixteen COMM-80 interfaces. A block diagram of the COMM-80 is presented in figure 1, and a picture of the prototype is in photo 1.

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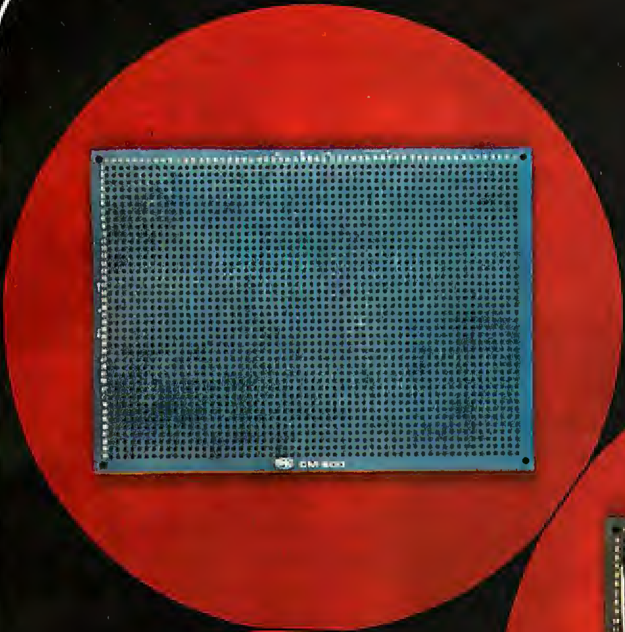

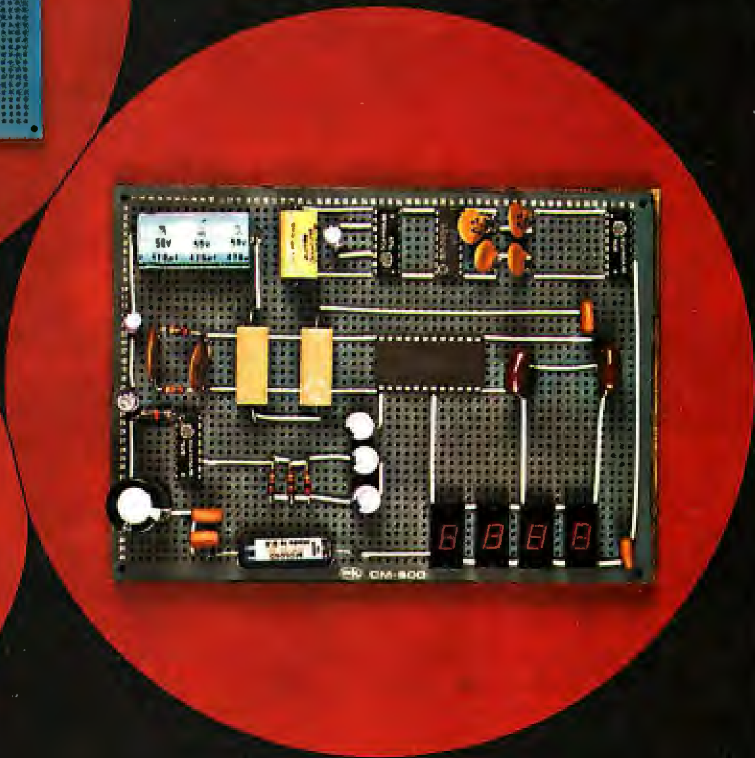

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What Is a Serial Port?

Communication between computers, terminals, and other peripheral devices can be in either serial or parallel mode. In parallel mode, the entire information segment (ie: data word) is transmitted or received simultaneously in a single time frame. In serial mode, this same information is divided into its constituent bits and these bits are transmitted individually over a longer period of time. In cases where high-speed data rates are involved, such as in interaction with a floppy-disk drive, the communication is usually in parallel and can involve as many as forty data and control lines. Serial mode is generally used for lower-speed exchanges.

Photo 2: *Here are two ways of adding RS-232 communication capability to the Radio Shack TRS-80. The COMM-80 unit is shown on the left; the combination of the Radio Shack expansion interface and serial-interface board is shown on the right.*

Photo 3: *A TRS-80 equipped with Level II BASIC, the COMM-80 interface, and a Novation CAT modem can be used as a remote terminal for a time-sharing service such as the Source.*

An example a little closer to home is the addition of a video terminal and a printer to a computer system. Both the terminal and printer are designed to accept American Standard Code for Information Interchange (ASCII) coding, which requires only 7 bits to define a character.

The connections between the computer and the video terminal can be either serial or parallel. The choice in this case is not determined by data rate but by expense. Parallel communication is relatively easy and inexpensive for a computer. Few components are involved, and a 6-foot length of nine-conductor cable (seven lines to carry the 7-bit ASCII data, one line each for data strobe and ground) will not cost too much. Serial interfacing is another matter entirely.

Microprocessors do not naturally communicate in serial format. There are no single machine-language instructions to perform this function. To serialize data we must add a separate hardware device called a universal asynchronous receiver/transmitter (UART). It looks just like a parallel port to the processor, but internally the UART is a very complicated device.

A UART is a special large-scale integration (LSI) circuit that accepts a data byte in parallel form from the processor and converts it into a universally accepted serial format. Any two terminals set at the same data-transmission rate could conceivably be interconnected to communicate, regardless of internal operating-system differences. The expense for this flexibility is in the neighborhood of $200 to $500 per data channel, depending upon the computer bus configuration.

Transmitting Serial Data

Serial data can be transmitted in either *synchronous* or *asynchronous* format. I will address this discussion only to the latter format since asynchronous communication is the technique employed in the COMM-80. The asynchronous format allows unlimited time gaps to occur between transmission of characters.

The internal structure of a UART consists of a separate parallel-to-serial transmitter and a serial-to-parallel receiver joined by common programming pins. The two sections can be used independently provided

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they adhere to the same bit-format options. Sending a character from the processor is simply a matter of performing a parallel-output operation to the UART. The decoded-output strobe loads the UART with the data and initiates the serialization process.

Figure 2 shows a plot of logic levels versus time during the transmission of a single character. When no data is being sent, the data-transmission line remains in a logic 1 state. A 1-to-0 high-to-low transition on the line signifies that a character is being sent. The first bit is called a *start bit*. The next 5 to 8 bits are data; these are followed by a parity bit. Finally, the end of transmission is defined by the addition of 1 or 2 stop bits at the end of the character. The start, stop, and parity bits are all added as part of the UART's function.

Meanwhile, the receiver section of the UART is continuously monitoring the input line for the start bit of a character. When the start bit comes, the following data bits are placed into a holding register and their parity is checked against the state of the parity bit. Completion is signaled by setting a *data-available* flag. This flag, plus others defining *buffer status, parity,* and *overrun errors,* is read by the processor to determine when input data is ready or when another character can be transmitted. The individual pin functions of a typical UART are described in table 1.

RS-232C Interface Characteristics

So far, I have discussed only serialization of the data. I have said nothing about voltages or logic conventions associated with control of the information transmitted between

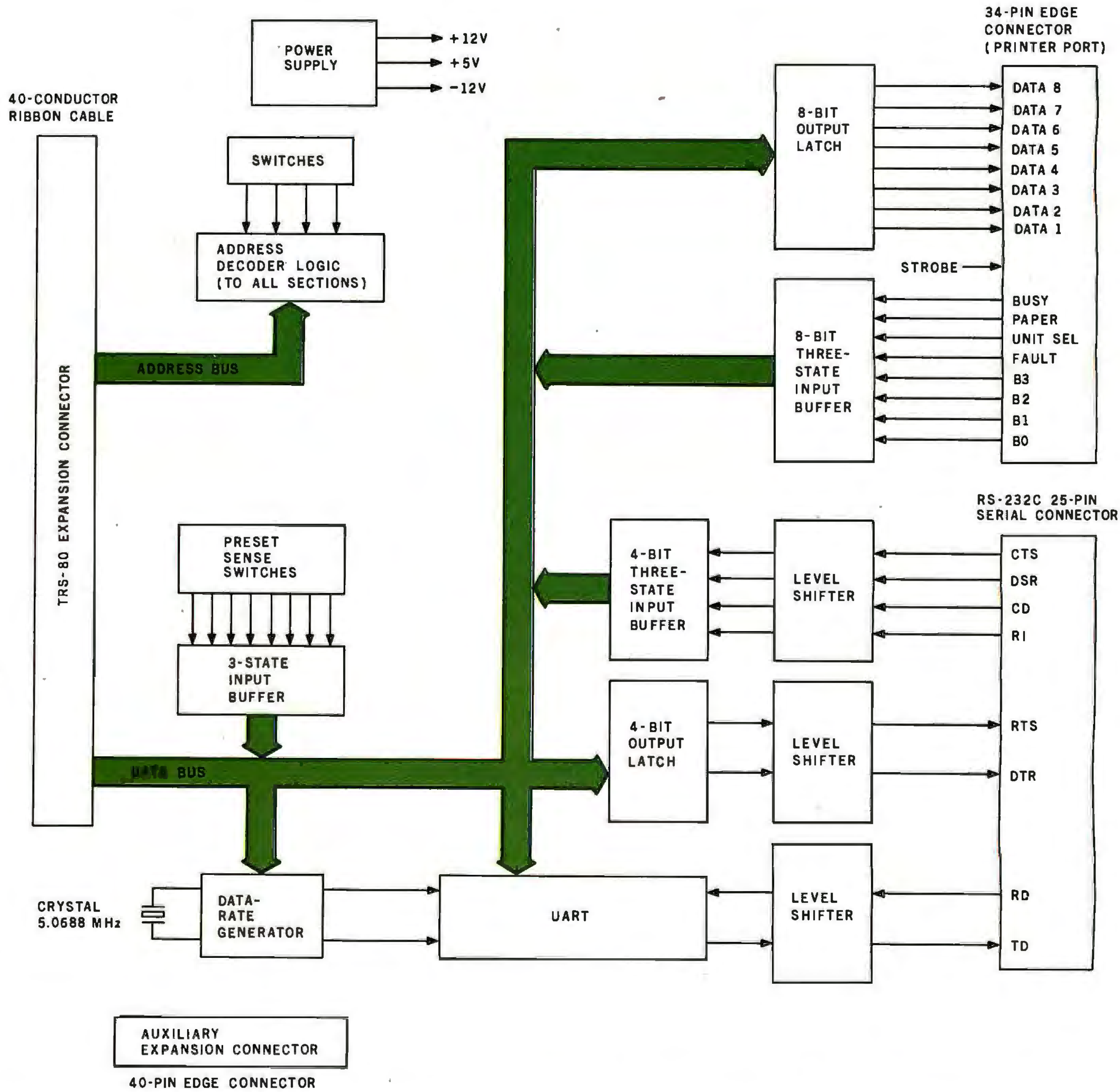

Figure 1: *Block diagram of components and data flow in the COMM-80 serial and parallel interface for the Radio Shack TRS-80.*

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base 2 inc. P.O. BOX 3548 FULL., CAL. 92634 / (714) 992-4344 equipment. The Electronic Industry Association (EIA) RS-232C electrical specification defines voltage levels and control signals: a logic level 1 is called a "mark" or "off" and is considered to be anything more negative than −3 V. A logic 0 is called a "space" or "on" and is considered to be anything more positive than +3 V. As a rule, designers tend to use +12 V and −12 V for the 0 and 1 logic states.

In addition to standardizing the serial format, the EIA also specifies that the connector for RS-232C be a 25-pin, D subminiature type (called a *DB-25*). The pin assignments and functions are shown in table 2.

The COMM-80 Hardware

The COMM-80 is driven only by signals present on the buses of the computer. All sections communicate with the processor as memory-mapped or directly addressed input/output ports. Figure 3 illustrates the complete schematic diagram of the COMM-80 interface in three sections.

There are two major sections: parallel printer port and serial port. They are joined together by a common address-decoding circuit and power supply.

Address Decoding

A standard TRS-80 expansion interface has an edge connector commonly called the Centronics printer port. It actually combines an 8-bit parallel output port and a 4-bit parallel input port. The addressing for this section is hardwired for hexadecimal memory location 37E8. Part of this same address decoder is used for the Radio Shack serial-interface board. Coincidentally, the Radio Shack serial interface is decoded to use I/O port addresses E8 thru EB for data-transfer and control functions.

The address-decoding section of the COMM-80, consisting of IC1 thru IC7, is designed to decode this set of addresses as well as a range of other addresses. The range for the printer port is hexadecimal memory addresses 3708 to 37F8, and the serial range is hexadecimal I/O addresses 08 to F8. Figure 4 illustrates the switch settings for the different ranges.

There is a particular rationale for setting up the addresses this way. A user attaching a COMM-80 to his system would naturally set the switches for the range E8 thru EB, and the interface would then be completely compatible with standard TRS-80 software. Should an expansion-

Pin Number	Name	Symbol	Function
1	V_{CC} Power Supply	V_{CC}	+5 V Supply
2	V_{GG} Power Supply	V_{GG}	−12 V Supply (Not connected on AY-5-1015
3	Ground	V_{GL}	Ground
4	Received Data Enable	RDE	A logic 0 on the receiver-enable line places the received data onto the output lines.
5–12	Received Data Bits	RD8, RD7, RD6, RD5, RD4, RD3, RD2, RD1	These are the eight data output lines. Received characters are right justified; the least significant bit (LSB) always appears on RD1. These lines have three-state outputs.
13	Parity Error	PE	This three-state line goes to a logic 1 if the received-character parity does not agree with the selected parity.
14	Framing Error	FE	This three-state line goes to a logic 1 if the received character has no valid stop bit.
15	Over-Run	OR	This three-state line goes to a logic 1 if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver-holding register.
16	Status Word Enable	SWE	A logic 0 on this three-state line places the status word bits (PE, FE, OP, DAV, TBMT) onto the output lines.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is sixteen times the desired receiver data rate.
18			
18	Reset Data Available	RDAV	A logic 0 will reset the DAV line.
19	Data Available	DAV	This three-state line goes to a logic 1 when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A marking (logic 1) to spacing (logic 0) transition is required for initiation of data reception.
21	External Reset	XR	Resets shift registers. Sets SO, EOC, and TBMT to a logic 1. Resets DAV, and error flags to 0. Clears input data buffer. Must be tied to logic 0 when not in use.
22	Transmitter Buffer Empty	TBMT	The three-state transmitter buffer-empty flag goes to a logic 1 when the data bits holding register may be loaded with another character.

Table 1: *Pin functions for the AY-5-1013, AY-5-1015, or COM2017 UARTs.*

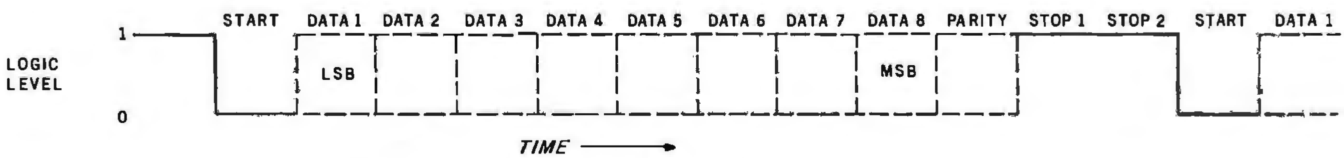

Figure 2: *Logic levels plotted against time during the transmission of an 8-bit data word in asynchronous serial format.*

Pin Number	Name	Symbol	Function
23	$\overline{\text{Data Strobe}}$	$\overline{DS}$	A strobe on this line will enter the data bits into the data-bits-holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character	EOC	This line goes to a logic 1 each time a full character has been transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	The entire character is transmitted bit by bit (that is, serially) over this line. It will remain at logic 1 when no data is being transmitted.
26	Data Bit Inputs	TD1	There are up to 8 data-bit-input lines available.
27		TD2	
28		TD3	
29		TD4	
30		TD5	
31		TD6	
32		TD7	
33		TD8	
34	Control Strobe	CS	A logic 1 on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control-bits-holding register. This line can be strobed or hardwired to a logic 1 level.
35	No Parity	NP	A logic 1 on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic 0.
36	Number of Stop Bits	TSB	This lead will select the number of stop bits (1 or 2) to be appended immediately after the parity bit. A logic 0 will insert 2 stop bits.
37	Number of Bits Per Character	NB2	These two leads will be internally decoded to select either 5, 6, 7, or 8 data bits per character. *NB2 NB1 bits/character* 0 0 5 0 1 6 1 0 7 1 1 8
38		NB1	
39	Odd/Even Parity Select	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic 0 will insert odd parity, and a logic 1 will insert even parity.
40	Transmitter Clock	TCP	This line will contain a clock whose frequency is sixteen times the desired transmitter data rate.

interface module be added to the system later, the user would merely flip a switch specified by table 3 to change the port address (the expansion interface is set only for 37E8). The switch circuit is shown in figure 4. The system could then accommodate two printers. As table 3 shows, there are sixteen possibilities, so there could be sixteen printers and sixteen serial ports. From this point on, however, I will refer only to the addressing range of E8 thru EB.

The Printer Port Is a Full 8 Bits

Since I explained parallel ports in detail last month, I will discuss the printer port briefly. Initially my intention was to provide a general-purpose I/O port so that the user could connect some of my other projects and interface designs. As it worked out, however, I decided to combine efforts and configure the parallel port to serve as the printer port as well. The major difference is that the COMM-80 incorporates a full 8-bit input and a full 8-bit output port. Its address is nominally hexadecimal 37E8 in memory-address space. Writing to memory location 37E8 latches data onto IC14 and IC15 (both 74LS75 devices), and reading memory location 37E8 gates the printer status signals through the three-state buffer IC19 (a 74LS244 device).

Once you have installed an RS-232 port, a whole new world of peripherals opens up.

Serial Port

The serial-port section requires four input and four output strobes to operate. As previously mentioned, the serial-port control addresses are nominally set for hexadecimal E8 thru EB. Figure 5 more explicitly illustrates the hardware derivation of these signals and lists their functions. These strobe signals coordinate the RS-232C handshaking, the sense switches, the data-rate generator, and the UART. All four subsections can be independently controlled in software by reading and writing to the appropriate port address.

The sense switches, for instance, are merely a convenience. It is a way for the user to present a frequently used combination of options. These switches, outlined in figure 6, allow selection of data rate, word length, parity condition, and number of stop bits. There is, however, no physical connection between these switches and the other sections. The software-driver routine coordinates the option selection.

First the routine determines the state of the switches by reading input port E9. It determines from the setting of switches SW6 thru SW8 what data rate the user wants. The particular code for that rate, selected from table 4, is written to output port E9. The remaining switch settings are written into the UART control register EA. Three bits of this output (b_0 thru b_2) and input port E8 are used for the RS-232C handshaking. The data-rate generator is presented in figure 7.

The sense switches are not absolutely necessary for operation of the serial interface. Most software drivers, such as the ST80 program written by Lance Micklus, offer a selection of the options through the keyboard. Separate data rates for the

Text continued on page 54

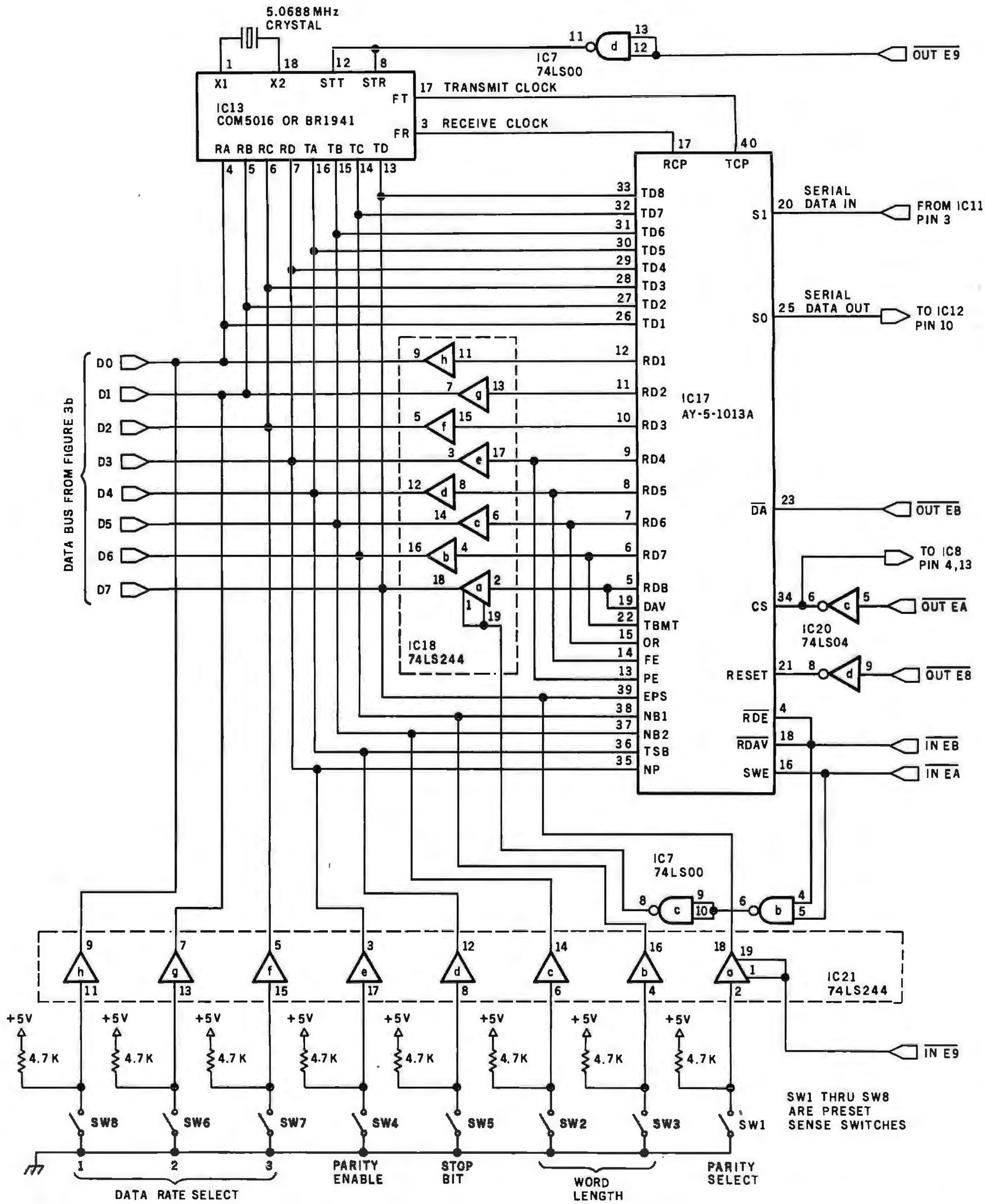

Figure 3a: *Section of schematic diagram of COMM-80 interface circuit. Shown here are the data-rate selector, the UART, and the option-selecting switches. The data-rate selector can be either a COM5016 or a BR1941. Various UARTs can be used instead of the AY-5-1013A, including the TR1602, COM2017, S1883, and TMS6011. A UART that uses a single +5 V power supply, such as the AY-3-1015, may also be substituted.*

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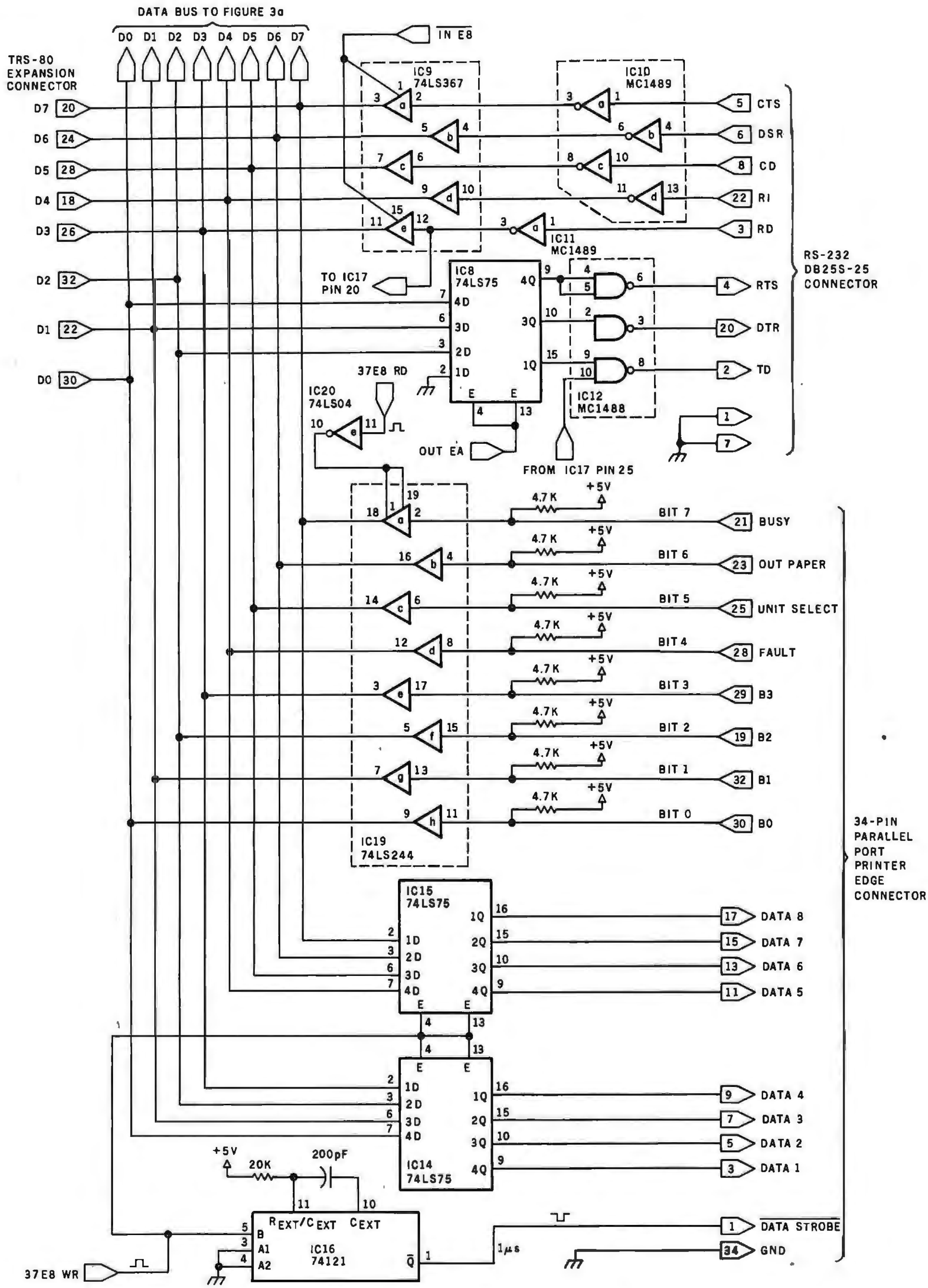

Figure 3b: *Section of schematic diagram of COMM-80 interface. Connections to data buses and peripheral connectors are presented here. Some care must be exercised in connecting the COMM-80 to the expansion bus. It is best to use shielded ribbon cable. The production version of the COMM-80 includes two auxiliary expansion-bus edge connectors, which are like the one on the back of the keyboard/processor unit.*

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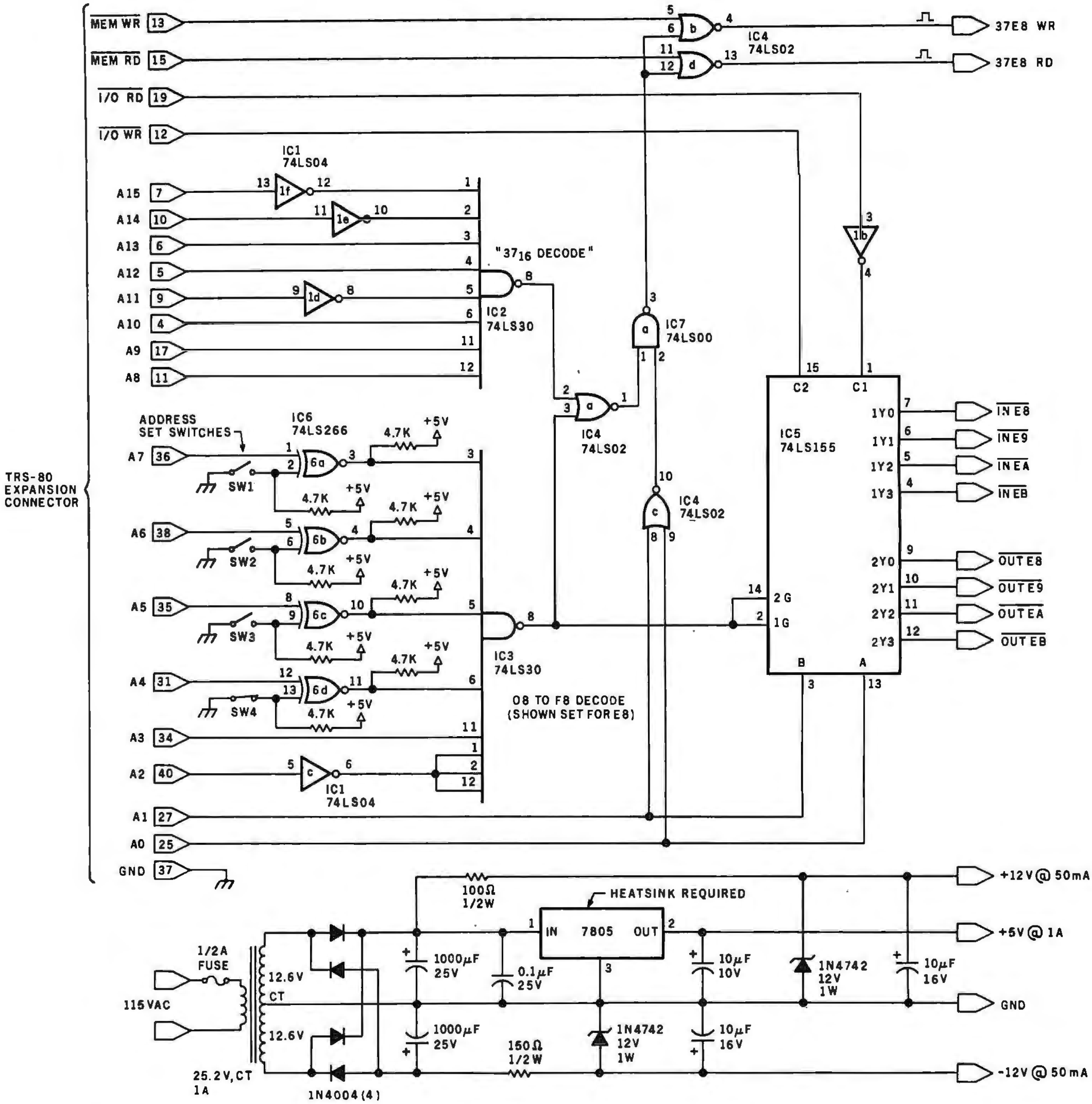

Figure 3c: *Section of COMM-80 interface circuit, including power supply and address-selection circuitry. Power to the interface should not be cut off while the TRS-80 is in operation, lest programs be lost. Both units should be powered up and down simultaneously.*

Text continued from page 49:
transmitter and receiver can also be established. This is easily accomplished by a direct output command to the data-rate generator using the codes from figure 6.

From this point on, serial communication proceeds by simply loading the UART with the data to be transmitted (using the Z80 instruction OUT EB) and reading the UART status register to see if the byte has been completely sent or if there is a received data word available (with the IN EA instruction).

The software driver needed for this interface is too long to discuss in this

Text continued on page 58

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Pin 1	PGND — Protective Ground This is chassis or equipment ground. It may also be tied to signal ground.
Pin 2	TD — Transmit Data This is the serial data from the terminal to the remote receiving equipment. When no data is being sent it is in a marking (1) condition.
Pin 3	RD — Receive Data This is the serial data from the remote equipment which is transmitted to the terminal.
Pin 4	RTS — Request to Send Controls the direction of data transmission. In full-duplex operation an "on" sets transmit mode and an "off" sets non-transmit mode. In half-duplex operation an "on" inhibits the receive mode and an "off" enables it.
Pin 5	CTS — Clear to Send Signal from the modem to the terminal indicating ability to transmit data. An "on" is "Ready" and an "off" is "not ready."
Pin 6	DSR — Data Set Ready Signal from the modem to the terminal. An "on" condition indicates that the modem is ready.
Pin 7	SGND — Signal Ground
Pin 8	CD — Carrier Detect An "on" indicates reception of a carrier from the remote data set; "off" indicates no carrier is being received.
Pin 20	DTR — Data Terminal Ready: "on" connects the communication equipment to the communications channel; "off" disconnects the communications equipment from the communications channel.
Pin 22	RI — Ring Indicator An "on" indicates that a ringing signal is being received on the communications channel.

Table 2: *Designations of pins on the DB-25 connector when used for communication with an RS-232C interface system and description of corresponding signals.*

Address Range	SW1	SW2	SW3	SW4
08 thru 0B	Closed	Closed	Closed	Closed
18 thru 1B	Closed	Closed	Closed	Open
28 thru 2B	Closed	Closed	Open	Closed
38 thru 3B	Closed	Closed	Open	Open
48 thru 4B	Closed	Open	Closed	Closed
58 thru 5B	Closed	Open	Closed	Open
68 thru 6B	Closed	Open	Open	Closed
78 thru 7B	Closed	Open	Open	Open
88 thru 8B	Open	Closed	Closed	Closed
98 thru 9B	Open	Closed	Closed	Open
A8 thru AB	Open	Closed	Open	Closed
B8 thru BB	Open	Closed	Open	Open
C8 thru CB	Open	Open	Closed	Closed
D8 thru DB	Open	Open	Closed	Open
E8 thru EB	Open	Open	Open	Closed
F8 thru FB	Open	Open	Open	Open

Table 3: *Use of the switch-selectable address decoder allows the I/O address range to be varied over the range shown here according to the switch positions specified. (See figure 4.) Radio Shack software uses the address range hexadecimal E8 thru EB.*

Listing 1: *Part of the output generated during a timesharing session on the Source, in which the TRS-80 equipped with the COMM-80 and a modem was used as a terminal. The Source is a service of the Source Telecomputing Corporation of McLean, Virginia. The hard copy was produced by an LA36 DECwriter connected to the TRS-80 through the COMM-80.*

```
>DATA SYSCOM

************************ SYSTEM COMMANDS ***********************

COMMAND                 DESCRIPTION
-------                 -----------

BASIC        PROGRAM IN THE BASIC LANGUAGE.
CHAT         TALK TO ANOTHER USER ON THE SYSTEM.
CRTLST       DISPLAYS THE CONTENTS OF A FILE, STOPPING EVERY 24
             LINES TO GIVE YOU TIME TO CATCH UP. (TYPING A RETURN
             RESTARTS THE DISPLAY.)
```

Listing 1 continued on page 58

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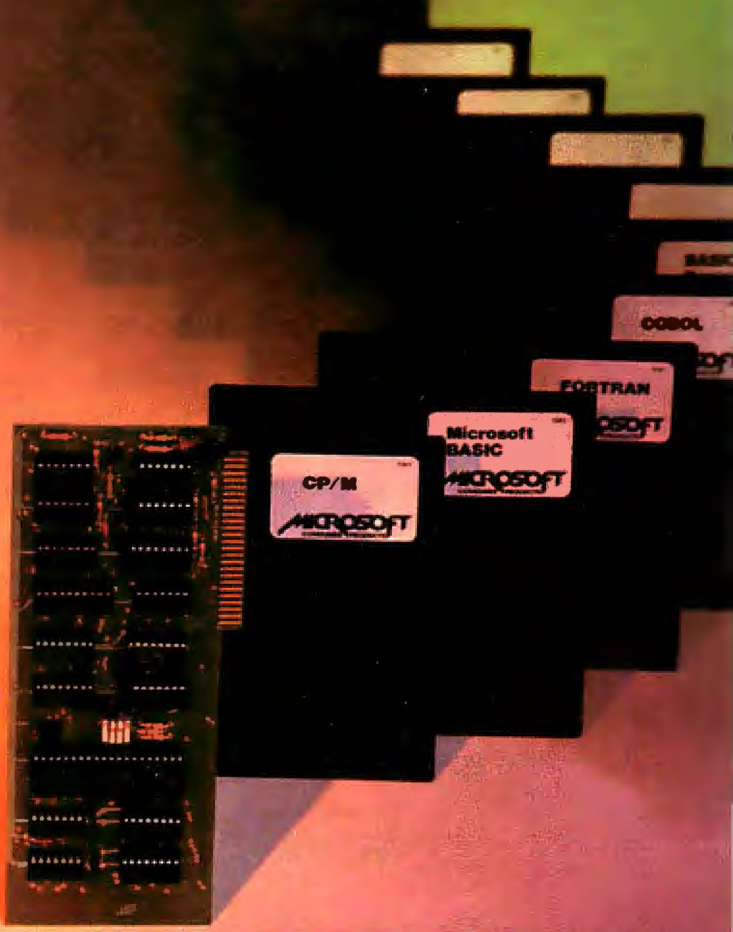

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Listing 1 continued:

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DEL             DELETES A FILE.
DELAY           AUTOMATICALLY DELAYS OUTPUT TO PRINTING TERMINALS
                WITH SLOWLY RETURNING CARRIAGES.
ED              TEXT EDITOR.
ENTER           TYPE IN A FILE.
FILES           PRINTS THE NAME OF ALL YOUR FILES.
FORTRN          COMPILES A FORTRAN PROGRAM.
ID              SYSTEM SIGN-ON COMMAND.
INFO            DISPLAYS CERTAIN OTHER LIBRARY PROGRAMS AND DATA BASES.
LOAD            LOADS A FORTRAN PROGRAM.

MAIL            INVOKES THE ELECTRONIC MAIL PROGRAM.
NSORT           SORTS A FILE.
OFF             SIGNS A USER OFF THE SYSTEM.
PLAY            PLAYS COMPUTER GAMES.
POST            INVOKES THE CLASSIFIED AD/BULLETIN BOARD PROGRAM.
R               RUNS A LIBRARY PROGRAM.
TIME            DISPLAYS THE TIME USED FOR THE CURRENT SESSION.
RUN             RUNS A LOADED FORTRAN PROGRAM.
TY              LIKE CRTLST, BUT DOES NOT STOP AFTER 24 LINES.
USAGE           SUMMARY OF YOUR SYSTEM USAGE THIS MONTH.

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TCA743      TCA766      TCA830      TCA914      TCB419      TCD011
TCD106      TCD140      TCD202      TCD248      TCD390      TCD419
TCD419      TCD437      TCD444      TCD459      TCD460      TCE052
TCE129      TCE201      TCE217      TCE274      TCE317
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UNITED FEATURES, ETC.) AS WELL AS SYNDICATED COLUMNISTS. FOR A
COMPLETE LIST OF FEATURES, INDEXED BY LOGICAL CONTENT, RETURN TO
THE "COMMAND" LEVEL, AND TYPE.............................UPI
3) SELECT FROM THE "GENERAL", "BUSINESS" OR "SPORTS" CATEGORIES;
 THE SYSTEM WILL THEN ASK YOU FOR ONE OR MORE "KEYWORDS".
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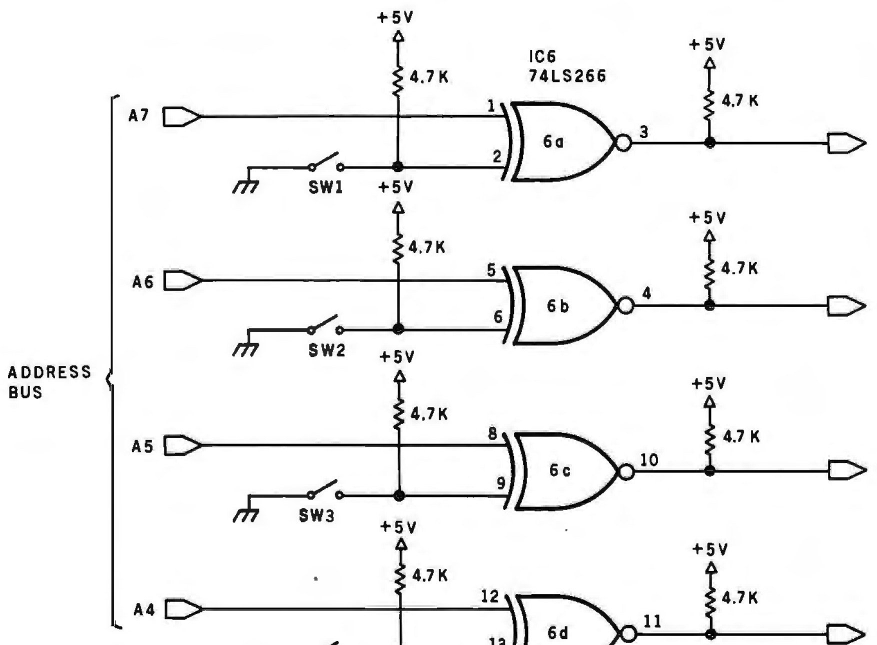

Figure 4: *By closing the proper switches, one of sixteen possible address ranges in the I/O-address space can easily be selected. The switches are optional; the desired address range may be hardwired. For complete compatibility with standard TRS-80 software, the hexadecimal address range E8 thru EB should be chosen.*

T_A / R_A	T_B or R_B	T_C or R_C	T_D / R_D	Data Rate	Clock Frequency
0	0	0	0	50	800 Hz
1	0	0	0	75	1200 Hz
0	1	0	0	110	1760 Hz
1	1	0	0	134.5	2152 Hz
0	0	1	0	150	2400 Hz
1	0	1	0	300	4800 Hz
0	1	1	0	600	9600 Hz
1	1	1	0	1200	19.2 kHz
0	0	0	1	1800	28.8 kHz
1	0	0	1	200	32.08 kHz
0	1	0	1	2400	38.4 kHz
1	1	0	1	3600	57.6 kHz
0	0	1	1	4800	76.8 kHz
1	0	1	1	7200	115.2 kHz
0	1	1	1	9600	153.6 kHz
1	1	1	1	19200	316.8 kHz

Table 4: *Chart to select data rates for the COM5016 data-rate generator. Transmission and reception rates may be set independently, according to the parameters specified here.*

Text continued from page 54:

article. Also, since this interface is software-compatible with existing TRS-80 hardware, there is no need to write your own driver routine. There are many sources, including the one listed with this article.

Using the COMM-80

Once you have an RS-232C port installed in your computer, a whole new world of peripherals opens up. The electronics industry has been turning out thousands of printers each year which use the RS-232C interface. For example, if you are interested in word processing, then you can attach a high-quality daisy-wheel printer to your TRS-80. Certain peripherals require a 20 mA current-loop interface; the required circuit is demonstrated in figure 8.

The most obvious application for the COMM-80 is to transform the TRS-80 from a mild-mannered personal computer into a full-fledged computer terminal. Photo 3 shows the system connected to a modem in actual use on the Source timesharing system. Listing 1 is a printout (from an LA36 DECwriter II also connected to the same serial interface) of typical user interaction on this national computer timesharing network. A look at

Text continued on page 62

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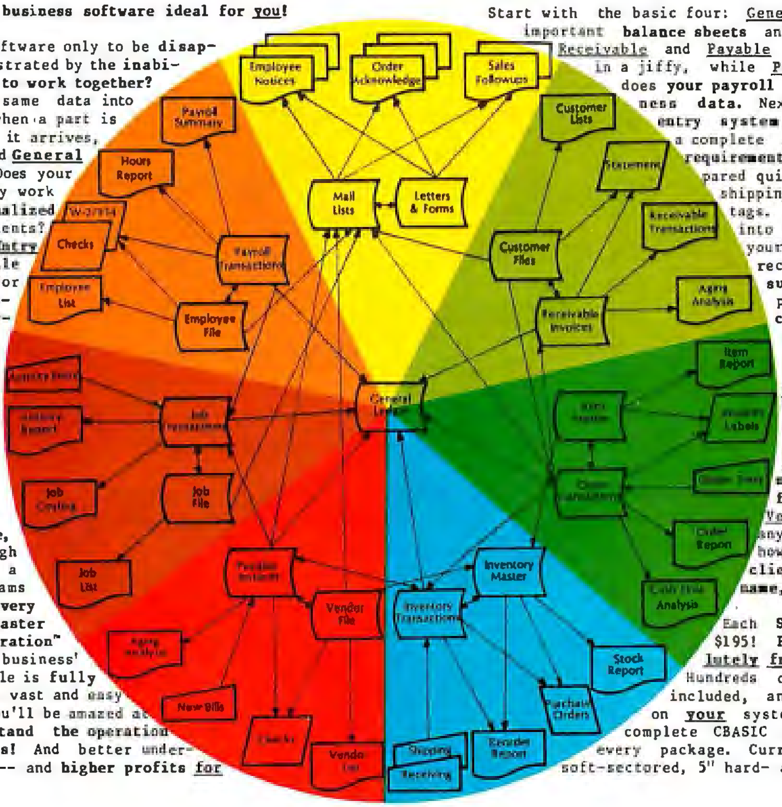

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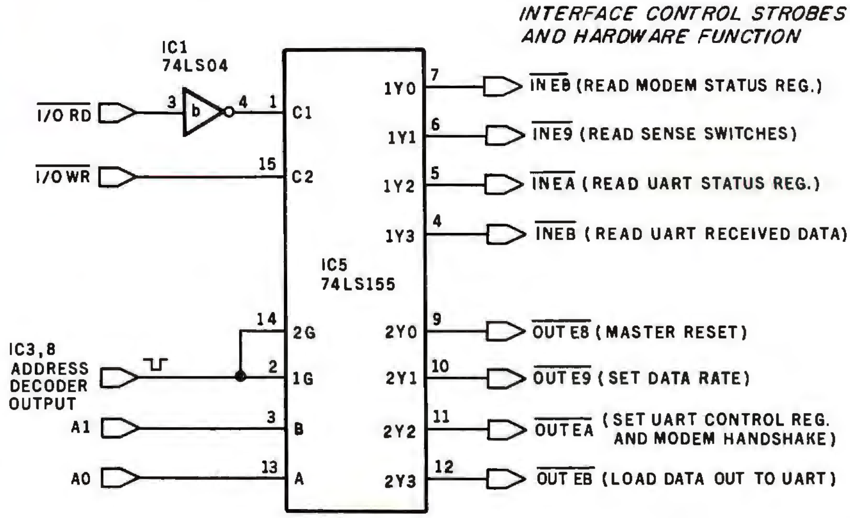
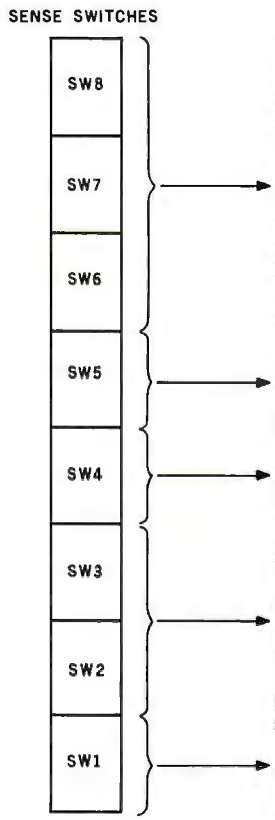


Figure 5: *Detail figure demonstrating interface-control strobes. The address decoder (made up of IC3 and IC6) can be set within the range of hexadecimal 08 to F8. TRS-80 compatibility requires a low address of E8. The output-strobe address notations presented refer only to this setting. Switch settings for other addresses are given in table 3.*



DATA RATE	SW8	SW7	SW6
110	CLOSED	CLOSED	CLOSED
150	OPEN	CLOSED	CLOSED
300	CLOSED	CLOSED	OPEN
600	OPEN	CLOSED	OPEN
1200	CLOSED	OPEN	CLOSED
2400	OPEN	OPEN	CLOSED
4800	CLOSED	OPEN	OPEN
9600	OPEN	OPEN	OPEN

STOP BITS	SW5
1	CLOSED
2	OPEN

PARITY ENABLE	SW4
ENABLED	CLOSED
DISABLED	OPEN

WORD LENGTH	SW3	SW2
5 BITS	CLOSED	CLOSED
6 BITS	OPEN	CLOSED
7 BITS	CLOSED	OPEN
8 BITS	OPEN	OPEN

PARITY SELECT	SW1
ODD	CLOSED
EVEN	OPEN

Figure 6: *Programmable sense switches are read by the processor to allow preselection of UART options under program control. The correspondence of options and switches is illustrated here.*

Number	Type	+5 V	GND	−12 V	+12 V
IC1	74LS04	14	7		
IC2	74LS30	14	7		
IC3	74LS30	14	7		
IC4	74LS02	14	7		
IC5	74LS155	16	8		
IC6	74LS266	14	7		
IC7	74LS00	14	7		
IC8	74LS75	5	12		
IC9	74LS367	16	8		
IC10	MC1489	14	7		
IC11	MC1489	14	7		
IC12	MC1488		7	1	14
IC13	COM5016	2	11		9
IC14	74LS75	5	12		
IC15	74LS75	5	12		
IC16	74121	14	7		
IC17	AY-5-1013A	1	3	2	
IC18	74LS244	20	10		
IC19	74LS244	20	10		
IC20	74LS04	14	7		
IC21	74LS244	20	10		

Table 5: *Power supplies needed by the integrated circuits in the COMM-80.*

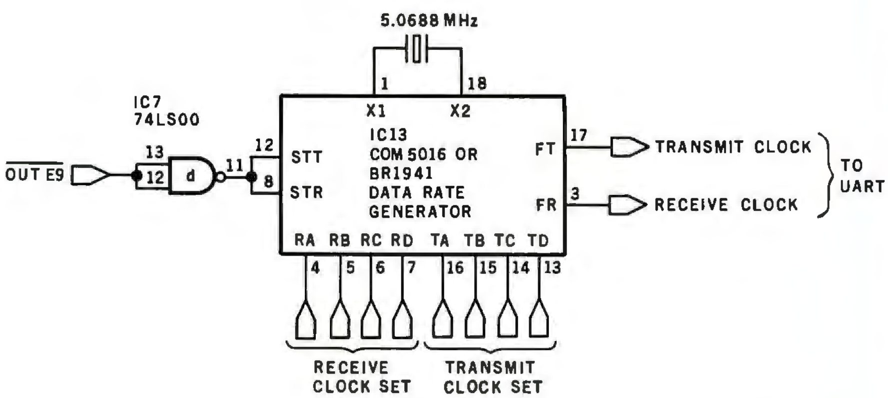


Figure 7: *The data-rate generator determines how fast data is sent and received. Transmission and reception rates can be set independently. The specifications for setting up the various possible data rates on the COM5016 are presented in table 4.*

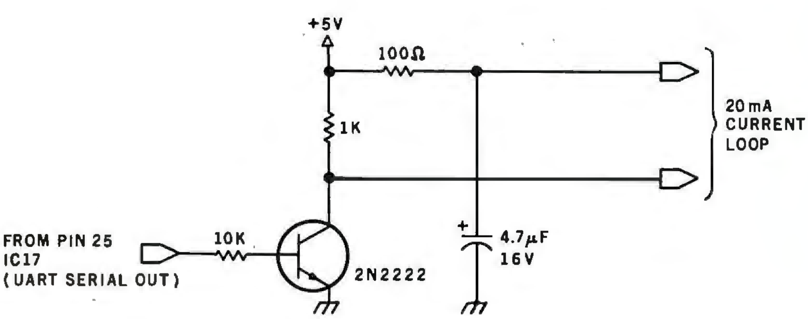
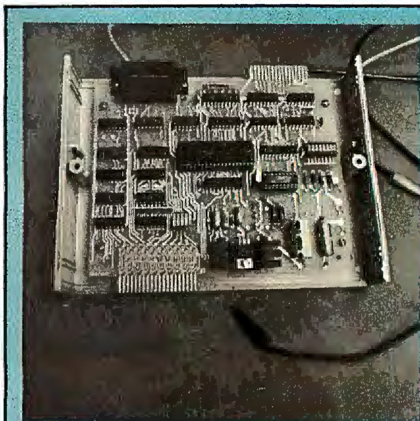


Figure 8: *Some peripheral devices (ie: a Teletype ASR33) must be connected by means of a 20 mA current-loop circuit; such a circuit that can be attached to the COMM-80 is shown here.*

Text continued from page 58:

some of the capabilities available through these networks might convince some people to use the network's facilities rather than spend thousands of dollars to build up an independent single-user system. At $2.75 per hour of connect time, it seems a reasonable alternative. For those of you wishing to contact me via the Source, my electronic-mail identification is TCE317. I welcome questions on this or any other topics that I might possibly be able to answer. ■



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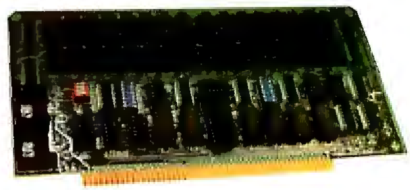

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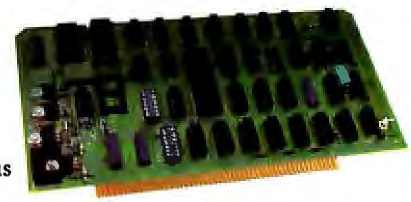

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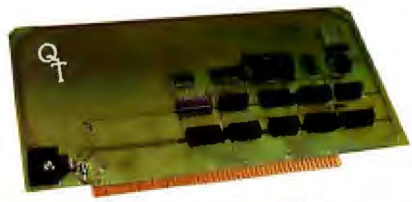

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Z80 Op Codes for an 8080 Assembler

William T Powers
1138 Whitfield Rd
Northbrook IL 60062

If you have a Z80-based machine and an 8080 assembler, you are at a crossroad. You can do one of three things: dispose of your old assembler and purchase a full Z80 assembler; restrict your coding to the subset of the Z80 machine language that is equivalent to the 8080 machine language; or hand-assemble the non-8080 instructions within your Z80 source code. This article details a method I have devised that allows me to assemble all the Z80 instructions using an 8080 assembler without resorting to hand-assembling.

This is how the process works. Suppose you want to exchange the program status word (accumulator, A, and flag byte, F) and its duplicate. In Z80 assembly language, this instruction is:

(Hexadecimal Address)	(Instruction Mnemonic)	(Operand)
1000	EX	AF,AF'

which translates to a 1-byte instruction, hexadecimal 08, to be placed at location hexadecimal 1000. If we have an 8080 assembler that allows us to assign a symbolic name to a 1-byte or 2-byte constant, a 1-byte constant XAF ("exchange the AF pair") can be defined as hexadecimal 08 by a pseudo-operation statement like:

```
XAF    DB  08H
```

(DB stands for "define byte," and this kind of pseudo-operation is called an *equivalence statement*.) Then, when we want to use this instruction in the same program, write

```
1000    DB  XAF
```

which will cause the assembler to place a hexadecimal 08 in memory location 1000. True, this is a makeshift solution, but it is better than hand-assembling, and its merits become more obvious as more complex Z80 instructions are encoded.

(This article will concentrate on explaining the set of mnemonics I have put together; so I will assume that the reader is familiar with the Z80 instruction set.)

Mnemonic Conventions

Two main factors were considered while compiling the list of mnemonics. First, the mnemonics had to suggest the function they perform. Second, they had to avoid using up all the nice letter combinations I like to use in a program.

In general, I have used the following conventions. The letter "X" used in a mnemonic means either *extended* or *indexed*. The abbreviation for the destination comes first, then the source, wherever possible. "M" means *move*, "L" means *load*, "S" means *store to memory*, and "R" means *register*. Many of the mnemonics are preceded by the letter "Z" to keep them from duplicating variable names. For some mnemonics, however, I have abandoned the Z prefix, in the interest of either shortening the mnemonic, making its meaning obvious, or constructing an analog to a useful 8080-code mnemonic as a way to ease the burden on the user's memory.

16-Bit Loads and Stores

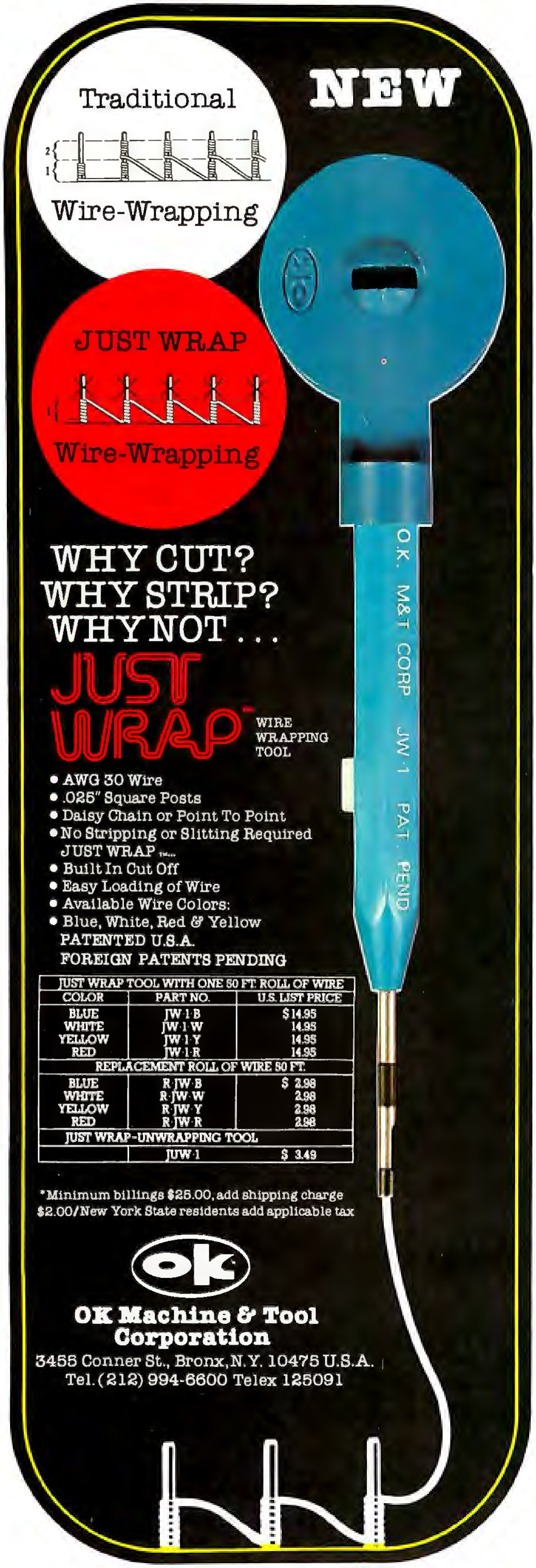
The Z80 has five instructions that are analogous to the 8080 load-HL-register-pair-direct (LHLD)instruction, five analogous to the store-HL-register-pair-direct (SHLD) instruction, and two analogous to the 16-bit immediate-load instruction (LXI). I will refer to the new mnemonics used here as the "Z-symbols."

The Z-symbols SBCD, SDED, SSPD, SIXD, and SIYD correspond to the SHLD instruction on the 8080. These instructions cause the BC registers, the DE registers, the stack pointer (SP), or one of the two index registers (IX and IY), respectively, to be loaded into the location whose address appears in the following 2 bytes. Notice that the middle two letters of the Z-symbol are an abbreviation for the registers to be stored.

The Z-symbols LBCD, LDED, LSPD, LIXD, and LIYD correspond to the LHLD instruction on the 8080. These instructions load the indicated registers from the memory location whose address is stored in the next 2 bytes.

LXIX and LXIY are immediate-mode instructions that coincide with the 8080 instruction LXI H,nn. Index register IX or IY is loaded with the number appearing in the following 2 bytes.

These previously mentioned Z-symbols compile into a 2-byte instruction followed by a 2-byte operand, for a



total of 4 bytes. Since the 8080 assembler cannot recognize the Z-symbols, they must appear in a program as pseudo-operations. On my assembler, the double-byte pseudo-operator is "define word" (DW), and the single-byte pseudo-operator is "define byte" (DB). For example, to load the IX register with the contents of memory location ADDRESS, we write:

```
1000    DW LIXD
1002    DW ADDRESS
```

The DW in each line is not pretty, but otherwise all these instructions look and act like normal assembly-language instructions. The second DW, which is simply a 2-byte address, can include computed offsets such as ADDRESS + 34H (hexadecimal 34 added to ADDRESS), or can be a literal such as 1FFFH (hexadecimal 1FFF). The LXIX and LXIY instructions (immediate load) work the same with the second DW being the 2-byte literal or mnemonic to be loaded.

In my opinion, two of the most useful instructions in this set are the Z-symbols LSPD and SSPD to load and store the stack pointer directly. As an example, if you want to use the stack pointer in a subroutine starting at hexadecimal 1000, start the subroutine with:

```
1000    DW   SSPD
1002    DW   STACK
```

This causes the stack pointer to be stored at the bytes at addresses STACK and STACK+1. Just before the return statement, the original stack pointer should be restored:

```
101A    DW   LSPD
101C    DW   STACK
```

To summarize, here are the Z codes for the instructions just covered:

SBCD, SDED, SSPD, SIXD, SIYD:
store register or register pair in memory
LBCD, LDED, LSPD, LIXD, LIYD:

Z80 Mnemonic	Z-code Mnemonic	Function	Machine Code (Hexadecimal)
RLC	ZRLC	rotate left circular	ii CB dd 06
RRC	ZRRC	rotate right circular	ii CB dd 0E
RL	ZRL	rotate left (with carry)	ii CB dd 16
RR	ZRR	rotate right (with carry)	ii CB dd 1E
SLA	ZSLA	shift left arithmetic	ii CB dd 26
SRA	ZSRA	shift right arithmetic	ii CB dd 2E
SRL	ZSRL	shift right logical	ii CB dd 3E

Table 1: *Z80 indexed rotate and shift instructions. The function of this table is to show the similarity of the machine codes for these instructions. The first byte of each instruction, listed here as "ii", is always hexadecimal DD for the IX register and hexadecimal FD for the IY register. The third byte, listed here as "dd", is the displacement required by the instruction. Note that the actual differentiation among the instructions occurs only in the fourth byte.*

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load register or register pair from memory
LXIX: load IX register with immediate 2 bytes stored with instruction
LXIY: load IY register with immediate 2 bytes stored with instruction

Relative and Indirect Jumps

The Z-symbols for the six relative jumps are:

JR	unconditional jump
JRNZ	jump if zero flag = 0 (result not zero)
JRZ	jump if zero flag = 1 (result is zero)
JRNC	jump if carry flag = 0 (no carry)
JRC	jump if carry flag = 1 (carry)
DJNZ	decrement register B and jump if result not zero

These relative jumps require a single-byte pseudo-operation (DB, for define byte) defining the instruction, followed by a single-byte pseudo-operation containing the relative displacement (−128 to +127) measured from the next instruction. They cannot be combined into a single DW pseudo-operation because the byte describing the relative jump will be one of the defined Z-symbols, whereas the relative displacement will vary with each use.

For example, to jump on carry-clear to a location two addresses beyond the next instruction, we would write:

```
1000    DB  JRNC
1001    DB  2H
```

If the relative jump is to a label, called LABEL, the displacement can be computed by a standard form involving the "$", which is the symbol for the current beginning of the first instruction after the jump):

```
1000    DB  JR
1001    DB  LABEL-$-1
```

There are two indirect jumps in the Z80 that are analogous to the 8080 command PCHL, which puts the contents of the HL register pair into the program counter. This causes a jump to the number contained in the HL register pair. The same can be done with the following Z-code instructions:

JIX	jump to the memory location contained in the IX register
JIY	jump to the memory location contained in the IY register

Input and Output

Now we begin to see instructions that are not simply direct substitutions of codes for symbols. Rather, the resulting instruction is the sum of several Z-symbol mnemonics (each of which represents an option available to a given instruction).

The input and output instructions refer to the data flow through the ports. Data flow between the port and the accumulator is covered by an 8080 assembler, but Z-symbols will have to be devised to generate instructions that initiate data flow between a port and either a

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register or a memory location. When performing input to a register, the associated register is a destination register; on output, the associated register is a source register.

The Z-symbols that are used are:

ZINP	input to a register
ZOUT	output from a register
INPI	input to a register and increment HL register pair by 1
OUTI	output from a register and increment HL register pair by 1
INPD	input to a register and decrement HL register pair by 1
OUTD	output from a register and decrement HL register pair by 1
ZRPT	add "repeat until register B equals 0" feature

These are all 2-byte (DW) mnemonics.

A ZINP or ZOUT is prepared for use by adding the mnemonic to it for the register being used (ZA1, ZB1, ZD1, ZE1, ZH1, ZL1, ZM1). For example, to get input into register D, write:

```
1000    DW   ZINP+ZD1
```

(In this example, the instruction is to be assembled at memory location hexadecimal 1000.) The assembler will add the two constants together, put the low byte of the sum in hexadecimal 1000 and the high byte in hexadecimal 1001. Looking at the table of Z-symbol mnemonics (table 2), we see that ZINP is hexadecimal 40ED and that ZD1 is hexadecimal 1000. Their sum is 50ED, and, looking at a table of Z80 instructions, we find that the hexadecimal code for this instruction (named IN D,(C) in Z80 assembly language) is ED followed by hexadecimal 50. No port address is specified since the instruction requires that register C contains the port number.

The Z80 has four input and output instructions that transfer blocks of information to or from a range of memory, the start of which is pointed to by the HL register pair. The port address is still held in register C. This powerful set of instructions can load or output up to 256 times with a single instruction. Register B is used as an index counter, with the instruction repeating until the value in B is decremented to 0.

The Z codes OUTI and INPI perform output and input with the HL register pair being incremented by 1, and the B register being decremented by 1 after the data move. OUTD and INPD similarly involve decrementing the HL and B registers each time. If OUTI, INPI, OUTD, or INPD is used alone, only 1 byte of memory is moved (although the incrementing and decrementing still takes place). The automatic repetition occurs when the Z-code mnemonic ZRPT (repeat) is added to any of the four codes.

For example, to cause a block of memory starting at the location pointed to by the HL register pair to be sent to the port pointed to by register C (the number of bytes sent as output being the value in register B), we should write this instruction:

```
1000    DW   OUTI+ZRPT
```

I should mention that here, and in all cases, the order of elements makes no difference because two quantities are just being added together. The previous instruction, for example, could just as well have read ZRPT+OUTI.

ZB1	0000	ZDAX	09DD	SBCD	43ED		
ZC1	0800	ZDAY	09FD	SDED	53ED		
ZD1	1000	ZDAC	4AED	SSPD	73ED		
ZE1	1800	ZDSB	42ED	SIXD	22DD		
ZH1	2000	ZXX	CBDD	SIYD	22FD		
ZL1	2800	ZYY	CBFD	ZLXI	2100		
ZM1	3000	ZRLC	00CB	LBCD	4BED		
ZA1	3800	ZRRC	08CB	LDED	5BED		
ZB2	0000	ZRL	10CB	LSPD	7BED		
ZC2	0100	ZRR	18CB	LIXD	2ADD		
ZD2	0200	ZSLA	20CB	LIYD	2AFD		
ZE2	0300	ZSRA	28CB	POPX	E1DD		
ZH2	0400	ZSRL	38CB	POPY	E1FD		
ZL2	0500	ZRLD	6FED	PSHX	E5DD		
ZM2	0600	ZRRD	67ED	PSHY	E5FD		
ZA2	0700	ZBIT	40CB	ZNEG	44ED		
ZSP	3000	ZRES	80CB	XTIX	E3DD		
ZBC	0000	ZSET	C0CB	XTIY	E3FD		
ZDE	1000	BIT0	0000	DJNZ	0010		
ZHL	2000	BIT1	0800	*JR	0018		
ZIX	2000	BIT2	1000	*JRNZ	0020		
ZIY	2000	BIT3	1800	*JRZ	0028		
ZX	00DD	BIT4	2000	*JRNC	0030		
ZY	00FD	BIT5	2800	*JRC	0038		
ZMXR	7000	BIT6	3000	JIX	E9DD		
ZMRX	4600	BIT7	3800	JIY	E9FD		
ZMXI	3600	ZINP	40ED	RETI	4DED		
ZADD	8600	ZOUT	41ED	RTNM	45ED		
ZADC	8E00	ZRPT	1000	I8080	46ED		
ZSUB	9600	OUTI	A3ED	I38	56ED		
ZSBB	9E00	OUTD	ABED	IVECT	5EED		
ZANA	A600	INPI	A2ED	*XAF	0008		
ZXRA	AE00	INPD	AAED	*EXX	00D9		
ZORA	B600	BLMI	A0ED	ZMAI	57ED		
ZCMP	BE00	BLMD	A8ED	ZMIA	47ED		
ZINR	3400	BLSI	A1ED	ZMAR	5FED		
ZDCR	3500	BLSD	A9ED	ZMRA	4FED		
ZINX	2300			ZXTI	E300		
ZDCX	2B00						
KLUGE	0535						

Table 2: *Z codes and their hexadecimal equivalents. This table of variable names (Z codes) and their hexadecimal values should be recreated in a given assembly-language program. This is done via the "define byte" (DB) and "define word" (DW) pseudo-operations (or the equivalent pseudo-operations on the user's 8080 assembler). For example, the first line might read, "ZB1 DB 0000H". All entries except those starred are to be defined as a 2-byte sequence (DW); the starred entries are single-byte sequences (DB).*

Block Moves and Searches

This section deals with four Z codes:

BLMD	block move in decreasing sequence
BLMI	block move in increasing sequence
BLSD	block search in decreasing sequence
BLSI	block search in increasing sequence

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The two block-move Z codes, BLMI and BLMD, move data from the location specified by the HL register pair into the location specified by the DE register pair, using the BC register pair as a 16-bit countdown register. BLMI moves the memory block from bottom to top, while BLMD moves from top to bottom. As in the case of the input-block and output-block instructions, these repeat automatically only if the Z-code mnemonic ZRPT is added to the BLMI or BLMD mnemonic. Without the repeat Z code ZRPT, the move will execute only once with appropriate incrementing and decrementing done as usual but looping to be taken care of externally.

To move hexadecimal 1FFF bytes, for example, from the locations ascending from 0000 into the locations ascending from hexadecimal 2000, load register pair BC with hexadecimal 1FFF, register pair HL with hexadecimal 0000, and register pair DE with hexadecimal 2000. Then write:

```
1000    DW   BLMI + ZRPT
```

The block-compare instructions (with Z codes BLSI and BLSD) work exactly the same as far as the mnemonics are concerned. The repetition mnemonic, ZRPT, is added only if automatic repetition is wanted. The block compares do not move data; instead, they search for the first memory location that matches the contents of register A. To use the search instructions, register pair HL is initialized to the first location to be compared and register pair BC to the number of items to be examined.

An exit from an automatic search loop will occur if a match is found or if the counter in register pair BC runs down to 0. The difference in termination can be told by looking at the flags. If register pair BC made it to 0 without a match occurring, the parity flag is set to 0. If a match occurred and caused the exit, the Z flag is set to 1. Thus, a following JZ or JRZ (jump or jump relative on 0) instruction will cause a jump only if a match was found. In Z code, an automatic block-search instruction in the descending direction looks like:

```
1000    DW   BLSD+ZRPT
```

Operations on Index Registers

The first two Z-code instructions that will be considered in this article are ZINX and ZDCX, which are the 16-bit analogs of the 8080 instructions INX and DCX:

ZINX, ZINY	increment either the IX or IY register by 1
ZDCX, ZDCY	decrement either the IX or IY register by 1
ZX	added to the above to select the IX register
ZY	added to the above to select the IY register

The ZINX and ZINY instructions are used to increment or decrement the 16-bit index registers. To designate which register, either ZX or ZY is added to one of the two mnemonics. (When referring to index registers IX and IY, the general mnemonics ZX and ZY will be used).

For example, to decrement register IX, write:

```
1000    DW    ZDCX+ZX
```

Two more Z80 instructions are POP and PUSH. Since these may occur often, I have assigned an individual Z-code mnemonic to each:

POPX	move data from stack to index register X
POPY	move data from stack to index register Y
PSHX	move data from index register X to stack
PSHY	move data from index register Y to stack

These are 2-byte mnemonics. If you study the symbol table, you will see how to condense the table by defining ZPOP and ZPSH and adding ZX or ZY (which already exist) to them.

The Z-code mnemonics used to exchange the contents of the index registers X and Y with the contents of the location pointed to by the stack pointer are XTIX and XTIY, respectively. These can be condensed to ZXTI+ZX and ZXTI+ZY if desired. XTIX, XTIY, and ZXTI are all 2-byte instructions:

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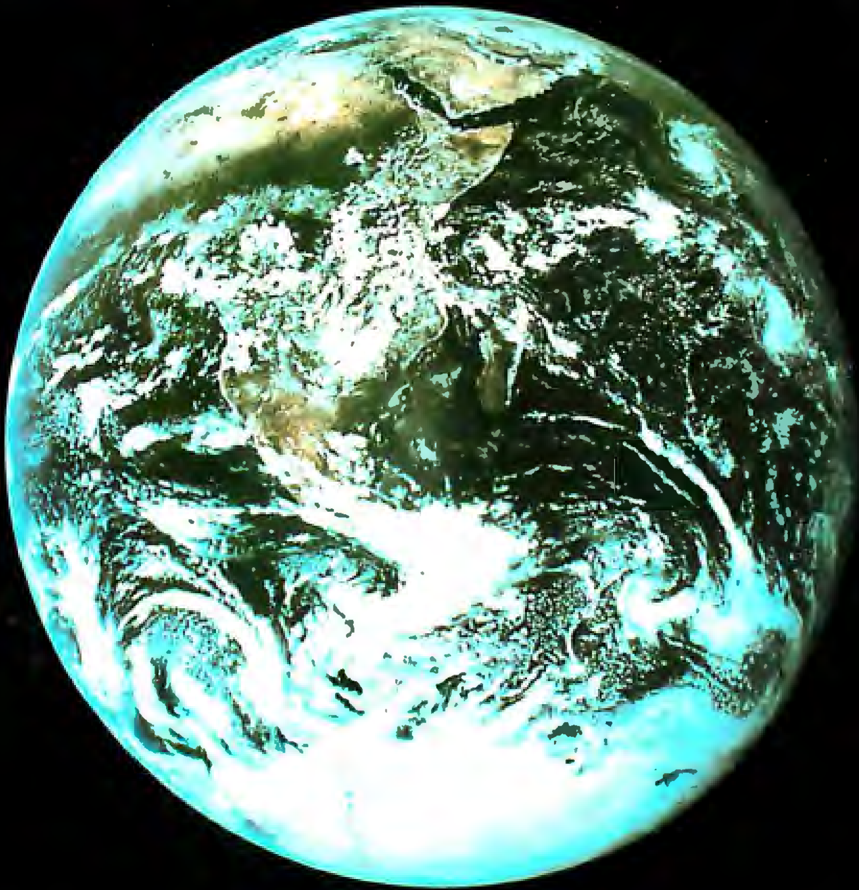

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XTIX	exchange IX with memory pointed to by stack pointer SP
XTIY	exchange IY with memory pointed to by stack pointer SP
ZXTI	same as XTIX if ZX added, same as XTIY if ZY added

As an example, the following sequence exchanges the top two 16-bit items in the stack (destroying the contents of the IX register):

```
1000   DW   POPX
1002   DW   XTIX
1004   DW   PSHX
```

16-Bit Arithmetic

The Z codes used in this section are:

ZDAX	add a register pair to the IX register
ZDAY	add a register pair to the IY register
ZDAC	16-bit add with carry
ZDSB	16-bit subtract with borrow
ZBC	added to select BC register pair as source register
ZDE	added to select DE register pair as source register
ZHL	added to select HL register pair as source register
ZSP	added to select the stack pointer as source register

The Z codes ZDAX and ZDAY are analogous to the 8080 instruction DAD. A 16-bit number is added to either the IX or IY register from the register itself, from the stack pointer, or from either the BC or DE register pair; one index register, however, cannot be added to the other, only to itself. As with the DAD instruction, the carry bit is not involved and no flags are affected. The following codes are added to either ZDAX or ZDAY to specify the register or register pair added to the IX or IY register: ZBC (add the BC register pair), ZDE, ZSP, ZIX (used with ZDAX only), ZIY (used with ZDAY only).

For example, to add without carry the DE register pair to the IY register, write:

```
1000   DW   ZDAY+ZDE
```

The Z80 also permits 16-bit arithmetic with carry or borrow (ZDAC, ZDSB), limiting the destination register to the HL register pair only. It also limits the source register to the BC, DE, and HL register pairs and the stack pointer (use of the IX or IY register is not permitted).

To subtract the contents of the stack pointer from the contents of the HL register pair, with the carry acting as a borrow bit and all relevant flags affected by the operation, we can write:

```
1000   DW   ZDSB+ZSP
```

8-Bit Indexed Arithmetic

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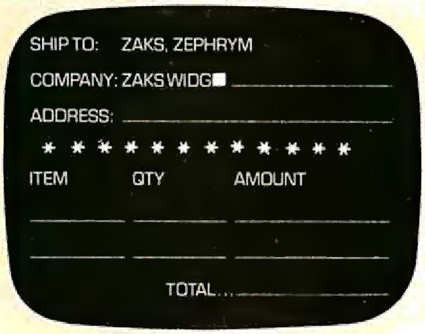

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```
 110  I = 4*J: K = (4*J-1) AND &HOFFO
**0025' L00110:   LD     HL,(J%)
**0028'           ADD    HL,HL
**0029'           ADD    HL,HL
**002A'           LD     (I%),HL
**002D'           DEC    HL
**002E'           LD     A,L
**002F'           AND    FO
**0031'           LD     L,A
**0032'           LD     A,H
**0033'           AND    OF
**0035'           LD     H,A
**0036'           LD     (K%),HL
```

BASIC compiler object code listing

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8080 arithmetic instruction. This mode is the calculation of the location in memory to be used as equal to the contents of the IX or IY register plus an 8-bit displacement stored with the instruction. The Z codes are:

ZADD	add contents of memory to accumulator, no carry
ZADC	add contents of memory to accumulator with carry
ZSUB	subtract contents of memory from accumulator, no borrow
ZSBB	subtract contents of memory from accumulator with borrow
ZANA	logical AND of memory with accumulator
ZORA	logical OR of memory with accumulator
ZCMP	compare accumulator to memory location
ZINR	increment contents of memory location by 1
ZDCR	decrement contents of memory location by 1

All the above Z codes, with the exception of ZINR and ZDCR, perform the given operation on the accumulator and the memory location pointed to, with the result being placed in the accumulator. ZINR and ZDCR are used to increment and decrement, respectively, the given memory location. All of the previously mentioned Z codes are completed by adding the Z code for the desired register (ZX to use the IX register, ZY to use the IY register).

For all ten of these instructions, the DW containing the 2-byte hexadecimal code for the instruction must be followed by a DB containing the 1-byte displacement. To add to the accumulator, for example, a number located at 3 bytes beyond the location pointed to by IX, we write:

```
1000    DW    ZADD+IX
1002    DB    3H
```

To increment the memory location 5 bytes beyond the location pointed to by the IY register, we write:

```
1000    DW    ZINR+ZY
1002    DB    5H
```

Immediate Indexed Moves

Here, use only one Z code:

MVXI	move the immediate byte to the specified (indexed) location

This instruction causes the processor to move the byte that immediately follows to the memory location specified above by an index register plus a displacement. This instruction involves a total of 4 bytes: 2 for the op code itself, 1 for the immediate displacement, and 1 for the immediate byte to be moved (in that order). Again, the op code is completed by adding either ZX or ZY to the Z code MVXI. The displacement and immediate byte can

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be represented as two DB pseudo-operations, especially if either or both are to be computed. If both are constants, they can be combined into a single DW word with a hexadecimal constant of nndd, where nn is the immediate byte and dd is the displacement byte. This is done because the DW pseudo-operation reverses the order of the bytes to ddnn before storage.

For example, to move a hexadecimal 80 to the memory location 6 bytes beyond the location pointed to by the IX register, we can say either:

```
1000    DW   MVXI+ZX
1002    DB   6H
1003    DB   80H
```

or

```
1000    DW   MVXI+ZX
1002    DW   8006H
```

Indexed Register Moves

There are two types of 8-bit move instructions peculiar to the Z80. Their Z codes are:

ZMRX move from register to indexed memory location
ZMXR move from indexed memory location to register

The indexed location is computed as before. The Z-code mnemonics ZMRX and ZMXR may seem confusing but are consistent with the Z80 convention of listing moves in the order "destination, then source."

To complete these Z codes, both an index-register symbol (ZX or ZY) and either a source-register or a destination-register symbol must be added. The problem is that the value to be added for the source or destination register differs with the function, necessitating two names for a given register.

Exchanges	DB XAF DB EXX DW XTI (X,Y)
16-bit Moves	DW S(BC,DE,SP,IX,IY)D; DW (ADDRESS) DW L(BC,DE,SP,IX,IY)D; DW (ADDRESS) DW LXI(X,Y); DW (CONSTANT) DW POP(X,Y) DW PSH(X,Y)
16-bit arithmetic	DW ZDA(X,Y) + Z(BC,DE,SP,IX*,IY*) DW ZD(AC,SB) + Z(BC,DE,HL,SP) DW Z(INX,DCX) + Z(X,Y) *:if X, do not use IY; if Y, do not use IX
Interrupt operations	DW I(8080,38,VECT) DW RETI DW RTNM
Input/output	DW Z(INP,OUT) + Zr1* DW (INPI,OUTI,INPD,OUTD) + ZRPT** *: r = A,B,C,D,E,H, or L **: use is optional
Block moves and searches	DW (BLMI,BLMD,BLSI,BLSD) + ZRPT* *: use is optional
Relative jumps	DB (DJNZ,JR,JRNZ,JRZ,JRNC,JRC); DB (DISPLACEMENT)
Indexed jumps	DW JI(X,Y)
Rotates and shifts	DW Z(RLC,RRC,RL,RR,SLA,SRA,SRL) + Zs2* DW ZRLD DW ZRRD
(indexed)	DW Z(XX,YY); DW Z(RLC,RRC,RL,RR,SLA,SRA,SRL) + KLUGE + (DISPLACEMENT) *: s = A,B,C,D,E,H,L, or M
Bit operations (indexed)	DW Z(BIT,RES,SET) + BITn* + Zs2** DW Z(XX,YY); DW Z(BIT,RES,SET) + BITn + KLUGE + (DISPLACEMENT) *: n = 0,1,2,3,4,5,6, or 7 **: s = A,B,C,D,E,H,L, or M
8-bit indexed arithmetic	DW Z(ADD,ADC,SUB,SBB,ANA,XRA,ORA, CMP,INR,DCR) + Zi*; DB (DISPLACEMENT) *: use ZX or ZY as appropriate
8-bit indexed moves	DW ZMRX + Zr1* + Z(X,Y) DW ZMXR + Z(X,Y) + Zr2* DW ZMXI + Z(X,Y) *: r = A,B,C,D,E,H, or L
8-bit moves	DW ZM(AI,IA,AR,RA)

Table 3: *A summary of usage for the Z codes used in this article. Several abbreviations have been used. The terms in parentheses can be replaced with any one of the terms separated by commas. For example, the line "DW XTI (X,Y)" implies two instructions, "DW XTIX" and "DW XTIY".*

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For example, Z code ZA1 is added to ZMRX because the accumulator is being used as a destination register; but ZA2 is added to ZMXR because the accumulator is being used as a source register. Generally, we can say that the ZMRX Z code requires a Z code of the form Zr1, where r is one of the following symbols: A, B, C, D, E, H, or L. Similarly, the ZMXR Z code requires a Z code of the form Zr2. The ZX or ZY to be added is the same for both ZMRX and ZMXR.

To move a byte from the memory location that is hexadecimal 17 bytes past the address pointed to by IX to register E, write:

```
1000   DW   ZMRX+ZE1+ZX
1002   DB   17H
```

Note that these instructions both require a following data byte for the displacement, which can be a literal (as shown here) or a computed value. One quick rule to tell whether to use Zr1 or Zr2 is as follows: look at the position of the "r" within the last two letters of the instruction mnemonic (ZMXR or ZMRX); if it is first (RX), use Zr1, but if it is second (XR), use Zr2.

Rotate and Shift Instructions

All the rotate and shift instructions, indexed or not, use the following basic Z-code instructions:

ZRLC	rotate left circular (bit 7 goes into bit 0)
ZRRC	rotate right circular (bit 0 goes into bit 7)
ZRL	rotate left with carry (bit 7 goes into carry flag)
ZRR	rotate right with carry (bit 0 goes into carry flag)
ZSLA	arithmetic shift left, pad with zeros on right
ZSRA	arithmetic shift right, pad with sign bit on left
ZSRL	logical shift right, pad with zeros on left

For register-rotate instructions, we must add to one of the above the Z code named Zs2, where s is the register that is to be rotated or shifted (with value A, B, C, D, E, H, L, or M). The memory location pointed to by the HL register pair can be rotated or shifted by adding the Z code ZM2 to one of the above instructions.

To rotate-left-circular register D, for example, write:

```
1000   DW   ZRLC+ZD2
```

When indexed rotates are used, a byte in memory is pointed to by the sum of the contents of an index register (either IX or IY) and a 1-byte displacement value stored with the instruction; it is this byte that is rotated or shifted. However, the structure of this 4-byte instruction does not lend itself easily to this method of using pseudo-operations to represent non-8080 instructions. A detailed explanation is followed by two solutions.

Table 1 contains the previous Z80 instructions in their indexed form. The first byte tells which index register is used for this instruction; it is hexadecimal DD for the IX register and hexadecimal FD for the IY register. The second byte is always hexadecimal CB.The third byte is the 8-bit displacement to be used by the instruction, and the fourth byte identifies the rotate or shift instruction.

The first method of building one of these 4-byte instructions (the method I am currently using) involves building two 2-byte groups with the define-word (DW) instruction. The first word is built by using either the ZXX or the ZYY Z code. This depends on whether the IX or IY register is used to help point to the byte to be operated on. Remember that the DW pseudo-operation reverses the order of bytes before storing them in memory.

The second word is built by creating a double-byte constant that is the sum of the Z-code mnemonic for the desired operation, the displacement, and a constant called KLUGE. This is an unattractive solution, but it is the only way to get the correct information into one line of assembly-language code. Basically, it zeros out the lower byte of the rotate or shift Z code to make room for the displacement byte.

To rotate right with carry the memory location 9 bytes beyond the location pointed to by the IY register, write:

```
1000 DW      ZYY
1002 DW      ZRR+KLUGE+9
```

A second solution involves building the last 2 bytes

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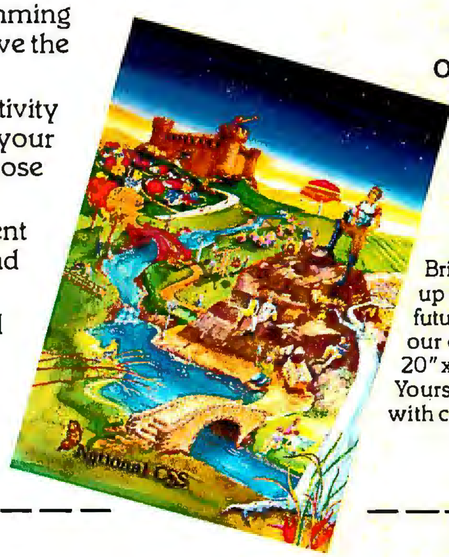

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using two define-byte (DB) pseudo-operations for the displacement and instruction Z code. First define a 1-byte Z code equal to the last byte of the instructions listed in table 1. (For example, set ZZRR equal to hexadecimal 1E for the rotate-right-with-carry instruction.) The previous example given would then take three lines of assembly-language code:

```
1000    DW   ZYY
1002    DB   9
1003    DB   ZZRR
```

In the first method, the only way I have found to handle negative displacements is to write the displacement as hexadecimal 100 minus the desired negative displacement; the added hexadecimal 100 takes care of the borrow that occurs when the negative-displacement byte is added in by 16-bit arithmetic. In the second method, putting a negative constant in the first DB pseudo-operation should do the trick.

Two unique instructions that belong with the rotate instructions have the following Z codes:

ZRLD	rotate accumulator and memory location left, decimal
ZRRD	rotate accumulator and memory location right, decimal

They use a define-word (DW) pseudo-operation and require no added Z codes.

Both instructions act on a byte pointed to by the HL register pair. Given a 16-bit number equivalent to the memory location followed by the accumulator, these instructions rotate left and right, respectively, the 16-bit number by 4 bits. If you consider both bytes as made of two 4-bit *nybbles* (as they are in, say, binary-coded decimal (BCD) arithmetic), the instructions have the effect of rotating 1 nybble within the 4-nybble number. These instructions are useful for BCD arithmetic, for programs dealing with hexadecimal numbers, and for shortening programs that use a large number of shifts or rotates together.

Bit Manipulation Instructions

All the bit instructions, indexed or not, use the following basic Z codes:

ZBIT	test specified bit
ZRES	clear specified bit to 0
ZSET	set specified bit to 1

For register-bit instructions, two Z codes must be added to one of the above Z-code instructions: one specifies which register is affected (its Z code is Zs2, where s specifies register A, B, C, D, E, H, L, or M); the other specifies which bit is to be affected (its Z code is one of BIT0, BIT1, BIT2,. . . ,BIT7). Also, the memory location pointed to by the HL register pair can be used by adding the Z code ZM2 to one of the above instructions.

To test bit 5, for example, in the D register, we write:

```
1000    DW   ZBIT+ZD2+BIT5
```

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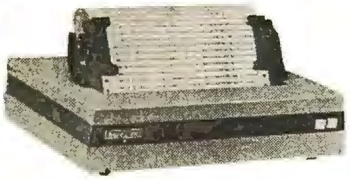

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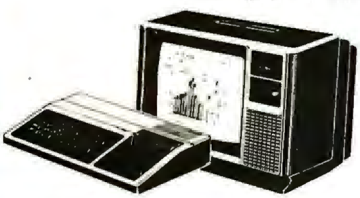

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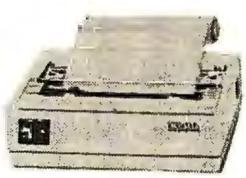

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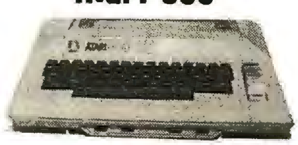

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tions is very similar to the indexed version for the shift and rotate instructions. However, due to the necessity of specifying a bit position, only the first solution, which uses two DW pseudo-operations to generate 4 bytes, will be discussed. The first DW is exactly the same as before, using the Z codes ZXX or ZYY to indicate use of the IX or IY register, respectively. The second DW is the sum of the Z-code instruction (above), the value of KLUGE, the BITn Z code (where n = 0 thru 7), and the displacement.

To clear bit 2 of the memory location 8 bytes past the location pointed to by the contents of the IX register, we write:

```
1000   DW   ZXX
1002   DW   ZRES+BIT2+KLUGE+8H
```

Miscellaneous Instructions

Here are some miscellaneous Z80 instructions and their corresponding Z codes:

RETI	return from interrupt
RETN	return from nonmaskable interrupt
I8080	8080-like interrupt (interrupt mode 0)
I38	interrupt to hexadecimal location 0038 (interrupt mode 1)
IVECT	vectored interrupt (interrupt mode 2)
ZMAI	move accumulator to interrupt register
ZMIA	move interrupt register to accumulator
ZMAR	move accumulator to refresh register
ZMRA	move refresh register to accumulator
EXX	exchange registers with alternate registers
XAF	exchange A and F registers with A' and F'
ZNEG	replace value in accumulator with its two's complement

RETI and RETN are the return-from-interrupt Z codes that stand for the Z80 instructions of the same name. I8080, I38, and IVECT are the Z codes for the Z80 instructions IM 0, IM 1, and IM 2, respectively, each corresponding to an interrupt mode available on the Z80.

The Z codes ZMAI, ZMIA, ZMAR, and ZMRA move between the accumulator and either the interrupt register or the refresh register in the Z80 as specified above. EXX changes the B, C, D, E, H, and L registers with their counterparts, B', C', D', E', H', and L'. The Z code XAF exchanges the A and F registers with their counterparts A' and F'. (The F register contains the Z80 flags.)

Finally, the Z code ZNEG replaces the contents of the accumulator with its two's complement.

The Z code EXX is a 1-byte (DB) instruction. All the others listed here are 2-byte (DW) instructions.

Final Remarks

A complete table of the Z codes employed in this article is given in table 2. A summary of the composite Z80 instructions that can be built using the Z codes is presented in table 3. The entire table (or, if you can keep track, only the Z codes you use) must be included with your assembly-language program. I assemble the program *without* the list of Z codes until I have found all the errors that are due to the absence of the Z-code equivalence statements. I then add the Z-code equivalence statements to the end of the program, do a complete assembly (creating the machine-language module), and stop the listing when I get to the Z codes (to save time and paper).

The Z80 microprocessor has a number of powerful instructions and instruction modes that are not on the 8080. I devised the method presented in this article to enable me to use these instructions without having to buy a Z80 assembler. I hope you have found this approach as useful as I have. ■

BYTE's Bits

Computer Camp

Computer Camp is being held this summer at Rancho Oso, near Santa Barbara, California. Five 2-week sessions will begin June 22 for beginning and advanced students aged 10 thru 15. There will be 2 campers per computer and instruction will cover all aspects of personal microcomputers. Balancing the program will be Rancho Oso's facilities that include horseback riding, tennis, swimming, and more. For more information and application forms, contact Computer Camp, 1235 Coast Village Rd, Suite G, Santa Barbara CA 93108, (805) 965-7777.

Ask BYTE

Conducted by Steve Ciarcia

Beginning this month Steve Ciarcia will answer questions on any area of microcomputing. The most representative questions received each month will be answered and published. Do you have a nagging problem? Send your inquiry to:

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Or, if you are a Source subscriber, send your questions to or chat with Steve (TCE317) directly. Unfortunately, because of the high volume of inquiries, individual replies by mail cannot be given. Please clearly mark all such questions with the words "Ask BYTE."

Dear Steve,

I have constructed the remote-keyboard circuit you described in "Come Upstairs and Be Respectable" (May 1977 BYTE, page 50) for use in several instances, and it has been a great help to me. I am presently planning on installing a video terminal and keyboard in our barn (the computer is 3000 feet away, in the house). What type of cable is suitable for this type of project (I may want to bury the cable)?

Randall Busse

Well, I suggest that you bury a twisted-pair shielded cable and use a pair of differential line-drivers and receivers. I have had good results with Texas Instruments' 75107As and 75110As. I have seen lines spanning 10,000 feet that operate quite nicely.

Unfortunately, you did not mention whether you intend to use direct video to drive your monitor, or if you are trying to transmit serial-data logic levels. For a serial terminal, a communications link similar to the one in my article will suffice, but direct video is more difficult to transmit over that distance. You could use video-quality coaxial cable and a video amplifier for this project, or you might try modulating a radio-frequency carrier and use a standard television set at the end of your cable.

*Either method will require some experimentation. . . .***Steve**

Dear Steve,

I enjoyed reading your article in the October 1979 BYTE on light-emitting-diode (LED) graphics displays ("Self-Refreshing LED Graphics Display," page 58). If a display were built using optical fibers, how would the price compare with a LED-type display? Can you suggest any references? Can you suggest a circuit board (or a manufacturer) that provides high-resolution color graphics with at least a 256-by-256 pixel display?

Robert Ashworth

I am afraid, Bob, that you are trying to compare apples and bananas. Light-emitting diodes are actually light sources while optical fibers are light conductors. The latter have no self-illuminating capability. You could make my LED graphics display into a fiber-optics display. This would be done by "piping" the emitted light to a remote location using optical fibers. Since LEDs are used in both cases, the fiber optics do not make the display any cheaper.

*I hesitate to recommend equipment because graphics depends heavily on the configuration of your computer system. The personal computer market is so dynamic that any suggestion I might make could be out of date by the time it was published....***Steve**

[Editor's Note: *We are planning to publish articles on the subject of high-resolution color graphics in a future issue of BYTE. Watch for it....***CPF]**

Dear Steve,

While sitting in my living room last summer watching Hurricane David whirl by, I wanted nothing more than to use my TRS-80 computer. Unfortunately, our power was out for several hours, and when it came back on, my work was complicated with several brief power interruptions. Has anyone developed a combination emergency and uninterruptible power supply suitable for home-computer systems?

My approach to this problem would start with a well-shielded transformer and regulated battery charger. A zener regulator would float-charge a sealed maintenance-free automobile battery at the manufacturer's recommended voltage to ensure long life. Rather than use a square-wave-type inverter, a crystal-controlled 60 Hz oscillator might be more appropriate, driving a 250 W amplifier that would produce a reasonable approximation of standard AC power. This would provide electricity for my computer and several peripheral devices, including a light bulb.

R B Nottingham

I have been thinking about uninterruptible power quite a bit lately. I first mentioned it in my articles on computer-controlled security for the home in the January thru March 1979 issues of BYTE. (See "Build a Computer-Controlled Security System for Your Home" January 1979 BYTE, page 56; February 1979 BYTE, page 162; March 1979 BYTE, page 150.)

I hesitate to guess at the cost of a 250 W amplifier with a peak output voltage of 176 V. In my own system I have battery backup sufficient for a half hour. The battery is connected directly to the power-supply regulators, and the system shuts down automatically before the power runs out.

*The dilemma I face is that everything in my house is electronically controlled, even the wood stove. (See "A Computer-Controlled Wood Stove" February 1980 BYTE, page 62.) My uninterruptible house requires that I walk out to the garage and start my 5 kW propane-fueled generator, while the computer is running under battery power....***Steve**

Manufacturer	Device Number
Fujitsu	MB 8114
Intersil	7114
Mostek	4114
National Semiconductor	MM 5256
Nippon	µPB 2114
Signetics	2614
Synertek	SY 2114
Texas Instruments	40L45

Dear Steve,

What programmable-memory parts have the same pinout specifications as Intel's 2114 device?

Edward Savage

According to the Texas Instruments MOS Databook, *the static memory circuits listed above are pin-for-pin compatible with the Intel 2114. Please note that these devices are available in a variety of operating speeds....***Steve** ■

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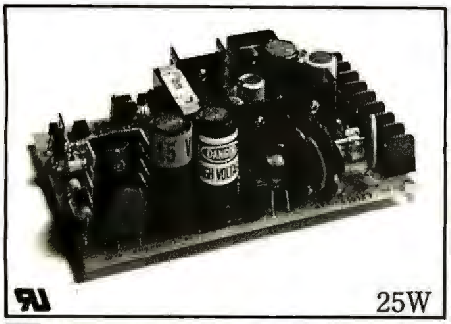

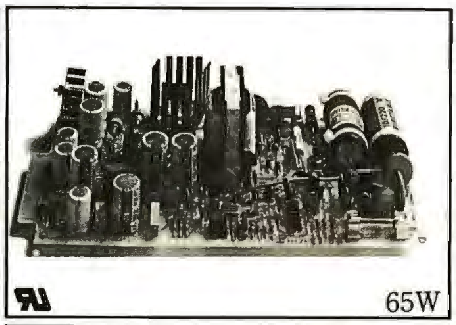

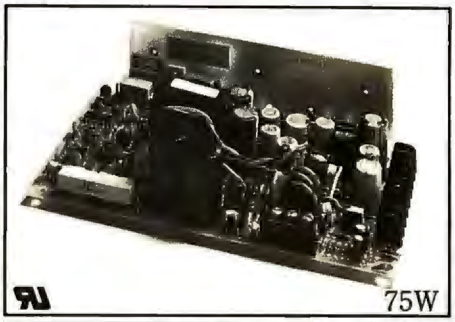

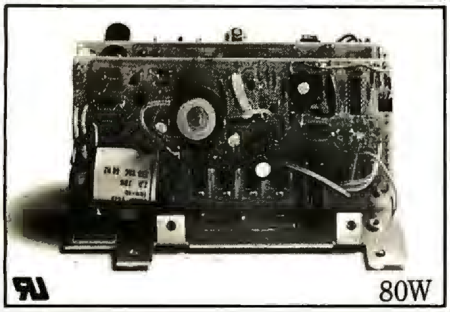

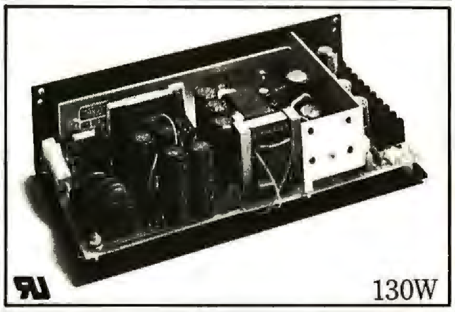

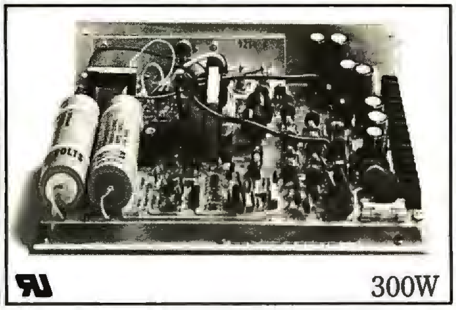

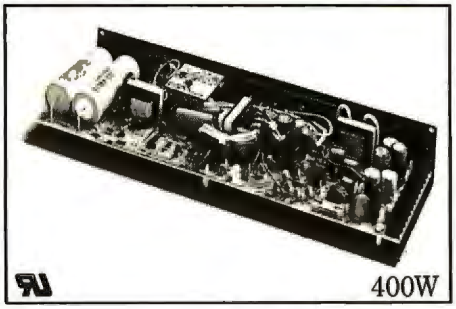

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My TRS-80 Talks to My Cromemco Z-2

Rod Hallen
Road Runner Ranch
POB 73
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Business computers communicate with each other all of the time. This is true whether they are located in adjacent rooms or halfway around the world from each other. You may ask, "Why can't personal computers communicate in the same manner?" Well, they can, and an intercomputer communications scheme is not really that difficult to implement.

I have owned as many as five personal computers at one time, but presently I'm concentrating on my Cromemco Z-2 and Radio Shack TRS-80. My Z-2 is used for word-processing and assembly-language program development; I bought the TRS-80 because it is the most popular machine on the market, and I want to write about the hardware and software for a large number of readers.

The Z-2 supports two ThinkerToys DISCUS 8-inch floppy disks, a fast Malibu 160 line printer, and a lot of other S-100 hardware, using software oriented to the CP/M operating system. The TRS-80 is a 16 K Level II machine with only one peripheral. That peripheral device is the Z-2, and therein lies my story.

Peripheral Devices

It doesn't take personal-computer enthusiasts long to find out that they will very quickly have more money invested in peripherals than in computers. In fact the computer itself is often the least expensive item. This is especially true for systems using printers and mass storage.

Good printers aren't cheap; neither are floppy-disk drives. And yet, the serious experimenter will want both. There are cases, such as mine, where peripherals are needed for two computers. Duplication of peripherals is not a cost-effective solution.

Since the Z-2 already supported everything I needed for the TRS-80, my first thought was about some sort of switching arrangement. This would have allowed the flip of a switch to transfer control of the printer and disks between computers. This sounds like a reasonable solution until you consider the actual implementation. My printer uses two parallel input/output (I/O) ports, and the disk system is oriented for the S-100 bus. Obviously, this means that nearly one hundred signal lines must be controlled. If both ports had been serial RS-232 types, the task might have been possible.

My major need was for hard-copy printouts of TRS-80 programs. It didn't take long to arrive at the idea of simply sending the program listings to the Z-2 and letting the Cromemco machine handle the printing. This scheme turned out to be much simpler than I had anticipated.

Although what follows is a design to interface these two particular computers, I have also included some hints about adapting this scheme to fit almost any situation.

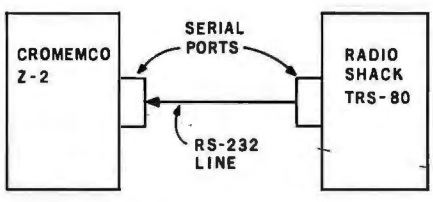

Figure 1: *This block diagram of the intercomputer communications channel shows one-way data transfer from the TRS-80 to the Z-2. With the appropriate modifications, the same scheme can be used for other systems.*

Theory

Figure 1 shows how the two computers are tied together. At the present time, the RS-232 line works in only one direction, from TRS-80 to Z-2. This is because the TRS-80 serial port was originally intended to drive a printer and is not configured to receive. However, it does contain most of the receiver components, which suggests an interesting follow-up project.

First, let us look at the data transmission *from* the TRS-80. TRS-80 Level II BASIC has two statements, LPRINT and LLIST, which are designed to send information to a printer. Both are similar in operation to PRINT and LIST. The TRS-80 maps the printer I/O port into memory address space as hexadecimal location 37E8. When LLIST or LPRINT is used as a command, the information referred to will be sent to hexadecimal memory address 37E8.

The TRS-80 serial interface must accomplish two things. First, it must decode the printer port address and let the microprocessor know when the next character can be sent. In addition, it must provide parallel-to-serial conversion because I had decided that the communications between the two machines would use the RS-232 format.

Once I had temporarily interfaced an IBM Selectric typewriter and a Teletype Model 43 to the TRS-80, so I already had the required serial printer port. The Radio Shack RS-232 board, which mounts in the expansion inter-

face, could be used instead.

I set the data-transfer rate at 2400 bps, which is the fastest that my port will run. I have also tried programming the Z-2 to display data as it is received. Unfortunately, 2400 bps is too fast to allow both storing and displaying of the data, so some characters are lost. I have written a routine for the Z-2 which sends incoming data directly to the printer, but I have found it preferable to make a disk file. This allows me to print as many copies as necessary.

Although no software changes of any kind are needed in the TRS-80, the Z-2 must be able to tell when characters are being sent to it and also what it should do with them. The program in listing 1, which I call TRSZ2, continually reads the input port which is being fed with data by the TRS-80. The characters thusly detected are stored in consecutive memory locations starting at hexadecimal 0100.

TRSZ2 is written in 8080 assembly language because it was originally intended for my computer which preceded the Z-2. It may be possible to improve the efficiency of this routine by using some Z80 instructions, but the limiting factor is still the RS-232-channel transfer rate, so not much would be gained. I hope the 8080 code will be useful to a greater number of readers than any Z80 version.

The TRS-80 does not output a line-feed character after each carriage return because line feeds are inserted automatically by the Radio Shack line printer (ie: the Centronics 779). TRSZ2 must also monitor the data as it is received to add a line feed after each carriage return.

The Z-2 also needs some way to determine when the transmission is concluded. At the end of each TRS-80 program which is to be sent to the Z-2, I add a shift-@ character (hexadecimal 60). When the Z-2 reads the shift-@, the operation is terminated.

Since listing 1 was designed to be used in a CP/M environment, it also performs two other functions. First, a CP/M end-of-file (EOF) character must be added to mark the end of the program stored in memory. CP/M recognizes hexadecimal 1A as the EOF. Second, CP/M requires that we tell it how many memory pages (ie: groups of 256 bytes) a program occupies before it is saved on disk.

This latter function is accomplished by converting the most significant byte of the storage pointer into two hexadecimal digits. As an example, suppose that the H and L registers contain hexadecimal 0A52 when listing 1 finds the end of the TRS-80 program. Since our storage area starts at hexadecimal address 0100, we have stored hexadecimal 0952 bytes of data (0A52 − 100 = 0952), which is more than nine pages and less than ten. CP/M does not consider partial pages, so we round up to the next integer. The H register contains hexadecimal 0A, which is decimal 10.

In the TRSZ2 routine, TEST and TABLE are used to convert the hexadecimal characters to ASCII, and the result is then sent to the screen one character at a time, followed by the message "H PAGES". At this point, in our example, the screen displays "0AH PAGES", and control is returned to CP/M. The transferred data may then be saved on disk by entering the proper CP/M commands.

Once a TRS-80 program has been stored on a CP/M disk, it is necessary only to call a print routine to get a hard copy. I have two ways to do this. If I type a control-P and then enter "TYPE FILENAME. TAB", the entire program will be listed on my printer. TYPE is a CP/M command which sends the specified file to the screen or to the screen and the printer, depending upon whether control-P has been toggled.

The TYPE command has one serious drawback: it does not take page length into account, and it prints continuously until the file has been completely listed. From the CP/M Users Group, I have obtained a program called PRINT which divides a listing up into pages of any desired length, and then titles and numbers each page. The address for the CP/M Users Group is given in a box near the end of this article.

Implementation

The procedure I usually follow is:

1. Write or load the TRS-80 program.

Text continued on page 94

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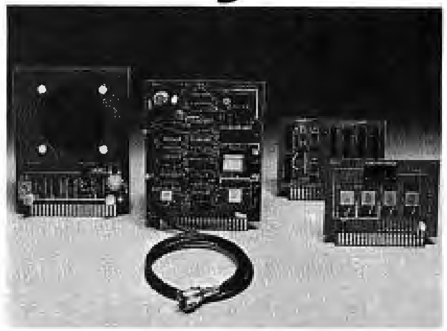

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Circle 58 on inquiry card.

Listing 1: *This routine, called TRSZ2, allows the Cromemco Z-2 to continually read the serial RS-232 input port. Most transfers are completed in a short time.*

```
                    ;*******************************************
                    ;* Z-2 PROGRAM TO READ DATA FROM SERIAL    *
                    ;* PORT 9 (CI-812) AND LOAD IT STARTING AT *
                    ;* 1ØØH FOR DISK SAVE.  OBJECT:            *
                    ;* COMMUNICATIONS WITH THE TRS-8Ø !        *
                    ;*                                         *
                    ;* ROD HALLEN  BOX 73 TOMBSTONE, AZ 85638  *
                    ;* REVISED  SATURDAY  9 JUNE 1979          *
                    ;*******************************************
                    ;
D7ØØ                        ORG     ØD7ØØH  ;LOAD ADDRESS OF PROG
Ø1ØØ =              BEGIN   EQU     1ØØH    ;STORAGE AREA
ØØØ8 =              SPSTAT  EQU     8       ;SERIAL PORT STATUS
ØØ4Ø =              MASK    EQU     4ØH     ;BIT 6 MASK
ØØØ9 =              SPDATA  EQU     9       ;SERIAL PORT DATA
F8Ø3 =              SCREEN  EQU     ØF8Ø3H  ;VIO ENTRY POINT
ØØØØ =              BOOT    EQU     Ø       ;CP/M WARM START
                    ;
D7ØØ 21ØØØ1                 LXI     H,BEGIN ;POINT TO STORAGE
D7Ø3 DBØ8           LOOP    IN      SPSTAT  ;GET STATUS PORT
D7Ø5 E64Ø                   ANI     MASK    ;CHECK BIT 6
D7Ø7 CAØ3D7                 JZ      LOOP    ;IF NO CHAR, DO AGAIN
D7ØA DBØ9                   IN      SPDATA  ;GET DATA PORT
D7ØC E67F                   ANI     7FH     ;RESET BIT 7
D7ØE FE6Ø                   CPI     6ØH     ;IS IT THE END?
D71Ø CA21D7                 JZ      EXIT    ;IF SO WE'RE DONE
D713 FEØD                   CPI     ØDH     ;IS IT A CR?
D715 C21CD7                 JNZ     LOAD    ;IF NOT, STORE IT
D718 77                     MOV     M,A     ;STORE CR
D719 23                     INX     H       ;POINT NEXT STORAGE LOC
D71A 3EØA                   MVI     A,ØAH   ;LOAD LF
D71C 77             LOAD    MOV     M,A     ;STORE IT
D71D 23                     INX     H       ;POINT NEXT STORAGE LOC
D71E C3Ø3D7                 JMP     LOOP    ;GET ANOTHER CHAR
                    ;
D721 36ØD           EXIT    MVI     M,ØDH   ;STORE CR
D723 23                     INX     H       ;POINT NEXT STORAGE LOC
D724 36ØA                   MVI     M,ØAH   ;STORE LF
D726 23                     INX     H       ;POINT NEXT STORAGE LOC
D727 361A                   MVI     M,1AH   ;STORE CP/M EOF
                    ;
D729 3EØD           ADDR    MVI     A,ØDH   ;LOAD CR
D72B CDØ3F8                 CALL    SCREEN  ;OUT TO VIDEO
D72E 3EØA                   MVI     A,ØAH   ;LOAD LF
D73Ø CDØ3F8                 CALL    SCREEN  ;OUT TO VIDEO
D733 EB                     XCHG            ;STORAGE POINTER TO DE
D734 7A                     MOV     A,D     ;GET MS BYTE
D735 E6FØ                   ANI     ØFØH    ;RESET BITS Ø-3
D737 ØF                     RRC             ;MOVE RIGHT 4 BITS
D738 ØF                     RRC             ;  "
D739 ØF                     RRC             ;  "
D73A ØF                     RRC             ;  "
D73B CD55D7                 CALL    TEST    ;FIG FIRST CHAR
D73E 7A                     MOV     A,D     ;GET MS BYTE AGAIN
D73F E6ØF                   ANI     ØFH     ;RESET BITS 4-7
D741 CD55D7                 CALL    TEST    ;FIG SECOND CHAR
D744 2186D7                 LXI     H,MSG1  ;POINT TO MESSAGE
D747 Ø6Ø9                   MVI     B,9     ;MESSAGE LENGTH
                    ;
D749 7E             MSG     MOV     A,M     ;GET CHARACTER
D74A CDØ3F8                 CALL    SCREEN  ;OUT TO VIDEO
D74D 23                     INX     H       ;INCREMENT MSG1 ADDRESS
D74E Ø5                     DCR     B       ;DECREMENT CHAR COUNT
D74F C249D7                 JNZ     MSG     ;GO GET ANOTHER
                    ;
D752 C3ØØØØ                 JMP     BOOT
                    ;
D755 2166D7         TEST    LXI     H,TABLE ;POINT TO TABLE
D758 BE             TEST1   CMP     M       ;DO THEY MATCH?
D759 23                     INX     H       ;INCREMENT TABLE
D75A C262D7                 JNZ     TEST2   ;NZ=NO MATCH
D75D 7E                     MOV     A,M     ;CHAR TO A
D75E CDØ3F8                 CALL    SCREEN  ;AND OUT TO SCREEN
D761 C9                     RET
D762 23             TEST2   INX     H       ;INCREMENT TABLE
D763 C358D7                 JMP     TEST1   ;NEXT CHAR
                    ;
D766 ØØ3ØØ131       TABLE   DB      Ø,3ØH,1,31H         ;CHARS IN ODD POSITIONS
D76A Ø232Ø333               DB      2,32H,3,33H         ;ARE HEX AND THE EVEN
D76E Ø434Ø535               DB      4,34H,5,35H         ;POSITIONS ARE THE
D772 Ø636Ø737               DB      6,36H,7,37H         ;ASCII EQUIVALENTS
D776 Ø838Ø939               DB      8,38H,9,39H         ;
D77A ØA41ØB42               DB      ØAH,41H,ØBH,42H     ;
D77E ØC43ØD44               DB      ØCH,43H,ØDH,44H     ;
D782 ØE45ØF46               DB      ØEH,45H,ØFH,46H     ;
                    ;
D786 48205Ø         MSG1    DB      48H,2ØH,5ØH         ;H,SP,P
D789 414745                 DB      41H,47H,45H         ;A,G,E
D78C 53ØDØA                 DB      53H,ØDH,ØAH         ;S,CR,LF

D78F                        END
```

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DIGITAL RESEARCH

Text continued from page 90:

2. Append shift-@ to the TRS-80 program.
3. Load TRSZ2 in the Z-2 and execute.
4. LLIST the TRS-80 program.
5. SAVE *XX* pages on Z-2.
6. PRINT resulting file.

The actual transfer happens very rapidly because of the speed of the RS-232 interface, the disks, and the printer.

Under CP/M, TRSZ2 can be loaded and executed in two different ways. After TRSZ2.ASM has been assembled, the file TRSZ2.HEX will reside on the disk. Typing "DDT TRSZ2.HEX" will load it starting at hexadecimal location D700, and then "GD700" will execute it. TRSZ2 loops continually until characters are detected at the input serial port.

As a preferred alternative, I have a utility routine from the CP/M Users Group called MOVDOWN which greatly simplifies this process. I have modified MOVDOWN so that any program which does not execute at the normal CP/M hexadecimal address of hexadecimal 0100 can be loaded and executed in the same way as any CP/M command file. My modified routine is called MOVUP.

Other Computers

The basic principles discussed so far will work with other computers, but of course there are some detail changes that must be made. The most important consideration is the availability of a serial I/O port intended for a printer or other peripheral device. The main difference of using a serial port for intercomputer communications, when compared to the usual serial-port peripherals, is the high data-transfer rate possible.

For the receiving end, a great amount of flexibility is possible. When setting up the system, I picked hexadecimal D700 as the location for TRSZ2 because this is free memory outside of the CP/M operating area. I set my CP/M system size at 4 K bytes less than the available user memory to leave room for programs such as this, my printer-driver routine, and others that must run undisturbed during the normal operation of CP/M.

Note that in listing 1, BEGIN is given the hexadecimal value 0100. This is the beginning of the text storage area, purely an arbitrary choice. I selected 0100 since it is the start of CP/M's disk-SAVE area.

SPSTAT is set to port 8 to indicate the status of my serial port. Whenever bit 6 is nonzero (tested by ANI MASK), a character is ready, and the next step is to read the serial data port (ie: SPDATA EQU 9). The received character is then stored in the memory location pointed to by the H and L registers. Bit masks and ports should be changed to match your particular configuration.

SCREEN defines the output port as my IMSAI VIO-C video interface board. Whenever location F803 is called, the character which is in the A register will appear on the screen. Finally, BOOT calls hexadecimal address 0000, which is the reentry point for CP/M. Substitute your monitor entry point if you are not running CP/M.

On non-CP/M systems you will, of course, need to use whatever tape- or disk-saving procedures are available to you. If this is difficult or undesirable, you might rewrite TRSZ2 so that it sends each character directly to the printer as it is received. In this case, the data-transfer rate must be adjusted to accommodate the slower peripheral device.

Flexibility

While the ability of the Cromemco Z-2 system to provide hard copy for the TRS-80 is a useful and economical feature, there are also many other advantages.

On the Z-2 I am using Microsoft Extended Disk BASIC which will accept TRS-80 Level II programs, except for a few statements. The reverse is also true. It is possible and desirable to write a program on one machine, then send it to the other for whatever modification is necessary. The Z-2 also runs a Z80 assembler and debugger, which could be used to generate assembly-language programs for the TRS-80. All of these will result in enormous flexibility of software design and utilization. ■

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Communicating in Two Directions

Mark R Titchener
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With the prices of microcomputer components becoming ever more attractive, the temptation to sprinkle terminals and peripherals throughout the house is becoming more difficult to resist. Since a computer is more flexible than a telephone, it's not unreasonable to have a bedside terminal (that wakes you in the morning and reminds you of your appointment with the dentist), a terminal in the study for serious work, another remote terminal in the den for the kids to play with safely, and the main system residing in the basement workshop.

The simultaneous and independent transmission of signals in opposing directions through a single line, as discussed here, has been done for years in communications systems (such as telephone links). I have not seen it applied to remote terminals or processors, so I present the idea along with some obvious applications.

Theory of Matching Bridges

In most systems the transmitters are simple current sources which, in the case of digital transmission, are switched *on* or *off*. Reception of the signals can be made by detecting the presence of a voltage across the nodes of a bridge, as shown in figure 1.

In order for the output signal to be unaffected by the local transmitter, the bridge must be balanced. For a transmission line to handle data without reflection problems, the bridge network must *terminate* the line with an impedance that closely matches the line's impedance. By definition, the impedance of an ideal current source is infinite; but the receiver impedance must also be high. If the receiver draws too much current, it will affect the bridge balance and impedance.

From the two conditions shown along with figure 1, it is a simple matter to derive the values R_1 and R_2, in terms of the characteristic impedance R_0. The relations derived are:

$$R_2 = 2\ R_0$$
$$R_1 = \tfrac{2}{3}\ R_0$$

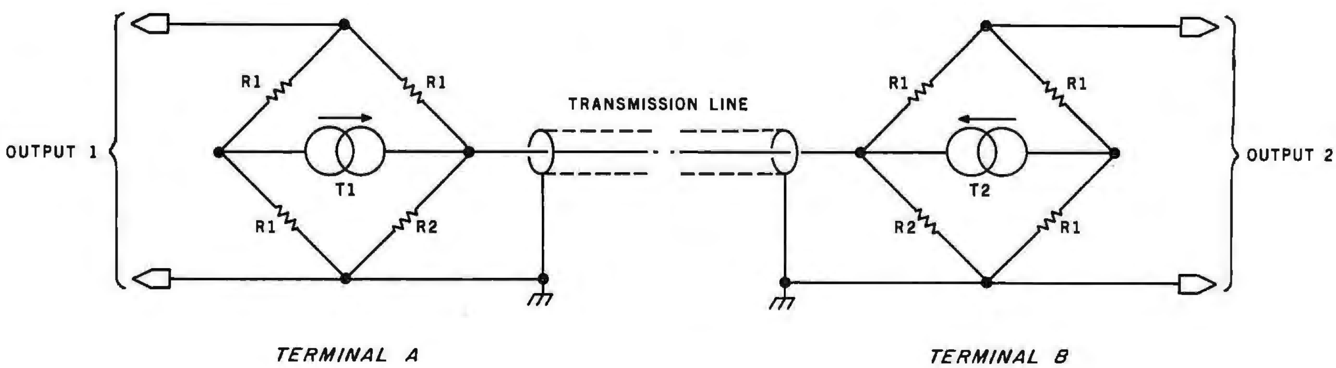


Figure 1: *The fundamental transmission scheme. T1 and T2 are current sources (ie: transmitters) which may be either on or off. Proper termination of the transmission line is accomplished by the selection of bridge impedances to fit the equation:*

$$\frac{1}{R_0} = \frac{1}{R_2} + \frac{1}{3\ R_1}$$

where R_0 is the impedance of the transmission line. Solving this equation simultaneously with the bridge balancing equation:

$$\frac{1}{R_1} = \frac{1}{R_0} + \frac{1}{R_2}$$

gives the exact resistance values required.

Circle 63 on inquiry card.

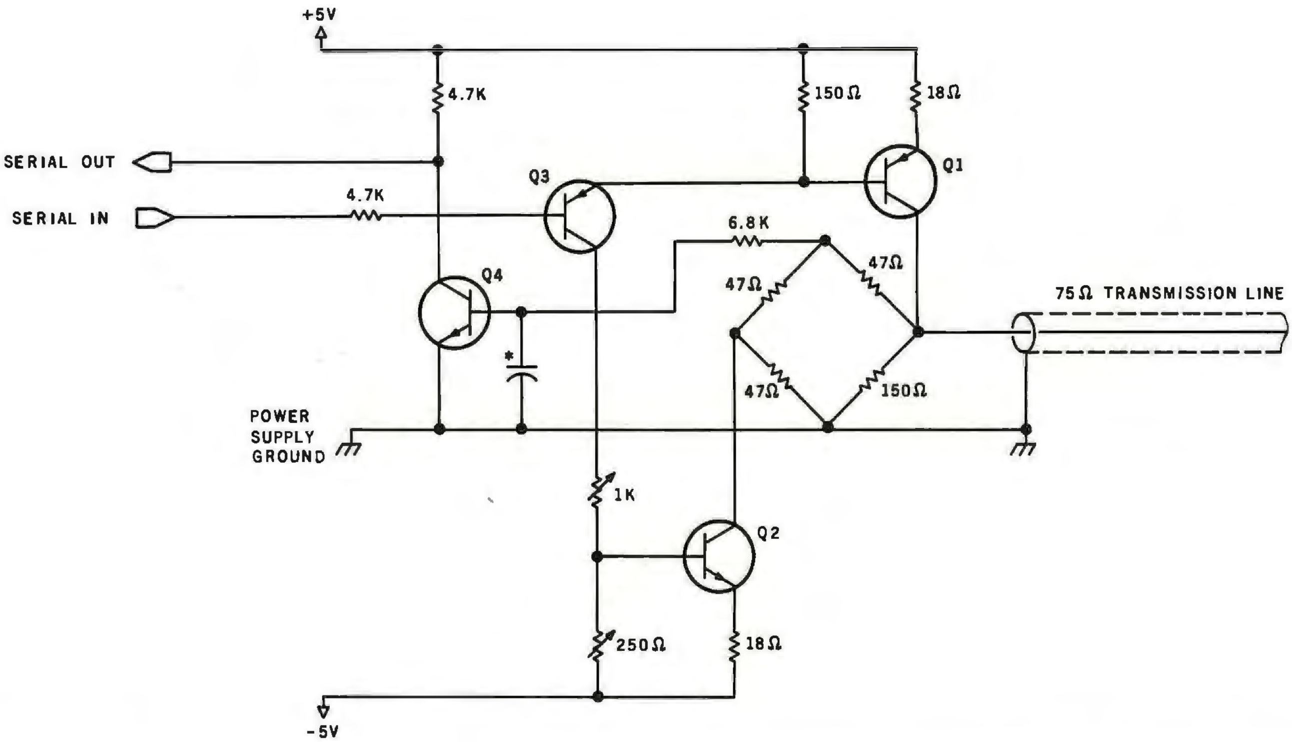


Figure 2: *Typical bidirectional line-driver circuit designed for a 75-ohm transmission line. Capacitor marked with an asterisk has a value determined by the data-transfer rate. (See text.)*

For 75-ohm coaxial line, the values R_2 = 150 ohms and R_1 = 47 ohms would be about right. Slight imbalance in the bridge may be corrected as will be described lat'r. The impedance of the bridge and cable combination is effectively 73 ohms. It is obvious that some variation may be introduced by the tolerance of the resistors, so you may have to choose the resistors carefully.

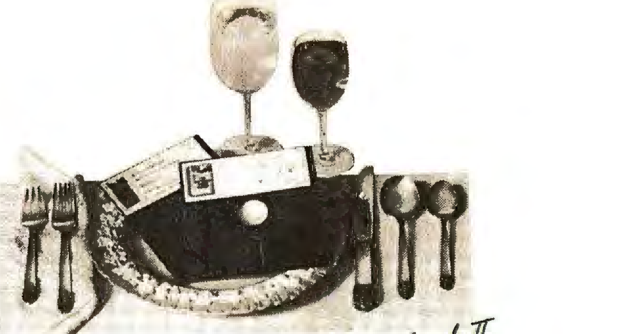
The Transmitter/Receiver Circuit

With this configuration in mind, some other arbitrary specifications of the circuit can be chosen. The components specified in figure 2 will be unsuitable for cable impedances other than 75 ohms. The supply voltages were selected as those most likely to be available from the processor or terminal with which the circuit is to be used. In electrically noisy environments, it may be necessary to use higher transmission voltages to hide the interference, in which case higher supply voltages will be required.

Using the 5 V supply, about 2 V is left as a suitable transmission voltage after biasing transistors Q1 and Q2. (The transmission voltage actually varies depending on whether both

Circle 65 on inquiry card.

No.13: Gourmet Goodies



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*Software consists of the operating system, text editor, assembler, debugger and other utilities for file management and system maintenance. Complete set of Digital Research's documentation and additional implementation notes included. Systems marked * and ** include firmware on 2708 and 2716. Systems marked + include $440 media charge. Systems marked Ⓜ require the special Ⓜ versions of software in this catalog. Systems marked v have minor variants available to suit console interface of system. ◊ Includes hardware addition to allow our standard versions of software to run under it. Call or write for full list of options.*

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transmitters T1 and T2 are in their *on* state.)

When a high input level causes Q3 to conduct, about 10 mA of current flows through the base resistors of Q1 and Q2. This biases each base at about 1.5 V with respect to the corresponding supply rails and defines the emitter resistor voltages at Q1 and Q2 to be 1 V. Thus, with a high input level, about 50 mA will be available from the collectors of Q1 and Q2. The two collectors of these transistors form the source and sink of the current transmitters, T1 and T2, shown in figure 1.

With the resistances given for R_1 and R_2, the voltage developed by the current source T1 is about 2 V at the cable. If the current sources at each end of the line are in the *on* state, this voltage rises to about 3.6 V. However, the voltage sensed by each receiver is about 1.2 to 1.3 V, with very little variation. When both T1 and T2 are on, no current flows in the transmission line.

The transistor Q4 is switched through a 6.8 k-ohm resistor which limits the base current to about 0.1 mA. This provides ample current for switching the output, and the 6.8 k-ohm resistor is of sufficiently high impedance to be ignored in the bridge balance and cable termination calculations. The output at the collector of Q4 is transistor-transistor-logic (TTL) compatible as is the input at the base of Q3.

The balance of the current source and current sink is crucial to good performance, and is adjusted using the 250-ohm potentiometer at the base of Q2. The 1 k-ohm bias-current control, used in setting up the base voltages of Q1 and Q2, should be adjusted to give 2 V at the cable connection. It will be found that this adjustment is not entirely independent of the balance adjustment; it may be necessary to readjust each to obtain proper operation.

Some immunity to noise and to the glitches produced by slight imbalance in the switching characteristics of Q1 and Q2 is given by the capacitor at the base of Q4. This value should be calculated to filter any frequencies greater than the third harmonic of the chosen data rate. The appropriate formula is:

$$c = \frac{1}{188f}$$

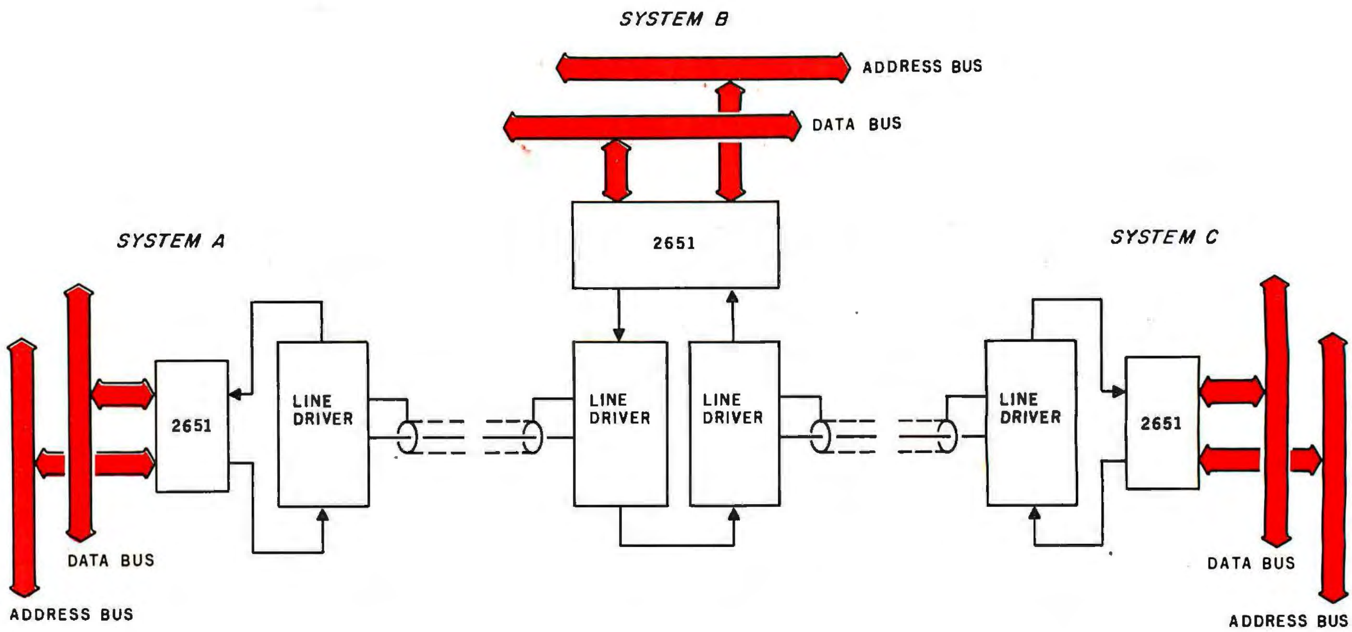

Figure 3: *Simple-ring network of three systems.*

where *c* is in farads and *f* is in bits per second.

Parallel-to-Serial Conversion

The output and input lines of this line driver may be directly coupled to the serial lines of a universal asynchronous receiver/transmitter (UART). Thus a simple link consisting of a single coaxial cable can connect a peripheral to the parallel port of the main system. This is possibly the simplest way to use such a scheme. However, in more sophisticated networks, some other arrangements are advantageous.

Ring Networks

The networks described next assume some degree of intelligence in each system, because the simplicity of the transmission system is reflected in the need for some software monitoring. The UART is not particularly well suited for these configurations, so interfacing may be better achieved with an integrated circuit such as the Signetics 2651 peripheral communications adapter (PCI). The features of this circuit include:

- simultaneous operation of transmitter and receiver
- synchronous or asynchronous transmission
- characters may be from 5 to 8 bits wide
- automatic, serial echo mode
- internal data-rate generator with sixteen common rates
- error detection
- single 5 V power supply required

In figure 3, the simple ring network of three systems is reduced to a linear configuration. The ring need not be limited to three systems, but may form the basis of a simple network where each office or room might be equipped with a terminal. Using this scheme, the data is shunted around the ring from one system to the next until its destination is reached. The 2651 then signals a flag to the system involved and the automatic echo mode is ceased. The incoming data block is diverted to the system's memory while fill characters (synchronous idle, SYN, or data-link escape, DLE) are substituted onto the ring, indicating that the line is free. When the block transfer has been completed, the 2651 will return to its automatic echo mode, thus allowing following data to circulate on the ring.

With this configuration, some flexibility is available in the initial wiring of the ring. The order of the systems within the network is not necessarily dictated by their physical locations. Each system, apart from the two end ones, may intercept the data passing in either of two directions. Thus if certain pairs are more often in communication, their placement may be arranged for greatest efficiency.

In figure 4 (see page 106), a somewhat more sophisticated system is shown. This time the physical linking of the systems is continued until a loop has been formed. Each system is now connected to the loop via two 2651s and has access to data circulating in either of two directions. The performance of such a network will depend largely on the sophistication of the associated software, but the possibilities are exciting.

The network might be described as being a *reconfigurable dual-ring network*, which enables simultaneous conversations between two or more pairs of systems, depending on their relative placement on the loop. If we consider any two systems, we see that one of four different conversation loops may be chosen (see figure 5, page 106); either one of the two rings may be used independently, or one of the two possible loops formed as a combination of the two data rings may be used.

At this point I sense that we may be beyond the reasonable, in terms of the experimenter's immediate interests. However, I believe these ideas may in one form or another stimulate thoughts on the subject from fellow BYTE readers. ■

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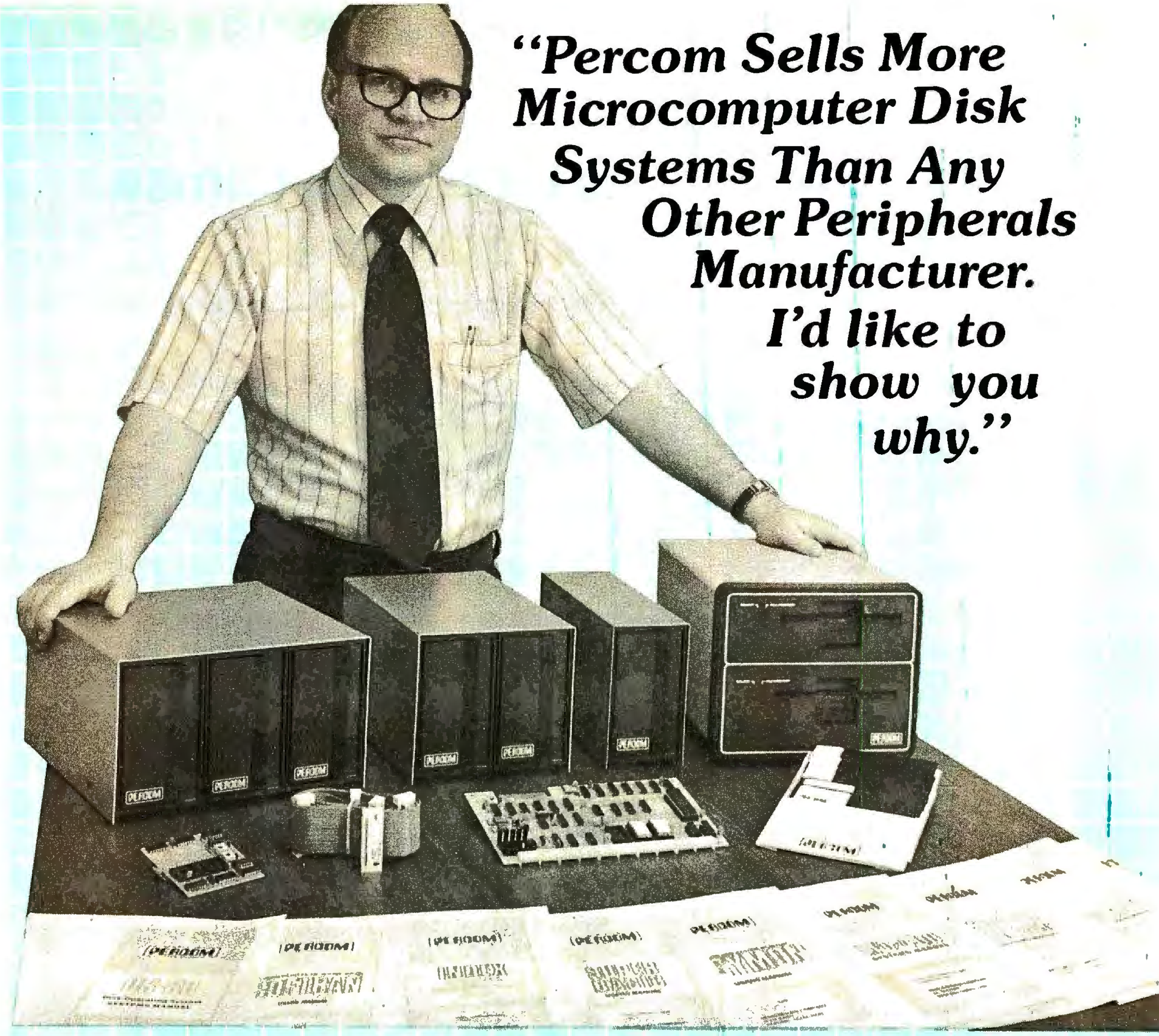

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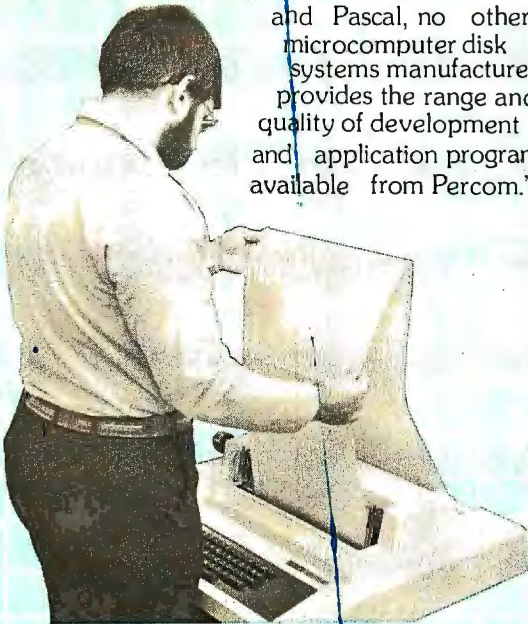

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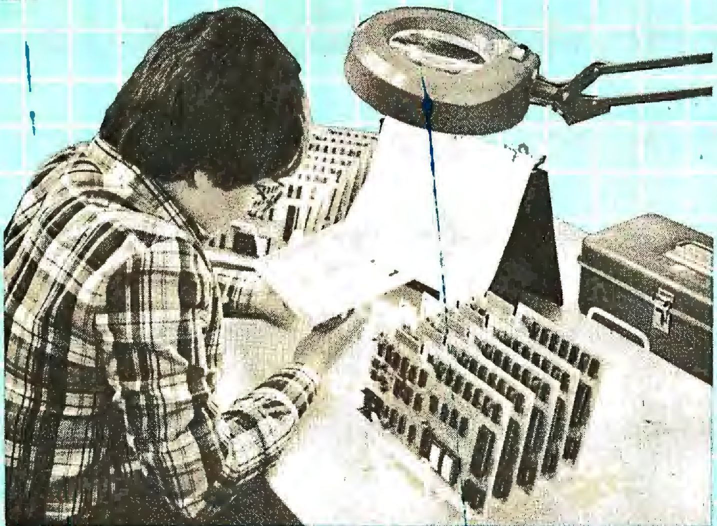

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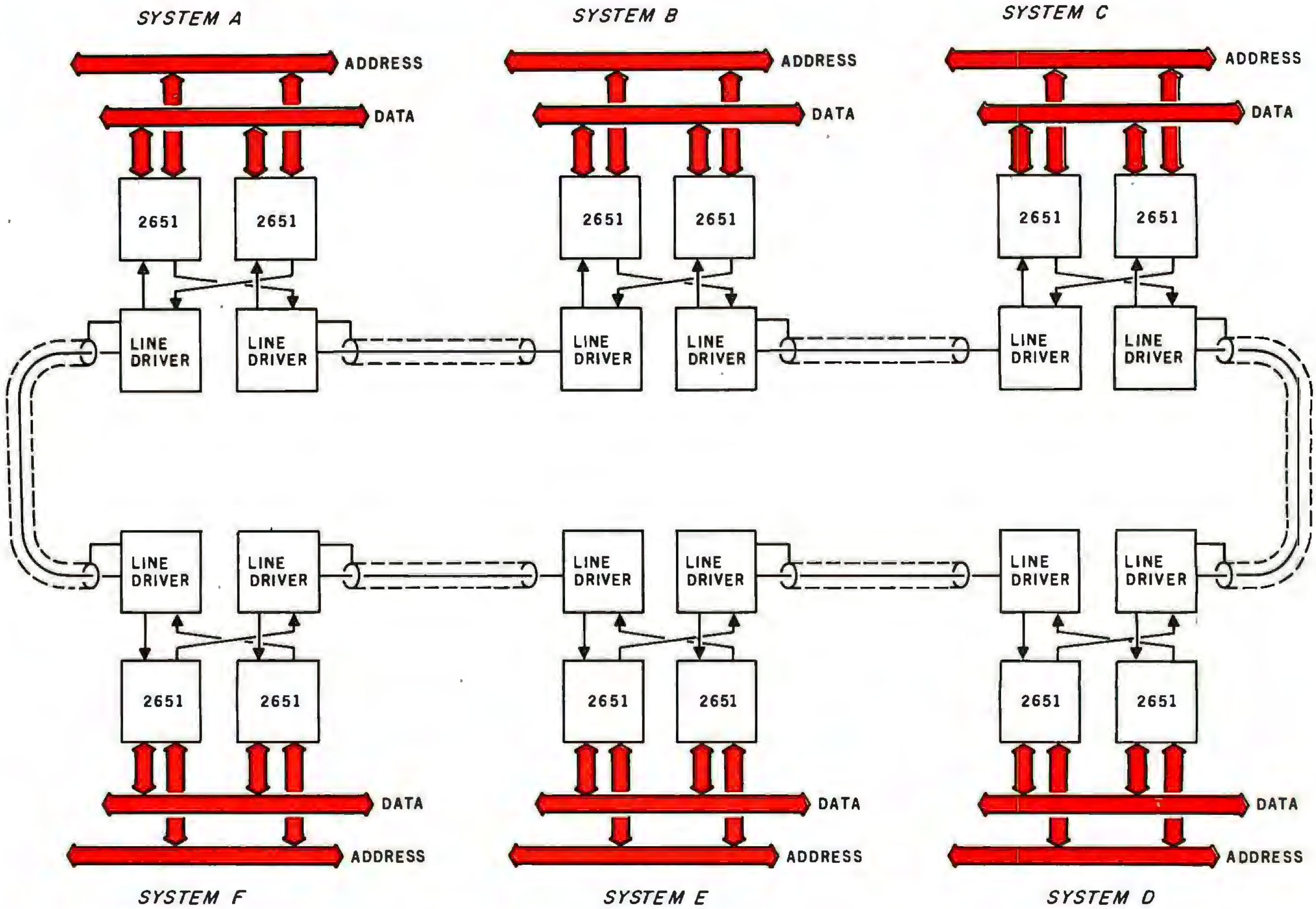

Figure 4: *Dual-ring network of six systems. Each system has access to data which may circulate in either direction.*

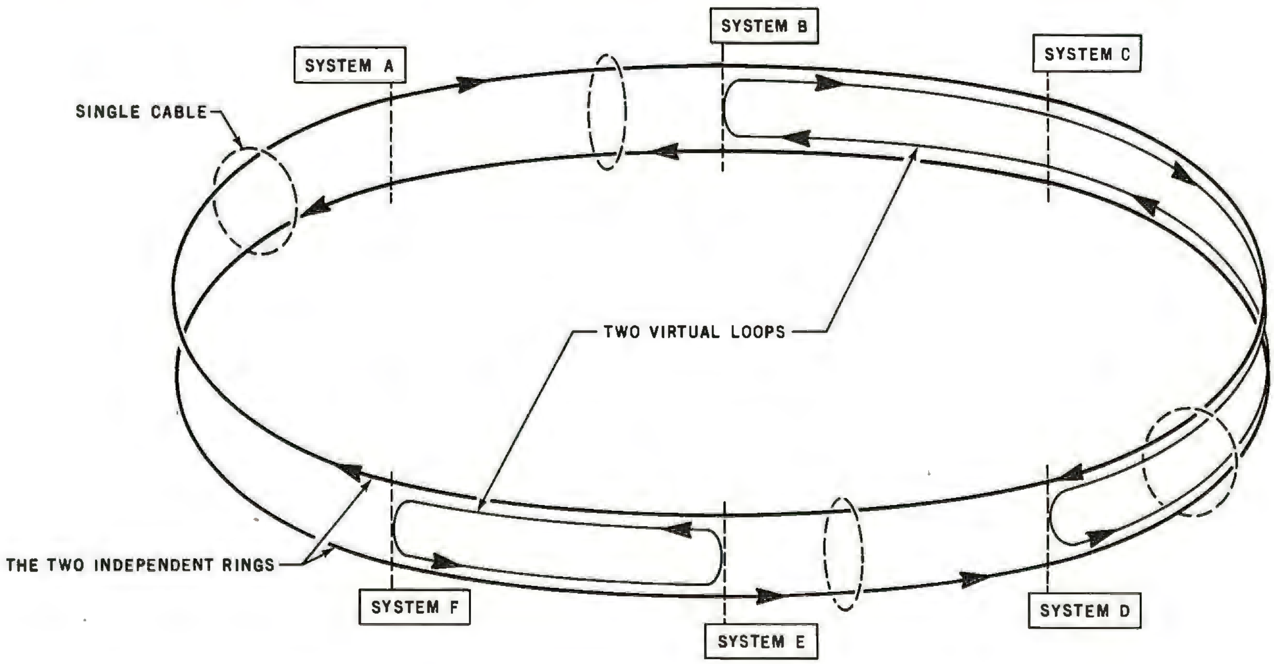

Figure 5: *Possible communications links using the dual-ring network.*

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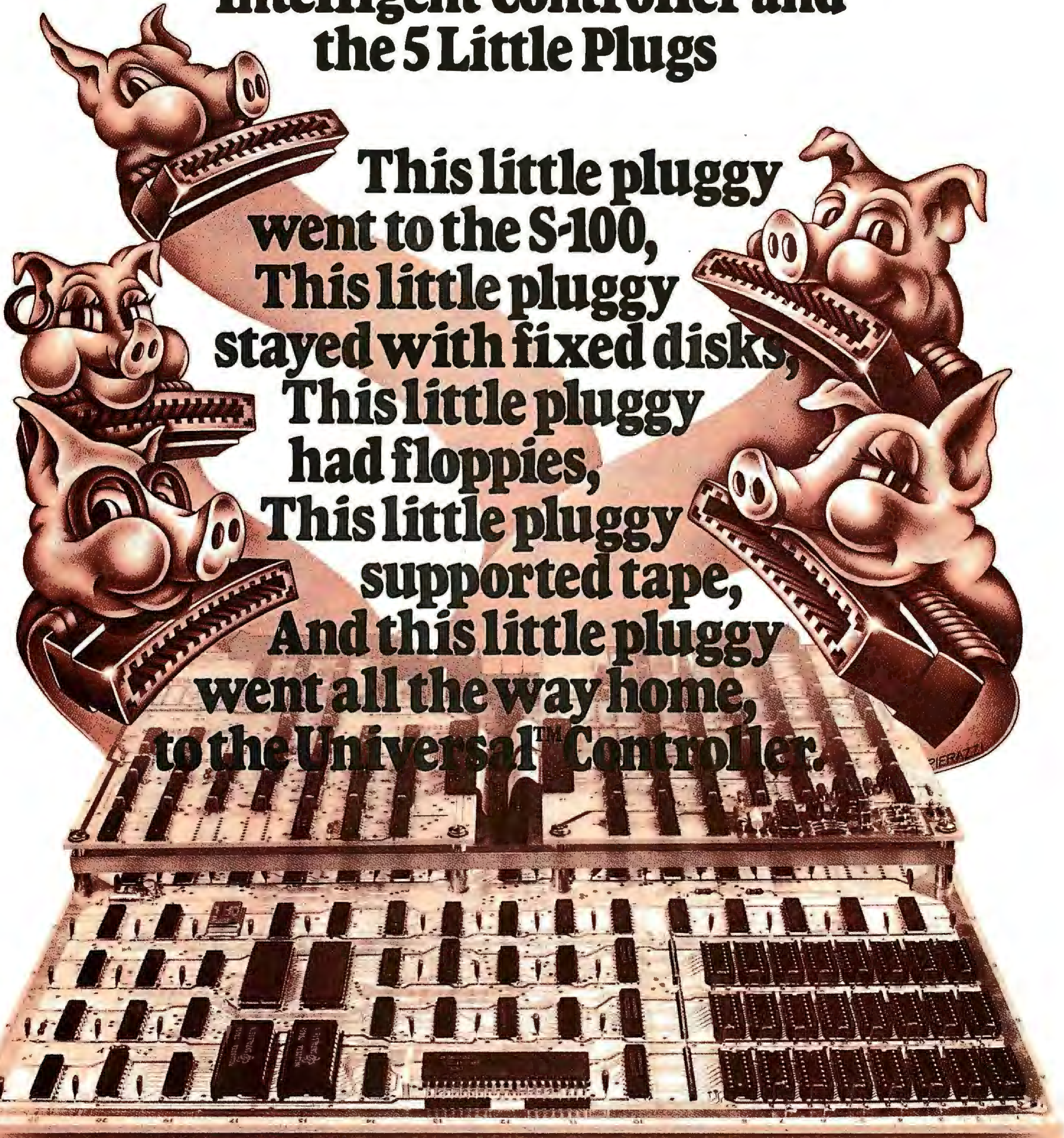

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Understanding ISAM

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More and more microcomputer systems are advertised as featuring ISAM files. The *indexed-sequential access method (ISAM)* permits rapid access to large amounts of data and is well suited to disk storage. However, ISAM does have some disadvantages. This article is intended to enable the personal-computer user to understand what ISAM is, how it works, and how to tell if the indexed-sequential access method is appropriate for a given application.

A brief look at two other access methods will be a helpful prelude to describing ISAM. *Sequential access* is the most common method for reading files, and it is easily understood. Records of a sequential file are accessed one after another in the order in which they are physically stored. The records are located adjacent to each other on the storage device.

In the *random-access* method, records are read or written via a unique *key* associated with each record. This key translates into a physical address—that is, the address in the storage device that contains both the specified key and its associated data. Here, the records are not necessarily located next to each other; they tend to be scattered over the storage area. Figure 1 shows the same file of three entries stored in both a random and a sequential manner.

The major problem with sequential files is speed. To obtain the one hundredth item from a sequential file, it is necessary to first read the preceding ninety-nine records. If the program makes a lot of unordered accesses to a sequential file, the response will be slow since the preceding records have to be read for each entry that is obtained. Events in the real world typically occur in an unordered manner. This means that the slow response time of a sequential file often precludes its use in real-time systems.

On the other hand, the advantage of the random-access file is speed. If the key of a record is known, we know exactly where to look for it. The programs can obtain any record in a random-access file with just one input/output (I/O) operation.

ISAM represents a compromise between the random- and sequential-access methods.

The problem with the random-access method for files is related to the size and composition of the record's key. Since there is a one-to-one correspondence between a key and a physical location, the storage medium must have a space available for every possible key value. If the key is a four-digit integer, that implies 9999 slots. However, if the key is a Social Security number, storage for 999,999,999 records would have to be allocated. (There are various randomizing or *hashing* techniques available to deal with this problem. See "Making Hash With Tables" by Terry Dollhoff, January 1977 BYTE, page 18, reprinted in the book *Program Design* from BYTE Books.)

ISAM represents a compromise between the random- and sequential-access methods. ISAM access is faster than sequential access but not as fast as random access. An ISAM file takes less storage than a random file but more storage than a sequential file.

Records in an ISAM file are stored adjacent to each other as they are in a sequential file, but the storage location of the individual record is not tied directly to the key of the record. (See figure 2.) Instead, data records (called *prime records*) are grouped together and stored as a *physical record*. The size of the physical record is the largest number of logical, prime records that will fit into a fundamental unit of mass storage (in a disk, this unit is called a *sector*). Along with each physical record, an *index* record is built that contains a pointer (address) to the physical record and the highest key value of any record within that physical record. In other words, the ISAM index file provides a means of translating from the key of a record to that record's physical location. (In most cases, use of the ISAM index file is made solely by the operating system so that the use is *transparent* to (unnoticed by) the program that is accessing the record "randomly.")

To clarify the previous general discussion, observe the following example. Suppose you are asked to maintain the membership data for a local computer club. Each member is assigned a unique three-digit membership number that can be used as a key for your file. After studying the data to be kept on each member, you determine that four records will fill a sector on the storage device. Records are updated regularly as the members pay their dues, added fairly often as the club grows, and deleted infrequently. There are currently seventy-two members, with membership numbers from 001 to 072.

In order to compare the three access methods, look at the storage space and I/O processing necessary

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```
{HANDLE A/D CONVERSION EVERY SECOND FOR 3 HOURS}
PROGRAM SAMPLER:
[*DEMONSTRATES THE POWER OF PASCAL/MT*]
CONST
  RTC___VECTOR=6; {FOR RTC___ISR}
TYPE
  TIME___OF___DAY = RECORD
                      HOURS      :  D..24;
                      MINUTES    :  0..60;
                      SECONDS    :  0..60
                           END;
VAR
  NOW: TIME___OF___DAY;
  SAMPLE: INTEGER;

PROCEDURE INCREMENT___ TIME___OF___DAY;
BEGIN
  . . . [*INCREMENTS NOW BY ONE SECOND*]
END;

PROCEOURE GET SAMPLE; {TALK TO A/O CONVERTER}
BEGIN
  SAMPLE: =INPUT [$3B]; {GET I/O PORT DATA}
  OUTPUT [$FA] = SHR [SAMPLE, 3]; {USE SHIFT RIGHT}
  WHILE TSTBIT [INPUT [$6C], 2] <> TRUE DO; {WAIT}
  INLINE [''LOA / $FOCO / ''STA / $309B]; {OJB CODE}
END;

PROCEDURE INTERRUPT [RTC___VECTOR] RTC___ISR;
BEGIN {INTERRUPT SERVICE ROUTINE}
  GET SAMPLE [* EVERY SECONO *]
  INCREMENT___ TIME___OF___DAY
END;

BEGIN
  NOW. SECONDS: = 0; NOW. MINUTES: = 0; NOW. HOURS: =0;
  INLINE [''MVI A, / $3E / ''SIM {8085}]; {START CLOCK}
  GET SAMPLE; {TAKE FIRST SAMPLE}
  WHILE NOW. HOURS <> 3 00; {SAMPLE FOR 3 HOURS}
END. {AT ENO RETURN TO OPERATING SYSTEM}
```

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for the following functions:

- Store the membership file.
- Update record 57.
- Add new member number 108.
- Delete record 12.
- Print a membership list for the entire club.

If the access method is sequential, the file will occupy eighteen sectors of storage (4 × 18 = 72). To read and then update record 57, the fifteenth sector must be obtained. When using a sequential-access method, the preceding fourteen sectors must be read, giving a total of fifteen read operations and one write operation. Adding a record past the current end of file entails first reading the entire data set (eighteen reads) and then executing a write. Deleting record 12 implies rewriting every record from record 13 to the end of the file. Since the point of deletion has to be read first, every sector is read, and sectors 13 thru 18 are written. Finally, printing a membership list simply involves eighteen read operations. (This data is summarized in table 1.)

Suppose you choose to access the membership file using a random-access file. Since the I/O package reads *sectors* from the disk, it will make a one-to-one correspondence between the sector of a record and a

Sequential File Address	Record Key	Record Data	Random File Address	Record Key	Record Data
001	003	DDDDDDDD	001	(empty)	
002	005	DDDDDDDD	002	(empty)	
003	007	DDDDDDDD	003	003	DDDDDDDD
004	(empty)		004	(empty)	
005	(empty)		005	005	DDDDDDDD
006	(empty)		006	(empty)	
007	(empty)		007	007	DDDDDDDD

Figure 1: *Data organization in sequential-access and random-access files. In a sequential file, data records are stored physically adjacent to each other; this saves storage space, but the entire file must be rewritten if a new record is inserted. In a random file, data records are stored with respect to the record's key. This requires a larger initial investment in storage space but allows new records to be inserted without rewriting the entire file.*

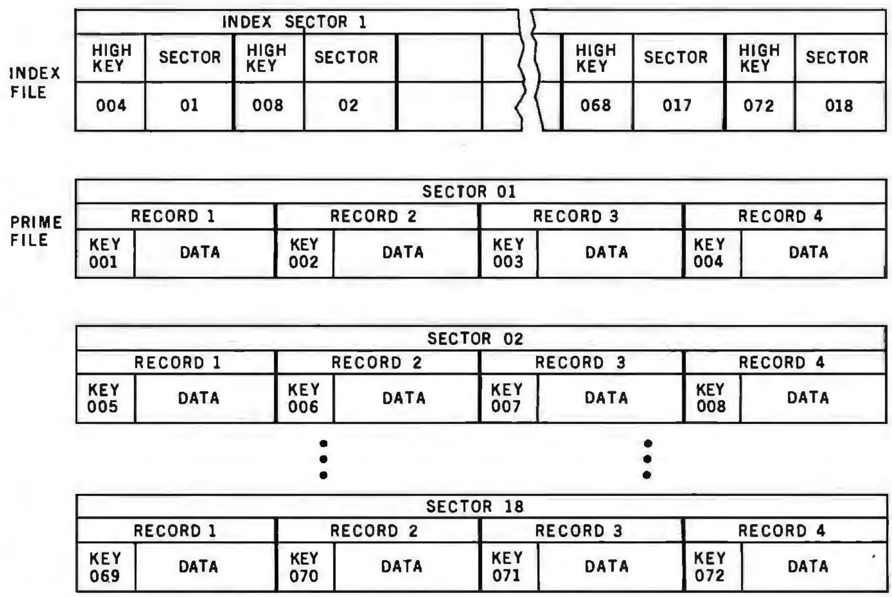

Figure 2: *Structure of an ISAM file. The ISAM file presented is actually two files. The prime file contains a series of contiguous physical records, each of which contains a number of logical records. (Here, one physical record equals one disk sector.) All the logical records contained within one physical record are in ascending-key sequence for the file. The second file, the index file, provides an index of physical records in ascending-key sequence. Together, these two files allow the ISAM file to be in ascending-key sequence without the use of the random-access method.*

person's membership number. This means that the random-access method will start by costing 999 sectors of storage, one sector for each possible membership number. Multiple records per sector are not possible with this addressing scheme, so 75% of each sector is unused (one sector could hold four records).

Once this price has been paid, the rest seems fairly simple. Reading record 57 costs the user one I/O operation, as does writing to update the record. The addition of record 108 takes just one write operation since the disk space is already there.

A deletion, though, raises some interesting questions for a random-access file. The sector cannot be eliminated from the disk, so it must be written over with a standard pattern to indicate that the slot is empty. This implies that the I/O package (or program) must recognize the pattern that indicates an empty record. Because all records are empty before the file is created, a formatting program must be run to create 999 empty records before the first real record can be added to the random file.

The use of random access also sets a physical limit to the size of the file — that is, to a maximum of 999 entries. Will the club ever grow beyond 999 members? If it does not, this approach is fine. But if there is a possibility of having more than 999 members in the club, the key size must be changed and the allocation for the random-access file must be increased to 9999 sectors.

Producing a membership list from this random file means that *every* sector in the data set must be read unless you know the highest key currently assigned. Even if you know that the highest key is 108, you will have to execute a minimum of 108 read operations. Again, these figures are given in table 1.

If ISAM is chosen as the access method, the records can be stored four to a sector (the content of a sector is sometimes called a *block*). However, you must build an index file to tie the record's key to its physical location. (A good I/O package will create the index file automatically.) Records in the index file will consist of the highest key from the records in a given sector and the physical address (or sector number) of that sector. There are only eighteen index records, since only eighteen sectors are needed to save seventy-two records. These eighteen sectors are called *prime blocks*. The index records are small enough to fit in one sector of the storage device.

Getting back to the evaluation questions in table 1, an update of record 57 involves reading the index (which can be done with one read operation), searching the index records until there is a high or equal compare, then reading the prime sector that corresponds to the sector number from the index. The sector from the prime file is then rewritten, but it is not necessary to update the index sector (which stays the same). Adding record 108 involves reading the index sector and updating it as well as writing a new prime sector. Record 12 is deleted by locating the logical record, writing over it with a predetermined pattern, and updating the corresponding index record so that it contains a high key value of 11. Printing a membership list calls for accessing the index and reading each of the eighteen prime sectors. A summary of these results for an ISAM file are given in table 1.

Most readers will notice that a situation where a new record is added between two existing records has not yet been discussed. This was done deliberately so that ISAM's basic features could be reviewed. Now we must look at *overflow*.

Overflow processing is unique to ISAM files and can cause a tremendous increase in the number of I/O operations necessary to access ISAM records. Since fast response time is one of the attractive features of ISAM, overflow will be discussed in some detail. (Please note that there are several ways to implement ISAM, all of which involve overflow processing of some kind. Although the guidelines that will be developed are based on a detailed consideration of one implementation, the general prin-

Characteristic	Sequential Access Method	Random Access Method	ISAM (Indexed-Sequential Access Method)
Number of sectors used for storage	18	999	19
Number of I/O operations to update record 57	16	2	3
Number of I/O operations to add record 108	19	1	3
Number of I/O operations to delete record 12	34	1	4
Number of I/O operations to print memberships lists	18	108	19
Software must be able to recognize a deleted record?	no	yes	yes
Must run disk formatting program?	no	yes	no
Maximum file size	device limit	999	device limit

Table 1: *Comparison of disk-access methods. Using the example of a file containing seventy-two records, the characteristics listed here point up the relative strengths and weaknesses of each method.*

Action	I/O Count
Read Index file	1
Read Overflow Block 019	2
Read Overflow Block 017	3
Read Overflow Block 009	4
Read Overflow Block 001	5
(Key 266 in overflow block 1 is high)	
Write 252 as Overflow Block 020	6
Read Overflow Block 009 again	7
(Change Block 9 Link Field to 020)	
Write Updated Overflow Block 009	8

Table 2: *Processing a record that is in the overflow file of an ISAM file. Given the problem of writing a new record with a key of 252 to an ISAM file as represented in figure 6, this table lists the sequence of events necessary to add the new record, which will go into the overflow file between the records with keys 250 and 266.*

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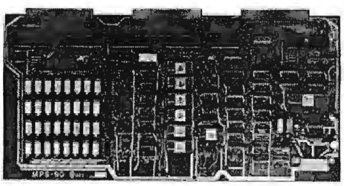

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ciples will apply to all ISAM implementations.)

One of the advantages of ISAM is that records whose keys differ greatly may occupy physically adjacent locations in the storage medium. For example, it is perfectly proper to have the ISAM prime block illustrated in figure 3. The index entry for this sector would carry 266 as the highest key entry.

Suppose that record 200 is to be added. If this record is written in its normal place, something must be done with record 266, as there can be only four records in a block. If 266 is relocated to the next block, the highest record in that block will be bumped, and so on. Bumping records in this manner would increase the access time significantly by necessitating the rewriting of the entire prime file from the point of addition on (as in a sequential file). Because access speed is one of the reasons for considering ISAM, this approach is usually avoided by writing bumped records into an *overflow file*. In addition, the format of the ISAM index record is modified to indicate the presence and address of any overflow entries. Figure 4 presents the disk file example with the extensions necessary to add record 200 to an overflow file.

The pointer in the overflow field of the index is the address of the sector in the overflow file that contains the next record with a key that is higher than the prime block high key. In figure 4, the next record higher than 250 is found in overflow sector 1; apparently record 266 was the first overflow to occur for the prime file.

Each record in the overflow file consists of the key of the record, its data, and a *link field*. The link field contains a pointer to the next higher record in overflow associated with this particular disk sector. If more records are added to the original sector, the link fields in the overflow file form a chain of records displaced from the prime file. Suppose records with keys of 210 and 218 are added to the ISAM file on different days. Figure 5 shows how the blocks in the three files would appear.

The overflow pointer in the index record has changed to a value of 017, while the overflow key remains at 266. This shows three things: that there is an overflow chain for this set of prime records; that the highest key

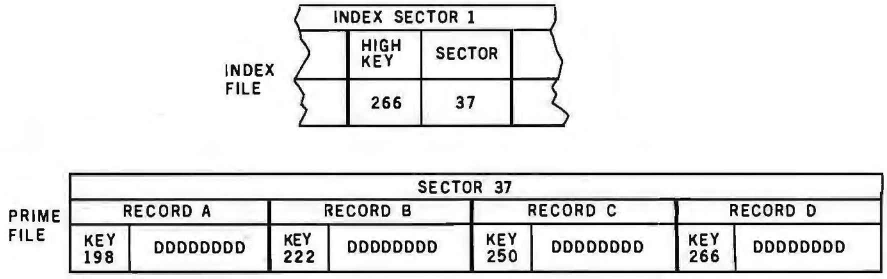

Figure 3: *A valid physical record in an ISAM file. Since an ISAM file does not require saving disk space for every possible key, records with nonadjacent keys can be adjacent in the file. If, for example, the record with key 252 were to be added to this file, this physical record would be rewritten with record 252 in the place of record 266. Record 266 would then be written in the overflow area for this physical record.*

in the chain is 266; and that the chain starts with overflow block 017. In this example, the overflow chain has three entries.

If a record is added whose key is greater than the highest key currently in the prime area, then that record is written at the end of the overflow file. The index and overflow link values are altered to put the new record in its proper place. For example, if record 220 is added, the prime block remains unchanged while the overflow and index blocks are modified as shown in figure 6.

The overflow records have three distinct characteristics. First, they are *not* in key sequence. Second, the records are *not* blocked. Third, the overflow records do *not* have the same format as the non-overflow records (link fields are present). Although there is only one overflow chain for each prime block, the chain may have multiple entries.

In order to access an ISAM record, the program may have to "walk" along an overflow chain until it finds the desired record. Any such overflow processing adds tremendously to the number of I/O operations executed during a retrieval. If the files looked like those in figure 6, it would take just two I/O operations to read record 198 (one read of the index file and a read of the prime file). However, retrieving record 266 takes five read operations, four of which are overflow reads. The processing necessary to add record 252 near the end of the overflow chain is listed in table 2.

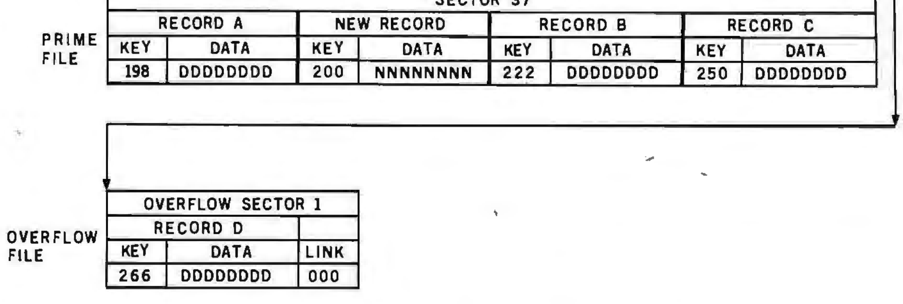

Figure 4: *Index entry for a given physical record in an ISAM file. Along with the pointer to the physical record (here, a disk sector), a pointer must be established to the first record in the overflow area that belongs to the current physical record. When record 200 is added to the file here, it bumps record 266 out of the same physical record. Record 266 is placed in the overflow file with a pointer to it from the index entry.*

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This brief description of the I/O operations associated with processing overflow chains indicates why ISAM overflow processing must be avoided at all costs. There is no more certain way of slowing down a program than to force it to process long overflow chains.

Each record in the overflow file consists of the key of the record, its data, and a link field.

Since it is fairly common to add new records to an existing file, some overflow is bound to occur. How can this overflow be removed? Many ISAM I/O packages provide a utility program that will *reorganize* an ISAM file — that is, rewrite the entire file so that all records are written into the prime disk file. After reorganization, the overflow file is empty and all delay associated with overflow records is eliminated. If such a utility is not available, a program to do the reorganization may have to be created.

The obvious next question is, "When should an ISAM file be reorganized?" Unfortunately, there is no precise answer. One guideline used in the past by this author is as follows: an ISAM file should be reorganized whenever the file response time increases by more than 30%, or whenever more than 20% of the records in the file are stored in overflow.

The first part of this guideline implies that there must be some way of measuring response time, even if it is subjective. There also must be someone assigned to a monitoring function. The second part suggests that there should be another utility program that will give certain information about an ISAM file. It must at least show the ratio of prime to overflow storage, and it might also tell the number of blocks that have overflow chains and the number of entries in each chain.

Now some criteria may be established for judging whether ISAM is appropriate for a given application. First, you must be certain that reorganization and diagnostic utilities are available (or that the user is willing to create them). It is difficult to see how ISAM files can be considered without such utilities unless very few records will ever be added to the file.

Next, see if the other two access methods can be eliminated. Is the sequential access method really too slow? What kind of response is required (not just desired) for this application? If rapid response (less than 1 second) to the user is a requirement, then sequential files are probably eliminated. Of course, this judgement has to be made on an application by application basis: if an inventory system is being designed, it is reasonable to require a reasonably prompt response to an inventory question. On the other hand, the need for immediately answered inquiries to a membership file for the computer club is less obvious.

To evaluate the random-access method, the keys to the file should be examined. Can a unique key be assigned that will translate to a physical address? If this key is alphanumeric and of any length, the number of possible key values may easily exceed the storage capacity. Even if the key is numeric, the range may be larger than the storage. In either case, the pure random-access approach is usually impractical.

If both sequential and random files are impractical, consider ISAM files. First, establish the approximate size and growth rate for the file. Once the system is fully operational, how many records are expected to be stored in this file? How often are records added to the file? Are they added uniformly with respect to time, or is there a particular period when there will be rapid growth for this file? For example, you expect a marked difference in the growth pattern for an inventory file for an auto parts store as opposed to an inventory file for a toy store, especially during the Christmas season. Rapid, irregular growth of an ISAM file indicates rapid growth of the overflow file; if computer time is limited, there may be potential problems with scheduling the file's reorganizations.

In connection with reorganizing the file, two questions must be asked. How long will it take to reorganize the full file? Can the user permit this file to be unavailable to him for the

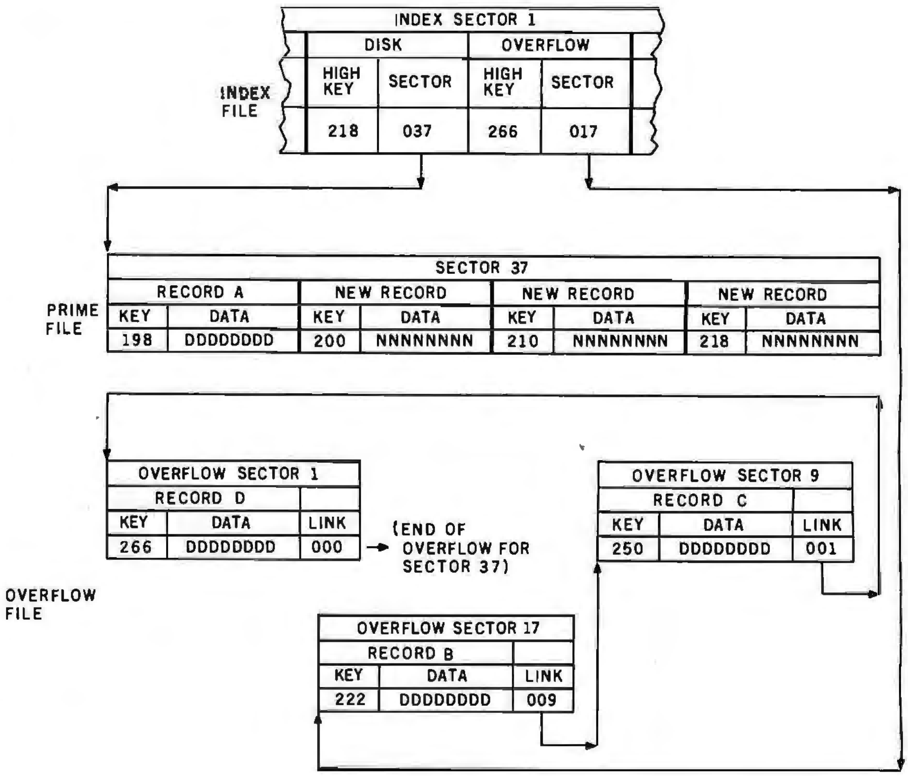

Figure 5: *Multiple-overflow records associated with a physical record. When more than one logical record originally from a given physical record is pushed into overflow, the records are threaded together in ascending-key sequence as presented. The overflow index points to the first overflow record. Each overflow record points to its successor, with a pointer of 000 indicating the end of the string of records.*

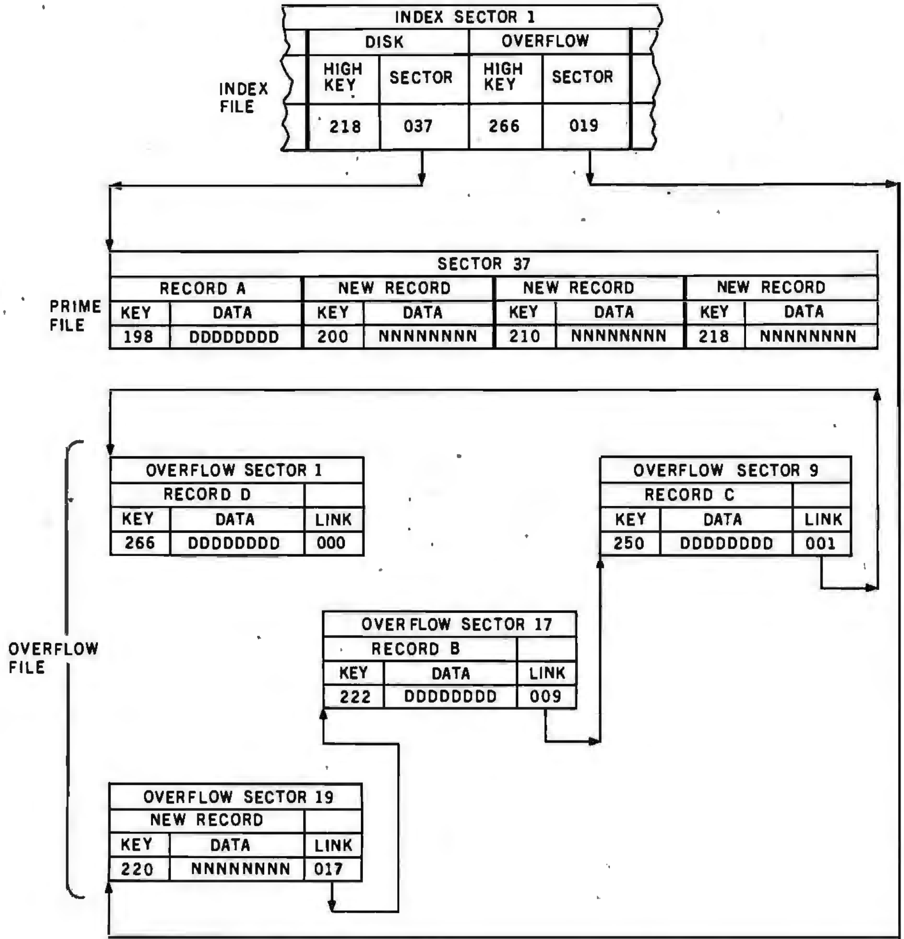

Figure 6: *Comparison of record-access times for overflow and non-overflow records. It takes two disk-read operations to access any record that is in the disk file: one to read the index entry, and one to read the physical record. Since an overflow record is read by chaining through the overflow records associated with a given index entry, retrieving an overflow record may take many disk-read operations. It will take five disk-read operations to read record 266: one to read the index entry, and four to read through records 220, 222, and 250, before arriving at record 266.*

length of time necessary for the reorganization? In particular, if the answer to the second question is "no," the file must be redesigned (and probably the application as well). Although this point may seen trivial at the very least, it indicates that large ISAM files may be inappropriate for businesses that are operated 24 hours a day, 7 days a week.

Now it is necessary to determine roughly how often the file must be reorganized. How long will it take the file to grow by 20%? If the answer is 90 days, you have 3 months to reorganize the file. If the answer is only 9 days, you may have a bit more of a problem in scheduling the processing necessary to do the reorganization.

In addition to the number of new records being added, also consider the relative activity of those records. Is a new record more likely to be accessed than an old record? If this is the case, then it is possible that the new record might be placed in overflow; this would cause either longer access time when the record is being referenced or time lost in reorganizing the file.

The indexed sequential-access method has many advantages, but it should not be selected without a thorough examination. When provided with a basic understanding of ISAM files and the questions suggested in this article, the personal computer user can determine if the ISAM method of data access is the best choice for his application. ■

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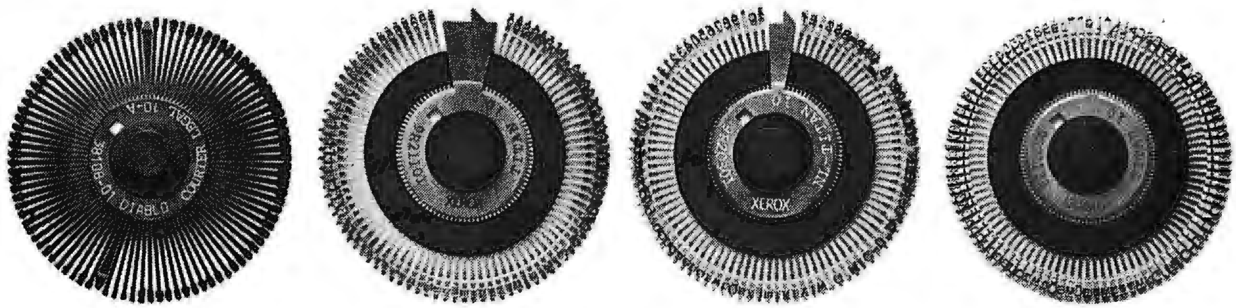

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A Time-Sharing/Multi-User Subsystem for Microprocessors

Don Kinzer
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Now that the personal computer has become firmly established, many users are developing an appetite for more complex and sophisticated systems. Disk-based systems, quite rare among users several years ago, are now commonplace.

Among the concepts being investigated and implemented by advanced experimenters are: real-time operating systems; multiprocessor systems (eg: resource sharing); advanced disk-operating systems; multitasking systems; parallel processing; and time-sharing/multi-user systems. Indeed, almost every feature of large computer systems is being considered for implementation on microcomputers. This article will explain some of the problems, techniques, advantages, and disadvantages of time-sharing/multi-user microprocessor systems. For the most part, the techniques are applicable to all currently popular microprocessors (eg: 6800, 8080, 6502). However, the exact implementation and circuitry required may differ depending upon the microprocessor.

The impetus for time-sharing or multi-user systems is to allow for more efficient use of processor time and to allow several people to share the processor. A microprocessor can do only one thing at a time: the trick is to make it *appear* to be doing more than one thing simultaneously. In most home computer applications, the processor is input/output (I/O) bound — that is, the processor spends much of its time waiting for I/O.

The only time the processor "wastes" is the overhead time required to change users.

The idea, then, is to let the processor execute the next user's job while the I/O interface handles the time-consuming serial I/O. This may lead to the false proposition that we need complicated I/O interfaces. But all serial I/O devices, such as the universal asynchronous receiver/transmitter (UART), or the asynchronous communications interface adapter (ACIA), are I/O processors. After they get the character to transmit, for example, they are processor independent, allowing the processor to do something else (usually a loop to wait for the device to come to a ready state, as in single-user systems).

Imagine two programs, both in memory, two I/O routines, and two terminals. Program A (Spaceflight, for example) uses I/O routine A that drives terminal A. Program B, a BASIC interpreter, uses I/O routine B that drives terminal B. Each I/O routine has the flowchart shown in figure 1. One program executes until it needs its I/O device and the device is busy. At that time, control is transferred to the other program after first saving the contents of the processor registers. When the other program meets the same condition with its I/O device, control switches back again.

But what happens if program A gets caught in a loop or if program B doesn't do any I/O? The answer is, of course, that the multi-user system fails. What we need is some way to insure that each user gets a share of the processor time. To accomplish this, we can adopt a whole new philosophy that gives each user equal time. The clock circuitry shown in figure 2 will interrupt the processor at regular intervals. The interrupt routine will consist of saving one user's registers, restoring the next user's register contents, and beginning execution. This solution is much more foolproof. No user can hang up the system unless interrupts are masked or disabled. However, this returns to the same problem we started out to solve: if user A is doing

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I/O and his device is not ready, processor time is wasted waiting for it.

The obvious solution is to use the best parts of both systems and eliminate the disadvantages of each: allow each user a time slice, and when the time has expired, move to the next user. Furthermore, if a user needs his I/O device and the device is busy, truncate (ie: terminate) his time slice and move to the next user. With this system, a user's program will execute until the allotted time runs out or an I/O request receives a busy response. Hence, the processor is always doing something useful, and the only time it wastes is the overhead time required to change users.

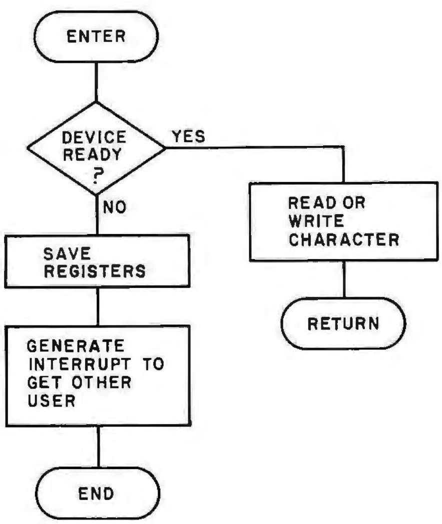


Figure 1: *Flowchart of I/O routines in a multi-user system. The software controlling both programs leaves the control with one until that program requires the use of an I/O device that is not currently available. This scheme is too simple to be used in a practical situation.*

The efficiency of the system, in terms of *processor time efficiency* (PTE), is defined as:

$$\text{PTE} = \frac{\text{execution time}}{(\text{execution} + \text{overhead time})}$$

Although the system can never be 100% efficient, it will be the system designer's goal to make the processor time efficiency as high as possible. This is subject to other constraints to be discussed later.

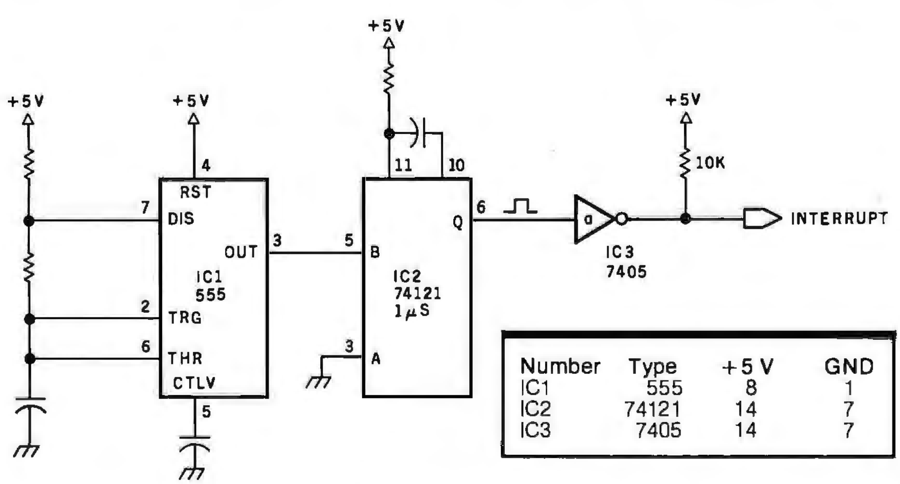
It is clear that we need some means to terminate a time cycle and concurrently generate an interrupt to the processor. Furthermore, we want to insure that when the current user prematurely terminates, the next can still get his full time allotment. The circuit in figure 3 will implement this for a 6800 microprocessor. An 8080 implementation might use IN or OUT instructions instead of memory-mapped I/O.

SEL is a signal that comes from a memory-mapped bit and indicates that we are addressing the interrupt circuitry, while VMA indicates a valid address on the bus. Normally, IC1a will time out (ie: Q output will drop low) after a certain period of time set by its resistor/capacitor combination. It will trigger IC1b for a 1 μs pulse. This pulse is fed to the interrupt line of the processor through the open-collector inverter IC2. Furthermore, when IC1b times out, it triggers IC1a and starts the cycle over again. However, when VMA and SEL are true and the processor is doing a write (ie: R/$\overline{\text{W}}$ false), IC1a will be cleared early. This action fires IC1b which then interrupts the processor and also triggers IC1a to start a new cycle. We now have a means for the processor to interrupt itself!

In general, when the system is first powered up, we do not want these interrupts occurring all over. Unless the system is in read-only memory, we must first load in the software including the interrupt handler. Furthermore, back-to-back one-shots usually have startup problems so that the circuit of figure 3 may not always run.

We can fix both of these problems simultaneously as shown in figure 4. Upon power-up or pressing the reset button, the $\overline{\text{RESET}}$ line becomes active and sets the RS flip-flop formed by IC4a and IC4b. Through IC5, IC4b holds IC1a cleared and IC4a holds the A input of IC1b high. Because IC1a is cleared, the B input of IC1b remains high as well. When VMA and SEL are true and the processor is executing a read operation, the RS flip-flop is reset. This removes the $\overline{\text{CLEAR}}$ signal from IC1a, thus triggering IC1b, which causes the processor to be interrupted. When IC1b times out, it triggers IC1a and then the cycle is the same as before. As you can see, when the system powers up, the interrupt timer is disabled until the processor reads a particular location (ie: the memory-mapped bit SEL), which then starts the timer. Furthermore, pressing the reset button will also disable the timer.

Memory management is important in such systems. For example, if we have a sixteen-user system and the users will never be running the same program, we can merely assemble all the programs so that they fit in the memory space available. Additionally, we need to set aside a *separate* temporary storage area for each user. With the 8080 this is no great disadvantage, but with the 6800 or 6502, there is the 256-word page 0 which is most efficiently used as temporary storage. With large programs requiring large amounts of storage, there



Number	Type	+5 V	GND
IC1	555	8	1
IC2	74121	14	7
IC3	7405	14	7

Figure 2: *Schematic diagram of a time-slicing interrupt clock. This circuit generates a periodic pulse that is used to interrupt the processor. When coupled with the appropriate software, the circuit can be used to divide processor time equally among all the running programs.*

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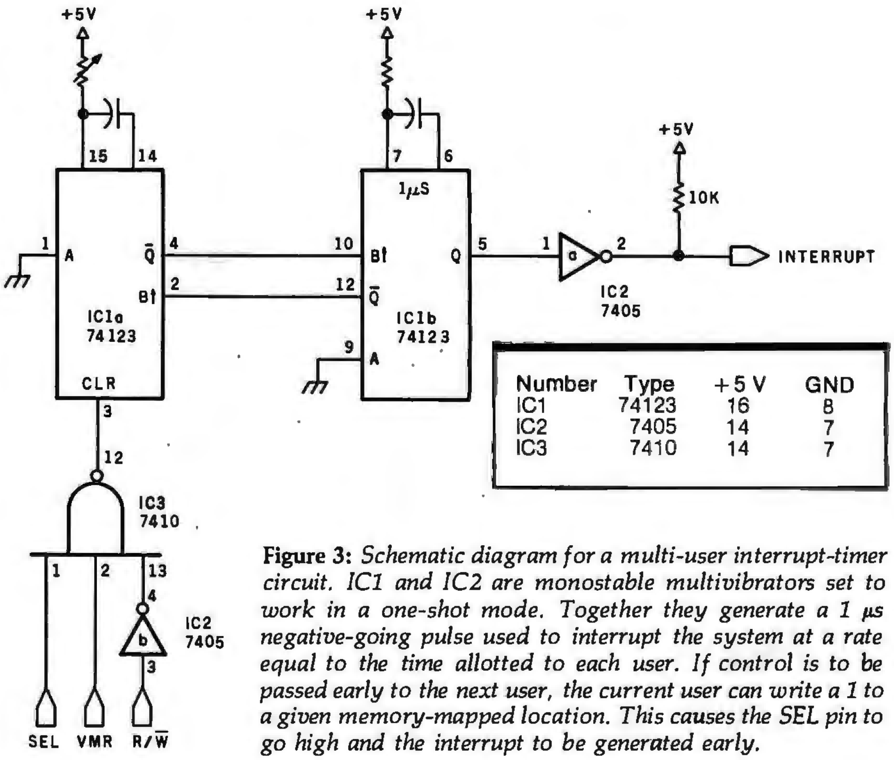
may not be enough page 0 memory to go around.

Further problems are encountered when we try to let all users run the *same* program at the *same* time. One approach is to have one copy of the program in memory for each of the users: sixteen users and sixteen copies. The amount of memory used may rule out multiple copies.

A second, more desirable approach is to overlay memory from the disk. Under this scheme, when we change users, we write memory out to the disk and load in the next user's memory. This is fine for extremely fast disks or very small programs, but the overhead time mentioned earlier becomes extremely large.

Hardware paging, a more reasonable solution, is very similar to disk-overlay paging. Using this technique, we set out to fool the processor by manufacturing our own address bits. Figure 5 shows a 16 K-byte memory system attached to a sixteen-user time-sharing system. As far as the processor is concerned, the 16 K bytes of memory occupy only 1 K bytes of memory. A 16 K-byte memory requires 14 address bits, A_{13} thru A_0, and the lower 10 bits are supplied by the processor with IC2 enabling the memory for hexadecimal addresses 0000 to 03FF (1 K bytes of memory). The other four address lines are supplied by IC1, a 4-bit binary counter.

Conveniently, we have sixteen blocks of memory, each of which is effectively the first 1 K-byte block in memory. The processor has no idea which 1 K-byte block it is and couldn't care less. If we have sixteen users, each has his own 0000-thru-03FF block of memory to use for temporary storage. Now, if every time we go to another user, we increment



Number	Type	+5 V	GND
IC1	74123	16	8
IC2	7405	14	7
IC3	7410	14	7

Figure 3: *Schematic diagram for a multi-user interrupt-timer circuit. IC1 and IC2 are monostable multivibrators set to work in a one-shot mode. Together they generate a 1 μs negative-going pulse used to interrupt the system at a rate equal to the time allotted to each user. If control is to be passed early to the next user, the current user can write a 1 to a given memory-mapped location. This causes the SEL pin to go high and the interrupt to be generated early.*

Number	Type	+5 V	GND
IC1	74123	16	8
IC2	7405	14	7
IC3	7410	14	7
IC4	7400	14	7
IC5	7408	14	7
IC6	7404	14	7

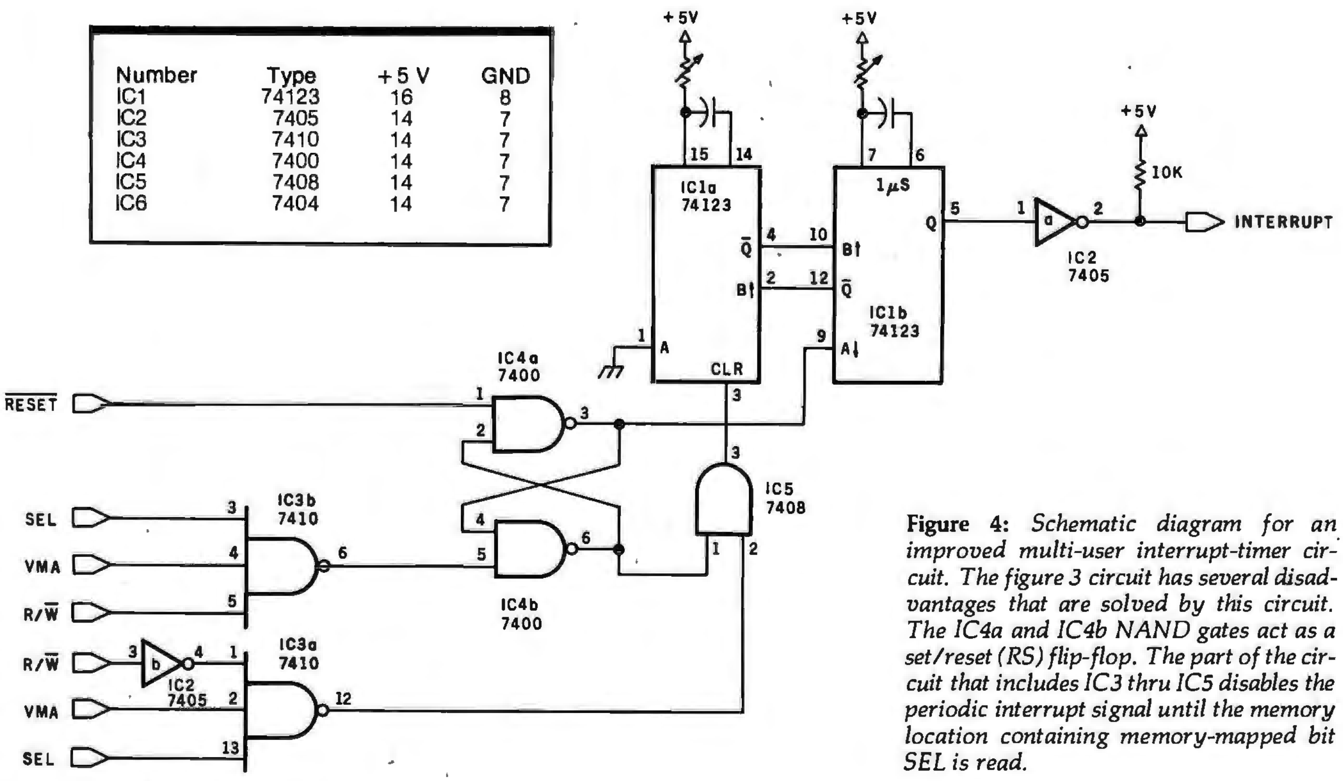


Figure 4: *Schematic diagram for an improved multi-user interrupt-timer circuit. The figure 3 circuit has several disadvantages that are solved by this circuit. The IC4a and IC4b NAND gates act as a set/reset (RS) flip-flop. The part of the circuit that includes IC3 thru IC5 disables the periodic interrupt signal until the memory location containing memory-mapped bit SEL is read.*

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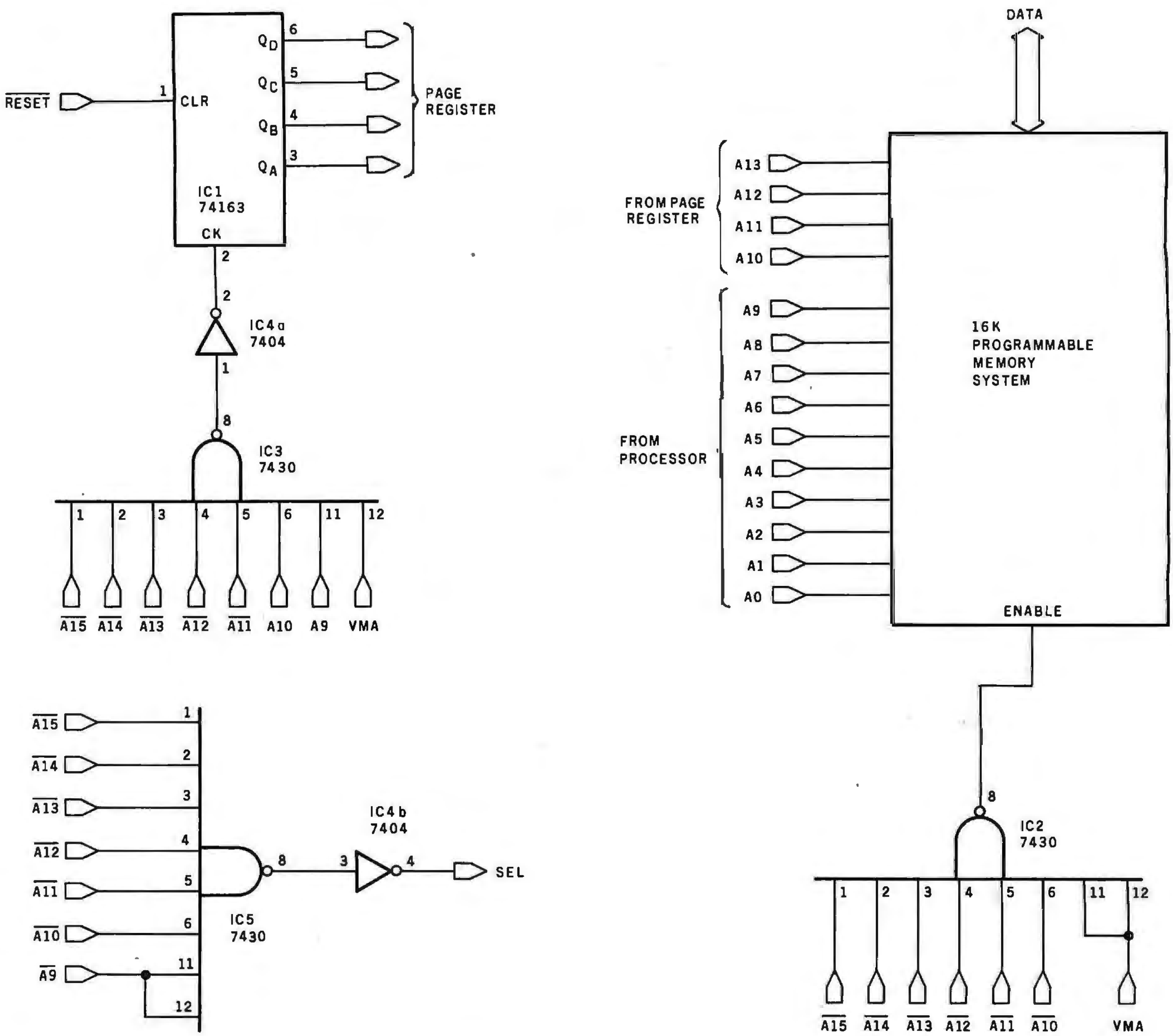


Figure 5: *Overview of a 16 K-byte hardware-paged memory design. The 16 K-byte block of memory shown appears to the computer as a 1 K block with hexadecimal addresses 0000 thru 3FFF. The block of memory is enabled when IC2 goes low, which occurs when address bits A15 thru A10 are low (that is, when an address of hexadecimal 03FF or lower is seen on the address bus). The 4-bit binary counter IC1 is incremented when IC3 goes low. This occurs when a hexadecimal address of 06xx (or 07xx) appears on the address bus; the software in listing 1 uses the hexadecimal address 0600. The SEL line goes high and causes an early interrupt in the circuitry of figure 4 when a hexadecimal address of 04xx (or 05xx) occurs on the address bus. The software in listing 1 uses the address 0400 in two different contexts.*

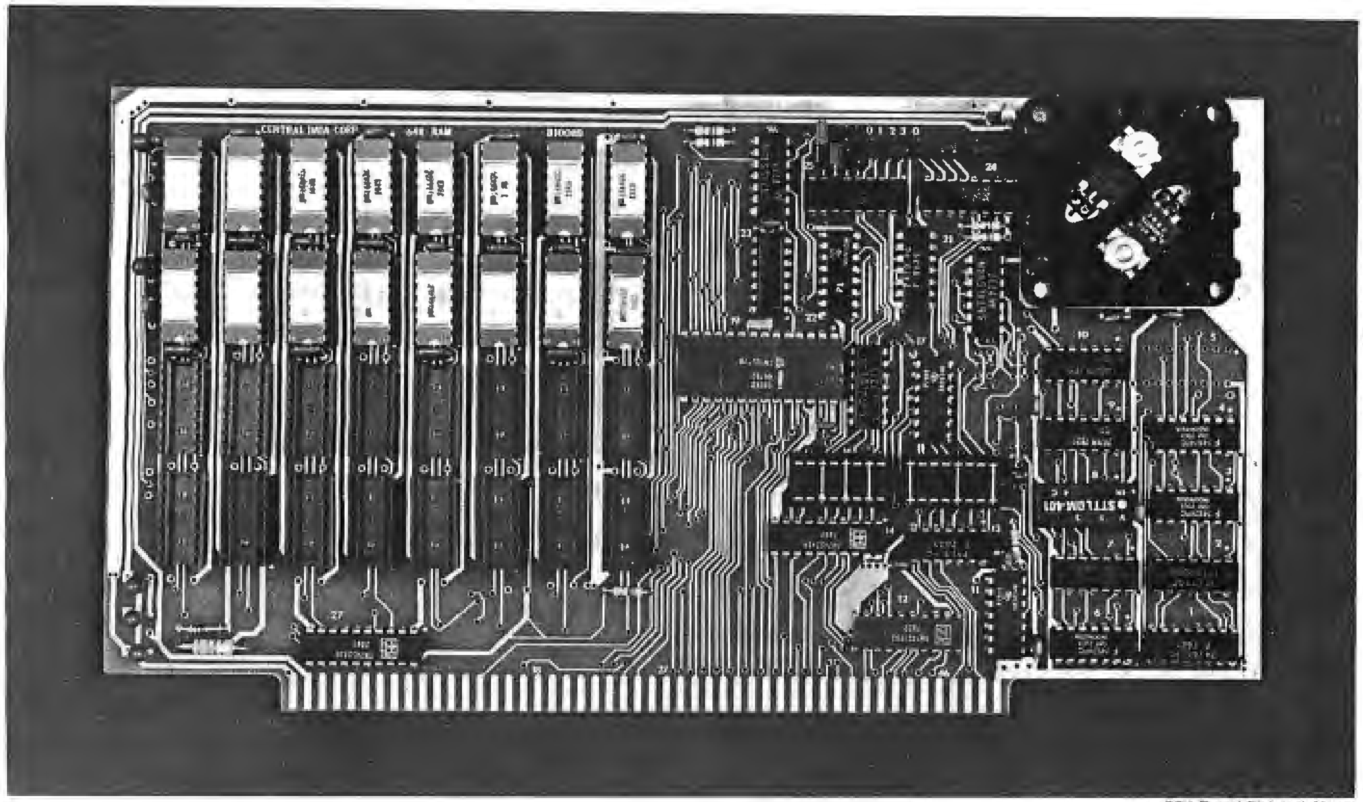
the page register (IC1), we have changed the physical memory which responds to addresses 0000 thru 03FF. This operation will take at most 6 μs, so we keep overhead low.

Since the circuit that first increments the page register and later increments the interrupt circuitry must be memory-mapped to an address outside the 1 K-byte memory space, the whole system occupies a 2 K-byte block. An 8080 would not need to waste this extra memory if IN and OUT instructions were used. Also note that RESET sets the page register to user 0.

The paging scheme, while having separate storage areas with identical addresses, will allow us to have only one copy of each program. This, of course, rules out the use of self-modifying code, unless that code modified is in the first 1 K of memory allotted to each user. On the other hand, code should not be written to modify itself.

Now that the hardware description is complete, I can discuss the software. Since my experimentation was done on a 6800, it will be used as an example. Implementation for a 6502 will be similar and that for an 8080 only slightly more involved. General flow for initialization, interrupt, and I/O routines is shown in figure 6. The 6800 machine code used to implement the flowcharts is given in listing 1. It is assumed that all users

Text continued on page 134



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Listing 1: *Software routines for the author's 6800-based multi-user system. INIT is an initialization routine called just after power-up or reset. INTERR is the interrupt routine that saves the status of a given user and prepares the system for the next user in line. OUTCH is the output routine used by the system. This software is assumed to work with the circuitry of figures 4 and 5. In INIT, reading TIMER causes SEL line of figure 5 to go high and the interrupt system in figure 4 to be enabled for the first time. In INTERR, writing to NUSER causes the page register in figure 5 to increment, causing the next user's block of memory to be immediately enabled. In OUTCH, writing to FORCE causes the SEL line in figure 5 to go high, causing an early interrupt to occur.*

```
Hexadecimal  Hexadecimal              Instruction
Address      Code          Label      Mnemonic    Operand      Commentary

                           *
                           * TIME SHARING SOFTWARE
                           *
03F2                                  ORG         $3F2
03F2                       STACK      RMB         8
03FA                       ACIAH      RMB         1
03FB                       ACIAL      RMB         1
03FC                       XSAVE      RMB         2
03FE                       SP         RMB         2
                           *
                           *
                           *
0400                       FORCE      EQU         $400         FORCED INTERRUPT ADDR
0400                       TIMER      EQU         $400         START TIMER ADDR
0600                       NUSER      EQU         $600         NEXT USER ADDRESS
                           *
                           *
                           *
2000                                  ORG         $2000
2000         0F            INIT       SEI                      DISABLE INTERRUPTS
2001         5F                       CLR B                    SET USER 0
2002         CE 03 F2      INITLP     LDX         #STACK
2005         FF 03 FE                 STX         SP           SET STACK POINTER
2008         CE 08 00                 LDX         #$800        LOAD PROGRAM ADDRESS
200B         FF 03 F8                 STX         STACK+6      SET USERS PC
200E         86 80                    LDA A       #$80
2010         B7 03 FA                 STA A       ACIAH        SET ACIA HIGH ADDR
2013         F7 03 FB                 STA B       ACIAL        SET ACIA LOW ADDR
2016         F7 06 00                 STA B       NUSER        SET NEXT USER
2019         5C                       INC B
201A         5C                       INC B                    GET NEXT USER ID
201B         C1 20                    CMP B       #16*2        CHECK DONE
201D         26 E3                    BNE         INITLP       LOOP TILL DONE
201F         C6 10                    LDA B       #16          SET USER COUNT
2021         FE 03 FA      STACIA     LDX         ACIAH        GET USERS ACIA ADDR
2024         86 03                    LDA A       #3
2026         A7 00                    STA A       0,X          RESET ACIA
2028         86 15                    LDA A       #$15
202A         A7 00                    STA A       0,X          SET CHARACTERISTICS
202C         B7 06 00                 STA A       NUSER        SET NEXT USER
202F         5A                       DEC B                    COUNT DOWN
2030         26 EF                    BNE         STACIA       LOOP TILL DONE
2032         8E 03 F9                 LDS         #STACK+7     SET USER 0 STACK
2035         B6 04 00                 LDA A       TIMER        START INTERRUPTS
2038         0E                       CLI                      ENABLE INTS
2039         7E 08 00                 JMP         $800         GO TO USERS PROGRAM
                           *
                           *
                           *
203C         BF 03 FE      INTERR     STS         SP           SAVE USERS SP
203F         B7 06 00                 STA A       NUSER        SET NEXT USER
2042         FE 03 FE                 LDX         SP           GET THIS USERS SP
2045         3B                       RTI                      START PROCESSING HIM
                           *
                           *
                           *
2046         FF 03 FC      INCH       STX         XSAVE        SAVE X
2049         FE 03 FA                 LDX         ACIAH        GET USERS ACIA ADDR
204C         A6 00         CHECKR     LDA A       0,X          GET STATUS
204E         47                       ASR A
204F         24 08                    BCC         NOTRED       BRANCH IF NOT READY
```

Listing 1 continued on page 132

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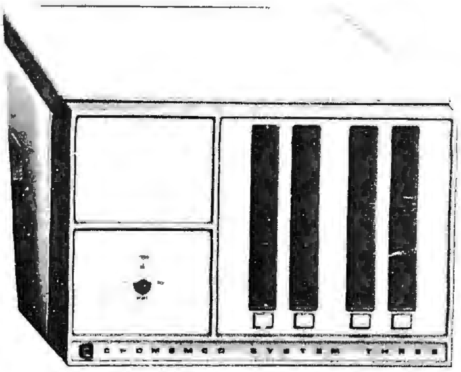

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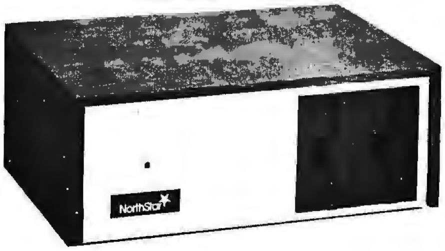

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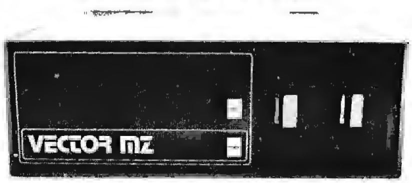

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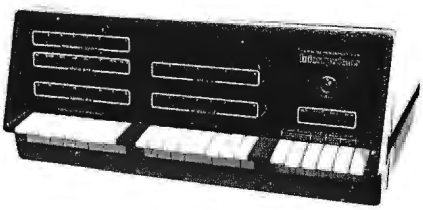

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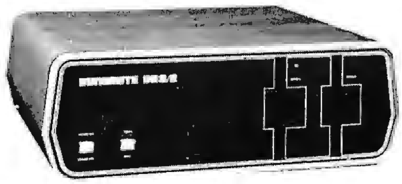

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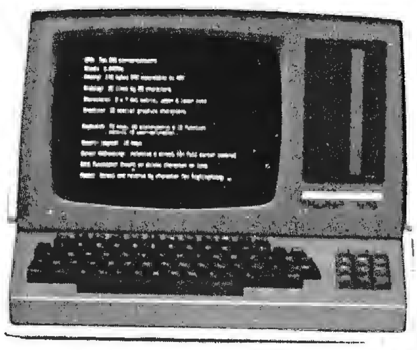

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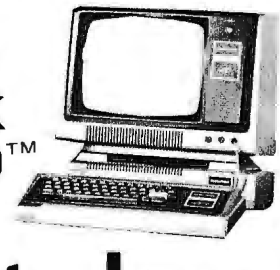

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```
2051   A6 01               LDA A  1,X       ELSE GET DATA
2053   84 7F               AND A  #$7F      MASK OFF PARITY
2055   FE 03 FC            LDX    XSAVE     RESTORE X
2058   39                  RTS
2059   B7 04 00  NOTRED    STA A  FORCE     FORCE INTERRUPT
205C   20 EE               BRA    CHECKR    GO CHECK AGAIN
                 *
                 *
                 *
205E   36        OUTCH     PSH A            SAVE CHARACTER
205F   FF 03 FC            STX    XSAVE     SAVE X
2062   FE 03 FA            LDX    ACIAH     GET USERS ACIA ADDR
2065   A6 00     CHECKD    LDA A  0,X       GET STATUS
2067   47                  ASR A
2068   47                  ASR A
2069   24 07               BCC    NOTDON    BRANCH IF BUSY
206B   32                  PUL A            GET CHARACTER BACK
206C   A7 01               STA A  1,X       SEND IT
206E   FE 03 FC            LDX    XSAVE     RESTORE X
2071   39                  RTS              DONE
2072   B7 04 00  NOTDON    STA A  FORCE     FORCE INTERRUPT
2075   20 EE               BRA    CHECKD    GO CHECK AGAIN
                 *
                 *
                 *
                           END
       NO ERROR(S) DETECTED

    SYMBOL TABLE:
ACIAH   03FA   ACIAL    03FB   CHECKD  2065   CHECKR  204C
FORCE   0400   INCH     2046   INIT    2000   INITLP  2002
INTERR  203C   NOTDON   2072   NOTRED  2059   NUSER   0600
OUTCH   205E   SP       03FE   STACIA  2021   STACK   03F2
TIMER   0400   XSAVE    03FC
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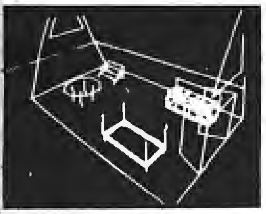

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By Ken Germann

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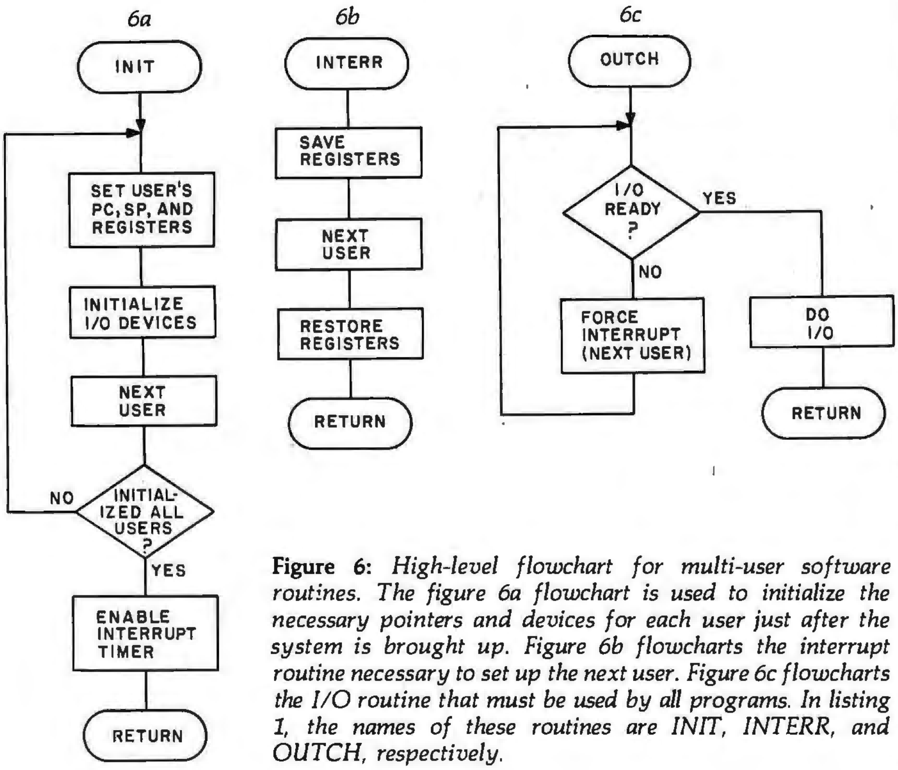

Figure 6: *High-level flowchart for multi-user software routines. The figure 6a flowchart is used to initialize the necessary pointers and devices for each user just after the system is brought up. Figure 6b flowcharts the interrupt routine necessary to set up the next user. Figure 6c flowcharts the I/O routine that must be used by all programs. In listing 1, the names of these routines are INIT, INTERR, and OUTCH, respectively.*

Text continued from page 128:
are running the same program (for example, BASIC) that starts at hexadecimal 0800. Furthermore, it is assumed that ACIAs are used for the I/O interface and are located contiguously at hexadecimal 8000, with each one occupying two memory locations. No pointer initializations are shown for any programs that require them. If you are going to run BASIC, you will need to set pointers in user areas to indicate the memory area to be used as source-code storage for that particular user.

The overhead in the interrupt handler is a mere 36 μs, including the time to respond to the interrupt, assuming that you have 1 MHz system clock. The interrupt rate, or time-slice length, depends on several factors and must be selected according to the software being run. If the I/O devices are running at 1200 bps, the character time is 8.33 ms. Continuing our example of sixteen users, a good starting point would be 1/16 of this time. This would allow each user to output at full speed, but would have 93% efficiency (ie: PTE). A more efficient system could be realized by lengthening the time slice at the expense of slowing effective output speed. The trade-off here depends on the computing-to-I/O ratio to be encountered in the application.

The apparent efficiency perceived by a single user also depends on the amount of I/O being encountered. If no users are doing I/O, then the *speed reduction factor (SRF)* for each user will be:

$$SRF = \frac{PTE}{16}$$

where 16 is the number of users. As a worst-case example, if a certain operation takes N μs to execute on a single-user system, it will now take N/SRF μs to execute. However, if some or all other users are doing nothing but I/O, the apparent speed rises considerably.

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Book Reviews

The Network Nation: Human Communications via Computer

by S R Hiltz and M Turoff
Addison-Wesley, 1978
hardcover $29.50
softcover $17.50

One of the most promising areas in personal computing is public-information utilities, which can bring people into communication with each other and open doors to vast information resources. One aspect of the new computer communications media is computer *conferencing*. A computer conference is a structured town meeting where all the discussants may "speak" and "listen" simultaneously without being present at the same times and places. A computer conferencing facility monitors the progress of the discussion and provides a complete and constantly available verbatim transcript of the entire conference.

The Network Nation is a comprehensive treatment of this new electronic communications medium, written by two professionals very much involved with its genesis. Murray Turoff is a computer scientist who is one of the pioneers in computer conferencing. Starr Roxanne Hiltz is a sociologist who, in collaboration with Turoff, has made careful studies of the psychological and sociological dynamics of computer conferences. This book treats you to an overview of what a computer conference is, what it is like to participate, and how the new medium is different from conventional face-to-face conference situations. Examples are drawn from the historical antecedents of present systems and the most important existing programs. Applications of these systems in high-level planning and decision making, scientific conferencing, etc are presented. Future applications for mass public use are predicted along with speculation on the psychological, sociological, and cultural implications that may be expected from the widespread availability of computer conferencing.

The Network Nation is an entertaining, informative, and thought-provoking book that should appeal to a wide range of readers. It is unusual in its technical excellence as well as its emphasis on human and cultural issues. It should be read by everyone interested in the direction that our technology is taking us and particularly by those interested in personal computing. The authors summarize best the impact of their subject in the following quotation drawn from the preface of the book.

"Computerized conferences [are] a new form of human communication utilizing the computer. We believe that it will eventually be as omnipresent as the telephone and as revolutionary, in terms of facilitating the growth and emergence of vast networks of geographically dispersed persons who are nevertheless able to work and communicate with one another at no greater cost than if they were located a few blocks from one another."■

Glen A Taylor
19 June Pl
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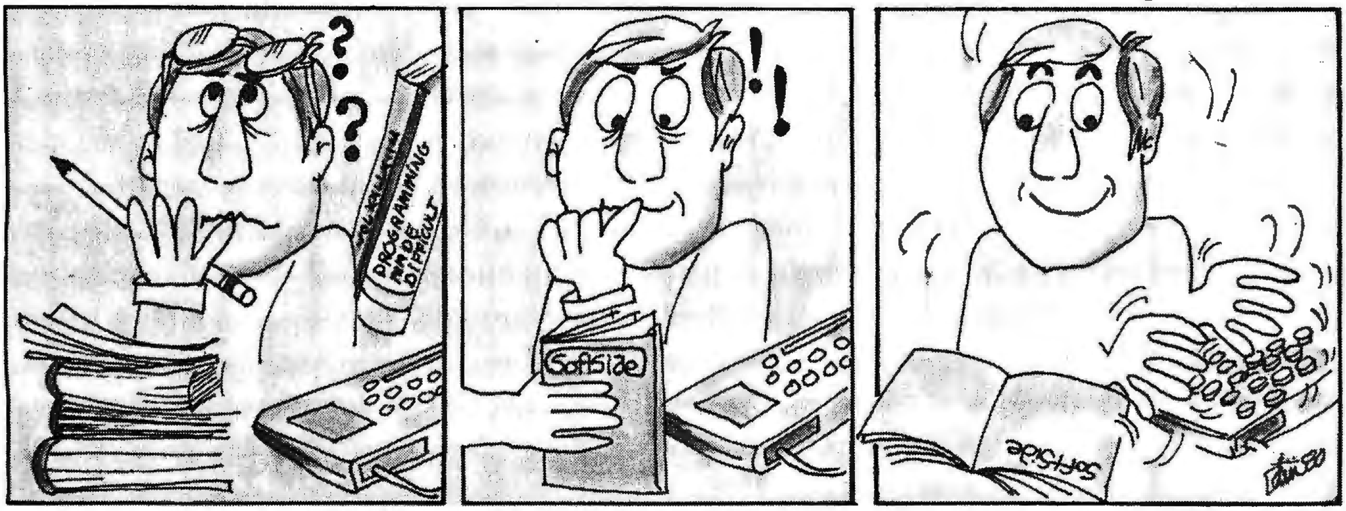
SOFTSIDE MAGAZINES the fun way to learn programming...



The easiest and most entertaining way to learn to program is by entering games into your computer. You get to see how other programmers accomplish certain tasks, gain experience with new BASIC instructions, and the reward of playing the game when you finish serves as constant encouragement.

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Our games are very good. Many of the games we have published have sold individually for $8, $10, or even $15 each! One issue is normally worth the price of a years subscription for the game value alone.

For example, our May Issue of the S-80 Edition for the TRS-80 and Video Genie computers is a special Star Trek Issue. We include two complete Star Trek games, including one for which over 2000 people paid $14.95 each. We include 8K of remark statements not included in the commercial version so you can understand how it works and make your own modifications. There is a ten page article and flight manual lavishly illustrated with examples from the actual play of the game. You can even subscribe on cassette or diskette if you don't want to type in the line listings. The game issue also includes an article on Star Trek, the Motion Picture, including five programs developed on a 4K Level I TRS-80 to be used as displays in the movie! Another program included is an uncopyrighted day of the week routine that you can use in your own programs.

The May issue of our Apple Edition includes a high speed, colorful, challenging version of the space invaders game that is so popular in the arcades. Other features include the second installment of the book, "Intimate Instructions in Integer BASIC", Right/Left — a game for very young children, Small Marquee — a word guessing game, Black Box — a game of deduction, Magic Cave — a game seeking treasure in a hazardous dungeon, plus a disk catalog program and a method for protecting your program against copying.

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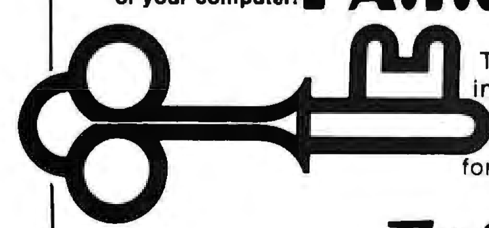

The guide to using machine language routines from Level II BASIC (TRS-80) in your own programs. Contains comments on the complete code of Level II BASIC, several programs to explore and use the subroutines in read only memory, and explanations of how to use the material. Includes line listing for a complete monitor and Z-80 disassembler. This book includes Supermap and the TRS-80 Disassembled Handbook, independently published at $30.

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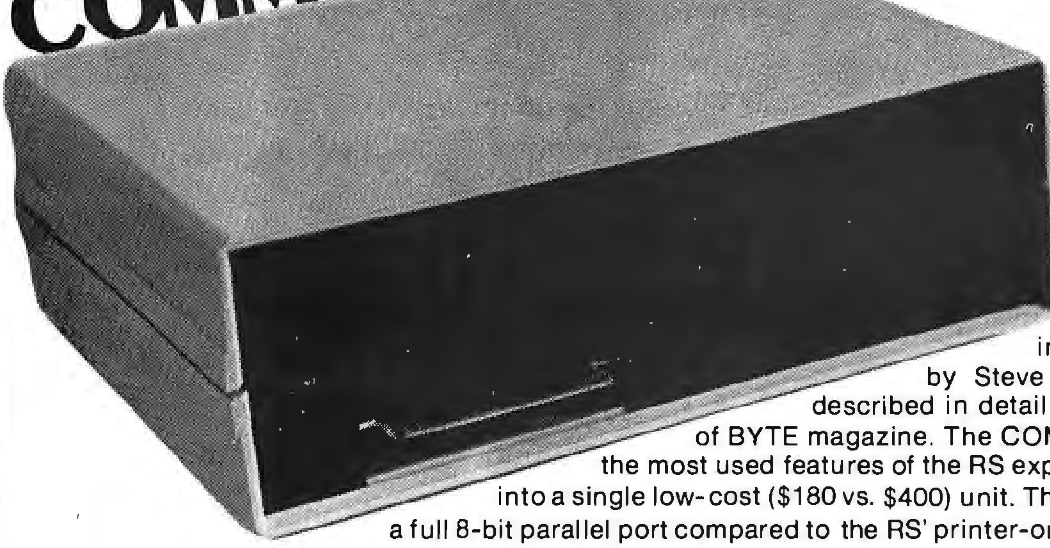

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A Telephone-Dialing Microcomputer

John Renbarger
Moore School of Electrical Engineering
University of Pennsylvania
Philadelphia PA 19104

Introduction

This article describes an application of computers to personal control of communication facilities. I have added some simple hardware to my KIM-1 microcomputer and have successfully dialed local and long-distance numbers on my home telephone. Although I made use of an expanded KIM to develop the programs listed here, the final program and data tables fit into the standard KIM memory.

In the form presented here, the system accepts a single telephone number from the KIM keypad, dials it, and stores it for redialing. In my system, only one number is stored in the computer at a time, but the routines could be used by a supervisory program to select and dial from a list of several stored numbers.

Two methods of dialing are available. One method uses pulses to control a solenoid that interrupts the telephone connection. The other method, which is faster, generates dual-tone, multiple-frequency signals that are acoustically coupled to the telephone receiver.

How to Use the Program

After loading into KIM, the dialer program is started at address hexadecimal 0200. The program will accept any telephone number up to eleven digits long from KIM's keypad. As the number is entered, the last six digits appear in the display, rolling earlier digits off the left edge of the display. All eleven digits are stored in the computer's memory. If you make a mistake, pressing the GO key clears the number, puts six Fs in the display, and lets you start over.

You can generate higher frequencies by using a larger increment to step through the waveform table.

When the number has been entered correctly, there are two options for dialing. The first option is to push KIM's AD key. The system will produce data for a digital-to-analog (D/A) converter to generate a pair of audio tones for each of the stored digits. These tones are the same ones produced by push-button telephones. The tones will operate the telephone switching circuits if the sound is coupled to the receiver mouthpiece by a speaker held nearby.

The second option is to push KIM's DA key. The system will briefly break the telephone connection the proper number of times and at the correct rate, the way a rotary-dial telephone does. A solenoid must be connected to the cradle button of the telephone receiver to operate the telephone switching circuits.

After the number has been dialed, it remains stored in the computer, ready to be dialed again. A new number can be entered by first pressing the clear (GO) key and then using the keypad to enter the new number. Since the present system can store and recall only one number, the primary usefulness of the device is to eliminate reentering a number when repeatedly calling a line that is busy.

If your telephone line to the central office is not set up to accept the Touch-Tone frequencies, you will be limited to the pulse-dialing method, using a solenoid to depress the cradle button. On the other hand, if you have a push-button telephone, your computer will be able to use both methods to dial.

Telephone System Basics — Tones

Push-button telephones dial other telephones by sending pairs of audio frequency tones over the telephone voice channel each time the user holds down a key on the telephone set. The telephone company selected the particular tones that are employed so they could be easily decoded, but we need only know what the frequencies are. Table 1 lists the frequencies generated by the various buttons.

Central-office switching facilities decode the tones and connect the desired circuits based on the sequence of tone pairs received. Each tone pair must last long enough to be recog-

Touch Tone is a registered trademark of the Bell System for its dual-tone, multiple-frequency signaling equipment.

Hexadecimal Offset	Hexadecimal Data	Telephone Digit	KIM-1 Key	Frequencies (Hz)
00	08 0C	0	0	941, 1336
02	02 0A	1	1	697, 1209
04	02 0C	2	2	697, 1336
06	02 0E	3	3	697, 1477
08	04 0A	4	4	770, 1209
0A	04 0C	5	5	770, 1336
0C	04 0E	6	6	770, 1477
0E	06 0A	7	7	852, 1209
10	06 0C	8	8	852, 1336
12	06 0E	9	9	852, 1477
14	08 0A	*	A	941, 1209
16	08 0E	#	B	941, 1477
18	00 00	none	C	silence

Table 1: *Dual-tone, multiple-frequency (ie: Touch-Tone) signals and tables within the DIAL program. Each Touch-Tone digit is composed of two frequencies, with a total of eight basic frequencies producing the tones for the twelve valid Touch-Tone keys. (See table 2.) The numbers necessary to produce each of the eight frequencies are contained in the table FRQINC (at 2 bytes per frequency). The two numbers in the DATA column point to the appropriate numbers in the FRQINC table necessary to make the two frequencies used by this key. These same numbers (the contents of the DATA column) are in the table TONTAB (see listing 1), and the number pairs are pointed to by the number in the OFFSET column.*

nized as a digit by the switching equipment, and there must be enough separation between tone pairs to distinguish separate digits. Experimentally, a tone pair duration of about 150 ms and a separation of about 75 ms seem to work with my telephone.

Telephone System Basics — Dial Pulses

When you pick up the receiver on a telephone, an electrical connection is made to the lines leading to the central office. When you replace the receiver on the cradle the connection is broken or interrupted. This applies to both push-button and rotary-dial telephones.

The rotary dial on a telephone is a mechanical device which periodically breaks the connection leading to the central office. As you place your finger in a numbered hole and rotate the dial to the stop, the connection is still maintained. When you release the dial, as it travels back to its resting position it breaks the connection at the rate of about ten times per second, thus dialing that digit.

A number of interruptions equal to the value of the digit you dialed will occur each time you release the dial, with the exception that 0 (ie: the digit zero) causes a total of ten interruptions. If you dial a 7, for example, seven interruptions will occur when you release the dial.

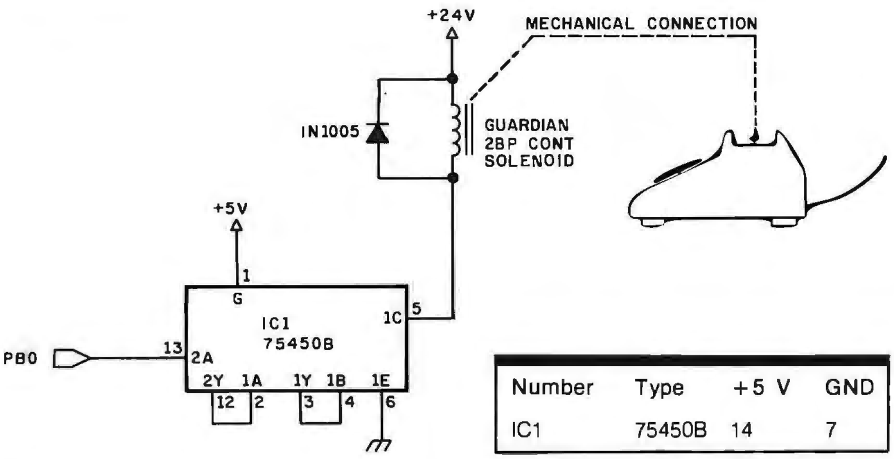
The central-office circuitry counts the number of interruptions to determine which digit was dialed. The longer pause between digits is interpreted as evidence that one digit is complete and that another may begin.

Numbers can also be dialed by pushing the cradle switch button at the rate of ten times per second. This means that a solenoid plunger can be mounted to depress and release the cradle switch on the telephone set.

Since the telephone company prohibits the installation of unapproved equipment on the telephone lines, the only method of interrupting the phone line to be considered here is that of using a solenoid to push the cradle button rather than the method of making any direct connection to the line. Jules Gilder's book *Telephone Accessories You Can Build* (see References) contains solenoid installation suggestions.

There is no problem with using the dual-tone, multiple-frequency method of dialing as long as the coupling is done through the microphone of the handset and not by direct connection to the lines leading to the telephone.

If you are interested in learning more about the operation of the telephone system in general, the References include other sources, such as Peter Luff's *Scientific American* article.



Number	Type	+5 V	GND
IC1	75450B	14	7

Figure 1: *Schematic diagram for solenoid interface to the computer. In this method, the computer interrupts the phone line by pressing and releasing the cradle switch button on the body of the telephone set. IC1 is a TTL-compatible peripheral driver capable of switching up to 300 mA at 30 V. A logical 0 at the output bit PB0 leaves the push-type solenoid unenergized, and a logical 1 energizes the solenoid, pushing the cradle switch button down and interrupting the telephone line.*

Software Required — Pulses

For generating interrupting pulses, an output bit on one of the KIM's input/output (I/O) lines connected to a solenoid driver can be used. KIM's programmable interval timer can help to simplify the programming to control the duration of the solenoid on and off periods. The on time for a pulse (ie: the length of the interruption) seems to be about 35 ms and the off time (ie: the time between interruptions) seems to be about 65 ms.

When a telephone number is entered to the program for dialing, each digit must cause a corresponding number of pulses to be output (eg: one pulse for a 1 digit, two pulses for a 2 digit, and so on). Ten pulses are sent for the 0 digit.

The program must generate these pulses at the rate of ten per second and pause for about ½ second between digits, thus allowing the telephone system to distinguish between digits. For the program in this article, pulses on the KIM output line PB0 control a solenoid connected as shown in figure 1.

Software Required — Tones

One method of generating tone pairs for the telephone network is to produce two square waves of the correct frequencies using just two computer output bits, combining the resulting tones by filters and a resistive network. This would give a waveform with much distortion, but it might be adequate for the telephone system.

I have chosen to generate low-distortion *sine* waves by using the computer to shuffle data and send values to a digital-to-analog converter. I generate audio waveforms in real time by transmitting a byte to an 8-bit converter at a rate that is more than triple the frequency of my highest tone. This technique, described below, uses a table that holds the values for the shape of a sine waveform. The idea is based on Hal Chamberlin's work. (See References.)

The sine waveform table occupies exactly 256 bytes and starts at the beginning of a page boundary. So that I need deal only with positive values, and to avoid overflow with addition, the values stored in the table range from a minimum of 0 to a maximum of hexadecimal 7F. See the SINTAB table which starts at hexadecimal 0300 in listing 1 for the values stored in the table. Since exactly one cycle is stored, going from the last entry in the table to the first entry will give a smooth transition to the next cycle of a continuous waveform. My table is stored in page 03 of memory.

Waveform Generation

To give you an idea of how the real-time waveform generation works, I will use an example. Starting at the first table location, I get a value from the table and convert that value to a voltage. Later, after a fixed interval, I will go to the next table location, get the value stored there, and

Text continued on page 160

Hexadecimal Offset	Hexadecimal Integer, Fraction	Frequency (Hz)
00	00,00	0 (silence)
02	0B,3E	697
04	0C,6B	770
06	0D,BE	852
08	0F,2D	941
0A	13,80	1209
0C	15,8C	1336
0E	17,D2	1477
10	1A,56	1633

Table 2: *The basic frequencies used in the Touch-Tone system and their relation to the FRQINC table. The sound-producing routine SOUND creates the digital values that will become an analog audio signal by lookup in a table containing a sine wave "template." The frequency of the sine wave is varied by changing the number of values of the template skipped over before releasing the next digital value. The values in FRQINC are the increment values necessary to generate the given frequency, expressed as a hexadecimal integer-and-fraction pair.*

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- Too many software packages are now available to list them here.

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All pricing and specifications are subject to change.

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Circle 88 on inquiry card. Circle 89 on inquiry card.

Listing 1: *Program listing for the main program, which includes the telephone number entry, audio-tone dialing, and pulse-dialing routines. The main routine, DIAL, starts at hexadecimal 0200. The sine wave table starts at hexadecimal 0300; it can be moved if the new beginning address starts on a page boundary and if the byte at PAGE1 points to that page number. The program uses routines SCANDS and GETKEY of the KIM monitor.*

```
ADDRESS  OBJECT    LABEL    INSTRUCTION OPERAND                        COMMENTARY
         CODE               MNEMONIC
0000                        *=$00
0000               INC1F    *=*+1
0001               INC1I    *=*+1
0002               PNT1F    *=*+1
0003               PNT1I    *=*+1
0004     03        PAGE1    .BYTE $03                  PNT1I AND PAGE1 TOGETHER POINT TO A LOCATION IN
0005               INC2F    *=*+1                      SINTAB.  THIS ENABLES USE OF INDIRECT ADDRESSING
0006               INC2I    *=*+1
0007               PNT2F    *=*+1
0008               PNT2I    *=*+1
0009     03        PAGE2    .BYTE $03
000A               TEMPX    *=*+1
000B     0B        NDIGIT   .BYTE $0B
000C                        *=$10
0010     00 00     FRQINC   .DBYTE $0000,$0B3E,$0C6B,$0DBE,$0F2D  VALUES FOR INC#I, INC#F (NOTE ORD
0012     0B 3E
0014     0C 6B
0016     0D BE
0018     0F 2D
001A     13 80              .DBYTE $1380,$158C,$17D2,$1A56
001C     15 8C
001E     17 D2
0020     1A 56
0022     08 0C     TONTAB   .DBYTE $080C,$020A,$020C,$020E        HOLDS PAIRS OF OFFSETS FROM START
0024     02 0A
0026     02 0C
0028     02 0E
002A     04 0A              .DBYTE $040A,$040C,$040E,$060A        OF FRQINC.  EACH BYTE FOR ONE TON
002C     04 0C
002E     04 0E
0030     06 0A
0032     06 0C              .DBYTE $060C,$060E,$08CA,$080E        TONTAB WITH DIGIT NUMBER FROM 00
0034     06 0E
0036     08 0A
0038     08 0E
003A     00 00              .DBYTE $0000
003C               DIGTAB   *=*+NDIGIT             SPACE FOR THE DIGITS OF THE TELEPHONE NUMBER
0047                        *=*+1                  LOCATION FOR LAST KEYCODE
0048               MAXKEY   =$0C                   HIGHEST DIGIT ALLOWED IN TELEPHONE NUMBER
0048               INH      =$F9                   KIM DISPLAY VARIABLES
0048               POINTH   =$FB
0048               DAC      =$1700
0048               DACDIR   =$1701
0048               PORTB    =$1702
0048               PBDIR    =$1703
0048               T1024    =$1707
0048               TSTAT    =$1707
0048               DUMMY    =$194B
0048               SCANDS   =$1F1F
0048               GETKEY   =$1F6A
0048                        *=$0100
0100     A2 00     TONES    LDX   #$0C
0102     86 0A     TONES1   STX   TEMPX            SAVE X, IT WILL BE ALTERED BY SETUP
0104     B5 3C              LDA   DIGTAB,X
0106     20 11 01           JSR   SETUP            GET READY AND THEN MAKE THE TONES
0109     A6 0A              LDX   TEMPX
010B     E8                 INX
010C     E4 0B              CPX   NDIGIT           DONE ALL DIGITS OF NUMBER?
010E     30 F2              BMI   TONES1
0110     60                 RTS
0111     C9 0C     SETUP    CMP   #MAXKEY          KEYS ABOVE MAXKEY NOT ALLOWED
0113     10 2A              BPL   SETUP1
0115     0A                 ASL   A
0116     A8                 TAY
0117     B9 22 00           LDA   TONTAB,Y         GET OFFSET INTO FRQINC FOR FIRST TONE
011A     AA                 TAX
011B     B5 10              LDA   FRQINC,X         GET FREQ INCR FOR FIRST TONE
011D     85 01              STA   INC1I            INTEGER PART
011F     B5 11              LDA   FRQINC+1,X
0121     85 00              STA   INC1F            FRACTIONAL PART
0123     B9 23 00           LDA   TONTAB+1,Y       GET OFFSET INTO FRQINC FOR SECOND TONE
0126     AA                 TAX
0127     B5 10              LDA   FRQINC,X
0129     85 06              STA   INC2I
012B     B5 11              LDA   FRQINC+1,X
```

Listing 1 continued on page 146

Listing 1 continued:

```
0120  85 05             STA   INC2F
012F  20 40 01          JSR   SOUND
0132  A9 4A             LDA   #$4A
0134  8D 07 17          STA   T1024
0137  8D 07 17          STA   T1024
013A  AD 07 17  DLY     LDA   TSTAT        PAUSE BETWEEN SENDING OF TONE PAIRS
013D  10 FB             BPL   DLY
013F  60        SETUP1  RTS
0140  A0 00     SOUND   LDY   #$00         THIS SUBROUTINE GENERATES THE TONE PAIRS
0142  A9 92             LDA   #$92
0144  8D 07 17          STA   T1024
0147  8D 07 17          STA   T1024
014A  18        SOUND1  CLC                THIS LOOP TAKES 63 STATES TO EXECUTE
014B  B1 03             LDA   (PNT1I),Y    GET VALUE FROM SINTAB WITH INDIRECT ADDRESSING
014D  71 08             ADC   (PNT2I),Y    Y=0. PNT#I, PAGE# CONTAINS THE ADDRESS
014F  8D 00 17          STA   DAC
0152  18                CLC
0153  A5 02             LDA   PNT1F        INCREASE THE POINTER TO SINTAB
0155  65 00             ADC   INC1F        BY ADDING VALUE FROM FRQINC
0157  85 02             STA   PNT1F
0159  A5 03             LDA   PNT1I
015B  65 01             ADC   INC1I
015D  85 03             STA   PNT1I
015F  18                CLC
0160  A5 07             LDA   PNT2F
0162  65 05             ADC   INC2F
0164  85 07             STA   PNT2F
0166  A5 08             LDA   PNT2I
0168  65 06             ADC   INC2I
016A  85 08             STA   PNT2I
016C  AD 07 17          LDA   TSTAT        CHECK IF TIMER OUT YET (NEGATIVE)
016F  10 D9             BPL   SOUND1       LOOP AGAIN IF NOT
0171  60                RTS
0172                    *=$0200
0200  A2 FF     DIAL    LDX   #$FF         EXECUTION STARTS HERE
0202  9A                TXS                INITIALIZE STACK POINTER
0203  20 23 02          JSR   INIT
0206  20 1F 1F  LOOK    JSR   SCANDS       LIGHT DISPLAY FOR A WHILE
0209  20 6A 1F          JSR   GETKEY       LOOK FOR KEY CLOSURE
020C  A6 0B             LDX   NDIGIT
020E  D5 3C             CMP   DIGTAB,X     CHANGED FROM LAST CODE?
0210  95 3C             STA   DIGTAB,X
0212  F0 F2             BEQ   LOOK         NO, LOOK AGAIN
0214  C9 15             CMP   #$15         LOOK AGAIN IF IT JUST SAYS KEY RELEASED
0216  F0 EE             BEQ   LOOK
0218  20 63 02          JSR   CMND         IT IS A NEW KEY, LET CMND HAVE IT
021B  B0 E9             BCS   LOOK         IF CARRY SET, CMND TOOK IT
021D  20 3D 02          JSR   DIGIT        ELSE GIVE IT TO DIGIT
0220  B8                CLV
0221  50 E3             BVC   LOOK
0223  A9 FF     INIT    LDA   #$FF         SET DIRECTION REGISTERS
0225  8D 01 17          STA   DACDIR       OUTPUTS
0228  8D 03 17          STA   PBDIR        OUTPUTS
022B  A9 00             LDA   #$00
022D  8D 02 17          STA   PORTB
0230  A9 0F     ZERO    LDA   #$0F         STORE $0F VALUES INTO TELEPHONE NUMBER
0232  A6 0B             LDX   NDIGIT
0234  CA        ZERO1   DEX
0235  95 3C             STA   DIGTAB,X
0237  D0 FB             BNE   ZERO1
0239  20 4C 02          JSR   SHIFT2       PUT F'S IN DISPLAY
023C  60                RTS
023D  C9 0C     DIGIT   CMP   #MAXKEY      KEYS ABOVE MAXKEY NOT ALLOWED
023F  10 21             BPL   DIGIT1
0241  A2 00     SHIFT   LDX   #$00         SHIFT NEW DIGIT INTO TELEPHONE NUMBER
0243  B5 3D     SHIFT1  LDA   DIGTAB+1,X
0245  95 3C             STA   DIGTAB,X
0247  E8                INX
0248  E4 0B             CPX   NDIGIT
024A  30 F7             BMI   SHIFT1
024C  A2 41     SHIFT2  LDX   #DIGTAB+5    SETUP LOOP
024E  A0 FB             LDY   #POINTH
0250  B5 00     SHIFT3  LDA   00,X         THIS LOOP SHIFTS DIGITS THRU DISPLAY VARIABLES
0252  0A                ASL   A
0253  0A                ASL   A
0254  0A                ASL   A
0255  0A                ASL   A
0256  15 01             ORA   $01,X
0258  99 00 00          STA   $00,Y
025B  E8                INX
```

Listing 1 continued on page 148

```
025C  E8                  INX
025D  88                  DEY
025E  C0 F9               CPY   #INH        DOWN TO LOWEST LOCATION YET?
0260  10 EE               BPL   SHIFT3
0262  60        DIGIT1    RTS
0263  18        CMND      CLC
0264  C9 10               CMP   #$10
0266  10 01               BPL   CMND1
0268  60                  RTS               RETURN IF KEYCODE IS $00 TO $0F
0269  C9 10     CMND1     CMP   #$10        AD KEY GENERATES TONES
026B  D0 05               BNE   CMND2
026D  20 00 01            JSR   TONES
0270  38                  SEC
0271  60                  RTS
0272  C9 13     CMND2     CMP   #$13        GO KEY RESETS EVERYTHING
0274  D0 05               BNE   CMND3
0276  20 30 02            JSR   ZERO
0279  38                  SEC
027A  60                  RTS
027B  C9 12     CMND3     CMP   #$12        + KEY AVAILABLE FOR USER
027D  D0 05               BNE   CMND4
027F  20 4B 19            JSR   DUMMY
0282  38                  SEC
0283  60                  RTS
0284  C9 11     CMND4     CMP   #$11        DA KEY GENERATES PULSES
0286  D0 04               BNE   CMND5
0288  20 8D 02            JSR   PULSE
028B  38                  SEC
028C  60        CMND5     RTS
028D  A2 00     PULSE     LDX   #$00
028F  86 0A     PULSE1    STX   TEMPX       SAVE X, CLICK MODIFIES X
0291  B5 3C               LDA   DIGTAB,X    GET NEXT DIGIT OF TELEPHONE NUMBER
0293  20 9E 02            JSR   CLICK
0296  A6 0A               LDX   TEMPX
0298  E8                  INX
0299  E4 0B               CPX   NDIGIT      CHECK IF ALL DIGITS OF NUMBER HAVE BEEN PASSED TO CLI
029B  30 F2               BMI   PULSE1
029D  60                  RTS
029E  C9 0A     CLICK     CMP   #$0A        PULSE DIALING ONLY GOOD FOR DIGITS 0-9
02A0  10 40               BPL   CLICK5
02A2  C9 00               CMP   #$00
02A4  D0 02               BNE   CLICK1
02A6  A9 0A               LDA   #$0A        MAKE 0 DIGIT HAVE TEN PULSES
02A8  A8        CLICK1    TAY
02A9  A2 01     CLICK2    LDX   #$01
02AB  8E 02 17            STX   PORTB       START INTERRUPTION
02AE  A2 25               LDX   #$25
02B0  8E 07 17            STX   T1024
02B3  8E 07 17            STX   T1024
02B6  AE 07 17  CLICK3    LDX   TSTAT       HOLD FOR 35 MSEC
02B9  10 FB               BPL   CLICK3
02BB  A2 00               LDX   #$00
02BD  8E 02 17            STX   PORTB       RE-ESTABLISH CONNECTION
02C0  A2 3D               LDX   #$3D
02C2  8E 07 17            STX   T1024
02C5  8E 07 17            STX   T1024
02C8  AE 07 17  CLICK4    LDX   TSTAT       HOLD FOR 65 MSEC
02CB  10 FB               BPL   CLICK4
02CD  88                  DEY
02CE  D0 D9               BNE   CLICK2      ANY MORE PULSES TO GO?
02D0  A0 01               LDY   #$01
02D2  A2 FF     DLY1      LDX   #$FF        DO THIS LOOP TWICE FOR A 0.5 SEC PAUSE BETWEEN DIGITS
02D4  8E 07 17            STX   T1024
02D7  8E 07 17            STX   T1024
02DA  AE 07 17  DLY2      LDX   TSTAT
02DD  10 FB               BPL   DLY2
02DF  88                  DEY
02E0  10 F0               BPL   DLY1
02E2  60        CLICK5    RTS
02E3                      *=$0300
0300  40        SINTAB    .BYTE 64,65,67,68,70,71,73,74
0301  41
0302  43
0303  44
0304  46
0305  47
0306  49
0307  4A
0308  4C                  .BYTE 76,77,79,80,82,83,85,86
0309  4D
030A  4F
```

Listing 1 continued on page 150

SuperSoft announces a complete line of CP/M* compatible software

ACCOUNTING

SuperSoft offers a complete, interactive accounting system at an affordable price. We started with the Osborne accounting system, the standard of the industry, and made it even better. Since either the General Ledger and the Accounts Payable/Receivable can stand alone, you do not need to purchase the entire system at once. This means that you can start with what you need and up-grade later. Look for a compatible Payroll package in the future.

ACCOUNTS PAYABLE/RECEIVABLE: A complete, user oriented package which features:

automatic postings to general ledger (optional)

accounts payable: • check printing with invoice • invoice aging

accounts receivable: • progress billing • customer statements • partial invoice payments • invoice aging

The entire package is menu driven and easy to learn and use. It incorporates error checking and excellent user displays. This package can be used stand alone or with the General Ledger below. Requires: 48K CP/M, terminal with cursor positioning and clear screen, one 8" disk or Two 5" disks. CBASIC2 required.

Supplied with extensive user manual: $200.00. Manual alone: $20.00.

GENERAL LEDGER: A complete, user oriented package which features:

- Accepts postings from external programs (i.e. AP/AR above)
- Accepts directly entered postings
- Maintains account balances for current month, quarter, and year and previous three quarters
- Financial reports: trial balance, income statement balance sheet, and more.

Completely menu driven and easy to learn and use. Excellent displays and error checking for trouble free operation. Can be used stand alone or with Accounts Payable/Receivable above. Minimal requirements: 48K CP/M, terminal with cursor positioning, home and clear screen, one 8" disk or Two 5" disks. CBASIC2 required.

Supplied with extensive user manual: $200.00. Manual alone: $20.00.

TEXT PROCESSING

TFS—Text Formatting System: An extremely powerful formatter. More than 50 commands. Features include:

- left & right margin justification
- headers and footers
- page numbering
- chaptering
- dynamic insertion from disk file
- exdented & indented paragraphs
- works with any printer or CRT
- tabbing
- auto paragraphing
- auto list numbering
- centering
- user defined macros
- underlining and backspace
- much, much more

TFS lets you make multiple copies of any text. For example: Personalized form letters complete with name & address & other insertions from a disk file. Text is not limited to the size of RAM making TFS perfect for reports, manuals or any big job.

Text is entered using CP/M standard editor or most any CP/M compatible editor. TFS will link completely with Super-M-List making personalized form letters easy.

Requires: 24K CP/M.

Supplied with extensive user manual: $85.00. Manual alone: $20.00.

Source to TFS in 8080 assembler (can be assembled using standard CP/M assembler) plus user manual: $250.00.

MAILING LIST

SUPER-M-LIST: A complete, easy to use mailing list program package. Allows for two names, two address, city, state, zip and a three digit code field for added flexibility. Super-M-List can sort on any field and produce mailing labels direct to printer or disk file for later printing or use by other programs. Super-M-List is the perfect companion to TFS. Handles 1981 Zip Codes!

Requires: 24K CP/M.

Supplied with complete user manual: $75.00. Manual alone: $10.00

UTILITIES

Utility pack #1: A collection of programs that you will find useful and maybe even necessary in your daily work (we did!). Includes:

CMP: Compare two files for equality.
ARCHIVER: Compacts many files into one, useful when you run out of directory entries.
SORT: In core sort of variable length records.
XDIR: Extended, alphabetical directory listing with groupings by common extension.
PRINT: Formatted listings to printer.
PG: Lists files to CRT a page at a time.
...plus more...

Requires: 24K CP/M.

Supplied with instructions on discette: $50.00.

SYSTEM MAINTENANCE

DIAGNOSTICS I: Easily the most comprehensive set of CP/M compatible system check-out programs ever assembled. Finds hardware errors in your system, confirms suspicions, or just gives your system a clean bill of health. Tests:

- Memory
- Disk
- CPU (8080/8085/Z80)
- Printer
- Terminal

To our knowledge the CPU test is the first of its kind anywhere. Diagnostics I can help you find problems before they become serious. A good set of diagnostic routines are a must in any program library.

Minimal requirements: 24K CP/M. Supplied with complete user manual: $50.00 Manual alone: $15.00.

SOFTWARE SECURITY

ENCODE/DECODE: A complete software security system for CP/M. Encode/Decode is a sophisticated coding program package which transforms data stored on disk into coded text which is completely unrecognizable. Encode/Decode supports multiple security levels and passwords. A user defined combination (One billion possible) is used to code and decode a file. Uses are unlimited. Below are a few examples:

- data bases
- payroll files
- programs
- general ledger
- correspondence
- tax records
- inventory
- accounts pay/rec
- mailing lists

Encode/Decode is available in two versions:

Encode/Decode I provides a level of security suitable for normal use. Encode/Decode II provides enhanced security for the most demanding needs. Both versions come supplied on discette and with a complete user manual.

Encode/Decode I: $50.00
Encode/Decode II: $100.00 Manual alone: $15.00

PROGRAMMING LANGUAGES

ENHANCED 'TINY' PASCAL: We still call it 'Tiny' but it's bigger and better than ever! This is the Famous Chung/Yuen 'Tiny' Pascal with more features added. Features include:

- recursive procedures/functions
- FOR (loop)
- IF...THEN...ELSE
- READ & WRITE
- integer arithmetic
- sequential disk I/O
- WHILE
- REPEAT...UNTIL
- CASE
- one dimensional arrays
- 'PEAK' & 'POKE'
- more

'Tiny' Pascal is fast. Programs execute up to ten times faster than similar BASIC programs.

SOURCE TOO! We still distribute source, in 'Tiny' Pascal, on each discette sold. You can even recompile the compiler, add features or just gain insight into compiler construction.

'Tiny' Pascal is perfect for writing text processors, real time control systems, virtually any application which requires high speed. Requires: 36K CP/M. Supplied with complete user manual and source on discette: $85.00.

Manual alone: $10.00.

INTERCOMPUTER COMMUNICATIONS

TERM: a complete intercommunications package for linking your computer to other computers. Link either to other CP/M computers or to large timesharing systems. TERM is comparable to other systems but costs less, delivers more and source is provided on discette!

With TERM you can send and receive ASCII and Hex files (COM too, with included convertion program) with any other CP/M computer which has TERM or compatible package. Allows real time communication between users on separate systems as well as acting as timesharing terminal.

- Engage/disengage printer
- terminal mode for timesharing between systems
- send files
- error checking and auto retry
- conversational mode
- receive files

Requires: 32K CP/M.

Supplied with user manual and 8080 source code: $100.00

Manual alone: $15.00.

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*CP/M REGISTERED TRADEMARK DIGITAL RESEARCH

Circle 92 on inquiry card.

Listing 1 continued:

```
211  030B  50
211  030C  52
211  030D  53
211  030E  55
211  030F  56
212  0310  58        .BYTE 88,89,91,92,93,95,96,97
212  0311  59
212  0312  5B
212  0313  5C
212  0314  5D
212  0315  5F
212  0316  60
212  0317  61
213  0318  63        .BYTE 99,100,101,103,104,105,106,107
213  0319  64
213  031A  65
213  031B  67
213  031C  68
213  031D  69
213  031E  6A
213  031F  6B
214  0320  6C        .BYTE 108,109,111,112,113,114,115,115
214  0321  6D
214  0322  6F
214  0323  70
214  0324  71
214  0325  72
214  0326  73
214  0327  73
215  0328  74        .BYTE 116,117,118,119,120,120,121,122
215  0329  75
215  032A  76
215  032B  77
215  032C  78
215  032D  78
215  032E  79
215  032F  7A
216  0330  7A        .BYTE 122,123,123,124,124,125,125,125
216  0331  7B
216  0332  7B
216  0333  7C
216  0334  7C
216  0335  7D
216  0336  7D
216  0337  7D
217  0338  7E        .BYTE 126,126,126,127,127,127,127,127
217  0339  7E
217  033A  7E
217  033B  7F
217  033C  7F
217  033D  7F
217  033E  7F
217  033F  7F
218  0340  7F        .BYTE 127,127,127,127,127,127,126,126
218  0341  7F
218  0342  7F
218  0343  7F
218  0344  7F
218  0345  7F
218  0346  7E
218  0347  7E
219  0348  7E        .BYTE 126,125,125,125,124,124,123,123
219  0349  7D
219  034A  7D
219  034B  7D
219  034C  7C
219  034D  7C
219  034E  7B
219  034F  7B
220  0350  7A        .BYTE 122,122,121,120,120,119,118,117
220  0351  7A
220  0352  79
220  0353  78
220  0354  78
220  0355  77
220  0356  76
220  0357  75
221  0358  74        .BYTE 116,115,115,114,113,112,111,109
221  0359  73
221  035A  73
221  035B  72
```

Listing 1 continued on page 152

Listing 1 continued:

```
221   035C   71
221   035D   70
221   035E   6F
221   035F   6D
222   0360   6C            .BYTE 108,107,106,105,104,103,101,100
222   0361   6B
222   0362   6A
222   0363   69
222   0364   68
222   0365   67
222   0366   65
222   0367   64
223   0368   63            .BYTE 99,97,96,95,93,92,91,89
223   0369   61
223   036A   60
223   036B   5F
223   036C   5D
223   036D   5C
223   036E   5B
223   036F   59
224   0370   58            .BYTE 88,86,85,83,82,80,79,77
224   0371   56
224   0372   55
224   0373   53
224   0374   52
224   0375   50
224   0376   4F
224   0377   4D
225   0378   4C            .BYTE 76,74,73,71,70,68,67,65
225   0379   4A
225   037A   49
225   037B   47
225   037C   46
225   037D   44
225   037E   43
225   037F   41
226   0380   40            .BYTE 64,62,60,59,57,56,54,53
226   0381   3E
226   0382   3C
226   0383   3B
226   0384   39
226   0385   38
226   0386   36
226   0387   35
227   0388   33            .BYTE 51,50,48,47,45,44,42,41
227   0389   32
227   038A   30
227   038B   2F
227   038C   2D
227   038D   2C
227   038E   2A
227   038F   29
228   0390   27            .BYTE 39,38,36,35,34,32,31,30
228   0391   26
228   0392   24
228   0393   23
228   0394   22
228   0395   20
228   0396   1F
228   0397   1E
229   0398   1C            .BYTE 28,27,26,24,23,22,21,20
229   0399   1B
229   039A   1A
229   039B   18
229   039C   17
229   039D   16
229   039E   15
229   039F   14
230   03A0   13            .BYTE 19,18,16,15,14,13,12,12
230   03A1   12
230   03A2   10
230   03A3   0F
230   03A4   0E
230   03A5   0D
230   03A6   0C
230   03A7   0C
231   03A8   0B            .BYTE 11,10,9,8,7,7,6,5
231   03A9   0A
231   03AA   09
231   03AB   08
231   03AC   07
```

Listing 1 continued on page 154

By Netronics

ASCII/BAUDOT, STAND ALONE

Computer Terminal

COMPLETE FOR ONLY . . . 149^{95}

The Netronics ASCII/BAUDOT Computer Terminal Kit is a microprocessor-controlled, stand alone keyboard/terminal requring no computer memory or software. It allows the use of either a 64 or 32 character by 16 line professional display format with selectable baud rate, RS232-C or 20 ma. output, full cursor control and 75 ohm composite video output.

The keyboard follows the standard typewriter configuration and generates the entire 128 character ASCII upper/lower case set with 96 printable characters. Features include onboard regulators, selectable parity, shift lock key, alpha lock jumper, a drive capability of one TTY load, and the ability to mate directly with almost any computer, including the new Explorer/85 and ELF products by Netronics.

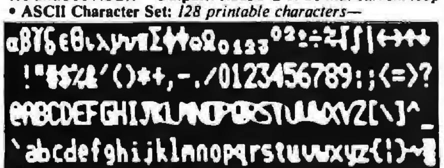
The Computer Terminal requires no I/O mapping and includes 1k of memory, character generator, 2 key rollover, processor controlled cursor control, parallel ASCII/BAUDOT to serial conversion and serial to video processing—fully crystal controlled for superb accuracy. PC boards are the highest quality glass epoxy for the ultimate in reliability and long life.

VIDEO DISPLAY SPECIFICATIONS

The heart of the Netronics Computer Terminal is the microprocessor-controlled Netronics Video Display Board (VID) which allows the terminal to utilize either a parallel ASCII or BAUDOT signal source. The VID converts the parallel data to serial data which is then formatted to either RS232-C or 20 ma. current loop output, which can be connected to the serial I/O on your computer or other interface, i.e., Modem.

When connected to a computer, the computer must echo the character received. This data is received by the VID which processes the information, converting to data to video suitable to be displayed on a TV set (using an RF modulator) or on a video monitor. The VID generates the cursor, horizontal and vertical sync pulses and performs the housekeeping relative to which character and where it is to be displayed on the screen.

Video Output: *1.5 P/P into 75 ohm (EIA RS-170)* • **Baud Rate:** *110 and 300 ASCII* • **Outputs:** *RS232-C or 20 ma. current loop* • **ASCII Character Set:** *128 printable characters—*



BAUDOT Character Set: *A B C D E F G H I J K L M N O P Q R S T U V W X Y Z - ? : • 3 $ # ( ) . , 9 0 1 4 ! 5 7 ; 2 / 6 8 •* **Cursor Modes:** *Home, Backspace, Horizontal Tab, Line Feed, Vertical Tab, Carriage Return. Two special cursor sequences are provided for absolute and relative X-Y cursor addressing* • **Cursor Control:** *Erase, End of Line, Erase of Screen, Form Feed, Delete* • **Monitor Operation:** *50 or 60Hz (jumper selectable.*

Continental U.S.A. Credit Card Buyers Outside Connecticut

CALL TOLL FREE 800-243-7428

To Order From Connecticut Or For Technical Assistance, Etc. Call (203) 354-9375

Netronics R&D Ltd., Dept. PE-9
333 Litchfield Road, New Milford, CT 06776

Please send the items checked below—

- ☐ **Netronics Stand Alone ASCII Keyboard/Computer Terminal Kit, $149.95** plus $3.00 postage & handling.
- ☐ **Deluxe Steel Cabinet** for Netronics Keyboard/Terminal In Blue/Black Finish, **$19.95** plus $2.50 postage and handling.
- ☐ **Video Display Board Kit** alone (less keyboard), **$89.95** plus $3 postage & handling.
- ☐ **12" Video Monitor** (10 MHz bandwidth) fully assembled and tested, **$139.95** plus $5 postage and handling.
- ☐ **RF Modulator Kit** (to use your TV set for a monitor), **$8.95** postpaid.
- ☐ **5 amp Power Supply Kit** In Deluxe Steel Cabinet (± 8VDC @ 5 amps, plus 6-8 VAC), **$39.95** plus $2 postage & handling.

Total Enclosed (Conn. res. add sales tax) $______
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☐ Visa ☐ **Master Charge** (Bank # ______)

Acct. # ______
Signature ______ Exp. Date ______
Print Name ______
Address ______
City ______
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Start Computing For Just $129.95 With An 8085-Based Professional Computer Kit—

Explorer/85

100% compatible with all 8080A and 8085 software & development tools!

No matter what your future computing plans may be, Level "A"—at $129.95—is your starting point.

Starting at just $129.95 for a Level "A" operating system, you can now build the exact computer you want. Explorer/85 can be your beginner's system, OEM controller, or IBM-formatted 8' disk small business system... yet you're never forced to spend a penny for a component or feature you don't want and you can expand in small, affordable steps!

Now, for just $129.95, you can own the first level of a fully expandable computer with professional capabilities—a computer which features the advanced Intel 8085 cpu, *thereby giving you immediate access to all software and development tools that exist for both the 8085 and its 8080A predecessor (they are 100% software compatible)*—a computer which features onboard S-100 bus expansion—plus instant conversion to mass storage disk memory with either 5-1/4" diskettes or standard IBM-formatted 8" disks.

For just $129.95 (plus the cost of a power supply, keyboard/terminal and RF modulator, if you don't have them already), Explorer/85 lets you begin *computing* on a significant level... *applying* the principles discussed in leading computer magazines... *developing* "state of the art" computer solutions for both the industrial and leisure environment.

Level "A" Specifications

Explorer/85's Level "A" system features the advanced Intel 8085 cpu, an 8355 ROM with 2k deluxe monitor/operating system, and an 8155 ROM-I/O—all on a single motherboard with room for RAM/ROM/PROM/EPROM and S-100 expansion, *plus* generous prototyping space.

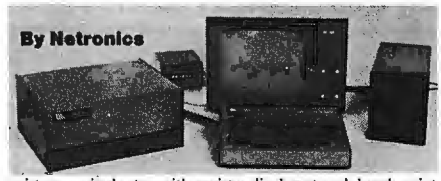
(Level "A" makes a perfect OEM controller for industrial applications and is available in a special Hex Version which can be programmed using the Netronics Hex Keypad/Display.)

Level "A" at $129.95 is a complete operating system, perfect for beginners, hobbiests, or industrial controller use.

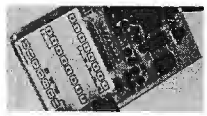
PC Board: glass epoxy, plated through holes with solder mask • **I/O:** provisions for 25-pin (DB25) connector for terminal serial I/O, which can also support a paper tape reader ...provision for 24-pin DIP socket for hex keyboard/display... cassette tape recorder input... cassette tape recorder output... cassette tape control output... speaker output... LED output indicator on SOD (serial output) line... printer interface (less drivers)... total of four 8-bit plus one 6-bit I/O ports • **Crystal Frequency:** 6.144 MHz • **Control Switches:** reset and user (RST 7.5) interrupt... additional provisions for RST 5.5, 6.5 and TRAP interrupts onboard • **Counter/Timer:** programmable, 14-bit binary • **System RAM:** 256 bytes located at F800, ideal for smaller systems and for use as an isolated stack area in expanded systems... RAM expandable to 64k via S-100 bus or 4K on motherboard.

System Monitor (Terminal Version): 2k bytes of deluxe system monitor ROM located at F000 leaving 0000 free for user RAM/ROM. Features include tape load with labeling... tape dump with labeling... examine/change contents of memory ...insert data... warm start... examine and change all registers... single step with register display at each break point, a debugging/training feature... go to execution address... move blocks of memory from one location to another... fill blocks of memory with a constant... display blocks of memory ... automatic baud rate selection... variable display line length control (1-255 characters/line)... channelized I/O monitor routine with 8-bit parallel output for high speed printer... serial console in and console out channel so that monitor can communicate with I/O ports.

System Monitor (Hex Version): Tape load with labeling... tape dump with labeling... examine/change contents of memory... insert data... warm start... examine and change all registers... single step with register display at each break point ...go to execution address. Level "A" in the *Hex Version* makes a perfect controller for industrial applications and can be programmed using the Netronics Hex Keypad/Display.



By Netronics



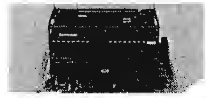
Hex Keypad/Display.

Hex Keypad/Display Specifications

Calculator type keypad with 24 system defined and 16 user defined keys. 6 digit calculator type display which displays full address plus data as well as register and status information.

Level "B" Specifications

Level "B" provides the S-100 signals plus buffers/drivers to support up to six S-100 bus boards and includes: address decoding for onboard 4k RAM expansion select-able in 4k blocks... address decoding for onboard 8k EPROM expansion selectable in 8k blocks... address and data bus drivers for onboard expansion... wait state generator (jumper selectable), to allow the use of slower memories... two separate 5 volt regulators.



Explorer/85 with Level "C" card cage.

Level "C" Specifications

Level "C" expands Explorer's motherboard with a card cage, allowing you to plug up to six S-100 cards directly into the motherboard. Both cage and cards are neatly contained inside Explorer's deluxe steel cabinet. Level "C" includes a sheet metal superstructure, a 5-card gold plated S-100 extension PC board which plugs into the motherboard. Just add required number of S-100 connectors

Level "D" Specifications

Level "D" provides 4k or RAM, power supply regulation, filtering decoupling components and sockets to expand your Explorer/85 memory to 4k (plus the original 256 bytes located in the 8155A). The static RAM can be located anywhere from 0000 to EFFF in 4k blocks.

Level "E" Specifications

Level "E" adds sockets for 8k of EPROM to use the popular Intel 2716 or the TI 2516. It includes all sockets, power supply regulator, heat sink, filtering and decoupling components. Sockets may also be used for soon to be available RAM IC's (allowing for up to 12k of onboard RAM).

Order A Coordinated Explorer/85 Applications Pak!

Experimenter's Pak (SAVE $12.50)—Buy Level "A" and Hex Keypad/Display for **$199.90** and get FREE Intel 8085 user's manual plus FREE postage& handling!

Student Pak (SAVE $24.45)—Buy Level "A," ASCII Keyboard/Computer Terminal, and Power Supply for **$319.85** and get FREE RF Modulator plus FREE Intel 8085 user's manual plus FREE postage & handling!

Engineering Pak (SAVE $41.00)—Buy Levels "A," "B," "C," "D," and "E" with Power Supply, ASCII Keyboard/Computer Terminal, and six S-100 Bus Connectors for **$514.75** and get 10 FREE computer grade cassette tapes plus FREE 8085 user's manual plus FREE postage & handling!

Business Pak (SAVE $89.95)—Buy Explorer/85 Levels "A," "B," and "C" (with cabinet), Power Supply, ASCII Keyboard/Computer Terminal (with cabinet), 16k RAM, 12" Video Monitor, North Star 5-1/4" Disk Drive (includes North Star BASIC) with power supply and cabinet, all for just **$1599.40** and get 10 FREE 5-1/4" minidiskettes ($49.95 value) plus FREE 8085 user's manual plus FREE postage & handling!

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Netronics R&D Ltd., Dept. RE 10
333 Litchfield Road, New Milford, CT 06676

Please send the items checked below—

- ☐ **Explorer/85 Level "A" Kit** (ASCII Version), **$129.95** plus $3 p&h.
- ☐ **Explorer/85 Level "A" Kit** (Hex Version), **$129.95** plus $3 p&h.
- ☐ **8k Microsoft BASIC** on cassette tape, **$64.95** postpaid.
- ☐ **8k Microsoft BASIC in ROM Kit** (requires Levels "B," "D," and "E"), **$99.95** plus $2 p&h.
- ☐ **Level "B" (S-100) Kit, $49.95** plus $2 p&h.
- ☐ **Level "C" (S-100 6-card expander) Kit, $39.95** plus $2 p&h.
- ☐ **Level "D" (4k RAM) Kit, $69.95** plus $2 p&h.
- ☐ **Level "E" (EPROM/ROM) Kit, $5.95** plus 50¢ p&h.
- ☐ **Deluxe Steel Cabinet** for Explorer/85, **$49.95** plus$3 p&h.
- ☐ **ASCII Keyboard/Computer Terminal Kit** (features a full 128 character set, upper & lower case, full cursor control, 75 ohm video output convertible to baudot output, selectable baud rate, RS232-C or 20 ma. I/O, 32 or 64 character by 16 line formats, and can be used with either a CRT monitor or a TV set (if you have an RF modulator), **$149.95** plus $2.50 p&h.
- ☐ **Hex Keypad/Display Kit, $69.95** plus $2 p&h.
- ☐ **Deluxe Steel Cabinet** for ASCII Keyboard/Terminal, **$19.95** plus $2.50 p&h.
- ☐ **Power Supply Kit** (± 8V @ 5 amps) in deluxe steel cabinet, **$39.95** plus $2 p&h.
- ☐ **Gold Plated S-100 Bus Connectors, $4.85** each, postpaid.
- ☐ **RF Modulator Kit** (allows you to use your TV set as a monitor), **$8.95** postpaid.
- ☐ **16k RAM Kit** (S-100 Board expands to 64k), **$199.95** plus $2 p&h.
- ☐ **32k RAM Kit, $329.95** plus $2 p&h.
- ☐ **48K RAM Kit, $459.95** plus $2 p&h.
- ☐ **64k RAM Kit, $589.95** plus $2 p&h.
- ☐ **16k RAM Expansion Kit** (to expand any of the above up to 64k), **$139.95** plus$2 p&h each.
- ☐ **Intel 8085 cpu User's Manual, $7.50** postpaid.
- ☐ **Special Computer Grade Cassette Tapes, $1.90** each or 3 for **$5**, postpaid.
- ☐ **12" Video Monitor** (10 MHz bandwidth), **$139.95** plus $5 p&h.
- ☐ **North Star Double Density Floppy Disk Kit** (One Drive) for Explorer/85 (includes 3 drive S-100 controller, DOS, and extended BASIC with personalized disk operating system—just plug it in and you're up and running!), **$699.95** plus $5 p&h.
- ☐ **Power Supply Kit** for North Star Disk Drive, **$39.95** plus $2 p&h.
- ☐ **Deluxe Case** for North Star Disk Drive, **$39.95** plus $2 p&h.
- ☐ **Experimenter's Pak** (see above), **$199.90** postpaid.
- ☐ **Student Pak** (see above), **$319.85** postpaid.
- ☐ **Engineering Pak** (see above), **$514.75** postpaid.
- ☐ **Business Pak** (see above), **$1599.40** postpaid.

Total Enclosed $ ______
(Conn. res. add sales tax) By—
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Print Name ______
Address ______
City ______
State ______ Zip ______

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Circle 96 on inquiry card.

Circle 97 on inquiry card.

Listing 1 continued:

```
231  03AD  07
231  03AE  06
231  03AF  05
232  03B0  05      .BYTE 5,4,4,3,3,2,2,2
232  03B1  04
232  03B2  04
232  03B3  03
232  03B4  03
232  03B5  02
232  03B6  02
232  03B7  02
233  03B8  01      .BYTE 1,1,1,0,0,0,0,0
233  03B9  01
233  03BA  01
233  03BB  00
233  03BC  00
233  03BD  00
233  03BE  00
233  03BF  00
234  03C0  00      .BYTE 0,0,0,0,0,0,1,1
234  03C1  00
234  03C2  00
234  03C3  00
234  03C4  00
234  03C5  00
234  03C6  01
234  03C7  01
235  03C8  01      .BYTE 1,2,2,2,3,3,4,4
235  03C9  02
235  03CA  02
235  03CB  02
235  03CC  03
235  03CD  03
235  03CE  04
235  03CF  04
236  03D0  05      .BYTE 5,5,6,7,7,8,9,10
236  03D1  05
236  03D2  06
236  03D3  07
236  03D4  07
236  03D5  08
236  03D6  09
236  03D7  0A
237  03D8  0B      .BYTE 11,12,12,13,14,14,16,18
237  03D9  0C
237  03DA  0C
237  03DB  0D
237  03DC  0E
237  03DD  0E
237  03DE  10
237  03DF  12
238  03E0  13      .BYTE 19,20,21,22,23,24,26,27
238  03E1  14
238  03E2  15
238  03E3  16
238  03E4  17
238  03E5  18
238  03E6  1A
238  03E7  1B
239  03E8  1C      .BYTE 28,30,31,32,34,35,36,38
239  03E9  1E
239  03EA  1F
239  03EB  20
239  03EC  22
239  03ED  23
239  03EE  24
239  03EF  26
240  03F0  27      .BYTE 39,41,42,44,45,47,48,50
240  03F1  29
240  03F2  2A
240  03F3  2C
240  03F4  2D
240  03F5  2F
240  03F6  30
240  03F7  32
241  03F8  33      .BYTE 51,53,54,56,57,59,60,62
241  03F9  35
241  03FA  36
241  03FB  38
241  03FC  39
241  03FD  3B
```

Listing 1 continued on page 156

Listing 1 continued:

```
241  03FE  3C
241  03FF  3E
242  0400                        .END


END OF MOS/TECHNOLOGY 650X ASSEMBLY VERSION 5.1
NUMBER OF ERRORS =   0,  NUMBER OF WARNINGS =   0

        SYMBOL TABLE

SYMBOL   VALUE  LINE DEFINED        CROSS-REFERENCES

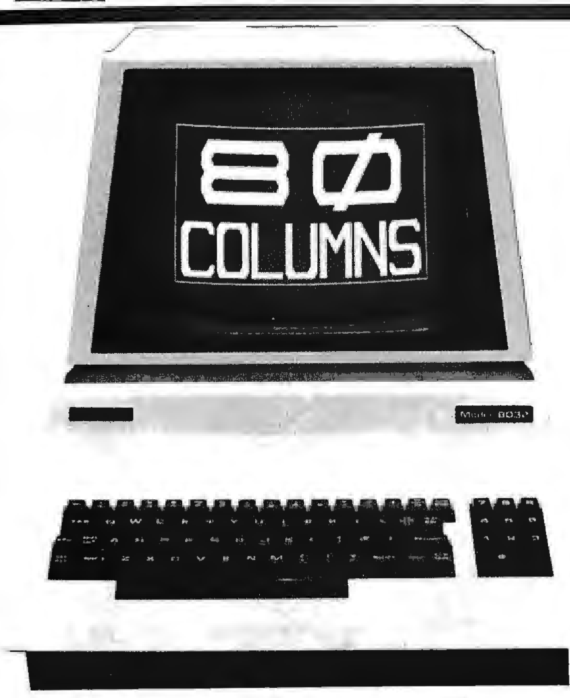
CLICK    029E        178   172
CLICK1   02A8        183   181
CLICK2   02A9        184   199
CLICK3   02B6        189   190
CLICK4   02C8        196   197
CLICK5   02E2        208   179
CMND     0263        145   105
CMND1    0269        149   147
CMND2    0272        154   150
CMND3    027B        159   155
CMND4    0284        164   160
CMND5    028C        168   165
DAC      1700         26    75
DACDIR   1701         27   111
DIAL     0200         94  ****
DIGIT    023D        122   107
DIGIT1   0262        144   123
DIGTAB   003C         21    38   100  101  118  125  126  130  171
DLY      013A         65    66
DLY1     02D2        201   207
DLY2     02DA        204   205
DUMMY    194B         32   161
FRQINC   0010         15    51    53   57   59
GETKEY   1F6A         34    98
INC1F    0000          2    54    78
INC1I    0001          3    52    81
INC2F    0005          7    60    85
INC2I    0006          8    58    88
INH      00F9         24   142
INIT     0223        110    96
LOOK     0206         97   102   104  106  109
MAXKEY   000C         23    45   122
NDIGIT   000B         13    21    42   99  116  128  175
PAGE1    0004          6  ****
PAGE2    0009         11  ****
PBDIR    1703         29   112
PNT1F    0002          4    77    79
PNT1I    0003          5    73    80   82
PNT2F    0007          9    84    86
PNT2I    0008         10    74    87   89
POINTH   00FB         25   131
PORTB    1702         28   114   185  192
PULSE    028D        169   166
PULSE1   028F        170   176
SCANDS   1F1F         33    97
SETUP    0111         45    39
SETUP1   013F         67    46
SHIFT    0241        124  ****
SHIFT1   0243        125   129
SHIFT2   024C        130   120
SHIFT3   0250        132   143
SINTAB   0300        210  ****
SOUND    0140         68    61
SOUND1   014A         72    91


SYMBOL  VALUE  LINE DEFINED         CROSS-REFERENCES

TEMPX   000A    12   37      40  170 173
TONES   0100    36  151
TONES1  0102    37   43
TONTAB  0022    17   49      55
TSTAT   1707    31   65      90  189 196 204
T1024   1707    30   63      64   70  71 187 188  194  195  202  203
ZERO    0230   115  156
ZERO1   0234   117  119
```

NEECO PROUDLY INTRODUCES

COMMODORE'S NEW 8000 SERIES (80 column) COMPUTERS



$1695 (available May/June '80)

CBM™ 8050 DUAL DRIVE FLOPPY DISK

The CBM 8050 Dual Drive Floppy Disk in an enhanced version of the intelligent CBM 2040 Disk Drive. The CBM 8050 has all of the features of the CBM 2040, and provides more powerful software capabilities, as well as nearly one megabyte of online storage capacity. The CBM 8050 supplies relative record files and automatic diskette initialization. It can copy all the files from one diskette to another without copying unused space. The CBM 8050 also offers improved error recovery and the ability to append to sequential files.

HARDWARE SPECIFICATIONS
Dual Drives
Two microprocessors
974K Bytes storage on two 5.25" diskettes (ss)
Tracks 70
Sectors 17-21
Soft sector format
IEEE-488 interface
Combination power (green) and error (red) indicator lights
Drive Activity indicator lights
Disk Operating System Firmware (12K ROM)
Disk Buffer (4K RAM)

FIRMWARE
DOS version 2.0
Sequential file manipulation
Sequential user files
Relative record files
Append to sequential files
Improved error recovery
Automatic diskette initialization
Automatic directory search
Command parser for syntax validation
Program load and save

CBM™ 8000 SERIES BUSINESS COMPUTERS

The new Commodore 8000 series computers offer a wide screen display to show you up to 80-character lines of information. Text editing and report formatting are faster and easier with the new wide-screen display. The 8000 series also provides a resident Operating System with expanded functional capabilities. You can use BASIC on the 8000 computers in both interactive and program modes, with expanded commands and functions for arithmetic, editing, and disk file management. The CBM 8000 series computers are ideally suited for the computing needs of the business marketplace.

SCREEN
2000 character display, organized into twenty-five 80-column lines
64 ASCII, 64 graphic characters
3 x 8 dot matrix characters
Green phosphor screen
Brightness control
Line spacing: 1½ in Text Mode
1 in Graphics Mode

KEYBOARD
73-key typewriter style keyboard with graphic capabilities
Repeat key functional with all keys

MEMORY
CBM 8016: 16K (15359 net) random access memory (RAM)
CBM 8032: 32K (31743 net) random access memory (RAM)

POWER REQUIREMENTS
Volts: 110V
Cycles: 60 Hz
Watts: 100

SCREEN EDITING CAPABILITIES
Full cursor control (up, down, right, left)
Character insert and delete
Reverse character fields
Overstriking
Return key sends entire line to CPU regardless of cursor position

INPUT/OUTPUT
Parallel port
IEEE-488 bus
2 cassette ports
Memory and I/O expansion connectors

FIRMWARE
24K or ROM contains:
BASIC (version 4.0) with direct (interactive) and indirect (program) modes
9-digit floating binary arithmetic
Tape and disk file handling software

The 8000 Series will be available May/June '80

Model 8016	Model 8032	2040 Dual Floppy
	Available Now	
$1495	$1795	$1295

commodore

CBM™ IEEE MODEM

SPECIFICATIONS
•Full or half duplex operation
•300 bits per second
•Standard IEEE 488 interface
•Switch selectable originate, off, answer-full duplex, test, half duplex
•Visible indicators are transmit data, receive data, carrier ready, test
•Frequency shifted modulation
•Bell 103/113 compatible

"Execeptional performance - even on noisy phone lines"

Available June/July

$395

VISICALC FOR CBM $150 (Available June)

*CBM is a registered trademark of Commodore. All prices and specifications are subject to change without notice.

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 Circle 102 on inquiry card. Circle 103 on inquiry card.

NEECO PROUDLY INTRODUCES

MULTI-CLUSTER

"Multi User Management System for Commodore CBM/PET Computers"*

UP TO 8 CBM/PETS MAY NOW SIMULTANEOUSLY ACCESS ONE 2040!

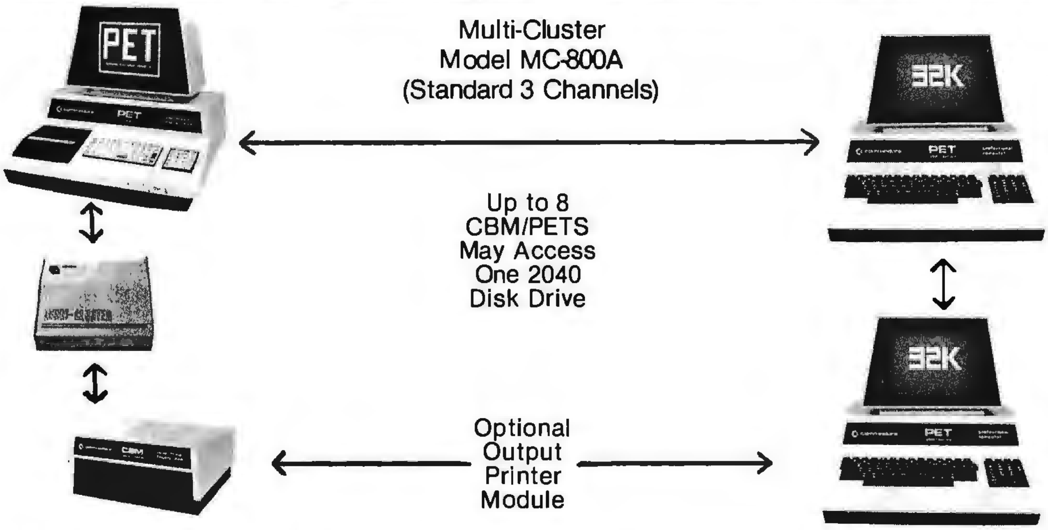
Channel Module CM-800

Multi-Cluster Model MC-800A Standard 3 Channels)

$995

- Up to 8 Channel (3 Standard) for CBM/PET Computers.
- Up to 8 CBM/PETS can multi-use one Commodore 2040 dual disk drive simultaneously with equal access.
- Multi-Cluster supports all 2040 disk O/S commands including sequential, random access, and user files.
- Multi-Cluster does not utilize any RAM or ROM from the 2040 or host CBM/PET units.
- Multi-Cluster is compatible with all known softwear that utilize the IEEE port.
- Multi-Cluster can be fully implemented on 8 PETS, completely ready to use, in less than 15 minutes.
- Simply plug the Multi-Cluster unit into the IEEE port of the 2040 Disk Drive, then attach a Channel Module, #CM800, (3 Channel Modules are standard with unit), to the IEEE port of each PET.

THE MULTI-CLUSTER SYSTEM HAS BEEN USED AND FULLY-TESTED BY NEECO



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Text continued from page 142:
convert it. After going through all 256 table locations, I will return to the beginning of the table for the next value, continuing to go through the table for as long as I want a tone to be produced.

The fixed interval between output samples is 63 μs for my program when it is run on a KIM-1 with a 1 MHz clock. Using this time for the example, it will take 256 steps/cycle multiplied by 63 μs/step = 16.1 ms to go through the sine table once (one cycle of the waveform). As I continue to increment through the table for subsequent cycles, I am producing a continuous sine waveform with a period of 16.1 ms, or a frequency of 1/16.1 ms = 62 Hz.

If I skip every other table location — that is, add 2 instead of 1 to get the next location — then it will take me half the time to step all the way through a complete cycle ((128 steps/cycle) × (63 μs/step) = 8.1 ms/cycle) and the frequency of the tone will be doubled (1/8.1 ms/cycle = 124 Hz). You can generate higher frequencies by using a larger increment to step through the waveform table. However, there is a practical and theoretical) upper limit to the increment size: it should not be more than one third (practical) to one half (theoretical) of the length of the table itself. This means that the practical frequency upper limit is 5300 Hz ((3 steps/cycle) × (63 μs/step) = 189 μs/cycle).

So far, the important points are that I use a fixed sample rate to step through a waveform table, using a small increment size for a low frequency and a large increment size for a high frequency. The increment sizes up to now have been exact integers, restricting me to discrete frequencies (62 Hz, 124 Hz, 248 Hz, etc). How can I get all of the frequencies in between?

The control program in this case was made very simple.

I will use a 2-byte increment and a 2-byte pointer. These have both an integer part and a fractional part. As I step through the table I will add both the integer part and the fractional part to the 2-byte table pointer, but will ignore the fractional part when I use the pointer as an offset from the beginning of the waveform table. Thus I will maintain a table pointer with both integer and fractional parts, but I will index into the table with just the integer part. For example, with 2.5 as the increment size used to choose successive samples within the 256-entry table, the program will take (on the average) not 256 but 256/2.5 = 102.4 steps to create one cycle of the sine wave. With each step taking 63 μs, the waveform has a period of 6.45 ms, which is equivalent to a frequency of 155 Hz.

Combining two tones could be done by using two digital-to-analog converters and combining the audio frequency tones with a resistive network. However, I can let the computer add the instantaneous waveform values before sending the results out to the digital-to-analog converter. The resulting waveform is the same.

My program keeps track of two increment sizes and two table pointers. When the processor has both values for a single sample instant, it performs an ADC (ie: add) instruction and sends the result to the digital-to-

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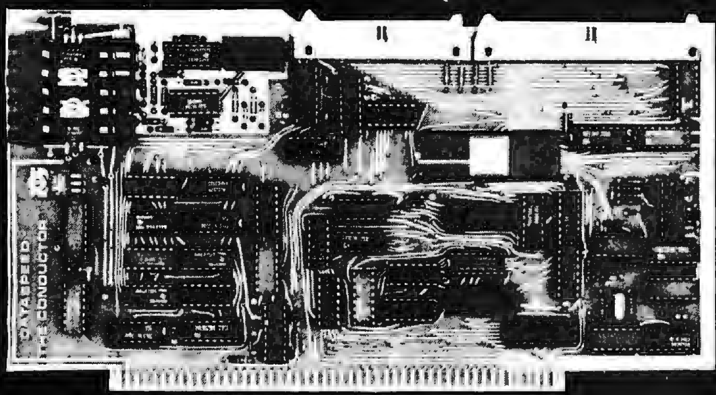

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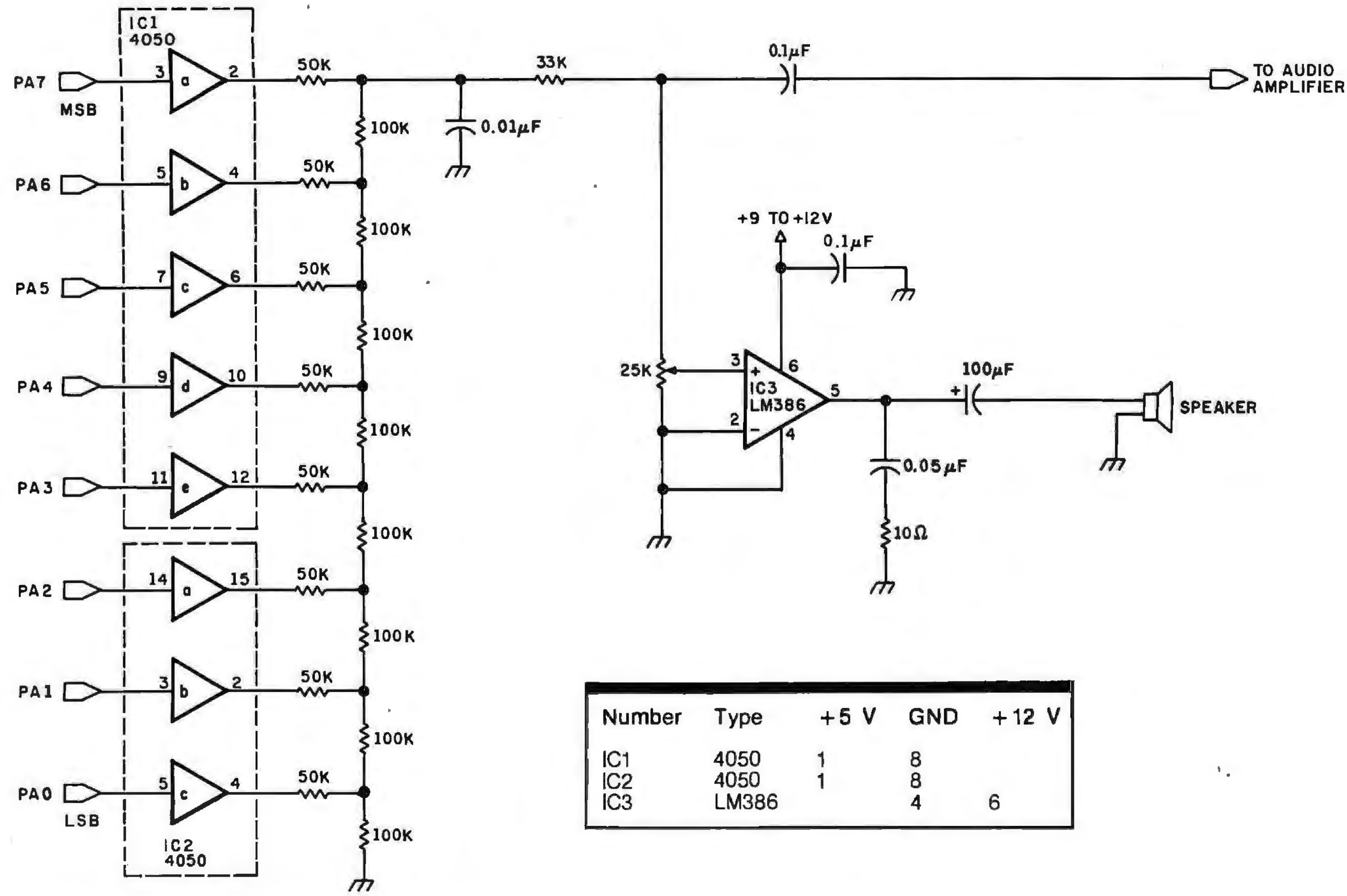

Number	Type	+5 V	GND	+12 V
IC1	4050	1	8	
IC2	4050	1	8	
IC3	LM386		4	6

Figure 2: *Schematic diagram of circuit for audio dialing. The tones used for dual-tone, multiple-frequency (ie: Touch-Tone) dialing are generated by the conversion of an 8-bit digital quantity to an analog signal. Here, a resistive ladder converts the 8-bit value to an analog voltage, and a resistor-capacitor pair acts as a low-pass filter with a cutoff frequency of about 3 kHz. The signal can either be sent to an external amplifier, or it can be amplified by the circuit centering around IC3.*

analog converter. The maximum value of the sum must never exceed the 8-bit range of a single byte, so the waveform values themselves must all be less than one half of hexadecimal FF. (This gives the previously stated value of hexadecimal 7F.)

The waveform produced is a staircase approximation to the superposition of two frequencies. The sharp transitions in the voltage levels produced by this method are full of high-frequency harmonics. Filtering will be required to get rid of these unwanted frequencies.

Hardware Required — Tones

Hardware required to generate tone pairs consists of a simple 8-bit digital-to-analog converter, a low-pass filter, an amplifier, and a small speaker. (See figure 2 for a schematic diagram of the circuit I used.)

The 8-bit latched output from the computer is applied to a ladder-network digital-to-analog converter using complementary metal-oxide semiconductor (CMOS) buffers. This is unsigned binary conversion: a code of hexadecimal FF produces close to 5 V output and a code of hexadecimal 00 produces close to 0 V output.

A similar ladder network could be constructed using transistor-transistor logic (TTL) integrated circuits, but CMOS buffers give more accurate results (even though the quality of conversion is not too important in this application). For each of the 50 k-ohm resistors shown, I used two 100 k-ohm resistors in parallel.

The output of the digital-to-analog converter goes through a single-pole, low-pass filter with a cutoff frequency of about 3 kHz. The output of the filter can be fed to an amplifier and speaker system. Use a capacitor in series (as shown in figure 2) to block the DC voltage offset from the converter. Make your connection at the wiper of the potentiometer if your amplifier lacks a volume control of its own. The volume-control potentiometer I used a 25 k-ohm linear trimmer, but almost anything from 20 k thru 100 k should work fine.

I found it convenient to use an integrated-circuit audio amplifier to drive my speaker (one side of a pair of headphones). The manufacturer of the LM386 suggested the simple circuit I used. The input is direct coupled (ie: the DC offset voltage potential from the converter will be maintained through the amplifier stage). The output capacitor blocks direct current to the speaker; it must be of a value of at least 100 µF to produce a sound loud enough to work with my system.

Another factor in loudness is the supply voltage for the LM386. A 5 V supply will produce tones that are clearly audible but which are not loud enough to work the telephone circuits when I use the headphone speaker. The headphones work fine using a 9 V or a 12 V supply. If a speaker lower in impedance than mine is used, the 5 V power supply may be sufficient.

My circuits were constructed on an

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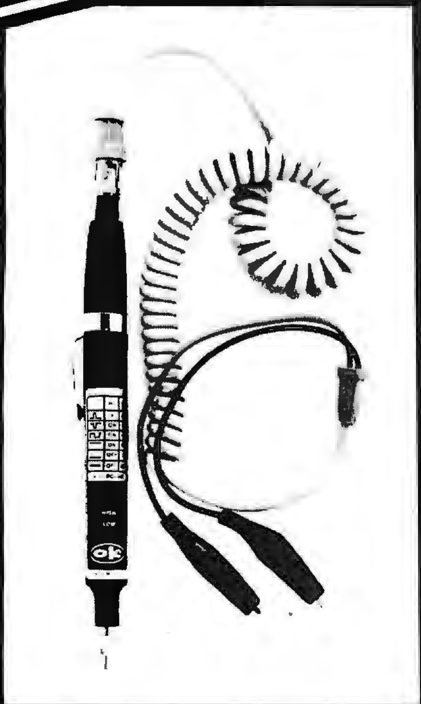

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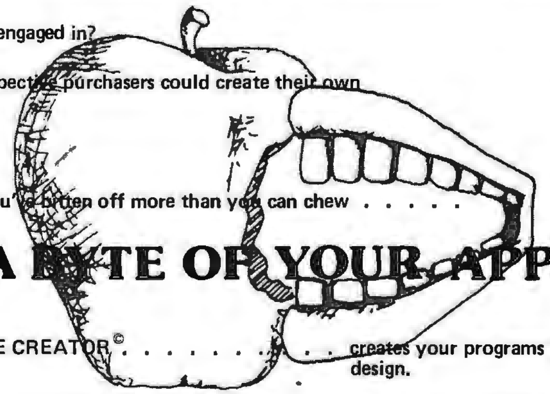

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integrated-circuit breadboard without much attention paid to component layout and wire lengths. The 0.05 μF capacitor and 10-ohm resistor on the amplifier output were recommended by the manufacturer for stability, but they were not required in my system.

When you run the program to generate tones, adjust the volume control to give an output as loud as possible without clipping distortion. If you have an efficient speaker, perhaps you can set the volume control lower than would otherwise be necessary. Try dialing some local numbers to test correct operation. I have found that (in my local telephone system) dialing my own number will give a busy signal if everything is working properly. If a dial tone remains after the system has produced the tones, or if there is silence, I know the system needs adjustment.

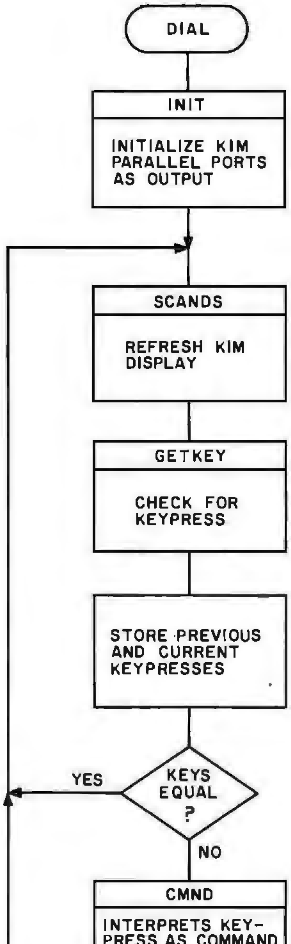

Figure 3: *Flowchart for DIAL, the main loop of the program used to store and dial a telephone number. SCANDS and GETKEY are KIM monitor routines to display data on the KIM readout and to check for a keypress, respectively. CMND executes the most recent keypress if it is a valid command, and DIGIT stores and displays the digit key just pressed during the process of entering the number to be dialed.*

Software Required — Control

There must be an overall controlling mechanism to accept user commands and digits and to execute the proper routines. The control program in this case was made very simple, relying on calls to subroutines to execute desired operations. The KIM monitor routines are used to collect input data from the keypad and to put information into the display. Other routines are called to set up I/O registers, to enter a digit from the keypad into memory as part of the telephone number, and to interpret and execute a command key when pressed.

The remainder of this article is a discussion of the individual routines used in the dialer program. Refer to the flowcharts in figures 3 and 4 for a general idea of the program's logic. I shall first describe the overall software structure and then each of the subroutines in more detail.

Listing 1 shows the main routine of the program. I kept it very short and relied on subroutines to do the work so that I could concentrate on getting the basic program flow to work before I tried out the more complicated and error-prone subroutines.

When I was testing the main routine, I changed the subroutine addresses to call KIM location hexadecimal 194B, which contains hexadecimal 60, a return instruction. Each such subroutine call is a dummy providing an immediate return. When the main routine worked to my satisfaction, I began writing the subroutines and one by one replaced the dummy calls with calls to a new routine to be tested.

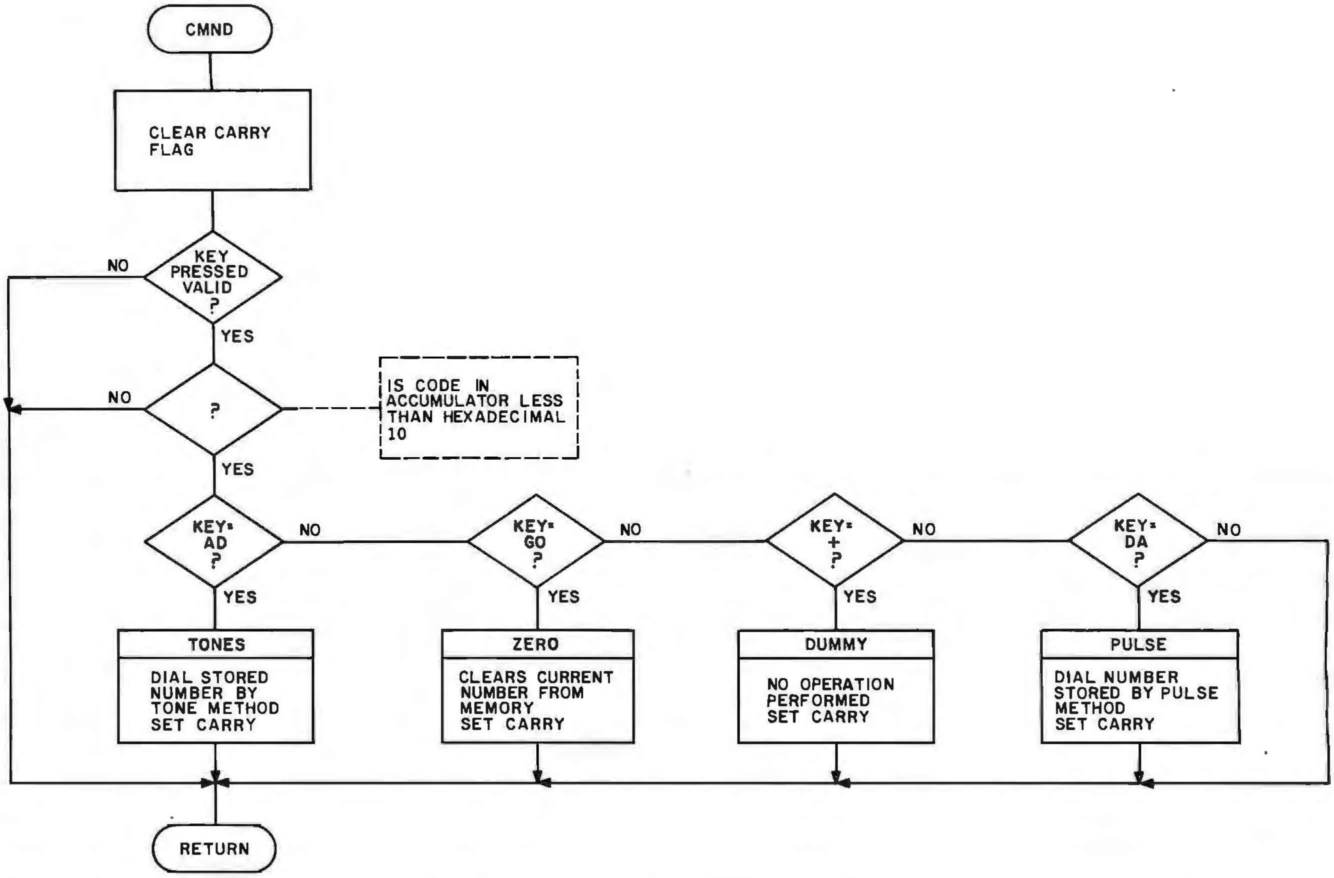

Figure 4: *Flowchart for CMND, a command decoding subroutine. TONES and PULSE cause the telephone number currently in memory to be dialed by the audio-tone and pulse-dialing methods, respectively. ZERO clears the current number from memory, and DUMMY is a trivial subroutine used to test the calling routines. The CMND subroutine returns with the status of the carry flag denoting whether or not the last keypress is a valid command (set) or a digit (cleared).*

The logic of the main program is not too complicated. First, a call to an initialization routine is made to set up data-direction registers of the I/O devices and to load variables with starting values. I then use two KIM routines to put data in the display (SCANDS) and to check for a key closure on the KIM keypad (GETKEY).

Key Pressed	Code Returned
none	15
0	00
1	01
2	02
3	03
4	04
5	05
6	06
7	07
8	08
9	09
A	0A
B	0B
C	0C
D	0D
E	0E
F	0F
AD	10
DA	11
+	12
GO	13
PC	14

Table 3: *Codes returned by the KIM monitor subroutine GETKEY. These values must be known in order to decode a keypress in the CMND subroutine.*

If no key is pressed, the GETKEY routine returns with a value of hexadecimal 15 in the accumulator. If one of the keys (except for reset and stop) is pressed, a hexadecimal code from 00 to 14 will be stored in the accumulator. (See table 3 for the key names and the codes returned by GETKEY.) The main routine waits for a hexadecimal 15 from GETKEY between separate closures on the keypad. In this way, the program can distinguish between an old key still held down and a second closure of the same key.

Further processing of a key will determine whether the key is a command (GO, AD, DA, PC, +) or a digit (0 thru 9 and A thru C). If the key is a command, then the action called for will be carried out by invoking the appropriate subroutine.

The keycode is passed to the CMND subroutine in the accumulator. If that routine returns with the carry flag set, then a command was carried out and no further processing need be done. If the carry flag is cleared (=0) when the subroutine returns, then it was not a valid command keycode and processing will be done in the DIGIT subroutine.

The DIGIT routine also checks for valid digit codes and returns immediately if the code is out of range. If the code is a digit, then the DIGIT subroutine will take that code and store it into memory as the next digit of the telephone number. The display will also show the new digit, as I will show later. When digit processing is over, the program makes an unconditional relative jump to service the keyboard and the display.

Subroutine INIT loads the I/O control registers with data-direction information, making all bits of application port A and B into outputs (although only lines PA0 thru PA7 and PB0 are used in this application).

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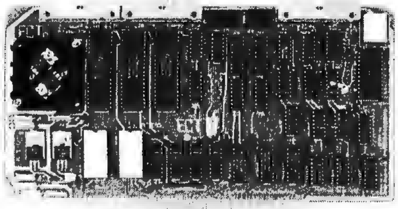

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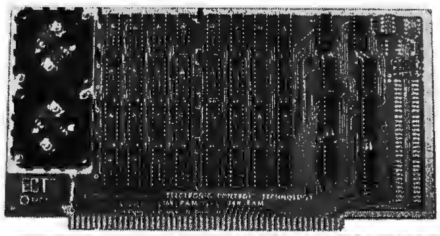

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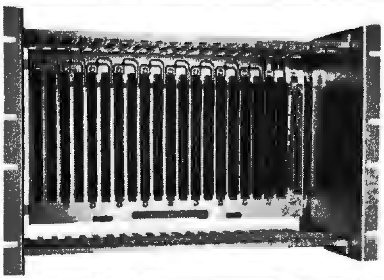

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04	03	PAGE1	SINTAB is page 03.
05 06	XX XX	INC2F, INC2I	As above for note 2.
07 08	XX XX	PNT2F, PNT2I	
09	03	PAGE2	SINTAB is page 03.
0A	XX	TEMP0	Temporary storage
0B	XX	TEMP1	Temporary storage
0C	0B	NDIGIT	Maximum number of digits in telephone number

Table 4: *Definitions and locations for variables and constants within the DIAL program. There are pointers (PNTxx) and increment values (INCxx) to two frequencies (xxx1x and xxx2x), each of which has a fractional (xxxxF) and an integer (xxxxI) byte. PAGE2 points to the page boundary that contains the beginning of the sine wave table SINTAB. The increment values are valid only if the KIM-1 board is running at 1 MHz.*

The entry point labeled ZERO can be called as a subroutine by other parts of the program. It clears out the digits stored in memory by replacing them all with hexadecimal 0F. Then subroutine SHIFT2 (part of subroutine DIGIT) is called to update the display variables (INH, POINTL, POINTH) to show all Fs.

The CMND subroutine examines the keycode and passes control to the correct subroutine to carry out the action required. The CMND routine initially clears the carry flag. If the keycode in the accumulator from the DIAL routine does not match with a valid command code, then the routine will return with the carry flag still cleared.

Otherwise, the keycode is compared with each valid command code. If a match is found, the command is carried out by calling a subroutine. When that subroutine returns, the carry flag is set to 1, and control is returned to the main program, which must examine the carry flag to see if a command was executed. If this is the case, then no further processing of the keycode is required.

The DIGIT subroutine also examines the keycode and appends it to the telephone number if it is a valid digit key. The routine first checks to see if the keycode is within the proper range to be a valid digit (hexadecimal 00 thru 0C). If so, then the new digit is shifted into the string of previously entered digits. This is facilitated by storing the keycode in the next byte beyond the string of old digits.

The KIM display contents, which are held in locations 00F9 (INH, the two rightmost digits of KIM's display), 00FA (POINTL, the next two digits), and 00FB (POINTH, the two leftmost digits), are also changed to reflect the six most recent digits entered. At the start (or whenever the GO key is pressed), the display shows "FFFFFF", and the memory also contains all hexadecimal 0F bytes to act as a flag that no digit is to be dialed.

Be aware of telephone company restrictions concerning direct connection to the telephone circuits.

The PULSE subroutine is called by the CMND subroutine when the keycode for solenoid dialing of the stored number is processed. It steps through the stored-digit table one digit at a time, passing each digit, through the accumulator, to the CLICK subroutine that pulses the solenoid to dial the digit. As the program is currently set up, the number of digits stored is eleven. This number can be changed by modifying hexadecimal location 000C (NDIGIT) to some number other than hexadecimal 0B (11 decimal). After calling CLICK eleven (NDIGIT) times, control is passed back to the CMND routine.

The CLICK subroutine pulses the output bit that controls the button-pressing solenoid. The keycode in the accumulator is checked to see if it is a valid digit. In this case, the valid digits are those of a standard dial telephone, 0 thru 9. The basic function of this routine is to cause the solenoid to close the correct number of times for the digit which was passed to it. The user must make sure that the length of line interruptions caused by the solenoid actuation and the separation in time between interruptions is within phone company tolerances; the values given here will work for a KIM-1 running at the standard 1 MHz frequency.

One catch is that a dialed digit 0 is not zero interruptions but ten. The zero must be tested for and the value in the accumulator changed to ten if a match is found. The CLICK routine times the interruption for approximately 35 ms and waits approximately 65 ms between interruptions. Furthermore, after the last click for any digit, the routine delays an additional half second before returning. This is to simulate the pause taken between digits when a person uses a rotary-dial telephone.

Notice that each time I use the timer, I load the initial value twice. This is to avoid improper timer operation that occurs when the timer is loaded just as it times out from the countdown in progress (and it is always counting down). (See Timothy Martin's letter in *KIM-1/6502 User Notes*.)

The operation of the TONES subroutine is similar to that of PULSE. It is called by the CMND routine to count the eleven digits passed to the subroutines SETUP and SOUND, which do the dialing — in this case the sounding of tone pairs. A code for the digit to be dialed is passed to SETUP in the accumulator.

Subroutine SETUP prepares data for use by the tone-generating routine, SOUND. The subroutine checks the accumulator for a valid digit (in this case, anything between hexadecimal 00 and 0F). Only 00 thru 0B actually produce tone pairs, 0C produces a pause, and 0D thru 0F cause an immediate return.

The code in the accumulator is first multiplied by two (via a shift left

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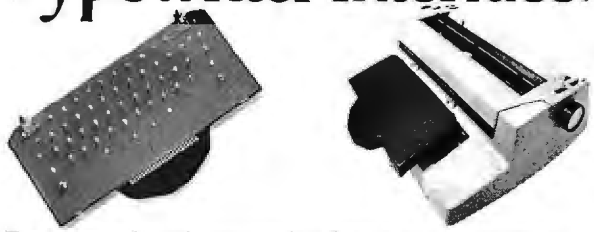

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(ASL) instruction) and used as an offset from the beginning of data table TONETAB. The reason for multiplying by two is that the table contains value pairs.

Two-tone or frequency-identifier codes are obtained from the table. These two identifiers are each used as indices into another data table, FRQTAB. From this table, we get increment values (both integer and fractional parts) that are used by SOUND to step through the waveform table.

SOUND will produce the dual tones for a fixed length of time. When control returns to SETUP, a delay of approximately 75 ms is inserted before returning to TONES. The purpose of this delay is to allow the telephone company equipment to distinguish between individual digits.

The purpose of subroutine SOUND is to produce a waveform at the output of the digital-to-analog converter that is the superposition of two sine waves of different frequency. The routine actually computes the composite waveform by adding instantaneous values for two tones.

Data for a single cycle of a pure sine wave is stored in hexadecimal locations 0300 thru 03FF, filling all of page 03 of memory. A loop in the SOUND routine is repeatedly executed for 150 ms, determined by a value loaded into the interval timer (T1024). It is very important to remember that the loop always takes 63 μs to execute once. Each time through the loop, a new value of the waveform (the instantaneous voltage out of the digital-to-analog converter) is determined by adding together values from the table for the two frequencies. The waveform values are obtained by using only the integer part of a 2-byte pointer (PNT1I, PNT1F or PNT2I, PNT2F) kept for each tone as an offset into the sine-wave table.

After one instantaneous value has been output to the digital-to-analog converter, the pointers are increased by adding both integer (INCR1I and INCR2I) and fractional (INCR1F and INCR2F) parts of an increment value. The carry out from the fractional addition must be added in with the integer part. If the sum of the integer parts for the printer goes above 255, the carry is ignored, and the table reference will wrap around to the beginning of page 03. A continuous sine wave will be produced.

Summary

Additional hardware needed to add to a microcomputer for controlling the dialing of numbers with a telephone receiver is minimal. The software shown here is complex, but it has been written in modular form to enhance its usefulness in customized applications. Be aware of telephone company restrictions concerning direct connection to the telephone circuits; do not use any method of connection that destroys the electrical integrity of the telephone system. ■

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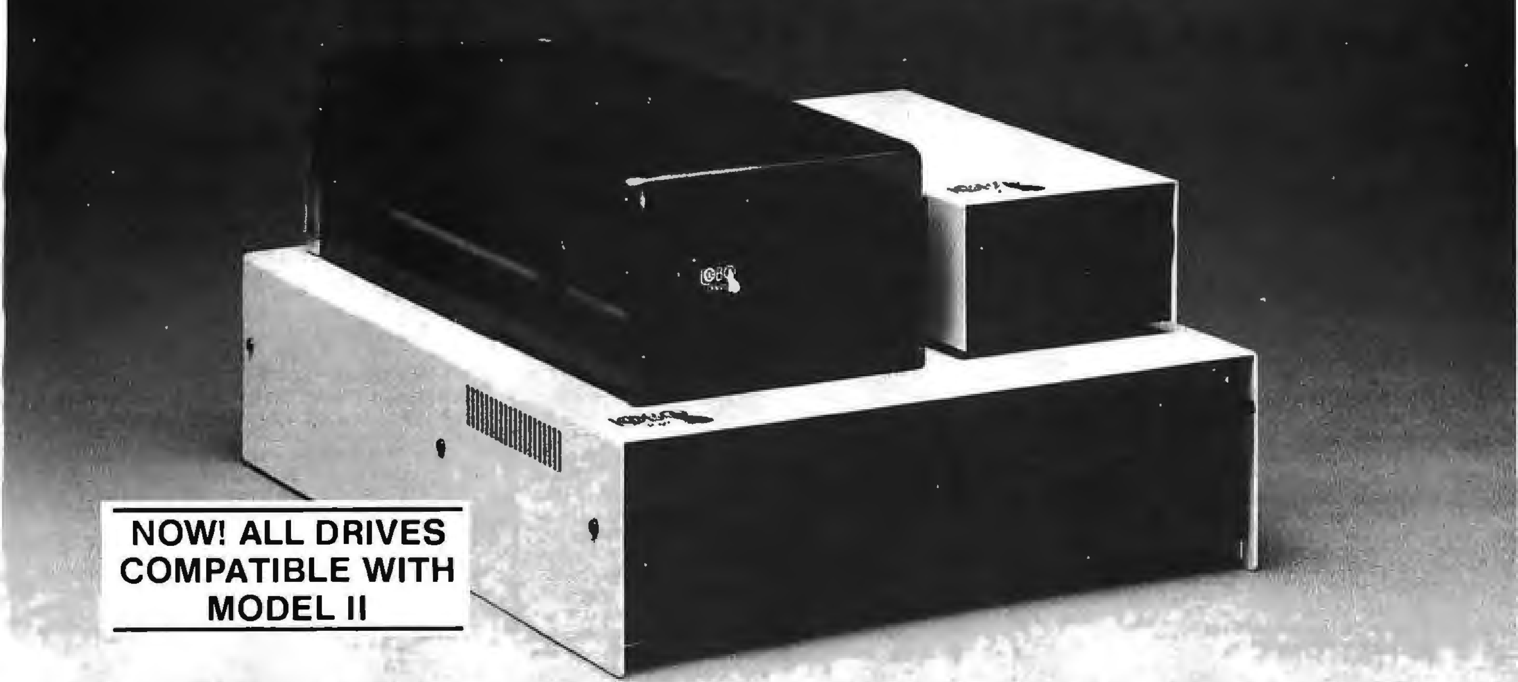

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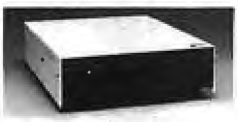

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NEWS AND SPECULATION ABOUT PERSONAL COMPUTING

Conducted by Sol Libes

New IBM Microcomputer, More On The Way? IBM is not sitting by idly in the microcomputer revolution. It has introduced a new desktop computer, the model 5120, which sells for $13,500 and features 16 K bytes of programmable memory and either BASIC or APL in read-only memory. But *Electronics* magazine, a McGraw-Hill publication, recently reported the prediction of a $4500 IBM computer. The IBM 5105 microcomputer was predicted by Creative Strategies Inc of San Jose, California, an industry analysis firm. The 5105 will be made in Japan, and it will be designed to interface with the S-100 bus. Creative Strategies predicts that the desktop machine will have, among other features, at least 16 K bytes of programmable memory, a high-speed magnetic tape cartridge for mass storage, and a small thermal printer. They also predict the introduction of the 5130, a multiterminal version of the 5105 machine.

Smalltalk For Microcomputers: Rosetta Inc, a company located in Houston, Texas, has been working for the past year on an original interactive language called "Rosetta Smalltalk." The language, inspired by but not connected with Xerox Corporation's Smalltalk language, can be expanded to include new features and has been designed to run on a Z80 system. For evaluation purposes, Rosetta Inc is privately offering a prototype version of the language to several selected owners of Z80-based systems.

IMSAI Back In Business: IMSAI is back in operation as the IMSAI Computer Division of Fischer-Freitas Corporation. IMSAI declared bankruptcy last summer. Its manufactured stock, trademarks, software, etc, were purchased by Fischer-Freitas. The company is now selling the complete line of IMSAI products and will continue to support all IMSAI hardware and software products.

Will Your Copilot Be A Computer? A research project at the University of Illinois, Urbana-Champaign, is working on an experimental computer system that will determine the correct procedures for airplane pilots to follow in unexpected situations. The system will monitor the flight plan and airframe stress; it will also adjust control settings in response to changing environmental conditions, detect malfunctions, and predict failures. Thus the computer will apply its data, analyze the problem, compute the solution, warn the pilot, and provide instructions through a synthesized voice. The pilot will be able to request assistance from the computer via voice input. The research group expects to have an operational model within three years.

Zenith To Produce Home Computer: Zenith Radio Corporation is the first television manufacturer to plunge into the home-computer market. Actually, Zenith entered this market in a limited way last year with the acquisition of Heath and the formation of Zenith Data Systems. Zenith now plans to produce an under-$1000 home computer on its color television production line. The unit will compete with the Radio Shack TRS-80 and other computers.

National Introduces New 16-Bit Microprocessors: National Semiconductor will soon be shipping samples of its 16-bit microprocessors. There is the 16008, a 16-bit microprocessor with 8-bit input/output (I/O), the 16016 microprocessor with 16-bit I/O, and the 16032 16-bit microprocessor with 24-bit memory addressing (8 megabytes). Furthermore, the 16008 and 16016 are "bilingual"(ie: they execute two instruction sets, their own and the 8080's instruction set).

IBM Testing Josephson-Junction-Based Computer: IBM's Research Division is currently testing a prototype computer that uses 4000 circuits employing Josephson-junction logic devices. These devices operate in the 35 to 40 picosecond range. This project could lead to a tiny computer (1 or 2 cubic inches) with a projected cycle time of 2.5 ns. This is eighty times faster than IBM's System 370/168.

Josephson-junction technology uses the phenomenon of superconductivity occurring at temperatures near absolute zero (0° K). In a Josephson-junction device, a magnetic field is used to turn the electron flow on or off. This technology provides a big leap forward in miniaturization and will result in reduced costs.

Video Cassette To Be Used For Winchester Backup: Pixel Corporation of Burlington, Massachusetts, plans to manufacture 500-megabyte data-storage systems that use video-cassette recorders (VCRs).

Corvus Systems Inc of San Jose, California, a maker of Winchester hard-disk drives, is presently field-testing an interface to its disk controller that enables it to be attached to a consumer VCR. Corvus claims a data-storage capacity of 100 megabytes for the system. Corvus

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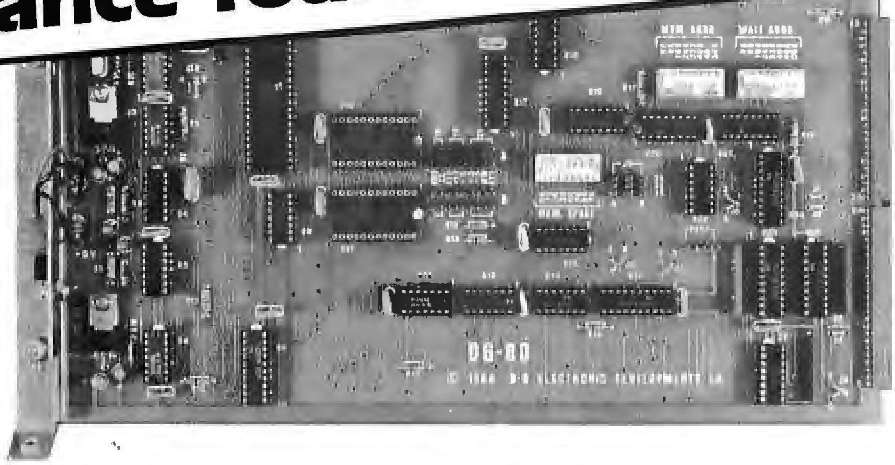

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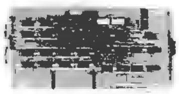

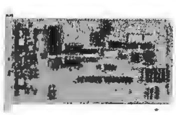

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expects to sell its interface controller for $790. Added to the cost of $1000 to $1500 for the video recorder, this gives a total cost of $1800 to $2300 for the disk backup system.

Development of video recorders proceeds apace. BASF, the German maker of floppy-disk drives and media, recently established the BASF Video Corporation in Fountain Valley, California. BASF Video will soon produce a consumer video-cassette recorder. BASF showed a 72-track recorder at a recent electronic show. The unit stores 94.6 megabytes using a longitudinal-scan method, rather than the more common helical-scan technique. The longitudinal method is preferable for random-access applications. Some Japanese manufacturers may introduce low-cost longitudinal-scan video recorders that can be used for data storage.

In comparison with competing data-storage techniques, the VCR-based systems provide a good price/performance ratio. For instance, the 3M ½-inch cartridge tape drive with controller stores 75 megabytes of data at a list price of $21,150.

8-Inch Winchester Disk Standard Being Developed: An American National Standards Institute (ANSI) committee is nearing adoption of a standard interface for the 8-inch Winchester fixed-disk drives. Such a standard would hasten acceptance of such drives by original-equipment manufacturers (OEMs), and large-scale integration (LSI) chips would be quickly developed to carry out the standard. The interface should support concurrent device operations, unidirectional data pass, nonreturn-to-zero (NRZ) data transmission, and should be able to handle variable data rates up to 10 megabytes/second over cables up to 8 meters in length. Cost will also be considered. Final adoption of the standard should be reached in mid-1980.

UCSD Pascal News: The University of California, San Diego (UCSD) has arbitrarily revoked licenses to distribute UCSD Pascal. These licenses were previously granted to and paid for by a number of computer clubs. The clubs had paid $250 for the license and they, in turn, had allowed club members to copy the software package at costs ranging from $5 to $50. A user now must pay $250 to obtain a copy of the UCSD package....A newsletter for UCSD Pascal users is being published by Jim McCord, 330 Vereda, Legenda CA 93017. Send Jim $2 to get on the mailing list. The first issue of the newsletter was 9 pages long and full of information....An international Pascal Users Group (PUG) has been formed. To join, send $6 to PUG, c/o Dick Shaw, Digital Equipment Corporation, 5775 Peachtree Dunwoody Rd, Atlanta GA 30342. Your effort will get you an occasional newsletter that is several hundred pages long....

Economic Woes Of The Personal-Computer Industry: The current rocketing interest rates on business loans are said to be cutting profits and curtailing the growth of personal-computer manufacturers, distributors, and dealers. Some smaller businesses may collapse, while throughout the field decreasing inventories are prolonging customer waiting time. In some instances, finance charges and interest rates run as high as 24 to 30 percent, when money is available. Retail stores are finding it difficult to finance small-business systems, and distribution of new products is curtailed. ComputerLand Corporation of San Leandro, California, reports that potential store owners are having trouble buying franchises.

Motorola Introduces 32-Bit Microcomputer Bus: Motorola has introduced a new microcomputer-development system with address and data buses that are 32 bits wide. The system can support 8-bit, 16-bit, and the forthcoming 32-bit microprocessors. (Most experts feel, however, that 32-bit microprocessors are still about five years away from production.) Called the "Versabus," it allows direct addressing of up to four billion words of memory. Motorola has published a specification for the bus, which can be obtained by contacting the Motorola engineering offices.

Memory News: Intel Corporation has announced a new 16 K-by-1-bit metal-oxide semiconductor (MOS) static programmable memory with a 40 ns access time. Known as the 2167, it will draw about 500 mW from a single +5 V supply and will be transistor-transistor-logic (TTL) compatible on all pins. The estimated date of availability has not been set; however, it will probably be the final quarter of 1980....Several manufacturers are in the initial production phases of 64-K bit dynamic memory devices. Included are Texas Instruments and Motorola.

256 K-Byte Programmable-Memory Devices Announced: Nippon Telephone and Telegraph and NEC-Toshiba have announced that 256 K-byte programmable-memory devices are under development by the two companies. The devices have been constructed in prototype form, and speculation is that production is still a couple of years away.

This announcement has great significance because it is one indication that leadership in the high-density, integrated circuit technology has passed from the US to Japan.

Bell Laboratories Licenses UNIX For Microcomputer Systems: Bell Laboratories, via the AT&T Western Electric Company subsidiary, has licensed Onyx Systems Inc of Cupertino, California, for implementation of UNIX on a Z8000-based microcomputer system. The system will be introduced this month.

Random Rumors And News Bits: Several toy manufacturers are working on electronic toys with voice output for the Christmas season. However, most manufacturers are reluctant to divulge any details. But you can expect the rage of Christmas 1980 to be talking toys....Radio Shack is very secretive about the sales volume of the TRS-80 computers. But one top executive recently revealed that, as of March 1, 1980, Radio Shack had manufactured 370,000 TRS-80s. That means that since 1979 Radio Shack has been producing 600 to 700 TRS-80s per day....Contrary to predictions, 8-inch Winchester disks are meeting with resistance from potential purchasers. Most OEMs are adopting a "wait and see" attitude. One problem is that backup storage for the nonremovable disks that have a capacity of greater than 10 megabytes is still lacking. Furthermore, the prices for the larger 14-inch drives are very competitive with the larger 8-inch drives. The greatest demand for hard 8-inch

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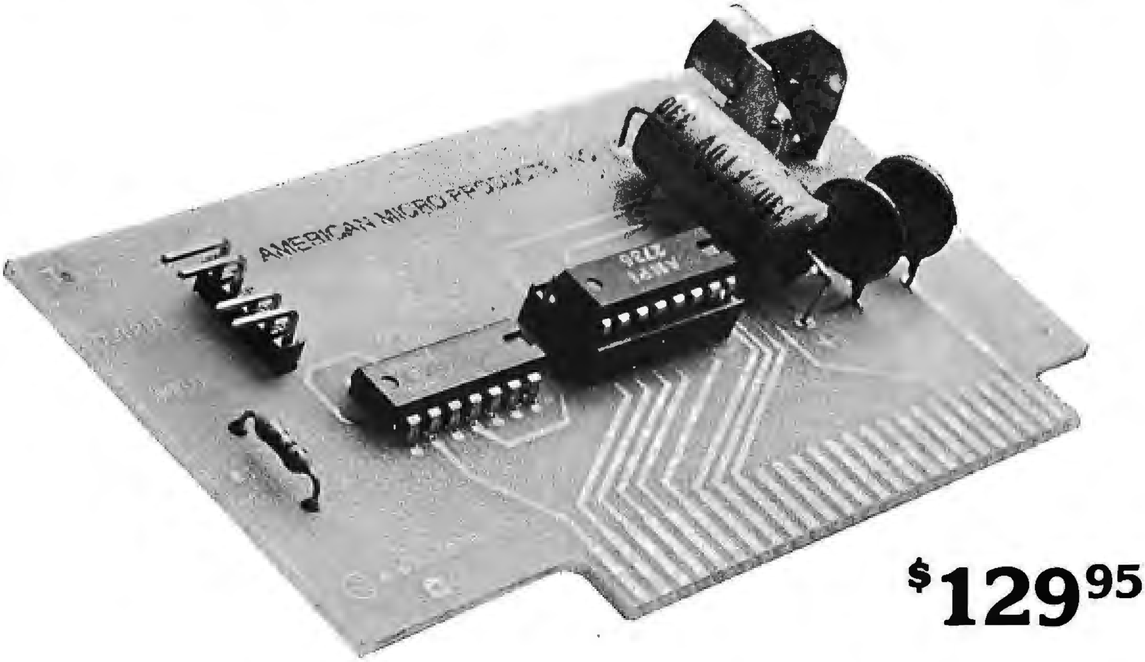

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disks is expected to be for drives with a capacity of less than 10 megabytes....Initial sales reports for the Texas Instruments (TI) 99/4 personal computer indicate a "ho-hum" response to the unit. Sales have not been up to expectations. TI will start shipping the unit without a color monitor (as is done with the Apple and Atari computers) and will reduce the price to $950 in an effort to improve the lagging sales....Diablo printer and service prices are due to be raised by 8.5 percent this month. Labor and material costs were cited as reasons for the increases.

Tandy Signs Floppy-Disk Supplier: Tandy Corporation (parent company of Radio Shack) has signed an agreement with Datapoint Corporation for the latter to manufacture 8-inch and 5-inch floppy-disk drives. Radio Shack currently purchases drives from Shugart, Control Data, and Tandem Magnetics.

Robot Hand Developed: The Research Institute of Industrial Safety of the Japanese Ministry of Labor has announced development of a manipulator that operates like a human hand. It has 12 degrees of freedom, three joints, and can apply 10 newtons of force. It uses the Winslow-effect clutch, which is based on an instantaneous, reversible, and substantial change in apparent viscosity when a fluid is subjected to an external electric field.

Integrated Circuit Black Market Emerges: Apparently a black market exists for integrated circuits. Intel Corporation reported in January that 10,000 unmarked integrated circuits, mostly type-2732 erasable programmable read-only memories (EPROMs) valued at one million dollars, were stolen. One black-market dealer has already been arrested for illegal possession of integrated circuits manufactured by Intel, Signetics, and National Semiconductor. All the devices were cosmetic rejects. Two former Intel employees have been arrested for stealing parts. Last summer, Intel reported a large loss of parts that turned up in Germany. In February, Wang Laboratories disclosed that $750,000 worth of Intel EPROMs had been stolen.

Zilog Increases Z8000 Instruction Set: Zilog has introduced two new versions of the Z8000, called the Z8001 and Z8002. Both operate in conjunction with Extended Processing Unit (EPU) integrated circuits to expand the Z8000's instruction set. One or more EPUs may be added to a system; the EPU uses previously undefined op codes to provide floating-point arithmetic, data-base search and maintenance operations, network interfaces, and graphics-support operations. This is a concept similar to Intel's 8087 mathematical coprocessor for the 8086. The standard Z8000 will not operate with the EPU. Six instructions have been added to the Z8001/2 to allow these versions to work with the EPU.

Machine-Independent Language Offered: Systems Consultants Inc of San Diego, California, has introduced what they describe as the first universal high-level compiler language for microcomputers. Called PLMX, the language system contains a library of compiled programs, an I/O interface, and code generator. PLMX syntax is identical to that of Intel's PL/M language. Currently versions of PLMX are available for TEKDOS (Tektronix) and CP/M operating systems. Code can be generated for 8080, 8085, Z80, 6800, TMS 9900, and CDP 1802 systems. A single license for PLMX costs $1000.

Office Of The Future To Include Personal Computers: Computer manufacturers are working hard on the "office of the future" where everyone will have a computer at his or her desk. Systems are now available for the engineer's desk, such as Hewlett-Packard's recently introduced HP-85 and Tektronix's 4050. Both computers are chiefly designed for electrical engineers and can function as a desktop computer work-station for computer-assisted design (CAD).

Several 16-Bit S-100 Microcomputers Debut: Several manufacturers have announced 16-bit processor boards for S-100 systems. I know of the following so far: Ithaca Intersystems and National Multiplex Corporation are introducing boards that use the Z8000; Ackerman Digital Systems, the 68000; Godbout Electronics, a dual-processor board using the 8085A and 8088 (which is a 16-bit 8086 with 8-bit input/output); Digicomp Research Corporation, a dual-processor system (two boards) with Z80 and Pascal Microengine.

Videotext Test To Be Conducted in Ohio: OCLC Inc, which furnishes on-line catalog services to more than 2000 libraries in the US and Canada, will conduct a three-month test in Columbus, Ohio, of a home videotext system starting in October. The potential user will need a $500 terminal that attaches to a television set and holds information in an amount equivalent to ten full television screens, down-loaded from a central data base. Applications will include banking services, community information, catalog listings, and encyclopedia data. Users will be able to pay bills, transfer funds, and obtain financial data. The goal is to ultimately provide the terminal for less than $100 with a typical $10 monthly service fee.

More Random News Bits: You can now lease the TRS-80 Model II computer system from Radio Shack, through an arrangement with the A and A Financial Corporation. The leases run for thirty-six months, preceded by a ninety-day warranty period....Percom Data Corporation has secured a contract with Texas Instruments to supply floppy-disk drives.

CORRECTION: The April BYTE News column contained an item reporting that Motorola was shipping samples of an erasable programmable read-only memory (EPROM) part that is organized as "8 K by 8 bytes." The EPROMs are really organized as 8 K by 8 *bits*. [*We apologize for this error....* **RSS**]

MAIL: I receive a large number of letters each month, as a result of this column. If you wish a response, please include a stamped, self-addressed envelope.

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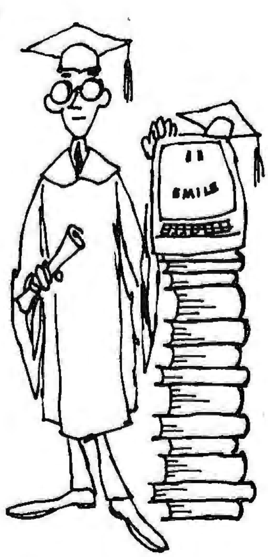

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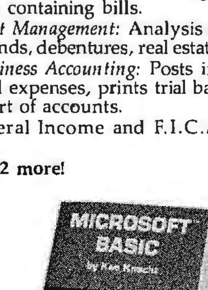

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BYTE's Bugs

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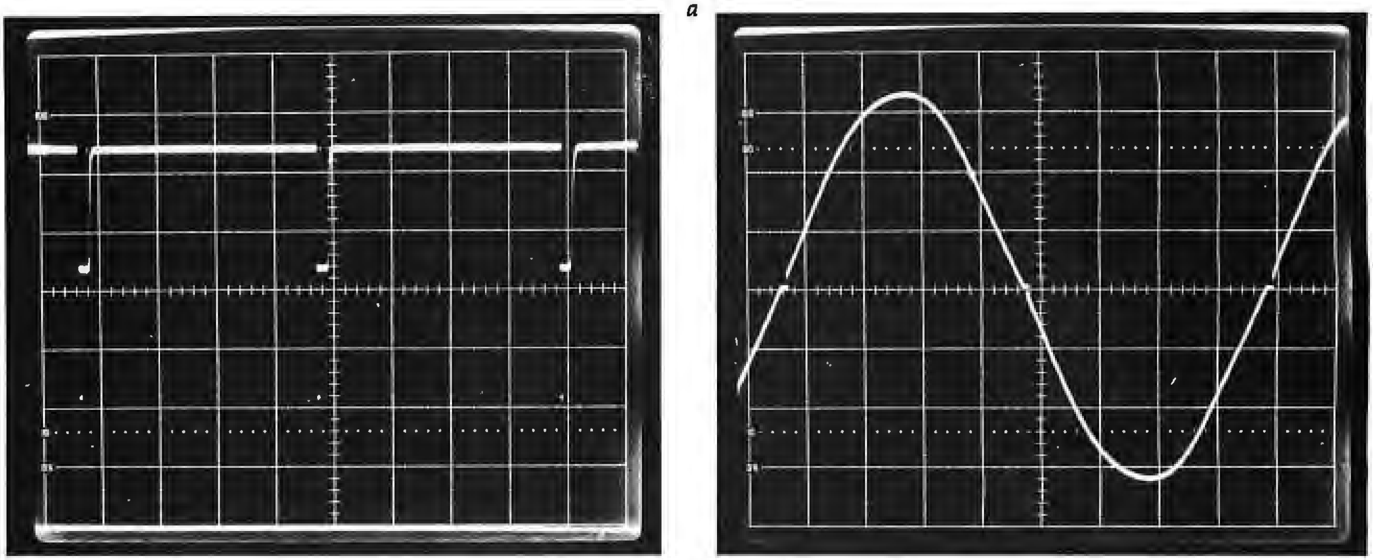

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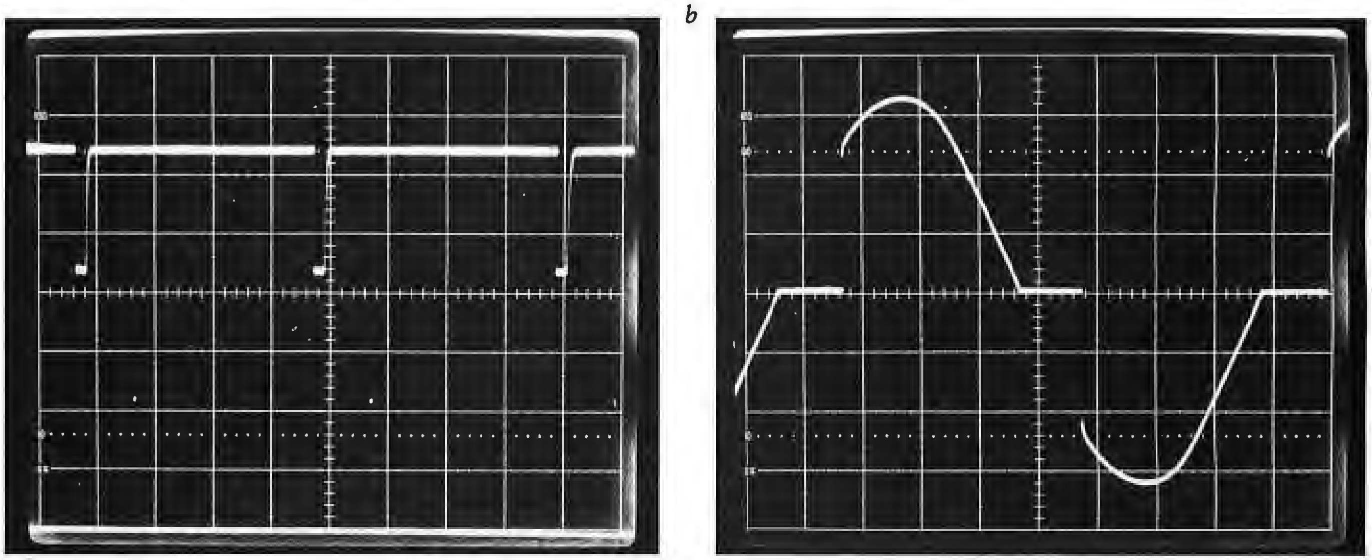

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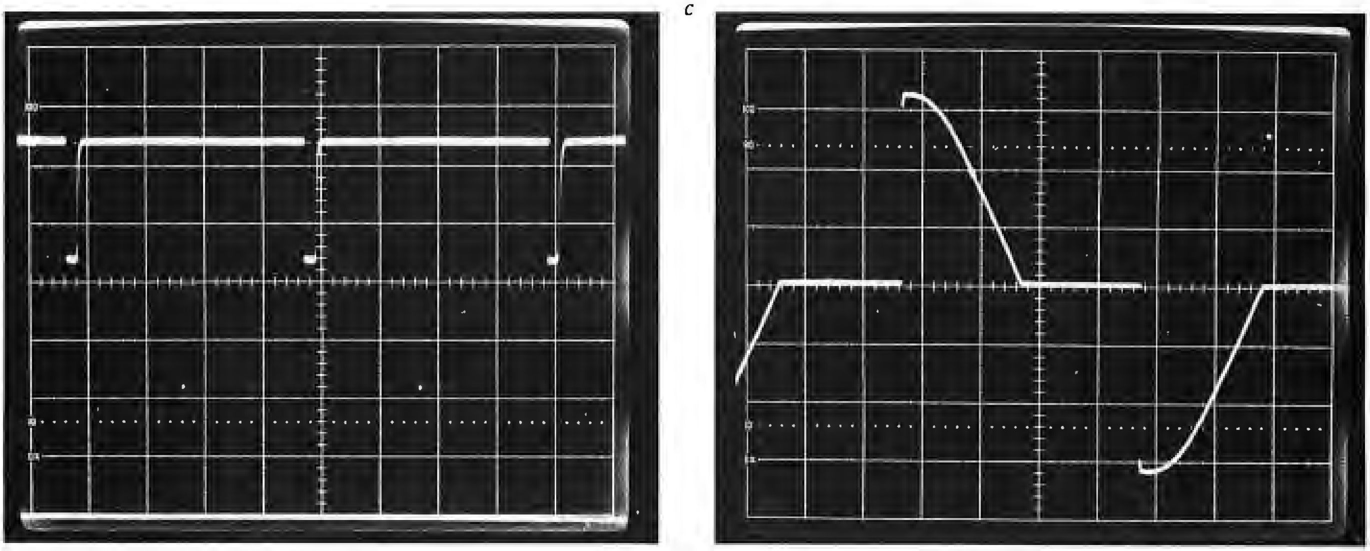

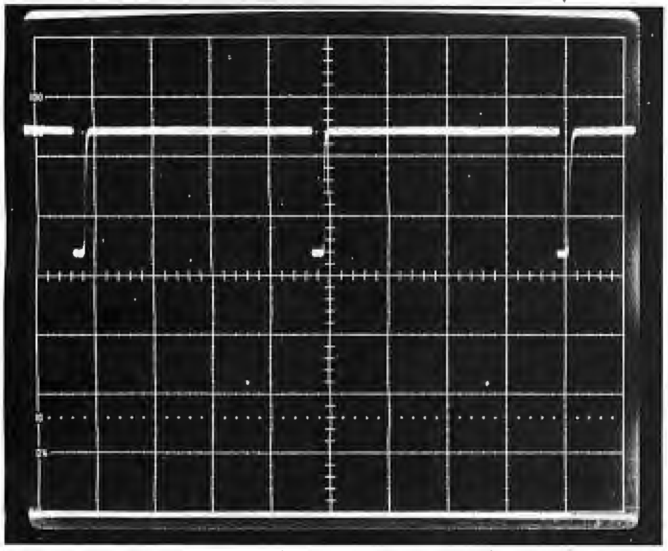

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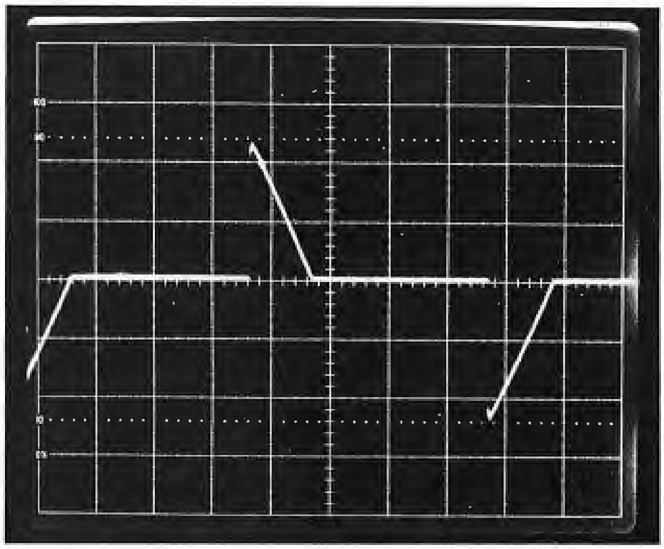

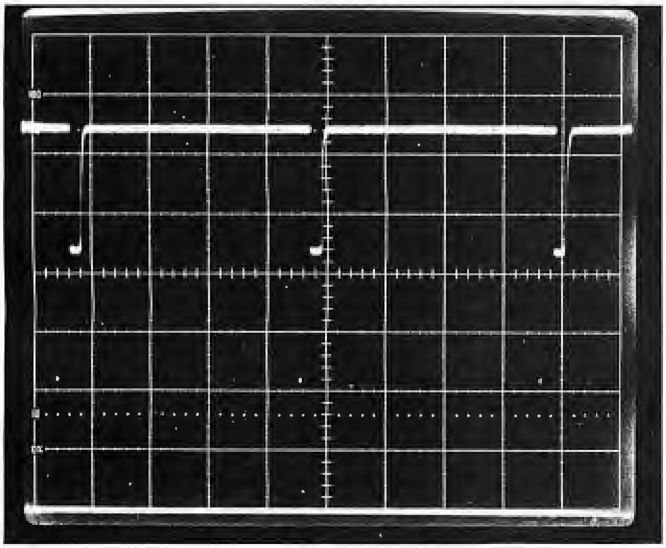

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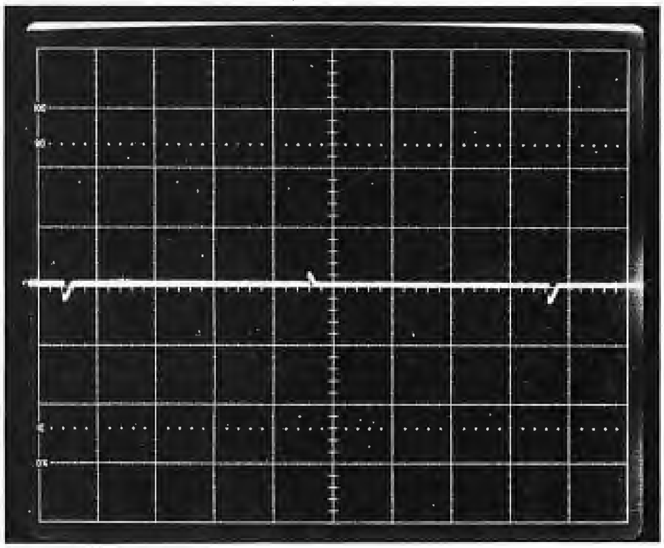

Taking a Dim View of Photographs

A series of photos in the article "A Computer-Controlled Light Dimmer, Part 1: Design," by John H Gibson (January 1980 BYTE, pages 56 thru 72) was inadvertently printed upside down. The series of pictures found in photo 2 on page 66 were inverted. The oscilloscope traces in the top row that appear to be positive pulses are in fact *negative* pulses from the timing-reference synchronizer. The positive output pulses at the bottom from the timer, mentioned in the photo caption, did not reproduce sufficiently well in print to be seen. The sections of sine curves in the bottom row of photos were also upside down, and therefore were meant to indicate opposite polarities from those implied.

To correct this error, we now present the series of photos here in the correct orientation, as they should have appeared in the January BYTE.

Bugs in the Data Cartridge

Gremlins struck the BYTE editorial department recently during the preparation of the article "Hewlett-Packard's New Personal Computer, The HP-85" (March 1980 BYTE, page 60). At the bottom of the left-hand column of page 62, the storage capacity of the data cartridge for the HP-85 should have been given as 780 program records consisting of 256 bytes each for a *total* of 192 K bytes, or 850 data records of 256 bytes each for a *total* of 210 K bytes. In addition, the procedure for printing the information on the screen is to simply press the COPY key. Our thanks to Jerry Fisher of Hewlett-Packard for pointing out these errors.

Dropping Balloons Reliably

I thoroughly enjoyed the balloon game in the article "Writing Animated Computer Games," by Tony Estep (November 1979 BYTE, page 152). I do not have a Sol computer, so I had to make a few patches to the program. I also added a drop counter, which may interest other readers.

The game as published drops balloons unreliably. To make the balloons drop consistently, change the code at hexadecimal location 01F6 to

```
CA 26 02   JZ BALN
```

The FINAL SCORE message is not centered. Change the code at location 04DE to

```
21 98 CD
   LXI H,VDMBAS+410
```

to center the message.

Many video terminals can clear the screen after receiving a form-feed character (hexadecimal 0C). If this works on your terminal, you can change the code at locations 0103 and at 0126 to

CD F0 06 CALL CLSNFF

and add the code as follows

```
06F0 0E 0C     MVI C, 0CH
06F2 CD 09 F0  CALL VIDEO
06F5 C9        RET
```

The game as published allows an unlimited number of balloons to be dropped. While this is interesting, in a way, it can lead the player to engage in real block-bombardment, dropping balloons without aiming at anything below. I have added a limit to the number of balloons available and a counter to tell how many balloons are left, to discourage waste of valuable resources. I have found that thirty-five balloons is a fair number. The code to provide this feature is shown in listing 1.

Olli Urrila
SF-44800
Pihtipudas
FINLAND■

Address	Object Code	Label	Mnemonics	Commentary
0291	C3 10 06		JMP TITLE	Jump to add more titling
0610	CD 64 05	TITLE	CALL PRINT	Send the previous message
0613	21 19 CD		LXI H,VDMBAS+119H	Load new message destination
0616	11 63 06		LXI D,MSG	Load start address
0619	CD 64 05		CALL PRINT	Send it
061C	C3 94 02		JMP IN1	JUMP back
0497	CD 20 06		CALL BALLS	Prepare to send "balloons left" message
0620	CD AB 04	BALLS	CALL SCOUT	Send the previous message
0623	21 1A CC		LXI H, VDMBAS+1AH	Load new message address
0626	11 72 06		LXI D,MSG	Load start address
0629	CD 64 05		CALL PRINT	Send it
062C	C9		RET	
062D	00 00 00		NOP; NOP; NOP	
0137	CD 30 06		CALL INIT	Initialize balloon counter
0630	E5	INIT	PUSH H	
0631	21 7D 06		LXI H, COUNTB	Counter, 'tens' address
0634	36 33		MVI M,033H	Put decimal 3 to tens counter
0636	23		INX H	Move to units counter
0637	36 35		MVI M,035H	Put decimal 5 to units counter
0639	E1		POP H	
063A	C9		RET	
01F6	CA 40 06		JZ DROP	Call counter if a drop was made
0640	21 7E 06	DROP	LXI H,COUNTL	Load units counter
0643	35		DCR M	Decrease by one
0644	3E 2F		MVI A,02FH	First 'digit' below 030H
0646	BE		CMP M	Is counter below zero?
0647	C2 26 02		JNZ BALN	If not, go back to game
064A	36 39		MVI M,039H	If yes, replace it with decimal 9
064C	2D		DCR L	Move to tens counter
064D	35		DCR M	Decrease by one
064E	3E 2F		MVI A,2FH	
0650	BE		CMP M	Is tens counter below zero?
0651	CA 57 06		JZ WASTE	If yes, go to end game
0654	C3 26 02		JMP BALN	Else go back to game
0657	21 8E CC	WASTE	LXI H,VDMBAS+8EH	Load message destination
065A	11 80 06		LXI D,MSG	Load message start address
065D	CD 64 05		CALL PRINT	Send message
0660	C3 DE 04		JMP OVER	Jump to game over
0663	2A 2A 20 33			
0667	35 20 42 41			35 BALLS (balloons)
066B	4C 4C 53 20			
066F	2A 2A 00			
0672	42 41 4C 4C			
0676	53 20 4C 45			BALLS LEFT . .
067A	46 54 20 20			
067E	20 00			
0680	2A 2A 20 59			
0684	4F 55 20 48			
0688	41 56 45 20			YOU HAVE WASTED
068C	57 41 53 54			
0690	45 44 20 41			ALL YOUR BALLS!
0694	4C 4C 20 59			
0698	4F 55 52 20			
069C	42 41 4C 4C			
06A0	53 20 21 20			
06A4	2A 2A 00			

TITLE 0610	BALLS 0620	INIT 0630
DROP 0640	WASTE 0657	COUNTB 067D
COUNTL 067E		

One small word about computers.

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The 8089 I/O Processor Handbook,
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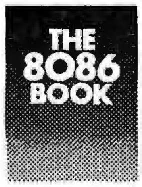
Intel is developing the co-processor concept; the 8089 is the first of the Intel co-processors. **The 8089 I/O Processor Handbook** provides a fully detailed description of this innovative device, its operation, and use in 8086 systems. This Osborne Handbook contains complete discussions of pins, signals, timing, the instruction set, and programming and configuration guidelines. Also describes the 8289 Bus Arbiter.

#39-X $5.95

The 8086 Book
by Russell Rector and George Alexy



A handbook for all 8086 microcomputer users, it includes 8086 programming instruction, a thorough analysis of the 8086 instruction set, and detailed hardware and interfacing guides which reveal the full power of the 8086 multiprocessing capabilities.

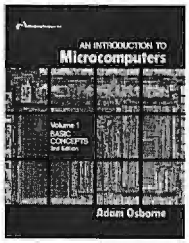
#29-2 $15.00

Z8000 Assembly Language Programming
by Lance Leventhal et al.

The first in this popular series of books to have the combined authorship of Dr. Leventhal, Dr. Adam Osborne, and Charles Collins. The Z8000 processor instruction set is described in detail, and the discussion of assembly language programming techniques makes the book an invaluable teaching tool, programming manual, and Z8000 reference book.

Available July. #36-5 $12.50

An Introduction to Microcomputers: Vol. 1, Basic Concepts, 2nd Ed.
by Adam Osborne



Since this book first appeared in 1976, more than 200,000 copies in four different languages have been sold, making it the best selling book on microprocessors ever written. Now it has been completely revised to reflect changes in this dynamic field. Basic Concepts, 2nd edition contains the most current information on microprocessor fundamentals to be found in any publication.

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6809 Assembly Language Programming
by Lance Leventhal

Another book in the popular series of assembly language programming texts, this for the powerful 6809 processor. In a comprehensive style and format, Dr. Leventhal describes the 6809 instruction set, provides numerous sample programs, and discusses the merits of assembly language programming techniques.

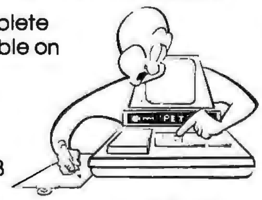
Available this fall. #35-7 $12.50

PET Personal Computer Guide
by Carroll Donahue and Janice Enger

For all users of the Commodore PET, this step-by-step guide offers advice on operating and equipment maintenance, how to cope with PET peculiarities and make the most of PET graphics. It gives instruction on PET programming techniques along with a complete PET BASIC command reference.

#30-6 $15.00

PET and the IEEE 488 Bus (GPIB)
by Eugene Fisher and C. William Jensen



The only complete reference available on interfacing the Commodore PET computer to any I/O device using the IEEE 488 interfacing port. It includes a list of the available IEEE 488 Bus-compatible instruments.

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BYTE's Bits

Bills Introduced in Congress

The Congress of the United States is beginning to take notice of personal computers. Two bills dealing with personal computers have been introduced in the House of Representatives. We believe that many of our readers will be interested in these bills, so we are printing the text of the bills here.

One bill, HR 3822, was introduced by the Honorable Thomas J Downey, Representative from New York. This bill would establish a National Center for Personal Computers in Education.

The other bill, HR 4326, was introduced by the Honorable James H Scheuer, also a Representative from New York. HR 4326, which is less directly concerned with personal computers, would establish a National Commission on the Scientific and Technological Implications of Information Technology in Education.

Presently both bills are sitting in committees. HR 3822 was sent to the Subcommittee on Elementary, Secondary, and Vocational Education of the Committee on Education and Labor. Both the committee and subcommittee are chaired by the Honorable Carl D Perkins of Kentucky. As of mid-March 1980, hearings have not been held nor any other action taken.

HR 4326 was referred jointly to the Committee on Education and Labor and to the Committee on Science and Technology. The Committee on Education and Labor has not referred HR 4326 to a subcommittee. However, the bill has been referred by the Committee on Science and Technology to the Subcommittee on Science, Research, and Technology, which is chaired by the Honorable George E Brown Jr from California. A hearing on HR 4326 was held for one day, on October 9, 1979. No further action has been taken.

H.R. 3822

96th CONGRESS
1st Session

To amend title III of the Elementary and Secondary Education Act of 1965 to establish a National Center for Personal Computers in Education.

IN THE HOUSE OF REPRESENTATIVES
MAY 1, 1979

Mr. Downey introduced the following bill; which was referred to the Committee on Education and Labor

A BILL

To amend title III of the Elementary and Secondary Education Act of 1965 to establish a National Center for Personal Computers in Education.

Be it enacted by the Senate and House of Representatives of the United States of America in Congress assembled, That title III of the Elementary and Secondary Education Act of 1965 (20 U.S.C. 2941 et seq.) is amended by adding at the end thereof the following new part:

"Part N—Computers in Education

"Program Authorized

"Sec. 393. (a) The Commissioner shall award grants to one applicant for the establishment and operation of a National Center for Personal Computers in Education (hereinafter in this part referred to as the 'Center') to instruct students in the use of personal computers and to develop programs designed to utilize personal computers and microcomputers as educational tools at all educational levels. The Center shall be operated during the fiscal years ending September 30, 1980, September 30, 1981, and September 30, 1982.

"(b) The responsibilities of the Center shall be to—

"(1) identify sources of courseware materials and provide information about such materials to interested parties;

"(2) develop courseware materials for use in areas in which available courseware materials are inadequate;

"(3) identify and develop curriculum materials for instructing students at all educational levels in the uses of computers;

"(4) provide special teacher training and demonstration computer systems to schools at all educational levels that have a large proportion of minority students;

"(5) develop methods for enabling handicapped individuals to use computers for communication and educational purposes;

"(6) conduct programs demonstrating the various educational uses of computers which shall include, but not be limited to—

"(A) the provision of computers in the classroom for student use which may include as many as one computer per four students,

"(B) the establishment of a laboratory that uses computers to simulate live experiments, and

"(C) the establishment of a computer library that would allow students to borrow personal computers for use outside the classroom;

"(7) assess the relative quality and merits of commercially available microcomputers and disseminate such assessments to educators;

"(8) monitor new developments in educational technology, including microcomputers and video disk systems, and disseminate information about such developments to educators;

"(9) develop teacher training materials, including computer programs, films, slides, pamphlets, and audio and video cassettes, that will—

"(A) instruct educators about personal computers and their uses to enable them to determine the amount of financial resources and personnel to commit to the use of computers in their educational system,

"(B) instruct educators in the methods of using computers to enhance the learning experiences of their students in the classroom, in laboratories, and at home, and

"(C) instruct teachers in computer programming and in the development of courseware materials;

"(10) establish a demonstration laboratory to exhibit examples of personal computer systems and courseware materials to enable educators to personally observe the operation of such computers and courseware materials;

"(11) publish a periodic newsletter to disseminate information on computers, computer training programs, and courseware materials;

"(12) assist Congress and interested Federal agencies in developing a program for establishing Regional Centers for Personal Computers in Education, that shall include, but not be limited to, appropriate goals and designs for such centers;

"(13) solicit from subscribers to the newsletter established under paragraph (11) of this section information concerning their computer education needs;

"(14) assist Congress and Federal agencies in identifying areas in which Federal funding will accelerate the educational impact of emerging computer technologies;

"(15) undertake any studies requested by Congress or Federal agencies relating to educational uses of computer technology;

"(16) establish a mechanism to inform the computer industry of the computer needs of the Nation's educational system and to receive from the computer industry information concerning recent developments in computers;

"(17) monitor developments in the area of intercommunication among users of personal computers and devise means of utilizing intercommunication to inform educators of the potential uses of personal computers;

"(18) assist interested local libraries in establishing programs to provide personal computers and video disk systems to the public; and

"(19) establish a model Community Personal Computer Center in one local shopping mall which shall—

"(A) provide a site for field trips by groups of local students,

"(B) provide demonstrations of the educational uses of personal computers to patrons of the mall,

"(C) conduct courses for community residents on the operation of personal computers, and

"(D) provide computer programs and books, magazines, and other information about computers on loan to the public.

"APPLICATION

"Sec. 394. The grants provided under section 393 of this title shall be awarded to one applicant from among those who have submitted an application to the Commissioner. Each application for such grants shall be submitted at such time, in such form, and containing such information as the Commissioner shall prescribe by regulation. An application shall not be approved unless it—

"(1) provides that the Center will be administered by, or under the supervision of, the applicant;

"(2) provides for the performance of the responsibilities described in section 393(b) of this title;

"(3) sets forth policies and procedures that will insure adequate evaluation of the performance of the Center;

"(4) provides for such fiscal control and fund accounting procedures as may be necessary to assure proper disbursement of and accounting for Federal funds paid to the applicant under this part; and

"(5) provides for making an annual report and such other reports in such form and containing such information as the Commissioner may reasonably require and for keeping such records and affording such access thereto as the Commissioner may find necessary to assure the correctness and verification of such reports.

"REPORT

"Sec. 395. The recipient of the grants provided under this part shall transmit a final report to the President not later than January 1, 1983. The final report shall contain a detailed statement of the activities of the Center and the recommendations of the recipient for using personal computers to improve the educational system of the United States.

"DEFINITIONS

"Sec. 396. For purposes of this part—

"(1) the term 'courseware materials' means educational materials for use with personal computers and includes, but is not limited to, computer programs and student-teacher workbooks that provide—

"(A) simulated laboratory experiences in the natural and social sciences,

"(B) discovery learning in mathematics,

"(C) drill and practice in communications, mathematics, and science,

"(D) educational games that provide learning experiences, and

"(E) materials to develop problem-solving skills in mathematics and science;

"(2) the term microcomputer' means a digital computer constructed primarily of microelectronic components;

"(3) the term 'personal computer' means a microcomputer that is portable, costs less than $2,000, and needs only an electrical outlet for use; and

"(4) the term 'computer' means a microcomputer or a personal computer.

"AUTHORIZATION OF APPROPRIATIONS

"Sec. 397. There is authorized to be appropriated to carry out the provisions of this part $750,000 for the fiscal year 1980, $1,250,000 for the fiscal year 1981, and $2,000,000 for the fiscal year 1982."

H.R.4326

96th CONGRESS
1st Session

To establish a national commission to study the scientific and technological implications of information technology in education.

IN THE HOUSE OF REPRESENTATIVES

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Circle 127 on inquiry card.

June 5, 1979

Mr. Scheuer introduced the following bill; which was referred jointly to the Committees on Education and Labor and Science and Technology

A BILL

To establish a national commission to study the scientific and technological implications of information technology in education.

Be it enacted by the Senate and House of Representatives of the United States of America in Congress assembled,

POLICY

Section 1. It is the policy of the United States that—

(1) the capability of the Nation's education system to prepare young people for the developing information-based society should be improved, with emphasis on achieving widespread development of computer skills; and

(2) computer-based techniques should be applied to the learning processes at all levels of education, whenever qualitative improvements can be demonstrated.

ESTABLISHMENT

Sec. 2. To carry out the purposes of this Act, there is established a commission to be known as the National Commission on the Scientific and Technological Implications of Information Technology in Education (hereafter in this Act referred to as the "Commission").

DUTIES OF THE COMMISSION

Sec. 3 (a) For the purpose of furthering the policy stated in section 1(1) of this Act, the Commission shall conduct studies that include, but are not limited to—

(1) a forecast of changes in information technology during the period from 1981 to 2000, with emphasis on the effect of such technology on education and lifestyles;

(2) a forecast of the need for individuals with computer skills during the period from 1981 to 2000, with emphasis on the need in the service sector of the Nation's economy for individuals skilled in information processing;

(3) a forecast of the effect of increased use of computers in education on school financing and local taxation during the period from 1981 to 2000;

(4) an investigation of incentives for increasing private sector involvement in the research and development, demonstration, dissemination, and utilization of computers for education purposes; and

(5) an investigation of the costs and benefits of alternative methods of training teachers in the use and application of information technologies and computer-based instructional materials.

(b) For the purpose of furthering the policy stated in section 1(2) of this Act, the Commission shall conduct studies that include, but are not limited to—

(1) an investigation of the status and effectiveness of existing computer-based instructional techniques;

(2) an investigation of research in the application of cognitive psychology and artificial intelligence to computer-based learning; and

(3) an investigation of institutional mechanisms for development of exemplary computer-based learning techniques.

MEMBERSHIP

Sec. 4. (a) The Commission shall consist of twelve members appointed by the President with the advice and consent of the Senate.

(b)(1) At least one member of the Commission shall be appointed from each of the following three categories:

(A) Individuals who are engaged in the professions of teaching, education administration, or education research.

(B) Individuals who are developers of computer-based instructional materials and computer equipment.

(C) Individuals who are enrolled in school or parents of such individuals.

(2) Not more than three members of the Commission shall be officers or employees of the United States.

(c) Members of the Commission shall be appointed for the duration of the Commission.

(d) The President shall designate the Chairman and the Vice Chairman of the Commission. The Vice Chairman of the Commission shall act as Chairman in the absence or disability of the Chairman or in the event of a vacancy in that office.

(e) The Commission shall not transact any business until a member has been appointed by the President and confirmed by the Senate for each of the twelve positions on the Commission.

(f) Seven members of the Commission shall constitute a quorum.

(g) Any vacancy in the Commission shall not affect the powers of the Commission and shall be filled in the

same manner in which the original appointment was made.

COMPENSATION

Sec. 5. (a)(1) Except as provided in paragraph (2) of this subsection, members of the Commission shall receive $150 for each day (including travel time) during which they are engaged in the actual performance of duties vested in the Commission.

(2) Members of the Commission who are full-time officers or employees of the United States shall receive no additional pay on account of their services on the Commission.

(b) While away from their homes or regular places of business in the performance of services for the Commission, members of the Commission shall be allowed travel expenses, including per diem in lieu of subsistence, in the same manner as individuals employed intermittently in the Government service are allowed expenses under section 5703 of title 5, United States Code.

ADMINISTRATION

Sec. 6. (a)(1) Within sixty days after the date on which the member appointed by the President for the twelfth position on the Commission is confirmed by the Senate, the Commission shall appoint an Executive Director and shall fix the rate of compensation for such position at a rate not to exceed the maximum rate of basic pay currently payable for GS-18 of the General Schedule under section 5332 of title 5, United States Code.

(2) With the approval of the Commission, the Executive Director may appoint such additional personnel as the Executive Director deems advisable and shall fix the rate of compensation for such personnel at a rate not to exceed the maximum rate of basic pay currently payable for GS-18 of the General Schedule under section 5332 of title 5, United States Code.

(3) Except as provided in paragraphs (1) and (2) of this subsection, the Executive Director and the personnel appointed under paragraph (2) of this subsection may be appointed without regard to the provisions of title 5, United States Code, governing appointments in the competitive service, and may be paid without regard to the provisions of chapter 51 and subchapter III of chapter 53 of such title relating to classification and General Schedule pay rates.

(b) With the approval of the Commission, the Executive Director may procure temporary and intermittent services to the same extent authorized by section 3109(b) of title 5, United States Code, but at rates not to exceed $150 per individual per day.

(c) The Commission is authorized to negotiate and enter into contracts with private organizations and educational institutions to carry out such studies and reports as the Commission deems necessary to carry out its duties under this Act.

(d) Under section 1862 of title 42, United States Code, the National Science Foundation was given a special mandate to foster computer technology for research and education. Therefore, the National Science Foundation is hereby directed to provide administrative support and services to the Commission.

COOPERATION WITH FEDERAL AGENCIES

Sec. 7 (a) Each department, agency, and instrumentality of the Federal Government is authorized

and directed to furnish to the Commission, upon request, such data, reports, and other information not otherwise prohibited by law as the Commission deems necessary to carry out its duties under this Act.

(b) The head of each department or agency of the Federal Government is authorized to provide to the Commission such services as the Commission requests on such basis, reimbursable or otherwise, as may be agreed between the department or agency and the Chairman or Vice Chairman of the Commission. All such requests shall be made by the Chairman or Vice Chairman of the Commission.

POWERS OF THE COMMISSION

Sec. 8. (a) For the purpose of carrying out its duties under this Act, the Commission, or at its direction, any subcommittee or member thereof, may hold such hearings, sit and act at such times and places, take such testimony, and receive such evidence as the Commission, or such subcommittee or member, may deem advisable. Any member of the Commission may administer oaths or affirmations to witnesses appearing before the Commission, or before such subcommittee or member.

(b)(1) The Commission may require by subpena the attendance and testimony of any witness and the production of any evidence that relates to any matter that the Commission is empowered to investigate by this Act. Such attendance of witnesses and production of evidence may be required from any place within the United States at any designated place of hearing within the United States. Subpenas may be issued under the signature of the Chairman or the Vice Chairman and may be served by any person designated by the Chairman or Vice Chairman. The subpenas of the Commission shall be served in the manner provided for subpenas issued by a United States district court under the Federal Rules of Civil Procedure for the United States district courts.

(2) If a person who has been issued a subpena under paragraph (1) of this subsection is guilty of contumacy or refuses to obey such subpena, any United States district court within the judicial district within which the hearing is to be conducted or within the judicial district within which such person is found, resides, or transacts business may, upon application by the Attorney General of the United States, order such person to appear before the Commission, or any subcommittee or member thereof, to produce evidence or to give testimony related to the matter under inquiry. Any person who disobeys such order of the court may be punished by the court as in contempt thereof.

(3) Notwithstanding paragraphs (1) and (2) of this subsection, a person shall be excused from testifying or from producing evidence in obedience to a subpena issued under this subsection if such person states in writing to the court ordering such person to testify or to produce evidence that the required testimony or evidence may tend to incriminate such person or subject such person to a criminal penalty.

(4) Any witness subpenaed by the Commission shall be reimbursed for reasonable and necessary travel expenses, including per diem in lieu of subsistence.

REPORTS

Sec. 9. (a) The Commission shall transmit a final report to the President and to each House of Congress not later than one year after the date on which the Executive Director of the Commission is appointed. The final report shall contain the results of the studies conducted under section 3 of this Act, the Commission's recommendations for improving computer-based education, and proposals for such legislative and administrative actions as the Commission deems necessary to accomplish its recommendations.

(b) The Commission may publish such interim statements as it deems advisable, including consultants' reports, transcripts of testimony, and Commission findings.

TERMINATION

Sec. 10. The Commission shall cease to exist thirty days after submitting its final report pursuant to section 9(a) of this Act.

AUTHORIZATION OF APPROPRIATIONS

Sec. 11. There is authorized to be appropriated for fiscal years beginning after September 30, 1980, not to exceed $2,000,000 to carry out this Act.■

A Race-Car Monitoring Program

Jeff Johnson, POB 2289, Socorro NM 87801

A computer-controlled racetrack was the final project in our computer science class in Real-Time Data Acquisition and Control Theory. Three of us assembled a Tyco two-lane track with lane-changing capabilities. We set photoresistors into the track as sensors and wrote FORTRAN code that displayed the status of a race in real time on a graphics display system owned by the New Mexico Institute of Mining and Technology Computer Science Dept.

Our system included the following components: PDP-11/34 computer with 80 K words (160 K bytes) of memory; an RX01 dual single-sided floppy-disk drive (256 K bytes per drive); a VT11 vector graphics display (1024 by 1024 resolution); an LA36 DECwriter; an AR11 16-channel analog-to-digital (A/D) converter; a DZ11 8-channel RS-232 interface, which also connects our computer lab with the DEC-20 main computer; and a disk-operating system (including two text editors, a macro-assembler, and a FORTRAN compiler).

Originally, the computer was to control the lane-switching capabilities and the speed of one of the race cars. Our digital-to-analog (D/A) converter was never implemented, so we settled for merely keeping track of the cars, with the computer continually monitoring the analog-to-digital (A/D) conversion channels connecting the sensors in the track. This may not sound very useful, but the computer actually performed functions that cannot easily be performed manually: keeping track of laps completed, determining the winning car, and timing the racers.

On a lane-switching track, there is no simple mechanical way to count laps, because the cars can exchange lanes during any lap. Therefore, "serious" racing is not practical without an observer to referee the race. Our observer is the computer.

Listing 1: *Race-car-monitor program written as a structured pseudocode algorithm.*

```
BEGIN RACE CAR PROGRAM:

  WHILE NOBODY OBJECTS TO RACING CARS DO:

    BEGIN
    INITIALIZATION:

      RECOGNIZE DATA OF TRACK CONFIGURATION, TYPICAL READINGS OF A/D CHANNELS
         WHEN DIFFERENT SENSORS SHADED(IN FORTRAN, THESE ARE DATA STATEMENTS).
      CALIBRATE SENSORS:
         DETERMINE AMBIENT SENSOR VALUES AND CORRESPONDING NOISE
     INITIALIZE VELOCITIES, LOCATIONS, LAPS, TIME TO APPROPRIATE VALUES
     CREATE DISPLAY:
        DISPLAY TRACK
        DISPLAY TEXT, NUMBERS(SEE FIGURE 2), REMEMBERING LOCATION OF
                TEXT, NUMBERS TO BE CHANGED LATER
        READ IN NUMBER OF CARS, DISPLAY CORRESPONDING CARS, REMEMBERING
                THEIR LOCATIONS WHICH WILL BE CHANGED LATER.

    WAIT FOR START SIGNAL.

    START ELAPSE TIME.

    WHILE NO CAR HAS COMPLETED 25 LAPS DO:
         FOR EACH CAR DO:
             MONITOR A/D CHANNEL OF NEXT TRACK/ IF READING IS NOT WITHIN
             NOISE LIMITS, WAIT THE TIME REQUIRED FOR CAR TO GET FULLY
             OVER THE SENSOR, THEN CALL PROCEDURE DETECT, PASSING THE
             PARAMETERS CAR#, AND A/D CHANNEL.
             /* HERE WOULD NORMALLY GO THE COMPUTER ACTION PROCEDURE CALL */
         END FOR
         MONITOR EMERGENCY TERMINATE CHANNEL, IF FOUND, GO TO BEGINNING.
         UPDATE ELAPSED TIME.
    END WHILE

    DECLARE WINNER, MONITOR REMAINING CARS UNTIL THEY FINISH, ALSO MONITORING
         EMERGENCY TERMINATION CHANNEL.

END WHILE;

PROCEDURE DETECT(CAR#,CHANNEL)

BEGIN
 IF THIS PROCEDURE HAS JUST PREVIOUSLY BEEN CALLED UNDER THE SAME CONDITIONS,
  THEN RETURN /* CAR HAS NOT YET LEFT THE SENSOR AREA */
 FIND SENSOR WITH READING CORRESPONDING TO PRESENT READING ON CHANNEL.
 PLACE CAR ON CORRESPONDING POSITION OF DISPLAYED TRACK.
 DETERMINE CURRENT, AVERAGE VELOCITY, DISPLAY THESE, AND THE TRACK# AND
  LANE CORRESPONDING TO THIS SENSOR.
 IF THIS SENSOR IS ON THIS CAR'S STARTING TRACK, INCREMENT THE NUMBER
  OF LAPS FOR CAR#.
RETURN
END PROCEDURE DETECT

END PROGRAM.
```

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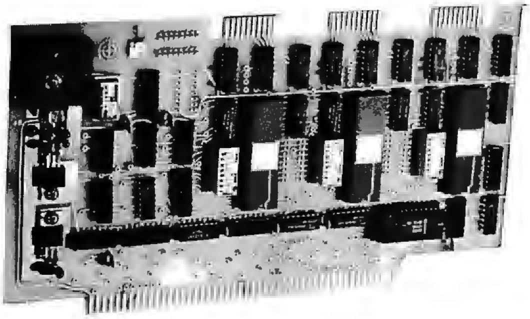

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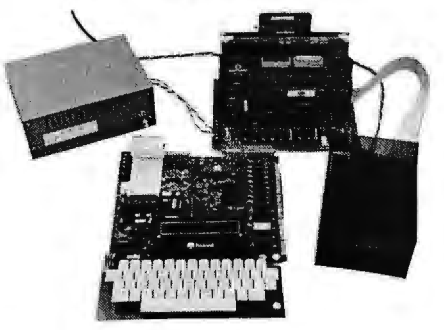

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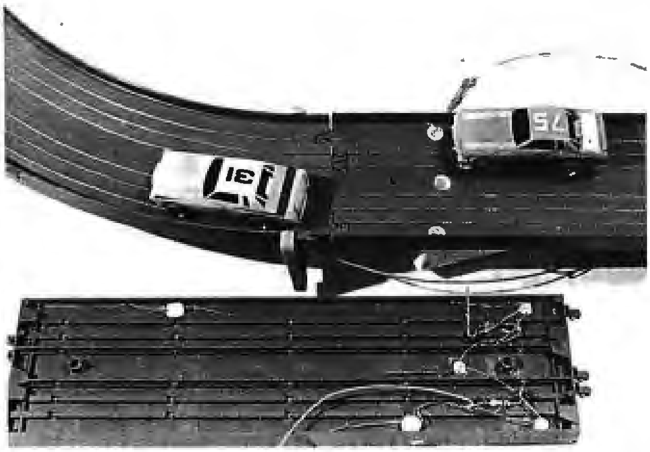

Photo 1: *A look at the racetrack showing the positioning of the light sensors.*

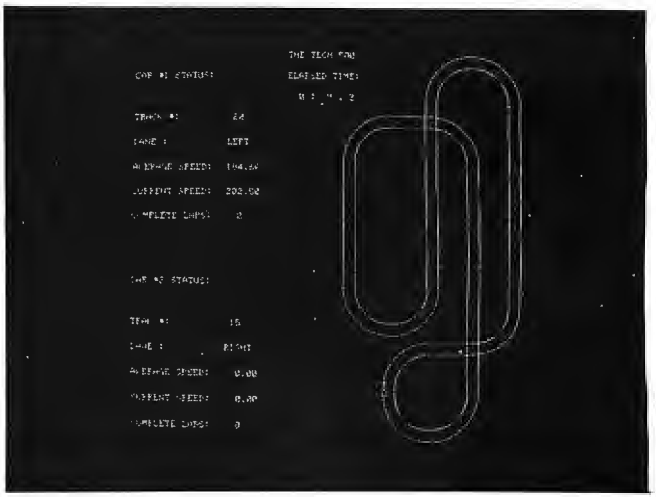

Photo 2: *Display on Digital Equipment Corporation VT11 vector graphics unit showing the layout of the racetrack and the position of the one car that is racing. The display resolution is 1024 pixels by 1024 pixels.*

After assembly of the hardware, we wrote a racetrack monitoring program. This program creates a graph of the track and causes the location of the cars on the graph and relevant data such as the current and cumulative average speed, the lane, the number of laps, the current track section for each car, and the elapsed time to appear on the graphics display (see photo 2). The algorithm for the program is given in listing 1.

The program keeps track of the first 25 laps of each car; 25 laps are one race. The computer can distinguish between the cars until one overtakes the other, whereupon a number of problems arise.

Generally, when a car attempts to pass another, there is a pile-up. We decided to make it easier. The cars start in two different locations, about half a lap apart, and finish the race after 25 laps or when one car catches up to another.

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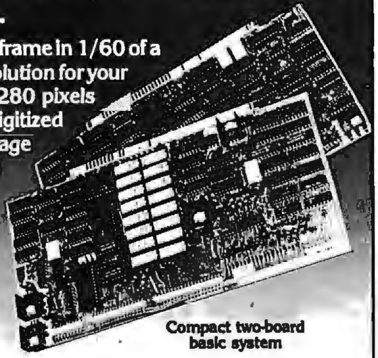

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Construction

The system was very simple to put together, taking about 20 man-hours. Three holes were drilled in the left, middle, and right lanes of each section of track (see photo 1).

Masking tape was placed on the top surface over each hole, the tracks were then turned upside down, and the photoresistors were placed in the holes. The holes were then filled with epoxy.

Since we had more sensors than analog-to-digital converter channels, we had to input several sensors into one channel. We decided to use six sensors per channel. To avoid confusion, resistors of various specific values were put in parallel with the photoresistors, evenly dividing the voltages. Since the analog-to-digital converter could read from 0 to 60, a car going over one sensor would give a value that was an integer multiple of 10, and the particular multiple uniquely determined that sensor.

After we had installed the appropriate resistors, we wired everything together. The wires were attached to a terminal-strip extension cord going to the analog-to-digital converter.

The final step was to place an incandescent lamp over the assembled track, because the only other illumination was provided by mercury lamps. Mercury lamps give sufficient 60 Hz noise to be detected by the photoresistors.

The problems encountered were as follows. Because the analog-to-digital converter channels were spread over more than one track, the motion of one car could conceivably affect the other's status. Two cars going over sensors connected to the same channel at the same time would give faulty information or none at all. There was a problem with race cars bouncing around and not keeping to their designated lane (especially around curves). This sensor restriction causes the difficulty in keeping track of passing.

Possible Improvements

Because each track had its own channel, the greatest difficulty was in determining which lane each car was in, since a car often tripped two of the sensors. This difficulty could be resolved by using two channels (and only two, better-spaced sensors) per track. The ambiguity of track identification could be resolved with one sensor per channel. However, with twenty-five track sections, we would need fifty analog-to-digital conversion channels.

Sophisticated software might resolve this problem. By treating each car through a process that monitors both ahead and behind each car for two track lengths, a correct status could be found after at least every two track sections, since there are no more than two track sections per channel.

A higher-quality model race-car set would greatly help, and I hope that in the future toy manufacturers will make available higher-quality racing sets. Toy companies might even come up with something similar to our system, using a microprocessor and light-emitting diode display. Such a system could have not only circuits along the track to bring power to the cars, but also circuits connecting sensors built into the track, so that the tangle of

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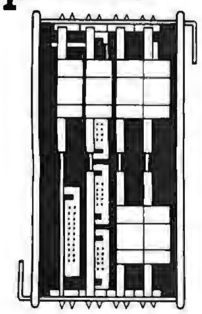

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wires that we encountered can be avoided.

The Computer Science Dept also has two LSI-11 systems that will someday be connected to the PDP-11/34 system through RS-232 lines. On these, programs could be used in a multiprocessing mode to monitor and control one particular car.

We determined that one output channel can control both the speed and the lane of the computer car. Should we be suitably inspired by the advent of a high-quality race-car set, we shall resume our original plan of racing against the computer. Our ultimate goal: having two computer programs race against each other. ■

Acknowledgements

I received advice and assistance in this project from Tom Nartker, Greg Freiberg, Russ Calvery, and Dick Carlson. A listing of the FORTRAN program to monitor the cars may be obtained by writing to me. Please include a self-addressed envelope with $0.28 US postage affixed.

Computing Time Between Dates

Paul E Condon, Staff Scientist, Lawrence Berkeley Laboratory
Bldg 90, Room 3078, University of California,
Berkeley CA 94720

There is an easier way to find the elapsed time between two dates than the one given by W B Agocs in the Programming Quickie "Day of Week and Elapsed Time Program" (September 1979 BYTE, pages 126 and 129). Zeller's congruence as given by Agocs is a specialized version of a formula for the elapsed time in days since February 28, 0000 AD:

$$N=[(13\times M-1)/5]+K+365\times Y+[Y/4]+36524\times C+[C/4]$$

M is the month number minus 2, except it is 11 or 12 of the previous year for January or February. K is the day of the month. Y is the year (modulo 100), and C is the century (ie: [(the year AD)/100]). The square brackets indicate the integer part of the enclosed expression. To find the elapsed time between two dates, evaluate N for each date and subtract.

If this leads to numerical overflow on a small system, one can replace C by (C-16). Then the formula will still work for all pairs of dates after the fifteenth century.

Also, Agocs should avoid so many GOTOs in coding the Zeller formula. Instead of lines 35 thru 115 of his listing 1, why not have:

```
35  LET M1 = M
40  LET Y1 = Y
45  LET MX = INT ((M + 9)/12)
50  LET M = M - 2 + 12 * MX
55  LET Y = Y - 1 + MX
60  LET C = INT (Y/100)
65  LET Y = Y - 100 * C
70  LET D1 = INT ((13 * M - 1)/5) + D + Y - 2 * C
80  LET D1 = D1 + INT (C/4) + INT (Y/4)
```

The variable MX is equal to 0 for January or February, and is 1 otherwise. ■

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JUNE 1980

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Laboratory Short Courses, Virginia Polytechnic Institute and State University, Blacksburg VA. Dr Peter Rony will conduct three short courses for scientists and engineers. For information, contact Dr Peter R Rony, Course Director, Virginia Polytechnic Institute, Blacksburg VA 24061, (703) 961-6370.

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June 2-4
Improving Productivity and Distributed Data Entry, Sheraton Center, New York NY. The conference and seminar schedule includes discussions on word processing, data processing, the future directions of data entry, improving data-entry productivity, automated offices, installing a data-entry incentive system, and more. Contact Data Entry Management Association, POB 3231, Stamford CT 06905.

June 2-5
The Ninth Annual Symposium on Incremental Motion-Control Systems and Devices, Ramada Inn, Champaign IL. Exhibition space is available for this conference. Contact Professor B C Kuo, POB 2772, Station A, Champaign IL 61820.

June 4-5
Microprocessors: Hardware, Software, and Application, Holiday Inn, Boston MA. This course is recommended for technical professionals who need an understanding of microprocessors in relation to their corporate and business careers. Contact Office of Continuing Education, Worcester Polytechnic Institute, Worcester MA 01609.

June 4-6
Salon de l'Ordinateur Computer Show, Place Bonaventure, Montreal, CANADA. This exhibition will feature over eighty manufacturers' hardware and software. For more information, contact Industrial Trade Shows of Canada, 36 Butterick St, Toronto, Ontario M8W 3Z8 CANADA.

June 9-13
Microcomputer Workshop, Carnegie-Mellon University, Pittsburgh PA. Engineers, research scientists, educators, and managers will benefit from this course. It covers all aspects of microcomputers and software. Hands-on training will be provided. The tuition is $585 and housing can be arranged. Contact the Post College Professional Education, Carnegie-Mellon University, Pittsburgh PA 15213.

June 10-13
Pascal Computer Programming, George Washington University, Washington DC.

Event Queue

Laboratory sessions and hands-on experience are two aspects of this course. For details of this and other courses being offered by the University, contact The Director of Continuing Engineering Education, George Washington University, Washington DC 20052, (202) 676-6106 or toll free (800) 424-9773.

June 14

Microcomputers in Business and the Professions: Systems Selection, Butler University, 4600 N Sunset Ave, Indianapolis IN. This seminar will cover various types of hardware and software, how to evaluate the kinds and performances of computers, and their applications in business and the home. The registration fee is $75. For information, contact College of Business Administration, Butler University, 4600 N Sunset Ave, Indianapolis IN 46208.

June 14-25

Introduction to Microcomputer Interfacing, Virginia Military Institute (VMI), Lexington VA. This hands-on course will feature the TRS-80 Level II system with one station for every two participants. The tuition is $450. Contact Dr Philip B Peters, Dept of Physics, VMI, Lexington VA 24450, (703) 463-6225.

June 15-18

International Summer Consumer Electronics Show, McCormick Place, McCormick Inn, and the Pick-Congress Hotel, Chicago IL. The Consumer Electronics Show (CES) will feature exhibits from many companies and seminars and discussions. Items to be displayed will range from televisions, tape recorders, telephones, and translators, to computers, component systems, auto sound systems, and electronic games. Attendance is limited to dealers and the press. Contact Consumer Electronics Show, Two Illinois Center, Suite 1607, 233 N Michigan Ave, Chicago Il 60601.

June 16-17

The BYTE Conference on Languages and Tools for Microcomputing, McGraw-Hill, 1221 Avenue of the Americas, New York NY 10020. The program covers block-structured languages and software systems, Pascal, Ada, C, LISP, FORTH, background context of traditional assembly-language tools, and more. Some of the speakers are Carl Helmers Jr, Editorial Director of BYTE magazine; Dr Ken Bowles, Dr Peter Grogono, Dr Fred Martin, Dr Henry Baker, and John Morse. For more information, contact McGraw-Hill Conference and Exposition Center, 1221 Avenue of the Americas, Rm 3677, New York NY 10020 (212) 997-4930.

June 16-19

The Thirteenth Annual Association of Small Computer Users in Education (ASCUE) Conference, University of Tennessee, Martin TN. Conference sessions will include presentations of papers and demonstrations of computers. Tutorials on structured programming, database management systems, programming in Pascal, and computer graphics will be included. Contact James Westmoreland, Computer Center, University of Tennessee at Martin, Martin TN 38238, (901) 587-7891.

June 16-20

Data Flow Concepts in Computer Language and Architecture, Massachusetts Institute of Technology (MIT), Cambridge MA. MIT's program will cover principles of data-flow computer organization and programming language design and applications. Certain architectures will be covered and techniques discussed. Familiarity with languages and architecture is a prerequisite. The tuition is $750. Living arrangements can be made through the school. Contact the Office of the Summer Session, Room E19-356, MIT, Cambridge MA 02139.

June 17-19

Data Comm, Palais des Expositions, Geneva, SWITZERLAND. Data communications and distributed-data processing are the main themes of this conference and exhibition. Software development and tools; computer languages; managing data-communications systems; and definitions, concepts, and applications of data communications and distributed-data processing are among the topics that will be covered in the conference.

For more information, contact Industrial and Scientific Conference Management Inc, 222 W Adams St, Suite 999, Chicago IL 60606.

June 16-27

Designing Microprocessor-Based Systems, Massachusetts Institute of Technology (MIT), Cambridge MA. This course is intended to give individuals with a technical background the ability to create cost-effective designs using microprocessors. Software techniques and hardware structures will be covered along with lab projects. Contact Francis F Lee, Professor of Electrical Engineering and Computer Science, Summer Session Office, MIT, Cambridge MA 02139, (617) 253-2598.

June 18-21

Association for Computational Linguistics, University of Pennsylvania, Philadelphia PA. The meeting will cover theoretical and methodological problems of computational linguistics, speech acts, analysis of multisentence texts, dialogue, machine translation, and computational semantics. For further information contact Don Walker, Artificial Intelligence Center, SRI International, 333 Ravenswood Ave, Menlo Park CA 94025.

June 20-22

The Fifth Annual Computerfest, Franklin University, Columbus OH. Sponsored by the Midwest Affiliation of Computer Clubs, this is a gathering of interested hobbyists, professionals, and business-oriented computer users. Workshops and discussions are the main features of the conference. Contact James Crowley, 4008 Rickenbacker Ave, Columbus OH 43213.

June 23-27

The First World Conference on Transborder Data Flow Policies, Rome, ITALY. Legal and social implications, economic dimensions, regulatory environment, interdependence caused by global communications, and assessing the status of data flow developments are some of the topics that will be covered in this forum. Write to the Intergovernmental Bureau for Informatics, POB 10253, 00144 Rome, ITALY.

June 30-July 3

Electronic Music Workshop, New England Conservatory, Boston MA. A combination of demonstrations and hands-on workshops are part of this course involving synthesizers, computers, and related materials. Arp, Moog, Buchla, and EML synthesizers will be available. Studio techniques will be discussed and demonstrations offered. Contact Robert L Annis, Summer School 1980—Electronic Music, New England

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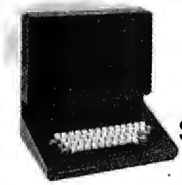

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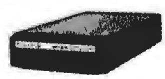

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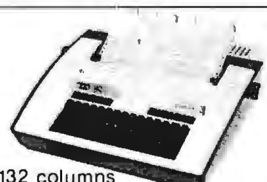

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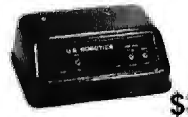

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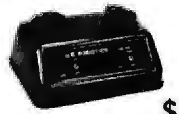

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Conservatory, 290 Huntington Ave, Boston MA, (617) 262-1120.

JULY 1980

July

TRS-80 Interfacing and Application for Scientific Instrumentation and Motorola 6801 Single Chip Microcomputer Design, Interfacing and Applications, Virginia Tech Facility, Dulles Airport. These are hands-on workshops sponsored by Virginia Polytechnic Institute and State University. For more information, contact Dr Linda Leffel, CEC, Virginia Tech, Blacksburg VA 24061, (703) 961-5241.

July 1

IEEE Indy Microcomputer Show, Sheraton Motor Inn East, Indianapolis IN. There will be exhibits, demonstrations, and technical seminars addressing all the applications of microcomputer systems. Contact Publicity Chairman, IEEE Indy Microcomputer Show, Naval Avionics Center, D/810, 6000 E 21 St, Indianapolis IN 46218, (317) 353-3047.

July 7-11

Computers and Related Products, Hyatt Regency Hotel, Seoul, SOUTH KOREA. This show is limited to approximately forty firms for exhibition. For details, contact Robert Wallace, Rm 6015A, US Dept of Commerce, Industry and Trade Commission, Washington DC 20230.

July 14-16

Diagnostic Software: Planning and Design, Sheraton-Lexington Motor Inn, Lexington MA. The seminar is for design, test, and diagnostic engineers. Design examples, lectures, informal sessions, and programming are part of the course. The fee is $450. Contact Professor Donald French, Institute for Advanced Professional Studies, One Gateway Center, Newton MA 02158.

July 14-18

SIGGRAPH '80, Seattle Center, Seattle WA. Panel discussions and readings will be included in this conference. The topics will include graphic displays, animation/dynamics, cartography, input techniques, video and color hardware, and more. For general information, write to SIGGRAPH '80, POB 88203, Seattle WA 98188.

July 22-24

Microcomputer Show, Wembley Center, London, ENGLAND. New products will be exhibited, along with presentations of papers. For information contact TMAC, 680 Beach St, Suite 428, San Francisco CA 94109.

AUGUST 1980

August 4-6

Data-Entry Management and Supervision Seminar, Chicago IL. Data-entry managers and supervisors will benefit from the techniques provided in this seminar. Topics will range from data-entry control techniques and improving data-entry operator productivity, to personnel communications and motivation. Contact MIC, 140 Barclay Center, Cherry Hill NJ 08034, (609) 428-1020.

August 12-14

Computer Graphics '80, Birmingham, ENGLAND. Computer Graphics '80 will bring together experienced users and specialists to present applications experiences and research findings. In addition to the conference, there will be an equipment exhibition and an animated film festival. To register, contact Paula Stockham, Online, Cleveland Rd, Uxbridge UB8 2DD, ENGLAND, phone Uxbridge (0895) 39262.

August 14-24

Electronics/China 80, Guangzhou (Canton), CHINA. This is the first exhibition of US electronic companies in the People's Republic of China. The United States-China Trade Consultants are the sponsors of the show. Products demonstrated will include circuit components, system elements, test instrumentation, product equipment, and materials. Details are available through Expoconsul Inc, Clapp and Poliak Inc, Princeton-Windsor Office Park, POB 277, Princeton Junction NJ 08550.

August 23-24

Personal Computer Arts Festival, Philadelphia Civic Center, Philadelphia PA. Tutorials, seminars, musical performances, and graphic extravaganzas will be featured in this show. Computer musicians and artists have until July 1 to submit material for presentation. Contact PCAF '80, c/o Philadelphia Area Computer Society, POB 1954, Philadelphia PA 19105.■

In order to gain optimum coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, 70 Main St, Peterborough NH 03458. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

Clubs and Newsletters

Southeastern Michigan Computer Organization (SEMCO)

The objective of SEMCO is to share ideas on programming, troubleshoot problems, and review new products. Meetings are held on the second Sunday of the month at the Ford Automotive Safety Center Auditorium at 7 PM in Detroit, Michigan. SEMCO's newsletter, *Data Bus*, is a monthly publication. Membership is $10 per year. Contact SEMCO, POB 02426, Detroit MI 48202.

Rochester Area Microcomputer Society (RAMS)

RAMS, which has been in existence for nearly four years, meets on the second Thursday of each month in room 1250 of the Science Building on the Rochester Institute of Technology campus. A RAMS' monthly meeting features a speaker plus reviews of products and news of interest. Their newsletter, *Memory Pages*, is published monthly. Membership in RAMS runs from October to September, and the dues are $7.50. For details, write RAMS, POB 90808, Rochester NY 14609.

Homebrew Computer Club

This pioneering personal-computer club is based in Mountain View, California. They meet monthly on the second Thursday at the Sherman Fairchild Medical Center Auditorium in Stanford, California. Their newsletter contains reviews of products, programs in different languages for all types of systems, bulletin board news, and more. To obtain information, contact Homebrew Computer Club, POB 626, Mountain View CA 94042.

Long Island Computer Association

The Long Island Computer Association is open to all computer users with interests in programming, applications, or related subjects. Dues are $10 per year; members receive a newsletter called *The Stack*. There are groups for 8080 users, TRS-80 users, and 6502 users. The meetings feature guest speakers and reports on individual members' projects. *The Stack* includes reports of the meetings, want ads, computer store listings, programs, and more. Contact the club at 3788 Windsor Dr, Bethpage NY 11714.

Delaware Valley Computer Society

The Delaware Valley Computer Society (DVCS) is dedicated to the development and improvement of its members' programming and hardware skills on the TRS-80. Meetings are held at 8 PM on the third Thursday of each month at the Bristol Township Municipal Building, near Levittown, Pennsylvania. Recent meetings have included discussions of fast graphics programming in Level II BASIC, interfacing with the real world, assembly-language programming, and beginner's BASIC programming. DVCS publishes a newsletter six times a year.

Membership dues are $12 per year. For information, contact DVCS, POB 651, Levittown PA 19058.

Apple's Contact 6 Newsletter

This newsletter is published by Apple Computer Inc, 10260 Bandley Dr, Cupertino CA 95014. It contains articles on programs, hardware, and other related items produced by the company. There is an editorial section and letters from Apple II owners and users. The newsletter also has product reviews of equipment for the Apple that is manufactured by other companies. Every issue includes valuable program listings for the Apple.

New York Amateur Computer Club

The New York Amateur Computer Club is an organization to promote the exchange of information about computers for personal use and to encourage fellowship among those interested in computing. General meetings are held once a month, normally on the second Thursday. Several specialized user groups also meet on a monthly basis. Club dues are $10 per year which includes a newsletter. For information, write to the club at POB 106, Church St Sta, New York NY 10007.

Newsletter for Texas Instruments' Programmable Calculator Users

The Texas Instruments Personal Programmable Calculator Club and its newsletter, *TI PPC Notes,* will continue coverage of all TI programmable calculators formerly covered by *52-Notes.* The new format will be mainly concerned with practical programming aids and routines. Active member participation is encouraged. Write TI PPC Club, Maurice E T Swinnen, 9213 Lanham Severn Rd, Lanham MD 20801.

Software Management Newsletter

Salt 'n' Pepper is a quarterly newsletter dealing with software management issues. An article in a recent issue entitled "Cost Effectiveness: A Challenge for OEMs" suggests that a higher degree of specialization and creativity will characterize successful original equipment manufacturers (OEMs) in the 1980s. Another article gives reasons for software products firms to consider offering a processing service. Other topics have included industry trends in software maintenance and software pricing. Subscriptions are $35 per year from Culpepper and Associates Inc, 4922 Heatherdale Ln, Atlanta GA 30360. ■

BYTE's Bits

An Othello Tournament for Humans and Computers

An Othello tournament is going to be held at Northwestern University on June 19. A one-day competition of three rounds is planned. There will be eight players: two or three humans and five or six computer programs. David Levy's program will run on a Commodore PET. Professor Peter W Frey of Northwestern University is sponsoring the event. He will be running his second-generation Othello program on either an Apple or a TRS-80 personal computer. Fidelity Electronics has been invited to enter their new Reversi Challenger. The Carnegie-Mellon program, as described in *Scientific American,* will be entered by Hans Berliner. Jonathan Cerf, the US national

Othello champion, may also compete in the event. BYTE magazine is going to co-sponsor the event. Contact Professor Peter W Frey, Cresap Neuroscience Laboratory, 2021 Sheridan Rd, Evanston IL 60201, (312) 492-7405.

Call for Papers on Computer Simulation

Papers are being solicited for the 1981 Summer Computer Simulation Conference to be held July 21 to 23, 1981, in Washington DC. The conference theme is "Simulation: Foundations and the Future." A 500-word summary or complete drafts of original papers must be submitted by November 15, 1980 to L G Culhane, The Mitre Corp, 1820 Dolley Madison Blvd, McLean VA 22102, (703) 827-6447.

The major areas of interest include simulation methodology, chemical sciences, biomedical systems, energy, system engineering, and special topics. Some other areas of special interest are government applications; simulation applications in sports, television, games, and movies; and microcomputer applications.

Call for Papers, Industrial Control

Papers are being solicited for the 1981 International Conference on the Application of Microcomputers to Industrial Control in the area of general systems to be held in Calcutta, INDIA. Hardware, software, and operational experience should be covered. A 300- to 600-word abstract is required by August 22, 1980. The full paper should not exceed twelve 8½- by 11-inch double-spaced pages. Three copies of the abstracts and papers are required. The deadline for the paper is September 26, 1980. Address material to Dr Sushil Dasgupta, Professor and Head of the Electrical Engineering Dept, Jadavpur University, 40B, Southern Ave, Calcutta-700029, INDIA.

The 1981 International Conference on Microcomputer Applications to Industrial Control will be held February 14 to 16 at Jadavpur University in Calcutta.

The First Annual National Conference on Artificial Intelligence

Recently we received a letter from Louis G Robinson, the conference coordinator of the American Association for Artificial Intelligence (AAAI). He wanted BYTE readers to know that the First Annual National Conference on Artificial Intelligence will be held at Stanford University August 19, 20, and 21st, 1980.

The AAAI is headed up by professor Allen Newell of Carnegie-Mellon University and professor Edward A Feigenbaum of Stanford University. The AAAI is intended to serve as a vehicle for communication among researchers in the US artificial intelligence community. This communication will be accomplished through two means. One means will be a magazine-format publication produced by the organization and the other will be an annual US artificial intelligence conference.

The first of these conferences is the 1980 Conference this August. The activities during the conference will include a one-day tutorial examining the current state of the art of US artificial intelligence to be held on August 18th at Stanford University. We are sure that many of our readers will be interested in attending this tutorial, to say nothing of the formal conference sessions on August 19, 20, and 21. We know that the AAAI will be an important, vital organization within the computer-science community during the years to come. ■

Interpersonalized Media: What's News?

James A Levin
The Communications Program
University of California, San Diego
La Jolla CA 92093

We are in the midst of a major change in the ways that we communicate. This change will affect many areas of our lives—the ways we are informed, educated, and entertained; the ways we interact with friends, organizations, and the world. New communication media are arising from the grass roots as personal computers become widespread and are interconnected. These media allow new possibilities for interactive, personalized communication, so I will call them interpersonalized media.

Already there are small-scale efforts to interconnect personal computers via telephone lines. There are several national personal-computer networks and many local computer "bulletin board" systems, five in the San Diego area alone. These developments will lead to such radically modified institutions as personalized news, classroomless education, and interactive soap operas. In this article, I will focus on the influence of these new media on the interchange of information that constitutes news.

About the Author

Jim Levin is a cognitive scientist interested in the implications of computer-mediated communications for the people involved. He teaches in The Communications Program and pursues research in the Laboratory of Comparative Human Cognition at the University of California, San Diego.

Personalized News

Imagine your own personal news staff, preparing a report every day on only those topics that you have expressed interest in: political news concerning Ghana, reports of advances in alternate energy sources, sports news about certain teams, want ads for Volkswagen Rabbits for sale within fifty miles for less than $3000, etc. By the time you specified a fairly detailed news profile, you would probably be receiving a unique, personalized news report.

> If the current decrease in the cost of computation and data storage continues, a system for distributing personalized news will soon be economically feasible.

Is this concept of personalized news a notion for some distant time in the future? No. The requirements for such a system are quite minimal and well within current capability. A prototype for parts of such a system exists at the Artificial Intelligence Laboratory at Stanford University, where the daily Associated Press wire contents are stored by a computer, and users are notified of stories that match their specified news profile. The details of storing, indexing, and retrieving large amounts of text have been worked out well. (However, the retrieval techniques are not foolproof. One user at Stanford, interested in dolphin research, asked to see all stories containing the word "dolphin." He was then puzzled that he was being notified of all the Monday morning football-score summaries, until he noticed the stories had the scores for the Miami Dolphins!)

The barrier to such systems has been economic—the costs of storage, computation, and communication have been too high to challenge the existing mass-distributed media of television, radio, and newspaper news. However, the cost of all three factors is rapidly dropping, and if the current decreases continue, a system for distributing personalized news will soon be economically feasible. (See the economic analysis by Panko in reference 11 for first-class business mail, for instance.) This development is especially likely when the interactive information system is integrated into a broader system for entertainment, education, and commercial interactions.

Electronic Mail

Electronic mail is an almost accidental development of interactive computer networks, but it may become the most significant use of computers in our everyday lives. It

began as interactive users of large computers needed ways to communicate with other users. Initially, mechanisms were developed to allow one person to type text that immediately appeared on the terminal of another user. However, these communication mechanisms could be used only if the other person was using the computer system at the same time.

Computer-mail systems were the next development, through which one user could type an entire message, to be seen by the other user whenever he or she next used the system. Since then, computer-mail systems have grown in power (and thus in convenience of usage) until they are now used even by people unable or unwilling to use computers for programming.

In the few organizations where they have been available for general use, electronic-mail systems have become a major communication medium. They are assuming much of the load previously carried by written memos and telephone calls, and even some of the interaction previously carried out face to face. For example, I have been using an electronic-mail system at the University of California, San Diego (UCSD) called MSG (which will be described in more detail later). Over the course of the five days before I wrote this, I received fourteen messages on this system. Two of these were directed specifically to me; two had been written to another person with a copy sent to me. Two more were directed to me as a member of a defined group of nine people, all concerned with a particular problem. This ability to send messages to a defined group of people easily allows these mail systems to be used for *teleconferencing* (described later).

The remaining eight messages were addressed to a group called "all," a group consisting of all thirty-seven users of this computer system. We can say that such messages are posted on an *electronic bulletin board.* But such use also leads to a potential problem, especially for systems involving a large number of people—the widespread distribution of electronic junk mail.

One unexpected property of text teleconferences is the tendency for multiple streams of conversation to form and flow in parallel.

Electronic Bulletin Boards

The use of electronic bulletin boards has already spread through the personal-computing community. A student of mine, Mary Loughran, discovered five electronic bulletin-board systems in operation in the San Diego area as of June 1979; two local "nodes" of nationwide bulletin-board systems, and three systems set up by individuals.

Electronic Junk Mail

The problem of electronic junk mail is a major issue for these bulletin-board systems, one that becomes critical for a widespread electronic-mail system. People get upset if they get a lot of junk mail. Fortunately, personal computers give us a direct way to deal with this problem—we can design and use electronic junk-mail "filters," programs that preprocess our electronic mail and systematically discard recognized junk mail. For example, if every message I have ever received from Bill Smith has not been worth reading, I can program my mail filter to automatically discard any messages from him.

As such junk-mail filters become widely used, general announcements (advertisements) will become more sophisticated, so that announcements are targeted only to people that are genuinely interested in them (or else are disguised as interesting messages). We can predict several rounds of action and counteraction like this within an electronic-mail system—beyond that, the system is likely to evolve into novel, currently unpredictable forms.

Teleconferences

Another mode of electronic interaction is the *teleconference*, which draws an analogy to more conventional, face-to-face meetings. Early computer teleconferencing systems had a chairman who assigned the floor to a speaker (who was then allowed to type in text that everyone else in the teleconference saw, until either he or she relinquished the floor or the chairman reclaimed it).

However, it was soon discovered that this new medium does not require a "floor" since many people can enter text simultaneously. More important, the participants do not even have to be simultaneously involved—the "tele-" aspect was then extended to mean "remote in time" as well as "remote in space." In this way, the non-real-time teleconference was born.

You may ask, "Why bother with computer-text conferences if you can just arrange a meeting or even a conference phone call?" First of all, anyone who has tried to arrange a meeting time for even a small number of busy people knows how difficult it is to find a common free time. This problem is aggravated by differing time zones; in arranging a conference telephone call that includes people from both the east coast and the west coast of the United States, you have only four hours during which both sets of people are normally available during the working day. Between London and Los Angeles there is only a one-hour window, and for much of the world there is no overlap at all.

Even when there is a considerable overlap, even a normal two-person phone call is not easy to conduct. You call the other person; she is in a meeting, so you leave a message; she returns the call an hour later only to find that you are in a meeting, and so on. I have gone as many as five rounds like this to establish communication, even when I have known I was not getting a "tele-runaround." In addition, the interruption of another phone call is amazingly disruptive—have you ever been able to finish a coherent thought when your phone rings?

But you might wonder, "Isn't a non-real-time teleconference a stilted, artificial, and ineffective way of conducting discussion or decision making?" The answer to this seems to be (1) yes, at the start, and (2) no, not after the participants acquire some experience with this new medium. A number of transcripts from different types of text teleconferences that seemed to work for the participants quite smoothly and effectively are

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recorded in the book *Network Nation: Human Communication via Computer* by Hiltz and Turoff. [*See the review by Glen Taylor on page 136 of this issue*....RSS]

Isn't spontaneity lost without real-time interaction? My experience with text teleconferences over several years has been that spontaneity is just as possible as in face-to-face meetings (and just as problematic—in how many meetings have you felt free to be spontaneous in your participation?).

One property of text teleconferences that is unexpected (and a bit disconcerting at first encounter) is the tendency for multiple streams or threads of conversation to form and flow in parallel. Multiple streams are disruptive in a face-to-face meeting, but are easily accommodated by many text-teleconferencing systems. In my experience, a new conversational thread does not appear out of the blue, but instead starts as a response to a message that branches from the main, continuing stream. Some participants follow the main stream; others follow the new branch. Many participants follow both, especially in non-real-time conferences where the urgency of real time is lacking.

Open News Networks: Being Your Own Editor and Reporter

We can now return to the general issues concerning the effect of new interpersonalized media on the ways that we exchange information. I started out with a discussion of personalized news. In effect, personalized news allows everyone to become his or her own news editor, since each person specifies which items he or she wants to see from the much larger pool of information.

Once editorial capability has become distributed, the restrictions on input and on transmission of information can be relaxed. Broadcast media structurally require strong central control of information, since the same few items are sent out to a large audience. Such restrictions are not needed for "narrowcast" media like personal letters, phone calls, personal conversation, or interpersonalized media.

Everyone can thus serve as a reporter of whatever he or she defines to be news and then act as editor, again defining the small part of a vast information pool which is considered news. The structure of information flow can change from the current "hourglass" form to that of an open network; the constriction in flow can be removed.

What Is News?

The kinds of changes discussed here may have a major impact on the ways we circulate information about the world. The general notion of what constitutes news will be challenged. Currently, "news" is information that is sufficiently interesting to a broad enough section of an audience to be judged worthy of being broadcast or otherwise disseminated by a commercial or governmental organization.

If a Little League baseball team in Peoria, Illinois, wins a local championship, that is generally not news for a San Diego, California, newspaper. However, if your nephew is playing on that team, then the result of the game *is* news to you (even if you live in San Diego). If you personalize the information you receive, then you are redefining what is news. Thus, news as information of general interest to a broad audience is replaced by news as information of specific interest to each particular individual.

There will still remain a role for news mediators in an open information network. Given a complex world and a large body of information about it, people will still depend on other people to collect, evaluate, and condense information. I will return to this issue of mediators after I consider a more general way to view these interactive information networks.

Mixed-Intelligence Information Networks

The examples we have explored of new forms of news networks are particular cases of general systems for sending and receiving information. You can picture yourself as part of a vast network, branches going in all directions, with you at one of the many places where branches converge, a *node* of the net. Each of the branches entering and leaving your node represents a way in which you receive and transmit information: by television, by newspaper, by phone call, or by word of mouth. The

possibilities discussed above are steps toward a *mixed-intelligence information network*, where some of the nodes are human (as in our current information networks) and some of the nodes are computers.

Let us look at the simplest case, in which you and your personal computer are sending and receiving electronic mail from a friend (and her personal computer). You type a message; your personal computer transmits it, placing a telephone call to your friend's personal computer (trying repeatedly if the line is busy). Your friend reads the message the next time she checks her mail, perhaps entering a reply message to be sent back to you. This network has four nodes: two human nodes and two computer nodes. By expanding the number of people involved, we can develop much more complex mixed-intelligence networks for sending and receiving information.

Dispatcher Mediators

Imagine that you want to send a message to all people who are interested in a certain topic, but you do not know who they are. You can broadcast a general message to everyone and let everyone decide whether he or she is interested, but that would be extremely expensive. Instead, you can send the message to a single person who keeps a list of people interested in the topic and ask that person to send the message on to the appropriate people. This single person can thus serve as a *dispatcher*, mediating the distribution of messages.

If a human dispatcher grows tired of forwarding the same kinds of messages to the same list of people, he can program his personal computer to automatically distribute these well-defined group messages. Thus, both human and computer dispatchers are likely to emerge in interactive information networks, with computers handling the routine cases and humans called upon to handle difficult cases.

A dispatcher lowers the cost of reaching a desired audience, raising the efficiency of the whole network. The dispatcher can then charge for the service provided according to the amount saved. Therefore, dispatchers will have incentive to develop accurate knowledge of which nodes in the net are interested in receiving what information.

Standing Answers

In any information network, people come to have different kinds of knowledge. Experts in different areas emerge, and others go to these experts to ask questions in the area of expertise. Expert advice can be expensive, as anyone who has gone to an auto mechanic lately can testify. One function of this high cost is to control access, so that the experts are not overwhelmed by demands on their time. (Another function is to make the experts rich.) In situations where the cost of accessing experts is kept low (as in Great Britain's system of socialized medicine), other kinds of barriers arise (difficulty in getting appointments, long waits in office waiting rooms, and other problems).

How can access to expert knowledge be handled in mixed-intelligence networks? Say that you are an expert member of such a system, on the topic of backpacking in San Diego County. You receive questions from all over, which you answer for a small fee. After a while, since you give good answers, questions pour in. Worse, most of the questions are the same. You get tired of answering the same old questions again and again and again.

What can you do? You can program your personal computer to scan through the incoming messages. Any that the computer can identify as a "standard" question, it answers with your "standard" answer. You have thus specified a *standing answer*, which is to be given to any incoming question matching your specification for the standing answer.

Slowly, you build up a computer data base of your specialized knowledge that is readily available to other people. You can easily add new information and remove incorrect or obsolete information. Questions that do not fit any standard pattern are automatically passed on for your expert human judgment, and any question that even *you*, the expert, cannot handle can be forwarded to another expert.

From the point of view of the question, it bounces around the network, with each node it visits attempting to answer it. Both computer and human nodes in this net can easily face the possibility of being unable to handle a question, since it is easy to pass the

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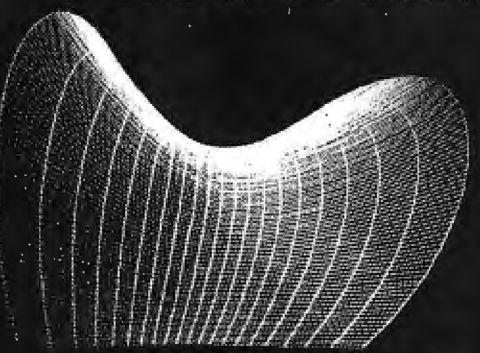

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question on to some other node if the current node cannot answer it.

To keep the network from filling up with unanswerable questions, any question that is unanswered after traversing enough nodes can be sent back to the asker with the answer of "unknown." In fact, if a small "handling charge" is added to a question at each step, then the asker can specify exactly how hard the system as a whole should work in trying to answer a question by specifying a maximum cost for a question. A question judged by the asker to be unimportant would either be answered in the first few steps or returned unanswered, while an important question would keep circulating on to new experts for consideration.

Any question can be answered differently by different experts. A mixed-intelligence information network easily handles this kind of conflict by sending *all* answers back to the asker.

The asker may not want to deal with multiple conflicting answers. This situation provides for another kind of mediator in these interactive networks: one that collects divergent answers to a question and selects one. This "sifter" role is similar to that played by editors and other gatekeepers in the current mass-media systems. The flexibility of these new interpersonalized media is illustrated here by the fact that a person can choose to have his or her answers edited or not, and can directly select the mediator.

If a given piece of expertise is in great demand, then it will spread through the network, becoming common knowledge.

Standing Questions

We started this exploration of interactive information systems by considering the possibilities for personalized news. I discussed the possibility for each person to specify his or her own "news filter." A more active way to view this personalization is that each participant in a mixed-intelligence network can formulate *standing questions.* These questions can reside in one or more of the nodes of the net, and any information arriving at that node which answers the standing question will be sent to the asker. For example, you might set up as a standing question, "What is the score of the most recent Pittsburgh Steelers' football game?" or "Has Fermat's Last Theorem been proven?" or "What will the weather be tomorrow?" Whenever the answer to any of these questions crosses a node containing the corresponding standing question, that node will send you that information.

Diffusion of Knowledge in a Mixed-Intelligence Network

Expertise can spread through these interpersonalized-media information networks in a way directed by the demand of the participants. Each node in the net can keep a record of how often it has asked a given question of a given expert. If the question is asked and answered often enough, then the node in question can store the answer received to be then used as its *own* standing answer, thereby moving that bit of knowledge one step outward through the net.

The decision at each node can be individually determined, but presumably would be based on the trade-off between the cost of contacting the expert and the cost of storing the information locally. This trade-off is conditioned on the likelihood of needing that information in the future, which can be judged by the need in the recent past. If a given piece of expertise is in great demand, it will spread through the network, becoming common knowledge.

In an area of knowledge that is rapidly changing, each node can guarantee the integrity of its own knowledge by leaving behind, with the experts consulted, standing questions that request any *updated* answers to those questions. In special cases, experts may want to selectively disseminate corrections to those nodes that had previously received answers to questions. In this way, knowledge among participants of an interpersonalized-media network can be flexibly and efficiently distributed and updated.

Feasibility Issues

Are the kinds of interpersonalized media I have described so far possible

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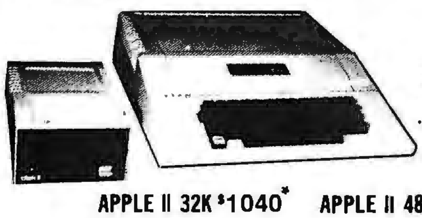

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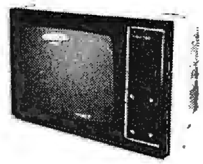

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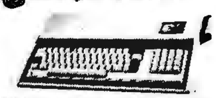

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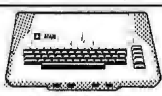

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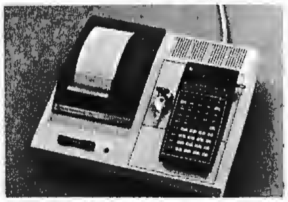

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Circle 182 on inquiry card. Circle 183 on inquiry card.

Listing 1: *A typical message sent using the electronic-mail system called MSG at the University of California, San Diego. This particular message was sent to two recipients, the author (Levin) and Hutchins.*

```
To: hutchins levin
From: dan
Date: Thu Nov 15 17:42:31 1979
Subject: wednesday at 3 pm
cc:
Message:

I have put the two of you down for 3 PM, Wednesday. OK?

My office.

dn
```

Listing 2: *The procedure for generating a message under the MSG electronic-mail system. All input by the user is shown underlined. The caret (^) indicates use of a control character, in this case a control-D.*

```
<—sndmsg
To: hutchins
Subject: tomorrows meeting with dan
cc: levin
cc:
Type message, end with^D
Should we get together shortly before 3 to go over what we'll cover with dan?
^D
```

now? If not, what capabilities are needed to make them feasible? These kinds of information networks depend heavily on distributed processing and storage, features that are optionally available with relatively inexpensive off-the-shelf personal computers. The existence of computer-based community bulletin boards demonstrates the feasibility of using current microcomputers (for example, the Apple II and Radio Shack TRS-80).

The physical interconnection can be provided by the dialed-telephone network (as in existing bulletin-board systems), by a combination of dialed and leased lines (as in existing nationwide packet-switched networks), by cable television lines, or by radio transmission.

The simplest format for message transmission is to transmit straight ASCII (American Standard Code for Information Interchange) characters through an acoustic-coupler modem. With noisy lines (generated by all of the physical interconnections described above), you lose characters, but for many purposes this is acceptable (the English language is considerably redundant). However, a protocol called Dialnet is currently being developed at Stanford University for personal computers (see *Dialnet Protocol* by M Crispin and I Zabala, Stanford Artificial Intelligence Laboratory, Palo Alto CA, 1979). This protocol, which sends information in error-resistant blocks called *packets*, and ones like it, can allow personal computers to use noisy lines to send noise-free messages.

In many cases, users are not overly concerned about the possibility that some unknown person might look at their electronic mail. Yet most often we prefer to know that nobody else is reading our mail. In some cases, this need for privacy is critical. There are many simple encoding/decoding algorithms that provide some security; unfortunately, these simple algorithms are relatively easy to decipher. (As an example of such a system, you can encode a message by calculating the exclusive-OR of text segments with a secret key, then have the receiver decode it by another exclusive-OR operation with the same key.)

Recently, a series of *trap-door* encoding/decoding algorithms have been developed, at Stanford by Diffie and Hellman in 1976 and later at the Massachusetts Institute of Technology (MIT) by Rivest, Shamir, and Adleman in 1977 (see references 4 and 12). Trap-door algorithms prom-

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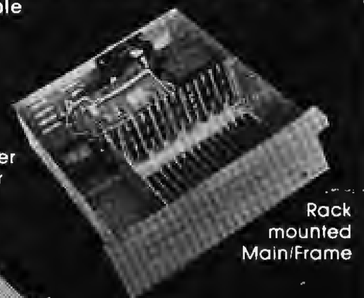

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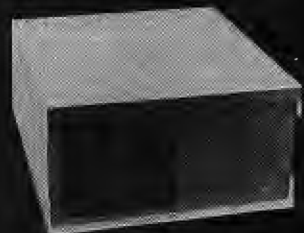

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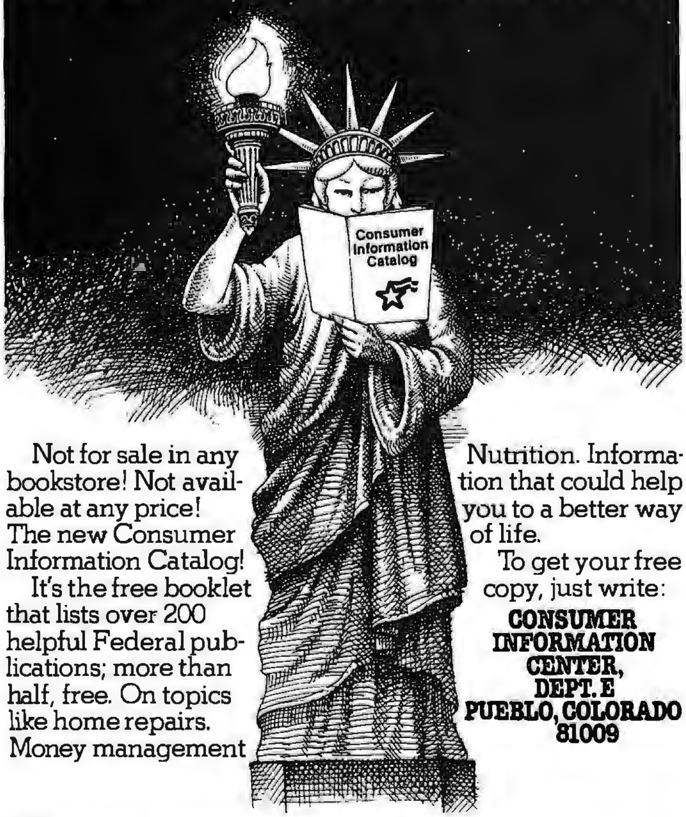

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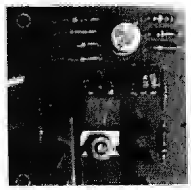

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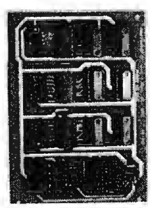

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ise an extremely high degree of security for even everyday use. A clear description of these cryptic functions is provided by Martin Gardner in the August 1977 issue of *Scientific American* (reference 5).

MSG: A Usable Electronic-Mail System

Many different software approaches have been tried for sending and receiving electronic mail. However, certain features are common to many existing electronic-mail systems. These have been included in a system called MSG. Every message is structured in a way illustrated in listing 1.

One command that is needed is S (an abbreviation for *sndmsg*), which automatically puts in the "From" and "Date" parts of the message header and assists in entering the rest of the message. For example, a message-generation sequence is shown in listing 2 (user input is underlined).

On the UNIX operating system, the MSG program announces the arrival of new mail to you with the following message:

From levin: tomorrows meeting with dan

Two commands are used to read mail. The H (for *header*) command allows you to skim over mail, since it prints out only the sender and subject headers of the message. The T (for *type*) command then prints out the messages specified. The D (for *delete*) command is used to delete messages.

A command that seems to add significantly to the utility of the mail system is the A (for *answer*) command, which quickly sends a reply to the originator of a message. When the A command is used, the MSG system automatically fills in the entire header, so that the user can easily compose a quick response.

The ability in MSG to define a *group* of people to receive messages allows this message system to be used for teleconferencing. With the MSG system, a user can type a list of names into a text file, then send one or more messages to all of these people simply by supplying the name of the text file.

The particular MSG system described here has other nice features, such as a *forward* command and the ability to keep several different mail files. But the capabilities described above seem to be the ones that make the system valuable enough to be used widely.

New Images of News

We have explored a new world—a world in which "news" is defined by each individual. Everyone serves as his or her own editor of news through the establishment of a set of standing questions. Everyone also serves as a reporter of news by submitting standing answers to the information network. These standing questions and standing answers bounce around the net until they are appropriately matched, possibly through the assistance of various kinds of mediators. Knowledge spreads through the net, following the heavily traveled paths to where it is needed.

This new kind of information network has major implications for us and for our society. I have touched on some of these issues here; I am also exploring the effects of this kind of interactive media on education and on entertainment (see references 8 and 9). These other uses of interpersonalized media will affect the information-interchange uses, since the educational and entertaining uses are likely to carry personal computers into homes, thus bringing about widespread use. Costs are dropping substantially, but even so, not many people are likely to invest several hundred dollars to improve their information access. However, they *are* likely to invest that amount for entertainment. So the educational and informational uses may well follow interactive entertainment.

For More Information

If you are concerned with developing new forms of interactive communication, I urge you to contact me and my associates by whatever medium you select. Our mailing address is given at the beginning of this article; our telephone number is (714) 452-4410. We are located at Third College, Media Center Communication Building, and my address for electronic mail is "catt:levin" for those with access to UCSD's word-processing system. ■

I want to thank the many Communications students at UCSD who participated in the development of these ideas, and Yaakov Kareev for helpful comments on earlier versions of this paper. My thanks to the many people across the country who participated in the evolutionary development of the MSG electronic-mail system, including Martin Yonke, John Vittal, and others at BBN, and Greg Haerr at UCSD.

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A Bits item in the March 1980 BYTE ("Real-Time BASIC Available Free," page 174) reported that the LLL BASIC system developed at the Lawrence Livermore Laboratory was available for just the duplication fee from the National Software Center in Argonne, Illinois. One of our readers called the Center and learned that the duplication fee for LLL BASIC is $159. ■

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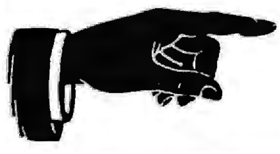

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Fifteen: A Game of Strategy

(or Tic-Tac-Toe Revisited)

John Rheinstein
10 Gould Rd
Lexington MA 02173

Most of us lost interest in the game of tic-tac-toe by the age of ten or twelve. By this time we had learned the strategy, and the game presented no further challenge. Upon casting the game in a different format, though, the strategy is no longer so obvious and a new, more challenging game may be developed. The game of Fifteen, described in Robert Teague's *Computing Problems for FORTRAN Solution*, is such a game.

Listing 1: *The game of Fifteen, written in Digital Group MaxiBASIC. The program can be easily modified to run in other versions of BASIC. Fifteen is a two player game. Players alternate picking numbers between 1 and 9, using each number only once. The object is to select numbers so that the sum of three of them is 15, while at the same time preventing the opponent from achieving the sum with three numbers.*

```
10      #" _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _"
20      #" F I F T E E N - A  G A M E  O F  S T R A T E G Y"
30      #" _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _"
40      #" D O  Y O U  W A N T  I N S T R U C T I O N S  (Y OR N)";
50      INPUT A$
60      IF A$ <> "Y" THEN 160
65      #""
70      #"  YOU AND THE Z-80 ALTERNATE PICKING NUMBERS BETWEEN"
80      #"  (INCLUDING)  1 AND 9 - YOU START. THE OBJECT IS TO"
90      #"  PICK THREE NUMBERS THAT SUM TO 15, AND TO KEEP THE"
100     #"  Z-80 FROM DOING THIS. "
110     #"  IF YOU PLAY PERFECTLY YOU MAY WIN OR FORCE A TIE. "
120     #"  IF YOU GOOF - THE Z-80 MAY WIN. "
160     DIM C (11) ,D (11)
170     FOR K=1 TO 11
180     READ C (K) ,D (K)  :NEXT K
190     FOR K = 1 TO 9
200     READ A1 (K) ,B1 (K)  : NEXT K
230     DIM B (9) ,A (3,3)
250     #""
260     #" N E W  G A M E  S T A R T S  N O W . . . "
270     FOR J=1 TO 3
280     FOR I=1 TO 3
290     LET A (I,J) =0
300     NEXT I
310     NEXT J
320     LET Z=0
330     #"" : #" Y O U R  M O V E",
340     INPUT C1
345     #""
350     IF C1 > 9 THEN 620
360     IF C1 < 1 THEN 620
370     R = A1 (C1) :C = B1 (C1)
```

Listing 1 continued on page 232

The game of Fifteen is a two player game. The players alternate picking numbers between 1 and 9, using each number only once. The object is to select numbers such that the sum of three of them is 15, and at the same time to prevent the opposing player from achieving a sum of 15 with three numbers. For example, assume that the two players are A and B. If the first player, A, picks the number 5, the status of the game may be indicated as shown below:

1	2	3	4	5	6	7	8	9
				A				

If the second player, B, then picks the number 3, we have:

1	2	3	4	5	6	7	8	9
		B		A				

Continuing, we might have:

1	2	3	4	5	6	7	8	9
		B	A	A	B			

Neither player can now achieve a sum of 15 in the next move, which might look as shown here:

1	2	3	4	5	6	7	8	9
B		B	A	A	B		A	

On the next turn A can win by picking 2 as follows:

1	2	3	4	5	6	7	8	9
B	A	B	A	A	B		A	

since the sum of 2 + 5 + 8 is 15.

The relationship between tic-tac-toe and the game of Fifteen, as described above, is based upon the 3 by 3 magic square:

6	1	8
7	5	3
2	9	4

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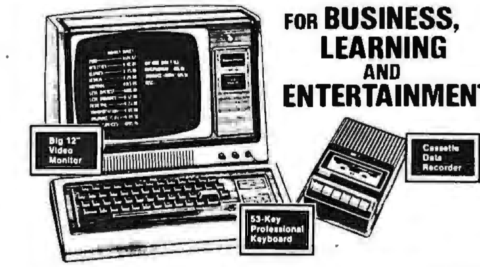

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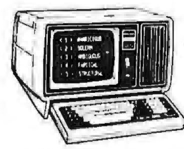

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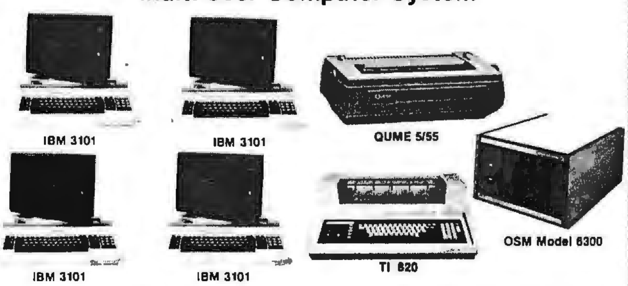

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It may be seen that the sum of any horizontal row, any vertical column, or any diagonal is 15. In addition, no other combination of three of these numbers sums to 15. Thus playing the game of Fifteen is the same as playing the game of tic-tac-toe if the relationship indicated in the magic square is known. If this relationship is not known, then derivation of the strategy, except by enumeration of all cases, is not trivial.

The accompanying listing was written in MaxiBASIC for a Digital Group Z-80 microcomputer. With minor changes it should run on any computer with BASIC. If your version of BASIC does not have an EXIT statement, then just leave this statement out of any lines in which it appears. The symbol # is a short form of the command PRINT. The program is based upon a modified version of the game of tic-tac-toe in David Ahl's *101 Basic Games.* As listed here, the computer will make a random move on its first or second move, after which it will play perfectly. If you play perfectly, you will either win or force a tie, each of these outcomes having roughly an equal probability of occurrence.

If you are playing the game of tic-tac-toe as listed in Ahl's book, inserting the following statement will make the game much more interesting by eliminating some less than optimal moves:

```
1915 B(8) = A(3,1) + A(2,2) + A(1,3)
```

I have found that friends who evidence no interest in playing the game of tic-tac-toe will play the game of Fifteen with great interest and find it to be challenging. As soon as I indicate the magic square relationship with tic-tac-toe, the interest quickly wanes after just a few more games. I hope you'll find the game interesting, too. ■

Listing 1 continued:

```
380    IF A (R,C) <>0 THEN 620
390    LET A (R,C) = -1
400    GOSUB 1660
410    IF Z=1 THEN 490
420    REM MACHINE MOVE
430    GOSUB 1100
440    REM TEST FOR GAME WIN
450    GOSUB 1660
460    IF Z=0 THEN 650
490    # " "
500    FOR K = 1 TO 9
510    B = A (A1 (K) ,B1 (K) )
520    # TAB (20) ;K ;
530    IF B <> 0 THEN 550
540    # "  "
545    GOTO 575
550    IF B > 0 THEN 570
560    # "     Y O U    " ;
565    GOTO 571
570    # "     Z - 8 0    " ;
571    IF ABS (B) > 1 THEN #" * " ;
573    # " "
575    NEXT K
580    # " "
590    IF Z<>0 THEN 2070
600    GOTO 330
620    # " I L L E G A L  M O V E,  T R Y  A G A I N"
630    # " "
640    GOTO 330
650    LET T2 = 0
660    FOR J=1 TO 3
670    FOR I=1 TO 3
680    IF A (I,J) <>0 THEN 700
690    LET T2=T2+1
700    NEXT I
710    NEXT J
720    IF T2 > 0 THEN 270
730    GOSUB 1340
740    GOTO 490
750    IF T2>1 THEN 490
760    FOR J=1 TO 8
770    IF B (J) = -2 THEN EXIT 800
780    NEXT J
790    GOTO 730
800    GOSUB 2000
810    GOTO 490
900    FOR J = 1 TO 9
910    B (J) = 0
920    NEXT J
930    FOR J = 1 TO 3
940    FOR I = 1 TO 3
950    B (J) = B (J) + A (J,I)
960    B (J+3) = B (J+3) + A (I,J)
970    NEXT I
980    NEXT J
990    B (7) = A (1,1) + A (2,2) + A (3,3)
1000   B (8) = A (1,3) + A (2,2) + A (3,1)
1010   RETURN
1100   FOR I = 2 TO 3
1110   C (I) = INT (2.99*RND (0) ) + 1
1120   D (I) = INT (2.99*RND (0) ) + 1
1130   NEXT I
1200   FOR I = 1 TO 8
1210   IF B (I) >1 THEN EXIT 1370
1220   NEXT I
1230   FOR I=1 TO 8
1240   IF B (I) <-1 THEN EXIT 1370
1250   NEXT I
1270   FOR K=1 TO 11
1280   LET I=C (K)
1290   LET J=D (K)
1300   IF A (I,J) <>0 THEN 1330
1310   LET A (I,J) = 1
1320   GOTO 1360
1330   NEXT K
1340   # " . . . T I E  G A M E . . . "
1350   LET Z=3
1360   RETURN
1370   IF I>3 THEN 1440
1380   FOR J=1 TO 3
1390   IF A (I,J) =0 THEN EXIT 1420
1400   NEXT J
1410   GOTO 1360
1420   LET A (I,J)=1
1430   GOTO 1360
1440   IF I>6 THEN 1510
1450   FOR J=1 TO 3
1460   IF A (J,I-3) =0 THEN EXIT 1490
1470   NEXT J
1480   GOTO 1360
1490   LET A (J,I-3) =1
1500   GOTO 1360
1510   IF I>7 THEN 1550
1520   FOR J=1 TO 3
1530   IF A (J,J) =0 THEN EXIT 1590
1540   NEXT J
1550   IF A (1,3) =0 THEN 1610
1560   IF A (3, 1) =0 THEN 1630
1570   LET A (2, 2) =1
1580   GOTO 1360
1590   LET A (J,J) =1
1600   GOTO 1360
1610   LET A (1,3) =1
1620   GOTO 1360
1630   LET A (3, 1) =1
1640   GOTO 1360
1660   LET T1 =0
1700   FOR J = 1 TO 3
1710   IF A (J, 1) <>A (J, 2) THEN 1750
1720   IF A (J, 1) <>A (J, 3) THEN 1750
1730   T1 = A (J, 1)
```

Listing 1 continued on page 234

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Listing 1 continued:

```
1740  A (J, 1) = 3*A (J, 1)
1745  A (J, 2) = A (J, 1) :A (J, 3) = A (J, 1)
1750  NEXT J
1760  FOR J = 1 TO 3
1770  IF A (1, J) <> A (2, J) THEN 1810
1780  IF A (1, J) <> A (3, J) THEN 1810
1790  T1 = A (1, J)
1800  A (1, J) = 3*A (1, J)
1805  A (2, J) = A (1, J) : A (3, J) = A (1, J)
1810  NEXT J
1820  IF A (1, 1) <> A (3, 3) THEN 1860
1830  IF A (1, 1) <> A (2, 2) THEN 1860
1835  T1 = A (2, 2)
1840  A (1, 1) = 3*A (1, 1)
1845  A (2, 2) = A (1, 1) : A (3, 3) = A (1, 1)
1860  IF A (1, 3) <> A (3, 1) THEN 1910
1870  IF A (1, 3) <> A (2, 2) THEN 1910
1880  T1 = A (2, 2)
1890  A (1, 3) = 3*A (1, 3)
1900  A (2, 2) = A (1, 3) : A (3, 1 ) = A (1, 3)
1910  IF T1 > 0 THEN 2030
1915  IF T1 < 0 THEN 2000
1920  GOTO 900
2000  # . . . Y O U  W I N — T H I S  T I M E . . ."
2010  LET Z=1
2020  RETURN
2030  #" . . . Z — 8 0  W I N S  T H I S  T I M E . . ."
2040  LET Z=2
2050  RETURN
2070  # " DO YOU WISH TO PLAY AGAIN (Y OR N) " ;
2080  INPUT X$
2090  IF X$= "Y" THEN 250
2120  # " "
2130  # " THANKS FOR THE GAME. HOPE YOU HAD FUN!! "
2135  #" "
2140  GOTO 9999
2150  DATA 2, 2, 1, 1, 3, 3, 1, 1, 3, 3, 1, 3, 3, 1, 1, 2, 3, 2, 2, 3, 2, 1
2160  DATA 2, 3, 3, 1, 1, 2, 1, 1, 2, 2, 3, 3, 3, 2, 1, 3, 2, 1
9999  END
READY
```


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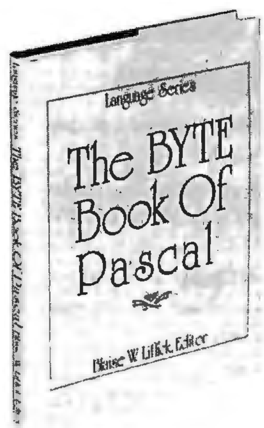

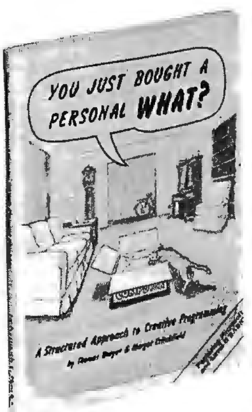

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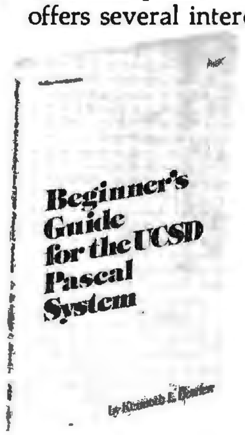

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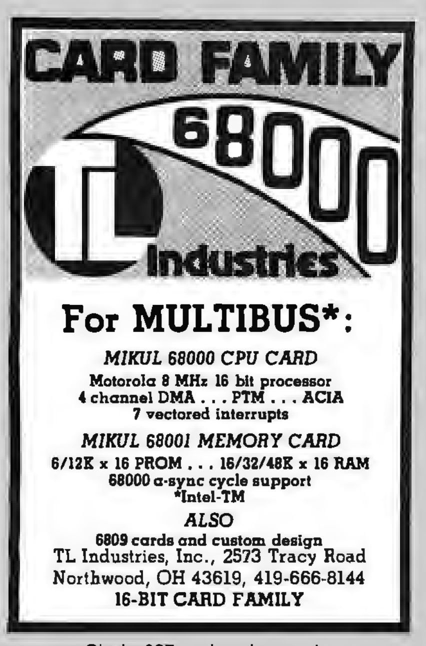

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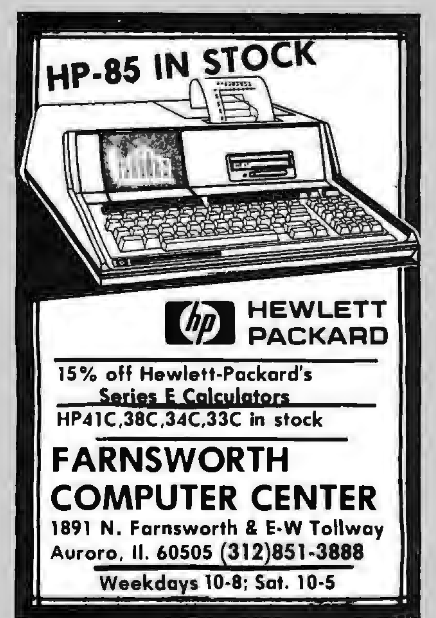

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Comment and Correction for Mouse

Tom Lane, 612 W Laurel, Ft Collins CO 80521

I enjoyed Peter Grogono's article on Mouse (July 1979 BYTE, page 198). It demonstrates that an interesting and powerful language can be implemented with very little effort, if carefully designed. The decision to express the program in a machine-independent form such as Pascal was especially commendable; it makes the program easier to understand and useful to a wider range of readers. I hope that other authors will follow this example.

A major benefit of a high-level program is that it is more easily understood and debugged than the equivalent assembly-language program. I hope to graphically demonstrate this claim by reporting on several bugs which I found in the Mouse interpreter program.

First off, there were several typographical errors in the listing. Line 42 should have read "CAL := CAL − 1", not "CAL := CAL = 1". This kind of syntax error would be caught by an assembler as well as a compiler, so Pascal is not ahead here. Line 176 should have been "PARAM: PARBAL := PARBAL + 1;" (a plus sign not a minus). In order to catch this error, one must understand the logic of the loop on lines 172 thru 179. The equivalent assembler code would be much more than eight lines long, and would contain a lot of extraneous detail (eg: how to access the STACK data structure); the incrementing and decrementing of PARBAL would not stand out at all.

The next problem I found was in the SKIP routine. It fails if it has to skip over a quoted string containing one of the bracketing characters. For example, consider the program fragment:

```
A. [ "PRINT A BRACKET ] HERE" ]
```

If A≤0, SKIP will be invoked to skip over the conditional clause. In its present form it will only skip to the first right bracket; the interpreter then tries to evaluate the rest of the quoted string. When the closing quote is reached, control takes off looking for a matching quote, which is never found. We can fix this by rewriting SKIP as follows:

```
CNT := 1;
repeat
   GETCHAR;
   if CH = '"' then
      repeat GETCHAR until CH = '"'
   else if CH = LCH then CNT := CNT + 1
   else if CH = RCH then CNT := CNT − 1
until CNT = 0
```

This bug looks like a simple oversight. Such oversights are probably more common in assembler programs, simply because there is more code and thus there are more opportunities to forget something.

The same problem exists in the loop on lines 182 thru 190, which searches for the desired actual parameter in a macroinstruction call. Furthermore, this loop will fail when an actual parameter being skipped over contains two adjacent macroinstruction calls, as in:

```
#A, #B, 1; #C, 2; , 34;
```

Here, after skipping over "#B, 1;" by calling SKIP at line 187, the GETCHAR on the same line advances CH to the following "#". But since this is already past the test for CH = '#', the second macroinstruction call is not recognized as such. If we were looking for the second parameter of A, "2" would be found instead of "34". What is really needed, following the call to SKIP, is to return to the GETCHAR call at line 183. With both problems fixed, the loop becomes:

```
repeat
   GETCHAR;
   if CH = '"' then
      repeat GETCHAR until CH = '"'
   else if CH = '#' then SKIP('#',';')
   else if CH = ',' then PARNUM := PARNUM − 1
   else if CH = ';' then PARNUM := 0
until PARNUM=0;
```

Notice that we have to modify the loop exit logic so that it will not exit after returning from SKIP (for we are not done scanning, even though CH=';'). I suspect that the original code did exit the loop in this case, and that this bug arose as a result of trying to fix the SKIP code rather than the exit condition. This particular bug would never have occurred in assembler code, since after the call to SKIP one would merely jump back to the top of the loop; it illustrates that "GOTO-less programming" has its own pitfalls.

Finally, there is a subtle problem with the allocation of local variables for macroinstructions. Consider the program:

```
#A, #B; ;
$A Q1= %A Q.! @
$B Q33= @
$$
```

When A is invoked it sets its local variable Q to 1, then evaluates its parameter, which results in B being invoked. B sets its local variable Q to 33. Since A and B have independent local variables, this should not change A's Q, so when A finally prints out the value of Q it should print 1.

With the interpreter as published, it prints 33. This can be seen by following the manipulations of OFFSET. Initially OFFSET=0, signifying that the main program's variables A thru Z occupy DATA locations 1 thru 26.

When macroinstruction A is invoked, OFFSET is set to 26 (see line 160 in the interpreter), so that A's variables occupy 27 thru 52; in particular, Q occupies 43. When we start to evaluate A's actual parameter, OFFSET is reset to 0 (see line 181). This is essential since variable names within the text of the actual parameter should refer to main program variables. When the call to B is processed, OFFSET is set to 26 (line 160 again), so B's variables are allocated on top of A's variables. Hence, when B stores into its Q, A's Q gets changed.

The problem essentially is that the variable OFFSET is used for two incompatible purposes. One is to keep track of the current context (ie: the set of locations to which the names A thru Z refer). The other is to remember how much of the DATA array is in use, so that fresh locations can be allocated when a macroinstruction is called. These uses are obviously incompatible because the total storage allocation changes only at macroinstruction call and return, while the context changes at macroinstruction call/return *and* when accessing actual parameters.

Once the problem is phrased this way, the fix is simple. I chose to retain OFFSET for indicating context, and to introduce a new variable LASTUSED for keeping track of free space. The required changes are:

> In line 17, add LASTUSED to the list of global integer variables.
> In line 88, add "LASTUSED := 26;"
> Replace line 160 with "OFFSET := LASTUSED; LASTUSED := LASTUSED + 26;"
> In line 166, add "LASTUSED := LASTUSED − 26;"

OFFSET is still saved and restored in the control stack; LASTUSED need not be, since it can only change as shown above.

All these bugs were found during two evenings of studying the interpreter listing, with no machine use whatever. The fixes were invented in the same period. I was later able to test the fixes on a Pascal machine; they all worked correctly the first time. I am sure you will agree that equivalent problems in an assembler program would not have been detected so easily nor fixed so readily.

The approach recommended by Mr Grogono, namely coding the algorithm in a high-level language and then translating to assembler, has great merit. It is capable of producing bug-free programs in a shorter time than the conventional methods. However, to achieve best results one must spend time examining the high-level program before plunging into assembler coding. (It helps a lot if you can actually run the program in that form.) As I hope I have demonstrated, it is much easier and quicker to remove bugs at this stage than later on.

Peter Grogono Replies:

First of all, I would like to commend Mr Lane for so carefully reading and checking the Mouse interpreter before rushing off to the nearest computer and attempting to implement it. If more programmers behaved likewise, there might not be a "software crisis" in industry today.

The proof copy of listing 6 that I received was a poor photocopy, hence the typographical errors in the program. The proof of the article was very clear, so I have no excuse for the error in the right-hand column on page 205; the definition of F should read:

```
$F N%A=1 (N.↑ N.* NN. 1−=) @
```

I have little to say about Mr Lane's other points. The problems that he identifies are all genuine bugs, and his corrections are simple and elegant. I would like to take this opportunity to apologize to other readers who have been inconvenienced by them.

As I mentioned in the article, Mouse is based on a language that I first implemented several years ago. The bugs are, perhaps, partly due to my confusion between the old and new versions of the language. This confusion also appears in the design. I now feel that I should have made % a postfix operator with a numerical operand, like the other unary operators. The formal parameters are then 1%, 2%,... rather than %A, %B,.... In general, % may be preceded by any expression that has a positive value. This extends the power of the language, as can be seen from the following program, which prints 15:

```
#S, 1, 2, 3, 4, 5, 0; !
$S N0= 0 ( NN.1+= N.%↑ N.%+ ) @
$$
```

The changes required to the interpreter are very small; in line 170 change

```
GETCHAR: PARNUM: = NUM (CH);
```

to

```
PARNUM: = POPCAL;
```

■

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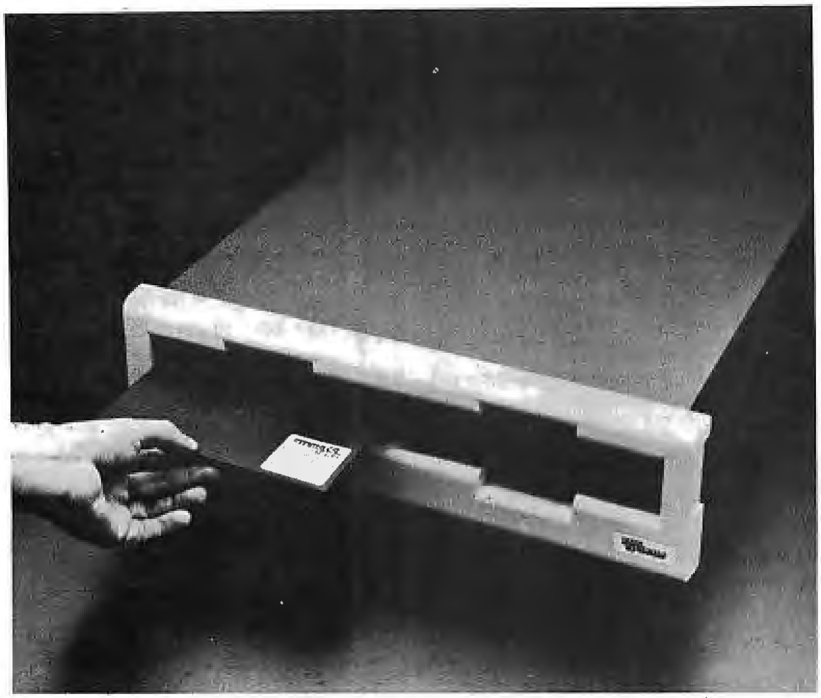

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Circle 597 on inquiry card.

Lobo Drives Offers Expansion Interface for TRS-80

Lobo Drives International, 935 Camino Del Sur, Goleta CA 93017, announced the addition of an enhanced expansion interface for the Radio Shack TRS-80 personal computer.

The model LX80 can expand memory storage capacity up to 40 megabytes. It provides facilities for up to 32 K bytes of programmable memory and offers a second serial port. The keyboard read-only memory (ROM) can be overridden for booting in diagnostics and customized operating systems. There is a bidirectional parallel port exclusively for Lobo Drives' model 7710T Winchester hard-disk drive. Other features include a parallel Centronics printer port, screen printer port, two microprocessor-controlled bidirectional serial ports, and a crystal-controlled real-time clock. The model LX80 expansion interface is priced at $525.

Circle 598 on inquiry card.

What's New?

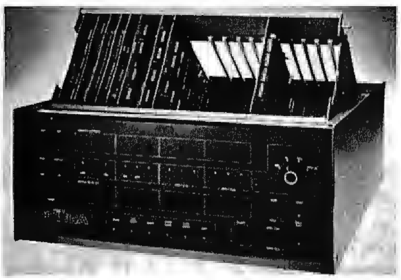
SYSTEMS

6809 SS-50 Microprocessor Card Is Also Stand-Alone Microcomputer

The SBC/9 card can be used as a stand-alone control computer or as an upgrade processor card for SS-50 bus microcomputers. It includes its own operating system; 1 K of programmable memory; I K bytes of read-only memory; and a full-duplex, RS-232C serial interface. The card is completely compatible with the SS-50 bus and requires no modification. The SBC/9 hardware features include a port for 8-bit bidirectional data lines, a multilevel data bus, extended address line capability to accommodate up to 16 megabytes of memory, a serial interface for use with cassette recorders, and more. The SBC/9 with the operating system and a manual sells for $199.95 from Percom Data Co, 211 N Kirby, Garland TX 75042.

Circle 599 on inquiry card.

Mainframe for PC/M's 12-bit, PDP-8-Compatible Microcomputer



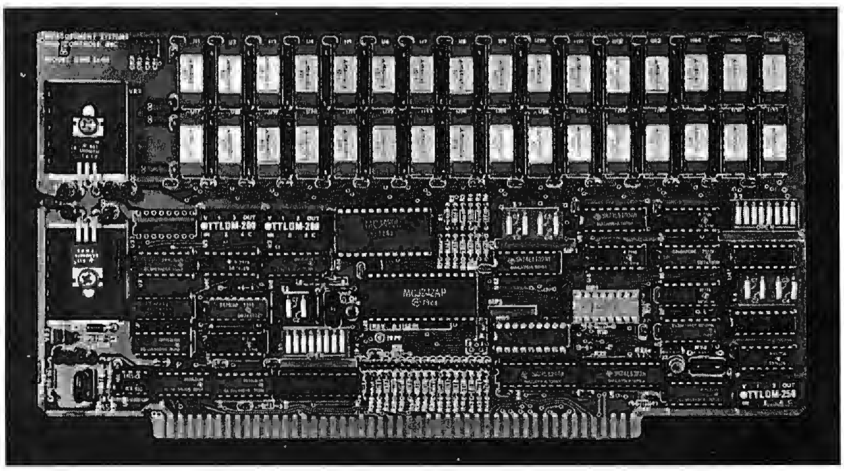
The PCM-12 Omega mainframe is compatible with Digital Equipment Corporation's PDP-8 series minicomputers. The PCM-12 is based on the 6100 microprocessor and is software-compatible with all PDP-8 systems. The mainframe includes connectors for 18 plug-in cards (enough for 32 K words of memory), and up to 14 peripheral interfaces and input/output (I/O) devices. The power supply is over-voltage protected and fold-back current limited. Operation is from 100 to 240 V, 50 or 60 Hz. The front panel structure provides real-time operational display and includes all PDP-8/E functions, plus built-in bootstraps for paper tape, RX01 and RX02 floppy disks, RK05 hard disk, and TU-58 DECtape. The Omega mainframe is priced at $889. Contact PC/M Inc, 6800 Dublin Blvd, Dublin CA 94566, (415) 829-8700.

Circle 601 on inquiry card.

R2E Introduces a Single Board Microcomputer

The model 80-20 is a small-business microcomputer system. The single board system includes a Z80 microprocessor; 32 K bytes of programmable memory, expandable to 64 K bytes; two single-sided, double-density, 5-inch floppy-disk drives with 140 K bytes of storage on each; an ASCII (American Standard Code for Information Interchange) keyboard; parallel Centronics printer interface; cabinet and power supply. The system also has a 1024-character uppercase and lowercase video display. Software for the model 80-20 includes R2E's BAL Language (Business Oriented BASIC) with sequential, indexed sequential, and random access file management, plus a macroassembler. Optional are FORTRAN, COBOL, Pascal, APL, CBASIC, and MBASIC (compiler and interpreter). These operate under CP/M. The 80-20 is priced under $3000. For more information, contact R2E of America, 47 Bedford St S E, Minneapolis MN 55414.

Circle 600 on inquiry card.



64 K-Byte Board Compatible with S-100 Bus Systems and MP/M

The DMB6400, a 64 K bank-selectable, dynamic-memory board, is compatible with Alpha Micro, Cromemco, North Star Horizon, and other S-100 bus computers, as well as MP/M systems. The memory board uses output-port addressing for the bank-select feature and is configured as 4 independent 16 K-byte banks of memory. Any of the 256 ports can be decoded, and 8 banks of memory are possible for each port. Each memory bank can be turned on or off at system reset, and phantom addressing can be used by any of the 4 banks. The memory board will run with all 8080 processors, 8085s at 3 MHz, and most Z80As at 4 MHz. In addition, it will run with the Marin M9900 processor. The boards come with documentation and are guaranteed for 1 year. Contact Measurement Systems and Control Inc, 867 N Main St, Orange CA 92668, for original equipment manufacturers and dealer pricing information.

Circle 602 on inquiry card.

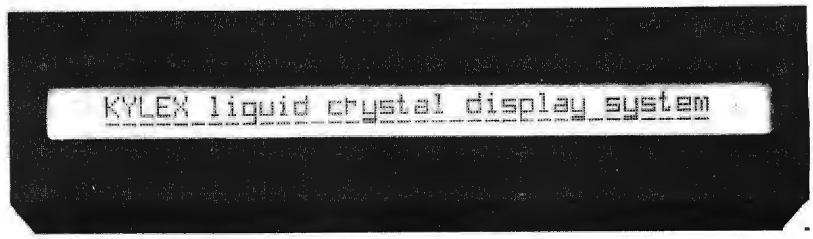
What's New?

MISCELLANEOUS

8-Inch Floppy-Disk Controller

Disk 2+2 is a single-density, 8-inch floppy-disk controller for the Apple II computer. It increases the data on line, increases the individual file size, and reduces the number of disks handled by the user. The board operates under the Apple disk operating system 3.1 or 3.2. It will control up to 4 standard 8-inch floppy-disk drives. The card uses a 1771 LSI controller integrated circuit that allows exchange from the Apple to IBM 3740 format. Disk 2+2 costs $400 and is available from Apple dealers. For more information, contact Sorrento Valley Associates, 11722 Sorrento Valley Rd, San Diego CA 92121.

Circle 603 on inquiry card.



One-Line, 40-Character, Dot-Matrix Liquid-Crystal Display (LCD)

Kylex Inc, 420 Bernardo Ave, Mountain View CA 94043, has introduced a one-line, 40-character, 5-by-10 dot-matrix LCD with integral electronics that can interface directly with microprocessors through a single peripheral parallel interface device. The LX140 is aimed at electronic typewriter, word processing, and terminal printer applications. It includes integral drive, refresh, temperature compensation, and power supply electronics. The LCD is designed for use in high ambient light conditions to reduce eye strain. The 5-by-10 dot matrix for each character provides display capability for the full ASCII (American Standard Code for Information Interchange) set, with each dot addressable.

Price for the LX140 in quantities of 100 and up is $199.

Circle 604 on inquiry card.

Sink the Bismarck

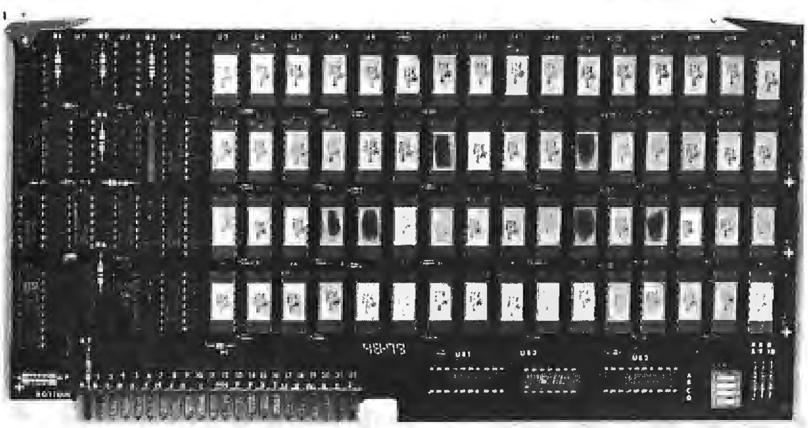
Computer Bismarck is an historical simulation game of the British attempt to seek and destroy the German battleship Bismarck in 1941. The game is played on an Apple II with Applesoft read-only memory (ROM) or an Apple II Plus. The game requires 48 K bytes of programmable memory and a floppy-disk drive. It features high-resolution color graphics and can be played by one or two players. Players take turns moving their vessels and aircraft across the North Atlantic. Only enemy units which are spotted are revealed to the players. Rules cover all of the critical aspects of the naval campaign, from weather to ship fuel capacities. Combat occurs when opposing units have spotted each other. Computer Bismarck comes with a program disk, rule book, and 7 player-aid charts for $59.95 from Strategic Simulations Inc, POB 5161, Stanford CA 94305.

Circle 605 on inquiry card.

64 K-Byte Dynamic Programmable Memory Board

The ST4203, a 64 K-byte dynamic programmable-memory board, is compatible with any processor in the STD BUS environment, and will operate at any microprocessor speed, up to and including 4.0 MHz. The onboard refresh controller feature allows the processor to synchronize to external events, or use peripheral controllers which require multiple WAIT states without regard to refresh timing. The ST4203 can take the place of four 16 K static programmable-memory cards, and it can make available 3 slots in the STD BUS card cage. Memory expansion for bank-selection and phantom-memory operations are selectable. A number of WAITRQ options are also available. Prices range from $220 for a card without memory to $700 for a complete 64 K-byte unit in the 2.5 MHz version. For more information, contact Applied Micro Technology, POB 3042, Tucson AZ 85702.

Circle 606 on inquiry card.



Memory Board for Hewlett-Packard 9845B/T Computer

Eventide Clockworks, 265 W 54th St, New York NY 10019, is manufacturing and marketing a board which adds 128 K bytes of programmable memory to the Hewlett-Packard (HP) 9845B/T computer. The Eventide WMAP-1 has identical capabilities to those of the HP part #09845-66526, but it costs half as much. The WMAP-1 board carries a full 1-year parts and labor warranty. Complete schematics, field installation instructions, and troubleshooting data are provided.

Circle 607 on inquiry card.

What's New?

MISCELLANEOUS

Catalog for Micah Software

A four-page foldout catalog lists software from Micah, POB 22212, San Francisco CA 94122. Micah software products include Expand, which expands CP/M to run Cromemco software; Spool, a spooler for CP/M or Cromemco; CBIOS, CP/M for Cromemco computers; and DUP/1, disk utilities for CP/M and CDOS. Micah also has Osborne business software and graphics software. Contact the company for a copy of the catalog.

Circle 608 on inquiry card.

Tabletop Winchester Tape Cartridge Add-On for DEC PDP-11

ABC Computers Inc, 500 Tonopah, POB 7529, Tahoe City CA 95730, (916) 583-5562, is offering a tabletop, 20-megabyte add-on Winchester system with a tape-cartridge backup unit for the Digital Equipment Corporation PDP-11 Series. The Winchester is the Marksman 14 drive from Cal Comp, a division of Xerox. The 17-megabyte tape cartridge is produced by DEI. The entire system is delivered in a 27.5 cm (10.5 inch) high cabinet complete with power supply and controller for $8600.

Circle 609 on inquiry card.

A New Software Vendor Directory

The Software Vendor Directory, a listing of microcomputer software vendors, is available from Micro-Serve Inc, POB 482, Nyack NY 10960. The publication lists over 700 vendors within 35 categories of hardware and operating systems. Software is classified into personal (games, etc), programming (operating systems, utilities, languages, etc), general business, and industry business (insurance, medical, etc). Vendors of books and other publications have also been included. The directory is designed for hardware and software vendors, computer stores, consultants, programming services, sales and marketing people; in short, those who need information on software products for microcomputers. *The Software Vendor Directory* is priced at $37.95. A quarterly update service is also offered at a price of $9.95 per issue.

Circle 610 on inquiry card.

12-Inch Monitor for Under $200

Leedex Corp, 2300 E Higgins Rd, Elk Grove Village IL 60007, has introduced a 12-inch black and white monitor, the Video 100-80. Built for industrial use, the monitor includes a metal cabinet and a removable face plate that provides mounting space for a floppy-disk drive. There is also space inside the cabinet for an 11-by-14 printed circuit board for custom-designed electronics. The 90-degree deflection picture tube allows an 80-character by 24-line display, and the unit features a 12 MHz bandwidth.

The Video 100-80 is plug compatible with Apple, Atari, Radio Shack, OSI, Microterm, and Exidy computers. It is priced under $200.

Circle 611 on inquiry card.

Light Pen for Apple II Users

The Lipson Light Pen is now available for the Apple II. The pen is packaged with 12 BASIC programs on cassette, a manual, cable, and a connector to PDL(0) on the Apple II. The demonstration programs are designed to be incorporated into programs created by the user. The pen utilizes a cadmium selenide cell for light detection, enabling the user to detect and measure varying intensities of light. High-resolution graphics, sound, and color are implemented in the demonstration programs. The Lipson Light Pen is available exclusively from ARESCO, POB 1142, Columbia MD 21044, for $24.95.

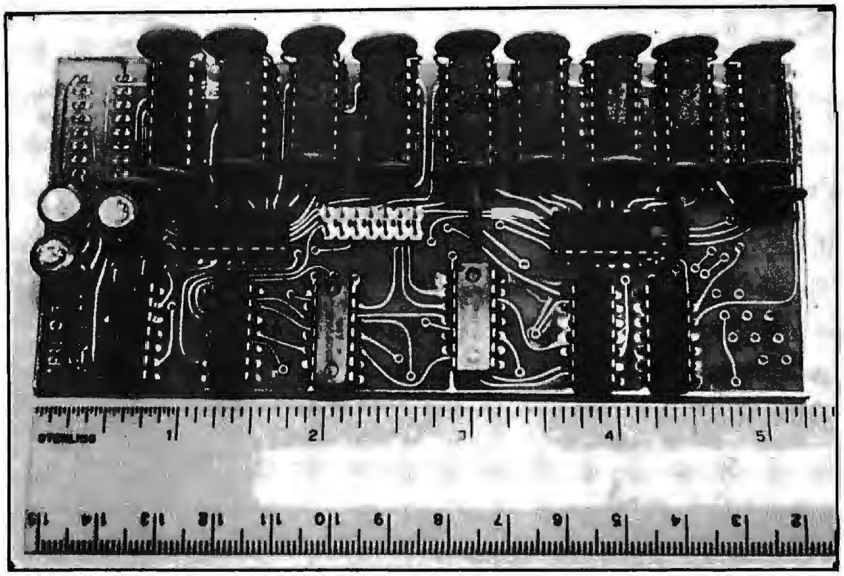
Circle 612 on inquiry card.

Floppy-Disk Head-Cleaning Kits from 3M

Scotch head-cleaning disks use a wet and dry method by which a cleaning solution is applied to the porous cleaning fabric in the disk envelope. The cleaning disk is then run in a normal manner for 30 seconds. Two-sided systems may be cleaned with the same technique. Each kit contains two disks and a bottle of fluid. A maximum of 30 cleanings is possible. Each 5- or 8-inch floppy-disk kit costs $30. Further details concerning the Scotch 7400 and 7440 head-cleaning disk kits may be obtained by writing to 3M, Dept DR80-1, POB 33600, St Paul MN 55133, (612) 733-9572.

Circle 613 on inquiry card.

Upgrade TRS-80 to Emulate Z80 CP/M System



The "Freedom Changes" are upgrades for the Radio Shack TRS-80 Model I personal computer. The Freedom Option reorganizes memory to emulate a standard Z80 machine that responds to CP/M software. The extended memory adds programmable memory to the Model I, bringing it up to 64 K bytes. Part of it is available in normal TRS-80 mode.

The Freedom Option consists of a board, system disk, and instructions. The board configures programmable memory at the bottom and the memory-mapped areas on top. The disk has the T8 operating system and the software to utilize the switch to make the system compatible with CP/M software. The disk format is changed to read and write in the IBM-compatible 128-byte sector convention. The system will recognize 35- or 40-track disk configurations. The extended memory puts certain unusable address locations into operation, thus adding 2560 bytes of programmable memory under normal TRS-80 operation. This space is ideal for programs such as RS-232 communication, debounce, lowercase, and more. In the Freedom mode, the extended memory allows the machine to function on programmable memory only.

Both changes require a 48 K-byte disk system. Only the extended memory requires minor hardware changes. The Freedom Option is priced at $245 and the extended memory is $295. Contact Field Engineering Consultants Ltd, POB 2368, Woburn MA 01888, (617) 944-5329.

Circle 614 on inquiry card.

Card File Consolidates AIM-65 with Expansion File

The MTU K-1005A-A card file integrates the AIM-65 computer, keyboard, and a series of expansion boards into a single compact unit. Drawing no power, the unbuffered motherboard utilizes the AIM bus structure to carry expansion connector signals to up to 4 additional boards. A fifth undedicated position is provided for a board not on the bus. The card file features a U-shaped black-anodized aluminum frame measuring 39.5 by 29.5 by 11.5 cm (15.5 by 11.5 by 4.5 inches). Other card files are offered for the PET, KIM-1, and SYM-1 computers.

The MTU K-1005A-A card file is priced at $95, including manual. For additional information, write Micro Technology Unltd, 841 Galaxy Way, POB 4596, Manchester NH 03108.

Circle 615 on inquiry card.

AC Remote-Control System for the PET

Honders Inc offers a complete AC remote-control system for the Commodore PET or CBM. Most electrical devices can be switched on or off and lamps can be dimmed or brightened under computer control. No additional wiring is needed. Up to 256 points can be controlled. This system is useful for security- and energy-control systems. The basic package includes a plug-in module to the PET's second port, 3 remote power controllers, and a cassette software package for demonstration and applications. The package may be ordered for $179 from Honders Inc, Kennel Rd, Cuddebackville NY 12729.

Circle 616 on inquiry card.

Sound Generator for the Apple II

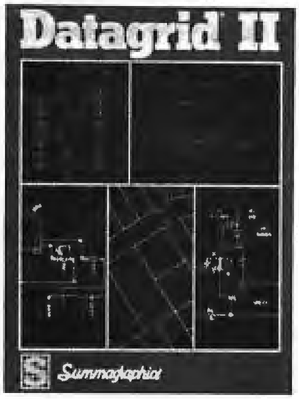
Symtec Inc has introduced a sound-synthesizer card for the Apple II. The Super Sound Generator, or SSG, uses 13 programmable registers to control three voices. The SSG is provided with an output cable and RCA phono plug for hook-up to stereo systems. It features separate 8-bit parallel input and output (I/O) ports for connection to accessories, such as an alphanumeric keyboard, an organ keyboard interface, or a parallel printer driver. SSG control is accomplished with a series of 4 POKES to 3 memory locations. The SSG card may be programmed in any language available for the Apple. The music composing software provides for entry and editing of the entire music score using keyboard commands. The score can be copied by a graphics printer. Stereo effects and orchestrations can be produced using multiple cards. Up to 21 voices can be accessed by the user with a complete complement of SSG cards. The Symtec SSG is available for $159.95 from Symtec Inc, POB 462, Farmington MI 48024.

Circle 617 on inquiry card.

What's New?

MISCELLANEOUS

Datagrid II Computer-Aided Drafting Systems Brochure



The Datagrid II series of computer-aided drafting systems is described in a brochure from Summagraphics Corporation. The Datagrid II series are used by engineers, draftsmen, and others to create designs and drawings. The brochure is free from Summagraphics Corp, Dept MS-80, 35 Brentwood Ave, Fairfield CT 06430, (203) 384-1344.

Circle 618 on inquiry card.

High-Resolution Video Display with a Refresh Rate of 60 Hz

A black and white high-resolution video display which refreshes at 60 Hz (eliminating the flicker of many high-resolution displays) has been introduced by Calma, 527 Lakeside Dr, Sunnyvale CA 94086. The RB1000 uses an internal graphics processor with its own raster memory that controls all display functions. This allows the refresh rate of 60 times per second. The high resolution of the 1280-by-1024 video monitor eliminates the "stair-stepping" appearance of nonorthogonal lines. Separate video screens for graphic displays and for nongraphic alphanumeric data are provided. The unit features selective erase, on-screen menus, and multiport views. The Calma RB1000 is available on Calma interactive-graphics systems as an extra item.

Circle 619 on inquiry card.

Anniversary Catalog from V R Data

V R Data has introduced its eighth anniversary catalog. The complete Centronics and Apple line of equipment and supplies from MPI, Pertec, Nashua, NEC, Memorex, Maxell, and Dysan are featured. V R Data also includes its disk head-cleaning kit for 5- and 8-inch floppy-disk drives, for $12.95. For a catalog, call toll free, (800) 345-8102, or write V R Data Corp, 777 Henderson Blvd, Folcroft Industrial Park, Folcroft PA 19032.

Circle 620 on inquiry card.

Letter-Quality Printer Interface from MicroPro

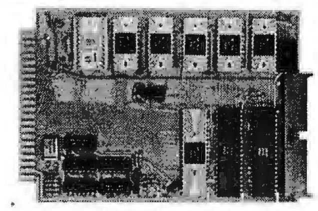
The I/OMaster S-100 interface board allows use of lower cost letter-quality printers and/or high-speed line printers within the same microcomputer configuration. The I/OMaster interfaces with less expensive versions of the NEC, Diablo, and Qume letter-quality printers, and can also be used with high-speed Centronics printers for draft and nonletter-quality applications. The board features two serial and two parallel ports, and 8-level interrupt-control and dual-interval timer circuitry. The two 8251-based serial ports have built-in 32-character first-in, first-out (FIFO) buffers to prevent loss of data during switching operations. The I/OMaster costs $400 from MicroPro International Corp, 1299 Fourth St, San Rafael CA 94901, (415) 457-8990.

Circle 621 on inquiry card.

Report on the Warnier-Orr Diagram

A Powerful Structured Tool: Warnier-Orr Diagram is a report providing a strong introduction to the Warnier-Orr diagram. The report includes an overview of system and program design and documentation tools; the need for proper logical tools; how to read a Warnier-Orr diagram; benefits of the diagram; the use of the diagram to develop the mini-specs of structured analysis and to document existing systems; and more. The report includes an annotated bibliography containing 20 entries, a capsule description of a software package to automate the diagram, and 5 illustrations. The Warnier-Orr report is available for $12 (prepaid) from Shetal Enterprises, Dept 2, 1787 B W Touhy, Chicago IL 60626.

Circle 622 on inquiry card.



What's New?

SOFTWARE

Word Processing for the UCSD Pascal Operating System

Renaissance Systems Inc, 11760 Sorrento Valley Rd, Suite M, San Diego CA 92121, has announced two software packages for the UCSD Pascal operating system. PROFF is a program to format and print text files. The PROFF package features adjustable margins; filling, centering, and adjusting; automatic pagination; text underscoring and printing. An "include" command allows reading from files other than the original input file.

The FORML package aids the user in document generation. Multiple copies of a form letter, each addressed to a different individual, can be produced. FORML requires a PROFF source file to perform textual substitution, then it calls PROFF to produce the modified copy of the document. The packages currently support output to a Diablo Hytype II printer, a disk file, the system console, or the system printer. The packages are available in machine-readable form on an 8-inch soft-sectored, single- or double-density floppy disk. Manuals are included with the package or purchased separately for $25. The PROFF package costs $425 and the PROFF and FORML package is $500.

Circle 623 on inquiry card.

Space Shuttle Landing Simulator for the Apple II

Modeled after the National Aeronautics and Space Administration (NASA) Shuttle Mission Simulator in Houston, Texas, this program is a real flight simulator (except for roll motion) with a visual display of the sky and ground. High-resolution color graphics show the shuttle's forward view using animation, projective geometry, and machine language to depict the runway, sky, ground, and distant scenery. Flight data, messages, and warnings are printed on the screen. Functional features are angle of attack control, speed brakes, full stall capability, landing gear, wheel brakes, eject, variable pitch rate control, and more. Runway stripes on rollout give a visual indication of motion. The program requires 48 K bytes of memory. Version A is for Applesoft read-only memory (ROM) and version B for Applesoft programmable memory. The price is $17 for the cassette and $21 for the floppy disk. It is available from Harvey's Space Ship Repair, POB 3478, University Park, Las Cruces NM 88003, (505) 522-1482 (evenings).

Circle 624 on inquiry card.

Keyboard Expandor

This hardware and software modification transforms Apple II microcomputers into complete uppercase and lowercase systems. Cap and shift locks are included; all Apple characters and monitor editing functions are maintained. Software is transparent to the user and compatible with the Apple disk operating system. Uppercase and lowercase can be used in text files, in PRINT and REM statements within BASIC programs, in disk operating system file names, and in immediate mode. The software runs in 250 bytes of memory. It costs $20 and is available from C and H Micro, POB 249, Clifton Park NY 12065.

Circle 628 on inquiry card.

Software for Music Board on CP/M-Compatible Disk

Software support for the Newtech Model 6 music board is available on CP/M-compatible disks. The MV80 Multivoice Music Interpreter allows the user to enter four-voice music in a simple notation. The waveforms for each voice can be individually controlled to create the impression of an instrumental quartet. MV80 requires CBASIC2 and a 40 K-byte or larger 8080, Z80, or 8085 CP/M system. MV80 is available on 8-inch floppy disks for $29.95 including a manual. Contact Newtech Computer Systems Inc, 230 Clinton St, Brooklyn NY 11201.

Circle 625 on inquiry card.

Atari and Texas Instruments Software

Image Computer Products Inc, 615 Academy Dr, Northbrook IL 60062, has introduced a series of programs for the Atari 400 and 800 series and the Texas Instruments 99/4 microcomputers. The programs include Baseball, Wall Street Challenge, Mind Master, Strategy Pack, Skill Builder, and Tournament Brick Bat. There are two copies of each program, which arrive on cassette. Some of the simulation games allow users to save the program on tape in the middle of a game, so that play can be resumed later. The prices for the programs are $19.95 and $29.95.

Circle 626 on inquiry card.

68' FORTH for 6809

68' FORTH is a 6809 implementation of the FORTH language, which is a combination operating system, interpreter, and compiler. It is well suited for situations where it is necessary to be able to quickly test and modify routines or data, especially in the development of algorithms, graphics, data collection and analysis, and instrument control. 68' FORTH consists of full FORTH Interest Group standard vocabulary to 31 characters, 16- and 32-bit integer mathematics, compiler error checking, and a source text editor. The system is supplied with additional vocabulary to simulate disk in memory, to use the disk for virtual memory, to interface with FLEX 9.0 text files, and to perform standard FORTH disk-block read and write. It is supplied on 5-inch floppy disks configured for SwTPC MF-68 systems. The minimum memory requirement is 8 K bytes for FLEX plus 12 K bytes of programmable memory. The disk plus documentation is $39.95 from Talbot Microsystems, 2433 Dorrington St, Houston TX 77030.

Circle 627 on inquiry card.

Four-Part Music System for PET

A B Computers, 115 E Stump Rd, Montgomeryville PA 18936, has announced a system that enables PET users to create and play musical compositions of up to four parts. The KL-4M board includes an 8-bit digital-to-analog (D/A) converter, a low-pass filter, and an audio amplifier. No additional hardware other than a speaker is required. Connection is made via the PET parallel and cassette ports. The KL-4M is compatible with any of the four-part music monitors. The Visible Music Monitor is written in 6502 machine language and displays the musical staff and notes for all four voices on the PET screen. It includes edit capabilities, successive piece loading without intervention, user-definable keyboard, tempo flexibility, transpose capability, and waveform modification capability. Music can be played with or without note display. The entire system is $59.90. The KL-4M board is $34.90 and the Visible Music Monitor is $29.90.

Circle 629 on inquiry card.

What's New?

SOFTWARE

I/OS Disk Operating System for Microcomputers

InfoSoft Systems Inc has introduced its I/OS disk operating system for 8080, 8085, and Z80 disk-based systems. The system is designed for use with hard and floppy disks and has a file capacity exceeding 268 megabytes. It features printer spooling, supports up to 15 disk units, includes a symbolic debugger, text editor, directory status, disk-copy and file-transfer programs, disk and memory diagnostics, and a printout formatting facility.

I/OS Version 3.0 is compatible with the CDOS 02.00 from Cromemco Inc. I/OS is also compatible with CP/M versions 2.0 and earlier. The price of the package is $150 plus a dealer configuration fee. Contact InfoSoft Systems Inc, 25 Sylvan Rd S, Westport CT 06880.

Circle 630 on inquiry card.

Home Improvements Program for the Imagination Machine

APF Electronics Inc, 444 Madison Ave, New York NY 10022, (212) 758-7550, has announced the Space, Size, and Surface program for its personal computer, The Imagination Machine. The program assists homeowners with home improvements involving maintenance, covering surfaces, and materials required. It calcuates the necessary materials for lawn projects, wall papering, painting, panelling, tiling, and more. The program asks for dimensions and areas to be covered or left uncovered, and then tabulates the amount of materials required to complete the job. The program also compares the costs of different products and computes various percentage margins to allow for extra materials due to patterns and fittings around doors and windows. The price for Space, Size, and Surface Guide program is between $19.95 and $29.95, depending on the format.

Circle 631 on inquiry card.

Educational Programs for the PET

This series of documented programs will run in 8 K bytes of programmable memory and requires no peripherals. One series is entitled "Mathematical Enrichment." Programs such as "Symmetry" and "Third-Dimension" suit themselves to planned curriculum or experimentation. A second series features cooperative games for various ages; many are based on the ideas of Jim Deacove of Family Pastimes. Prices range from $10 to $20 per documented cassette. For complete information, contact Go:Forth Microcomputing, 329-22 St E, Prince Albert, Saskatchewan, S6V 1N3 CANADA.

Circle 632 on inquiry card.

Lifeboat Puts CP/M on Altair Disk

The Lifeboat implementation of the CP/M operating system on the Altair and MITS 3202 series of floppy-disk systems takes advantage of the 300 K bytes of memory capacity per disk and the error-free characteristics of the equipment. No changes of any kind are required. With the use of CP/M on the Altair disk, users will have access to the broad range of systems and applications software available. Languages such as C, COBOL, FORTRAN, Pascal, and BASIC are available, as are applications from word processing to accounting. The price for the CP/M system is $145. Contact Lifeboat Associates, 2248 Broadway, New York NY 10024.

Circle 633 on inquiry card.

North Star BASIC SCAN Command

Scan is a machine-language utility program that can be added to North Star BASIC. It allows the user to scan a BASIC line from a single character or variable to complete sentences or key words. The SCAN command operates like LIST except that it lists only those lines that contain the item being scanned for. In the debug mode, it will find all references to any line number such as in GOSUB or GOTO statements. Scan works with single-, double-, or quad-density versions of North Star BASIC. It is available for $27.50 from Electronic Technicians Software Services, 1072 Casitas Pass Rd, Carpinteria CA 93013, (805) 684-6049.

Circle 634 on inquiry card.

What's New?

PUBLICATIONS

UCSD Pascal Newsletter

This newsletter is addressed to those using UCSD Pascal on LSI-11 computers. The first issue contains a detailed article on the situation regarding UCSD and Softech and the licensing problems. It also includes a precise report on the different versions of UCSD Pascal and the anomalies that exist in versions. The publisher is using 8-inch floppy-disk drives with his system and includes articles on the use of the drives and text formatting with the system. There are items of interest concerning new products for the system and letters from users. To get on the mailing list, send $2 to Jim McCord, 330 Vereda Leyenda, Goleta CA 93017.

Circle 635 on inquiry card.

Dataguide

Dataguide is a 500-page purchasing guide to original equipment manufacturers computer hardware, software, supplies, and accessories. It is published in the spring and fall; the subscription rate is $38 per year. *Dataguide* features a manufacturers directory and a product directory. The manufacturers directory contains over 1500 listings of companies with detailed information on each company. The product directory lists nearly 6000 companies organized under categories which include computers and microprocessors, memory systems, disk drives, tape drives, video displays, printers, and plotters, and more.

Subscription order forms may be obtained by contacting Sentry Publishing Co, 5 Kane Industrial Dr, Hudson MA 01749, (617) 562-9308.

Circle 638 on inquiry card.

Computer Careers Magazine

Computer Careers Magazine is dedicated to the computer job market. The audience is made up of systems analysts, programmers, data processors, and technicians. The magazine contains news and information directed to the computer professional, with an emphasis on career development. Feature articles in this twice monthly magazine cover career goals, communicating more effectively, preparing resumes, and choosing the right company. Other areas covered are company profiles, supportive editorials, and classifieds. Contact *Computer Careers Magazine*, 3901 MacArthur Blvd, Newport Beach CA 92660.

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Catalogs for Printers and Punched Paper-Tape Readers

Design literature and catalogs for printers and punched paper-tape readers are now available. Printers are numeric and limited-alphanumerical and are largely used for data logging. The readers read punched paper-tape prepared to American National Standards Institute (ANSI) standards for levels five to eight at up to 150 characters per second (cps) asynchronously, and are used for computer entry, numerical control, data transmission, and programmable read-only memory (PROM) programmers. For more information, contact Addmaster Corp, 416 Junipero Serra Dr, San Gabriel CA 91776, (213) 285-1121

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Circle 240 on inquiry card.

America's Largest Mail-Order Computer Store

HOBBYWORLD® ELECTRONICS, INC.

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BBB MEMBER

ATARI® Home Video System

The nation's best selling home video entertainment center is here! Currently supports a library of 23 video game cartridges with over 1300 variations and options. Comes with interchangeable joystick and paddle controllers, special circuits to protect home TV, realistic sound effects and produces crisp, bright colors on your TV screen. Also includes ATARI's "Combat" game with 108 variations and options.

CAT NO.	DESCRIPTION	WT.	PRICE
2375	ATARI Video Computer System	8 lb.	$188.95
2206	Driving Controller-Pair	2 lb.	$ 20.95
2207	Paddle Controller-Pair	2 lb.	$ 20.95
2208	Joystick Controller-Pair	2 lb.	$ 20.95

ATARI Game Cartridges

CAT NO.	DESCRIPTION	WT.	PRICE
2376	Starship	6 oz.	$16.75
2377	Black Jack	6 oz.	$16.75
2378	Space War	6 oz.	$16.75
2379	Surround	6 oz.	$16.75
2380	Slot Machine	6 oz.	$16.75
2381	Outlaw	6 oz.	$18.95
2382	Slot Racer	6 oz.	$18.95
2383	Video Olympics	6 oz.	$18.95
2384	Breakout	6 oz.	$18.95
2385	Canyon Bomber	6 oz.	$20.95
2386	Street Racer	6 oz.	$20.95
2387	Homerun	6 oz.	$20.95
2388	Basketball	6 oz.	$20.95
2389	Football	6 oz.	$20.95
2390	Bowling	6 oz.	$20.95
2391	Skydiver	6 oz.	$20.95
2392	Fun With Numbers	6 oz.	$20.95
2393	Brain Game	6 oz.	$20.95
2394	Superman	6 oz.	$28.50
2395	Casino	6 oz.	$28.50
2396	Backgammon	6 oz.	$47.25
2397	Video Chess	6 oz.	$47.25
2500	Space Invaders	6 oz.	$29.95

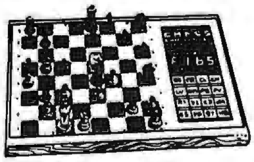
NOTE: Not for use with ATARI Programmable Computers

Backgammon Challenger $115.50

You will be challenged and intrigued by this game. Uses all strategies of the game, including a running game, hit and run, blocking and bear off games. YOU handle the dice! Choose offense or defense. Computer responses vary every game.
Weight 3 lbs. Cat No. 2411

Chess Challenger "7" / Chess "VOICE" Challenger

If you're into chess you will love Chess Challenger! 7 levels of play. "Mate in Two" and "Chess by Mail". Like to have your opponent call out the moves? Try "Voice" Chess Challenger. 96,000 Bits of Read Only Memory, and over 8,000 bits of Random Access Memory. Can be used by the blind as the game will audibly call every move, capture, and repeat board position.



Cat No. 2399	Chess Challenger "7"	Wt. 3 lbs.	117.95
Cat No. 2398	Chess Voice Challenger	Wt. 4 lbs.	353.95

STAR TREK III

One of the most advanced Star Trek games ever. Locate the 5 Class M Planets, battle Klingons, but watch out for black holes and pulsars. This version is 3 dimensional, not flat like other versions. Watch the Enterprise phasers hit and explode the Klingons! Extensive use of graphics throughout. At the end, return to Star Fleet command, where the data in the ships computer evaluates and rates your performance. Takes about 2 hours to play a game.
Cat No. 1041 TRS-80 level II/16K $15.75

16K Memory Add-On Kit $65.00

Everything needed to upgrade your TRS-80, Apple or Exidy! An additional 16K includes illustrated instructions, RAMS, and preprogrammed jumpers. No Special tools required. Wt. 4 oz.

CAT NO.	DESCRIPTION
1156	TRS-80 Keyboard Unit
1156-A	TRS-80 Exp. Interface (prior to 4/1/79)
1156-B	TRS-80 Exp. Interface (after 4/1/79)
1156-C	for APPLE II
1156-D	for EXIDY

SARGON II

Hayden

The champ of champs! Surpasses Microchess, and even Sargon I! Offers complex moves, 7 levels of play, activity indicator, a special "hint" mode, plus more! The best chess program ever!

Cat No. 2082	TRS-80	$31.50
Cat No. 2083	Apple II	$31.50

DISKETTE DRIVE HEAD CLEANING KIT

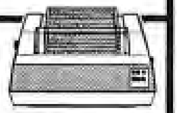
Diskette drive heads, like your 8 track car stereo cassette heads, need periodic maintenance to assure efficient and error-free operation. Unlike other peripheral devices, the read/write head(s) on diskette drives are extremely difficult to clean without partially disassembling the drive. The unique concept of the diskette head cleaning kit allows the user to clean the drive heads without disassembly in just minutes. Available for 8" or 5¼", both single and double sided disk drives. Kit contains 2 cleaning diskettes, a 4 oz. bottle of CS-85 cleaning solution and easy-pour dispenser. Weight 12 oz.

Cat No.	Description	Price
2499	8" Disk Drive Cleaning Kit	$30.75
2534	5¼" Disk Drive Cleaning Kit	$30.75

NOVATION "CAT" ACOUSTIC MODEM

The FIRST compact modem designed for the small computer user. Transmits data over standard telephone lines . . Exchange data or programs with other systems. Data transfer rate up to 30 char/sec. Complete and ready to use. Requires 110 VAC. 60 Hz.
Cat No. 1480 Weight 3 lbs. Price: $189.00

EMAKO 22 MICROPRINTER



The EMAKO 22 microprinter is a dependable, low cost, addition for your personal computer system. It features a 9X7 dot-matrix character format, bi-directional printing at 125 CPS and sprocket feed paper mechanism. Line length is selectable at 40, 80, or 132 characters per line. Forms may be loaded either from the bottom or the rear. Available with parallel or asynchronous serial interfacing.

Cat No.	Description	Weight	Price
2455	Parallel Interface Model	22 lb.	$834.75
2456	RS232-C Serial Model	22 lb.	$894.00

VERBATIM 5¼" DISKETTES

10 per box

CAT NO.	TYPE	DESCRIPTION	PRICE
1147	525-01	soft sector, TRS-80, Etc.	$33.00
1148	525-10	10 hole, hard, Apple, North star	$33.00
1149	525-16	16 hole, hard, micropolis	$33.00
2330	577-01	soft sector certified	$49.95
2331	577-10	10 hole, hard, certified	$49.95
2332	577-16	16 hole, hard, certified	$49.95

Fuller Electronics TRS-80 LPRINT/ LLIST PLUG

Many users are faced with the problem of running programs with LPRINT or LLIST, but they do not want a print out. In this case, all LPRINTS have to be removed from the program before it will run, and this takes time and ties up your keyboard. But there is an alternative! Simply connect the TRS-80 LPRINT/LLIST plug to your line printer port, and the program will run just as if there was a printer connected to your machine. Easy installation and detailed instructions. Wt. 2 oz.
Cat No. 2480 **$11.95**

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Page after page of exciting products. Computerized toys and games, personal computers, disk drives, integrated circuits, semi conductors. Add new dimension to your Apple, Atari, TRS-80, etc. with our special application boards and comprehensive software library. Hundreds of products available at terrific Hobbyworld prices. Circle our reader service number or write/phone for your free illustrated flyer today.

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Pay by check, Mastercharge, Visa, or C.O.D. Charge card orders please include expiration date. Payment in U.S. dollars only. Order by phone, mail or at our retail store. MINIMUM ORDER $10.00. Please include phone number and magazine issue you are ordering from. Prices valid thru last day of cover date. SHIPPING: USA: Add $2.00 for first 2 lbs., 35¢ each addt'l lb. for ground. For AIR add $3.00 first 2 lbs., 75¢ each addt'l lb. FOREIGN: surface: $3.00 first 2 lbs., 60¢ each addt'l lb. AIR: $11.00 first 2 lbs., $5.00 each addt'l lb. COOs: add $1.25 addt'l. Not responsible for typographical errors. Some items subject to prior sale or quantity limitations. 120 day guaranteed satisfaction. Exception: partially assembled kits.

MATCHLESS MS-80 TRS-80 MINI DISK DRIVE

Plugs into the expansion interface. Complete factory tested drive includes installation instructions and software listing to access 3 times faster than Radio Shack drives. 40 tracks instead of 35. Existing 35 track software completely compatable.

Cat No.	Description	Weight	Price
1375	MS-80 Disk Drive	8 lbs.	$464.25
2964	2 Drive Cable	8 oz.	$ 25.75
1396	4 Drive Cable	8 oz.	$ 41.95
1938	Accessing Software, tracks 36-40	4 oz.	$ 10.50
1485 D	MS-80 MPI 51 Manual	2 oz.	$ 1.75
1147	Verbatim Diskettes, (box of 10)	8 oz.	$ 33.00

CCS 7811B ARITHMETIC PROCESSOR

Assembled & tested, adds advanced arithmetic power to your Apple II. AMD AM 9511 based, 16 and 32 bit fixed point, 32 bit floating point operation. Float to fixed and fixed to float conversions. Trig and inverse functions, square roots, logs, exponentiation. Interrupt daisy chain, DMA daisy chain, and much more. Weight 2 lbs. Cat No. 1635 **$419.95**

19511 Business Center Drive Dept. B6 Northridge, Ca. 91324

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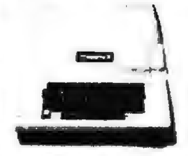
Circle 242 on inquiry card.

Apple II Or APPLE II PLUS

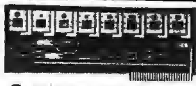


16K $975.95, Extra 16K E.S. RAM installed $74.95, extra 32K E.S. RAM installed $148.95.

PET COMPUTER

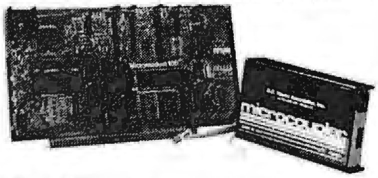
With 16K & monitor - $795. Dual Disk Drive - $10 95

PARALLEL TRIAC OUTPUT BOARD FOR APPLE II



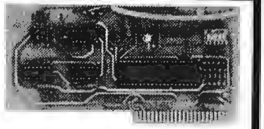
This board has 8 triacs capable of switching 110 volt 6 amp loads (660 watts per channel) or a total of 5280 watts. Board only $15.00 Part No. 210, with parts $119.95 Part No. 210A.

D.C. HAYES MICROMODEM



Fully S-100 bus compatible including 16-bit machines and 4 MHz processors. • Two software selectable Baud rates—300 Baud and a jumper selectable speed from 45 to 300 Baud. (110 standard). Supports originate and answer modes. • Direct-connect Microcoupler. This FCC-registered device provides direct access into your local telephone system, with none of the losses or distortions associated with acoustic couplers and without a telephone company supplied data access arrangement. • Auto-Answer/Auto-Call. The MICROMODEM 100 can automatically answer the phone and receive input; it can also dial a number automatically. • Automatic Reset and Disconnect. • Software compatible with the D.C. Hayes Associates 80-103A Data Communications Adapter. Micromodem-DCHA32625—$379.95

APPLE II PLUS SERIAL I/O INTERFACE

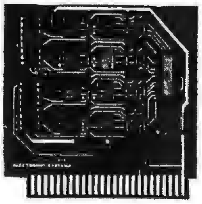


Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

APPLE II HOBBY/ PROTOTYPING CARD

Part No. 7907 $14.95

OPTO-ISOLATED PARALLEL INPUT BOARD FOR APPLE II

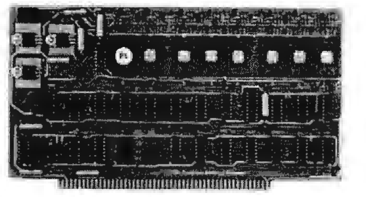


There are 8 inputs that can be driven from TTL logic or any 5 volt source. The circuit board can be plugged into any of the 8 sockets of your Apple II. It has a 16 pin socket for standard dip ribbon cable connection. Board only $15.00. Part No. 120, with parts $69.95. Part No. 120A.

REAL TIME 100,000 DAY CLOCK

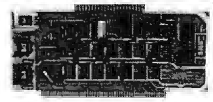
MT. HARDWARE Double the utility of your S-100 bus computer with a real-time clock that keeps time in 100µS increments for over 273 years. Program events for the entire period with real time interrupts...without derailing the system. Maintain a log of computer usage, time and date transaction printouts, call up lists...virtually any activity where time is a factor. On-board battery backup. MHPX004—$249.95

8K EPROM PICEON



• Programs 2708's address relocation of each 4K of memory to any 4K boundary • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.

TIDMA

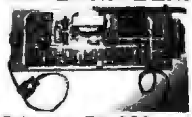


Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate • S-100 bus compatible • Board only $35.00 Part No. 112, with parts $110.00 Part No. 112A.

SYSTEM MONITOR

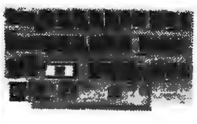
8080, 8085, or Z-80 System monitor for use with the TIDMA board. There is no need for the front panel. Complete with documentation $12.95.

SUPER MODEM



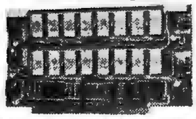
Orignate, RS-232 and 20mA compatable, Full duplex, and half duplex, direct connect or acoustic coupled, on board power supply, carrier detect light, DB25 plug, 300 BAUD, Type 103 compatable frequencies, Bare board Part No. 2000, $19.95, Kit Part No. 2000A, $99.95.

VIDEO TERMINAL



16 lines, 64 columns • Upper and lower case • 5x7 dot matrix • Serial RS-232 in and out with TTL parallel keyboard input • On board baud rate generator 75, 110, 150, 300, 600, & 1200 jumper selectable • Memory 1024 characters (7-21L02) • Video processor chip SFF96364 by Neculonic • Control characters (CR, LF, →, ←, ↑, ↓, non destructive cursor, CS, home, CL • White characters on black background or vice-versa • With the addition of a keyboard, video monitor or TV set with TV interface (part no. 107A) and power supply this is a complete stand alone terminal • also S-100 compatible • requires +16, & −16 VDC at 100mA, and 8VDC at 1A. Part No. 1000A $199.95 kit.

16K EPROM



Uses 2708 EPROMS, memory speed selection provided, addressable anywhere in 65K of memory, can be shadowed in 4K increments. Board only $24.95 part no. 7902, with parts less EPROMs $49.95 part no. 7902A.

WAMECO PRODUCTS

With ELECTRONIC SYSTEMS parts

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remex 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not included). PCBD $42.95

FPB-1 Front Panel. (Finally) IMSAI size hex displays. Byte or instruction single step. PCBD $42.95

MEM-1A 8Kx8 fully buffered, S-100, uses 2102 type RAMS. PCBD .... $24.95, $168 Kit

QMB-12 MOTHER BOARD, 13 slot, terminated, S-100 board only .... $34.95, $89.95 Kit

CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD .... $25.95, $89.95 Kit

RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCBD .... $25.95, $60.95 Kit

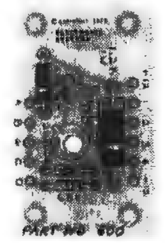
EPM-1 1702A 4K EPROM card PCBD .... $25.95, $49.95 with parts less EPROMS

EPM-2 2708/2716 16K/32K EPROM card PCBD .... $24.95, $49.95 with parts less EPROMS

QMB-9 MOTHER BOARD. Short Version of QMB-12. 9 Slots PCBD .... $30.95, $67.95 Kit

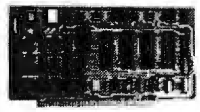
MEM-2 16Kx8 Fully Buffered 2114 Board PCBD .... $25.95, $269.95 Kit

RS-232/TTY INTERFACE



This board has two active circuits, one converts RS-232 to 20 mA, the other converts 20 mA to RS-232. Requires +12 and −12 volts. $9.95 Part No. 600A Kit.

SERIAL I/O



Four Serial I/O RS-232 ports. S-100 Bus, Software or jumper selectable baud rate (110, 300, 600, 1200, 2400, 4800, 9600, 19.2K), on board Xtal baud rate generator, Addressing, switch selectable, Parity or no parity (odd or even) switch selectable, 1 or 2 stop bits, 5 to 8 bits/character. Board only $29.95, Part No. 7908. With parts (kit) $199.95, Part No. 7908A.

S-100 BUS ACTIVE TERMINATOR

Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A

To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U.S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U.S. dollars. Dealer inquiries invited. 24 hour order line (408) 448-0800

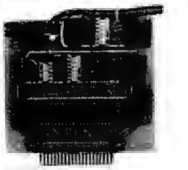
Send for FREE Catalog . . . a big self-addressed envelope with 41¢ postage gets it fastest!

ELECTRONIC SYSTEMS Dept. B P. O. Box 21638, San Jose, CA USA 95151

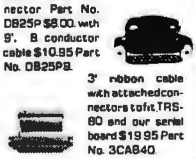
Circle 242 on inquiry card.

TRS-80 SERIAL I/O

• Can input into basic • Can use LLIST and LPRINT to output, or output continuously • RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line • Requires +5, -12 VDC • Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010 C. No connectors provided, see below.



EIA/RS-232 connector Part No. DB25P $8.00 with 9', 8 conductor cable $10.95 Part No. DB25P8.



3' ribbon cable with attached connectors to fit TRS-80 and our serial board $19.95 Part No. 3CAB40.

GAME PADDLES & SOUND

Includes: 2 game paddles, interface, software, speaker, power supply, full documentation including: schematics, theory of operation, and user guide; plus 2 games on cassette (Pong and Starship War). $79.95 Complete Part No. 7922C

DISKETTES

Box of 10, 5" $29.95, 8" $39.95.
Plastic box, holds 10 diskettes, 5" - $4.50, 8" - $6.50.

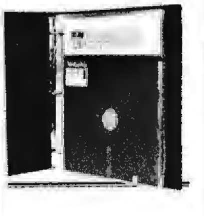
16K RAMS

For the Apple, TRS-80 or Pet $8 each Part No. 4116/2117.

LEEDEX MONITOR

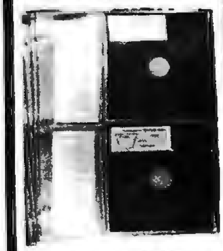
12" Black and White • 12 MHz Bandwidth • Handsome Plastic Case • $139.00

FLOPPY DISK STORAGE BINDER



Three-ring binder comes with ten transparent plastic sleeves which accommodate either twenty, five-inch or ten, eight-inch floppy disks. Binder & 10 holders $14.95 Part No. 8800; Extra holders 95¢ each. Part No. 800.

DISK JACKET™



Holds two 5-1/4 inch diskettes and will fit any standard three ring binder. $9.95/10 Pack.

S-100 INTERFACE

AN S-100 bus Adapter—Motherboard for the TRS-80. Kit, Part No. HUH81 OLXK, $295.95. Assembeled, Part No. HUH81 OLXA, $375.95.

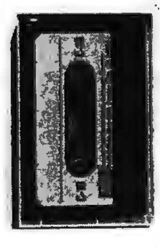
DIGICOM DATA PRODUCTS INC. Series 312 Acoustic Coupler

300 BAUD Originate, Part No. AC3122, $219.95. 300 BAUD Answer, Part No. AC3122, $219.95. 300 BAUD Answer/Originate, Part No. AC3123, $229.95.

TRENDCOM PRINTER

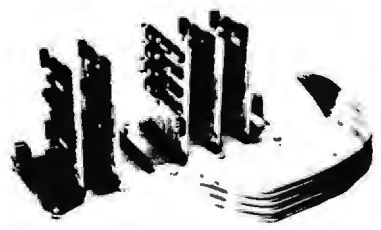
• 40 characters per second • 4-7/16 inch wide thermal paper • Graphics (TRENDCOM 100): 480 sevendot print postions per line. TRENDCOM 100, Part No. TRC0100, $495.95. TRENDCOM 200, Part No. TRC0200, $375.95. **Interface** for TRS-80, Part No. T80A $45.95. For Apple II, Part No. TRCAII, $75.95. For PET, ND. TRCP2, $79.95. For Scoccerer, TRCSR1 $45.95.

DIGITAL CASSETTE



5 min. each side. Box of 10 $9.95. Part No. C-5.

NOW! A FULL SUPPORT SYSTEM FOR TRS-80



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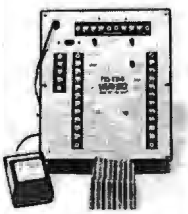

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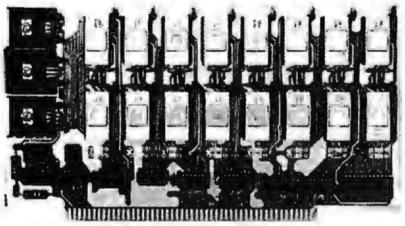

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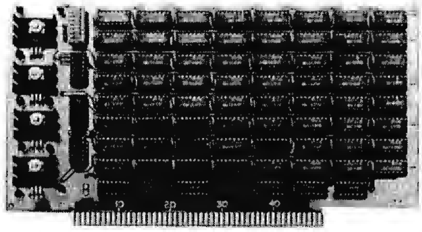

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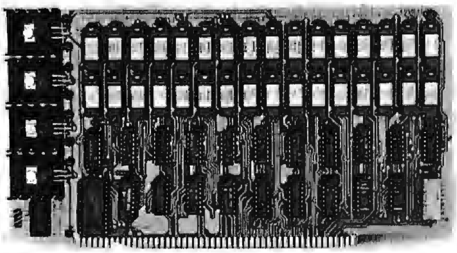

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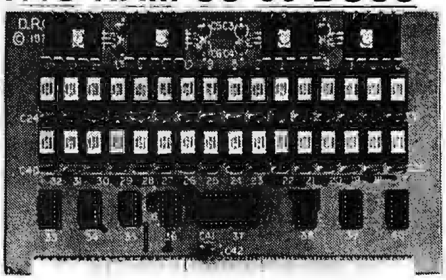

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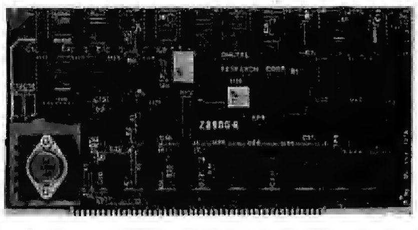

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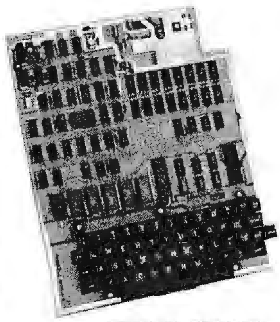

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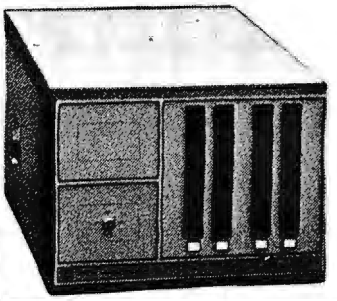

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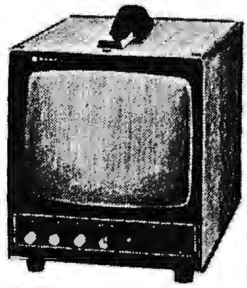

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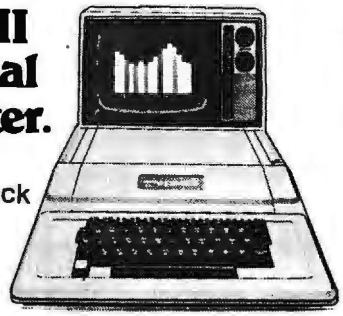

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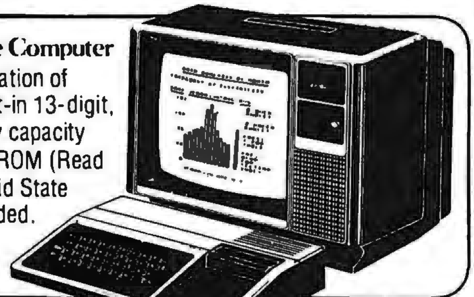

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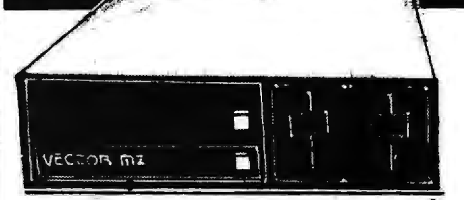

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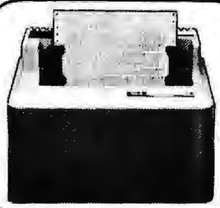

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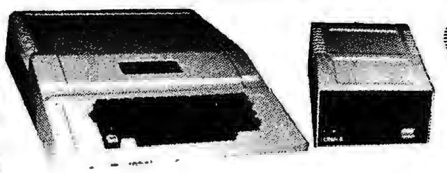

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74LS54	.35	74LS244	2.50
74LS73	.45	74LS251	1.29
74LS74	1.05	74LS257	.90
74LS75	.58	74LS258	1.50
74LS76	.45	74LS259	1.60
74LS86	.45	74LS266	.70
74LS90	.80	74LS279	.70
74LS92	.80	74LS290	.80
74LS93	.80	74LS293	.80
74LS107	.45	74LS295	1.50
74LS109	.45	74LS298	1.50
74LS112	.45	74LS365	.80
74LS113	.45	74LS366	.80
74LS114	.55	74LS367	.80
74LS125	.80	74LS368	.80
74LS126	.80	74LS375	.95
74LS132	.95	74LS377	2.75
74LS139	1.30	74LS386	.60
74LS161	1.19	74LS390	1.95

LINEAR CIRCUITS

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LM301/748 – .25
LM307 – .30
LM308 – .75
LM311 – .75
LM318 – 1.20
LM324 – .95
LM339 – 1.10
LM358 – .70
LM377 – 1.60
LM380 – .95
LM382 – 1.25
LM386 – .85
LM387 – 1.25
LM1800 – 1.75
LM1889 – 1.95
CA3018 – 1.95
CA3080 – .95
CA3086 – .95
DM1800 – 1.85
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LM537 – 2.50
LM553 – 2.50
LM565 – .49
LM566 – .95
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565 – .95
566 – 1.25
567 – 1.10
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703 – .85
709 – .25
710 – .45
711CH – .40
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747 – .50
LM1310 – 2.60
1458 – .50
3900 – .65
8038CC – 3.90
4136 – .95
LF355 – 1.75
NE540L – 2.50
1810PC – 2.20

SCR'S

1.5A	6A	35A	PRV
.45	.60	1.40	100
.70	.80	1.90	200
1.20	1.40	2.60	400
	1.80	3.60	600

TRIACS

PRV	1A	10A	25A
100	.45	.80	1.55
200	.84	1.30	2.10
400	1.30	1.80	3.10
600	2.00	2.75	4.30

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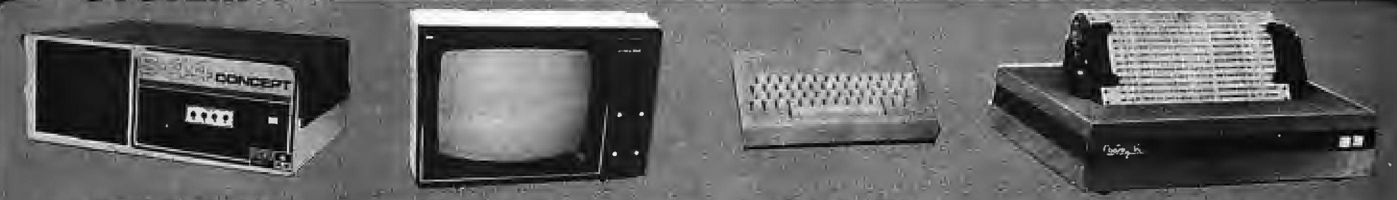


Twin Mini W/32K — Leedex Monitor — Keyboard — Base 2

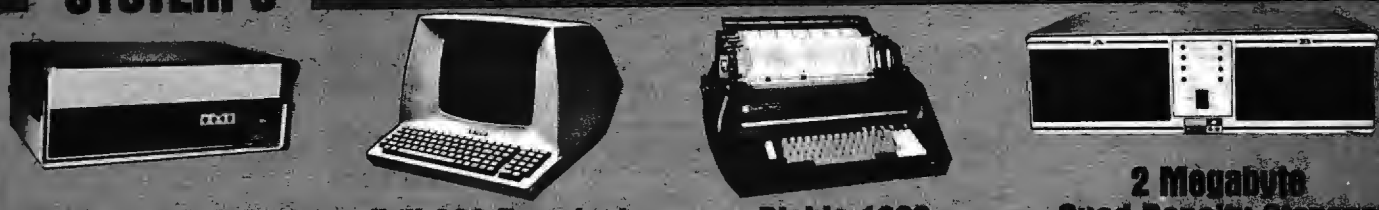
SYSTEM 2

MULTIUSER CAPABLE

32K S-100 Mainframe — T/V 912 Terminal — TI 810† — 1 Megabyte Double Density Storage

SYSTEM 3

MULTIUSER CAPABLE



64K S-100 Mainframe — T/V 920 Terminal — Diablo 1620 — 2 Megabyte Quad Density Storage

SYSTEM 4

MULTIUSER

† (Dealers Only)

Desk Enclosure — 32 Megabyte Disk — AT&T Model 300

Software:

CPM 1.4	$115.00	CBASIC	$115.00	WORDSTAR	$495.00	DATABASE	$150.00
CPM 2.0	$150.00	MBASIC	$300.00	ACCTS. PAYABLE	$699.00	INVENTORY	$440.00
MPM MULTI-USER	$350.00	FORTRAN	$395.00	ACCTS. RECEIVABLE	$699.00	QSORT	$ 95.00
		COBAL	$625.00	GENERAL LEDGER	$899.00	NAD	$ 79.00
		PASCAL	$265.00	SUPERSORT	$225.00	LETTERRIGHT	$180.00

West:
DELTA PRODUCTS
15392 Assembly Lane
Unit A, Huntington Beach
Calif. 92649
Tel: (714) 898-1492

Circle 257 on inquiry card.

DELTA PRODUCTS

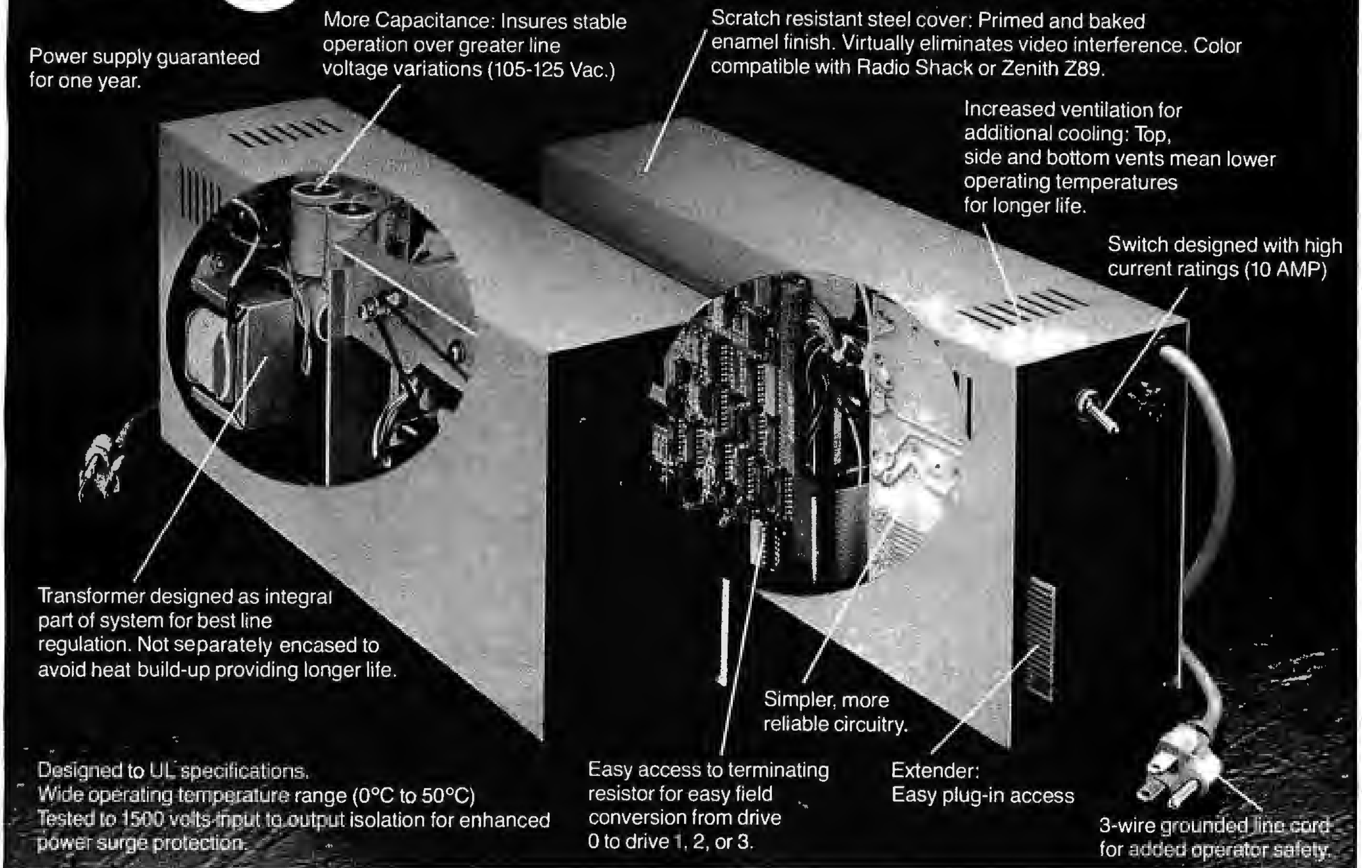
Telex: 182-126 DELTMAR SGHL

East:
DELTA PRODUCTS
1254 South Cedar Road
New Lenox, Illinois 60451
Tel: (815) 485-9072

Circle 258 on inquiry card.

Circle 259 on inquiry card.

Precision Engineered Drives...



With the number of disk drives on the market increasing, more and more people are beginning to ask what's underneath that cover.

The CCI™ series of disk drives have been designed for long life and ease of operation. The features shown above are what set our CCI drives apart from the rest. With a CCI drive you get an integrated professional design!

If you're still not convinced that you get the most for your money with a CCI drive, just ask for our complete specifications sheet. Then, compare our disk drives to anyone else's.

5¼" DRIVES

CCI-100	40 Track (102K Bytes) for TRS-80* Model I	$399.00
CCI-189	40 Track (102K Bytes) for Zenith Z89	$499.00
CCI-200	77 Track (197K Bytes) for TRS-80* Model I	$675.00

8" DRIVES

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All CCI drives are also available for 220 Vac (50Hz) operation.

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NEWDOS Plus for 5¼", 40 and 77 Track Drives—with over 200 modifications and corrections to TRSDOS $110.00

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CP/M for Model II, Altos $250.00

Software by S&M Systems

INSEQ-80™—Indexed Sequential Access Method (**ISAM**) for the TRS-80 Model I.

Four machine language programs that can be called from your BASIC program via USR functions to access records either sequentially or randomly. The INSEQ-80 programs maintain all indexes and chains for you. Includes reorganization utility to consolidate files. $49.95

Professional Business Software using INSEQ-80 for the TRS-80* Model I and Zenith Z89.

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*TRS-80 is a trademark of the Tandy Corporation

Products also available from: Radio Shack, NEC, Centronics, Paper Tiger, TI, Altos, MPI, Zenith, Mattell, ATARI, PET, OKIDATA, Apple, Eaton/LRC.

FRANCHISE AND DEALER (NATIONAL/INTERNATIONAL) INQUIRIES INVITED

Retail Stores: MA: Burlington, Charlestown, Framingham, Hanover **NH:** Manchester **RI:** Providence

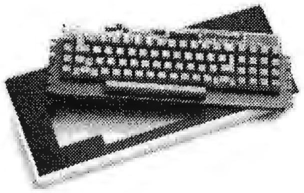
master charge — VISA

Circle 262 on inquiry card.

 Circle 263 on inquiry card.

Keyboard Special 1 !!

CHERRY "PRO" Keyboard $119.00
Streamlined Custom Enclosure 34.95
BOTH only $134.95



Keyboard Special 2 !!

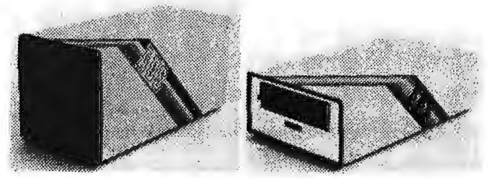
Keytronics 1660 .... $149.00
Hard Plastic enclosure 49.00
BOTH only $152.00

June Bonanza!!

4116 dynamic RAM, 16K
Set of 8, 16K, for Apple, TRS-80, Exidy, Heath & more. 200 Ns., prime parts, at the unheard of $49/8.
Large discounts available for quantity & dealers (500 & up). Offer limited while supply lasts, as these will vanish quickly!!!

Disk Subsystem

Matchmaker Technology
TURNKEY DISK SUBSYSTEMS



APPLE ...... Single density disk controller. Expanded Apple DOS
TRS-80 .... Single or double density. Expansion interface necessary. Space for 48K dynamic RAM on controller card RS232 port
SORCERER .. Full RS-232 Interface. One S-100 slot for memory expansion. Single or double density
All above units come as follows: Complete, assembled and tested, with two 8" floppy disk drives (Apple available in one drive model). Includes all cabling, connectors and documentation in a stunning color coordinated cabinet with power supply. Ready to go, plug in and run!!!

* * *

When ordering specify single or double sided drives

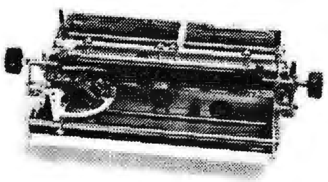
* * *

Software available for above disk add-ons

* * *

TRS-80 & Sorcerer operate on all CP/M compatible software

Daisy Wheel Printers



Qume Sprint 3\45

PRINTER (factory warr.)	$1499.
POWER SUPPLY (Borschert) (Shown mounted on rear of printer)	349.
COMBINATION SPECIAL	1699.
Cases available	200.
S-100 interface card	149.
SPRINT 5/45 RO, RS-232 Complete, assembled, in case, plug-in & print, hence, no muss & no fuss	$2699.
NEC Spinwriter	$2899.

Data Display Monitors

Please call us for particulars

Electrolabs
POB 6721, Stanford, CA 94305
415-321-5601 800-227-8266
Telex: 345567 (Electrolab Pla)
Visa MC Am. Exp.

Software

CP/M 1.4	$ 99
CP/M 2.0	149
OS-1 (incl. 1st yr. update) ..	249
Spellbinder (Exc. secretiarial type word-processor)	350

Peripheral Sale!!

Hiplot Plotter	$875.
Hipad Digitizer	715.
Televideo 912C	760.
Televideo 920C	860.
IDS 440 Paper tiger	899.
SD Expandoram II (A&T, 64K)	560.
Imsai 65K dynamic RAM III	399.
DC Hayes Micromodem 100 ..	399.
Super switcher power for hard disk & more	349.
CII HB 10 MBY	3300.
SA 4008	2799.
C-Basic	99.
Fortran Compiler	100.
C Compiler	600.
Basic compiler	350.

ESAT 200B

BI-LINGUAL 80x24 Communicating Terminal
Scrolling, full cursor, bell, 8x8 matrix, 110-19,200 baud, Dual Front Applications.
Arabic & Hebrew, Multilingual Data Entry Forms Drawing, Music, & Switchyards.
Alone .... $279.
with Cherry Pro keyboard & custom metal case .... $399.

NEW "UNIX-like" Operating System for Z-80

OS-1

OS-1 is truly a breakthrough in the micro world! OS-1 is NOT a "control program for micros" but is, instead a large, professional operating system designed to lower the cost and improve the quality of programming efforts. OS-1 provides a "friendly" human interface for both system programmers and users. Finally, with OS-1, the capability of a Z-80 system is vastly expanded.

OS-1 appears exactly like UNIX to the user, and includes virtual i/o, "set tty" and "login" commands, a shell, a hierarchical "tree" type file structure with 16Mby file size and an unlimited no. of files and devices. OS-1 allows the extremely useful "pipes" and "filters" to be implemented. OS-1 also provides for up to 1024 users and 64 groups and security for users, groups, files and devices. OS-1 occupies 12Kby and comes with a 4Kby "enhanced" cp/m adapter which runs ALL cp/m and most CDOS programs. Source code is supplied with adapter.

OS-1 (Including Debugger, "UNIX-type" editor, Linker-Loader & 1 Yr. update) **$249**

"C" Compiler (Whitesmiths') **$600**

Microsoft Compiler Interface (Interfaces MS Fortran & Cobal compilers directly to OS-1. This allows compiler output to "Command" OS-1 Routines. The Electrolabs' Software Group considers this interface indispensable. Contains over 100 separate routines) **$49**

Manuals:
(price applies to OS-1 purchase)

Introduction to OS-1 (60pg)	**$15**
OS-1 Users' Guide (150pg)	**$35**
Sys-Gen Manual for OS-1 (40pg)	**$10**
SET ------	**$45**

Circle 263 on inquiry card.

California Digital

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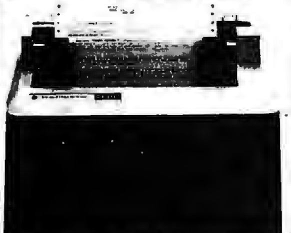
FREE Paper Tiger

With Purchase of The INTEGRAL DATA 440

Your Choice, $200 Value



1) Graphics Option Package
2) Interface for APPLE II
3) TRS-80 Printer Interface

California Digital has resently researched the complete low cost printer market. It is our opinion that the IDS440 Paper Tiger is, without doubt, the most versatile and offers the best value of any printer costing under $1,000.

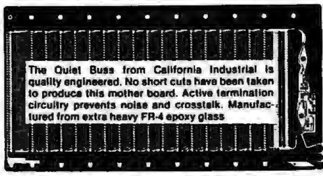
This quality dot matrix printer incorporates such features as software selectable character size to allow print densities upto 132 characters per line. Full forms handling capabilities and tractor feed mechansim adjustable to 9.5". The Paper Tiger is engineered to accept either parallel or RS232 serial ASCII. 110/220V.50/60Hz.

***** $995.00 plus shipping *****

S-100 Mother Board

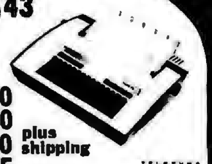
Quiet Buss

$29.95
8803-18
18 slot
IMSAI



The Quiet Buss from California Industrial is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy FR-4 epoxy glass.

TELETYPE® MODEL 43



4320 KEYBOARD

TTL	AAA	$1050
RS232	AAK	1150
Friction ...	AAE	1100
103 Modem	AAB	1575

plus shipping

$149 MOTOROLA

New factory surplus. M3000/3211 Motorola CRT monitors.

20 MHz bandwidth Electronics terminate into single ten pin (.156") edge connector. Requires DC power supply

FREE PLASTIC LIBRARY CASE

with purchase of each box of .... Memorex mini-diskettes. $5 value.

$24.95 BOX of 10 DISKETTES

HARD TO FIND 74LS

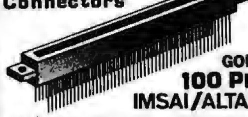
Not cheap....But available

examples

00	.39	123	1.29	161	1.79
02	.49	125	.89	163	2.19
04	.39	138	1.79	174	1.49
08	.39	139	1.39	175	1.09
74	1.49	148	....	240	1.95
75	.89	151	.89	244	1.95
86	.95	153	.89	245	....
90	.95	157	.89	367	.95

Minimum purchase 100 each

Edge Connectors



GOLD 100 PIN IMSAI/ALTAIR

Imsai solder.125x.250	$2.95	3/$7.50
Imsai w/w.125centers	$4.95	3/$13.00
Altair soldertail.140row	$5.95	3/$15.00
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25/50 solder tab .156"	$1.09	3/$2.00
36/72 wide post w/w.156	$1.95	3/$5.00

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Apple II standard 16K	$988
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Atari 400	450
Atari 800	850
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Northstar (Quad 32k Horizon)	2995
Vector MZ	
Compucolor II Model 3	1395
Rockwell Aim 65(1K)	375

CRT TERMINALS

ADDS Regent 25 (ten key pad)	850
ADDS Regent 40	1105
ADDS Regent 60	1495
Hazeltine 1420	850
Hazeltine 1500	995

MONITORS

Sanyo 9" black & white monitor	179
Leedex Video 100 12"	125
Leedex Video 100-80 12"	179

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IDS440G Tiger with Graphics	$995
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Printronix P-600	
Teletype Model 43 (RS232)	1180
Teletype Model 40(132 col.)	
NEC Spinwriter 5510 R/O	2595
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Novation Cat Acoustic	169

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Lobo hard drive for TRS80	3995
Lobo 400-1 5 1/4" for TRS80	388
Vista V-80 for TRS80 (40trk)	388
Corvus Systems hard drive	

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Apple drive without controller	495
Apple Parallel Interface	179
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Godbout Rack Enclosure	$289
Godbout Desk Top Enclosure	329
Electronic Controls ECT 100F	250
Cal. Digital 18 slot motherbd.	30

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Godbout Econoram Products	
Mullin TB-2 Extend. &Logic	49
Artec WW100 WireWrap Proto	25
SD 64K Expandoram Memory	

16 BIT S-100 BOARDS

Cal. Digital CAL-86	990
Tecmar 8086	650
Seattle Computers 8086	850
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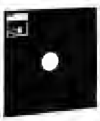
Cherry Pro ASCII Keybd.	129
Maxiswitch HEX Keyboard	49
UV Eraser II-E	65
Super Mod II RF Modulator	30

Scotch Data Products

Authorized Distributor



		10 Pak	50+
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740/2	Double side soft	65.00	6.00
741-0	Double density	53.00	4.90
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740-32	8" Hard sector	39.00	3.50
744-(0)(10)(16)	5 1/4"mini	39.00	3.50
Library case for any above:		Add $3.00	
834 A	Data Cassette	5.50	
DC100	Mini Cartridge	16.00	
DC 300	Data Cartridge	20.00	
920( )	Disk Cartridge	89.30	

Shugart Associates

SA800-R Floppy Disk Drive

The most cost effective way to store data processing information, when random recall is a prime factor. The SA800 is fully compatible with the IBM 3740 format. Write protect circuitry, low maintenance & Shugart quality.

$449.50

XEROX 800 WORD PROCESSING KEYBOARD ASCII ENCODED

This 77key word processing keyboard was manufactured by Microswitch for use in the Xerox 800 word processing system. The keyboard outputs a seven bit ASCII code along with an eighth bit that allows most keys to shift and double function as special characters. Extra large "Tab & Return" keys are designed into the layout of the keyboard to emulate the IBM Selectric. 17 illuminated keys serve for special word processing codes. The keyboard is equipped with two thumbwheel switches for defining line width.

Original Xerox acquisition over $400.00 California Digital USED price only $49.00 Excellent cond. Documentation included.

MEMORY

TRS-80 / APPLE II $59

16k memory (8) 4116's

Installation is simple. Anyone who has ever changed a spark plug should be able to up-grade his microcomputer.

How can California Digital offer these memory up-grade sets at 25% below our competition? Simple, we buy in volume, wholesale to dealers and sell the balance directly to owners of personal microsystems. These 16K dynamic memory circuits are factory prime and unconditionally guaranteed for one full year. NOW, before you change your mind, pick up the telephone and order your up-grade memory from California Digital. Add $3 for TRS80 jumpers.

STATIC	1-31	32-99	100-5C	-999	1K+
21L02 450nS.	1.19	.99	.95	.90	.85
21L02 250nS.	1.49	1.39	1.25	*	*
2114 1Kx4 450	5.95	5.50	5.25	4.75	4.50
2114 1Kx4 300	8.95	8.50	8.00	*	*
4044 4Kx1 450	5.95	5.50	5.25	*	*
4044 4Kx1 250	9.95	9.50	9.00	*	*
4045 1Kx4 450	8.95	8.50	8.00	*	*
4045 1Kx4 250	9.95	9.50	9.00	*	*
5257 low pow.	5.95	5.50	5.00	4.80	4.60

SPECIAL CIRCUITS

Z80A 4MHz.	24.95	AY5-1013A UART	4.95
8080A CPU	9.95	Floppy Disc Controllers	
8085	22.50	WD 1771 single D.	39.95
8086 Intel 16 bits	85.00	WD 1781 Double D	65.00
TMS9900 16 bits	49.95	WD 1791 D/D 3740	*

EPROMS		1-15	16-63	64+
1702A	2K	4.95	4.50	4.00
2708	8K	9.95	9.50	9.00
2716 5v	16K	29.95	27.50	*
2716 TI		24.88	20.00	*
2532		85.00	*	*

MICROCOMPUTER POWER SUPPLY

This regulated supply is powered by an 8 Amp center tapped industrial transformer. 36,000 MFD of filtering and dual pass transistor regulation make this power supply a must for any micro-computer workshop. Triple outputs. 5, 7.2, 6.5 Volt D.C.

$29

direct connect MODEM

UNIVERSAL DATA 103

Connects directly to the new modular phone jack. Fully powered from your existing telephone line. No need to locate external AC power. Crystal control prevents frequency drift. Direct connect feature eliminates loss of information due to carbon compression that is associated with acoustic modems. Runs circles around those other "Domesticated" modems.

$169

$850 Regent 25

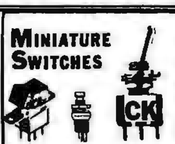
Through years of research the ADDS Corporation has evolved a low maintenance, extremely durable CRT terminal capable of withstanding an abusive 24 hour duty cycle. The Regent 25 features Intel 8085 microprocessor controlled circuitry along with the Cherry Switch long-life capacitance keyboard.

18 key cursor and numeric pad doubles to allow for user definable special functions. True descending lower case characters along with a fully addressable cursor makes the Regent 25 the ideal word processing terminal.

High-resolution screen is capable of displaying 96 upper and lower case ASCII characters and 32 control codes. This terminal is switch selectable to display six European languages.

At $850 (plus shipping) the Regent 25 offers the best value in todays CRT terminal market. Additional data upon request.

MINIATURE SWITCHES



your choice

	10	50	100	1k
$.98	$.88	.81	.73	.66

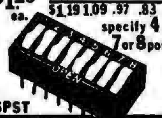
SPDT Miniature Toggles

7101 C&K	ON-NONE-ON
7107 jbt	ON-OFF(mnt.ON)
7108 CK	ON-(moment ON)
7103 CK	ON OFF ON
Rotary	3P-4-Pos.
Rotary	3P-6-Pos.
Push B (N.O.)	$.39ea. 4/$1

DIP Switch

	10	25	100	1k
$1.29 ea.	$1.19	1.09	.97	.83

specify 4, 7 or 8 pos.



SPST

$139.50 PORTABLE DATA ENTRY SYSTEM

These used data terminals were originally designed for chain store inventory control and order entry systems. The operator enters the inventory control number, merchandise on hand and the unit price. After all pertinent data has been entered into the recorder, the main warehouse is telephoned, the handset is placed in the acoustic coupler and all the recorded information is transmitted back to the master computer. With a little imagination and one of these portable entry systems, you should be able to exchange programs and computer information with associates across the country. All units were removed from service in working condition. Original cost $2,500. Each system comes complete with:

- Portable Cassette Drive Unit
- Removable Entry Keyboard with LED Display
- Five Gould "D" NiCads
- Acoustical Coupler
- Battery Charger
- DB25 Cable
- Shoulder strap
- Full Documentation

DISCOUNT Wire Wrap Center

IC SOCKETS

pin	wire wrap ea.	25	50	low profile ea.	25	50
8				17	16	15
14	37	36	35	18	17	16
16	38	37	36	19	18	17
24	99	93	85	36	35	34
40	169	155	139	63	60	58

KYNAR WIRE WRAP

50ft.	500	1,000	11,000
$.98	$9.	$15.	$105.

$34.95

$29.95 BW 630

OK HOBBY WRAP-30 wire wrap & strip tool

$5.45

(213) 679-9001

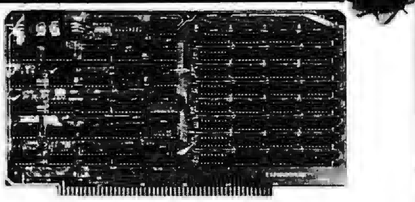
VISA · master charge

All merchandise sold by California Digital is premium grade. Most orders shipped same day as received. Shipping: first five pounds $2.00 $.40 for each additional pound. Foreign orders add 10%. Access will be refunded. California Res. add 6%. Open accounts offered to State supported educational institutions and companies with "Strong" Dunn & Bradstreet. COD's discouraged.

Circle 270 on inquiry card.

JADE. INFLATI
FOR THE 80's.

OPENING BOUT



EXPANDORAM
Expandable to 64K Using 4116 RAMS

Interfaces with most popular S-100 boards
Bank selectable; PHANTOM provision
Draws only 5 watts fully populated
Designed to work with Z-80, 8080, and 8085 systems
No wait states required
16K boundaries & protect via dip switches
Kits come with sockets for full 64K
Invisible refresh

MEM-16130K (16K KIT) $199.95
MEM-16130A (16K A&T) $249.95
MEM-32131K (32K KIT) $254.95
MEM-32131A (32K A&T) $304.95
MEM-48132K (48K KIT) $309.95
MEM-48132A (48K A&T) $359.95
MEM-64133K (64K KIT) $364.95
MEM-64133A (64K A&T) $414.95

Sale Price $475.00

32K STATIC RAM
Expandable 8K/32K, 2/4MHz, KIT/A&T

Switchable 2 or 4 MHz

THE JADE BIG Z
Z-80A CPU with Serial I/O Port

This CPU can accomodate a 2708, 2716, or 2732 EPROM in SHADOW mode, allowing you to use a full 64K of RAM. The MWRITE signal is generated automatically if you use the board without a front panel. There's also an independent on-board USART to control the RS232 serial port at baud rates from 75 to 19,200.

We've sold thousands of these high quality S-100 CPU boards at $159.95; but now, in a brief fit of financial insanity, we're offering them to you for only $135.00! **Don't pass this one up!**

CPU-30201K (KIT) $135.00
CPU-30201A (A&T) $199.00
CPU-30200B (BARE BOARD) .... $ 35.00

S D Systems

EXPANDORAM II
4 MHz RAM Board Expandable to 256K

S-100 bus compatible, up to 4 MHz operation
Expandable memory from 16K to 256K
Dip switch selectable boundaries
Page-mode allows up to 8 boards on the same bus
Invisible refresh; PHANTOM output disable
Designed to operate in Z-80 based systems

MEM-16630K (16K KIT) $279.95
MEM-16630A (16K A&T) $329.95
MEM-32631K (32K KIT) $349.95
MEM-32631A (32K A&T) $399.95
MEM-48632K (48K KIT) $419.95
MEM-48632A (48K A&T) $469.95
MEM-64633K (64K KIT) $489.95
MEM-64633A (64K A&T) $539.95

Solid State Music

PB-1
EPROM Programmer for 2708 or 2716

MEM-99510K (KIT) $125.00
MEM-99510A (A&T) $175.00

JADE DOUBLE-D
Double Density Disk Controller

Read/write single or double density, 8" or 5¼" drives
On board Z-80 insures reliable operation
CP/M compatible in either single or double density
Density is software selectable
Up to 4 single or double sided, single or double density drives may be mixed on the same system
EIA level serial printer interface on board-up to 9600 baud (perfect for despooling operations)
All the hard work of disk access is done by the on board Z-80A and 2K memory, leaving your host CPU free for its normal duties
Uses IBM standard formats for proven reliability
THIS BOARD REALLY WORKS!!!!!!

IOD-1200K (DOUBLE-D KIT) $295.00
IOD-1200A (DOUBLE-D A&T) $395.00
IOD-1200D (MANUAL ONLY) .... $ 15.00

Televideo

SMARTER TERMINAL
Lower Price, More Features

TELEVIDEO MODEL 912

Microprocessor controlled, 7 x 10 upper and lower case characters, underlining, reverse video, dual intensity, blinking fields, protected fields, self test, block and conversation modes, auxiliary RS-232 port, all standard baud rates from 75 to 9600 baud, 10 key numeric pad, 115/230 VAC, 50/60 Hz, nationwide field service through General Electric Corporation.

912B (TTY KEYBOARD) $825.00
912C (TYPEWRITER KEYBOARD) $875.00

TELEVIDEO MODEL 920

All the features of the 912 plus 11 special function keys, 6 editing keys, 2 transmission keys, making the 920 a perfect mate to a word processing or business computer.

920B (TTY KEYBOARD) $895.00
920C (TYPEWRITER KEYBOARD) $995.00

JADE
Memory Expansion Kits

TRS-80 APPLE EXIDY

Everything you need to add 16K of memory to your computer. Your kit comes neatly packaged with easy to follow instructions. In just minutes your computer is ready to tackle more advanced software.

$59.95

JADE DISKETTES
Magnificent Magnetic Media™

5¼" single sided, single density, box of 10
MMD-5110103 (SOFT SECTOR) $29.95
MMD-5111003 (10 SECTOR) $29.95
MMD-5111603 (16 SECTOR) $29.95
5¼" double sided, double density, box of 10
MMD-5220103 (SOFT SECTOR) $39.95
8" single sided, single density, box of 10
MMD-8110103 (SOFT SECTOR) $34.95
8" single sided, double density, box of 10
MMD-8120103 (SOFT SECTOR) $55.95
8" double sided, double density, box of 10
MMD-8220103 (SOFT SECTOR) $57.95

S D Systems

VERSAFLOPPY
Versatile Floppy Disk Controller

IBM 3740 soft sectored format
S-100 Z-80 or 8080 compatible
Controls up to 4 single or double sided drives
Compatible with all popular disk drives
CP/M compatible
Listings for control software included

IOD-1150K (KIT) $239.00
IOD-1150A (A&T) $289.00

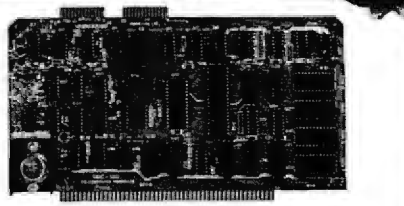
S D Systems

Z-80 STARTER
Complete Z-80 Microcomputer

On-board keyboard, display, EPROM programmer, cassette interface and S-100 interface
Wire-wrap area and room for 2 S-100 connectors
Two 8-bit parallel I/O ports, 4 channel CTC,
5 programmable breakpoints
Examine & change memory, I/O ports, or register

CPS-30010K (KIT) $299.95
CPS-30010A (A&T) $369.95

TITLE MATCH



S D Systems

SBC-100/200
2 or 4 MHz Single Board Computer

S-100 bus compatible Z-80 CPU
1K of on-board RAM
4 EPROM sockets accomodate 2708, 2716, or 2732
One parallel and one serial I/O port
4-channel counter timer chip (Z-80 CTC)
Software programmable serial baud rates

CPC-30100K (2 MHz KIT) $259.95
CPC-30100A (2 MHz A&T) $309.95
CPC-30200K (4 MHz KIT) $289.95
CPC-30200A (4 MHz A&T) $339.95

Coming Soon

NEW JADE P/S I/O
Parallel Serial Interrupt Board

Z-80 SIO, PIO, 2 CTCs, expands to 2 SIOs, 4 CTCs
4 serial ports (async, sync, bisync, SDLC/HDLC)
2 parallel ports with full handshake
Software baud rate generators, interval timers, counters, and generates 32 vectored interrupts
Designed especially for MP/M multi-user multitasking operating systems. For use with Z-80 only

IOI-1045B (BARE BOARD) .... $ 59.95
IOI-1045K (KIT) $199.95
IOI-1045A (A&T) $279.95

Solid State Music

I/O-4
2 Serial & 2 Parallel I/O Ports

IOI-1010K (KIT) $149.95
IOI-1010A (A&T) $199.95

Circle 267 on inquiry card.

ON FIGHTER ROUND #3.

KNOCKOUT PRICES

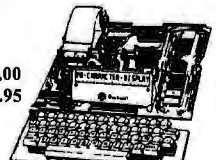
S D Systems
VERSAFLOPPY II
Double Density Disk Controller

Single or double density floppy disk controller
985600 bytes on 8" double sided diskettes
259840 bytes on double sided 5¼" diskettes
S-100 bus (IEEE) standard compatible
IBM 3740 format in single density
8" and 5¼" drives controlled simultaneously
Operates with Z-80, 8080, and 8085 CPU's
Controls up to 4 drives
Vectored interrupt operation optional

IOD-1160K KIT $299.95
IOD-1160A A&T $349.95

TKO CHAMPS

Special Package Price
ROCKWELL AIM-65
The Head-Start in Microcomputers



KIM-1 compatible
On-board printer
Full ACSII keyboard
AIM-65 w/1K RAM..$395.00
AIM-65 w/4K RAM..$439.95
8K BASIC ROM..$100.00
POWER SUPPLY..$59.95
CASE for AIM-65..$49.95
4K Assembler/Editor..$85.00

Special Package Price $599.00
4K AIM-65, 8K BASIC ROM, Power Supply, and Case.

Lobo Drives
DUAL DISK SPECIAL
Double Density, Single or Double Sided

Two double density certified 8" Shugart disk drives mounted in an attractive metal enclosure.

MSF-12800R (SINGLE SIDED) .... $ 995.00
MSF-125202 (DOUBLE SIDED) $1495.00

We Think It's Superior
SDOS
A New Disk Operating System

SDOS is a disk operating system which will run any program that runs under CP/M*. It is designed specifically for use with the SBC-100/Versafloppy (I or II) board set by S.D. Systems. SDOS actually has more functions than CP/M, including file attributes, disk label, and read/write logical blocks. It provides additional protection features and is expandable to a multi-user realtime system. And if all that doesn't impress you, SDOS also contains S.D.'s ASSEMBLER/EDITOR/LINKER package and CBASIC 2!

SFX-55001002M (5¼" W/MAN) $150.00
SFX-55001006F (8" W/MAN) $150.00
SFX-55001000D (MANUAL ONLY) .... $ 15.00

*CP/M is a trademark of Digital Research

Textool
ZIP* DIP II SOCKETS

16 PIN ZIP* DIP II .... $ 5.50
24 PIN ZIP* DIP II .... $ 7.50
40 PIN ZIP* DIP II .... $ 10.25

• ZERO INSERTION PRESSURE

RAMS
21L02 (2 MHz) ... $ 1.25
21L02 (4 MHz) ... $ 1.50
2114L (2 MHz) ... $ 5.75
2114L (4 MHz) ... $ 5.95
4116 .... $ 8.95
4127 (70ns) ...... $ 39.95
4164 (64K x 1) $175.00
5257 (2 MHz) ..... $ 6.75
5257 (4 MHz) ..... $ 7.25

SUPPORT DEVICES
8212 .... $ 4.95
8214 .... $ 4.65
8216 .... $ 2.95
8224 .... $ 3.25
8224-4 .... $10.95
8226 .... $ 3.85
8228 .... $ 4.95
8238 .... $ 4.95
8243 .... $ 8.00
8250 .... $14.95
8251 .... $ 6.50
8253 .... $13.95
8255 .... $ 6.50
8257 .... $19.95
8259 .... $17.95
8275 .... $49.95
8279 .... $15.95

Z80 SUPPORT
3881 (PIO) .... $ 9.50
3881-4 (PIO-4 MHz) $14.50
3882 (CTC) .... $ 9.50
3882-4 (CTC-4MHz) $14.95
3883 (SIO) $29.50
3884 (SIO) $49.50

BAUD RATE GENERATORS
MC14411 .... $10.00
CRYSTAL .... $ 4.95

UARTS
AY5-1013A $5.25
AY3-1014A $8.25
TR1602B $5.25
TMS6011 .... $5.95
IM6403 .... $9.00

6800 SUPPORT
6821P .... $ 5.95
6828P $11.95
6834P $12.95
6840P $18.75
6850P .... $ 4.80
6852P .... $ 5.79
6875L .... $ 7.40
68488P $25.00

PROMS
2708 (450ns) .... $ 8.95
2716 (450ns) $34.95
2716 (5v) $34.95
2732 (5v) $95.00
2758 (5v) $34.95

MICROPROCESSORS
Z-80 .... $10.95
Z-80A $14.95
6502 .... $11.50
6800 .... $11.95
6802 .... $17.95
6809 .... $39.95
8035 .... $24.00
8035-8 .... $24.00
8080A .... $ 6.59
8085 .... $15.95
TMS9900JL $39.95

Special Price for
NOVATION CAT
Acoustic Coupler/Modem

$149.95

Let your computer talk to other computers!
Bell Systems 103 compatible
300 baud, answer or orginate

IOM-5200A (SALE PRICED) $149.95

Get Down to Business
8" DISK FOR APPLE
Special *JADE* Package

Almost 5 times more capacity than the standard Apple 2 Drive System. Special package price includes: Sorrento Valley Associates interface and controller, 2 Shugart 8" disk drives, cabinet and power supply, software and cables.

List $1,995.00 .... $1495.00

Integral Data Systems
THE PAPER TIGER
132 Column Dot Matrix Printer

Up to 198 CPS
1.75 to 9.5 inch adjustable tractor.
Parallel and serial interface.
98 character ASCII set.
80 to 132 columns.
6 or 8 lines per inch.
Eight software selectable character sizes.
110, 300, 600, or 1200 baud.

PRM-33440 .... $950.00
PRM-33441 (GRAPHICS & 2K BUFFER) . $1050.00

Special Package Price

RS-232 SET
1 Male DB-25,
1 Female DB-25,
1 Cover

$6.50

Jade's New Motherboards
ISO-BUS
Silent, Simple and On Sale!

6 SLOT
BB .... $ 19.95
KIT .... $ 39.95
A&T .... $ 49.95

12 SLOT
BB .... $ 29.95
KIT .... $ 69.95
A&T .... $ 89.95

18 SLOT
BB .... $ 49.95
KIT .... $ 99.95
A&T $139.95

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COMPUTER PRODUCTS
4901 W.Rosecrans, Hawthorne, CA 90250

TERMS OF SALE: Cash, checks, credit cards money orders or from recognized institutions Purchase orders accepted. Minimum order $10.00 California residents add 6% sales tax. Minimum shipping and handling charge $2.50. Prices are for U.S. and Canadian delivery only and are subject to change without notice. For export prices and information send for a JADE INTERNATIONAL CATALOG.

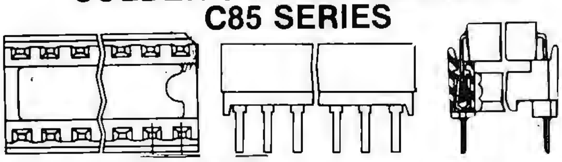
VISA · AMERICAN EXPRESS · MASTER CHARGE

Circle 267 on inquiry card.

PRIORITY ONE ELECTRONICS

Texas Instruments

FACE GRIP LOW PROFILE SOLDER TAIL DIP SOCKETS C85 SERIES

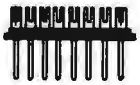


- Face grip design provides maximum retention force
- Anti-wicking feature
- Redundant contact points

PART NO.	PINS	1-9	PRICE 10-49	50-99	100-499	500-999	1,000 +
TIS-08LP	08	N/A	.15	.10	.08	.07	.06
TIS-14LP	14	N/A	.18	.15	.14	.12	.11
TIS-16LP	16	N/A	.20	.18	.16	.13	.12
TIS-18LP	18	.30	.25	.22	.18	.15	.13
TIS-20LP	20	.30	.25	.23	.20	.17	.145
TIS-22LP	22	.35	.30	.25	.22	.19	.17
TIS-24LP	24	.40	.35	.30	.24	.20	.18
TIS-28LP	28	.45	.40	.35	.28	.24	.21
TIS-40LP	40	.50	.45	.42	.40	.35	.31

*MINIMUM ORDER $1.00 Per Line item
Sockets purchased in multiples of 100 per type may be combined for best price

DIP PLUGS



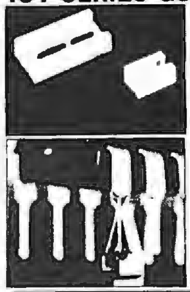
PART NO.	PINS	PRICE 1-9	10-24	25-99	100-249
KNX-080P	8	.50	.45	.43	.40
KNX-140P	14	.65	.60	.58	.55
KNX-160P	16	.70	.65	.62	.58
KNX-240P	24	1.15	1.05	.90	.95
KNX-400P	40	1.90	1.70	1.60	1.50

ROBINSON NUGENT, INC.

GOLD 3 LEVEL WIRE WRAP SOCKETS

AND OTHER LEADING MANUFACTURES

ICY SERIES GOLD 3 LEVEL WIRE WRAP SOCKETS

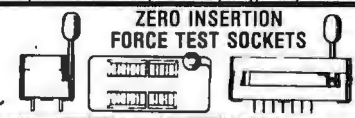


- Deep Chamfered Closed Entry Contacts
- RN Side Wipe Contact Design
- Terminal Barbs Allow Self-lock into PC Board
- Rugged Socket Body Design

PART NO.	PINS	PRICE* 1-9	10-24	25-99	100-249	250-999
RNS-08WWG	8	.50	.42	.40	.37	.33
RNS-14WWG	14	.60	.49	.47	.45	.42
RNS-16WWG	16	.65	.52	.50	.47	.44
RNS-18WWG	18	.85	.75	.70	.65	.60
RNS-20WWG	20	1.00	.90	.80	.75	.70
RNS-22WWG	22	1.25	1.15	1.10	1.05	1.00
RNS-24WWG	24	1.25	1.15	1.10	1.05	1.00
RNS-28WWG	28	1.60	1.50	1.40	1.30	1.20
RNS-40WWG	40	1.85	1.65	1.55	1.45	1.35

*Price based on gold not exceeding $500 per oz.
Sockets purchased in mulitples of 50 per type may be combined for best price.

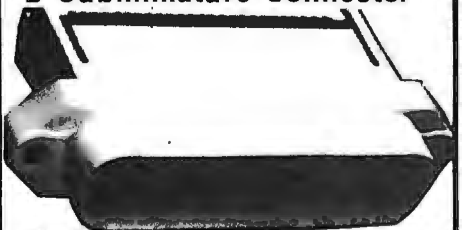
ZERO INSERTION FORCE TEST SOCKETS



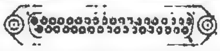
ZIP-16DIP $5.50
ZIP-24DIP $7.50
ZIP-40DIP $10.25

Litton WINCHESTER ELECTRONICS

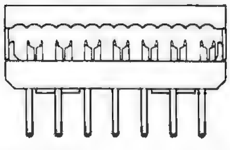
D-Subminiature Connector



P = Plug-Male
S = Socket-Female
C = Cover-Hood



PART NO.	NO. OF PINS	1-9	10-24	25-99
IDC-DE9P	9	4.00	3.60	3.20
IDC-DE9S	9	4.20	3.80	3.40
IDC-DE9C	9	1.10	1.00	
IDC-DA15P	15	4.20	3.75	3.40
IDC-DA15S	15	4.85	4.35	3.90
IDC-DA15C	15	1.25	1.10	.95
IDC-DB*25P	25	6.00	5.20	4.70
IDC-DB*25S	25	6.35	5.60	5.00
IDC-DB*25C	25	1.50	1.35	1.20
IDC-DC37P	37	8.00	7.20	6.40
IDC-DC37S	37	10.25	9.20	8.20
IDC-DC37C	37	2.00	1.80	1.60



Dip Plugs

PART NO.	NO. OF PINS	1-9	10-24	25-99
IDC-14DP	14	1.40	1.25	1.10
IDC-16DP	16	1.60	1.45	1.30
IDC-24DP	24	2.20	2.00	1.80

FLEX-COM

Edgecard Connector

PART NO.	NO. OF PINS	PRICE 1-9	10-24	25-99
IDC-20CE	10/20	4.15	3.75	3.30
IDC-26CE	13/26	4.75	4.30	3.80
IDC-34CE	17/34	5.70	5.10	4.50
IDC-40CE	20/40	6.50	5.80	5.25
IDC-50CE	25/50	7.00	6.30	5.40

RIBBON CABLE

Color Coded Laminated Cable for Insulation Displacement 28 Guage. 7 Strand

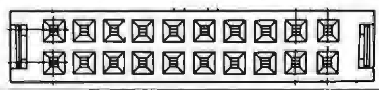
PART NO.	NO. OF CONDUCTORS	PRICE PER SPOOL 10 Ft.	100 Ft.
IDC-09CC	9	N/A	26.20
IDC-14CC	14	4.60	36.65
IDC-16CC	16	5.20	42.00
IDC-25CC	25	N/A	68.15
IDC-26CC	26	8.50	68.15
IDC-34CC	34	11.00	89.10
IDC-40CC	40	N/A	104.85
IDC-50CC	50	16.00	131.05

GRAY LAMINATED CABLE FOR INSULATION DISPLACEMENT
28 Gauge 7 Strand

PART NO.	NO. OF CONDUCTOR	PRICE PER SPOOL 10 Ft.	100 Ft.
IDC-09GY	9	N/A	18.05
IDC-14GY	14	N/A	26.20
IDC-16GY	16	4.00	30.20
IDC-20GY	20	N/A	38.50
IDC-25GY	25	N/A	50.32
IDC-26GY	26	6.00	50.32
IDC-34GY	34	8.10	65.25
IDC-40GY	40	N/A	76.85
IDC-50GY	50	11.00	93.10

IDC System

Socket Connector



PART NO.	NO. OF PINS	PRICE 1-9	10-24	25-99
IDC-20SKT	10/20	2.50	2.25	2.00
IDC-26SKT	13/26	3.20	2.85	2.30
IDC-34SKT	17/34	4.20	3.75	3.30
IDC-40SKT	20/40	5.00	4.50	3.90
IDC-50SKT	25/50	6.00	5.40	4.75

Header Connector

Right Angle Soldertail GOLD Header

PART NO.	1-7	10-24	25-99
IDC-RAH 20STG	1.60	1.45	1.30
IDC-RAH 26STG	2.00	1.80	1.60
IDC-RAH 34STG	2.60	2.35	2.10
IDC-RAH 40STG	3.00	2.70	2.40
IDC-RAH 50STG	3.60	3.25	2.90

Right Angle Wire Wrap Gold Header

PART NO.	1-9	10-24	25-99
IDC-RAH 20WWG	3.60	3.25	2.90
IDC-RAH 26WWG	4.30	3.90	3.50
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INSTALLATION/ASSEMBLY TOOLS are available call for prices & information.

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*SOCKET and CONNECTOR prices based on GOLD, not exceeding $500 per oz.
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PRIORITY ONE ELECTRONICS

CENTRONICS 730 Dot Matrix Printer

SAVE $100.00

PRICE $695.00

STANDARD FEATURES: • 50 Characters/second • Characters/line • 10 characters/inch • 3-way paper handling system • 7 x 7 dot matrix • 96 character ASCII • microprocessor electronics • unidirection print at 50 ips • high speed return approximately 10 ips • 21 lpm with 80 columns printed • 58 lpm with 20 columns printed • 80 character buffer • 6 lpi vertical • Centronics Colors and logo

FORMS HANDLING: Roll Paper 8.5 in x 5.0 dia with 1 in. core maximum dimension 3.5 in. wide with .38 in. core minimum dimension. Fan Gold: 9.0 in. /22.9 cm. wide pin to pin 9.5 in./24.1cm wide overall. Up to 3 ply paper with 2 carbons (total thickness not to exceed .012 inches) Cut Sheet: Maximum width 8.5 inches.

RIBBON SYSTEM: Continuous ribbon 9/16" (14mm) wide, 20 yards (18.3 meters) long. Mobius Loop allows printing on upper and lower portion on alternate passes

OPERATOR CONTROLS: Power on/off Reset Switch -allows disabling of printer without dropping AC.

DATA INPUT: 7 or 8 bit ASCII parallel, TTL levels with strobe. Acknowledge pulse indicates that data was received

PHYSICAL DIMENSIONS: Weight: less than 10 lbs /5 kg -Width: 14.5 inches/37 cm -Depth: 11.0 inches/28cm -Height: 4.89 inches/13cm -Dimensions exclusive of roll paper holder.

SHIPPING WEIGHT: 14 lbs.

CEN-730-1 (Parallel Int.)............LIST PRICE: $795.00

TRS-80/APPLE MEMORY EXPANSION KITS

4116's RAMS

from Leading Manufacturers

(16Kx1 200/250ns)

100% GUARANTEED

1,000's SETS SOLD

8 for $55.00

ADD $3.00 FOR PROGRAMMING JUMPERS FOR TRS-80 KEYBOARD

4116's 100 pcs & UP $5.50 each

1000 pcs & UP $5.00 each

4 MHZ EXPANDORAM II KIT

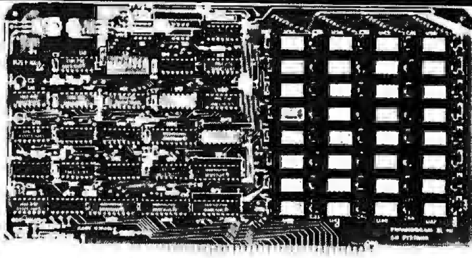
The S-100 Memory Board for the 80's

NEW

SD SYSTEMS' ExpandoRAM II is a state-of-the-art dynamic RAM board with capacities from 16K bytes (4116) to 256K bytes (4164). It operates on the industry S-100 Bus. The ExpandoRAM II's design allows eight boards to operate from the same S-100 Bus. Page mode operation provides the system with the capability of servicing multiple users without RAM interference. Invisible refresh and synchronization with wait states provide greater reliability, and processing speeds up to 4 Mhz.

The ExpandoRAM II is compatible with some S-100 CPU's based on the Z80 microprocessor. When other SD SYSTEMS 200 series boards are combined with the ExpandoRAM II, they create a microcomputer with exceptional capabilities and features.

- S-100 Bus Compatible
- Up to 4Mhz Operation
- Expandable Memory from 16K to 256K
- DIP Switch Selectable Boundaries
- Uses 16K (4115) or 64K (4164) Memory Devices
- Page Mode Operation Allows up to 8 Memory Boards on Bus
- Operates with Z80 CPU's
- Phantom Output Disable
- Invisible Refresh (Synchronized with Wait States)



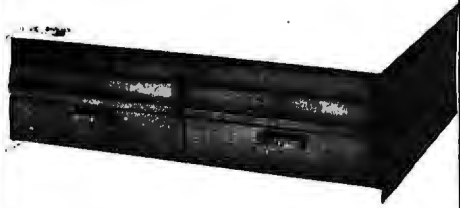
SDS - EXPANDOPRAM II KIT (4116)

Sale Price

16K... $280.00 48K.. $399.00

32K... $340.00 64K.. $459.00

LOBO 8" DISK DRIVE CABINET



New from Lobo, a dual Cabinet with power supply, and internal data cable hook-up.

- Cabinet accepts 2 801R, 800R, FD120, or FD200 style disk drives.
- Power Supply for 2 drives.
- Assembled, tested and guaranteed by Lobo Drives.
- Shipping Weight 30 lbs.

LBO — DUAL 8 PCS..........$329.00

BUY CABINET AND DRIVES AND SAVE

WITH 1 DRIVE
LBO-801R-1PSC $775.00

WITH 2 DRIVES
LBO-801R-2PSC $1250.00

DISC DRIVE ONLY

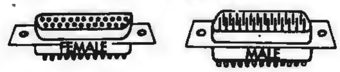
SHU-801R.......$499.00

EXTERNAL DATA CABLES

CARDEDGE TO CARDEDGE
PRI-50CE-CE $19.95

CARDEDGE TO SOCKET
PRI-50CE-SKT $19.95

RS232 and "D" SUB-MINIATURE CONNECTORS



P = Plug, Male Type - S = Socket, Female Type - C = Cover, Hood

PART NO.	DESCRIPTION	PRICE 1-9	10-24	25-99
CND-DE9P	9 Pin Male	1.70	1.50	1.40
CND-DE9S	9 Pin Female	2.35	2.10	2.00
CND-DE9C	9 Pin Cover	1.50	1.35	1.20
CND-DA15P	15 Pin Male	2.45	2.25	2.10
CND-DA15S	15 Pin Female	3.35	3.20	3.00
CND-DA15C	15 Pin Cover	1.60	1.45	1.30
CND-DB25P	25 Pin Male	2.90	2.70	2.50
CND-DB25S	25 Pin Female	3.75	3.65	3.35
CND-DB51212-1	1 pc Grey Hood	1.50	1.30	1.10
DB-P258C	2 pc Grey Hood	1.45	1.25	1.00
DB1226-1A	2 pc Black Hood	1.90	1.65	1.45
CND-DC37P	37 Pin Male	4.40	4.20	3.90
CND-DC37S	37 Pin Female	6.20	5.95	5.70
CND-DC37C	37 Pin Cover	2.25	2.00	1.75
CND-DD50P	50 Pin Male	5.75	5.45	5.00
CND-DD50S	50 Pin Female	9.65	8.85	8.25
CND-DD50C	50 Pin Cover	2.40	2.20	2.00
D20418-S	Hardware Set 2 pr.	1.00	.80	.70
CND-RS232-8FT	RS232, DB25P, EIA class 1 cable 8 con. 8 ft. long	18.00	16.00	14.00
CND-57-30360	Centronics 700 Series printer connector	9.00	7.50	6.00

NOVATION CAT

ACOUSTIC COUPLER/MODEM

List - $199.00 .... Sale $156.00

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Low Power 450ns in lots of 20.....$1.10

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Low Power 250ns in lots of 20.....$1.25

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1Kx4 300ns Low Power........8/$50.00

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4Kx1 300ns Low Power........8/$55.00

2708
8K 450ns EPROM ....8/$60.00-$8.50 ea.

2716
16K 5 Volt only EPROM......$24.00 ea.
10/$200.00

Verbatim

Part No.	Sectoring	Application	Pk. of 2	Box of 10
VRB-MD 525-01	Soft Sector	TRS-80 Apple	$ 8.95	$29.95
VRB-MD 525-10	Hard 10 Sector	North Star	$ 8.95	$29.95
VRB-MD 525-16	Hard 16 Sector	Micropolis	$ 8.95	$29.95
VRB-F032-1000	Hard Sector	Shugart 801R	$11.95	$37.00
VRB-F034-1000	Soft Sector	IBM 3740	$11.95	$37.00

SHIPPING WEIGHT 1 LB

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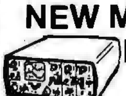

1 NLS MS-230 30 MHZ Scope...$598.15
2 NLS 41-141 10 to 1 Combo Probe$54.00
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LIST PRICE.................$697.15
MS 230 COMBO PRICE........ $547.15
SAVE $150.00

THE FAMOUS GODBOUT

ECONORAM II
8K 450ns RAM
UNKIT CLOSE OUT
$109.00ea. 2/$200.00

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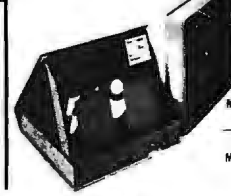

Part No		
MMM-KS-10	GREY BLACK BLUE BIEGE	8" DISKETTE HOLDER $4.50 or 3/$10.00
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*SOCKET and CONNECTOR prices based on GOLD, not exceeding $500 per oz.

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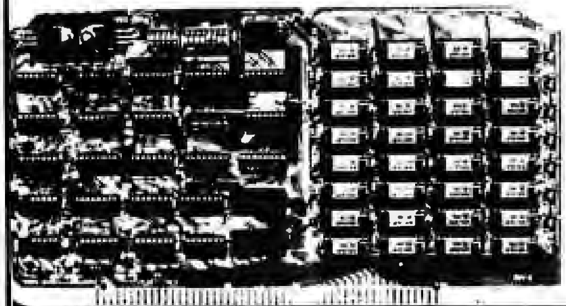
SD SYSTEMS

FACTORY REBATE SALE

WOW

When you purchase any S.D. SYSTEMS Computer Board, either kit or A&T from PRIORITY 1 ELECTRONICS you will receive a COUPON FOR A $25.00 CASH REBATE Direct from the Manufacturer SD SYSTEMS. Combine the Rebate with our already low prices, and you can hardly afford to pass up this special offer.

SD EXPANDORAM *The Ultimate S-100 Memory*



The EXPANDORAM is available in versions from 16K up to 64K, so for a minimum investment you can have a memory system that will grow with your needs. This is a dynamic memory with the invisable on-board refresh, and IT WORKS!

EXPANDO 64 KIT (4116)

	List Price	Sale Price
16K	385.00	189.00
32K	550.00	244.00
48K	715.00	298.00
64K	880.00	349.00

- Interfaces with Altair, IMSAI, SOL-8, Cromenco, SBC-100, and others.
- Bank Selectable
- Phantom
- Power 8VDC, ± 16VDC, 5 Watts
- Lowest Cost Per Bit
- Uses Popular 4116 RAMS
- PC Board is doubled solder masked and has silk-screen parts layout.
- Extensive documentation clearly written
- Complete Kit includes all Sockets for 64K
- Memory access time: 375ns, Cycle time: 500ns.
- No wait states required.
- 16K boundries and Protection via Dip Switches
- Designed to work with Z-80, 8080, 8050 CPU's

VERSAFLOPPY II

DOUBLE DENSITY, DOUBLE SIDED, DISC.CONTROLLER

NEW

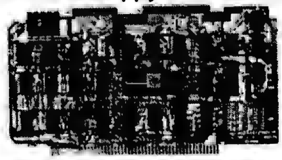
GENERAL DESCRIPTION
Versafloppy II is a flexible disk drive controller that incorporates a wide rangeof capabilities intoone board It operates with double density soft sectored format which provides 985.600 bytes of storage on a double sided 8 inch diskette and 129.920 bytes per side on a five inch mini diskette The Versafloppy II directly controls many popular disk drives These include Shugart SA400 and SA450, Shugart SA800 and SA850, Mayflower MFE500 and MFE700, Per Sci 70 and 277, and Siemans, BSI 105

- S-100 BusIEEE Standard Compatible
- IBM 3740 Compatible Soft Sectored Format for Single Density Drives
- Operates with bothStandard (8") and Mini (5") Drives Simultaneously
- Provides Control for Double SidedOperation
- Operateswith Z80, 8080, and 8085 Central Processing Unit
- Controls upto four drives
- Vectored Interrupt Operation Optional
- Control and Diagnostic Software Available in PROM
- SDOS Disk Operating System Compatible

SDS-VERSAFLOPPY II KIT......$335.00
SDS-VERSAFLOPPY II KIT.....$425.00

DISC CONTROLLER

SD"VERSAFLOPPY" KIT
The Versatile Floppy Disk Controller

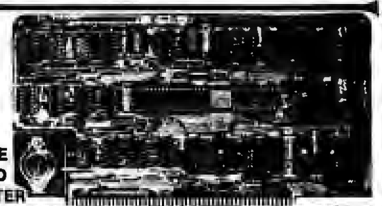


FEATURES IBM 3740 Soft Sectored Compatible S 100 BUS Compatible for Z 80 or 8080 Controls up to 4 Drives (single or double sided) Directly controls the following drives
1 Shugart SA400/450 Mini Floppy
2 Shugart SA800/850 Standard Floppy
3 PERSCI 70 and 277
4 MFE 700/750
5 CDC 9404/9406
6 GSI/Siemans FDD120 8
34 Pin Connector for Mini Floppy 50 Pin Connector for Standard Floppy Operates with modified CP/M operating system and C Basic Computer The new Versafloppy from S D Computer Products provides complete control for many of the available Floppy Disk Drives Both Mini and Full Size FD1771B 1 Single Density Controller Chip Listings for Control Software are included in price
CP/M for SD Versafloppy $100.00

DISC CONTROLLER
SD "VERSAFLOPPY" KIT
The Versatile Floppy Disk

$235.00

SINGLE BOARD COMPUTER



With On-Board RAM, PROM, CTC

- S-100 Bus Compatible
- Z80 Central Processing Unit
- 1024 Bytes of Random Access Memory
- 8K Bytes of PROM using 2716
- Parallel Input and Output Ports
- Four Channel Counter/Timer (Z80-CTC)
- Software Programmable Baud Rate Generator
- No Front Panel Required for Operation

Sale Price

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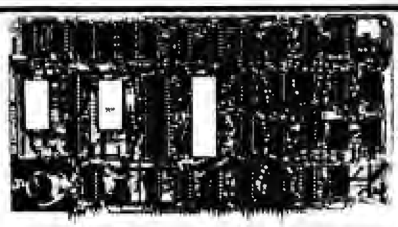
SDS-SBC-100 2MHZ A&T........$350.00
SDS-SBC-200 4MHZ KIT........$299.00
SDS-SBC-200 4MHZ A&T........$369.00



VDB-8024 VIDEO DISPLAY BOARD

With on-board Z80 Microprocessor

- S-100 bus Compatible
- Full 80 Characters by 24 Lines Display
- Characters Displayed by High Resolution 7 x 10 Matrix
- Composite or TTL Video Output
- Keyboard Power and Interface
- Forward and Reverse Scrolling Capability
- Blinking, Underlining, Field Reverse, Field Protect and Combinations
- Full Cursor Control
- 96 Upper and Lower Case Characters
- 32 Special Character Set
- 128 Additional User Programmable Characters (Optional)
- On-Board Z80 Microprocessor
- 2K Bytes Independent On-Board RAM Memory
- Glitch-Free Display

Sale Price

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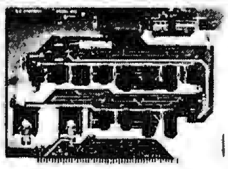
SDS-VDB-8024 A&T..........$469.00



PROM-100

Programming Board for PROM Development

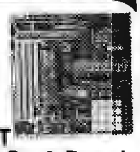
NEW

SD SYSTEMS' PROM-100 is a versatile PROM programming board offering complete EPROM programming capability. The board operates on the industry standard S-100 Bus. Support software verifies the erasure of EPROM and verifies the loaded program. SD SYSTEMS' PROM-100 offers a support-software listing with its operations manual.

- S-100 Bus Compatible
- Programs the Following EPROM s: 2708, Intel 2758, 2716, 2732 and Texas Instruments 2516
- Dip Switch Selection of EPROM type
- 25 VDC Programming Pulse Generated On Board
- Maximum Programming time: 16,384 Bits in 100 Seconds
- Power Requirement: +8VDC at 300 ma.; +16 VDC atr 100 ma.; −16 VDC at 60 ma.
- TTL compatible
- Software Provides for Reading of Object File from SDOS, CP/M or PROM and Programming into EPROM
- Program Verification • Verification of Erasure
- Zero Insertion Force Socket

Sale Price

SDS-PROM-100 KIT........... $175.00
SDS-PROM-100 A&T........... $225.00



Z80 STARTER KIT

A Complete Microcomputer On A Board

- Z80 CPU with 158 Instructions
- On-Board Keyboard and Display
- On-Board PROM Programmer for Single Voltage PROMS (2716, 2758, TI2516)
- Kansas City Standard Cassette Interface
- Simple Key Controlled Audio Cassette Load and Dump
- Expansion Provision for Mounting Two S-100 Connectors (Sockets Not Included)
- Wire Wrap Area for Custom Circuitry
- Single Step through RAM or PROM
- Memory Examine and Change
- Port Examine and Change
- Z80 CPU Register and Change
- 2K Byte ZBUG Monitor in ROM
- 1K Bytes of RAM (Expandable to 2K Bytes)
- A 4 Channel Hardware Counter/Timer (Z80-CTC)
- Two Bi-Directional 8-Bit I/O Ports (Z80-P10)
- Up to 5 Programmable Breakpoints
- Switch Selectable PROM or Monitor Restart
- Vectored Interrupts provided by Z80-CTC and

Sale Price

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SDS-Z80 STARTER A&T........$439.00

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7400 TTL

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SN7402N	.20	SN7473N	.35	SN74162N	1.95
SN7403N	.20	SN7474N	.35	SN74163N	.89
SN7404N	.25	SN7475N	.49	SN74164N	.89
SN7405N	.20	SN7476N	.35	SN74165N	.89
SN7406N	.29	SN7479N	5.00	SN74166N	1.25
SN7407N	.29	SN7480N	.50	SN74167N	1.95
SN7408N	.20	SN7482N	.99	SN74170N	1.59
SN7409N	.20	SN7483N	.69	SN74172N	6.00
SN7410N	.18	SN7485N	.89	SN74173N	1.25
SN7411N	.25	SN7486N	.35	SN74174N	1.00
SN7412N	.25	SN7489N	1.75	SN74175N	1.00
SN7413N	.40	SN7490N	.45	SN74176N	.79
SN7414N	.70	SN7491N	.59	SN74177N	.79
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SN7420N	.20	SN7494N	.65	SN74181N	1.95
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SN7422N	.39	SN7496N	.65	SN74184N	1.95
SN7423N	.25	SN7497N	3.00	SN74185N	1.95
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SN7426N	.29	SN74107N	.35	SN74188N	3.95
SN7427N	.25	SN74109N	.59	SN74190N	1.25
SN7429N	.39	SN74116N	1.95	SN74191N	1.25
SN7430N	.20	SN74121N	.35	SN74192N	.79
SN7432N	.25	SN74122N	.39	SN74193N	.79
SN7437N	.25	SN74123N	.59	SN74194N	.89
SN7438N	.40	SN74125N	.49	SN74195N	.69
SN7439N	.25	SN74126N	.49	SN74196N	.89
SN7440N	.20	SN74132N	.75	SN74197N	.89
SN7441N	.89	SN74136N	.75	SN74198N	1.49
SN7442N	.59	SN74141N	.79	SN74199N	1.49
SN7443N	.75	SN74142N	2.95	SN74S200	4.95
SN7444N	.75	SN74143N	2.95	SN74251N	.99
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SN7453N	.20	SN74152N	.59	SN74367N	.69
SN7454N	.20	SN74153N	.59	SN74368N	.69
SN7459A	.25	SN74154N	1.50	SN74390N	1.95
SN7460N	.20	SN74155N	.79	SN74393N	1.95
		SN74156N	.79		
		SN74157N	.65		

CMOS

CD4000	.39	CD4028	.89	CD4070	.55
CD4001	.39	CD4029	1.49	CD4071	.49
CD4002	.39	CD4030	.49	CD4072	.49
CD4006	1.19	CD4035	.99	CD4076	1.39
CD4007	.25	CD4040	1.49	CD4081	.39
CD4009	.49	CD4041	1.49	CD4082	.39
CD4010	.49	CD4042	.99	CD4093	.99
CD4011	.39	CD4043	.89	CD4098	1.19
CD4012	.25	CD4044	.89	MC14409	14.95
CD4013	.49	CD4046	1.79	MC14410	14.95
CD4014	1.39	CD4047	2.50	MC14411	14.95
CD4015	1.19	CD4048	1.35	MC14419	4.95
CD4016	.59	CD4049	.49	MC14433	13.95
CD4017	1.19	CD4050	.69	MC14506	.75
CD4018	.99	CD4051	1.19	MC14507	.99
CD4019	.49	CD4053	1.19	MC14562	11.95
CD4020	1.19	CD4056	2.95	MC14583	2.49
CD4021	1.39	CD4059	9.95	CD4508	3.95
CD4022	1.19	CD4060	1.49	CD4510	1.39
CD4023	.29	CD4066	.79	CD4511	1.29
CD4024	.79	CD4068	.39	CD4515	2.95
CD4025	.23	CD4069	.45	CD4518	1.29
CD4026	2.95			CD4520	1.29
CD4027	.69			CD4566	2.25

74C00

74C00	.39	74C85	2.49	74C163	2.49
74C02	.39	74C90	1.95	74C164	2.49
74C04	.45	74C93	1.95	74C173	2.60
74C08	.49	74C95	1.95	74C192	2.49
74C10	.39	74C107	1.25	74C193	2.49
74C14	1.95	74C151	2.90	74C195	2.49
74C20	.39	74C154	3.00	74C922	7.95
74C30	.39	74C157	2.15	74C923	6.25
74C42	1.95	74C160	2.49	74C925	8.95
74C48	2.49	74C161	2.49	74C926	8.95
74C73	.89			80C95	1.50
74C74	.89			80C97	1.50

LINEAR

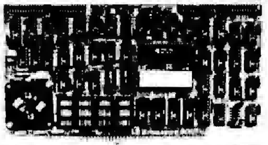
78MG	1.75	LM340K-18	1.35	LM710N	.79
LM106H	.99	LM340K-24	1.35	LM711N	.39
LM300H	.80	LM340T-5	1.25	LM723N/H	.55
LM301CN/H	.35	LM340T-6	1.25	LM733N	1.00
LM302H	.75	LM340T-8	1.25	LM739N	1.19
LM304H	1.00	LM340T-12	1.25	LM741CN/H	.35
LM305H	.60	LM340T-15	1.25	LM741-14N	.39
LM307CN/H	.35	LM340T-18	1.25	LM747N/H	.79
LM308CN/H	1.00	LM340T-24	1.25	LM748N/H	.39
LM309H	1.10	LM358N	1.00	LM1310N	1.95
LM309K	1.25	LM370N	1.95	LM1458CN/H	.59
LM310CN	1.95	LM373N	3.25	MC1488N	1.95
LM311N/H	.90	LM377N	4.00	MC1489N	1.95
LM312H	1.95	LM380N	1.25	LM1496N	.95
LM317K	6.50	LM380CN	.99	LM1556V	1.75
LM318CN/H	1.50	LM381N	1.79	MC1741SCP	3.00
LM319N	1.30	LM382N	1.79	LM2111N	1.95
LM320K-5	1.35	NE501N	8.00	LM2901N	2.95
LM320K-5.2	1.35	NE510A	6.00	LM3053N	1.50
LM320K-12	1.25	NE529A	4.95	LM3065N	1.49
LM320K-15	1.35	NE531H/V	3.95	LM3900N(3401)	.59
LM320K-18	1.35	NE536T	6.00	LM3905N	1.49
LM320K-24	1.35	NE540	6.00	LM3909N	1.25
LM320T-5	1.25	NE544N	4.95	MC5558V	.59
LM320T-5.2	1.25	NE550N	1.30	8038B	4.95
LM320T-8	1.25	NE555V	.39	LM75450N	.49
LM320T-12	1.25	NE556N	.99	75451CN	.39
LM320T-15	1.25	NE560B	5.00	75452CN	.39
LM320T-18	1.25	NE562B	5.00	75453CN	.39
LM320T-24	1.25	NE565N/H	1.25	75454CN	.39
LM323K-5	5.95	NE566CN	1.75	75491CN	.79
LM324N	1.49	NE567V/H	.99	75492CN	.89
LM339N	.99	NE570N	4.95	75493N	.89
LM340K-5	1.35	LM703CN/H	.69	75494CN	.89
LM340K-6	1.35	LM709N/H	.29	RC4136	1.25
LM340K-8	1.35			RC4151	3.95
LM340K-12	1.35			RC4194	4.95
LM340K-15	1.35			RC4195	4.49

74LS00TTL

74LS00	.35	74LS51	.29	74LS139	1.05
74LS01	.35	74LS54	.29	74LS151	1.05
74LS02	.35	74LS55	.29	74LS155	1.05
74LS03	.35	74LS73	.54	74LS157	1.05
74LS04	.42	74LS74	.54	74LS160	1.15
74LS05	.42	74LS75	.71	74LS161	1.39
74LS08	.35	74LS76	.54	74LS162	1.25
74LS09	.42	74LS78	.49	74LS163	1.39
74LS10	.35	74LS83	1.05	74LS164	1.50
74LS11	.75	74LS85	1.50	74LS175	1.25
74LS13	.59	74LS86	.54	74LS181	2.49
74LS14	1.25	74LS90	.71	74LS190	1.39
74LS15	.35	74LS92	.90	74LS191	1.39
74LS20	.35	74LS93	.90	74LS192	1.39
74LS21	.35	74LS95	.99	74LS193	1.39
74LS22	.35	74LS96	1.15	74LS194	1.39
74LS26	.35	74LS107	.54	74LS195	1.39
74LS27	.35	74LS109	.54	74LS253	1.25
74LS28	.35	74LS112	.54	74LS257	1.05
74LS30	.35	74LS123	1.50	74LS258	1.75
74LS32	.42	74LS125	1.05	74LS260	.83
74LS37	.45	74LS132	.99	74LS279	.90
74LS40	.35	74LS136	.59	74LS367	.75
74LS42	1.05	74LS138	1.05	74LS368	.75
74LS47	1.05			74LS670	2.49

Cromemco
incorporated

Z80-4MHz Single Card Computer



Cromemco's Single Card Computer is a complete computer which brings the power of the Z-80 and the flexibility of the S-100 bus to the dedicated computer environment.

The card offers 4 MHz operation, 8K bytes of on-board 2716 PROM, and 1K bytes of static RAM memory. This stand-alone card also provides a RS-232 (or 20mA current loop) serial interface with programmable baud rates to 76,800, vectored interrupt, 24 bits of bidirectional parallel I/O, and 5 programmable timers. Only a power supply and PROM software are required for operation. The Single Card Computer is assembled and tested (Model SCC-W) for $450. The Monitor and Control BASIC are available in two ROM's (Model MCB-216) for $80.

SCC-W (Assembled) **$450.00**

Processor: 4MHz Z-80
Instruction Set: 158 instructions incl. the 78 instructions of the 8080
ROM Capacity: 8K Bytes located from address 0000 to 1FFF
ROM Type: Intel 2716 PROM or equivalent
RAM Capacity: 1K Bytes located from address 2000 to 23FF
RAM Type: 4045, Static

Serial I/O Ports:
I/O Levels: RS-232 or 20mA current loop
Baud Rates: 110 to 76,800 (software selectable)
Parallel Ports:
Input Ports: 24 bits 8x3 bidirectional
Output Ports: 24 bits 8x3 bidirectional
Input Load: One TTL equivalent
Output Drive: 20 TTL loads
Interval Timers:
Number of timers: 5

Timer range: 0-16.32 milliseconds (software sel.)
Timer resolution: 64 microseconds
Vectored Interrupt:
No. of restart locations (Z-80 mode): 65,536
General Information:
UART type: 5801 Bus: S-100
Power requirements: +8V at 1.4A, +18V at 70mA, −18V at 25mA
Operating environment: 0-55°C

DISCRETE LEDS

XC556R	.200"	red	5/$1	MV50	.085"	red	6/$1	XC111R	.190"	red	5/$1
XC556G	.200"	green	4/$1	XC209R	.125"	red	5/$1	XC111G	.190"	green	4/$1
XC556Y	.200"	yellow	4/$1	XC209G	.125"	green	4/$1	XC111Y	.190"	yellow	4/$1
XC556C	.200"	clear	4/$1	XC209Y	.125"	yellow	4/$1	XC111C	.190"	clear	4/$1
XC22R	.200"	red	5/$1	XC526R	.185"	red	5/$1				
XC22G	.200"	green	4/$1	XC526G	.185"	green	4/$1				
XC22Y	.200"	yellow	4/$1	XC526Y	.185"	yellow	4/$1	INFRA-RED LED			
MV10B	.170"	red	4/$1	XC526C	.185"	clear	4/$1	¼"x¼"x1/16" flat			5/$1

DISPLAY LEDS

TYPE	POLARITY	HT	PRICE	TYPE	POLARITY	HT	PRICE
MAN 1	Common Anode-red	.270	2.95	MAN 6730	Common Anode-red ± 1	.560	.99
MAN 2	5 x 7 Dot Matrix-red	.300	4.95	MAN 6740	Common Cathode-red-D.D.	.560	.99
MAN 3	Common Cathode-red	.125	.25	MAN 6750	Common Cathode-red ± 1	.560	.99
MAN 4	Common Cathode-red	.187	1.95	MAN 6760	Common Anode-red	.560	.99
MAN 7G	Common Anode-green	.300	1.25	MAN 6780	Common Cathode-red	.560	.99
MA 7Y	Common Anode-yellow	.300	.99	DL701	Common Anode-red ± 1	.300	.99
MAN 72	Common Anode-red	.300	.75	DL704	Common Cathode-red	.300	.99
MAN 74	Common Cathode-red	.300	1.25	DL707	Common Anode-red	.300	.99
MAN 82	Common Anode-yellow	.300	.49	DL728	Common Cathode-red	.500	1.49
MAN 84	Common Cathode-yellow	.300	.99	DL741	Common Anode-red	.600	1.25
MAN 3620	Common Anode-orange	.300	.49	DL746	Common Anode-red ± 1	.630	1.49
MAN 3630	Common Anode-orange ± 1	.300	.99	DL747	Common Anode-red	.600	1.49
MAN 3640	Common Cathode-orange	.300	.99	DL749	Common Cathode-red ± 1	.630	1.49
MAN 4610	Common Anode-orange	.300	.99	DL750	Common Cathode-red	.600	1.49
MAN 4640	Common Cathode-orange	.400	.99	DL338	Common Cathode-red	.110	.35
MAN 4710	Common Anode-red	.400	.99	FND70	Common Cathode	.250	.69
MAN 4730	Common Anode-red ± 1	.400	.99	FND358	Common Cathode ± 1	.357	.99
MAN 4740	Common Cathode-red	.400	.99	FND359	Common Cathode	.357	.75
MAN 4610	Common Anode-yellow	.400	.99	FND503	Common Cathode(FND500)	.500	.99
MAN 4840	Common Cathode-yellow	.400	.99	FND507	Common Anode (FND510)	.500	.99
MAN 6610	Common Anode-orange-D.D.	.560	.99	5082-7730	Common Anode-red	.300	.99
MAN 6630	Common Anode-orange ± 1	.560	.99	HDSP-3400	Common Anode-red	.800	1.50
MAN 6640	Common Cathode-orange-D.D.	.560	.99	HDSP-3403	Common Cathode red	.800	1.50
MAN 6650	Common Cathode-orange ± 1	.560	.99	5082-7300	4 x 7 sgl. Digit-RHDP	.600	19.95
MAN 6660	Common Anode-orange	.560	.99	5082-7302	4 x 7 Sgl. Digit-LHDP	.500	19.95
MAN 6680	Common Cathode-orange	.560	.99	5082-7304	Overrange character (±1)	.500	15.00
MAN 6710	Common Anode-red-D.D.	.560	.99	5082-7340	4 x 7 Sgl. Digit-Hexadecimal	.600	22.50

RCA LINEAR

CA3013T	2.15	CA3082N	2.00
CA2023T	3.25	CA3083N	1.60
CA3035T	2.48	CA3086N	.85
CA3039T	1.35	CA3089N	3.75
CA3046N	1.30	CA3130T	1.39
CA3059N	3.25	CA3140T	1.25
CA3060N	3.25	CA3160T	1.25
CA3080T	1.25	CA3401N	.59
CA3081N	2.00	CA3600N	3.50

CALCULATOR CHIPS/DRIVERS

MM5725	$2.95
MM5738	2.95
DM8864	2.00
DM8865	1.00
DM8887	.75
DM8889	.75
9374 7-seg. LED driver	1.50
MM5309	4.95

CLOCK CHIPS

MM5309	4.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5387/1998a	4.95
CT 7001	6.95

MOTOROLA

MC1408L7	4.95
MC1408L8	5.75
MC1439L	2.95
MC3022P	2.95
MC3061P	3.50
MC4016(74416)	7.50
MC4024P	3.95
MC4040P	6.95
MC4044P	4.50

LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100
8 pin LP	.17	.16	.15
14 pin LP	.20	.19	.18
16 pin LP	.22	.21	.20
18 pin LP	.29	.28	.27
20 pin LP	.34	.32	.30
22 pin LP	.37	.36	.35
24 pin LP	.38	.37	.36
28 pin LP	.45	.44	.43
36 pin LP	.60	.59	.58
40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100
14 pin ST	.27	.25	.24
16 pin ST	.30	.27	.25
18 pin ST	.35	.32	.30
24 pin ST	.49	.45	.42
28 pin ST	.99	.90	.81
36 pin ST	1.39	1.26	1.15
40 pin ST	1.59	1.45	1.30

SOLDERTAIL (GOLD) STANDARD

	1-24	25-49	50-100
8 pin SG	.39	.35	.31
14 pin SG	.49	.45	.41
16 pin SG	.54	.49	.44
18 pin SG	.59	.53	.48
24 pin SG	.79	.75	.69
28 pin SG	1.10	1.00	.90
36 pin SG	1.65	1.40	1.26
40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100
8 pin WW	.59	.54	.49
10 pin WW	.69	.63	.58
14 pin WW	.79	.73	.67
16 pin WW	.85	.77	.70
18 pin WW	.99	.90	.81
20 pin WW	1.19	1.08	.99
22 pin WW	1.49	1.35	1.23
24 pin WW	1.39	1.26	1.14
28 pin WW	1.69	1.53	1.38
36 pin WW	2.19	1.99	1.79
40 pin WW	2.29	2.09	1.89

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ASST. 1	5 ea.	10 OHM / 27 OHM	12 OHM / 33 OHM	15 OHM / 39 OHM	18 OHM / 47 OHM	22 OHM / 56 OHM	50 PCS	$1.75
ASST. 2	5 ea.	68 OHM / 180 OHM	82 OHM / 220 OHM	100 OHM / 270 OHM	120 OHM / 330 OHM	150 OHM / 390 OHM	50 PCS	1.75
ASST. 3	5 ea.	470 OHM / 1.2K	560OHM / 1.5K	680 OHM / 1.8K	820 OHM / 2.2K	1K / 2.7K	50 PCS	1.75
ASST. 4	5 ea.	3.3K / 8.2K	3.9K / 10K	4.7K / 12K	5.6K / 15K	6.8K / 18K	50 PCS	1.75
ASST. 5	5 ea.	22K / 56K	27K / 68K	33K / 82K	39K / 100K	47K / 120K	50 PCS	1.75
ASST. 6	5 ea.	150K / 390K	180K / 470K	220K / 560K	270K / 680K	330K / 820K	50 PCS	1.75
ASST. 7	5 ea.	1M / 2.7M	1.2M / 3.3M	1.5M / 3.9M	1.8M / 4.7M	2.2M / 5.6M	50 PCS	1.75

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TL494CN	Switching Regulator	4.49
TL496CP	Single Switching Regulator	1.75
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MM5320	TV Camera Sync. Generator	14.95
MM5330	4½ Digit DPM Logic Block (Special)	3.95
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XR210	4.40			XR2264	4.25
XR215	4.40			XR2556	3.20
XR320	1.55			XR2567	2.99
XR-L555	1.50	JE2206KB	19.95	XR3403	1.25
XR555	.39	XR1800	3.20	XR4136	1.25
XR556	.99	XR2206	4.40	XR4151	3.95
XR567CP	.99	XR2207	3.85	XR4194	4.95
XR567CT	1.25	XR2208	5.20	XR4202	3.60
XR1310P	1.95	XR2209	1.75	XR4212	2.05
XR1468CN	3.85	XR2211	5.25	XR4558	.75
XR1488	1.95	XR2212	4.35	XR4739	1.15
XR1489	1.95	XR2240	3.45	XR4741	1.47

DIODES

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
				1N4002	100 PIV	1 AMP	12/1.00
				1N4003	200 PIV	1 AMP	12/1.00
1N746	3.3	400m	4/1.00	1N4004	400 PIV	1 AMP	12/1.00
1N751	5.1	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N754	6.8	400m	4/1.00	1N3600	50	200m	6/1.00
1N757	9.0	400m	4/1.00	1N4148	75	10m	15/1.00
1N759	12.0	400m	4/1.00	1N4154	35	10m	12/1.00
1N959	8.2	400m	4/1.00	1N4733	5.1	1w	28
1N965	15	400m	4/1.00	1N4734	5.6	1w	28
1N5232	5.6	500m	28	1N4735	6.2	1w	28
1N5234	6.2	500m	28	1N4736	6.8	1w	28
1N5235	6.8	500m	28	1N4738	8.2	1w	28
1N5236	7.5	500m	28	1N4742	12	1w	28
1N5242	12	500m	28	1N4744	15	1w	28
1N5245	15	500m	28	1N1183	50 PIV	35 AMP	1.60
1N456	25	40m	6/1.00	1N1184	100 PIV	35 AMP	1.70
1N458	150	7m	6/1.00	1N1185	150 PIV	35 AMP	1.70
1N485A	180	10m	5/1.00	1N1186	200 PIV	35 AMP	1.80
1N4001	50 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR(2N1849)	$1.95
C36M	35A @ 600V	SCR	1.95
2N2328	1.6A @ 300V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC.	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC.	1.95

TRANSISTORS

C106B1	.50			2N3904	4/1.00
MPSA05	.30	2N3055	.89	2N3905	4/1.00
MPSA06	5/1.00	MJE3055	1.00	2N3906	4/1.00
TIS97	6/1.00	2N3392	5/1.00	2N4013	3/1.00
TIS98	6/1.00	2N3398	5/1.00	2N4123	6/1.00
40409	1.75	PN3567	3/1.00	2N4249	4/1.00
40410	1.75	PN3568	4/1.00	PN4250	4/1.00
40673	1.75	PN3569	4/1.00	2N4400	4/1.00
2N918	4/1.00	MPS3638A	5/1.00	2N4401	4/1.00
2N2219A	2/1.00	MPS3702	5/1.00	2N4402	4/1.00
2N2221A	4/1.00	2N3704	5/1.00	2N4403	4/1.00
2N2222A	5/1.00	MPS3704	5/1.00	2N4409	5/1.00
PN2222 Plastic	7/1.00	2N3705	5/1.00	2N5086	4/1.00
2N2369A	4/1.00	MPS3705	5/1.00	2N5087	4/1.00
MPS2369	5/1.00	2N3706	5/1.00	2N5088	4/1.00
2N2484	4/1.00	MPS3706	5/1.00	2N5089	4/1.00
2N2906	4/1.00	2N3707	5/1.00	2N5129	5/1.00
2N2907	5/1.00	2N3711	5/1.00	PN5134	5/1.00
		2N3724A	.65	PN5138	5/1.00
2N2925	5/1.00	2N3725A	1.00	2N5139	5/1.00
MJE2955	1.25	2N3772	2.25	2N5210	5/1.00
2N3053	2/1.00	2N3823	1.00	2N5449	3/1.00
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22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.05	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075

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.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22 mf	.33	.27	.22

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.1/35V	.39	.31	.25	1.5/35V	.41	.33	.26
.15/35V	.39	.31	.25	2.2/35V	.51	.41	.33
.22/35V	.39	.31	.25	3.3/25V	.53	.43	.34
.33/35V	.39	.31	.25	4.7/25V	.63	.51	.41
.47/35V	.39	.31	.25	6.8/25V	.79	.63	.50
.68/35V	.39	.31	.25	15/25V	1.39	1.12	.89
1.0/35V	.39	.31	.25	22/6V	.79	.63	.50

MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead				Radial Lead			
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.14	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

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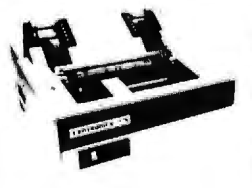

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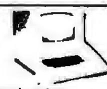

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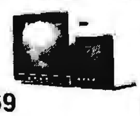

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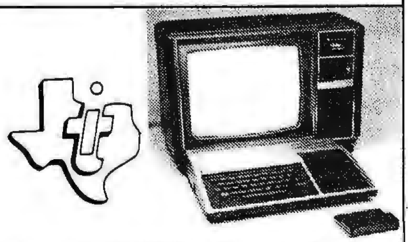

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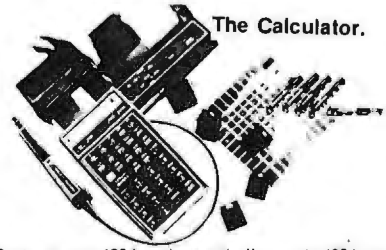

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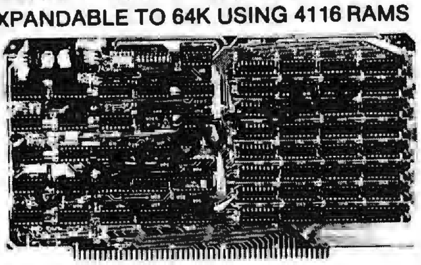

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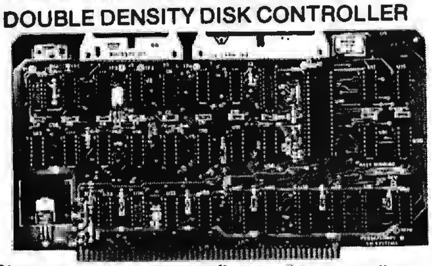

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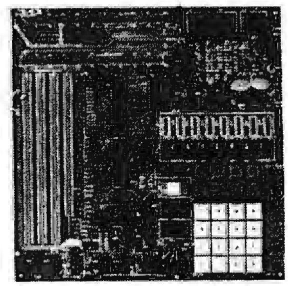

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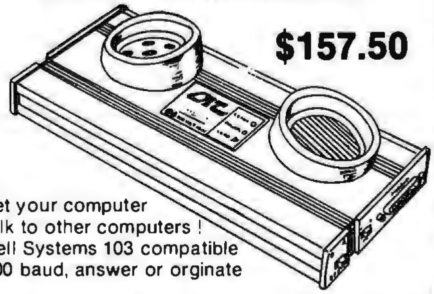

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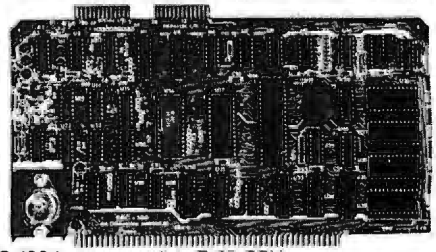

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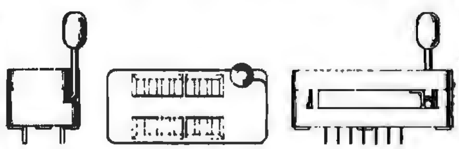

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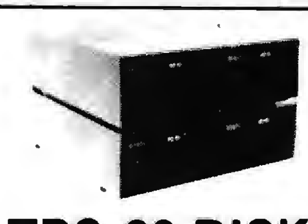

TRS-80 DISK DRIVE (CABLES INCLUDED)

TRS-80 I (5¼″)	$395.00
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APPLE II	$1550.00

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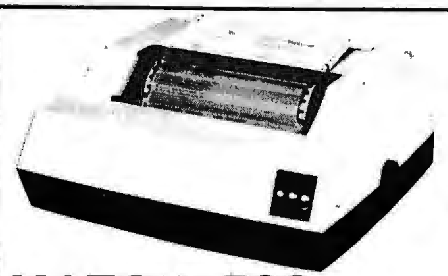

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FOR **APPLE** **$849.00
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**Includes parallel interface with documentation.
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4116-200 ns

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Z80 (2 MHz)	$10.95
Z80A (4 MHz)	$12.95
6502	$11.25
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6802	$19.50
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8035-8	$20.00
8080A	$ 3.95
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8086-4	$60.00
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8216	$ 2.95
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8238	$ 6.00
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8251	$ 7.00
8253	$19.00
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8257	$17.95
8259	$19.95
8275	$69.95
8279	$17.50
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21L02 (450 ns)
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2114L (250 ns) $5.50 ea.
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2513 (Lower case)	$10.95
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2513 Lower (5 v)	$10.95
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6571AP	$10.95

Look at these QT Values . . .

APPLE PRODUCTS

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WIZARD CONTROLLER for 8" Disk Drive	$360.00
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INTROL X-10 SYSTEM (turns appliances on/off)	$275.00
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AIO/Serial-Parallel Board A&T	$155.00
INTEGER Firmware Card	$179.00
PARALLEL INTERFACE CARD	$90.00
VISICALC(Business Software Package)	$124.95
SUPER-MOD II (connects Apple to TV)	$25.00
ROM WRITER (Epromburner) Mountain Hardware (order)	$175.00
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APPLE CLOCK	$280.00
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VB2 I/O Mapped Video Interface	$29.95
IO2 Parallel I/O Interface	$34.00
IO4 2P + 2S I/O Interface	$28.95
SB1 Music Synthesizer	$39.95
OB1 Vector Jump & Prototyping Board	$29.95
MB6B 8K Static RAM	$25.95
MB7 Low Power 16K Static RAM	$26.95
MB8 4K 1702 EPROM Board	$29.95
MB8A 16K 2708 EPROM Board	$34.95
T1 Terminator	$26.00
MTI 15 Slot Motherboard	$45.00
XB1 Extender Board	$13.50

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AIO Apple Parallel Interface Firmware	$25.00
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Paper Tape of MUS-X1 Interpreter	$ 9.00
CP/M Compatible 8" Disk, containing • MUS-X1 Music Interpreter • Test Program • 18 Encoded Music Selections	$25.00
SB1 Booklet (with 21 Encoded Music Selections)	$10.00
Manuals	
SB1 Music Synthesizer Manual	$10.00
All Other Manuals	$ 5.00
100 Pin edge connector (short st)	$ 3.00
100 Pin edge connector (standard ww)	$ 4.00
Card Guides	$ .15

S-100 KITS & ASSEMBLED BOARDS

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Assembled & Tested	$199.95
PB1 2708/2716 EPROM Programmer	
Kit with Textool sockets	$124.95
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Kit	$125.00
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Upgrade Kit for 80x24 Display	
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4 MHz	$ 89.00
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Kit	$ 59.00
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Kit	$129.95
Assembled & Tested	$189.95
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Assembled & Tested	$279.00
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Kit	$129.95
Assembled & Tested	$149.95
250 ns RAM	
Kit	$159.95
Assembled & Tested	$224.95
MB7 Low Power 16K Static RAM	
Kit	$269.96
Assembled & Tested	$375.00
CB2 Z-80 CPU	
Kit	$185.95
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MB3 4K 1702 EPROM Board	
Kit - without EPROMs	$ 85.00
Assembled & Tested	$125.00
MB8A 16K 2708 EPROM Board	
Kit - without EPROMS	$ 85.00
Assembled & Tested	$139.00
T1 Active Terminator	
Kit	$ 34.00
Assembled & Tested	$ 64.00
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Kit (with Connectors)	$129.95
Assembled & Tested	$149.95
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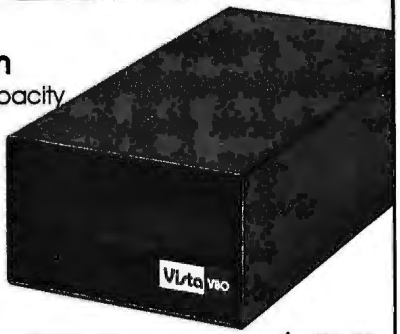
The VISTA V-80 Disk Drive System

- 23% more storage capacity than TRS-80
- 120 day warranty
- 40 track patch at NO CHARGE



Single drive system	$ 395.00
Two drive system	$ 770.00
Four drive system	$ 1450.00
Two drive cable	$ 29.95
Four drive cable	$ 39.95

The VISTA V-80 Expansion Module

- Provides double density modification to your current Radio Shack interface (lets you format diskettes in either single or double density).
- Increases storage capacity up to 204K bytes (on single 40 track drive).
- Includes all hardware and software.

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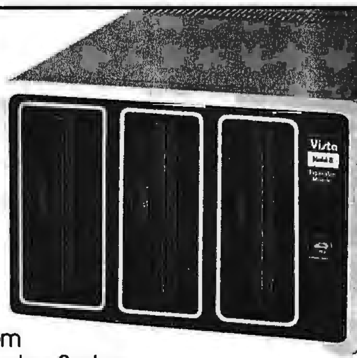
The VISTA Model II

- Provides one, two or three drives.
- Adds up to 1.5 million bytes of on-line storage.
- 120 day warranty
- Does everything Radio Shack's expansion system will do...for less!



$1000.00	Single drive Expansion System
$1550.00	Two drive Expansion System
$2100.00	Three drive Expansion System
$ 525.00	Additional drives alone

The TRS-80 Printers

Centronics 730... **$945.00**
7x7 dot matrix-
80 column

Anadex
DP8000... **$895.00**
9x7 dot matrix-
80 column

VISTA
Printer... **$745.00**
5x7 dot matrix-
80 column

Cables..................... **$27.50 each**

Other Products

1. VISTA Verbatim diskettes (hard or soft sector) Certified 40 track .... $ 38.95
2. 16K RPM upgrade kits, guaranteed for 120 days. **PRIME PRODUCT** .... $ 74.50
3. NEW! DOS + ... $ 110.00
4. LNW expansion bare board .... $ 66.95
5. H.C. Pennington book, **TRS-80 Disk and Other Mysteries** .... $ 18.95
6. DDT Disco-Tech disk drive timer .... $ 19.95
7. Cryptext (An Encryption Module)................ $299.00

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MPI B51	40 Track, Double Density-204K	$275.00
MPI B52	Dual Head, Double Density-408K	$375.00
Siemens	FDD100-5 40 Track Double Density 204K	$275.00
Siemens	FDD100-5 Flippy, records both sides	$290.00
Siemens	FDD100-8 8" Single Sided Drive	$448.00

The VISTA V-200 for Exidy

- Completely packaged system, tested and ready to plug in, includes: power supply, two 40 track drives, case, controller, all cabling and total CPM documentation.
- Storage capacity from 400K to 1.2 meg.
- System software-VISTA CP/M Disk Operating System and BASIC-E Compiler recorded on 5-1/4" diskettes.

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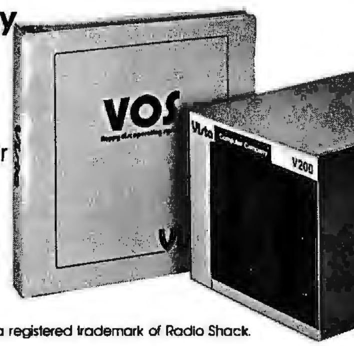

Vista

CALL TOLL-FREE 800-854-8017

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The Vista Computer Company 1401 Borchard Street • Santa Ana, California 92705 • 714/953-0523

Circle 275 on inquiry card.

Unclassified Ads

FOR SALE: Ohio Scientific Challenger 2P, Sup'r'mod II TV interface, and cassette recorder ready to hook up to your TV or monitor. Original cost $750, will sacrifice for $575. First certified check or money order gets system, manuals, and programs. R A Post, 9111 Pawnee Ln, Leawood KS 66206.

FOR SALE: Expandor Black Box printer with base and cover, $385. Also, ESP-I on disk, $20. Paul G Kuty, Old County Rd, Francestown NH 03043, (603) 547-2777.

WANTED: TRS-80 programs wanted to swap; Level 2. Write or send tape to G M Fuller, 16 Maryburn Rd, Twizel, NEW ZEALAND.

SORCERER USERS: I am a games fanatic and have many games programs. Will trade one for one. Send cassette with game and receive another. I am specially interested in graphics and machine-language programs. I will also help with or exchange ideas on any other original programs. I have university degrees in computing and math. Send program (preferably airmail) to Paul Balin, 19 Starkey St, Forestville, NSW 2087, AUSTRALIA.

WANTED: Correspondence with people using systems based on Intel's SBC 80/10; specifically those interfacing the SBC with a floppy disk and/or using CP/M and Pascal. J Scott Nintzel, 3843 Granada Ln N, Oakdale MN 55109, (612) 770-6926.

FOR SALE: Set of BYTE magazine from first issue to present; complete except for issue number 11, August 1976. Peter Ricke, 1383 Rockland, POB 546, Calumet MI 49913, (906) 337-0180.

FOR SALE: PET 8 K computer with keyboard, video display, and cassette interface storage. Brand-new condition. Must sell. $350. Bruce Tempone, (215) 446-8693 after 6 PM ET.

WANTED: I would like any free booklets, pamphlets, catalogs, or brochures on computers and electronics. Anthony Atella, 269 Beckwith St, Cranston RI 02910.

FOR SALE: TRS-80 computer. Level II/16 K with numerical keyboard. Includes game tapes for blackjack, backgammon, and Microchess. Also, a tape which allows the computation of elliptical and parabolic orbits from three positions, elliptical orbit from four positions, and elliptical and parabolic positions from elements. Instructions included. $650. You pay shipping. Brian Warner, Rt 3, POB 603, Mullins SC 29574

FOR SALE: KIM-1 with cassette recorder, power supply, and all documentation. Includes Microchess and other game software on cassette. Works perfectly. $140 or best offer. Jeff Thompson, 1700 Washington Creek Ln, Dayton OH 45459, (513) 435-3169.

FOR SALE: Benrus video display module. 7 by 5 by 17 inch module contains 6 by 10 cm high-frequency video display, X and Y amplifiers (sensitivity .1 V/cm), z-axis modulation, and high-voltage supplies. Completely transistorized, operates from 110 VAC. High-frequency response extends beyond 30 MHz. Excellent for computer graphics or for construction of a high-frequency scope; used, excellent condition, $100. Also, have limited number of 4027, 250 ns 4 K by 1 dynamic programmable memories equivalent to 4096 and 2104A; $1.50 each. M Bickerton, 2631 Wharton St, Philadelphia PA 19146, (215) 467-3549.

FOR SALE: Apple II computer with 48 K, 250 ns programmable memory, disk with controller, three boxes of diskettes, all original manuals, and programs in original container. Less than three months old, barely used, in perfect condition. A lot of software included. Original cost over $1800. Will sacrifice at $1500. Chase Roh, 1803 Old Maple Ln, Savoy IL 61874, (217) 356-1900 or 398-0700.

WANTED: Back issues of the *Radio Shack TRS-80 Microcomputing Newsletter.* I will pay $0.50 an issue plus postage. Send information on the issues you have. David Fischer, Branch POB 1394, Rome NY 13440, (315) 339-1037 days.

FOR SALE: ELF II system with full BASIC and 12 K programmable memory. Also included: ASCII keyboard, video display board, Giant Board, 5 A power supply, cassette recorder, and full documentation. Plus cabinets for ELF II and ASCII keyboard. $825 for complete system, plus shipping. Will throw in Tiny BASIC and Short Course programming manuals, plus game cassette package. Kevin Mast, 308 Jackson Ave, Defiance OH 43512, (419) 782-6147.

FOR SALE: Cromemco multichannel microcomputer analog interface kit (new, unassembled in original packing) Model D-7AI/O. Original price $145; first offer over $40 gets it. I will pay postage. V Roningen, 4707 9th St S, Arlington VA 22204, (703) 521-1451.

FOR SALE: Heathkit H8 with 16 K of memory and serial input/output (I/O). Also includes Info 2000 dual 8-inch disk drives and controller. Disk controller upgrades system to a Z80 and runs under CP/M. By flipping a switch, system will run under Heath cassette software (two cassette drives included). Includes many extras, too. $1000 takes all plus a bonus of an H10 paper-tape reader/punch free. R Nicosia, 234 41st St, Lindenhurst NY 11757.

FOR SALE: AIM-65 microcomputer system. 4 K programmable memory. Assembler/Editor read-only memory. Standard enclosure. Extra paper. Excellent condition. Hardly used. $480 or best offer. David Kusek, POB 24, Storrs CT 06268, (203) 429-0600.

FOR SALE OR SWAP: Okidata CP110 matrix bidirectional printer. Upper and lowercase with Centronics-type interface. Takes Teletype-style roll paper. Comes complete with service manual, thirteen extra ribbons, and about $90 extra paper rolls. Printer itself sells new for about $1800. Will sell all for $500 FOB Berkeley. Or will swap for heavy-duty (Model B I/O writer?) IBM Selectric. Dick Blumenstein, 202 Stanford Ave, Kensington CA 94708, (415) 524-5666.

WANTED: People in the San Francisco Bay Area interested in creating an outstanding, alternative computer network and information resource—user owned and run. Billy Smith, 2325½ Howe St, Berkeley CA 94705, (415) 848-0884.

WANTED: Word processor in good working condition. Will consider Wang, CPT, Ty-Data Series 3600, Quintype 70, or others. Also, need Friden Justowriter and Flexowriter. Give price, age, all pertinent details. Albert Pile, R R 1, Box 67, Bardstown KY 40004.

FOR SALE: IBM Selectric Model 735 input/output writer. Can be used as a typewriter or computer terminal. Excellent condition—recently refurbished by IBM. Uses Correspondence Code (easily converted to BCD or ASCII in hardware or software). Includes user manual and complete computer-interface instructions. $425 plus shipping. Video monitor: Ultronic Videomaster 12-inch high-resolution (15 MHz) raster display. Excellent condition, with circuit diagram. $60. Joe Blau, 2344 Evergreen St, Yorktown Hts NY 10598, (914) 245-1015.

FOR SALE: 4 K programmable-memory circuits. Thirty-two UPD414D (Mostek MK4015N) from converting two Exidy Sorcerers from 8 K to 32 K. Make me an offer for some or all. Steven Larky, 2423 Nottingham Rd, Bethlehem PA 18017.

WANTED: Dental software for the Apple II. Anything that can be used in a dental office. Interesting games, too. Dr Kahn, 51 Upper Sheep Pasture Rd, Setauket NY 11733.

FOR SALE: TRS-80, Level 2.2 with 32 K, expansion interface, Radio Shack disk, power supply, keyboard, cassette unit, manuals. Software includes Invasion Force, Business Income Tax Package, and eleven diskettes all in perfect condition. Shipped prepaid. $1850. Jim Handy, 2102 Courtland Cir, Carrollton TX 75007, (214) 492-3670.

WANTED: Software in the scientific, business, engineering, and technical fields that has been written, adapted, purchased, and/or tested to run on the new HP-85 in 16 K or 32 K. I am a new owner and would like to trade information about using various peripherals with the HP-85. Dan Berkeley, POB 2972, Littleton CO 80161, (303) 781-0320.

FOR SALE: ASR33 Teletype keyboard-printer terminal with tape reader-punch. Fully operational with documentation and could be interfaced to any computer. With stand, $450, or without stand, $400. Shipping extra. Patel, 418 Guild Hall Dr, Columbia SC 29210, (803) 781-5647.

FOR SALE: Ohio Scientific Challenger 1P, 8 K of programmable memory. Javelin video display monitor. Cassette recorder and twelve programs included. $450 for the entire system. Ben Galewsky, 1035 Dowlen Rd, Beaumont TX 77706.

FOR SALE: Programmable memory for S-100 bus systems. Ithaca Audio 8 K programmable memory; $100. Also, an 8 K programmable-memory board by Quantronics Problem Solvers, with phantom line; $125. A 2708 programmable read-only memory programmer by Optimal Technology; $40. Hal Skurnick, 14 LeRoy Pl, Chappaqua NY 10514, (914) 238-4961.

FOR SALE: Brand-new microcomputer. Commodore PET 2001-8 with 32 K and video display. Best reasonable offer. John W Cook, 8670 Tanglewood Trl, Chagrin Falls OH 44022, (216) 543-7785.

FOR SALE: KIM-1 with power supply, 1 K programmable memory, 2 K read-only memory, user manual, wall-size schematic, hardware manual, programming manual plus *Programming a Microcomputer: 6502.* Asking $125 or best offer. Ed, (617) 544-2207 in PM.

FOR SALE: Tektronix 4051. 32 K programmable memory. All manuals included. $3000. Jay Ross, POB 247, Ortonville MN 56278, (612) 839-6181.

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Please note that it may take three or four months for an ad to appear in the magazine.

March BOMB
Ciarcia Wins With Ease

"Ciarcia's Circuit Cellar" continued as the best-liked feature in the BOMB voting, as Steve Ciarcia won again with his article "Ease into 16-Bit Computing" (page 17). It placed 2.30 standard deviations above the mean. Steve will take home another $100 first-place prize. Second place in the tally went to Editor-in-Chief Chris Morgan for his article "Hewlett-Packard's New Personal Computer, The HP-85" (page 60), which had a standard deviation of 0.91 above the mean. Third place was taken by James R Lewis for "TRS-80 Performance, Evaluation by Program Timing" (page 84), and fourth place was taken by D Martin Harrell for "Operation Codes for 8080, 8085, and Z80 Processors" (page 194.)■

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