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the small systems journal

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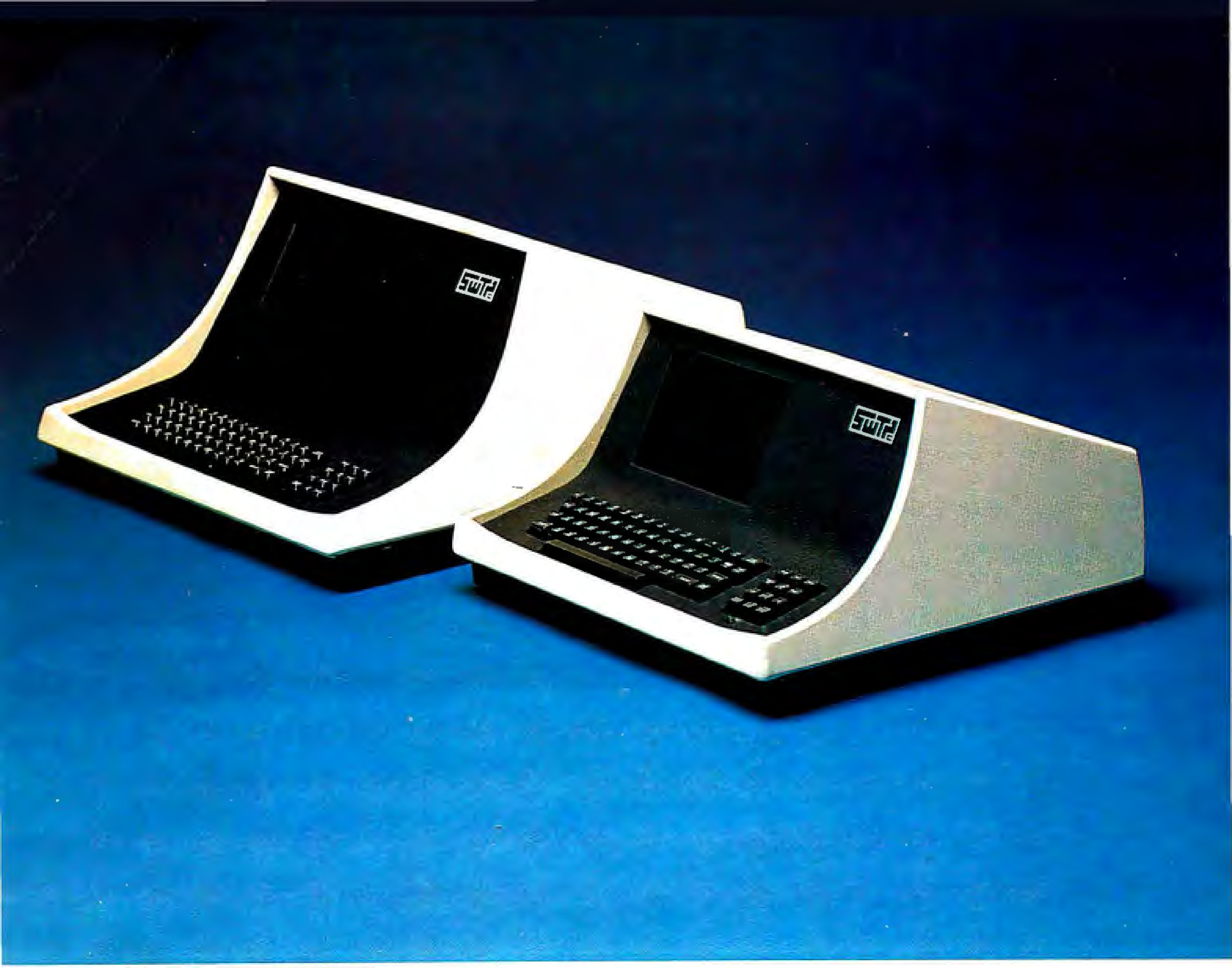
PROGRAMMING METHODS



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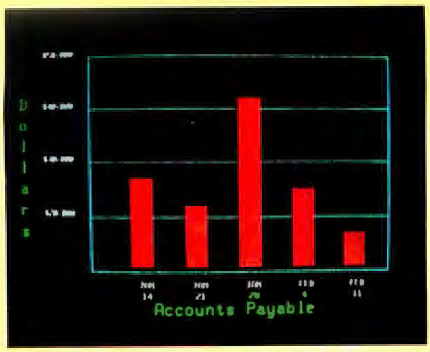

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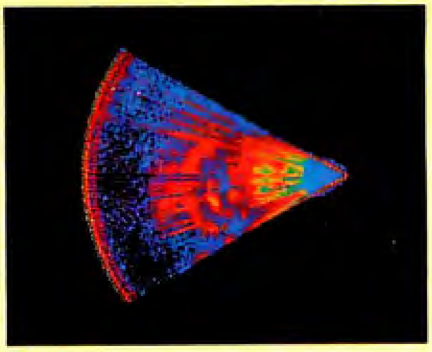

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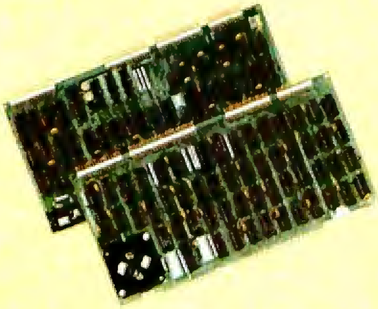

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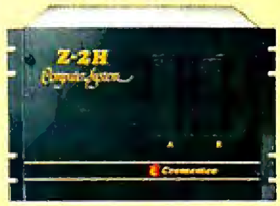

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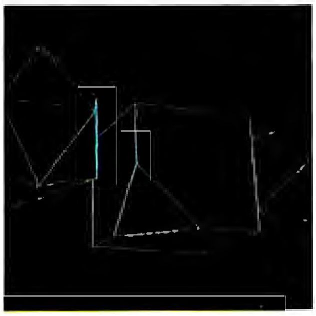

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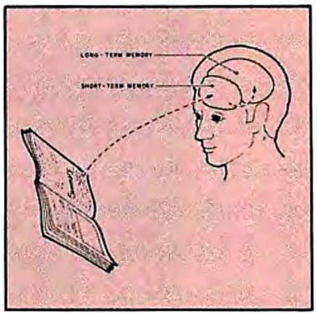

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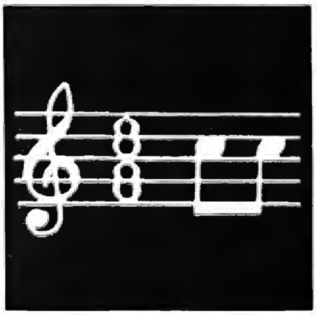
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In This Issue

Do you have trouble making all the pieces fall in place when you are writing a new program? Robert Tinney's cover this month symbolizes the theme of programming methods. But the symbolism is only pictorial—the process of designing and putting a new program together is often much harder than assembling an intricate jigsaw puzzle. This issue includes several articles on different aspects of programming and design: "What Is Good Documentation?" by Jim Howard; "Structured Programming and Structured Flowcharts" and the editorial, "Is This Really Necessary?", both by Editor Gregg Williams; "A Coding Sheet for FORTH," by John O Bumgarner; and "A Simple Approach to Data Smoothing," by Fred Ruckdeschel and Janice A Krinsky.

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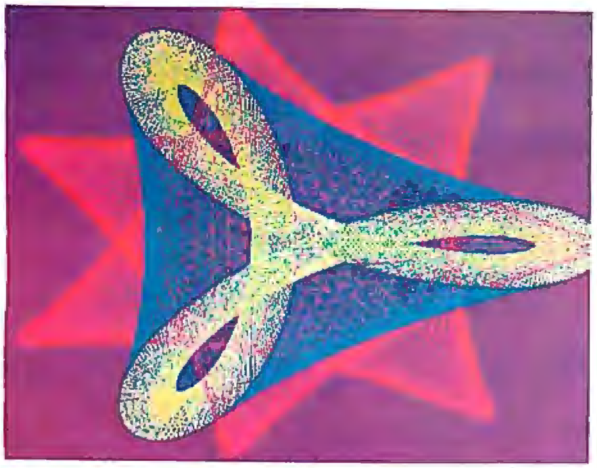

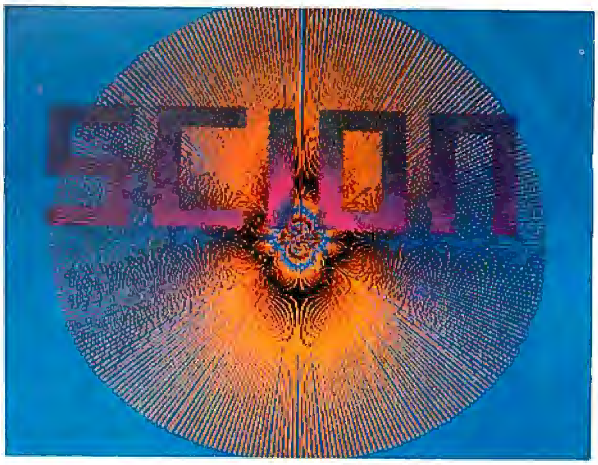

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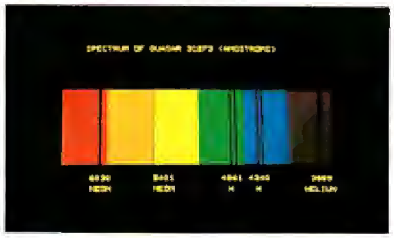

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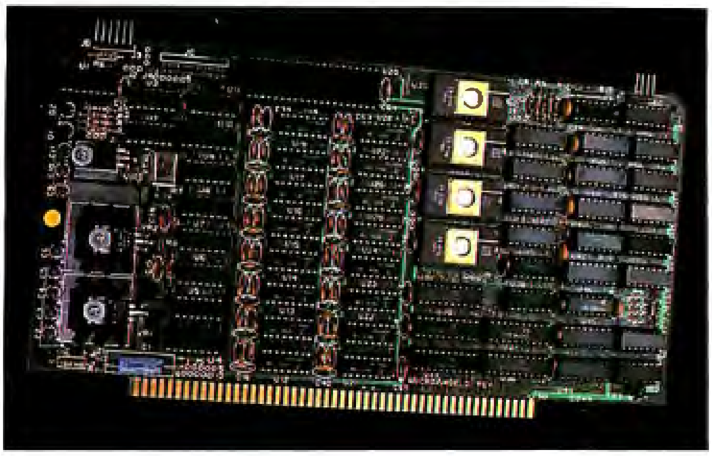

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Editorial

Is This Really Necessary? A First Look at Design Techniques

Gregg Williams, Editor

Complete the following sentence:

> When I start programming, the first thing I do is ______________________.

Some people draw flowcharts. A few adventuresome—usually foolhardy—souls type in lines of BASIC directly on their computers. Most of us start by scribbling and sketching on sheets of paper. However, is that enough? Perhaps so, if you're writing for yourself; but if anything important is at stake—time, money, or reputation—you probably need to spend more time designing.

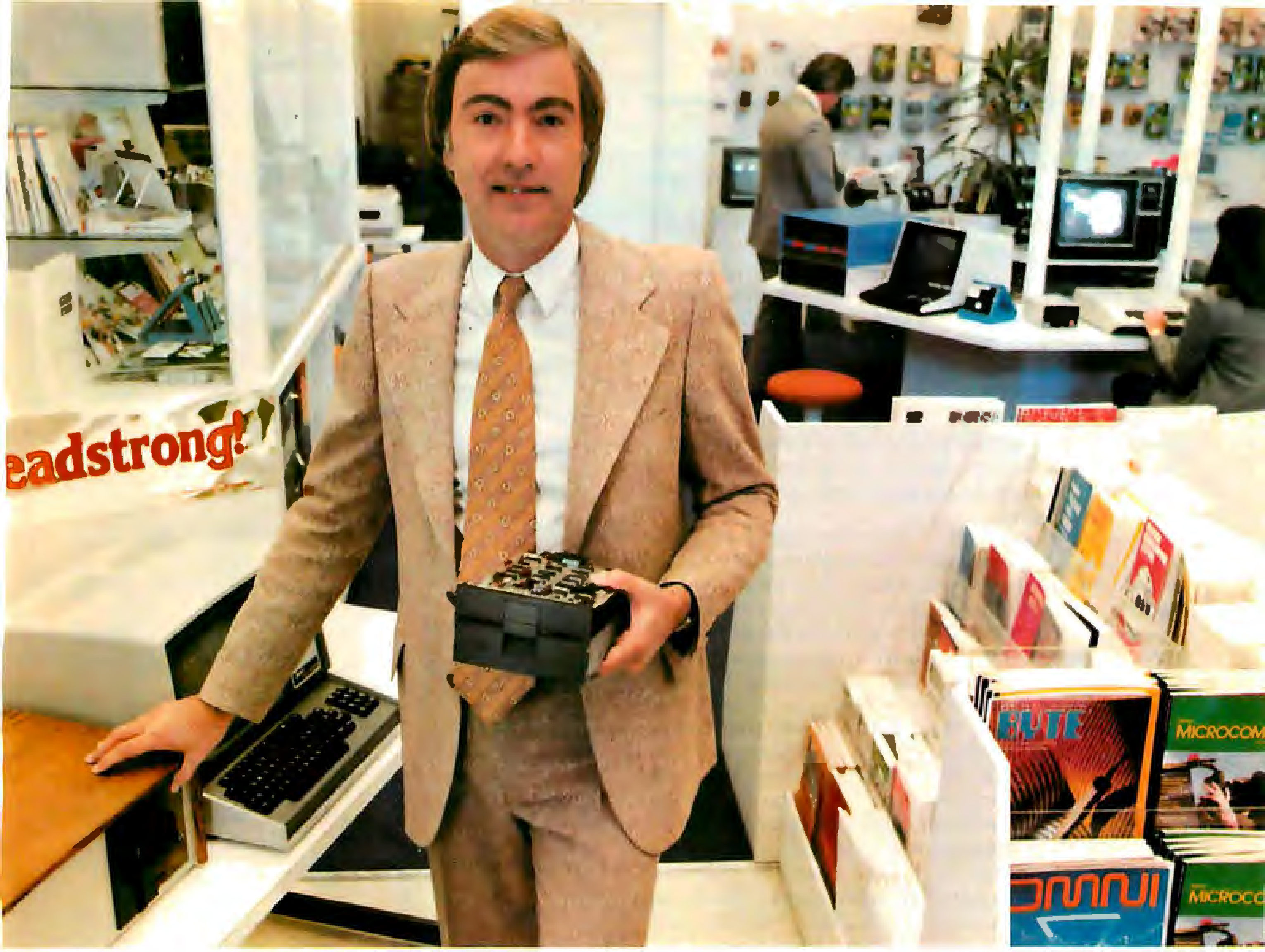
In this editorial, I'll show you what design is, why you need it, and how it works. I'll also present some new design tools (of which there are more and more every day), a design example, and a sampling of good books on design and programming. I promise to stay as far away from the concept of "structured programming" as possible. Much has been written about it elsewhere. I want to concentrate on what happens *before* you start programming.

What Is Design?

Webster's New Collegiate Dictionary defines *design*, the verb, as "to conceive and plan." As a noun, a design is "a preliminary sketch showing the main features of something to be executed." In terms of programming, design becomes proportionately more important depending on the size of the problem: We speak of *program design* when we write a game program for ourselves, *project design* when we design and write an accounting system on an existing computer at work, and *system design* when we draft a proposal for a hardware/software combination that will implement a given set of requirements for a data base system. (Actually, "system design" is used in the literature to describe the design of anything larger than one program; but I wanted to make a distinction between project design and system design because of the widely varying amounts of work they require.)

In designing and writing programs, I've found that the point dividing system design from program design is the point at which I have specified the function of the program and its use of computer resources (eg: are records stored on disk in a random-access file and called as needed, or are they read into memory before any processing is done?). *After* this point, I am designing the program (usually a fairly straightforward—though nontrivial—process). *Before* this point, I'm making certain critical decisions that strongly influence the requirements and performance of the proposed implementation of the program. In this sense, such decisions will often need to be made even when I'm designing and writing a single program. I can then see that both *system* design and *program* design have enough in common so I can eliminate the modifier and speak simply of *design*. I can safely say then that *design is concerned with making a set of performance-related decisions and specifying the program(s) that implement them.*

(An integral part of design, of course, is *documentation*. Documentation of the overall design should be followed by documentation of the program design and its implementation. The finished documentation package, which should clarify both the organization of the system/project/program and the details of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the program(s) involved, will be of immense help to you, or anyone else, during debugging, testing, and maintenance.)

To put the role of design in perspective let's look at the lifespan of a medium-sized system:

- **(System) Design:** This is the step I talk about in most of this article. It includes finding out what the problem is, devising alternative schemes to solve it, deciding on the one that (you think) will result in the "best" implementation, and filling in the design details with regard to the items that go into the system (input), the manipulations made on these items (process), and the results that are generated by the system (output). By the end of this process, you will have divided the entire system into programs and specified the input, process (what, not how), and output of each one.
- **Program Design:** This is where structured programming is used. You know what the program is supposed to do and what computer resources are to be used; now you must fill in the details of *how* its objectives are to be accomplished. It is commonly accepted that the best way to design a program is to repeatedly break the task to be accomplished into subtasks, until each subtask is simple enough to be programmed in the language you are using. Note that the design process ends without your having written *any* lines of computer code. In this step, you are simply filling in the details of what the program is to do without worrying about the particular syntax of the computer language you will use. (There are numerous design notations to help in this process. The two I like most are *structured pseudocode*, described below, and *structured flowcharts*, which is described in my article, "Structured Programming and Structured Flowcharts," on page 20 of this issue.)
- **Coding:** This is what most people call "programming," even though they are referring to the entire design/coding process. Coding is the specific act of translating a program design into the particular syntax of the computer language you are using (often called the *target language*). The more detailed the design is, the more coding becomes a rote task. The completeness of the design is determined by several factors. These are: how well you think you know the application being programmed and the computer language used, how important it is to get the program right the first time, and how many surprises (mostly of the "oops, I forgot to..." kind) you can tolerate during

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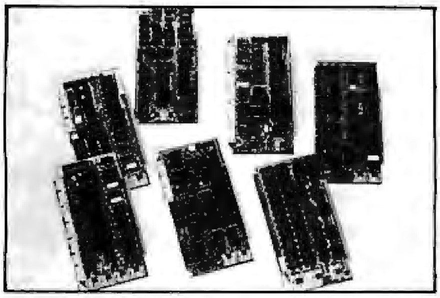

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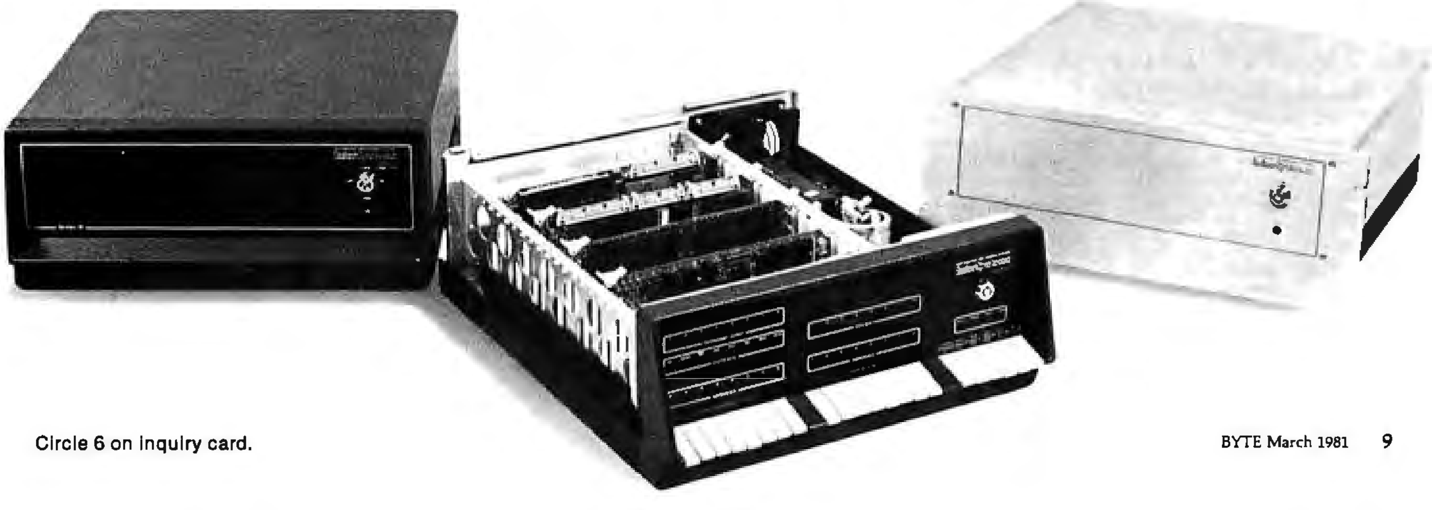

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coding. In most informal situations (ie: when you're not programming for hire), a sketchy design provides an acceptable compromise between no design and a rigorous design.

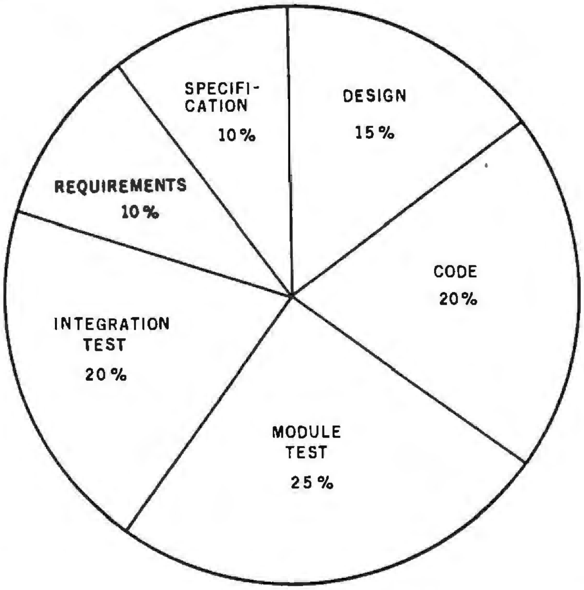

Figure 1: *A pie chart giving average percentages for activities within the process of designing, writing, and testing a program. The chart does not include maintenance of the program, which is estimated to take twice as much time as design, writing, and testing.*

- **Testing and Debugging:** This section is actually two intertwined processes—*testing,* the search for errors (both syntactic and logical), and *debugging,* the elimination of those errors. Most programmers estimate that this process can take as much time as both designing and coding. The results in figure 1 (by M V Zelkowitz in " Perspectives on Software Engineering," *ACM Computing Surveys,* June 1978, page 198) support this conclusion. The amount of needed debugging and testing greatly increases depending on the program's size and importance. It decreases with the amount of design and structured programming carried out before the coding. In a multiprogram system, programs are first tested and debugged (labeled "module test" in figure 1), then the entire system is tested and debugged (labeled "integration test" in figure 1).
- **Maintenance:** This section applies mostly to large programs for personal use and systems that are used in a work environment. Maintenance runs the gamut from fixing the occasional (or not-so-occasional) bug, to adding new features, or to moving a system of programs to an entirely new computer system. It's been estimated that maintenance occupies up to 90 percent of a (professional) programmer's time. Fortunately, most personal computer users don't have to carry this burden.

Why Designing Is Necessary

Whether we like it or not adventures begin only when something unexpected happens. In fantasy, adventures are always positive and exciting; in real life and in programming, they are usually unwanted, inconvenient, and sometimes costly or dangerous. Only short personal programs can squeeze by without some basic design work behind them. If the program gets longer, or if you are writing for somebody else (either friends or employers), you probably can't afford a programming "adventure." Remember that the design process includes finding and making decisions that influence the quality of a program or system. In other words, *the more important it is to write the best program, the more design you need to do.*

Here are some reasons that argue strongly in favor of well-thought-out design:

- Limited resources (eg: not enough computer memory or disk space, or a slow system response time)
- Time/money constraints (ie: the need to complete a program or system within deadline and under budget)
- The need for increased reliability
- The need for program stability and flexibility in the face of long-term maintenance

In addition to contributing to the quality and reliability of a program, design also contributes to your mental health as a programmer—you usually *save* time when you design; you eliminate all-night emergency programming marathons; the process of testing and debugging is shorter and less nerve-racking; and you're less likely to have your program "crash" at an embarrassing or crucial moment.

Some Popular Excuses, and Rebuttals

"I don't know where to start": Read some of the books

Text continued on page 200

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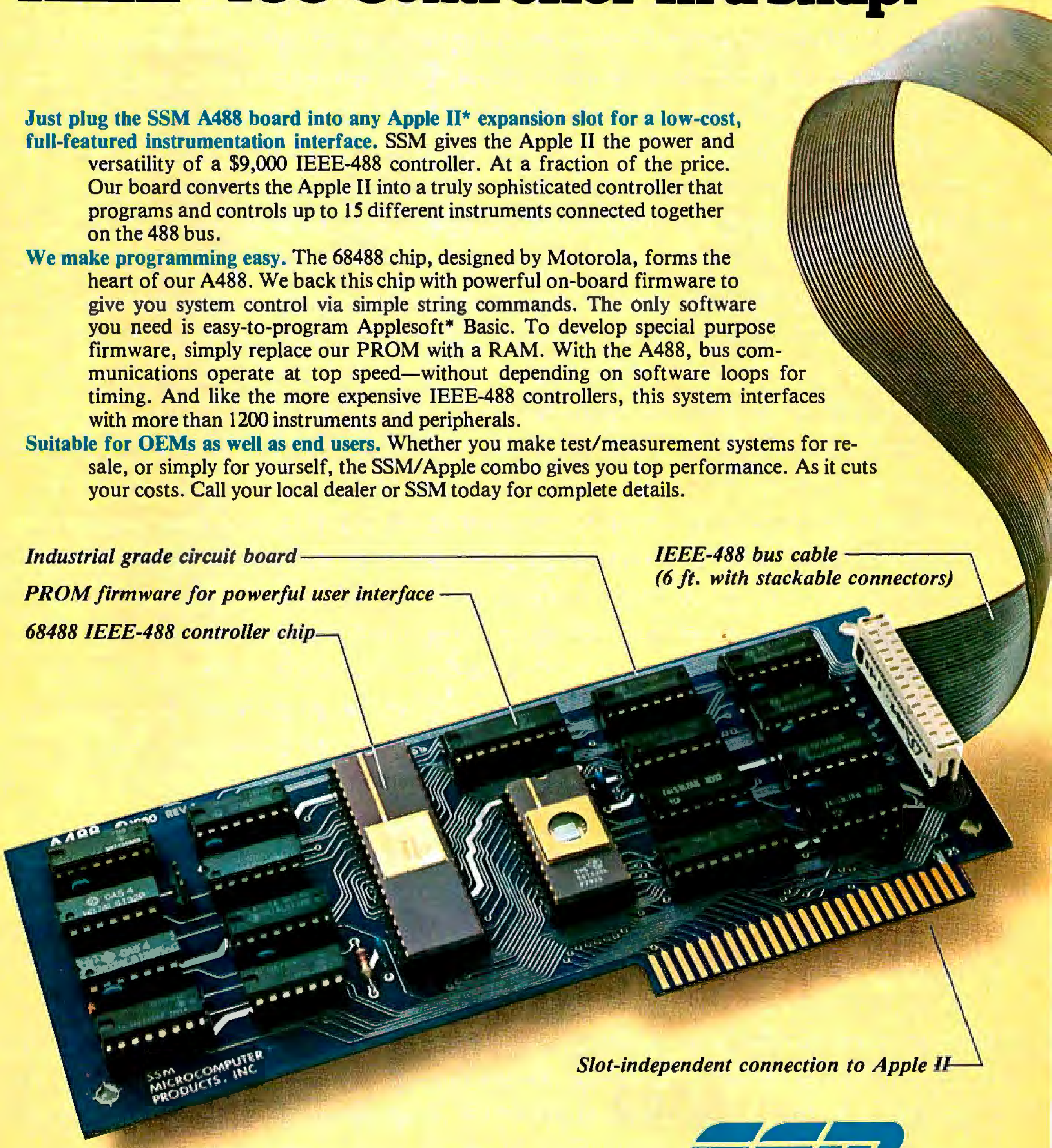

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Letters

On Technical Writing

I enjoyed Chris Morgan's editorial on technical writing ("What's Wrong with Technical Writing Today?" December 1980 BYTE, page 6), but there is a sad exception to his first law: Academics can benefit from not writing clearly. I suggest a paper by J S Armstrong in the April 1980 *Interfaces*, published by The Institute of Management Sciences.

Armstrong, from the Wharton School, found that material more difficult to read was rated higher in research competence. "Management scientists gain prestige by unintelligible writing." My wife, an academic biologist, and I have seen similar hypotheses about academic publishing in computer science. (*Communications of the ACM* may be a perfect example.)

Since such "news" would only undermine the effort you folks are making at BYTE, you must keep all this a secret.

Gerald Ruderman
Management Decision Systems Inc
300 Third Ave
Waltham MA 02154

In the December 1980 editorial, Chris Morgan says that "Jargon isn't intrinsically bad...."

Ha! I caught you. Jargon *is* intrinsically bad; it may be necessary sometimes—an evil necessity—but it's always bad. I've often wondered if those who edited BYTE were in favor of jargon. Now I know.

Like many aspects of our society, jargon has two purposes: an obvious one, and a hidden, unadmitted one. The obvious purpose is to save space, as Mr Morgan pointed out. The hidden one is to exclude outsiders from the circle of the insiders.

To use jargon in explaining the workings of a particular product would be justifiable in a manual directed toward sophisticated, knowledgeable professionals, if the product were released in a specific, well-known context. An example is all the funny words people familiar with IBM equipment always use. Such an approach in a journal like BYTE is entirely inappropriate.

The distinctive difference between BYTE and some of its less successful competitors is that many BYTE articles, even though written in jargon, try to explain something, while too many articles in other magazines use jargon purely for the purpose of mystifying.

Jargon may have many purposes, but the rapid, effective spread of information is not one of them. If you really wish to communicate ideas, *write in English*—or some common human language.

The balance of Mr Morgan's editorial was actually quite to the point. I'd like to add, "DON'T use big concepts when small ones will do."

James Gregor Owen
14 Ocean Dr
Freeville NY 13068

*The December editorial apparently struck a nerve among readers, judging from the comments we received. Mr Owen raises a point I did not cover: the "high priesthood" syndrome that arises when a writer sets out to impress and mystify through jargon. At BYTE, we wage a (not always successful) battle against this philosophy, and hope that our readers will continue to tell us when we go astray. I'd also like to thank the editors at General DataComm Industries Inc, Danbury, Connecticut, and several other readers who caught some minor gaucheries in my editorial. Oh, the irony of it....*CM

Intel's Educational Products

As the manager of Intel Corporation's Educational Products Group I would like to thank BYTE for suggesting our company as a source for blemished components. Steve Ciarcia's reply to an "Ask BYTE" letter has generated a large response from students and educators. (See "Quick and Cheap," December 1980 BYTE, page 320.) In order to help BYTE's readers to more fully benefit from our program, I would like to bring some additional information to their attention.

The Educational Products Group has the responsibility for the administration of the component kit program. To avoid delays of up to 4 weeks, all inquiries should be directed to us, not the product manager.

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instead we offer a broad line of kits based upon the 8085, 8048, 8086, and 8088 microprocessors. The 8086 and 8088 kits include a serial monitor. Kit prices range from $35 up to $90, and each contains enough components to construct a minimum system.

Intel is in the process of expanding the program, and we publish a quarterly magazine to let prospective members of the academic community know of these developments.

Please contact us if you would like more information on how we can help you. Our telephone number is (408) 987-5020.

Steven A Lapham
Manager, Educational Products
Intel Corporation
3065 Bowers Ave
Santa Clara CA 95051

Intertec Responds to Criticism

In response to Mr Phillip Lemmons's letter (see "Superb Brain," October 1980 BYTE, page 22), I would like to make the following observation. We at Intertec disagree with his analysis of the situation and feel that clearing up the facts would be a benefit to Intertec and our users alike.

Everyone must realize that nothing remains static in the computer industry. New ideas constantly emerge, resulting in a stream of new developments. The continual upgrading of technology, and the subsequent evolution of computer software and hardware, is the basis of high technology as all of us know it today. As responsible manufacturers, we feel obliged to pass on these technological advancements to our users.

As improvements are added to our products, we offer our previous customers, whenever feasible, an upgrade option at nominal cost. If the modification cannot be accomplished with a simple EPROM change, for instance, we still feel a responsibility to offer some kind of solution to our customers.

Such is the case with Mr Lemmons's "$1500 enhancement." The modifications to which he refers involved changing the whole unit: processor module, power supply assembly, disk drives, etc. In January 1980, the SuperBrain was modified to offer even more capabilities than our advertisements claim. Therefore, had Mr Lemmons purchased this enhancement, he would, in effect, have received a completely new unit for $1500—half the end-user cost for the same unit.

As for the software problem Mr Lemmons referred to, we are confident that an EPROM update costing $100 would have taken care of his problems. Mr Klein of Information Engineering sold it to him for $150. Admittedly, Mr Lemmons may have received this update a little sooner than he would have had he purchased directly from the factory; nevertheless, the EPROM is available from us.

For an end-user price of $2995 for our basic SuperBrain model, we think (and we have thousands of testimonials from happy SuperBrain users to support this) that Intertec offers the best price/performance ratio in the industry.

If any other BYTE readers have problems similar to Mr Lemmons's, please call our Product Services department at (803) 798-9100. Our staff of application engineers will be glad to assist you in any way possible.

At Intertec, the customer has always been (and still is) our main concern. Our phenomenal growth in recent years would not have been possible if we did not hold steadfastly to this simple management principle. We hope Mr Lemmons (and any others who may be dissatisfied with us) will understand our point of view and give us a chance to demonstrate the sincerity of all of our customer-support programs.

Denise Stevens
Marketing Communications Manager
Intertec Data Systems
2300 Broad River Rd
Columbia SC 29210

Hurray for muSIMP

I recently purchased muSIMP/muMATH for my Radio Shack TRS-80 Model I, so I was interested in Gregg Williams's review in the November 1980 BYTE. (See "The muSIMP/muMATH-79 Symbolic Math System," page 324.) The version I purchased is the small, inexpensive TRS-80 version, which does not include the trace, array, and matrix packages.

While the discussion of muMATH was complete, I was disappointed that Mr Williams only touched briefly on the capabilities of the underlying muSIMP language used to implement muMATH. The introduction of a low-cost version (or any version) of LISP for the TRS-80 should be marked as a major development. muSIMP is a close cousin of LISP, and, in this light, muMATH is seen as a powerful illustration of its capabilities. The impressive achievements of muMath

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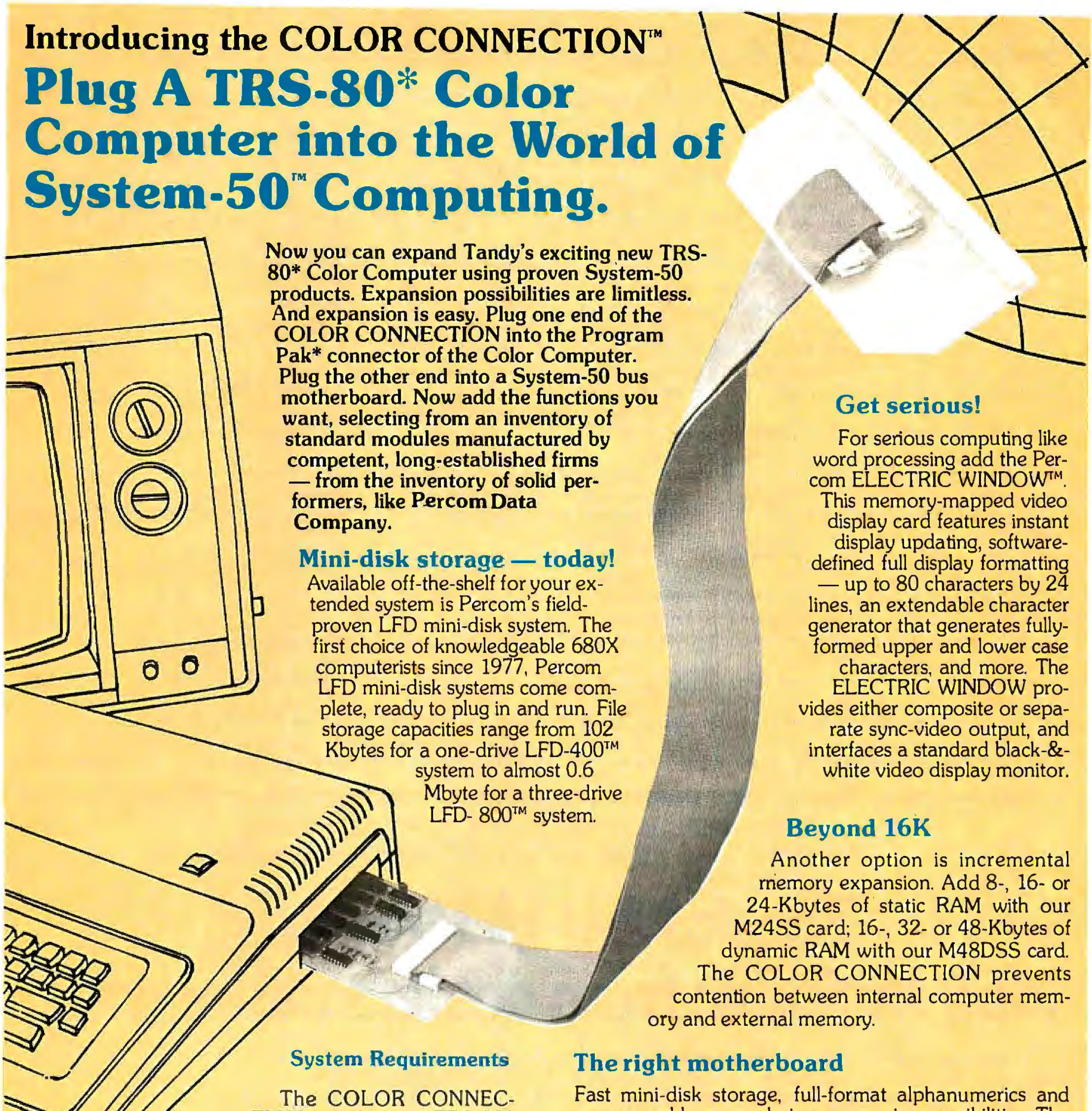

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have overwhelmed the fact that muSIMP is a general language suitable for more than symbolic mathematics applications. The differences between muSIMP and LISP are mostly at the user interface. The input syntax and the output format have been altered to provide a congenial environment for symbolic mathematics, but internally muSIMP is LISP with only a few minor alterations (which could well be regarded as improvements over the original). These alterations are summarized in "LISP-Based Symbolic Math Systems" by David R Stoutemyer, which appeared in the BYTE LISP issue of August 1979, page 176.

At $75 (plus another $20 for the complete reference manual) muSIMP for the TRS-80 is a great bargain. Yet Microsoft's ads have pushed muMATH with only a passing reference to muSIMP's close relationship to LISP.

The documentation that comes with the TRS-80 version of muSIMP/muMATH does not include a number of important muSIMP functions. For example, the functions related to property lists are not even mentioned. Property-driven functions are a major component of muMATH's power and extensibility. The TRS-80 owner who wants to explore the power of muSIMP definitely needs to purchase the full reference manual to supplement the material that accompanies the package.

The full reference manual is impressive. It includes listings of on-line tutorials apparently available with the larger CP/M version. Unfortunately, it does not specifically address the system environment of the reduced TRS-80 package. A number of system functions are not included (SAVE, LOAD, OBLIST). While the manual is extremely useful to the TRS-80 owner, it would be even more useful if it included a summary of the differences between the full CP/M version and the reduced TRS-80 version.

In short, for the TRS-80 owner who is interested in experimenting with artificial intelligence projects, muSIMP alone is worth the price of the muSIMP/muMATH package.

John R Goldin
66 Brownell St
New Haven CT 06511

BYTE Saluted

I am a career Army officer. After five years of assignments outside of the data-processing field, I have returned to that arena; however, the landscape has changed. It is covered with new technology, methods, technical terms, and jargon.

I want the world to know how useful BYTE is in overcoming the insecure feeling of operating in this new landscape. Particularly noteworthy and helpful is BYTE's editorial policy of parenthetically explaining all jargon and technical terms. While other trade journals seem to take delight in obscurity, BYTE consistently targets on clarity. I hope other publications will follow BYTE's lead. It's needed.

Keep up the good work, BYTE!

James H Powers
Lieutenant Colonel, US Army
Director, ADP (Automatic Data Processing)
Support Division
US Army War College
Carlisle Barracks PA 17013

Self-Replicating Code

I would like to point out the shortest self-replicating program I know of. It is written in Microsoft BASIC, as found in the Commodore PET (also known as the

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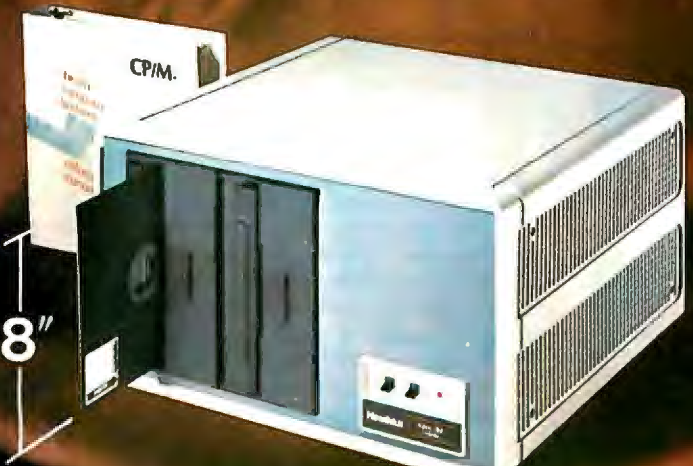

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CBM 2001). It relies on the fact that PET BASIC sees all commands the same way. In many BASICs, you can write a 1-line instruction without a line number and it will be executed when entered. But PET BASIC also allows commands like RUN or LOAD to be inserted into a program with a line number, like any instruction. The program is:

```
1 LIST
```

Because of the compact storing of code in the PET's memory, the program takes up only 2 bytes, one for the line number, and one for the PET's internal representation of LIST (the space between is provided by the subroutine that controls the printout of integers).

I'm currently in the 9th grade, and am fluent in BASIC. I intend to learn Pascal when the school library gets the book it just ordered.

William Sommerfeld
3 Mary Ln
Greenvale NY 11548

Printers Challenged

For some months now, I have been searching for a printer that meets all of my needs, and have met with little success. I have lost hope of finding what I want by looking at magazine advertisements, visiting computer stores, and circling numbers on reader-service cards. I would like to issue this challenge:

If any printer manufactuer or distributor has a machine that fits all (and I mean all) of the requirements listed below, I will buy it, pure and simple.

- It must have some form of letter-quality printing. A fast, low-quality mode and a slow, high-quality mode would be fine. ("Letter-quality," as far as I am concerned, means lowercase letters with descenders.)

- It must be able to handle both single-sheet and fanfold paper (with either pin or tractor feed).

- It must have graphics capability. I can write the graphics software if I must, but the graphics must be real, not block graphics or plotting of Xs.

- It must have at least some minor forms control. Even a simple top-of-page for 11-inch paper would be sufficient.

- I must have some convenient way to get the printer fixed when it breaks. I live in Brooklyn; a service center anywhere in the New York City metropolitan area would be fine.

- The printer should cost $1000 or less. The highest I am willing to go, including tax, shipping, and all the options I need, is $1200.

Are all these requirements unreasonable? I don't think so. There are a number of printers advertised in BYTE that miss by only one or two points. For example, MPI's 88G printer does not have lowercase descenders and the closest place I could have it repaired is in Ridgewood, New Jersey; otherwise, I would have purchased it right away. The Centronics 737 has no graphics (no Centronics I know of does). Okidata's Slimline cannot handle single sheets, while their Microline has no descenders and only block graphics. The Base2 prints in dark-blue ink and can't handle single sheets either, neither can the Anadex GraphicsPLUS... and so on.

I suppose printer manufacturers have their own reasons for not including this capability or that feature in their printers, but I have a pretty good reason for wanting the features I want. I don't do just one thing with my computer, I do a whole range of things, from business writing to hobbies to simulations to music synthesis. I refuse to invest in another printer that does not help me use my computer to its greatest potential.

Bill Seligman
667 Rugby Rd
Brooklyn NY 11230

Run Down

Being a Hewlett-Packard fan and owning an HP-41C, I was anxious to read Bruce D Carbrey's review of the calculator in the December 1980 BYTE. (See "A Pocket Computer? Sizing up the HP-41C," page 244.) I feel that the review was quite good and that all of Mr Carbrey's judgments were fair and realistic, especially when comparing it with Texas Instruments' TI-59.

However, I must disagree with one of Mr Carbrey's observations. He said that the typical life-span of the nonrechargeable size-N batteries is 1 to 2 months. I have had my calculator for 13 months, and I have used it a good deal during that time. Only a week ago did it become necessary to replace the original set of batteries.

Fred W Scheifele
108 Shelly Ln
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Structured Programming and Structured Flowcharts

Gregg Williams, Editor
BYTE
POB 372
Hancock NH 03449

Structured programming—that phrase, unfamiliar to me and, I assume, to most people several years ago—is now endowed with such magical powers that most books on programming include it somewhere in their titles.

But what is structured programming? Most of us feel that it is probably good for us, like getting regular exercise or brushing our teeth after each meal. You may also think it's too complicated (not true), that it slows down programming (wrong, it usually speeds it up), or that it cannot be done unless your computer runs a language like Pascal or ALGOL (wrong again).

Simply put, structured programming is a set of techniques that makes programs easier to write, easier to understand, easier to fix, and easier to change. These techniques are simple and general and can be adapted to any computer language that has a *goto* statement—that includes BASIC, assembly language, FORTRAN, and COBOL. The purpose of this article is to show you a new form of notation that will help you write structured programs. But first, let's review structured programming.

The Elements of Structured Programming

A structured program is like a set of notes written in outline form. The headings accompanied by Roman numerals—I, II, III, and so on—provide the overall organization. Each Roman numeral topic is broken into several component topics (A, B, and C, for example) and each of these is subdivided further (1, 2, 3, ...) and further (a, b, c, ...) as needed. Table 1 shows a problem and its solution written in this outline form.

The above example demonstrates a process known as *decomposition:* breaking a task (problem) into its subtasks. This process represents the *most* important concept in structured programming, ie: that a problem can be solved by repeatedly breaking it into subproblems, until *every* subproblem can be solved. If you plan this decomposition before you try to write it out in the narrow, precise, and time-consuming syntax of the target language (ie: the programming language you use to solve the problem), you will have a better chance of getting your program right the first time.

It has been mathematically proven that any program can be written using three basic constructs.

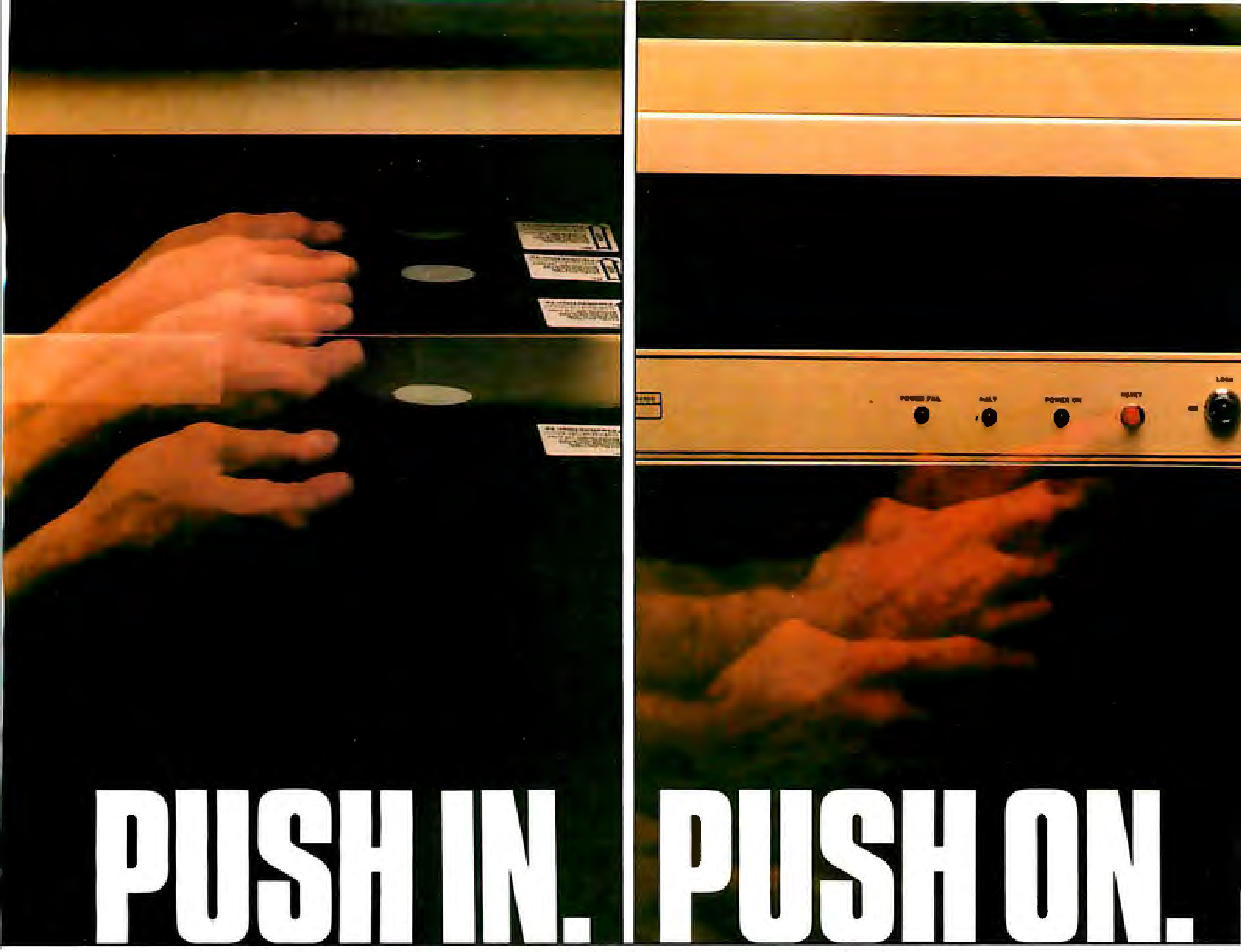
But how do you decide which way to break the problem into subproblems? Common sense helps. Ask yourself, "What sequence of actions and decisions would I have to make if I were doing this without a computer?"

The rest of the answer comes from the literature of structured programming. It has been mathematically proven that *any* program can be written using three basic patterns, called *programming constructs* (or simply *constructs*): sequence, *if...then...else,* and *while...do.* The first construct, sequence, gives you the basic capability of breaking a task into a set of subtasks that accomplish the main task when executed sequentially.

The second construct, *if...then... else,* performs one of two subtasks, depending on the truth or falsity of a stated condition. An everyday example of this construct is given in the following sentence: "If it is raining outside, I will take my umbrella with me; if it is not, I will leave the umbrella at home."

The third and least familiar construct, *while...do,* is actually a generalized *do-loop* that repeats a set of actions (called the *body* of the loop) while a stated condition is true. You use this construct when making iced tea from a mix: "As long as (while) the mix is not completely dissolved, I will continue to stir it."

If you combine lines of code in the three ways described above, the resulting program is said to be *structured.* In most languages (BASIC, for example) you will still use *goto* statements, but they will be *restricted* to carrying your program to specific points, ie: the beginnings and ends of tasks or subtasks. Each module (subtask) in a structured program has a property known as "one-in, one-out"; that is, there is only one entrance and one exit from these modules, and no module will ever jump into the middle of another one. Instead of being like a plate of spaghetti, a program is more like a string of pearls (with each pearl containing another, smaller string of pearls, and so on); each module has a definite and unchanging position on the string. When such regularity can be counted on, existing modules can be changed or deleted, and entirely new modules can be add-



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Structured Programming: A Qualification

About a year ago, I thought that structured programming was the ultimate tool in the analysis, design, and implementation of a computer program. I had read several books on the subject, browsed through a great many more, and successfully applied the techniques to real-world problems. Many books spoke of structured design, *but I saw the concept as simply the same structured programming tools applied to the earlier process of program design—that is, of transforming a situation to be solved into a set of programs that will accomplish the task. I was more wrong than right.*

Through my experience with a particular programming project, I suddenly recognized a major point that I had formerly not comprehended: that structured programming does not *encompass the entire process of programming. The process of programming begins with some sort of description or specification of the program to be written. With small programs (the kind we spend most of our lives writing), this is usually enough. But as the problem gets bigger (and perhaps more ill-defined), more and more crucial design decisions must be made before you divide the problem into programs.*

I also learned that certain design decisions within a given program are overlooked by the main ideas of structured programming. Structured programming is a literal-minded discipline that deals exclusively with the orderly disassembly of a problem into the series of program statements that solves it. It does this while assuming several givens: the overall algorithm to be used (eg: bubble sort or heapsort), the data structures used (eg: linked lists, arrays, or binary trees), and implementation details (eg: sequential or random-access files, the packing of one or two characters per byte). These details, which may have a tremendous effect on the quality of the program (in such aspects as size, speed, readability, and maintainability), are factors that are evaluated and weighed in the design process.

The purpose of these paragraphs is two-fold: first, to affirm that the techniques described in this article can make a significant improvement in your skills as a programmer and that they are sufficient for many programs; and, second, to emphasize that the quality of a program can often be greatly improved by attention to the design decisions that are made in the early stages of analyzing the program design. I am including a list of particularly helpful books and articles in the references at the end of this article.

ed without problems caused by unexpected module interaction.

That is the theory of structured programming—now for putting it into practice. Figures 1 thru 3 show the three constructs (sequence, *if... then...else*, and *while...do*) in standard flowchart form and as BASIC code. (For a more detailed look at writing structured programs in BASIC, see "Applied Structured Programming," listed in the references. This article appears in an anthology that contains several other good articles on program decomposition—sometimes called *top-down design* or *programming by stepwise refinement*—and structured programming.)

Problem: Given a numeric array V with N elements, find the largest element, MAXV, and its index, MAXINDEX. These variables are related as follows:

- 1 < MAXINDEX < N
- MAXV = V (MAXINDEX)
- MAXV is the largest value in V(1), V(2),...V(N).

Solution:

I. Set problem up:
  A. Set MAXVAL = -9 x 10^{20}
  B. Set MAXINDEX = 0
  C. Set INDEX = 1
II. Find largest element:
  A. Set up a loop that increments the variable INDEX from the beginning to the end of the array V.
  For each value of INDEX:
    1. Compare the current array value (V (INDEX)) to MAXVAL:
      a. if MAXVAL is equal or larger, do nothing;
      b. if MAXVAL is smaller, replace MAXVAL with the current array value and MAXINDEX with the current index (the value of INDEX).
III. Print the largest element (MAXVAL) and its index (MAXINDEX).

Table 1: *A problem and its solution in outline form. The common outline form used for summarizing a body of material can also be used to give structure to the emerging design of a program. Table 1a gives a statement of the problem and table 1b gives its solution in outline form.*

The Origins of a New Notation

When I got my first job as a commercial programmer, I realized that I was going to have to write longer programs than I had previously written. This prompted me to adapt structured programming techniques to my work in BASIC, COBOL, and RPG II. (As it turned out, my longest program was a 35-page COBOL program that grew to 75 pages without going out of control. I could not have done this without the rigorous use of structured programming techniques.)

As my programs grew larger, I became dissatisfied with the methods I used to plan my programs. Conventional flowcharts obscured the structure of my programs. Nassi-Schneiderman charts and Warnier-Orr diagrams were unsatisfactory for other reasons.

The best solution offered in structured programming texts was *structured pseudocode,* an informally written Pascal-like "program" that uses terse English phrases to describe the program. Listing 1 shows the structured pseudocode for the program outlined in table 1b. I used structured pseudocode extensively to outline programs but found that the details of the resulting pseudocode often obscured the overall design of the program.

In retrospect, I can see that I wanted a design notation that could do the following:

- Completely describe the algorithm to be programmed
- Provide overview and detailed documentation that was easy to read
- Not need to be redrawn every time

Text continued on page 26

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Listing 1: *A structured pseudocode solution of the FINDMAX problem given in the text and in table 1. Structured pseudocode is a terse, informal, Pascal-like program that helps the user design a program before writing it in a formal programming language.*

```
Program FINDMAX:
Initialize system variables (MAXV = $-9 \times 10^{20}$, MAXINDEX = 0, INDEX = 1)
While INDEX $\leq$ N
  find value of current array element ( CURRV = V (INDEX) );
  if current array element (CURRV) > maximum element so far (MAXV)
    new maximum element = current element
    new maximum index = current index ( MAXINDEX = INDEX )
  endif
  increment INDEX by 1
endwhile
print MAXV, MAXINDEX
(end of program)
```

Listing 2: *A BASIC implementation of the FINDMAX problem from table 1. In this program, the variable MAXINDEX has been shortened to MINDEX to distinguish it from the variable MAXV. This program is written in TRS-80 Model I Level II BASIC, and it will run on other computers that use Microsoft BASIC.*

```
100 :
110 REM                      PROGRAM FINDMAX
120 :
130 REM      THIS PROGRAM TAKES AN ARRAY OF NUMBERS, V, AND
140 REM   FINDS THE LARGEST ELEMENT, MAXV, AND ITS INDEX,
150 REM   MAXINDEX, SUCH THAT:
160 REM                 MAXV = V (MAXINDEX)
170 :
180 REM      (FOR THE PURPOSES OF ILLUSTRATION, WE WILL ASSUME
190 REM   THAT THE DATA IS ALREADY IN THE ARRAY V.)
200 :
210 :
220 REM ================== MAIN PROGRAM =====================
230 :
240 DIM V(12)
250 GOSUB 800: REM   --NOT PART OF ALGORITHM IN FIGURE 6; THIS
260 REM                    SUBROUTINE ENTERS DATA INTO ARRAY V
270 :
280 REM ---------- BOX 1: INITIALIZATION ROUTINE -------------
290 :
300 MAXV = -9 * 10[20
310 MINDEX = 0
320 INDEX = 1
330 :
340 REM ---------- BOX 2: FIND LARGEST VALUE -----------------
350 :
360 REM -- (BEGINNING OF WHILE...DO LOOP)
370 IF INDEX > N THEN 520
380     CURRV = V (INDEX)
390 :
400     IF CURRV < MAXV THEN 440
410          MAXV = CURRV: REM -- (THIS PART EXECUTED IF FALSE)
420          MINDEX = INDEX
430 :
440     INDEX = INDEX + 1
450 :
460 REM -- (JUMP TO BEGINNING OF WHILE...DO LOOP)
470 GOTO 370
480 :
490 :
500 REM ----------- BOX 3: PRINT FINAL VALUES ----------------
510  :
520 PRINT:  PRINT "THE LARGEST VALUE IN THE  V  ARRAY IS:"
530 PRINT "          V("; MINDEX ; ") = "; MAXV
540 PRINT
550 :
560 END
570 REM ============= END OF MAIN PROGRAM ==================
760 :
770 :
780 REM ----------- SUBROUTINE TO FILL V ARRAY ---------------
790 :
800 DATA 12: REM -- (NUMBER OF ITEMS TO BE READ IN)
810 DATA 1, 15, -28, 3.24, -17.92, 0, 5, 1, 0, 21.4, -205, 17
820 READ N
830 FOR I=1 TO N: READ V(I): NEXT I
840 RETURN
```

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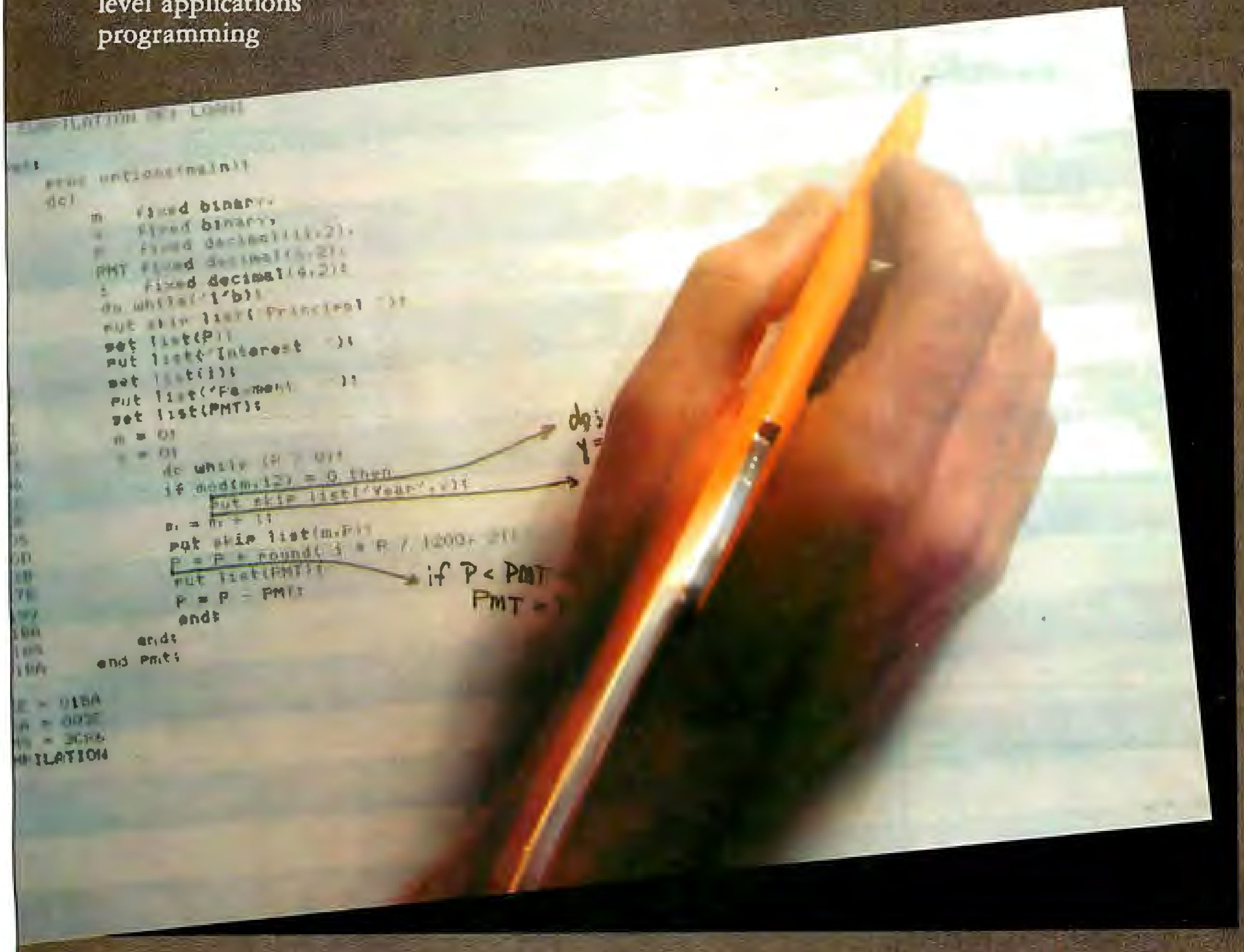

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Text continued from page 22:

a change was made in the flowchart

- Use a minimum of unfamiliar notation
- Be visually pleasing

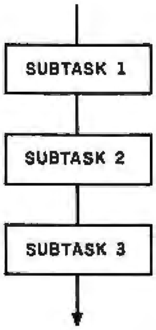
This *structured flowchart* notation, which I developed over a period of several years, meets these criteria.

Basic Constructs in Structured Flowcharting

According to the tenets of structured programming, any program can be expressed as a combination of four basic building blocks. These are sequence, *if...then...else*, *while...do*, and decomposition. (The first three constructs, described in conventional flowcharts in figures 1a thru 3a, are given in structured flowcharts in figures 4a, 4b, and 4c, respectively.)

The sequence construct (figure 4a) is identical for both conventional and structured flowcharts; however, a later construct, decomposition, will distinguish the structured flowchart sequence construct from its conventional counterpart.

(a)

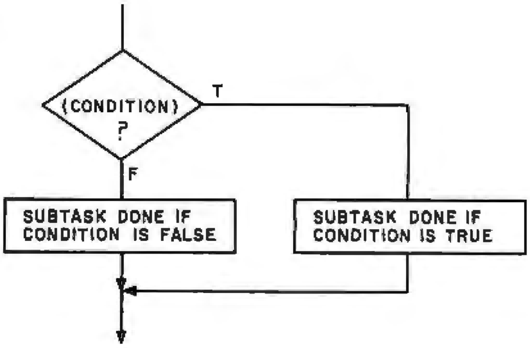


(b)

```
100  (BASIC statement for subtask 1)
110  (BASIC statement for subtask 2)
120  (BASIC statement for subtask 3)
          .
          .
          .
```

Figure 1: *Sequence as a control structure. Figure 1a shows how a linear sequence of subtasks is drawn using conventional flowchart notation. Figure 1b shows the equivalent sequence as a series of BASIC lines.*

(a)

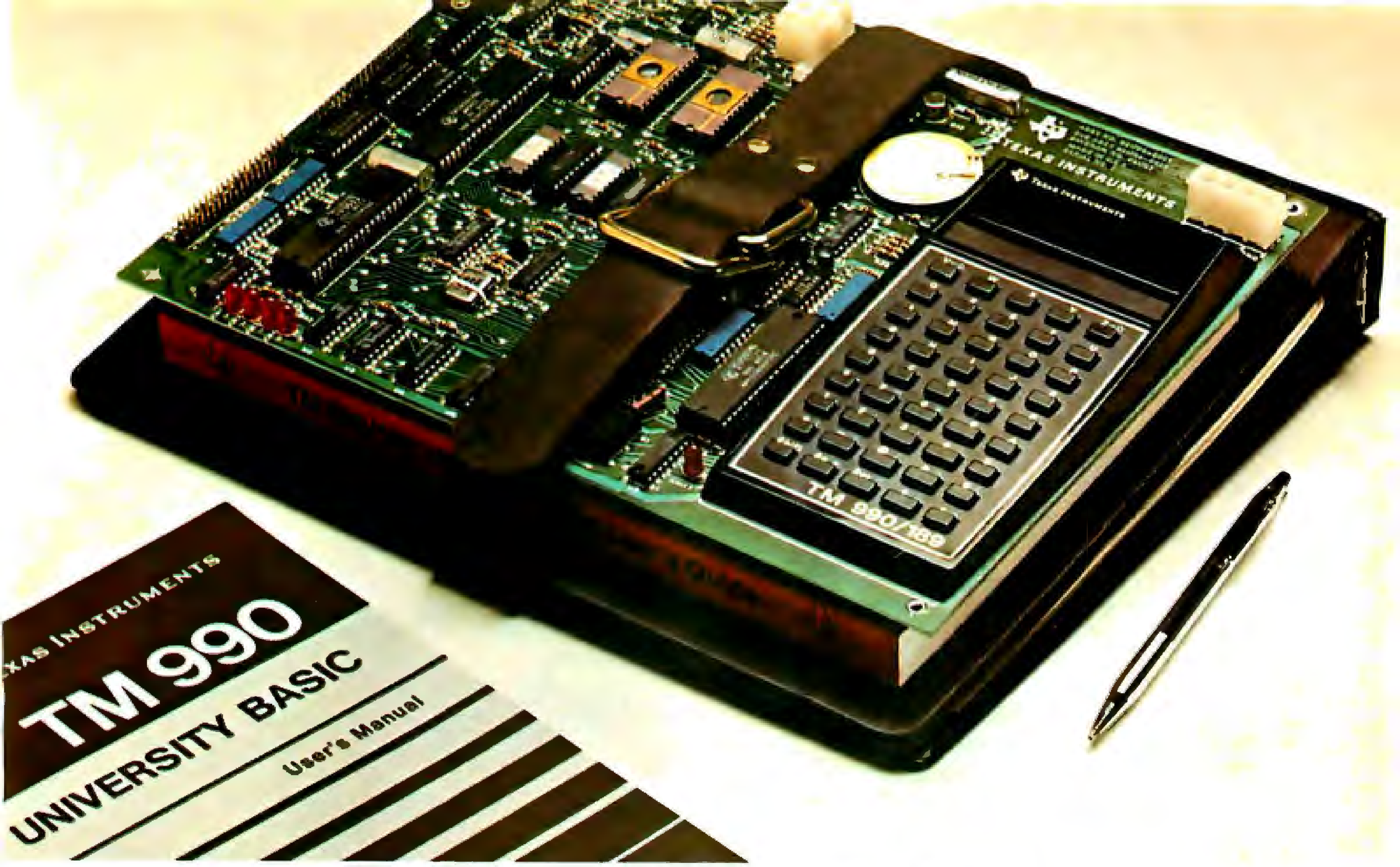


(a) CONVENTIONAL

(b)

```
100  IF (condition) THEN 200
120  (BASIC statements for subtask
     done if condition is false)
          .
          .
          .
190  GOTO 300
200  (BASIC statements for subtask done if
     condition is true)
          .
          .
          .
299  (last statement of "true" subtask)
300  (first statement of next construct)
```

Figure 2: *The* if...then...else *construct as a control structure. Figure 2a shows the conventional notation for this construct, while figure 2b shows the BASIC equivalent.*



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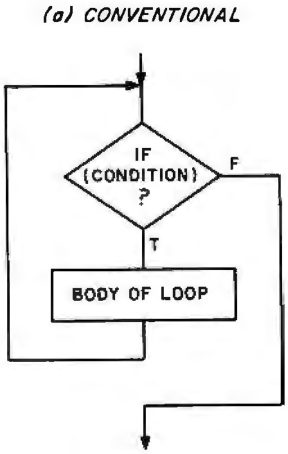

(b)

```
100  IF (opposite of condition) THEN 300
110  (BASIC statements for body of loop,
     done if condition is true)
       .
       .
       .
299  GOTO 100
300  (first statement of next construct)
```

Figure 3: *The* while...do *loop as a control structure. Figure 3a shows the* while...do *loop in conventional flowchart notation. Figure 3b shows the equivalent loop in BASIC code.*

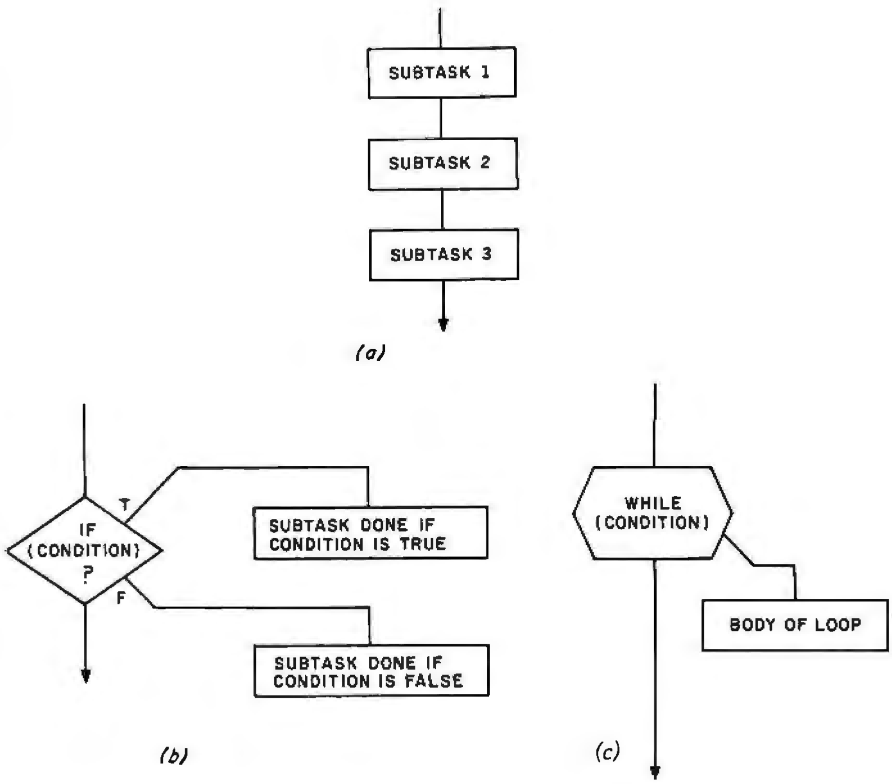

Figure 4: *The basic structured flowchart notations. Figure 4a shows the structured flowchart notation for a sequence of tasks; it is equivalent to the flowchart of figure 1a. Figure 4b shows the structured flowchart notation for the* if...then...else *construct (equivalent to figure 2a); note that it is the placement of the letters T and F (for* true *and* false*) that determines the conditions under which a given subtask is performed. Figure 4c shows the structured flowchart notation for the* while...do *construct (equivalent to figure 3a); the diagonal line leading down indicates that the condition (in the hexagon) is performed* before *the body of the loop.*

The *if...then...else* construct is fairly straightforward in the conventional flowchart (figure 2a). In the structured flowchart version (figure 4b), the boxes to be performed are to the right of the decision diamond, with the understanding that only one of the two boxes will be performed based on the value of the condition in the diamond. If the "else" side of the construct is not needed, the box labeled F is eliminated. In this case, if the condition does not evaluate to *true*, no action is performed, and control continues with the next construct following the decision diamond.

The notation for the *while...do* construct is not as easily derived. The conventional flowchart cannot directly express this kind of loop; it must use a decision diamond and an external loop (figure 3a). The structured flowchart version (figure 4c) introduces a new symbol, a hexagon. (Actually, the hexagon is used to denote one of several kinds of loop structures; the word *while* makes this a *while...do* loop.) The box connected below and to the right of the hexagon is performed as long as the condition

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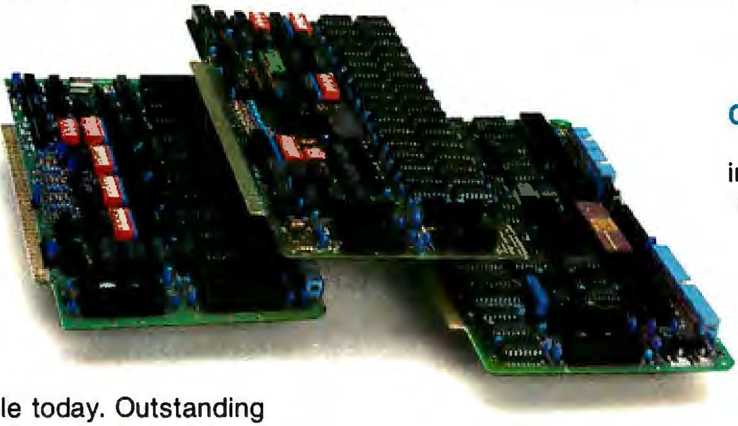

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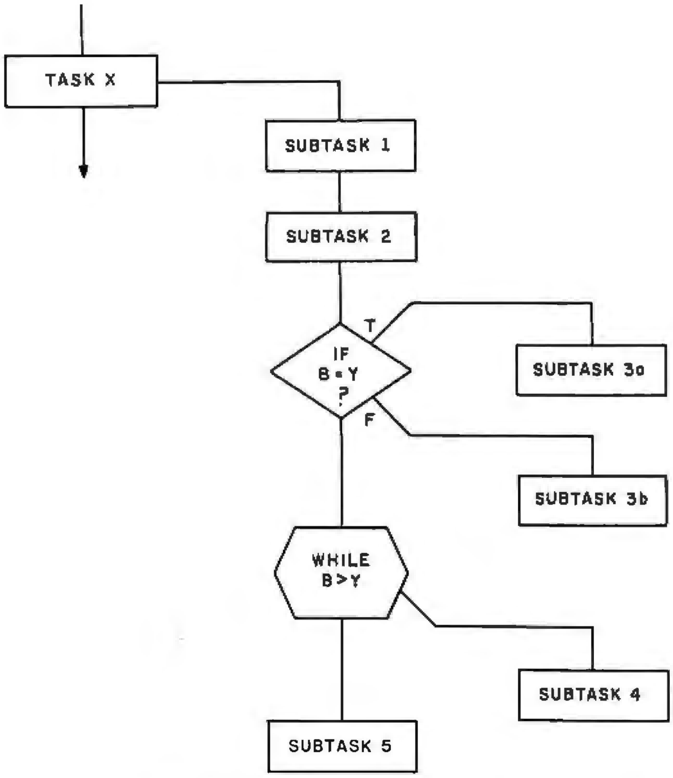

Figure 5: *Example of the subdivision of a task. A central rule of structured flowcharts is that any box can be broken into multiple boxes that represent the necessary subtasks. Here, task X is broken into five subtasks executed in top-to-bottom order. Subtasks 1, 2, and 5 are simple subtasks. Subtask 3 is an* if...then...else *construct. Subtask 4 is a* while...do *loop.*

listed in the hexagon is true. The condition is performed first (denoted by the position of the hexagon being spatially *above* the box being performed); this allows the possibility of the body of the loop being performed zero times if the condition is initially false.

The fourth and pivotal construct of this programming notation, decomposition, can best be stated as a rule: *any box representing a task can be broken into multiple boxes that represent the necessary subtasks.* The subtasks may be rectangular boxes that represent simple tasks, or they may be any other valid structured flowchart construct (*if...then...else, while...do*, etc). They are written top to bottom in the order of performance, with the line denoting program flow entering each subtask box from its top and exiting from the bottom.

Figure 5 illustrates the above construct. Task X is composed of five subtasks performed in numeric sequence. Tasks 1, 2, and 5 are simple subtasks. Subtask 3 is an *if...then...else* construct that allows either subtask 3a or subtask 3b to be per-

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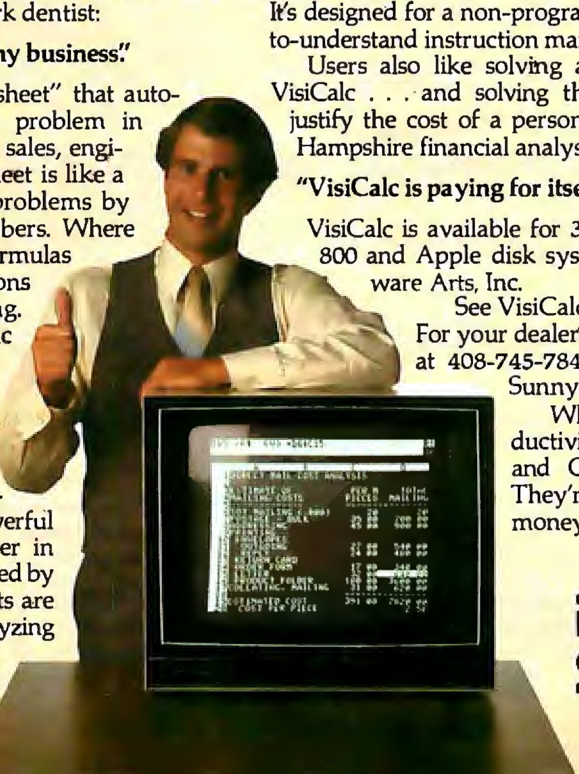

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formed. Subtask 4 is performed as long as the condition within the hexagon (B>Y) is true. Of course, any subtask box may be further divided into its component subtasks.

Since any box can be broken into component subtasks, you can now see how this notation is used to design a program. The boxes in the leftmost column give the overall design of the program; boxes are then expanded to the right as each box (task) is divided into boxes representing the appropriate combination of subtasks. As a result, you can scan any one of several of the leftmost column of boxes for an overview of varying depths of the program design, or you can study the implementation of any major or minor subtask by concentrating on only the boxes and control structures growing to the right of the given subtask.

An Example

The following example will illustrate the process of developing a program using structured flowcharts. Using the example of table 1a, suppose you are given an array of N numbers, V(1), V(2),...V(N), and have to find the index value MAXINDEX such that the largest value in the V array is MAXV=V(MAXINDEX). The entire structured flowchart for this problem is given in figure 6.

Cover the right three-fourths of the flowchart so that only the subtasks numbered 1, 2, and 3 are visible. This is what the "first pass" of the flowcharting effort should look like. Subtask 1 is the initialization of the problem. Subtask 2 is the determination of MAXINDEX and MAXV. Subtask 3 is the printing of these two values. Since the task in subtask 3 is simple enough to be directly accomplished in the target language (for example, BASIC), it need not be subdivided.

Subtasks 1 and 2 are developed concurrently. Subtask 2 is basically a loop that examines V(1), V(2),...V(N) in turn, keeping the appropriate values for MAXV and MAXINDEX for the I elements encountered thus far. The values of MAXV, MAXINDEX, and INDEX must be set (as is done in subtasks 1.1, 1.2, and 1.3). Note that this loop could have been done more easily using a do-loop; other optimizations could also have been made, but this example is given for the purposes of illustration only.

The main work for each element is done as subtask 2.1.2: if the current V element being examined (ie:CURRV) is greater than the maximum V element so far, MAXV and MAXINDEX are set to the current array and index values, respectively. These subtasks, numbered 2.1.2.1 and 2.1.2.2, are performed only when the relationship given in the diamond of 2.1.2 is true.

Once the structured flowchart has reached the level of detail shown in figure 6, most of the design considerations have been conceived and perfected; it is then a simple task to translate the program into BASIC (see listing 2) or any other general-purpose computer language. The benefits are more pronounced when used with a larger program. If a structured flowchart is subdivided to the right until each box represents a task that can be directly coded in the target language, you will catch most of the "oops, I forgot to..." insertions and changes that programmers generally think of *after* they have started coding the program.

Other Control Structures

Although the three constructs discussed so far are sufficient for writing any program, it is not always convenient to use only these constructs. Other control structures can be devised for the convenience of the programmer. For example, boxes 1.3,

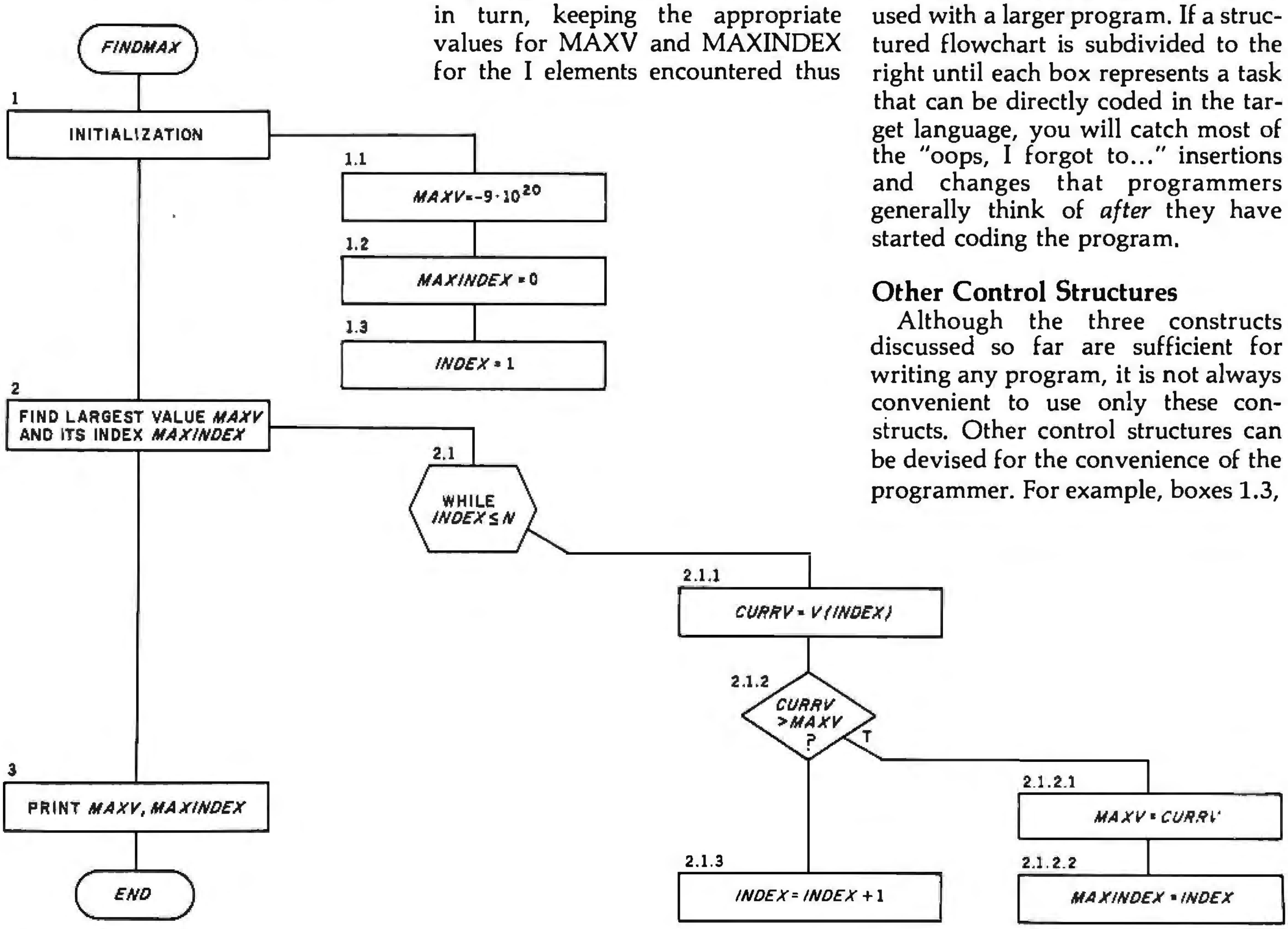
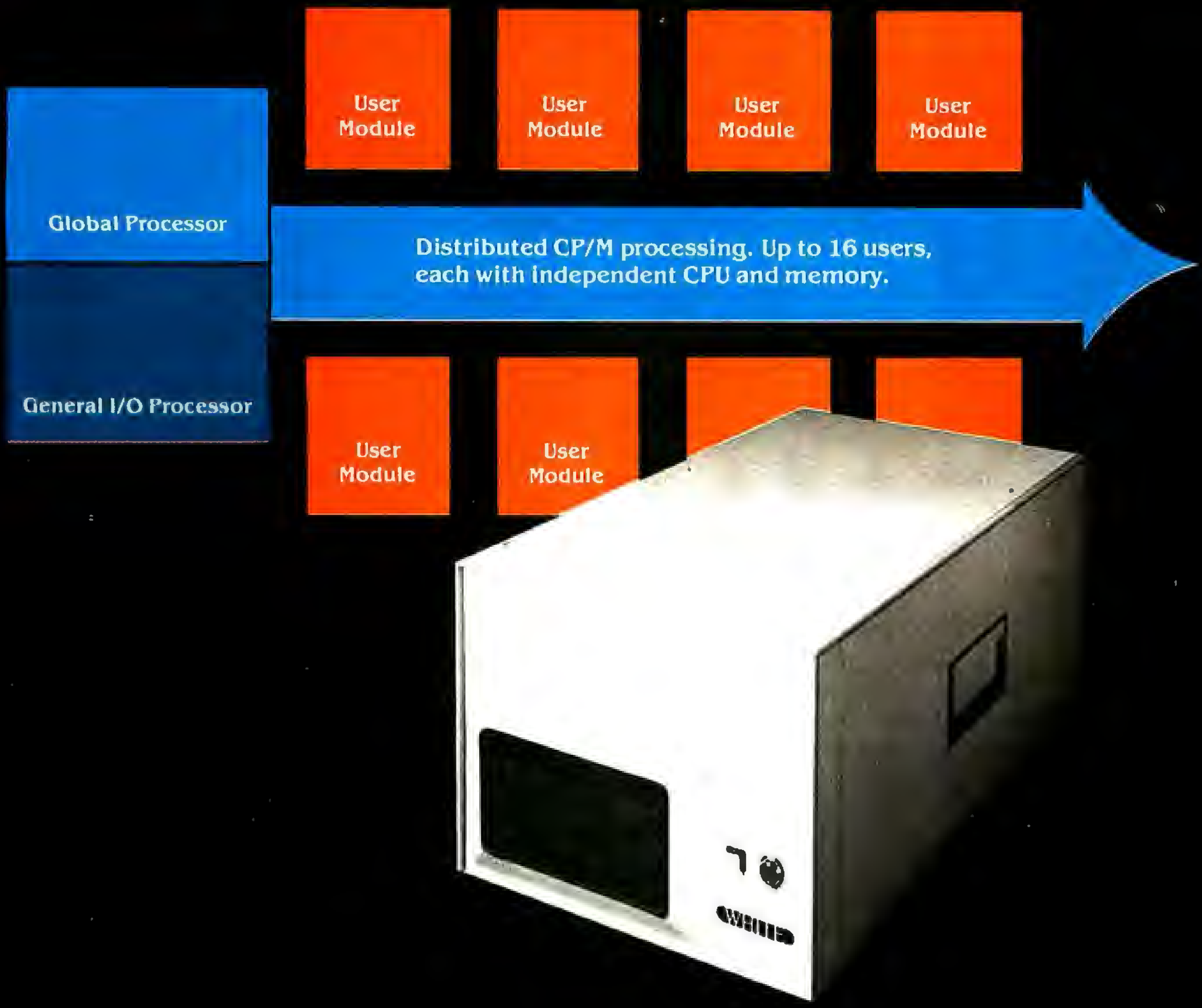


Figure 6: *Structured flowchart for program FINDMAX. Given an array V with N elements, the problem is to find the largest element, MAXV, and its index within the V array, MAXINDEX. The numbers above each box give the sequence and level of that box in relation to the entire problem. For example, box 1 can be broken into three subtask boxes: 1.1, 1.2, and 1.3.*

Circle 23 on inquiry card. ⟶



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2.1, and 2.1.3 in figure 6 can be replaced by a control structure that is available in most programming languages—a *do-loop* that varies INDEX from 1 to N. An example of the notation I have devised for this is given in figure 7a; the body of the loop is performed according to the parameters given in the hexagon.

Another well-known control structure is the *repeat...until* loop, shown in figure 7b. The position of the body of the loop, above and to the right of its associated hexagon, is meant to signify that the body of the loop is performed *before* the condition is tested. Although the meaning of this notation does not implicitly follow from its form, it was chosen for its simplicity and consistency with the notation already developed.

Other constructs come to mind: a *case* structure, an unconditional *goto*, and two controlled *gotos*—the *restart* (restart the innermost containing loop) and the *exit* (go to the first task after the innermost containing loop). Although I have used some of these constructs for quite some time, they are not presented here because I am not yet satisfied with the notations I have developed for them. In any case, structured flowcharts are meant to be a personal notation—you should add to and modify these constructs to fit your needs.

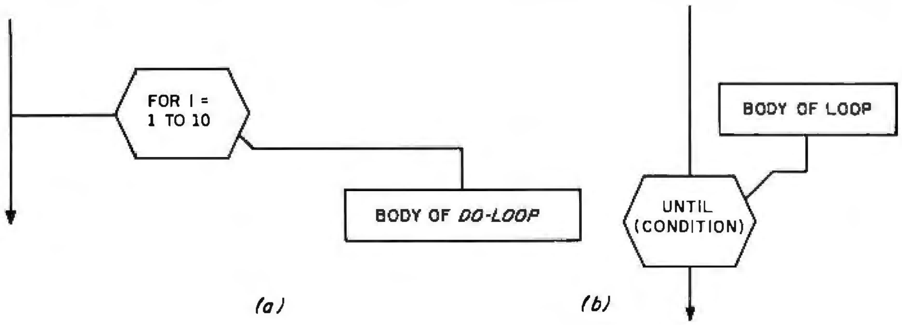

Figure 7: *Structured flowchart notation for a* do-loop *and a* repeat...until *loop. In the* do-loop, *figure 7a, the hexagon contains all pertinent information defining the loop, and in the form most comfortable to the user. In the* repeat...until *loop, figure 7b, the notation is interpreted as showing the body of the loop being executed* before *the condition is tested. In both cases, the box representing the body of the loop can be expanded to the right, into its component subtasks.*

Conclusions

I have found structured flowcharts helpful in designing programs. The notation is obviously intended for weakly structured languages (like BASIC), as its utility decreases when the structure of the target language increases.

The notation is, at the moment, informal, and it should stay that way. It should be extended and modified in whatever way seems useful to you. In particular, you should use additional notation for special features of the target language (eg: global and local variables, use of a stack of intermediate computation) when applicable. If the structured flowchart is to be read by another person, however, you should define all the structures used in terms of their equivalent unstructured (conventional) flowcharts.

If the final structured flowchart is to be redrawn, you should do so with clarity in mind. Place only those boxes that help explain the overall design with the main flowchart; leave the implementation details to subordinate flowcharts.

I hope you will find this notation useful. I would appreciate your suggestions, criticism, and comments. ■

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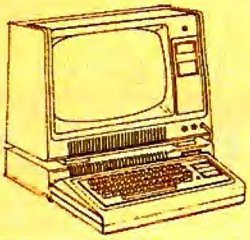

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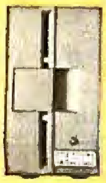

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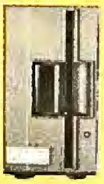

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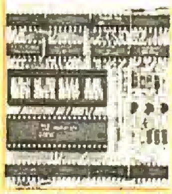

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Build the Disk-80

Memory Expansion and Floppy-Disk Control

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The term "memory expansion" no longer causes the same pained expression among computer owners as it did a few years ago. Back in the "Model T" days of personal computing, it was a major undertaking, often the largest expense of setting up a personal computer system. At that time, volatile memory integrated circuits contained only a fraction of the capacity of those available today, and mass storage often consisted of slow audio cassettes.

Back in 1975, if you were adding 32 K bytes of memory to your computer you would probably have used 256 type-2102A 1 K by 1-bit static memory chips. These cost between $2 and $5 each, and you probably would have needed a power supply larger and heavier than the computer. Believe it or not, the 2102A was a major improvement over the previous type-1101 memories (256 by 1-bit static devices). It would have taken 1024 (1 K) of the type-1101 components to make 32 K bytes.

Since that time, memory technology has progressed by leaps and bounds, and the cost per bit has dropped considerably. Many computer manufacturers now use dynamic rather than static memory. The result is much higher density, lower system cost, and easier after-market memory expansion on most computers.

The 64 K-byte personal computer system is more common than you would imagine. Adding another 16 or 32 K bytes of memory these days simply means plugging a few (8 or 16) integrated circuits into a memory-expansion unit or motherboard. Usually the standard power supply suffices.

Even with these advantages, using dynamic memory is not quite as simple as it sounds. There are considerable differences between static and dynamic memory. Most people know relatively little about designing a dynamic-memory system, and even professional designers are intimidated by having to deal with multiplexing addresses, selecting bus drivers, sequencing activation of power supplies, and decoupling and noise. I don't expect that reading this article will make you into an authority on dynamic memory, but perhaps you will at least have a better understanding of it.

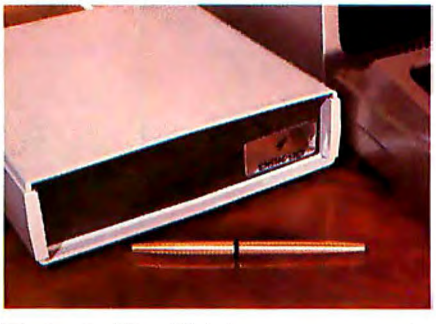


Photo 1: *The Disk-80 mounted in its enclosure and attached to the TRS-80 Model I computer. The Disk-80 is about half the size of the Radio Shack TRS-80 Expansion Interface.*

Mass-storage technology has also progressed during this same period. Displacing the audio cassette as the exclusive medium, the floppy disk and Winchester-technology hard disk have become the *de facto* storage standards.

For some time I have wanted to present articles on dynamic-memory and disk-controller integrated circuits. I have delayed chiefly because I generally prefer to present my articles as usable applications.

The three largest-selling personal computers, the Radio Shack TRS-80, the Apple II, and the Commodore

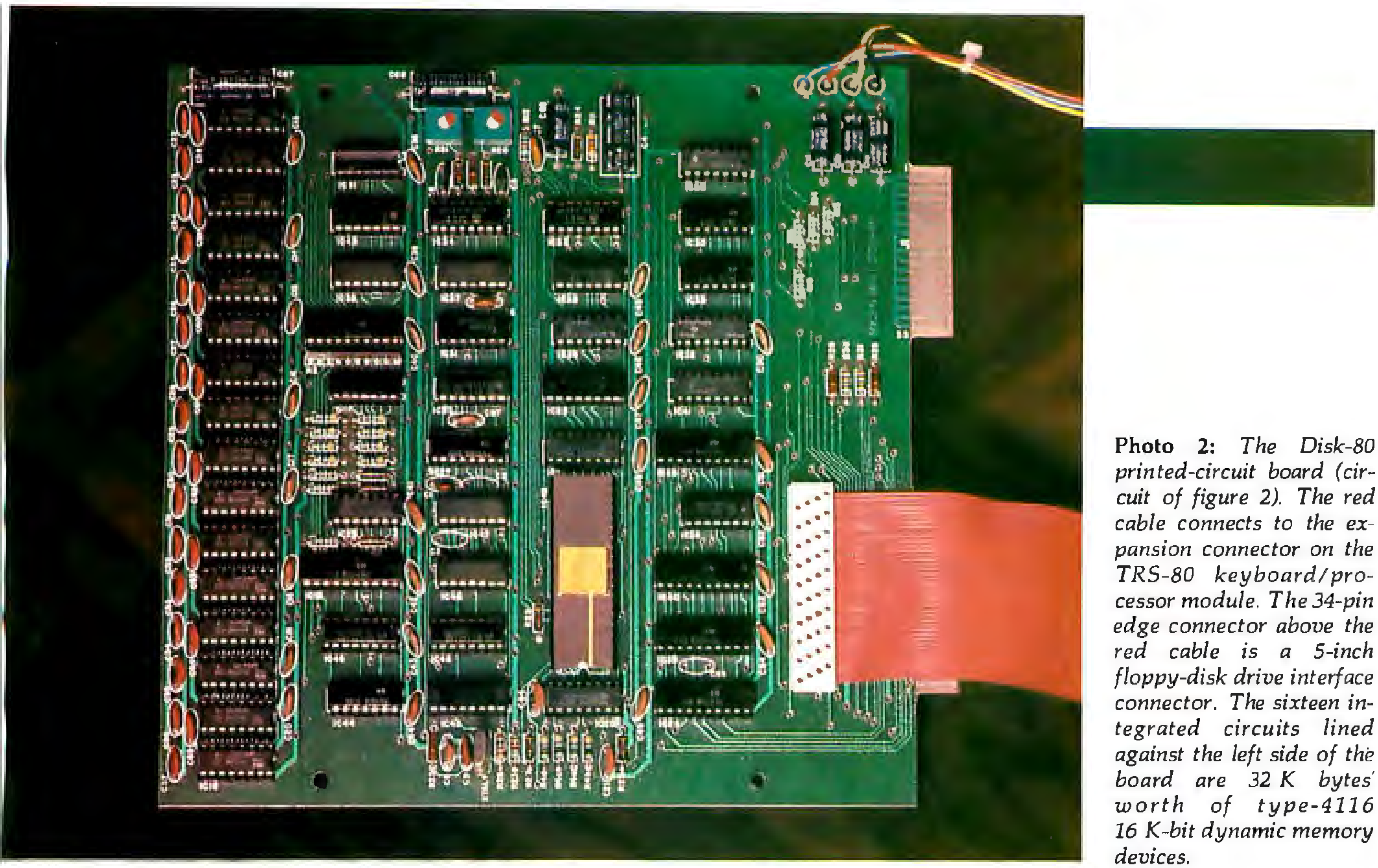


Photo 2: *The Disk-80 printed-circuit board (circuit of figure 2). The red cable connects to the expansion connector on the TRS-80 keyboard/processor module. The 34-pin edge connector above the red cable is a 5-inch floppy-disk drive interface connector. The sixteen integrated circuits lined against the left side of the board are 32 K bytes' worth of type-4116 16 K-bit dynamic memory devices.*

PET, use 16 K-bit dynamic-memory chips. Only the TRS-80 Model I requires the user to add extra memory via an external module, the TRS-80 Expansion Interface. (The TRS-80 Model III does not.)

This month's hardware project, the Disk-80, is an expansion interface for use with the TRS-80 Model I that expands the user memory and provides for the attachment and control of floppy-disk drives. Dynamic memory and a specialized floppy-disk-drive controller are used. Although this project was designed for use with the TRS-80 Model I, the elements of the systems and the principles involved are applicable to any personal computer.

What's Inside the Disk-80?

The Disk-80, shown in photo 1, is completely hardware- and software-compatible with the TRS-80 Model I and includes hardware enhancements for increased reliability. Readers familiar with the TRS-80 Expansion Interface will note that the Disk-80 is considerably smaller.

The keyboard/processor module of the TRS-80 Model I system is a single-board computer with memory-mapped video display and keyboard. The only provision for I/O (input/output) in the basic configuration is an I/O port for an audio-cassette recorder and a single-bit relay line for control of the recorder motor. Any user-memory expansion beyond 16 K bytes and any printer or disk I/O must be handled externally. The unit sold by Tandy/Radio Shack to perform these functions is called the TRS-80 Expansion Interface.

Figure 1 is a block diagram of the Disk-80. It attaches to the keyboard/processor unit through the 40-pin TRS-BUS connector and provides the following functions: 32 K-byte user-memory expansion, Centronics-compatible parallel printer port (full 8 bits), real-time clock, four-drive 5-inch floppy-disk controller, external data separator (used in reading floppy disks), buffered TRS-BUS connection to other peripheral devices, and power supply.

The three major functional sections are as follows:

- Memory-expansion section, which accommodates up to 32 K bytes of dynamic memory;
- Four-drive 5-inch floppy-disk controller; and
- Parallel printer port.

The activities of these sections are coordinated through a common address decoder.

The Disk-80 system is divided into two circuit boards. The main board, shown in photo 2 and outlined schematically in figures 2a, 2b, and 2c, contains everything except the power supply and the printer port. The other board, referred to as the power-supply/printer-interface board, is shown in photo 3 on page 45.

Disk-80 Addressing

The disk controller, printer, and real-time clock are addressed as memory-mapped parallel I/O ports through IC28, a 74LS155 decoder. Eight strobe signals are produced to decode memory addresses within the range of hexadecimal 37E0 to 37EC (only six of these are used in the Disk-80) to coordinate these peripherals. Their functions are shown

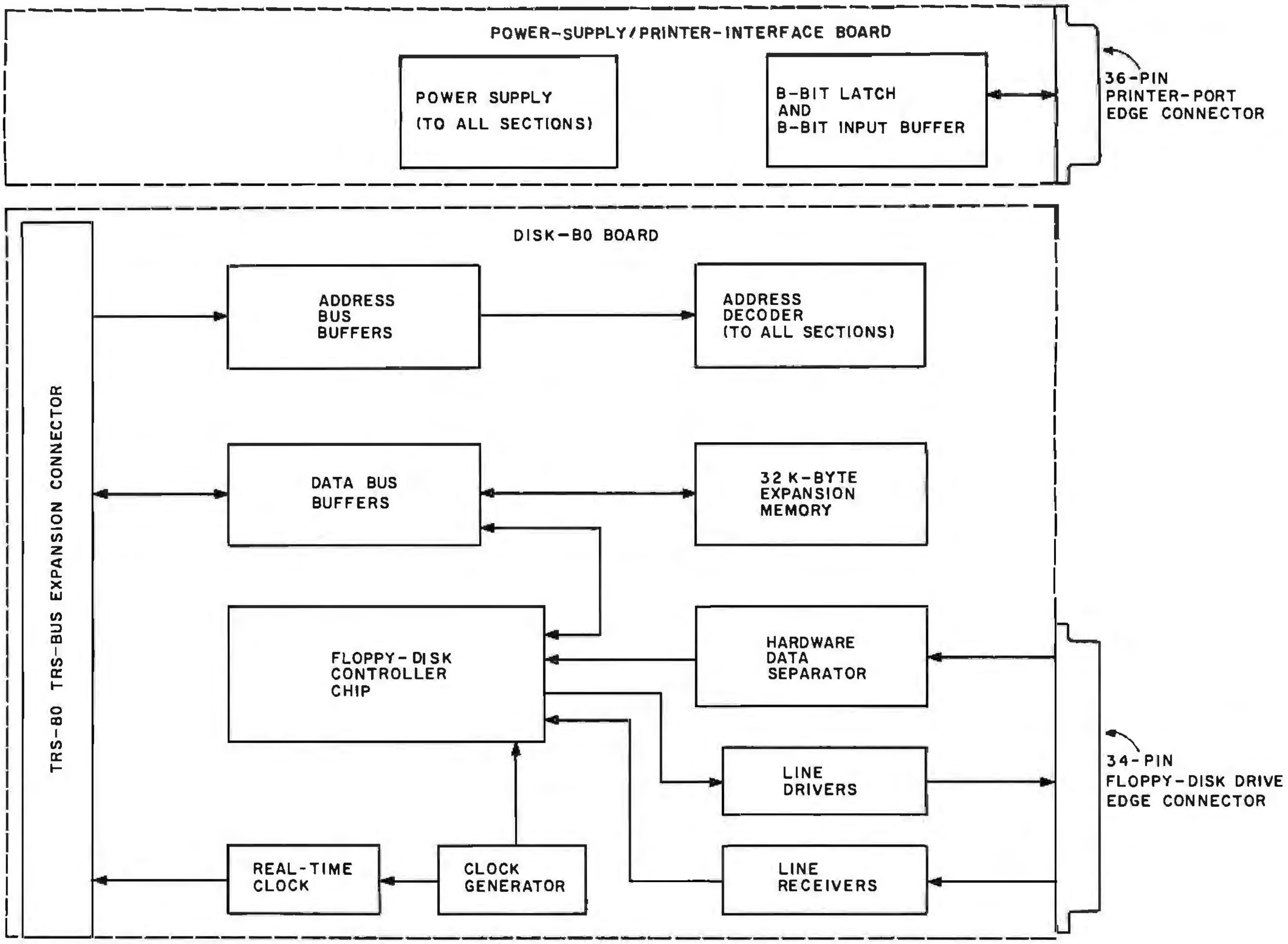


Figure 1: *Block diagram of the Disk-80 expansion interface for the Radio Shack TRS-80 Model I.*

Elements of the systems presented and the principles involved are applicable to any personal computer.

in table 1 on page 44.

IC26, an eight-input NAND gate, and IC27, a 74LS139 decoder, function as memory-bank decoders. They produce two strobe signals. One, designated $\overline{\text{32 K}}$ (or informally, 32 K enable), is the active-low enable strobe for expansion memory between hexadecimal addresses 8000 and BFFF. The second strobe, $\overline{\text{48 K}}$ (or 48 K enable), controls the bank of memory between C000 and FFFF.

Operation of Dynamic Memory

When designing memory systems, it is necessary to understand both the components and the computer system. In the past, the most popular dynamic memory components were MK4096- and MK4027-type 4 K by 1-bit devices. Today the standard memory component in personal computers is the MK4116. (More recently, maximum density has increased to 64 K bits per chip. Unfortunately, these parts are expensive, about $70 each, and are not yet generally used in personal computers.)

The 4116 is a 16 K-bit dynamic memory device. The 14 address bits required to specify one of the 16,384 cell locations that each store a single bit of data are multiplexed into seven shared pins. The timing of the signals presented to these pins is shown in figure 3 on page 45.

During execution of a Z80 memory-read or memory-write instruction, a 16-bit address is present on the processor's address bus. If the memory address is between hexadecimal 8000 and FFFF, the processor will try to find the addressed memory devices in the Disk-80's memory-expansion section. Decoding address lines A14 and A15 determines whether the location is in the 32 K or the 48 K memory range and enables the appropriate bank. The remaining 14 bits are multiplexed directly into the eight 4116s (one 4116 is used for each bit of the addressed byte location).

IC20 and IC21, 74LS157 quad 2-to-1-line multiplexers, apply the first 7 row-address bits to each 4116 when the MUX (multiplex) and $\overline{\text{RAS}}$ (row-address strobe) signals are low. This latches the row address into the 4116. Next, the MUX signal goes high, applying the 7 column-address bits to the 4116, and $\overline{\text{CAS}}$ (column-address strobe) goes low. At the conclusion of this sequence, data is either written into or read from the 4116

Text continued on page 44

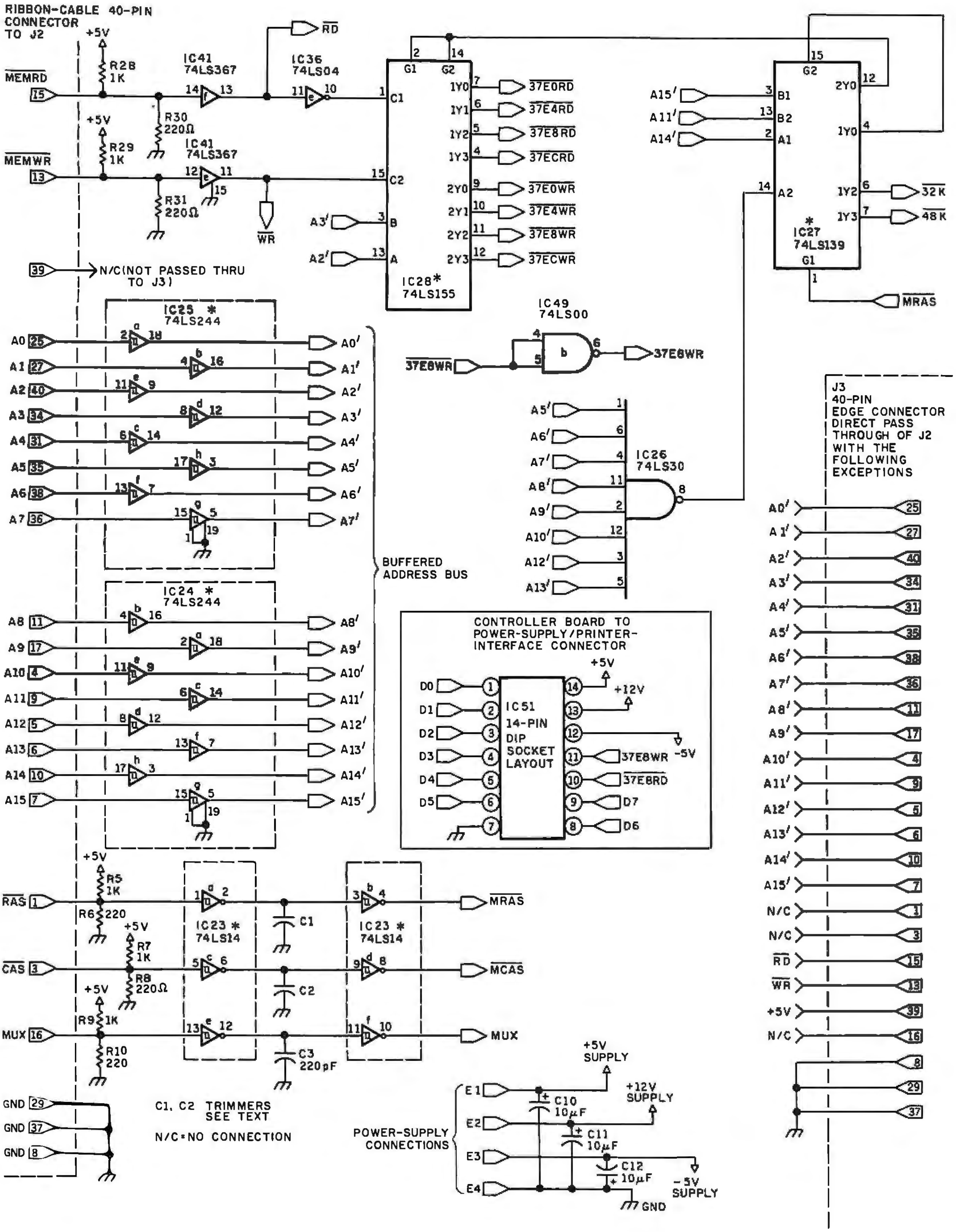


Figure 2a: *Schematic diagram of the address-decoding and buffering section of the Disk-80. Figure notes are found in the text box on page 44.*

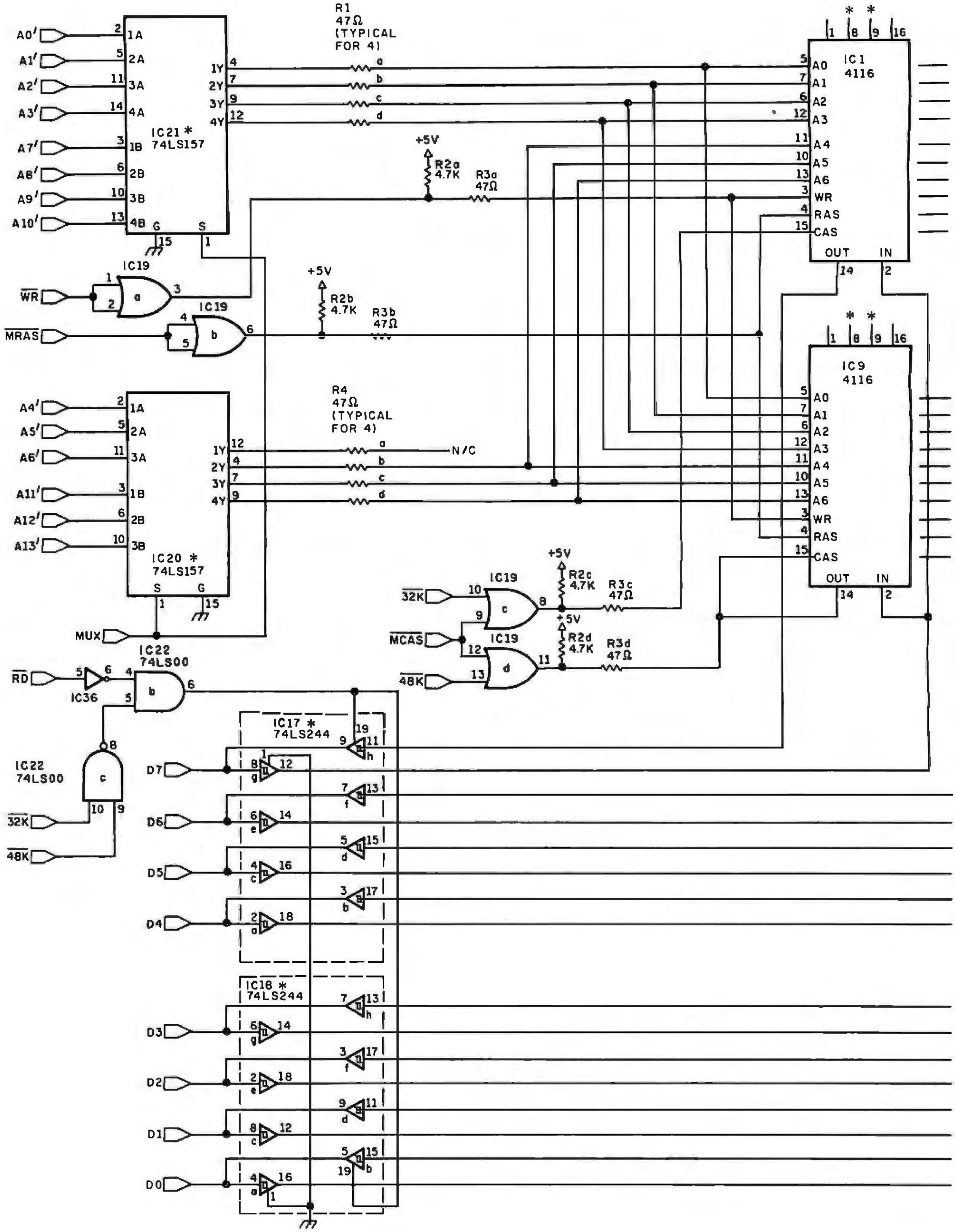
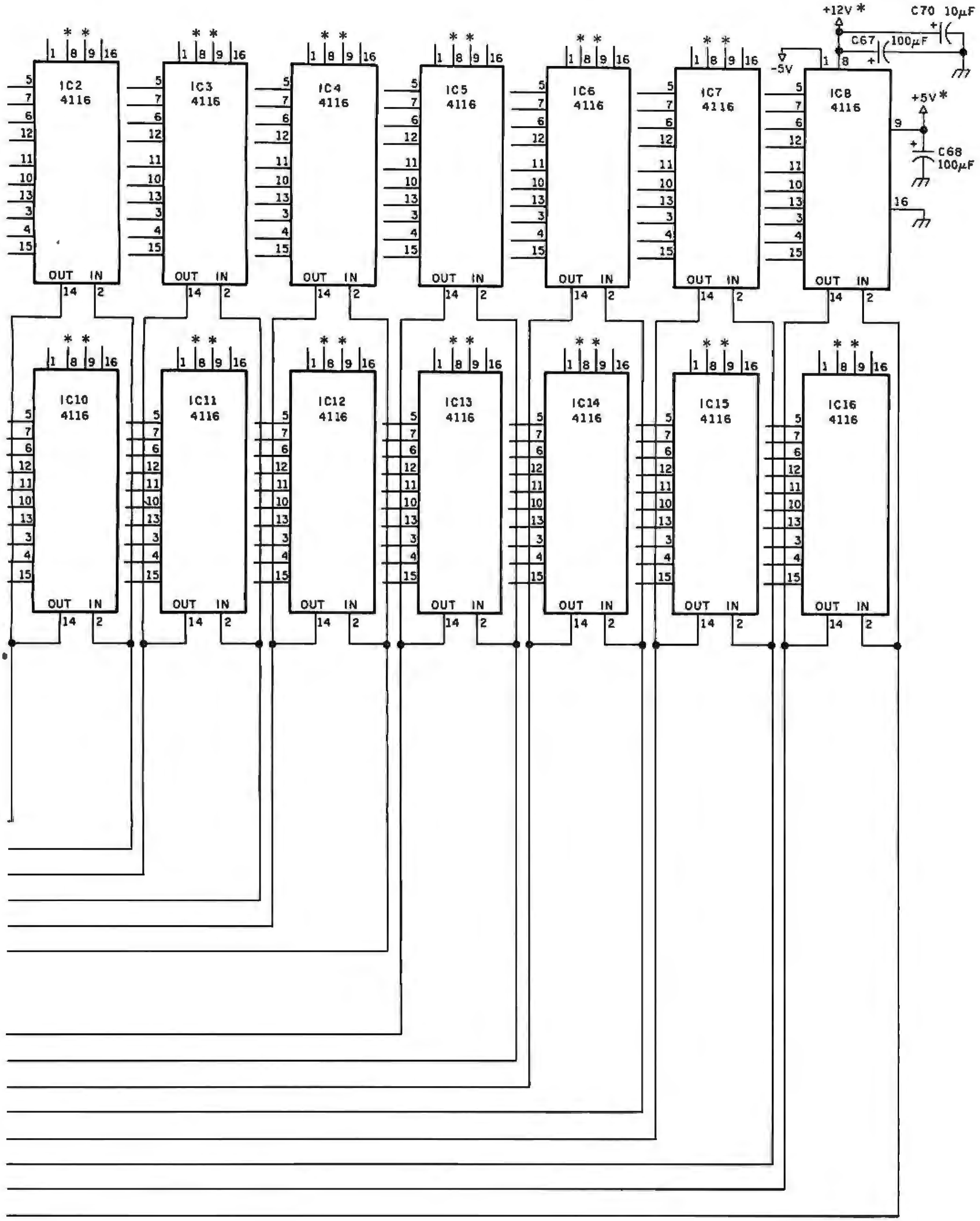


Figure 2b: *The memory-expansion section of the Disk-80 module. See notes on page 44.*


+12V *
C70 10µF
C67 100µF
-5V
+5V *
C68 100µF
IC2 4116
IC3 4116
IC4 4116
IC5 4116
IC6 4116
IC7 4116
IC8 4116
IC10 4116
IC11 4116
IC12 4116
IC13 4116
IC14 4116
IC15 4116
IC16 4116
* *
1 8 9 16
5 7 6 12 11 10 13 3 4 15
OUT IN
14 2
9
16

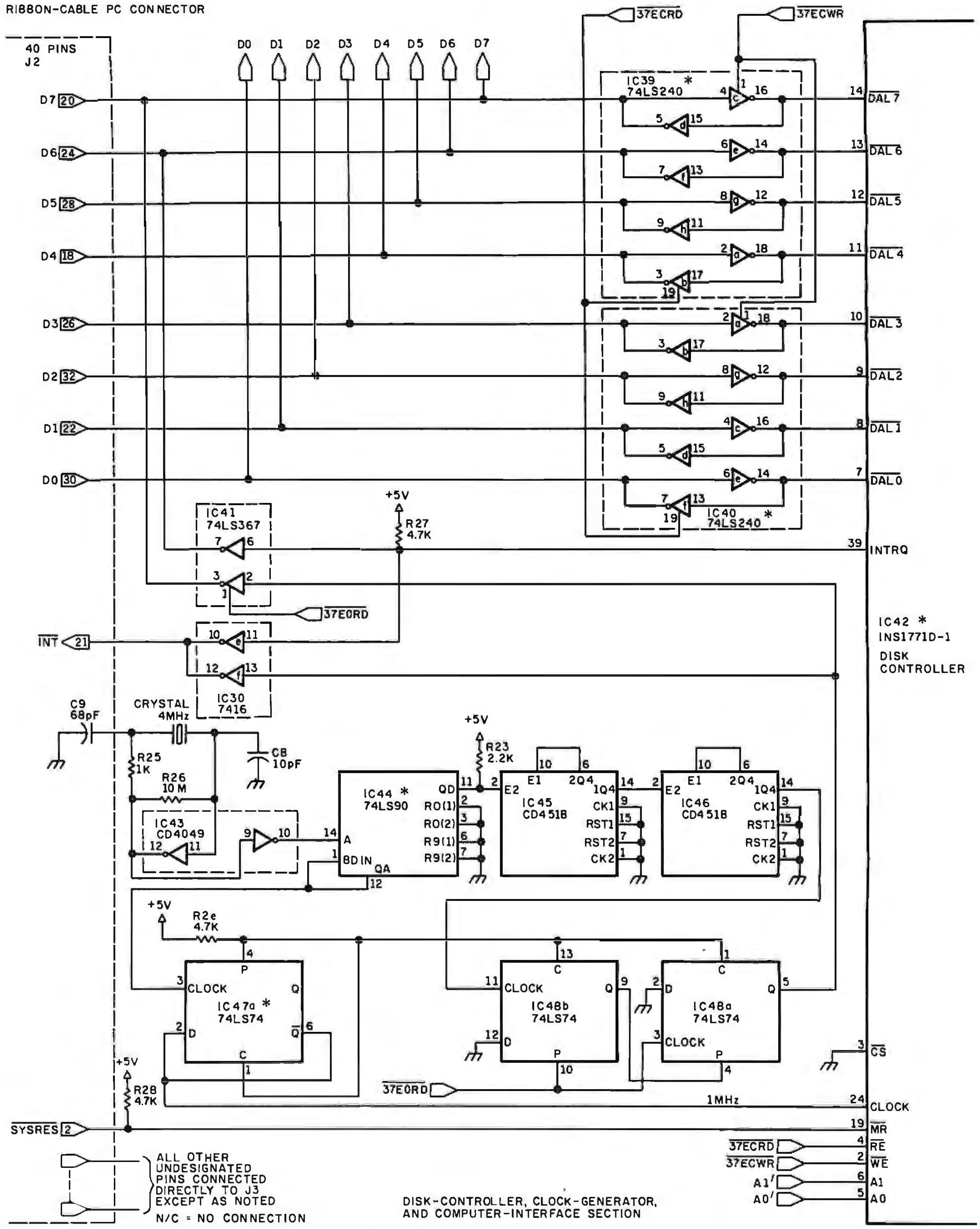
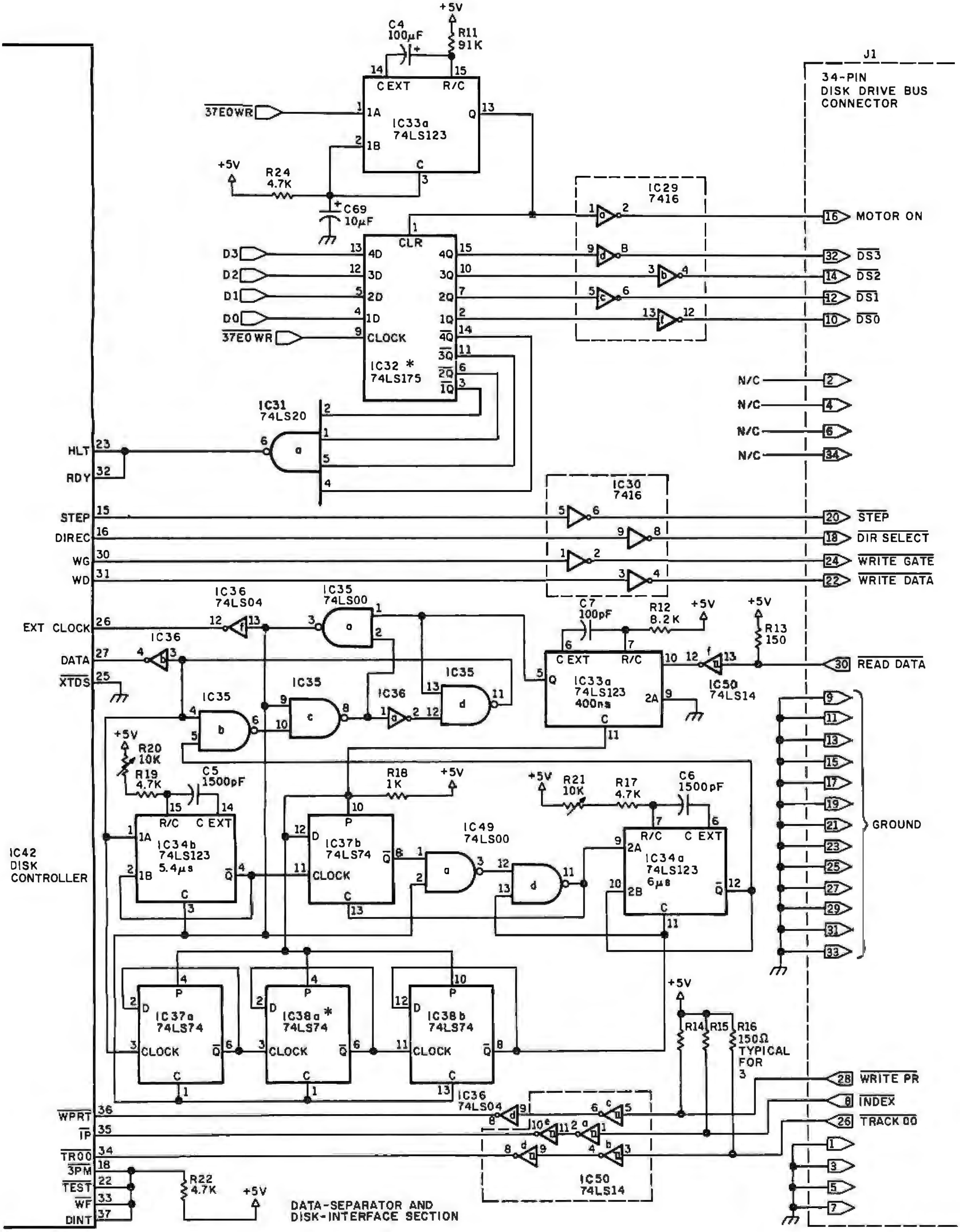


Figure 2c: *Schematic diagram of the disk-controller, clock-generator, keyboard/processor-module-interface, external-data-separator, and disk-drive-interface sections of the Disk-80 expansion module. See figure notes on page 44.*



DATA-SEPARATOR AND DISK-INTERFACE SECTION

Text continued from page 38:

depending upon the polarity of the $\overline{\text{Write Enable}}$ input. In turn, the $\overline{\text{Read Enable}}$ line controls the direction of data flow through the memory data buffers, IC17 and IC18, 74LS244 non-inverting octal buffers.

The MUX, $\overline{\text{CAS}}$, and $\overline{\text{RAS}}$ signals are generated within the TRS-80 keyboard/processor module in a 3-bit shift register. Figure 4 on page 46 illustrates, in simplified logic, the derivation of these signals.

At the beginning of each read or write cycle, the Z80 microprocessor's $\overline{\text{MREQ}}$ (memory request) line is pulled low. The $\overline{\text{MREQ}}$ signal is also used by the TRS-80 as the $\overline{\text{RAS}}$ signal. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (negative-logic read-enable and write-enable) lines are logically ORed to feed the CLR (clear) inputs and the D input of FF1, the first flip-flop in the 3-bit shift register. When either $\overline{\text{RD}}$ or $\overline{\text{WR}}$ goes low, a logic 1 is loaded into FF1 at the occurrence of the rising edge of the 10.6445 MHz master clock pulse. On the next clock pulse, the logic 1 is shifted into FF2, the second flip-flop, of which the Q output controls the MUX signal. The next clock pulse shifts the logic 1 into flip-flop FF3. The inverted Q output of FF3 is the $\overline{\text{CAS}}$ signal to memory. When the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ line goes high again, the three flip-flops are cleared and the address multiplexers are reset.

It is easy to see that multiplexing the addreses is fairly simple, especially when the signals needed are available on the 40-pin TRS-BUS connector.

Interestingly enough, Radio Shack did not use these signals in late-production TRS-80 Expansion Interfaces. Because some of the signal pulses are very short in duration (about 200 ns) and susceptible to noise, the early-production Expansion Interfaces had to have a buffered cable to eliminate memory errors. Eventually, this arrangement was

Write Strobes
37E0 — disk-drive select (1 of 4)
37E4 — not used
37E8 — printer data out
37EC — set disk-controller registers

Read Strobes
37E0 — read real-time clock/reset interrupt
37E4 — not used
37E8 — read printer status
37EC — read disk-controller registers

Table 1: *Hexadecimal memory-mapped addresses of registers used by the Disk-80 to coordinate the disk-drive controller, the printer interface, and the real-time clock.*

IC Number	Type	+5V	GND	+12V	−5V
1 thru 16	4116 (200 ns)	9	16	8	1
17	74LS244	20	10		
18	74LS244	20	10		
19	74LS32	14	7		
20	74LS157	16	8		
21	74LS157	16	8		
22	74LS00 .	14	7		
23	74LS14	14	7		
24	74LS244	20	10		
25	74LS244	20	10		
26	74LS30	14	7		
27	74LS139	16	8		
28	74LS155	16	8		
29	7416	14	7		
30	7416	14	7		
31	74LS20	14	7		
32	74LS175	16	8		
33	74LS123	16	8		
34	74LS123	16	8		
35	74LS00	14	7		
36	74LS04	14	7		
37	74LS74	14	7		
38	74LS74	14	7		
39	74LS240	20	10		
40	74LS240	20	10		
41	74LS367	16	8		
42	INS1771D-1	21	20	40	1
43	CD4049	1	8		
44	74LS90	5	10		
45	CD4518	16	8		
46	CD4518	16	8		
47	74LS74	14	7		
48	74LS74	14	7		
49	74LS00	14	7		
50	74LS14	14	7		
51	*				

Table 2: *List of integrated circuits and power-wiring requirements for the Disk-80, excluding those integrated circuits found on the optional power-supply/printer-interface circuit board. The entity marked IC51 on the schematic diagram is really a connector for the 14-conductor ribbon cable running between the power-supply/printer-interface board and the disk-controller board.*

Notes

1. *On IC1 thru IC16 (the 4116 components) the +5 V lead on each IC should have one decoupling capacitor. One decoupling capacitor should be on every other chip for the +12 V and −5 V leads, for a total of thirty-two decoupling capacitors. Careful placement of decoupling capacitors is absolutely critical to proper operation.*

2. *All other places where decoupling capacitors are required are denoted by an asterisk (*) on the diagram.*

3. *All capacitors are 12 V ceramic disk type unless otherwise noted.*

4. *All resistors are 1/4 W 5% tolerance carbon-film type unless otherwise noted.*

replaced with a circuit in the Expansion Interface that derives the MUX and CAS signals by sending RAS through a delay line. Of the three original signals, only the RAS signal, which has the longest pulse duration, is used.

If cable lengths are kept to a minimum and proper signal termination is employed, there is no good reason why any signal available from the keyboard/processor module should not be used. The Disk-80 uses a combination of active termination and Schmitt-trigger inputs to guarantee reception of all available signals.

Memory Refreshing

So far you have heard only the good things about dynamic memory. One of the less desirable characteristics is called memory refreshing. Unlike static memory, which stores data in active bistable circuits composed of three transistors, the dynamic 4116 stores its 1s and 0s in single-transistor cells that simulate capacitors. As from a capacitor, the electrical charge that represents a bit slowly drains off unless it is "refreshed." Refreshing is accomplished by *addressing* all memory cells (or a required minimum of them) on a regular basis.

The 4116 is a RAS-only-refresh device. Instead of addressing all 16,384 bit-cell locations, only the 128 rows are cycled. This type of refreshing uses only the RAS signal and is achieved in less time than methods that use both row and column addressing. Because the MUX and CAS pulses are not used, the memory is not enabled, and the refreshing does not interfere with other system operations. However, all 128 rows must be addressed at least every 2 ms to avoid loss of data.

Refresh circuits are generally binary counters that generate sequential addresses which are applied to the memory chips. The Z80 processor includes a built-in 8-bit RAS-only refresh register. During the decoding and execution of an instruction op code, the 7 bits of the refresh register contents are placed on the low-order lines of the address bus, and the MREQ line is strobed. In effect, the Z80 accomplishes "hidden refresh" as it executes its normal program. For more information on this capability, I refer you to the Zilog *Z80-CPU Technical Manual.*

Sequencing the Power Supply and Decoupling

Unfortunately, in addition to refreshing dynamic memory, a designer has to be concerned about sequencing the turning on of the power supplies. While some brands of type-4116 memory devices are more tolerant than others, the following rule must be applied: *the −5 V supply (V_{BB}) must be applied to the 4116 before the +12 V supply (V_{DD}), and the −5 V supply must remain on until the +12 V supply has been removed.* The +5 V (V_{CC}) supply is less critical, but it is best to turn it on and off synchronously with the +12 V supply. Many dynamic-memory components have been destroyed by designers not adhering to these rules.

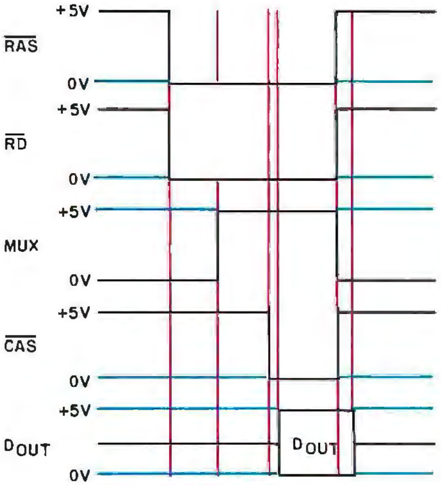


Figure 3: *RAS, CAS, and MUX timing diagram for 4116-type 16-pin dynamic-memory integrated circuit. A 14-bit address (16,384 by 1) is multiplexed into seven address pins. When MUX and RAS are low, the row-address bits are read into the 4116. Later, when MUX is high and CAS goes low, the column bits are read into the 4116, activating the data output for that memory cell.*

Supplying Power

Power-supply sequencing is important because many power supplies overshoot their rated voltages when they are turned on. If V_{BB} (−5 V) is not turned on and V_{DD} (+12 V) overshoots to more than +15 V, the chip will blow. Applying V_{BB} first provides an extra margin to prevent device destruction. Also, V_{BB} must never go positive with respect to any other input.

The Disk-80 power supply, shown in photo 3 with the optional printer interface, meets these requirements. It is designed such that the time constants of the various sections produce a phased start-up and shutdown. This sequential operation is primarily achieved by use of filter components

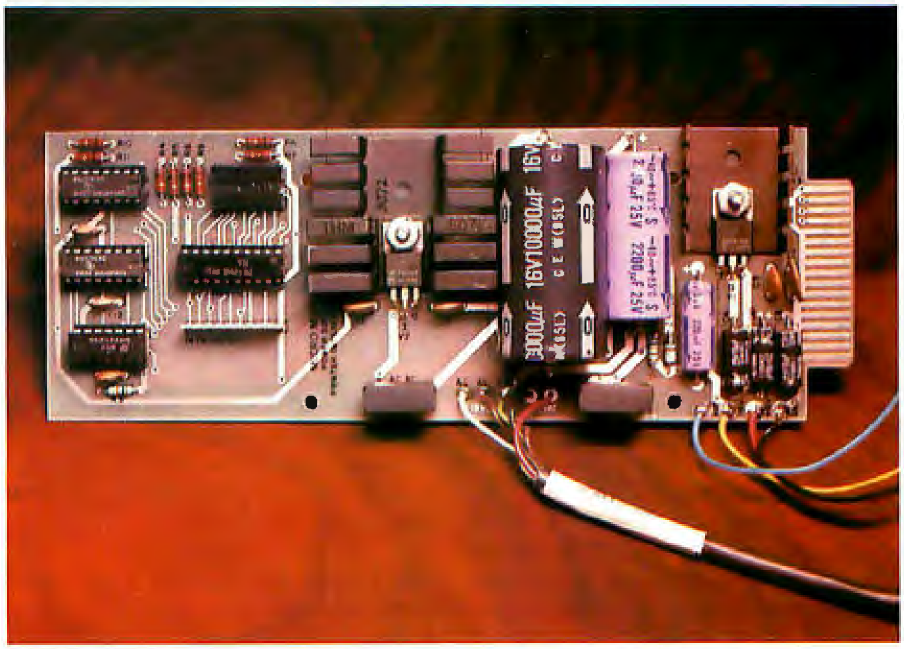


Photo 3: *The Disk-80 power supply with the parallel printer interface. The power supply provides 1 A at +5 V, 400 mA at +12 V, and 50 mA at −5 V, and is designed for use with dynamic memories such as the 4116 that require sequenced application of power.*

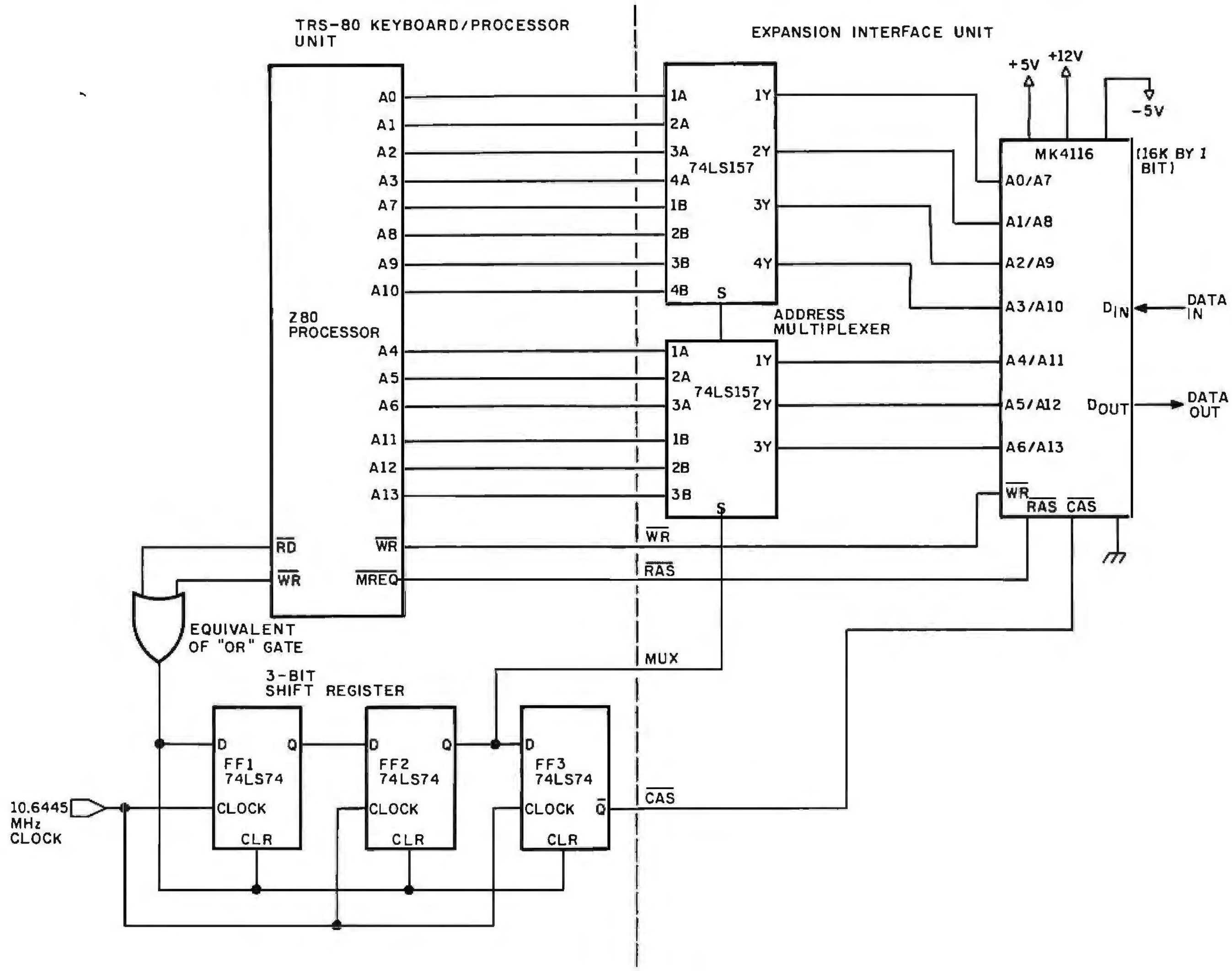


Figure 4: *Simplified schematic diagram of the internal circuitry of the TRS-80 Model I showing the derivation of the memory-refresh logic.*

that are matched to the transformer impedance. Also, because I have designed it around a transformer with specific secondary voltages, the Disk-80 power supply is very efficient and produces relatively little heat. It is designed as a separate circuit board, allowing it to be used with any project requiring power for dynamic memory. It easily powers the full fifty-four-chip Disk-80, including 32 K bytes of memory.

A Centronics-compatible parallel printer port can be optionally built on the power-supply board. A schematic diagram of this port was printed in my previous article, "I/O Expansion for the TRS-80, Part 2: Serial Ports," BYTE, June 1980, page 42.

Finally, techniques of properly distributing power and decoupling transient noise voltages must be addressed. Correct layout of the components in the Disk-80 is critical. The 4116s can generate high-current transients when in operation. Resulting voltage spikes can cause data loss unless the voltage transients are minimized by properly placed decoupling capacitors (a capacitor, usually a ceramic disk type with a value of 0.01 μF to 0.1 μF attached between power and ground).

Some suggestions that are of particular concern in the memory area of the circuit board:

- Decouple the V_{BB} and V_{DD} supply lines on every other chip.
- Distribute larger capacitors around the board to reduce supply-voltage droop.
- Decouple V_{CC} every few chips.
- Keep signal lines short.

Real-Time Clock

To be compatible with TRS-80 hardware, the Disk-80 contains a real-time clock. It provides an interrupt to the Z80 at a rate of 40 times a second (every 25 ms). When the NMI (nonmaskable interrupt) is enabled, the clock-produced interrupts cause the Z80 to transfer control to a specific ROM (read-only memory) address (the interrupt vector). Unless there is a user-supplied routine to be executed, the Z80 simply returns from the interrupt sequence and continues where it left off. Various disk operating systems for the TRS-80 use an interrupt-servicing routine called in this manner to increment a time-of-day clock or event timer.

Five-Inch Floppy-Disk Controller

The Disk-80 uses an LSI (large-

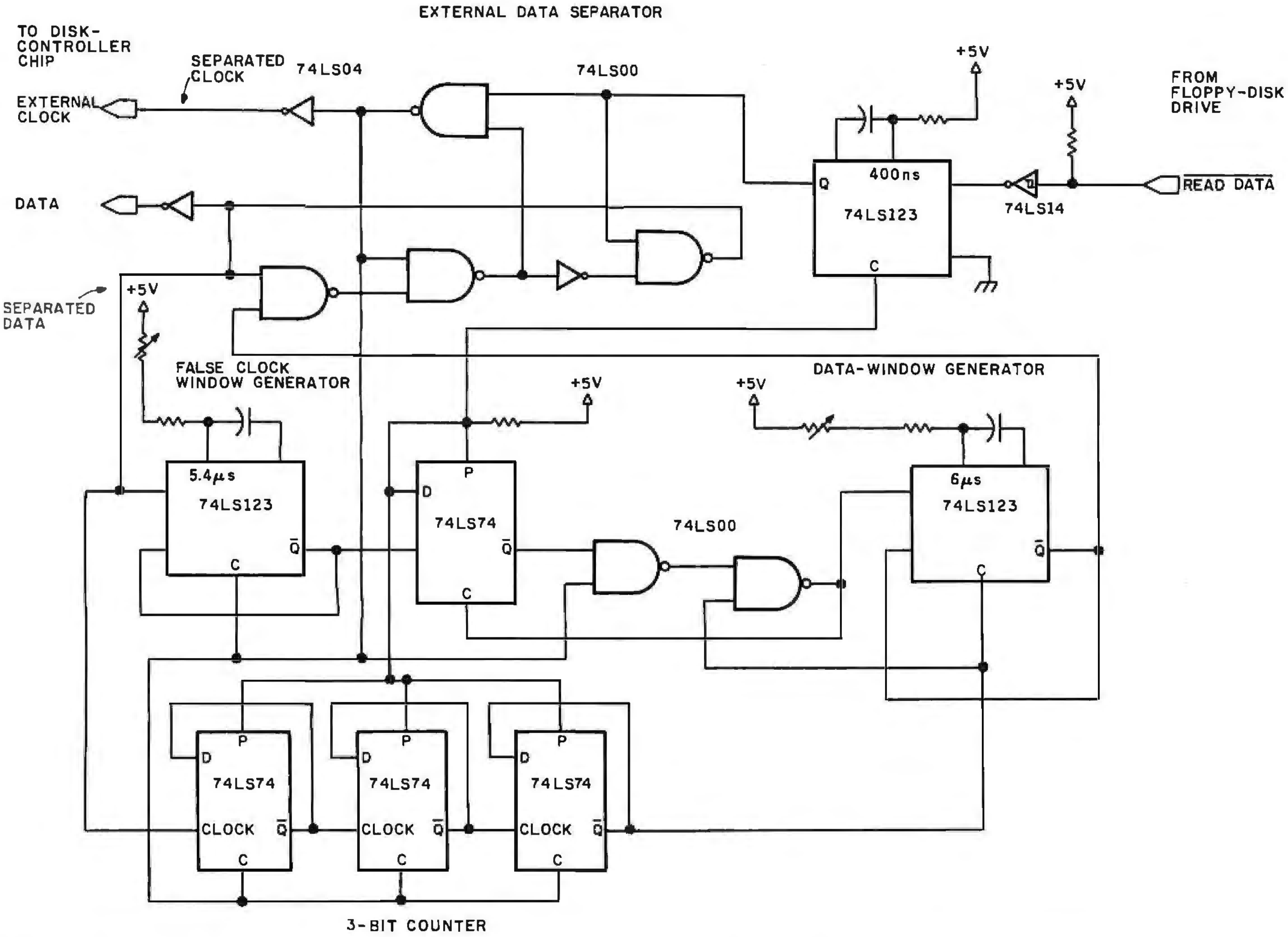


Figure 5: *Simplified schematic diagram of a 5-inch floppy-disk external data separator. The internal data separator of the FD1771 is not recommended for use in such applications. This circuit can be added to any existing TRS-80 Expansion Interface (which does not have an external data separator) to improve performance.*

scale integration) floppy-disk-controller integrated circuit. This one component performs the following functions: encoding, decoding, pattern recognition, serial-to-parallel and parallel-to-serial conversion, CRC- (cyclic redundancy check) character generation, and control of the disk-drive mechanism.

Floppy-disk controllers are available from a number of manufacturers in both single- and double-density versions. Since practically all TRS-80 Model I disk software is stored in single density, the Disk-80 uses a Western Digital FD1771-B01 single-density disk-controller integrated circuit. This component is second-sourced by National Semiconductor as the INS1771D-1.

The standard single-density 5-inch floppy-disk drive stores 110 K unformatted bytes per disk distributed on thirty-five tracks (some drives can use forty or more tracks). Using a soft-sectored format like that used in the IBM 3740 Data-Entry System, each track is divided into 16 sectors storing 128 bytes each. The total amount of data that can be stored on a disk is a function of the disk operating system and the number of tracks per disk supported by the drive itself.

The 5-inch floppy disk is rotated by a DC motor at a speed of 300 rpm. An 8-inch floppy-disk drive contains an AC synchronous motor, which spins the disk at 360 rpm. The bit density of the data is the same, but, due to the differences in rotational speed and disk diameter, the 5-inch drive transfers data at 125 kbps (thousand bits per second) as compared to the 8-inch drive's rate of 250 kbps. The 5-inch drive's lower data rate makes programmed I/O a practical transfer method. Programmed data transfer through specific registers requires less complex hardware than DMA (direct memory access) transfer.

Drive selection is handled by IC32, a 74LS175 4-bit register, and IC33a, a 74LS123 one-shot (monostable multivibrator). Only one drive is selected at a time, and the drive motors are turned off between disk accesses. To address a particular drive, a one-of-four drive code is loaded into IC32 through the memory-mapped register at hexadecimal address 37E0. This action starts a 5-second "motor-on" timer, which is activated whenever a drive is selected. It also activates the Head Load Time (HLT) control line on the FD1771. The software takes into account the 1 second required for the motor to come up to speed and the 80 ms required for head loading. Unless another access is made to this same drive, the motor will shut off

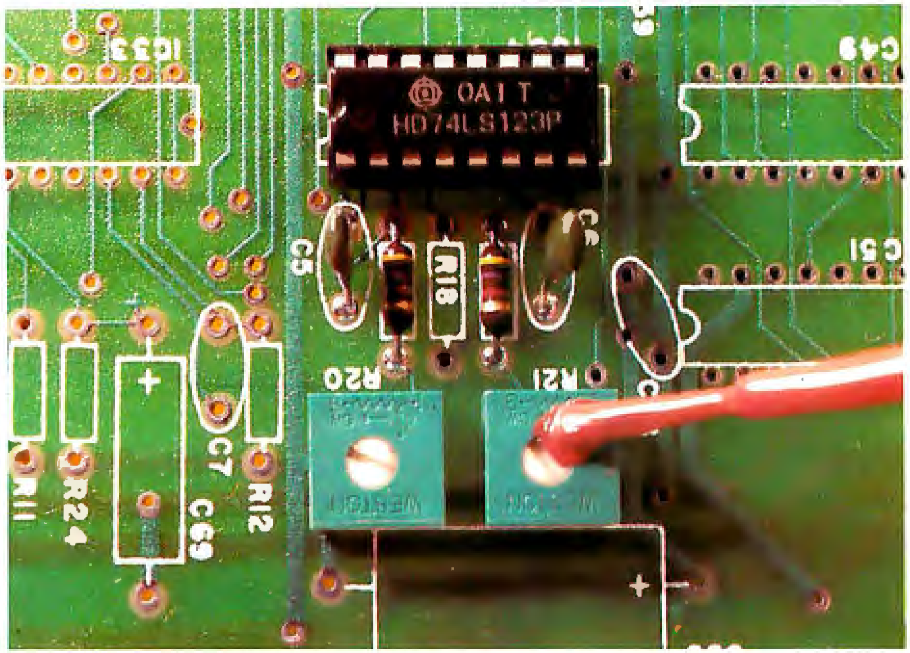


Photo 4: *External-data-separator section of the Disk-80 board. An external data separator is recommended when using the FD1771 disk controller with the 5-inch floppy disks. This circuit (shown in figure 5) can also be added to the Radio Shack TRS-80 Expansion Interface to improve performance. After setting the adjustment potentiometers, use nail polish as shown to lock their positions.*

after 5 seconds.

The Z80 bus structure makes it relatively easy to use a floppy-disk system. All data, commands, and control for the FD1771 are handled through conventional memory-reference instructions. Eight memory-mapped ports (four in and four out) handle all the communication between the Z80 and the FD1771. The range of addresses is hexadecimal 37EC to 37EF.

The Z80 controls the FD1771 through eleven commands, which are divided into four groups:

- Type I —Commands that move the read/write head: Restore, Seek, Step, Step-in, Step-out.
- Type II —Commands that read and write data: Read sector, Write sector.
- Type III—Commands that perform status checking and formatting: Read address, Read track, Write track.
- Type IV—Force-interrupt command.

An address map of Type I, II, and III FD1771 register-access functions is shown in table 3 on page 50. The commands and data are communicated to the FD1771 by setting the appropriate logic levels on address lines A0 and A1 (pins 5 and 6 on the FD1771) and strobing either the $\overline{\text{RE}}$ (read-enable) or $\overline{\text{WE}}$ (write-enable) inputs (pins 4 and 2).

Many disk-control commands require a parameter such as a track or sector address. This data must first be loaded into the appropriate register in the FD1771. To send a track address, for example, the 8-bit track address is loaded into the Z80's accumulator, and a store-accumulator [LD (HL), A] instruction to the track-register port at address 37ED is executed.

Of the FD1771's sixteen control

The following items are available postpaid in the US from:

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INS1771D-1 disk controller chip with manual	*INS1771D-1*	*$24*
16 K bytes (8 chips) of memory: 4116s, 200 ns prime units	*16 K MEM*	*$40*
Power supply complete kit: PC board and parts (add $15 for printer port and parts)	*PWR Kit*	*$38*
Disk-80 complete kit: case, power supply, printer port, cable and 16 K memory	*Disk-80 Kit*	*$275*
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lines, seven interface directly to the disk drive through drivers and receivers (type-7416 and 74LS14 components). The Write Data line transmits the digitized serial composite data to be written on the floppy disk. The Write Gate line enables the actual writing process. The Index input transmits the pulse from the index-hole photodetector that indicates the beginning of a track, and the Write Protect line tells the controller when a write-protected disk has been inserted into the drive. The Track 00 line is activated when the read/write head is positioned over track 00 (the outermost track) of the disk's surface. The Direction Select line defines the direction in which the head will move when the Step line is pulsed. Each pulse moves the head one track.

Hexadecimal Memory-Mapped	A1	A0	37EC Read Enable	37EC Write Enable
37EC	0	0	Status Register	Command Register
37ED	0	1	Track Register	Track Register
37EF	1	0	Sector Register	Sector Register
37EF	1	1	Data Register	Data Register

Table 3: *Memory-mapped addresses used by the Disk-80 to communicate with the FD1771 or INS1771 floppy-disk-controller integrated circuit. The FD1771 interacts with the Z80 processor by memory-reference instructions, not by DMA. The FD1771 can execute eleven high-level function commands.*

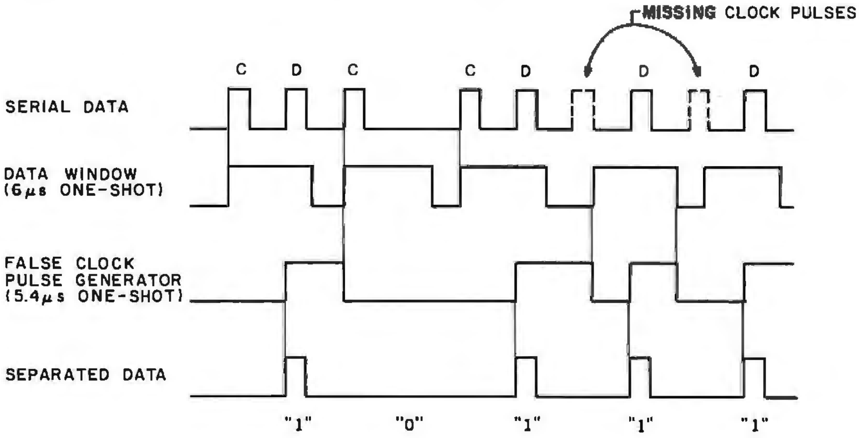

Figure 6: *Timing diagram illustrating the operation of the external data separator shown in figure 5 on page 47. Clock pulses are denoted by the letter C, data pulses by the letter D.*

An External Data Separator Is the Best Insurance

As previously mentioned, the 5-inch floppy-disk drive transfers data at 125 kbps, while an 8-inch drive transfers at 250 kbps. The difference in data rates affects the data separator's timing values as well as the clock rate used by the controller chip. The 5-inch drive requires a 1 MHz clock, while a standard 8-inch drive uses a 2 MHz clock.

Data received from the drive's electronic circuitry is a multiplexed combination of data and clock pulses. The FD1771's internal data separator can separate the data and clock bits, but use of the FD1771's *internal* data separator is *not recommended where high reliability is required.* An *external* data separator must be added to maintain a soft-error rate better than 1 in 10^8.

The internal separator operates from the 1 MHz system clock, which is not synchronous with the clock pulses of the disk data. Due to mechanical variations and other factors, sometimes a bit of data can arrive at the FD1771 at a point in time "outside the data window," that is, when the controller is not expecting it.

[**Editor's Note:** *For a more detailed explanation of the importance of the data window, see "Interface a Floppy-Disk Drive to an 8080A-Based Computer" by John Hoeppner in the May 1980 issue of BYTE, page 72....***RSS**] The nonsynchronous data window's 1 µs (microsecond) resolution can move with respect to a data bit's arrival by enough that the data bit can actually fall outside the data window. This would be interpreted as an error.

To help eliminate what has been a major problem for TRS-80 Model I disk users, *the Disk-80 includes an external data separator*. Neither the Radio Shack TRS-80 Expansion Interface nor the LNW Research System Expansion Board has an external data separator. Figures 5 and 6 illustrate the circuitry and function of the Disk-80's external data separator.

The external data separator places a 400 ns (nanosecond) one-shot on the Read Data line from the drive. This arrangement reduces the Read Data input pulse width from 1.2 µs to 400 ns. When configured for external clock and data separation, the FD1771 requires pulse widths between 300 and 700 ns. The narrower the pulse width, the better the data separator's resolution.

To produce the separator's data window, a 6 µs one-shot is triggered by the leading edge of the clock pulse. Since the time between clock pulses is 8 µs, a data bit is expected within 4 µs after the clock pulse's leading edge. The extra 2 µs allow for shifts in the phase of the data or clock bits. This is all that is required to satisfy any potential timing problems. However, since we also have to be IBM 3740 compatible, more is required.

The IBM 3740 format creates a unique addressing mark by dropping three clock pulses during the address-mark clock pattern. To produce data windows during missing clock-pulse intervals, a false clock pulse is generated with a 5.4 µs one-shot. If the 5.4 µs one-shot times out past the expected instant of the next clock pulse, its own pulse's trailing edge triggers the other (6 µs) one-shot, generating a data window.

A 3-bit counter distinguishes between missing clock pulses and address marks. If the data separator is already in phase, it is constantly reset by the separated clock output. When the separator encounters the address mark, the counter is incremented by a pulse on the separated data line. On the occurrence of the fourth missing

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clock pulse, the data window is reset. The separator becomes in-phase again on the next true clock pulse.

Photo 4 shows the location of the false-clock and data-window adjustment potentiometers, R20 and R21, on the Disk-80 circuit board. These are the only user adjustments in the unit. The best method for setting them is to use an oscilloscope and a pulse source. With only IC34 inserted in the board and the +5 V supply on, apply a 50 to 100 kHz clock pulse first to IC34's pin 1. With a scope probe on pin 4, adjust R20 until the one-shot period is 5.4 μs. A similar clock signal is applied to pin 9 of IC34: that section should be set for a period of 6.0 μs by turning R21.

In Conclusion

The TRS-80 Model I may no longer be on the minds of the marketing moguls at Tandy Corporation, but the hundreds of thousands of Model I owners will want to keep using it. Now that you know what is inside an expansion interface, you could build one, if necessary.

Correctly assembling an expansion interface from the circuit diagrams of figure 2 is more than just making all the right connections, however. Layout, decoupling, and power distribution are probably the most critical factors to be considered.

I had to be aware of these same considerations while I was designing the Disk-80, and I had a dilemma when it came time to build the prototype I do for every Circuit Cellar article. The Disk-80 uses fifty-four integrated circuits and 120 resistors and capacitors. The *placement* of these components is as important, in many cases, as the *inclusion* of the component.

To eliminate major troubleshooting headaches and make it easier for others to construct this interface, I went straight from my schematic diagram to a printed-circuit board, without breadboarding or wire-wrapping. Besides making it easier for me, the result is an elimination of the concern that experimenters would have about the placement of components and decoupling capacitors and the routing of signal lines. The printed-circuit boards are available from The MicroMint, at the address given in the text box on page 48. The schematic diagram of the power supply is not provided here because the correct sequential application of the voltages depends on the use of the exact transformer and components I specified; the circuit may not work with substitute components. If you really want a schematic diagram and a parts list for the power supply, send a stamped, self-addressed envelope to The MicroMint.

I hope that many of you will take this opportunity to build your own expansion interfaces. ■

Next Month:
Build a low-cost logic analyzer.

References
1. *Z80-CPU Technical Manual.* Zilog Inc, 10460 Bubb Rd, Cupertino CA 95014, 1977.
2. Hoeppner, John. "Interface a Floppy-Disk Drive to an 8080A-Based Computer." BYTE, May 1980, page 72.

Editor's Note: *Steve often refers to previous Circuit Cellar articles as reference material for the articles he presents each month. These articles are available in reprint books from BYTE Books, 70 Main St, Peterborough NH 03458.* Ciarcia's Circuit Cellar *covers articles appearing in BYTE from September 1977 thru November 1978.* Ciarcia's Circuit Cellar, Volume II *presents articles from December 1978 thru June 1980.*

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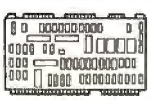
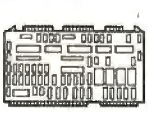
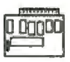
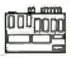
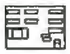
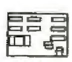
	**ISBC 80/10B Single Board Computer** 8080A-based microcomputer with one iSBX bus connector; 48 programmable I/O lines; one USART; timer; capacity for 1K-4K bytes RAM; up to 16K EPROM
	**ISBC 80/24 Single Board Computer** 8085A-2 based microcomputer operating at 4.8 MHz (2.4 MHz optional); two ISBX bus connectors; 48 programmable I/O lines; one USART; three programmable timers; programmable interrupt controller; capacity for 4K-8K bytes RAM; up to 16K EPROM
	**ISBX 311 Analog Input Multimodule** 8 or 16 input channels, voltage protected; 12-bit resolution; ±20 mV to 5V full scale; 20 kHz samples/sec; compatible with iCS 910 Signal Conditioning Termination Panel
	**ISBX 328 Analog Output Multimodule** 8 channels of analog output; voltage or 4-20 ma current loop; 12-bit resolution; compatible with iCS 910 Screw Termination Panel
	**iSBX 331 Fixed/Floating Point Math Multimodule** Fixed point single- (16-bit) and double- (32-bit) precision arithmetic; floating point single- (32-bit) precision functions; floating-to-fixed and fixed-to-floating point conversions; transcendental functions
	**iSBX 332 Floating Point Math Multimodule** Single- (32-bit) and double- (64-bit) precision arithmetic; compatible with proposed IEEE format and existing Intel floating point standard

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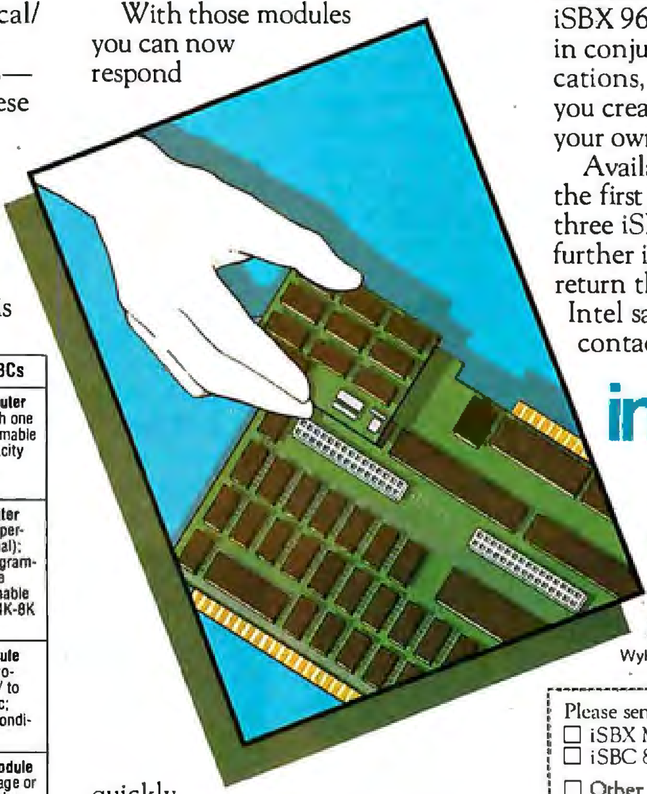

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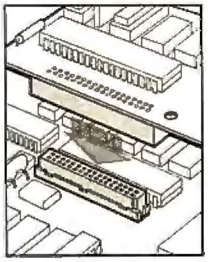

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Three-Dimensional Computer Graphics, Part 1

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The process of generating computer representations of three-dimensional structures has been pretty thoroughly worked out over the past fifteen years. Several books on computer graphics describe the necessary steps and commercial graphic software has been available for some time. Recently, three-dimensional graphic software has been made available even to those using microcomputers for personal or recreational purposes.

The software necessary for producing representations of simple shapes is not terribly complicated. In this article, I will try to lay out a few fundamental algorithms that can form the core of a three-dimensional graphics package. However, in order to make sense of these algorithms, considerable explanation will be necessary.

To generate an image of a three-dimensional shape, we have to have a computer-readable representation of the shape. (I will describe a couple of ways to represent shapes.) Then the data for the shape must be transformed to conform to the view of the shape that would be seen from a given point. The data must then be further transformed to fit the shape to the limits of a display surface (video display or plotter). Finally, those parts of the shape that are hidden from view, either because they exceed the limits of the display or because they are hidden by other parts of the shape, must be eliminated.

Getting the Data

The first decision to be made when generating three-dimensional data for input to a graphics system is which coordinate system to use. A right-handed Cartesian system is most often used. Standing at the origin of such a system, the x axis would go to the right, the y axis straight ahead, and the z axis straight up. If we think in terms of a small area of the earth, x would measure longitude (east positive, west negative), y latitude, and z altitude.

Points in this space can be defined as a trio of numbers giving x, y, and z coordinates. A three-dimensional drawing of an object can then be considered a set of lines connecting points in space. An object can be described by listing all its points in the order in which we would draw them. We can then draw the object by "following the dots."

However, we rarely see drawings that are made without ever lifting pencil from paper, so we should add an indicator wherever we move to a point without drawing a line. Thus one format for describing objects consists of a list of sets of numbers. Each set contains three numbers describing a position in space and a command to draw a line to that position or just move to that position without drawing a line, a total of three numbers and a character. An example of this format can be seen in figure 1a, with the associated data given in table 1a. The Pascal procedures given in listing 1 (on page 70) read and display objects defined in this format.

This format is fine if we just want to make drawings of objects that appear to be constructed of straight pieces of wire. To represent a solid object, we have to define a surface enclosing the object and therefore need another format. Surfaces are most easily represented if we define them as sets of faces, or polygons.

To define objects made of polygons, we must list the polygons individually. This can be done by listing the coordinates of each vertex (point) of the polygon in clockwise order (as seen from outside the object) around the periphery of the polygon. It is important that all polygons be described consistently since the clockwise order is useful for calculations determining which side of a polygon is facing the viewer.

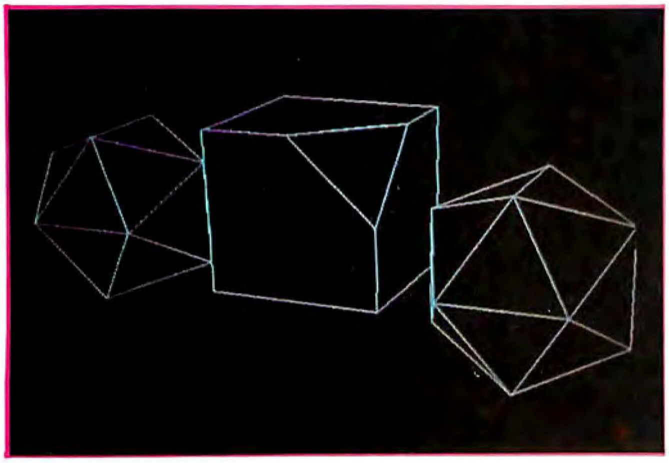

Photo 1: *High-resolution display of solid three-dimensional objects defined as sets of polygons.*

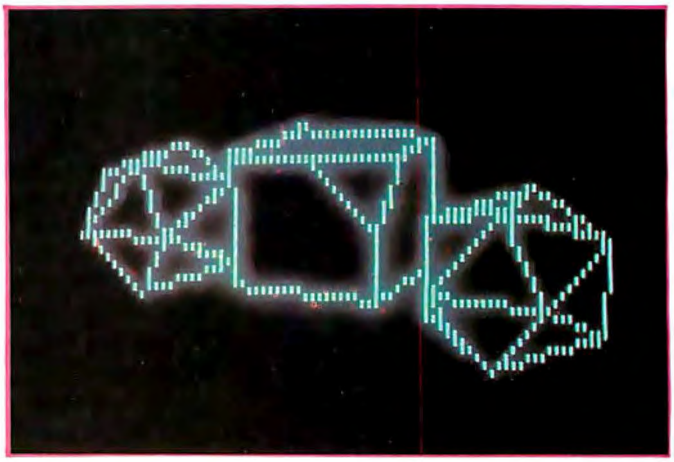

Photo 2: *Low-resolution display of the same objects as in photo 1.*

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A solid object is customarily defined as a group of adjoining polygons. Since neighboring polygons share vertices along common borders, objects can be more compactly defined by first listing all the vertices belonging to the object and then listing polygons by the numbers of the vertices they use. An example of this sort of format is seen in figure 1b, with data in table 1b. The procedures in listing 2 read and display objects as a set of polygons.

Now that we know how to read and display objects, where do we get the data describing the objects? The simplest way is to dream it up. After all, much of the joy of computer graphics lies in creating imaginary worlds. Take a piece of graph paper and draw front and side views of an object you'd like to represent. Then measure the vertices of the object by counting squares from some point of origin on the paper. The front view will give you the x and z coordinates, and the side view will give you the y coordinate (see figure 2).

People who are involved in creating three-dimensional graphics generally build software to aid in designing objects. For example, a program to generate surfaces of revolution is relatively easy to write. Then shapes such as wine glasses and vases are easy to make. A surface of revolution can be defined by a sequence of points following a path up one side of the surface. The points then sweep out a surface by rotating about a central axis. Surfaces of revolution are widely used in computer imagery.

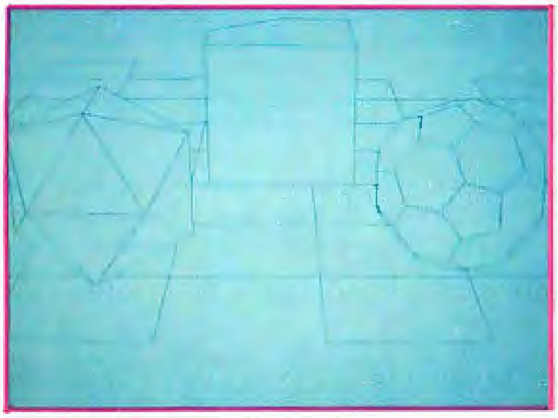

Photo 3: *Removal of hidden surfaces can be clearly observed in this display generated on a custom graphics display unit connected to a Digital Equipment VAX 11/780.*

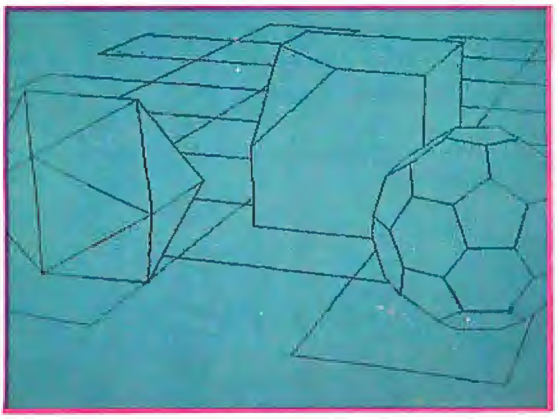

Photo 4: *Transformation of a scene due to a change in the location of the eyepoint as well as transformation of the objects within the scene. Compare with photo 3.*

More advanced techniques make use of high-speed interactive graphics terminals (costing $20,000 to $150,000) in conjunction with elaborate software to define and modify shapes. See the papers by Crow and Parent (listed among the suggested readings at the end of this article) for examples of this approach to data gathering.

Defining a View of Some Objects

Once data describing an object is available, it is time to figure out how to look at it. In the real world, when we look at an object, what we see is determined by our viewpoint and the position of the object. How can we emulate this in an imaginary world?

We want the choice of viewing an object from any viewpoint. Therefore we must have an algorithm that will move the vertices of the object to the proper position, given a particular viewpoint. The input to this algorithm consists of two points in space: the position from which we are looking and the position at which we are looking. I will refer to these as the *eyepoint* and the *center of interest*, respectively.

In order to understand how such an algorithm works, we need to know more about how to move objects about in an imaginary world. So far I have defined an object within its own space or frame of reference. Now we would like to arrange a number of objects in a scene, each in a different position and orientation.

Changing the position of an object is relatively simple. Using the longitude, latitude, altitude model of space, we can move an object east by simply adding some positive number to the x coordinates of all its vertices. To move an object north, we add some positive number to all its y coordinates. To move an object up or down, we change all its z coordinates. This process is called *translation*.

Similarly, to change the size of an object we multiply all its coordinates by the same number. This is called *scaling*. To make an object twice as large in every dimension, we multiply all coordinates of every vertex by two. Thus, changing the position or size of an object is relatively straightforward. Rotating an object or combining successive operations, however, requires more sophisticated techniques.

Objects can be moved about quite elegantly using techniques provided by matrix algebra. We devise a sort of template that is filled in to provide the operation desired. Filled templates, called *transformation matrices*, can then be combined to provide complicated operations.

A template, or *matrix*, consists of sixteen positions (four rows by four columns). Numbers loaded into a matrix are combined with vertex coordinates to yield updated coordinates by matrix multiplication. The first column of the matrix affects only the x coordinate and therefore contains all the numbers that define the updated x coordinate. The second column treats the y coordinate similarly, and the third column handles the z coordinate. The fourth column is for completeness, to make things more elegant. It also allows us to pull some fancy tricks such as finding the inverse of a transformation. I won't use the fourth column in this article, however.

A vertex is "transformed" by the matrix as follows: To get the new x coordinate, the old x coordinate is

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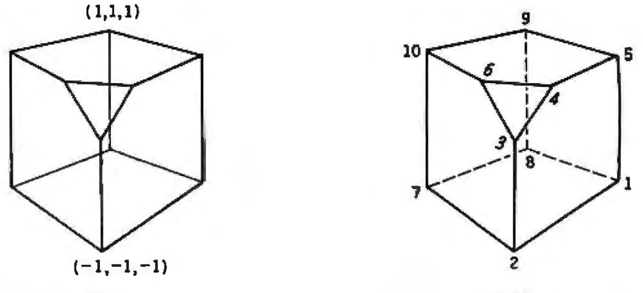
1a

```
m     1.0  -1.0  -1.0
d    -1.0  -1.0  -1.0
d    -1.0  -1.0   .00
d    -.00  -1.0   1.0
d     1.0  -1.0   1.0
d     1.0   1.0   1.0
d     1.0   1.0  -1.0
d     1.0  -1.0  -1.0
d     1.0  -1.0   1.0
m    -1.0  -1.0   .00
d    -1.0  -.00   1.0
d    -1.0   1.0   1.0
d    -1.0   1.0  -1.0
d    -1.0  -1.0  -1.0
m    -1.0  -.00   1.0
d    -.00  -1.0   1.0
m    -1.0   1.0  -1.0
d     1.0   1.0  -1.0
m     1.0   1.0   1.0
d    -1.0   1.0   1.0
```

1b

```
    10     7    (NumPts NumPolys)
 1     1.0  -1.0  -1.0
 2    -1.0  -1.0  -1.0
 3    -1.0  -1.0   .00
 4    -.00  -1.0   1.0
 5     1.0  -1.0   1.0
 6    -1.0  -.00   1.0
 7    -1.0   1.0  -1.0
 8     1.0   1.0  -1.0
 9     1.0   1.0   1.0
10    -1.0   1.0   1.0
    5    1   2   3   4   5
    4    8   1   5   9
    4    7   8   9  10
    5    2   7  10   6   3
    4    8   7   2   1
    5    5   4   6  10   9
    3    3   6   4
```

Table 1: *Data for an object defined as a set of lines (table 1a) and for an object defined as a set of polygons (table 1b). In table 1a, the "m" and "d" in the first column mean "move to" or "draw to" the point with x, y, and z coordinates as given in the next three columns, respectively. In table 1b, the first line gives the number of points (10) and polygons (7) in the shape. The next 10 lines give the point number (1 thru 10) and the x, y, and z coordinates of the point. The last seven rows describe the seven polygons: the first number gives the number of points making up that polygon, and the rest of the numbers on that line give the point numbers (as described by the point description lines) that make up the polygon. Both tables 1a and 1b describe the shape shown in figure 1b.*



(1a) *(1b)*

Figure 1: *Three-dimensional object displayed as a set of straight lines defined by 10 points (figure 1a) and a set of polygons defined by using the same points (figure 1b). See table 1 for associated data.*

multiplied by the top number in the first column, then added to the product of the old *y* coordinate and the second number in the first column. The sum is then added to the product of the old *z* coordinate and the third number in the first column. Finally, the whole thing is added to the bottom number in the first column. The new *y* coordinate can be obtained by combining the second column and the old vertex coordinates in the same way. Similarly, the new *z* coordinate is produced using the third column. The Pascal procedure in listing 3 (on page 70) transforms a vertex.

Under the rules stated above, the bottom row of the matrix holds numbers that translate the object. A number at the bottom of the first column is added to all *x* coordinates to move an object east or west. Similarly, numbers at the bottom of the second and third columns affect the *y* and *z* coordinates. To scale objects, we enter the scaling factor along the top-left-to-bottom-right diagonal of the matrix. The top-left number in the matrix is multiplied by the old *x* coordinate to yield the new *x* coordinate. Similarly, the second number in the second column multiplies the *y* coordinate and the third number in the third column multiplies the *z* coordinate.

Rather than trying to explain rotations in the limited space here, I will simply illustrate how to fill in the matrix. Trying a few examples by hand should convince you that rotations work. Simple rotations are those that rotate an object about one of the axes of our space. For instance, to rotate an object about the *z* axis by an angle A, use the following matrix:

$$\begin{array}{cccc} \cos(A) & \sin(A) & 0 & 0 \\ -\sin(A) & \cos(A) & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{array}$$

Note that this matrix leaves the *z* coordinate unchanged, which is what we would expect from a rotation about the *z* axis. Furthermore, a rotation through a zero angle leaves everything unchanged since the cosine of zero is 1 and the sine of zero is 0.

I always use the convention that a positive rotation occurs in a counterclockwise direction looking in the negative direction along the axis about which you are rotating. This means that if the thumb of your right hand is pointed in the same direction as that axis, your fingers will curl in the direction of positive rotation. Keeping

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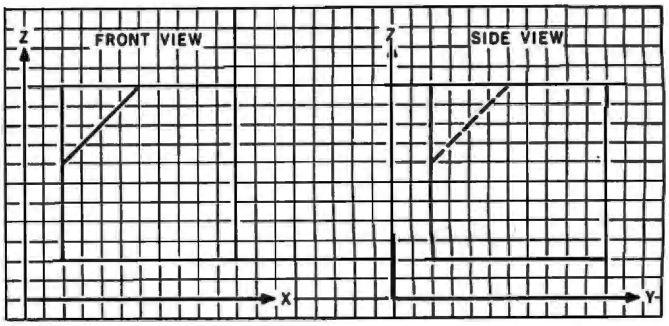

Figure 2: *Vertices for objects to be displayed in three dimensions may be measured from front and side views laid out on ordinary graph paper.*

track of such things requires a strong sense for visualizing space. When in doubt, I sketch things with pencil and paper.

To rotate about the x axis, use the following matrix:

$$\begin{matrix} 1 & 0 & 0 & 0 \\ 0 & \cos(A) & \sin(A) & 0 \\ 0 & -\sin(A) & \cos(A) & 0 \\ 0 & 0 & 0 & 1 \end{matrix}$$

To rotate about the y axis, use the following matrix:

$$\begin{matrix} \cos(A) & 0 & -\sin(A) & 0 \\ 0 & 1 & 0 & 0 \\ \sin(A) & 0 & \cos(A) & 0 \\ 0 & 0 & 0 & 1 \end{matrix}$$

Combining these fundamental rotations results in even more interesting rotations.

Note that all transformations occur relative to the origin of the given space. Thus, to rotate or scale an object without changing its position, we must first be sure that it is centered on the origin. Therefore, a rotation or scaling "in place" (ie: without changing position) requires a translation to center on the origin, followed by rotation or scaling, then a second translation back to the original position.

Once all the objects in a scene have been transformed to the desired positions and orientations, a view from a given eyepoint in the direction of the object of interest is simulated by an additional transformation that places the object in the desired position and orientation. This simulation can be achieved by combining a few rotation matrices.

In the first step, we move everything so that the eyepoint lies at the origin of the space and the center of interest lies on the y axis, or due north. To do this, we translate the eyepoint to the origin and apply the same matrix to all the other data. The translation matrix is as follows:

$$\begin{matrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ -\text{Eye.X} & -\text{Eye.Y} & -\text{Eye.Z} & 1 \end{matrix}$$

where Eye.X, Eye.Y, and Eye.Z are the x, y, and z coordinates of the eyepoint.

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A rotation about the z axis can now be used to move the center of interest in a northerly direction. In particular, we move the center of interest into the plane defined by the y and z axes. The angle of rotation is found by passing the center of interest through the eyepoint translation matrix defined above and then applying the following formulas:

$$\cos(A) = C1.Y/\sqrt{(C1.X)^2 + (C1.Y)^2}$$
$$\sin(A) = C1.X/\sqrt{(C1.X)^2 + (C1.Y)^2}$$

where *A* is the angle of rotation and C1.X and C1.Y are the *x* and *y* coordinates of the translated center of interest, respectively (see figure 3).

The process of moving the center of interest onto the *y* axis is completed by rotating the object about the *x* axis, using the following formulas:

$$\cos(A) = C2.Y/\sqrt{(C2.Y)^2 + (C2.Z)^2}$$
$$\sin(A) = -C2.Z/\sqrt{(C2.Y)^2 + (C2.Z)^2}$$

where C2.Y and C2.Z are, respectively, the *y* and *z* coordinates of the translated and rotated center of interest (see figure 4).

Because all this is done with the intention of displaying the resulting coordinates on a flat surface, one more transformation is called for. It is useful to think about the display surface (video display, plotter, etc) as a space in which the *x* axis measures width, the *y* axis height, and the *z* axis depth. We can place our transformed coordinates into this space by interchanging the *y* and *z* axes, using the following matrix:

$$\begin{matrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{matrix}$$

Given coordinates for an eyepoint and a center of interest, we can use the matrix multiply procedure to combine the above operations into a single orientation for displaying a view of the scene. The procedure in listing 4 (on pages 70 and 72) builds such a matrix. We refer to the resulting arrangement of a scene as the *eyespace*.

Clipping

Once all the data in the scene is transformed to the eyespace, we must decide how much of the scene fits on the display. The display can be thought of as a window into an imaginary world. Things such as the size of the window and our distance from it determine what can and cannot be seen: We can use the edges of the window and the origin of the space (ie: the eyepoint) to define planes that clip parts of polygons not visible through the window (see figure 5).

The clipping window defines the *field of vision* in much the same way that the film gate and lens in a camera limit the field captured by the film. The window can be defined as a polygon corresponding to the boundaries of the display as we expect to view it. For example, if we are in the habit of looking at a 12-inch video display from a distance of 16 inches or so, the clipping window should be a rectangle about 6 inches high and 8 inches across, located 16 inches from the eyepoint.

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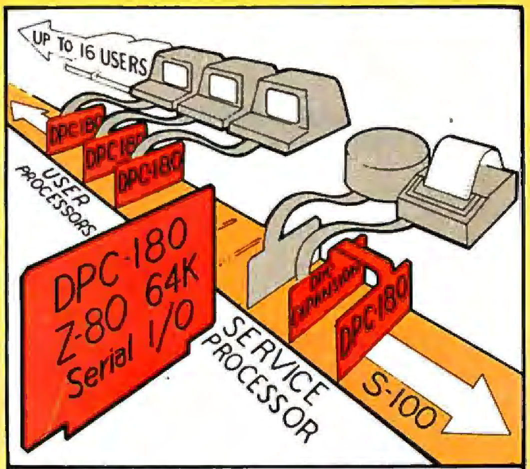

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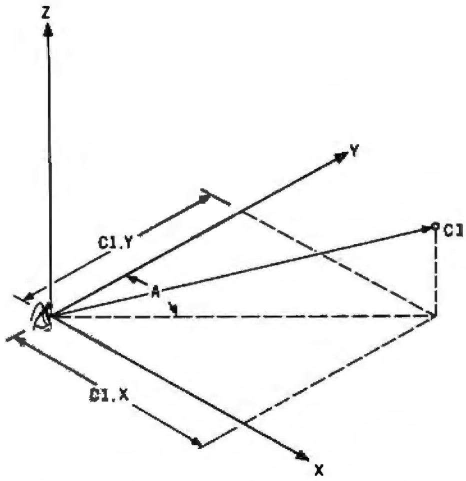

Figure 3: *Graphical representation of calculating the rotational angle about the z axis in computing the eyespace matrix.*

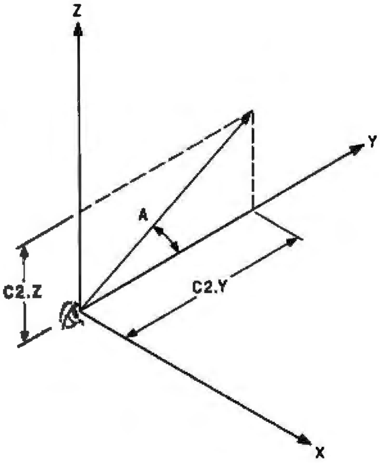

Figure 4: *Graphical representation of calculating a rotation about the x axis.*

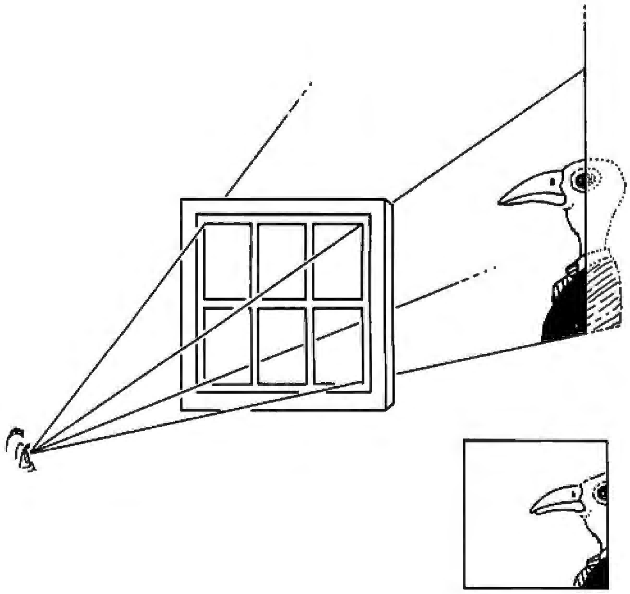

Figure 5: *Representation of how a viewing window "clips" portions of polygons lying outside the pyramid defined by the window and the eyepoint.*

The first step of the clipping process is to define the planes to be clipped against. Planes can be defined by four numbers, the coefficients of an equation of the following form:

$$A \times x + B \times y + C \times z + D = 0$$

We can simplify this equation somewhat since all the planes we are interested in pass through the origin. For all planes passing through the origin, the fourth coefficient, *D*, equals zero.

Our window can then be characterized by a sequence of sets of three numbers, each set describing one plane. Listing 5 produces the coefficients of the plane equations needed for clipping. Input is assumed to be a polygon. Each clipping plane is determined by three points: the eyepoint and the two endpoints of an edge from the input polygon. This assumes that polygon vertices are taken clockwise as seen from the eyepoint and that a "left-handed" (width, height, depth) eyespace is used.

Once we have the clipping-plane coefficients, they can be applied to all the vertices of a polygon to find out which lie inside and which lie outside the field of view. The clipping coefficients are applied to a vertex using the following formula in Pascal style:

```
Distance : = Vtx.X * Clp.X + Vtx.Y * Clp.Y +
             Vtx.Z * Clp.Z
```

This operation (known as a vector *dot product*) yields a distance measure that tells us how far inside or outside the viewable area the vertices lie. Negative numbers indicate that a vertex lies outside, positive numbers that a vertex lies inside. If distances for all clipping planes applied to all vertices of a polygon are positive, it is completely visible. If distances for all vertices and any of the clipping planes are negative, the polygon is entirely outside the window and thus not visible (assuming the clipping window is convex). If some distances are positive and some are negative, we may have to cut the polygon into inside and outside portions.

The procedure in listing 6 takes a polygon and clips it by a set of plane coefficients stored in a second polygon array. Each plane is tested in turn against each polygon vertex. Vertices lying inside (on the positive side of) a plane are copied to a temporary polygon array. Where two adjacent vertices are found to lie on opposite sides of a plane (ie: $D1 \times D2 < 0.0$, meaning the signs of the distances are different), the intersection point of the clipping plane and the edge connecting the two vertices is copied to the temporary array. When all the vertices of the polygon have been clipped against one plane, the temporary array is copied back into the input array and clipped against the next plane. This process eliminates parts of polygons lying outside an unbounded pyramid emanating from the eyepoint and delimited by the window polygon.

Displaying

Any polygon found to lie within the field of vision must be displayed. An additional transform is necessary to take the coordinates of the eyespace to the coordinates used by the display device, the "screen space." Furthermore, a division is necessary to achieve the appearance of

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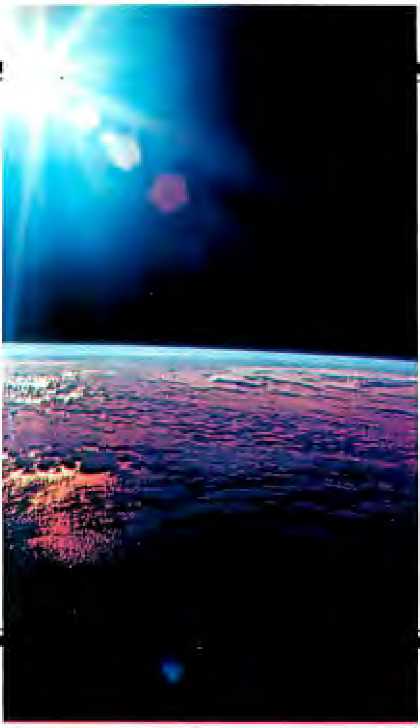

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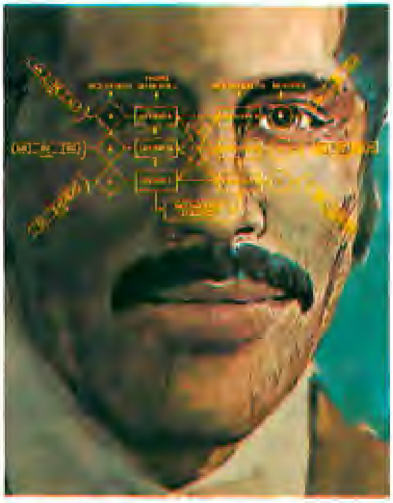

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perspective (ie: objects in the distance should be smaller). This transform can take the form of a scaling matrix as follows:

Scale.X : = DotsAcross * WinDist/WinWidth
Scale.Y : = DotsDown * ($^4/_3$) * WinDist/WinWidth

The matrix is then:

$$\begin{matrix} \text{Scale.X} & 0 & 0 & 0 \\ 0 & \text{Scale.Y} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ \text{Middl.X} & \text{Middl.Y} & 0 & 1 \end{matrix}$$

In the above transform, DotsAcross is the number of dots across the display, DotsDown the number of lines on the display from top to bottom, WinDist the distance to the window in eyespace, WinWidth the width of the window, and Middl.X and Middl.Y are the *x* and *y* coordinates of the middle of the display (in screen space, usually DotsAcross/2 and DotsDown/2). The factor ($^4/_3$) takes into account that the standard video display is $^4/_3$ as wide as it is high (the *aspect ratio*). It is assumed that the window has the same proportions as the display.

Nonrectangular windows require a more careful calculation. If the maximum width of the window is less than $^4/_3$ times the maximum height, another number must be substituted for the window width in the above calculations. That number should be the maximum of the window width and $^4/_3$ times the window height. Of course, if we use a display with a different aspect ratio, the width of the display divided by its height should replace the $^4/_3$.

The procedure in listing 7 divides the *x* and *y* coordinates of each vertex by its *z* coordinate to achieve the perspective effect, then applies the transformation to display coordinates directly, rather than using a matrix transformation.

This completes the process of computing an image of objects with all data shown, as though the objects were made of pieces of straight wire. Next, we look at how to achieve the appearance of solid objects capable of hiding each other.

Hidden Faces

There are two methods that allow solid objects to hide parts of themselves or other objects. The first uses the plane equation of each polygon to determine whether or not it lies on the far side of its object. If it does, the polygon is clearly hidden by closer parts of the object. The second uses a clipping procedure similar to the one described earlier to remove parts of faces that are hidden by closer faces.

In everything that follows, polygons are assumed to be convex. Restricting things in this way simplifies the task considerably at a very small increase in the cost of preparing object descriptions.

Earlier in the article, I stressed the importance of taking the vertices of all polygons in a consistent order, usually clockwise as seen from outside the object. Many objects are closed surfaces, meaning that the inside of the object can be seen only by passing through the surface. In fact, if we choose to do so, we can construct all objects as closed surfaces for display purposes.

In any event, if a polygon appears on the screen with its vertices in counterclockwise order, we must be seeing it from the inside. If we are looking at a closed surface from the inside, some other part of the surface must lie between us and the polygon in question. Therefore, when making pictures of solid objects made of closed surfaces, we can immediately reject any polygons appearing in counterclockwise order.

Earlier we used planes for clipping by evaluating the positive or negative distance from a point to the plane. Similarly, when the eyepoint lies on the positive side of the plane of a polygon, the vertices of that polygon appear in clockwise order. When on the negative side, they appear in counterclockwise order. Some of the procedures developed earlier can be used to determine whether or not a polygon "faces the eyepoint."

Three of the vertices of the polygon define a plane. Here we can use the procedure developed earlier for finding a plane defined by two window vertices and the eyepoint. Use the three points to define two lines. If the two lines are treated as direction vectors (subtract one endpoint from the other), the two vectors can be passed to the procedure, which then returns coefficients for a plane parallel to the polygon and passing through the origin. These coefficients, when used in a dot product with one vertex of the polygon, yield a number that tells us on which side of the polygon the eye lies. The function in listing 8 does the job.

If a closed convex surface is being displayed by itself, the above process is adequate to produce the image with only visible faces shown. However, if the surface is not convex, or there is more than one object involved, further procedures are necessary.

Those polygons surviving the clipping procedure and the "eye-facing" test can be sorted by their distance from the eyepoint. We base the sort on the average of the *z* coordinates of each polygon in turn. If all polygons are roughly the same size, no two polygons intersect each other, and no two polygons lie close to each other in nearly parallel planes, the sort order will allow us to eliminate hidden parts of polygons. Most scenes involving separated, reasonably simple objects will conform to the above conditions.

Since the polygons must be transformed, clipped, and tested for "eye-facing" one by one, it makes sense to use an insertion sort to order the polygons displayed. A list of polygons to be displayed is built by inserting each new polygon description (number of vertices and position in vertex array) in the already sorted list of previous polygons. A binary search can be used to reduce the search time for finding the insertion point. The procedure in listing 9 implements a binary insertion sort. Note that polygon vertices are stored in an array in contiguous groups. The *z* coordinate of the first element of the group is used to hold the average *z* coordinate of the polygon for subsequent tests.

Sorting is a major part of nearly all hidden-line and hidden-surface algorithms. For a thorough discussion of sorting and other aspects of hidden-surface algorithms, see the paper by Sutherland and others listed in the suggested readings. Also see the third volume of Donald E Knuth's *The Art of Computer Programming* for a thorough treatment of sorting in general.

Text continued on page 82

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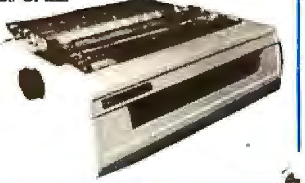

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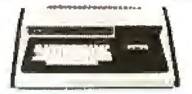

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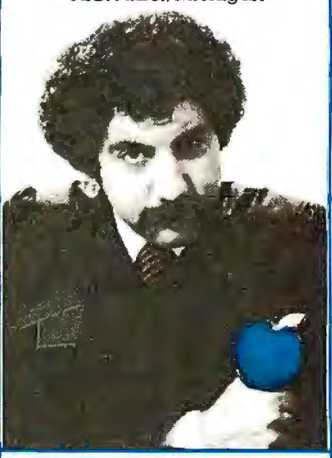

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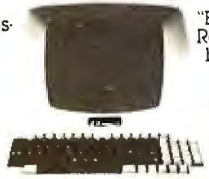

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Listing 1: *Pascal procedure to read data describing a three-dimensional object and display it as a collection of straight lines.*

```
type    Point = record X,Y,Z : real; Draw : boolean; end;

var     Points : array [1..MaxPts] of Point;
        I, NumPts : integer;

procedure ReadObject( FileName : string);
var     I, NumPts : integer;
   Cmd         :  char  ;
begin
reset(ObjFile,FileName);                (* open input file *)
readln(ObjFile,NumPts);                 (* get number of points *)
for I:=1 to NumPts do
        with Points[I] do
                begin
                readln(ObjFile,Cmd,X,Y,Z);
                if Cmd = 'd' then Draw := true else Draw := false
                end;
close(ObjFile);
end;

procedure DrawObject;
var     TmpPt : Point;
begin
Start;                                  (* initialize display *)
for I:=1 to NumPts do
        begin
        Transform(Points[I], TmpPt);    (* transform to display *)
        with TmpPt[I] do
                if Draw then Drawto(X,Y);       (* draw to next pt *)
                        else Moveto(X,Y);       (* move to next pt *)
        end;
Finish;                                 (* close-out dispaly *)
end;
```

Listing 2: *Procedure to display a three-dimensional object with surfaces defined as polygons.*

```
type    Point = record X,Y,Z : real end;
        Polygon = record Start,PolyVtces : integer end;

var     Points : array [1..MaxPts] of Point;
        Polygons : array [1..Maxpols] of Polygon;
        Vertices : array [11..MaxVtces] of integer;
        NumPts,NumVtces,I,J : integer;

procedure ReadObject( FileName : string );
begin
reset(ObjFile,FileName);                (* open input file *)
readln(ObjFile,NumPts,NumPolys);
for I:=1 to NumPts do                   (* read in points *)
        with Points[l] do
                readln(ObjFile,J,X,Y,Z);
NumVtces := 0;                          (* initialize size of vertex array *)
for I:=1 to NumPolys do                 (* read in polygon descriptions *)
        with Polygons[I] do
                begin
                Start := NumVtces;      (* start point in vertex array *)
                read(ObjFile,PolyVtces);        (* number of vertices *)
                for J:=1 to PolyVtces do        (* read vertex pointers *)
                        read(ObjFile,Vertices[NumVtces+J]);
                readln                  (* go to next line of input *)
                NumVtces := NumVtces + PolyVtces;
                end;
end                                     (* ReadObject *)

procedure DisplayObject;
var     TmpPt : Point;
begin
for I:=1 to NumPolys do
        with Polygons[I] do
                begin
                Transform(Points[Vertices[Start+PolyVtces]],TmpPt);
                with TmpPt do Moveto(X,Y);
                for J:=1 to PolyVtces do
                        begin
                        Transform(Points[Vertices[Start+J]],TmpPt);
                        with TmpPt do Drawto(X,Y);
                        end;
                end;
        end;                            (* DisplayObject *)
```

Listing 3: *This procedure will transform the vertices of a polygon using a four-by-four matrix.*

```
var     Mt : array [1..4,1..4] of real;

procedure Transform( Pt : Point; var NewPt : Point );
begin
NewPt.X := Pt.X*Mt[1,1] + Pt.Y*Mt[1,2] + Pt.Z*Mt[1,3] + Mt[1,4];
NewPt.Y := Pt.X*Mt[2,1] + Pt.Y*Mt[2,2] + Pt.Z*Mt[2,3] + Mt[2,4];
NewPt.Z := Pt.Z*Mt[3,1] + Pt.Y*Mt[3,2) + Pt.Z*Mt[3,3] + Mt[3,4];
end;
```

Listing 4: *Distance and viewing angle transforms are determined by this procedure, which builds a transformation matrix based on the relationship between the coordinates of the eyepoint and those of the center of interest.*

```
procedure GetEyeSpace( EyePt,CntrInt : Point );
var     Mtx : Matrix;
        C1,C2 : Point;
        Hypotenuse,CosA,SinA : real;

procedure Ident( var Mtx : Matrix );    (* initialize matrix *)
var    I,J : counter;
begin
for I:=1 to 4 do
        for J:=1 to 4 do
                if I = J then Mtx[I,J] := 1.0 else Mtx[I,J] :=0.0;
end;                                    (* Ident *)
```

Listing 4 continued on page 72

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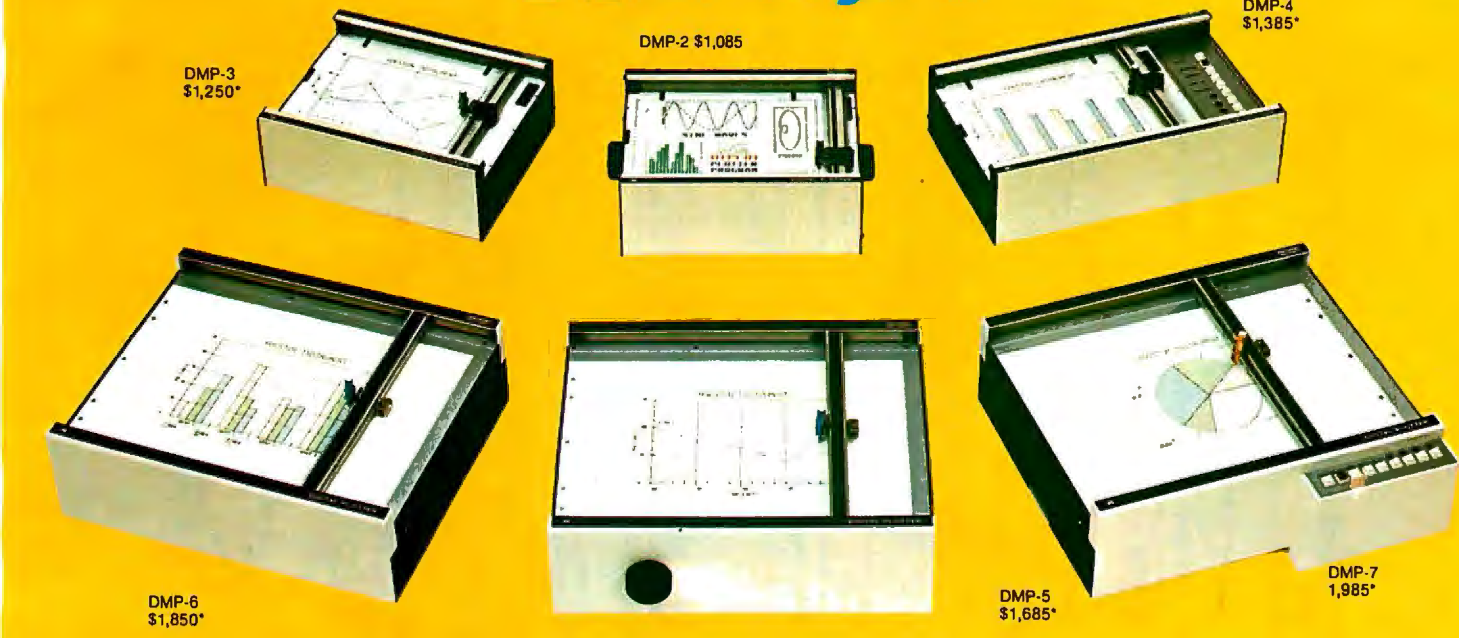

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Listing 4 continued:

```
procedure MatrixMult( Mt1,Mt2 : Matrix; var Result : Matrix );
var     I,J,K : counter;
begin
for I:=1 to 4 do
        for J:=1 to 4 do
                begin
                Result[I,J] := 0.0;
                for K:=1 to 4 do
                        Result[I,J] := Result[I,J] + Mt1[K,J]*Mt2[I,K];
                end;
end;                                    (* MatrixMult *)
procedure Transform( Pt : Point; Mtx : Matrix; var NewPt : Point );
begin
NewPt.X := Pt.X*Mtx[1,1] + Pt.Y*Mtx[1,2] + Pt.Z*Mtx[1,3] + Mtx[1,4];
NewPt.Y := Pt.X*Mtx[2,1] + Pt.Y*Mtx[2,2] + Pt.Z*Mtx[2,3] + Mtx[2,4];
NewPt.Z := Pt.X*Mtx[3,1) + Pt.Y*Mtx[3,2) + Pt.Z*Mtx[3,3] + Mtx[3,4];
end;                                    (* Transform *)

begin                                   (* EyeSpace Procedure body *)
Ident(EyeSpace);
with EyePt do                           (* load eyepoint translation *)
        begin EyeSpace[1,4]:=-X; EyeSpace[2,4]:=-Y; EyeSpace[3,4]:=-Z; end;
Transform( CntrInt,EyeSpace,C1 );       (* translate ctr. of interest *)

Ident(Mtx);                             (* load rotation about Z axis *)
with C1 do Hypotenuse := sqrt( X*X + Y*Y );
if Hypotenuse  0.0 then
        begin
        CosA := C1.Y / Hypotenuse; SinA := C2.X / Hypotenuse;
        Mtx[1,1] := CosA; Mtx[2,1] := SinA;
        Mtx[1,2] := -SinA; Mtx[2,2] := CosA;
        MatrixMult( EyeSpace,Mtx,EyeSpace );
        end;
Transform( CntrInt,EyeSpace,C2 );       (* rotate ctr. of interest *)

Ident(Mtx);                             (* load rotation about Z axis *)
with C2 do Hypotenuse := sqrt( Y*Y + Z*Z );
if Hypotenuse  0.0 then
        begin
        CosA := C2.Y / Hypotenuse; SinA := -C2.Z / Hypotenuse;
        Mtx[2,2] := CosA; Mtx[3,2] := SinA;
        Mtx[2,3] := CosA; Mtx[3,3] := CosA;
        MatrixMult( EyeSpace,Mtx,EyeSpace );



        end;

Ident( Mtx );                           (* load switch between Y and Z axes *)
Mtx[2,2] := 0.0; Mtx[3,3] := 0.0;
Mtx[2,3] := 1.0; Mtx[3,2] := 1.0;
MatrixMult( EyeSpace,Mtx,EyeSpace );
end;                                    (* GetEyeSpace *)
```

Listing 5: *The field of vision for a three-dimensional display is bounded by "clipping planes," the coefficients of which are calculated in this procedure.*

```
type    OnePoly = array [1..MaxSides] of Point;

procedure GetPlanes( var Poly : OnePoly; NumPts : integer );
var     I,LstI : integer;
        TmpPoly : OnePoly;

begin   (* get plane equation coefficients for polygon edges *)
LstI := NumPts;                         (* leading vertex of the edge *)
for I:=1 to NumPts do
        begin
        with Poly[I] do
                begin           (* vector cross-product using edge endpoints *)
                TmpPoly[I].X := Y * Poly[LstI].Z - Z * Poly[LstI].Y;
                TmpPoly[I].Y := Z * Poly[LstI].X - X * Poly[LstI].Z;
                TmpPoly[I].Z := X * Poly[LstI].Y - Y * Poly[LstI].X;
                end;
        LstI := I;
        end;                            (* for Loop *)
for I:=1 to NumPts do                   (* copy back to input polygon *)
        with TmpPoly[I] do
                begin Poly[I].X := X; Poly[I].Y := Y; Poly[I].Z := Z; end;
end;                                    (* GetPlanes *)
```

Listing 6: *Procedure to determine if any vertices of a polygon lie outside previously defined clipping planes; if this is so, the polygon is modified accordingly.*

```
var     Window : OnePoly                (* clipping window *)
        WindowSize : integer;           (* number of edges in clip window *)

function DotProd( Pt1,Pt2 : Point ) : real;
begin                                   (* vector dot-product *)
DotProd := Pt1.X * Pt2.X + Pt1.Y * Pt2.Y + Pt1.Z * Pt2.Z;
end;                                    (* DotProd *)

procedure ClipIn(var Poly : OnePoly; var NumPts : counter);
var     I,J,LstJ,TmpPts : counter;
        D1,D2,A : real;
        TmpPoly : OnePoly;

begin
for I:=1 to WindowSize do               (* for each window edge *)
        if NumPts  0 then
             begin
             D1 := DotProd( Poly[NumPts],Window[I] );
             LstJ := NumPts;
```

Listing 6 continued on page 74

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Listing 6 continued:

```
             TmpPts := 0;
             for J:=1 to NumPts do      (* for each polygon edge *)
                    begin
                    if D1  0.0 then    (* is leading vertex inside? *)
                         begin
                         TmpPts := TmpPts + 1;
                         with TmpPoly[TmpPoints] do
                             begin      (* copy leading vertex *)
                             X:=Poly[LstJ].X; Y:=Poly[LstJ].Y; Z:=Poly[LstJ].Z;
                             end;
                         end;           (* if leading vertex inside *)

                    D2 := DotProd( Poly[J],Window[I] );
                    if D1 * D2  0.0 then  (* does edge straddle window? *)
                         begin
                         A := D1 / (D1 - D2);
                         TmpPts := TmpPts + 1;
                         with TmpPoly[TmpPts] do
                             begin
                             X := A * Poly[J].X + (1.0 - A) * Poly[LstJ].X;
                             Y := A * Poly[J].Y + (1.0 - A) * Poly[LstJ].Y;
                             Z := A * Poly[J].Z + (1.0 - A) * Poly[LstJ].Z;
                             end;
                         end;
                    LstJ := J;
                    D1 := D2;
                    end;                (* NumPts loop *)
             for J:=1 to TmpPts do      (* copy polygon back to input *)
                    with TmpPoly[J] do
                         begin Poly[J].X:=X; Poly[J].Y:=Y; Poly[J].Z:=Z; end;
             NumPts := TmpPts;
             end;                       (* WindowSize loop *)
end;                                    (* ClipIn *)
```

Listing 7: *This procedure achieves a perspective effect by dividing the x and y coordinates of each vertex by the z coordinate.*

```
procedure MakeDisplayable( var Pt : Point );
begin
Pt.X := Scale.X * Pt.X / Pt.Z + Middl.X;
Pt.Y := Scale.Y * Pt.Y / Pt.z + Middl.Y;
end;
```

Listing 8: *This Pascal function determines whether or not a polygon will be hidden by another part of the same surface in a three-dimensional display.*

```
function FacesEye( Poly : OnePoly ) : boolean;
var     TmpPt : Point;
        TmpPoly : OnePoly;
begin
with Poly[2] do                         (* make copy of second Vertex *)
        begin TmpPt.X:=X; TmpPt.Y:=Y; TmpPt.Z:=Z; end;
                                        (* directed vector from second to *)
                                        (* first vertex *)
        TmpPoly[1].X := Poly[1].X - Poly[2].X;
        TmpPoly[1].Y := Poly[1].Y - Poly[2].Y;
        TmpPoly[1].Z := Poly[1].Z - Poly[2].Z;
                                        (* directed vector from second to *)
                                        (* third vertex *)
        TmpPoly[2].X := Poly[3].X - Poly[2].X;
        TmpPoly[2].Y := Poly[3].Y - Poly[2].Y;
        TmpPoly[2].Z := Poly[3].Z - Poly[2].Z;
        GetPlanes( TmpPoly,2 );         (* get plane coeffiicients *)
        if DotProd( TmpPt,TmpPoly[1] ) = 0.0
                then FacesEye := false
                else FacesEye := true;
end;                                    (* FacesEye *)
```

Listing 9: *Based on the average value of their z coordinates, polygons are sorted by their distance from the eyepoint in this binary insertion sort procedure.*

```
var     OutVtces : array [1..MaxVtces] of Point;
        OutPolys : array [1..MaxPolys] of Polygon;
        NumDisplay,NumVtxOut : integer; (* # polygons, # vertices *)

procedure InsertSort( Poly : OnePoly ; NumPts : integer );
var     I,J,K : integer;
        AvDepth : real;
begin                                   (* binary-insertion sort on average *)
                                        (* depth *)
AvDepth := 0.0;
for I:=1 to NumPts do
        with Poly[I] do                 (* store vertices and find average *)
                                        (* depth *)
                begin
                OutVtces[NumVtxOut + I + 1].X := X;
                OutVtces[NumVtxOut + I + 1].Y := Y;
                OutVtces[NumVtxOut + I + 1].Z := Z;
                AvDepth := AvDepth + Z; (* sum depths *)
                end;
AvDepth := AvDepth / NumPts;            (* divide for average *)
OutVtces[NumVtxOut + 1].Z := AvDepth;   (* store for later *)

J := 0;                                 (* initialize for insertion search *)
I := (NumDisplay +1) div 2;
K := NumDisplay;
while (J  I) do                       (* binary search for insertion point *)
        if AvDepth  OutVtces[OutPolys[I].Start].Z
                then begin K := I; I := ( I + J ) div 2; end
                else begin J := I; I := ( I + K + 1 ) div 2; end
for J:=NumDisplay downto I+1 do         (* found it, now insert *)
        begin                           (* move everything above insertion *)
                                        (* point up one*)
        OutPolys[J + 1].Start := OutPolys[J].Start;
        OutPolys[J + 1].NumVtx := OutPolys[J].NumVtx;
        end;
OutPolys[I + 1].Start := NumVtxOut + 1; (* store new entry *)
OutPolys[I + 1].NumVtx := NumPts;
NumVtxOut := NumVtxOut + NumPts + 1;    (* vertex count *)
NumDisplay := NumDisplay + 1;           (* polygons stored *)
end;                                    (* InsertSort *)
```

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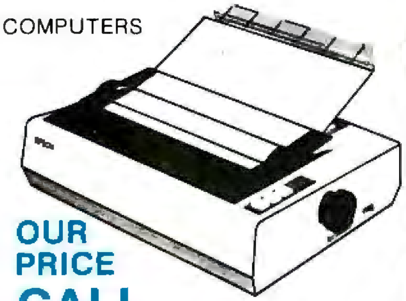

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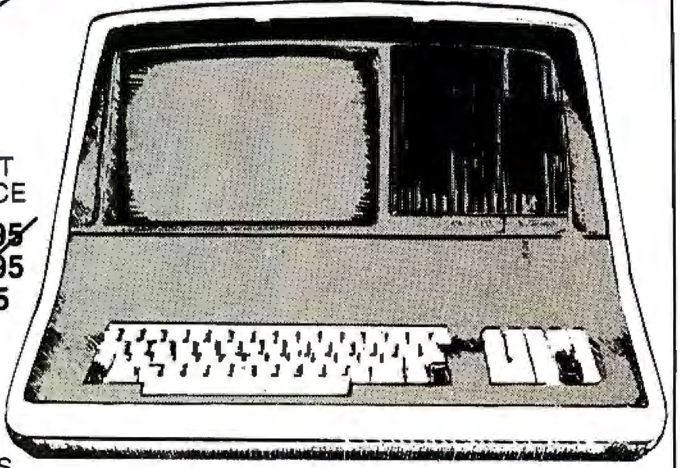

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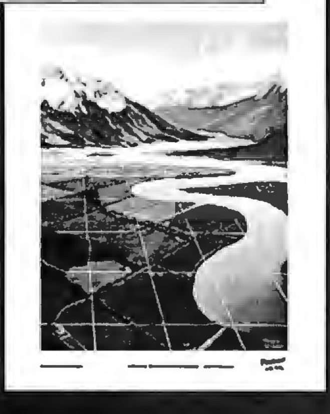

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Listing 10: *Once sorted, polygons are checked to determine if a polygon closer to the eyepoint hides all or part of one that is farther away.*

```
procedure ClipOut( Poly : OnePoly; var NumPts : integer; Place : integer );
var     I,LstI,NumDrawn : integer;
        Pt1,Pt2 : Point;
        Drawn : boolean;

procedure ClipAfter( Index : integer; Pt1,Pt2 : Point );
var     I,J : integer;
        D1,D2,A : real;
        Out : boolean;
        Pt3 : Point;

begin                                   (* recursively check polygons for *)
                                        (* overlap with input edge *)
if Index  Place                       (* is polygon closer than edge in*)
                                        (* sorted list? *)
then with OutPolys[Index] do
        begin
        I := Start + NumVtx;            (* pick up last edge first *)
        Out := false;
        repeat                          (* for each polygon edge *)
            D1 := DotProd( Pt1,OutVtces[I] ); (* distance to first point *)
            D2 := DotProd( Pt2,OutVtces[I] ); (* distance to 2nd point *)
            if ( D1 = 0.0 ) and ( D2 = 0.0 )
            then begin                  (* both points visible *)
                    Out := true;
                    ClipAfter( Index + I,Pt1,Pt2 ); (* try next one *)
                    end
            else if D1 * D2  0.0
                    then begin          (* one point visible *)
                         A := D1 / (D1 - D2); (* get clipped point *)
                         Pt3.X := A * Pt2.X + ( 1.0 - A ) * Pt1.X;
                         Pt3.Y := A * Pt2.Y + ( 1.0 - A ) * Pt1.Y;
                         Pt3.Z := A * Pt2.Z + ( 1.0 - A ) * Pt1.Z;
                         if D1  0.0
                              then begin (* Pt1 visible, try next one *)
                                   ClipAfter( Index+1,Pt1,Pt3 );
                                   with Pt3 do (* go on with hidden part *)
                                   begin Pt1.X:=X; Pt1.Y:=Y; Pt2.Z:=Z; end;
                                   end
                               else begin   (* Pt2 visible, try next one *)
                                   ClipAfter( Index + 1,Pt3,Pt2 );
                                   with Pt3 do (* go on with hidden part *)
                                       begin Pt2.X:=; Pt2.Y:=Y; Pt2.Z:=Z; end;
                                   end;
                               end;     (* one point visible *)
             I := I - 1;                (* count down for next edge *)
       until Out or ( I = Start );      (* all visible  or edges exhausted *)
             end
else begin                              (* reached end of list of closer
                                        (* polygons, display *)
       MakeDisplayable( Pt1 ); Make Dispalyable( Pt2 );
       Moveto( Pt1.X,Pt1.Y ); Drawto( Pt2.X,Pt2.Y );
       Drawn := true;                   (* mark as displayed *)
       end;
end;                                    (* ClipAfter *)



(* ClipOut procedure body *)
begin                                   (* clip each poly edge by all closer *)
                                        (* polys, draw what's left *)
NumDrawn := 0;
Lstl := NumPts do
for I:=1 to NumPts do
        begin                           (* get endpoints for edge *)
        with Poly[LstI] do begin Pt1.X := X; Pt1.Y := Y; Pt1.Z := Z; end;
        with Poly[I] do begin Pt2.X := X; Pt2.Y := Y; Pt2.Z := Z; end;
        Drawn := false;
        ClipAfter( 1,Pt1.Pt2 );       (* clip to closer polys, then display *)
        if Drawn then NumDrawn := NumDrawn + 1;
        LstI := I;
        end;                            (* for loop *O
if NumDrawn = 0 then NumPts := 0;       (* mark as hidden if nothing drawn *)
end;                                    (* ClipOut *)
```

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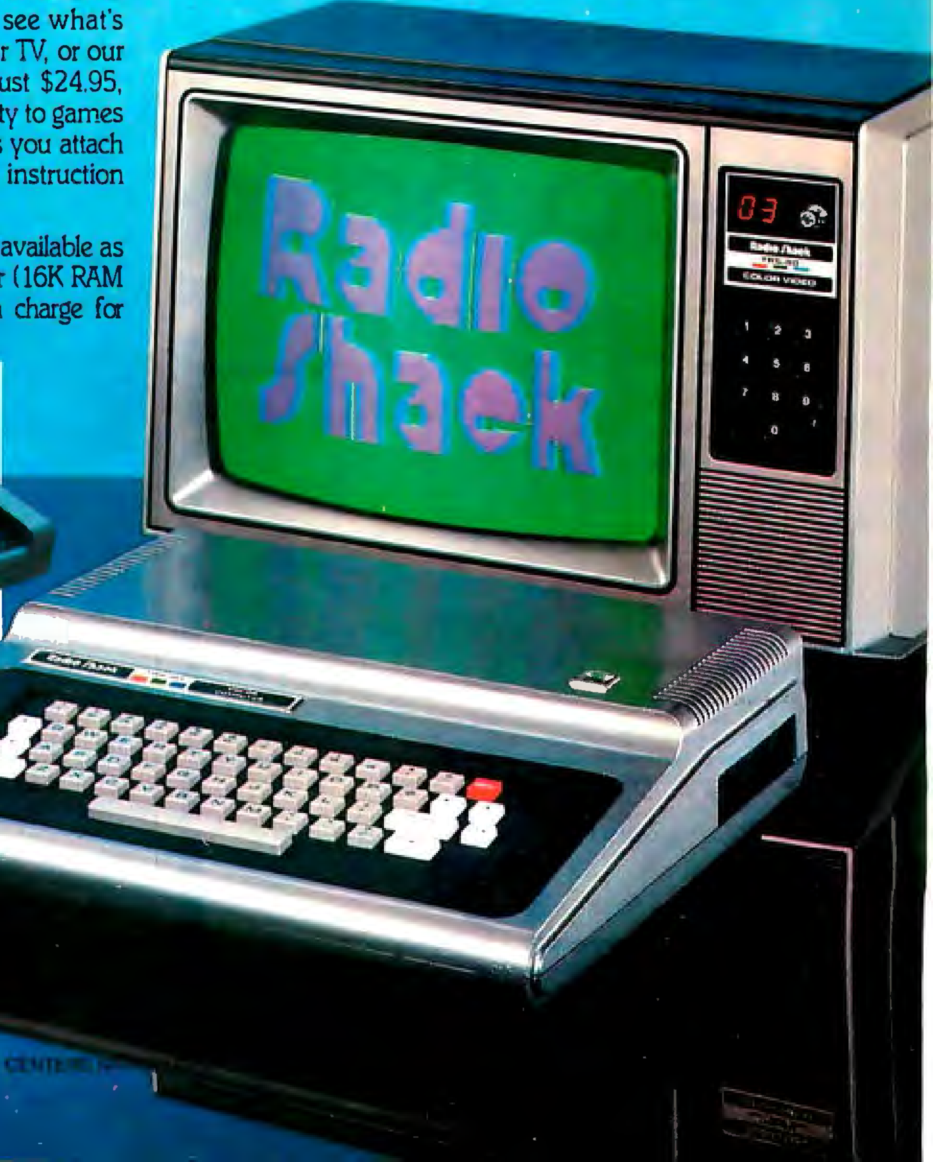

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Text continued from page 66:

Once the polygons are sorted, we can apply a clipping algorithm in a reversed sense. We will remove any parts of polygons lying inside a closer polygon as seen on the display. Starting with the closest polygon and working outward, each polygon will be clipped by all its predecessors. Remember, keeping things simple will require that polygons be convex. (Nonconvex polygons can always be broken into a set of convex ones.)

In order to use a polygon for clipping, its edges must be converted to clipping planes. Therefore, once any part of a polygon is determined to be visible, the entire polygon is subsequently converted to plane coefficients using the same procedure used earlier to convert the window description for clipping.

Since each polygon edge, once clipped, can be displayed without further treatment, it is easiest to clip each edge individually. This process is not as straightforward as it may seem. A polygon may clip an edge into two parts, each of which must then be subsequently clipped by the remaining polygons. Of course, any of the later polygons may further divide one of the edge fragments. This sort of situation is best handled using recursion. Therefore, the procedure given in listing 10 recursively clips a polygon by all closer polygons and flags visible polygons for use in subsequent clipping. Hidden polygons obviously need not be used to clip more distant polygons.

Conclusion

The preceding procedures provide essentially everything needed to display three-dimensional line drawings representing solid objects modeled by polygons. An effort has been made to make the procedures concise. This has been done at the expense of efficiency and sometimes, perhaps, even at the expense of clarity. I have assumed the availability of a display of some kind that can be used to draw lines. Most systems capable of full graphics provide software for generating lines.

In the interests of completeness, Part 2 will present a complete program incorporating the procedures described above. I have been able to use it, somewhat crudely, with a semigraphic terminal (Zenith H-19) and the UCSD Pascal system (see photo 2) and, more satisfyingly, with a 500-line raster display and a Pascal interpreter running under the UNIX operating system (see photos 1, 3, and 4; photos are on pages 54 and 56).

If you have a serious interest in three-dimensional graphics, a full understanding of what has been presented here is heartily recommended. In addition, you should consult the suggested readings listed below for more material. Many people have spent time on the problems discussed in this article and have published useful articles describing other ways to produce computer-generated three-dimensional images.

In addition to line drawing images, much computer graphics is now displayed using the features offered by raster displays. Quite realistic imagery is possible, offering a vast array of possibilities well beyond those described here. There is much work to be done in this area yet, so if you are interested, go to it! ■

Acknowledgments

Mary Lieb handled text-editing and formatting chores. Some of the software development and all the higher-resolution computer-generated images were done on equipment supplied in part by the National Science Foundation (equipment grant # MCS 80-06322) and in part by the Ohio State University.

Suggested Reading

Newman, W and R Sproull, *Principles of Interactive Computer Graphics*, 2nd edition, McGraw-Hill, 1978. The classic text on computer graphics—some consider it difficult, but you must read it if you are serious about the subject.

Rogers, D F and J A Adams, *An Introduction to Computer Graphics*, McGraw-Hill, 1977. A cookbook approach to the subject with many useful algorithms listed in BASIC.

Giloi, W K, *Interactive Computer Graphics*, Prentice-Hall, 1978. An introductory textbook with a somewhat different approach than that of the two books above.

Knuth, D E, *The Art of Computer Programming: Volume 3, Sorting and Searching*, Addison Wesley, 1973. A treasure trove of algorithms and analyses of algorithms—a very important book.

Sutherland, I E, et al, "A Characterization of Ten Hidden-Surface Algorithms," *ACM Computing Surveys*, March 1974. A very informative explanation of the extant hidden-surface algorithms of the time. *Computing Surveys* is available in most technical libraries.

Crow, F C, "A System for the Design of Three-Dimensional Objects," *Proceedings of the ACM National Conference, 1977.* A system for designing three-dimensional shapes involving simple curved surfaces, available from the Association for Computing Machinery, 1133 Avenue of the Americas, New York NY 10036.

Parent, R, "Three-Dimensional Object Synthesis," *Proceedings of SIGGRAPH '76*, 1976. A more comprehensive system for building three-dimensional objects. See also the proceedings of the annual SIGGRAPH conferences for the last five years or so, which contain papers describing most of the interesting work done in recent years—the best way to keep up with what's going on. Available from the Association for Computing Machinery, listed above.

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Product Review

The Micro Matrix Photopoint Light Pen

Stephen B Gray, 219 W 81 St, Apt 7C, New York NY 10024

Because it's called a *light pen*, and because of the way it *seems* to be used, many people have the incorrect impression that a light pen does something directly to the image on the video screen. In actuality, it's the other way around. A light pen contains a photodiode that detects the movement of a point of light on the video screen, determines the coordinates of that point, and branches to a specified action for that point.

For example, if you're playing tic-tac-toe, you only have to point the light pen at the square in which you want to place your X. With a scan limited to nine areas on the video screen, the photodiode detects which area you're pointing to and puts an X in that square.

Applications

As hinted above, one of the most popular applications for the light pen is games. Instead of pressing a key, you need only point the pen. This eliminates having to memorize which key does what.

Another popular application is the fast selection of items in a screen menu. Some advanced graphics programs use light pens and menus. A screen may present a selection of shapes along one side, for example. You touch one, then touch the point on the screen where you want the computer to place the shape. Using small menus along the bottom of the screen, you control the size and rotation of the shapes to create complex subjects.

Micro Matrix Photopoint

One of the several light pens on the market for the Radio Shack TRS-80 is the $19.95 Photopoint from Micro Matrix, POB 938, Pacifica CA 94044. (The Photopoint is also available from Quality Software, 6660 Reseda Blvd, Suite 105, Reseda CA 91335.) The documentation notes that "The light pen allows the user to use their CRT as a programmable keyboard where your own BASIC program (or a prepackaged one) can be written to ask questions and the operator just points at the appropriate answer. No more fumbling with keyboards! The Photopoint can be used with any DOS and with any size memory (must be a Level II TRS-80)." Fortunately, the rest of the documentation is not as confusing as that first sentence.

For your $19.95 you receive a light pen that looks like a slender felt-tip pen, with a two-part cable which connects to a 9 V battery and to your recorder. You also receive a cassette with backgammon, tic-tac-toe, Word Sampler, and a light-pen subroutine; documentation containing another game and a listing of the subroutine is also included.

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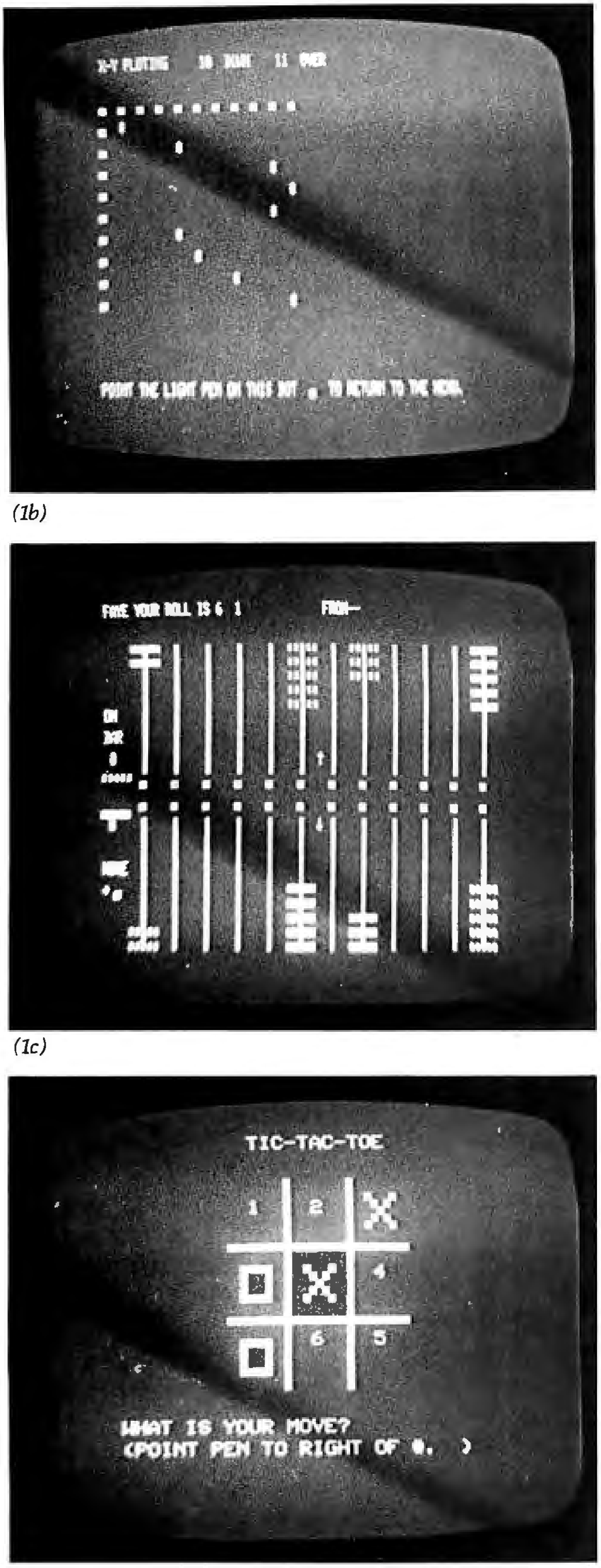

(1b)

(1c)

```
WHAT IS YOUR MOVE?
(POINT PEN TO RIGHT OF #.  )
```

Photo 1: *Three of six demonstration programs included with the Micro Matrix Photopoint light pen: x, y plotting (1a), backgammon (1b), and tic-tac-toe (1c). The light pen requires a TRS-80 Level II with 16 K bytes of programmable memory.*

Using the Photopoint

The pen's miniature plug is connected either to your cassette recorder's auxiliary or microphone jack. When plugged into the auxiliary jack, the pen responds to graphics but not to normal text. When plugged into the microphone jack, the pen is sensitive to both text and graphics (the suggested mode for most uses).

One of the main reasons for Photopoint's comparatively low price is that it uses the amplifier in your tape recorder. To turn on the amplifier, remove any cassette from the recorder; then, while holding in the record interlock pin (at the rear of the cassette compartment), press the RECORD and PLAY buttons simultaneously. The only thing left to do is connect a 9 V battery to the battery clip, and you're set to go.

After loading the light-pen subroutine, you will see a menu from which you can choose any of six demonstration programs.

The light pen doesn't read instantly; you have to wait for the scan to pass the square you're aiming at, and then a bit longer for the software to react. One good way to get a feel for what is going on is to place a broadcast-band AM radio near the TRS-80 keyboard. You'll hear something like a "dit-dit-dit-un-pah" as the computer recognizes a flashing square. Since it can't "read" a static square, the program flashes the squares in sequence to give the photodiode a target to pick out.

The first two demonstration programs are similar, with a series of eight squares arranged horizontally (in program 1) and vertically (in program 2). When any square is touched by the light pen, the number of the square (1 thru 8) is printed on the screen. The third demonstration program uses the same principle—this time with a series of fifty blocks; the fourth scans eight randomly placed squares; and the fifth (see photo 1a) plots lines and curves by lighting an asterisk when a pair of squares along the x and y axes are touched.

The backgammon program (see photo 1b) allows you to use the light pen to roll the dice, redraw the board, or play a new game. Or, you can move by aiming the light pen at FROM and TO selection squares.

Tic-tac-toe (see photo 1c) is played with a large field and double-size characters. You play against the computer, and indicate a square by pointing the pen to the right of the number in that square.

The computer puts an X in the square you select, then an O in the square it selects. The process continues until the computer detects that the game has been won or drawn.

The fourth program on the cassette is Word Sampler. You or the computer enters a sentence. Then you point the light pen at any word, and the computer displays that word above the sentence, starting at the left margin and continuing with further words you select. Thus you can construct a new sentence by rearranging the words of the old one.

The fifth program is called Cube Chase. After you key in eight lines, you point the light pen at a white square on the screen, and the square quickly moves elsewhere.

If you plug the light pen into the auxiliary jack, remove the black plastic plug from the microphone jack, and then whistle or snap your fingers, the cube will change its position on the screen. (This works on my CTR-41, although perhaps not on some other cassette recorders.)

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BY-3-1

The explanation is simple: The TRS-80 receives its information from the Photopoint light pen through tape port 255. The program makes the recorder think the light pen is a microphone. A sudden change of impedance occurs when a scanning blip of light is detected by the pen's photodiode.

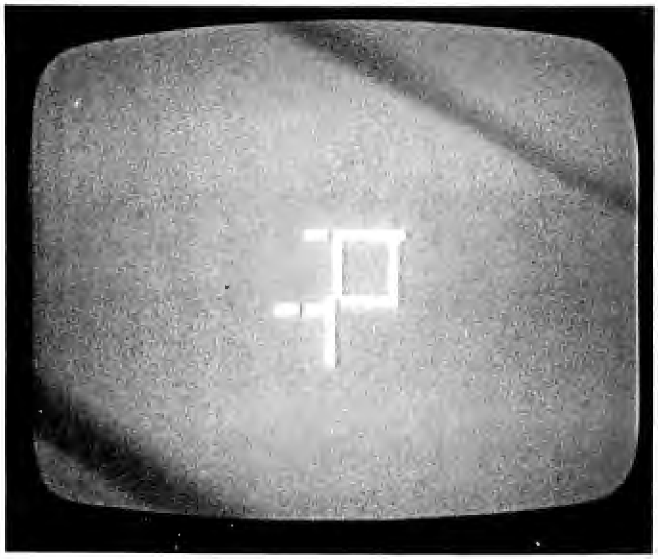

Photo 2: *Quick Draw enables use of the light pen to draw or erase figures in a 48 by 64 graphic field. More complex drawing programs may be written but the manual gives no information on how to do this.*

Micro Matrix is also reportedly planning an interface for Sargon II so you can play chess using a light pen. Also planned are a number of chase games.

PENBASIC

For $14.95, Micro Matrix is offering Steve Bjork's PENBASIC, which adds ten new commands to Level II BASIC. Among the most interesting are:

- P=&NOTE(exp) produces a tone on the cassette output with (exp) ranging from 0 (highest pitch) to 255 (lowest pitch).
- P=&PEN PEEK tests to determine if the light pen is pointed at a lighted part of the display.
- P=&PEN performs a full screen search for the pen position. If the pen is not found, a −1 is returned; if it is found, PRINT @ (position) is returned.
- P=&PEN USING searches for the pen only at the points specified in the expression.
- P=&PEN FOR searches for the pen at the points defined in a one-dimensional integer array.

Using PENBASIC, any of the 1024 locations on the TRS-80 video display can be detected. The four-page PENBASIC manual explains eight of the ten commands and includes brief examples of using them within programs. The manual appears to be written for those with a good knowledge of BASIC. In fact, two of the functions aren't explained at all.

Along with PENBASIC, the demonstration tape contains two programs: Quick Draw and Line of Five.

Quick Draw (see photo 2) enables you to use the light pen to draw and erase figures in a 64 by 48 graphic field. You use related key commands to draw, erase, position the cursor, load and save to and from tape, and end the program. Turning on a square can take several seconds (sometimes longer). Quick Draw is described as a "simple drawing program," which hints that more complex (and, perhaps, faster) programs can be written. The manual gives no clues how to do this.

Line of Five is described as "the first in a series of application programs for PENBASIC." It's a simple game of capturing five squares in a row before the computer does. The computer plays a fairly aggressive game but can be beaten.

The Micro Matrix Photopoint light pen and PENBASIC make a useful package for examining light-pen applications. What makes it even more attractive is that the price is the lowest on the market.■

Why Can't a Light Pen Use the Raster Scan?

The Exidy Sorcerer is probably the only home computer that can use the raster scan, according to Mike Banks, president of Micro Matrix. The Sorcerer uses the microprocessor to control the video and sets up a counter to keep track of the vertical scan. The TRS-80 has no such counter, and thus cannot ask, as the Sorcerer can, "What was the count at the moment I saw the light?" In PENBASIC, when the PEN PEEK command detects a lighted part of the display, it is merely looking to see if the tape-recorder output, at port 255, is high or low.

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The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

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What's Inside Radio Shack's Color Computer?

Tim Ahrens, Jack Browne, Hunter Scales
3501 Ed Bluestein Blvd
Austin TX 78721

The only similarity between Tandy Corporation's new Color Computer and its older brother — the original TRS-80 — is the name. Even the microprocessor has been changed. In an apparent breakaway from the Z80, the Color Computer uses the Motorola MC6809E microprocessor as the workhorse of the new silver box. In fact, when we opened the enclosure, we didn't see any semiconductors that weren't made by Motorola.

The Color Computer is totally self-contained — no bulky separate power transformers — and the only cord, the one to the wall socket, has a standard three-prong connector. It can work with any color or black-and-white television set and has provisions for joysticks, a 1500 bps (bits per second) cassette interface, and an expansion connector for preprogrammed game cartridges.

Part	Number of Pins	Quantity	Device Number	Description
MC6809E	40	1	1	Microprocessor
MC6821	40	2	2, 3	Parallel Interface Adapter
MC6883	40	1	4	Synchronous Address Multiplexer
MC6847	40	1	5	Video Display Generator
MCM68A364	24	2	6, 7	8 K-byte Read-Only Memory
MCM4027	16	8	8 thru 15	4 K-bit Programmable Memory
MC74LS138	16	1	16	3-bit Decoder
MC74LS02	14	1	17	Quad 2-Input NOR Gate
MC74LS244	20	1	18	Octal Buffer/Line Driver
MC74LS273	20	1	19	8-bit Latch
MC14050B	14	1	20	Hex Noninverting CMOS Buffer
MC14529B	16	1	21	Dual 4-Channel Analog
MC1372	14	1	22	Color-Subcarrier Modulator
MLM339	14	1	23	Quad Voltage Comparator
MC723C	14	1	24	Voltage Regulator
MC78M12	3	1	25	Voltage Regulator
MC79M12	3	1	26	Voltage Regulator
MC79M05	3	1	27	Voltage Regulator
UM1285-8	NA	1	28	ASTEC Video Modulator

Table 1: *List of integrated circuits used in the TRS-80 Color Computer. Large-scale integration reduces the number of devices necessary to build in sophisticated capabilities, and improves reliability. All circuits used are manufactured by Motorola.*

Our aim in this article is to expose the insides of the computer and show what makes it run. Using this information, you should be able to expand the Color Computer in a number of ways, with a minimum of expertise. We will also describe the graphics interface so that do-it-yourself graphics routines should be a piece of cake.

System Hardware

Taking the cover off is simply a matter of removing seven screws and lifting the lid. Be warned, however, that Tandy takes a dim view of owners fooling around with their hardware. Opening the case voids the warranty on the machine (one of the screws lies under a paper label that gives this warning).

The first surprise is that the entire computer is built on a single printed-circuit board — including the power supply. Most of the digital circuitry lies inside an RFI (radio-frequency interference) shield — this was probably necessary to get FCC (Federal Communications Commission) Type Approval, but it also helps to give a clean display. To get a look at the parts, simply pry off the top of the shield.

There are only twenty-four DIPs (dual in-line packages) in the system and they are all made by Motorola. (The parts list is shown in table 1.) The machine comes stuffed with 4 K-byte memory circuits; but there is a simple way to change these to 16 K-byte devices and a tricky way to get 32 K bytes of on-board memory — more on this later.

While we do not yet have a schematic diagram, the block diagram in figure 1 should be sufficiently detailed to allow a thorough understanding of the system. There are four basic sections:

- the microprocessor
- the video-display circuitry
- the memory
- the other I/O (input/output) devices (keyboard, cassette, serial port, and joysticks)

The microprocessor is Motorola's advanced 8-bit machine, the MC6809E. It was designed to support today's high-level languages, including the Extended

Text continued on page 96

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- Output may be logged to disk
- Expanded memory test
- Expanded terminal test
- Expanded disk test

Diagnostics II provides the next level in system maintenance.
Requires: 32K CP/M
Price: $100.00 Manual only: $15.00

SYSTEM MAINTENANCE

SUPER-M-LIST: A complete, easy to use mailing list program package. Allows for two names, two addresses, city, state, zip and a three digit code field for added flexibility. Super-M-List can sort on any field and produce mailing labels direct to printer or disk file for later printing or use by other programs. Super-M-List is the perfect companion to TFS. Handles 1981 Zip Codes!
Requires: 48K CP/M
Supplied with complete user manual: $75.00 manual alone: $10.00

TFS-Text Formatting System: An extremely powerful formatter. More than 50 commands. Supports all major features including:
- left & right margin justification
- user defined macros
- dynamic insertion from disk file
- underlining and backspace

TFS lets you make multiple copies of any text. For example: Personalized form letters complete with name, address & other insertions from a disk file. Text is not limited to the size of RAM making TFS perfect for reports or any big job. Text is entered using CP/M standard editor or most any CP/M compatible editor.
Requires: 24K CP/M
Supplied with extensive user manual: $85.00 manual alone: $20.00
Source to TFS in 8080 assembler (can be assembled using standard CP/M assembler) plus user manual: $250.00.

TEXT PROCESSING

UTILITIES I: A collection of programs that you will find useful and maybe even necessary in your daily work (we did!).
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UTILITIES II: Many new programs not available elsewhere. Includes these "file" utilities:

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RPL:	Substitute strings in files

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Requires: 56K CP/M	$500.00
1 year maintenance	$300.00
manual alone	$ 50.00

Z8000 too!

SSS FORTRAN: The SSS FORTRAN compiler is fast, efficient, and complete (full 1966 ANSI standard with extensions). The RATFOR compiler compiles into FORTRAN allowing the user to write structured code while retaining the benefits of FORTRAN. The FORTRAN supports many advanced features not found in less complete implementations, including: complex arithmetic, character variables, and functions. Complete sequencial and random disk I/O are supported. SSS FORTRAN will compile up to 600 lines per minute! Recursive subroutines with static variables are supported. ROMable ".COM" files may be generated. SSS RATFOR allows the use of contemporary loop control and structured programming techniques. SSS RATFOR is similar to FORTRAN '77 in that it supports such things as:
- REPEAT...UNTIL
- WHILE
- IF...THEN...ELSE

SSS RATFOR is supplied with *source code* in FORTRAN and RATFOR.
System Requirements & Prices:
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- IF...THEN...ELSE
- WHILE
- PEAK & POKE
- READ & WRITE
- REPEAT...UNTIL
- more

'Tiny' Pascal is fast. Programs execute up to ten times faster than similar BASIC programs. SOURCE TOO! We still distribute source, in 'Tiny' Pascal, on each discette sold. You can even recompile the compiler, add features or just gain insight into compiler construction.
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PROGRAMMING LANGUAGES

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- error checking and auto retry
- terminal mode for timesharing between systems
- conversational mode
- send files
- receive files

Requires: 32K CP/M
Supplied with user manual and 8080 source code: $150.00
Manual alone: $15.00

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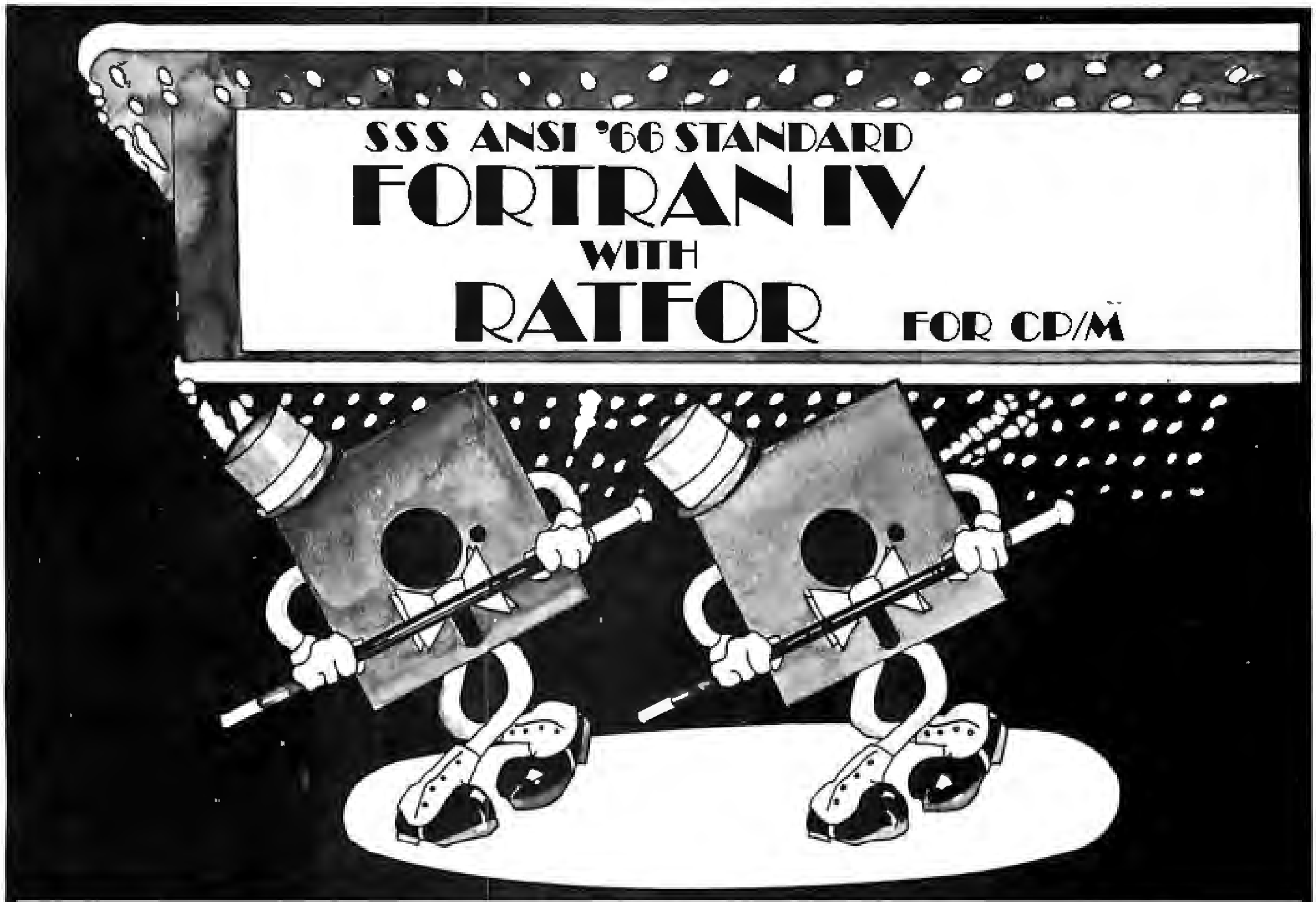

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SSS FORTRAN makes full FORTRAN IV available to microcomputers. SSS FORTRAN meets and exceeds the ANSI 1966 FORTRAN standard. The compiler supports many advanced features not found in less complete implementations, including: complex arithmetic, character variables, and functions. SSS FORTRAN will compile up to 600 lines per minute! Recursive subroutines with static variables are supported. ROMable ".COM" files may be generated.

FEATURES

Code generation:	ROMable ".COM" files or intermediate code files (saves disk space). External routines may be called.
Data types:	Byte, integer, real, double precision, complex, logical, character and varying length strings.
Operations:	All standard operations plus string comparisons, assignments, and .XOR.
Constants:	Hexadecimal, decimal, and character literals with features to imbed control characters.
Statements:	ANSI 1966 standard with multiple statement lines, statements may end with a ' ;'.
Controls:	Map, List, and Symbol table output options.
I/O:	Read, Write, Append, Rewind, Close, Delete, Rename, Search, sequencial and Random I/O on disk files. Supports all CP/M devices. The User can add device handlers to use custom I/O devices.
Errors:	Over 200 distinct compiler error messages, precision and illegal instruction warnings during execution.
Interrupts:	FORTRAN programs may be interrupted at any time; the stack pointer is always preserved.

FEATURING

SSS RATFOR

RATFOR is a preprocessor that compiles to SSS FORTRAN. SSS RATFOR allows the use of contemporary loop control and structured programing techinques. SSS RATFOR is similar to FORTRAN '77 in that it supports such things as:

REPEAT . . . UNTIL WHILE IF . . . THEN . . . ELSE
Begin End Brackets Macro Defines

SSS RATFOR is supplied with *source code*. The source code is distributed in both RATFOR and SSS FORTRAN. Not only does this prevent obsolescence, but allows the user to add enhancements as desired.

System Requirements & Prices

SSS FORTRAN requires a 32k CP/M system. Z80 only.
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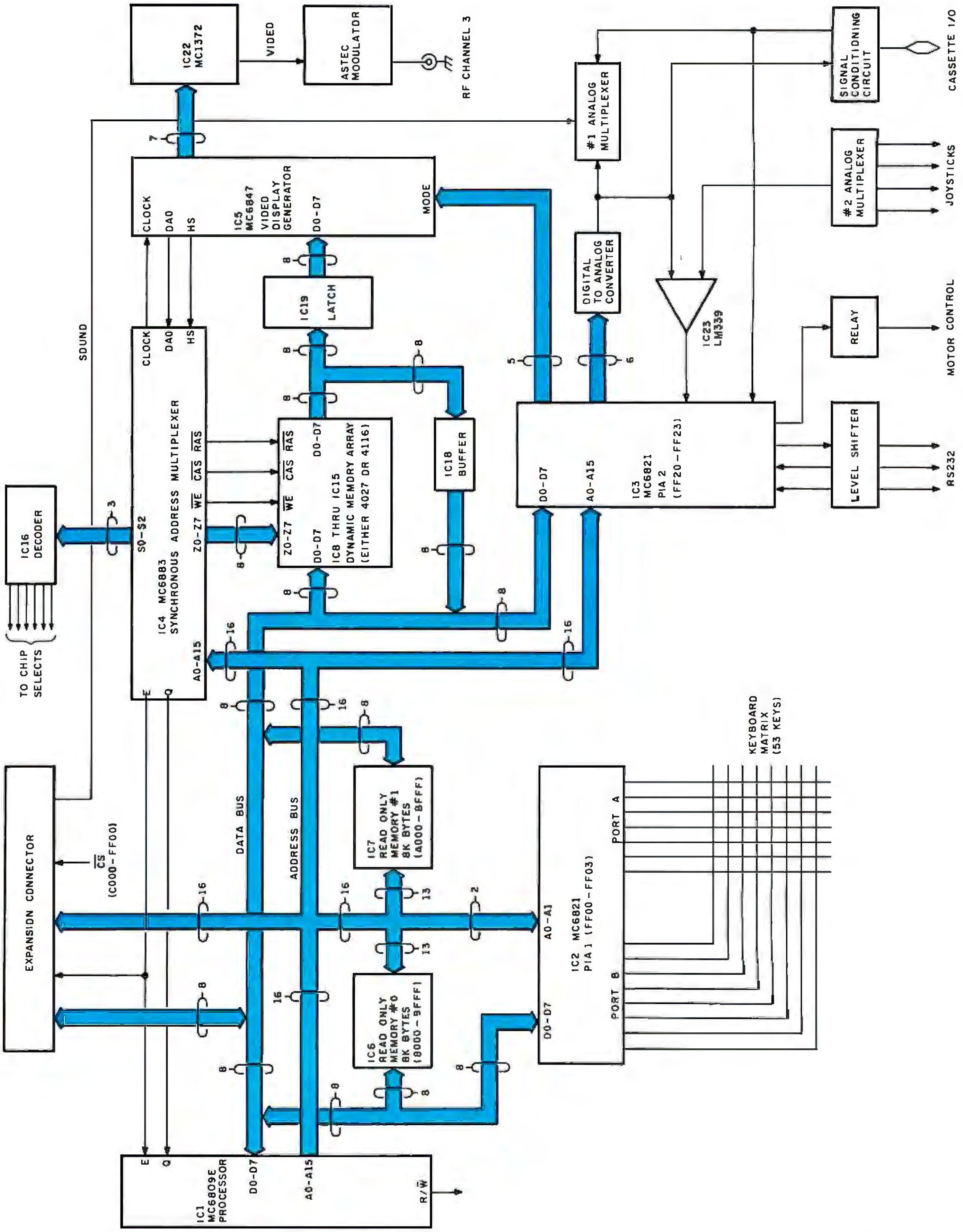

Figure 1: *Block diagram of the Radio Shack Color Computer. Although a detailed schematic diagram is not available, the connection of the main components can be readily determined. Note that the use of large-scale integrated circuits (the microprocessor, SAM dynamic-memory handler, video-display generator, and parallel port interfaces) means that a minimum number of components is necessary to build this flexible computer.*

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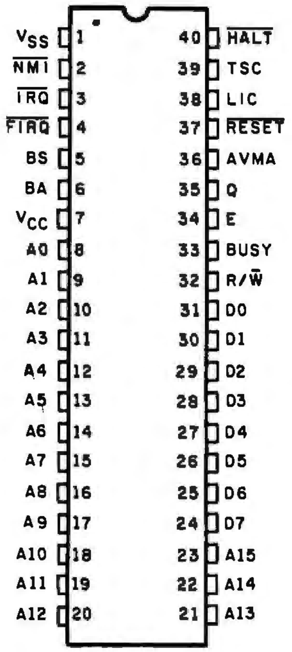

Figure 2: *Pin description of Motorola's MC6809E microprocessor. The device has several 16-bit instructions that, coupled with ease of programming and speed, make for a very powerful 8-bit processor.*

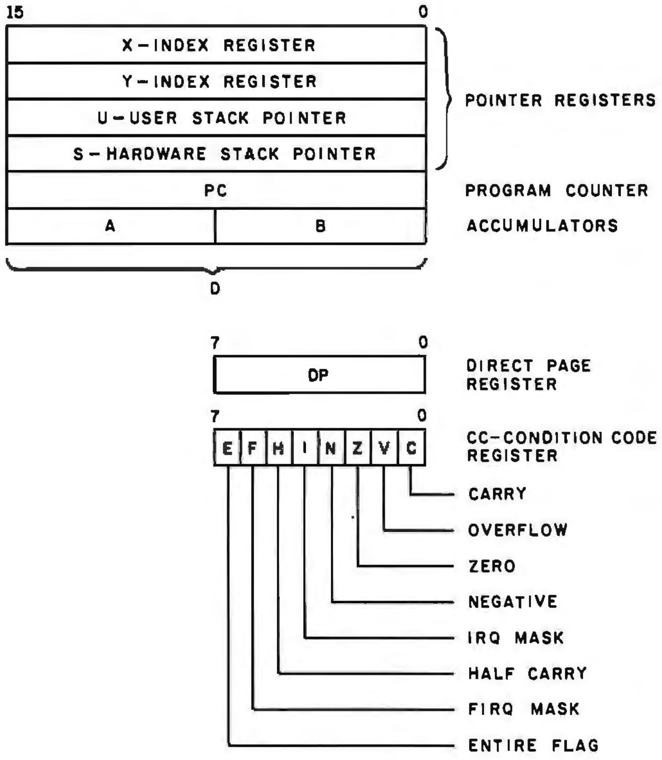

Figure 3: *Registers available in the 6809. Similar in architecture to the 6800, the 6809 has three extra registers to facilitate memory acesses: a direct page register, a user stack register, and a second index register. The instruction set is also more robust, with the addition of 16-bit add, subtract, and multiply operations.*

Text continued from page 90:

BASICs now available. It has two 16-bit index registers and two 16-bit stack pointers, as well as two 8-bit accumulators that can be used as a double-precision 16-bit accumulator. It supports both position-independent code (code that can be executed anywhere in memory without reassembly) and reentrant (interruptible) code.

The video display is generated by the Motorola MC6847 VDG (video display generator). This is a 40-pin LSI (large-scale integration) part that reads from ½ K bytes to 6 K bytes of memory, depending on mode, to produce an analog video signal. This signal is fed to the MC1372 color-subcarrier modulator to get composite video, which is then modulated by the ASTEC video modulator to channel 3 or 4.

The Color BASIC interpreter is stored in an 8 K by 8 bit ROM (read-only memory). Its companion, Extended BASIC, comes in another ROM of the same type. The basic machine comes with only the first ROM; the extended ROM costs $99 plus installation.

As mentioned, the computer comes with eight MCM4027 4 K-bit dynamic memory circuits. Tandy will upgrade your system to 16 K bytes by replacing these with MCM4116s (16 K-bit devices) for $119. Or you can buy the system with 16 K bytes and the Extended BASIC ROM for $599.

These memory circuits are controlled and refreshed by a special part, the MC6883 SAM (synchronous address multiplexer). It provides all the signals for the memory and the VDG and also provides the timing signals for the microprocessor.

The other I/O functions are all handled by parallel ports in the form of MC6821 PIAs (peripheral interface adapters). The keyboard is connected to these and is scanned and decoded in software. The serial port and cassette port are both derived from a single parallel line and are selected by software. The optional joysticks are encoded with an A/D (analog-to-digital) converter composed of a resistive-summing network hooked to a 6-bit parallel port and an LM339 comparator.

The MC6809E Microprocessor

The third-generation MC6809E 8-bit microprocessor features several 16-bit operations. This puts it functionally between the 8- and the 16-bit processors. A description of the MC6809E signals appears in figure 2.

The programming model of the MC6809E is shown in figure 3. Three registers were added to the register set of the original MC6800:

- a direct page register
- a user stack pointer
- a second index register

There are two 8-bit accumulator registers, the A register and the B register, that are used for data manipulation and serve as holding registers for arithmetic calculations. The MC6809E has many 16-bit arithmetic operations, including additions, subtractions, loads, stores, and an 8 bit by 8 bit multiplication. The 16-bit arithmetic operations use both accumulators—with the A register treated

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as the most significant byte. When the A and B registers are concatenated, they are referred to as the D register.

The DP (direct page) register is one of the new registers. Its contents form the high-order byte of the address bus during instructions utilizing the direct addressing mode. This register may be changed to allow direct addressing anywhere in the 64 K-byte memory map, as compared to the MC6800, which allowed direct addressing only in the first 256 bytes of the memory map. Direct addressing uses the immediate byte of the instruction as a 1-byte pointer into a single 256-byte "page" of memory. This shortens instruction execution time because the high-order byte is furnished by the direct page register. MC6800 source code compatibility is ensured because actuation of the RESET line clears the direct page register.

The MC6809E has four 16-bit pointer registers available to the user. The U and S registers support stack-oriented instructions such as PSH and PUL. The S register is used as the hardware stack pointer to support interrupts and subroutine calls. The U register gives the designer the capability of maintaining an independent stack.

The other two registers, X and Y, are intended primarily for use as index registers, although special indexing modes allow them to be used to maintain additional stack areas. All four pointer registers can be used as index registers, allowing indexed addressing, indirect addressing, or indexed indirect addressing. These pointer register capabilities permit the MC6809E to function efficiently as a stack processor, allowing the microprocessor to support graphics, high-level languages, and modular programming techniques.

The microprocessor's program counter, while primarily used by the processor to address the next instruction, may be referenced as an index register, thus allowing addressing relative to the program counter.

The condition code register defines the state of the microprocessor such that conditional branch instructions may be used. The condition code register also allows masking of some of the interrupts.

The register set is manipulated with the 59 instructions shown in table 2. Over 1460 different op codes are available to the programmer if all modes of the instructions are considered. However, only the 59 mnemonics must be remembered when using an assembler.

Efficient PIC (position-independent code) can be written using the capabilities of the MC6809E. The program counter can be used as a pointer to provide offsets within the program. For example, when a portion of PIC is executed, the stack addresses, peripheral addresses, and other addresses may be specified as offsets from the current program counter address.

Other key factors in effective position-independent code writing are the use of long and short relative-branch

Text continued on page 102

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8-BIT OPERATIONS

Mnemonic	Description
ABX	Add B register to X register unsigned.
ADCA, ADCB	Add memory to accumulator with carry.
ADDA, ADDB	Add memory to accumulator.
ANDA, ANDB	AND memory with accumulator.
ANDCC	AND immediate with condition code register.
ASLA, ASLB, ASL	Arithmetic shift left accumulator or memory.
ASRA, ASRB, ARS	Arithmetic shift right accumulator or memory.
BITA, BITB	Bit test memory with accumulator.
CLRA, CLRB, CLR	Clear accumulator or memory.
CMPA, CMPB	Compare memory with accumulator.
COMA, COMB, COM	Complement accumulator or memory.
DAA	Decimal Adjust A accumulator.
DECA, DECB, DEC	Decrement accumulator or memory.
EORA, EORB	Exclusive OR memory with accumulator.
EXG R1, R2	Exchange R1 and R2.
INCA, INCB, INC	Increment accumulator or memory.
LDA, LDB	Load accumulator from memory.
LSLA, LSLB, LSL	Logical shift left accumulator or memory.
LSRA, LSRB, LSR	Logical shift right accumulator or memory.
MUL	Unsigned multiply (8 bit by 8 bit = 16 bit).
NEGA, NEGB, NEG	Negate accumulator or memory.
ORA, ORB	OR memory with accumulator.
ORCC	OR immediate with condition code register.
PSHS (register list)	Push register(s) on hardware stack.
PSHU (register list)	Push register(s) on user stack.
PULS (register list)	Pull register(s) from hardware stack.
PULU (register list)	Pull register(s) from user stack.
ROLA, ROLB, ROL	Rotate accumulator or memory left.
RORA, RORB, ROR	Rotate accumulator or memory right.
SBCA, SBCB	Subtract memory from accumulator with borrow.
STA, STB	Store accumulator to memory.
SUBA, SUBB	Subtract memory from accumulator.
TSTA, TSTB, TST	Test accumulator or memory.
TFR R1, R2	Transfer register R1 to register R2.

16-BIT OPERATIONS

Mnemonic	Description
ADDD	Add to D accumulator.
SUBD	Subtract from D accumulator.
LDD	Load D accumulator.
STD	Store D accumulator.
CMPD	Compare D accumulator.
LDX, LDY, LDX, LDU	Load pointer register.
STX, STY, STS, STU	Store printer register.
CMPX, CMPY, CMPU, CMPS	Compare pointer register.
LEAX, LEAY, LEAS, LEAU	Load effective address into pointer register.
SEX	Sign extend
TFR register, register	Transfer register to register.
EXG register, register	Exchange register to register.
PSHS (register list)	Push register(s) onto hardware stack.
PSHU (register list)	Push register(s) onto user stack.
PULS (register list)	Pull register(s) from hardware stack.
PULU (register list)	Pull register(s) from user stack.

Table 2: *The 6809 instruction set.*

INDEXED ADDRESSING MODES

Mnemonic	Description
0, R	Indexed with zero offset.
[0, R]	Indexed with zero offset indirect.
,R+	Autoincrement by 1.
,R++	Autoincrement by 2.
[,R++]	Autoincrement by 2 indirect.
,−R	Autodecrement by 1.
,−−R	Autodecrement by 2.
[,−−R]	Autodecrement by 2 indirect.
n, P	Indexed with signed n as offset (n = 5, 8, or 16 bits).
[n, P]	Indexed with signed n as offset indirect.
A, R	Indexed with accumulator A as offset.
[A, R]	Indexed with accumulator A as offset indirect.
B, R	Indexed with accumulator B as offset.
[B, R]	Indexed with accumulator B as offset indirect.
D, R	Indexed with accumulator D as offset.
[D, R]	Indexed with accumulator D as offset indirect.

NOTE: *R = X, Y, U, or S; P = PC, X, Y, U, or S. Brackets indicate indirection. D means use AB accumulator pair.*

6809 RELATIVE SHORT AND LONG BRANCHES

Mnemonic	Description
BCC, LBCC	Branch if carry clear.
BCS, LBCS	Branch if carry set.
BEQ, LBEQ	Branch if equal.
BGE, LBGE	Branch if greater than or equal (signed).
BGT, LBGT	Branch if greater (signed).
BHI, LBHI	Branch if higher (unsigned).
BHS, LBHS	Branch if higher or same (unsigned).
BLE, LBLE	Branch if less than or equal (signed).
BLO, LBLO	Branch if lower (unsigned).
BLS, LBLS	Branch if lower or same (unsigned).
BLT, LBLT	Branch if less than (signed).
BMI, LBMI	Branch if minus.
BNE, LBNE	Branch if not equal.
BPL, LBPL	Branch if plus.
BRA, LBRA	Branch always.
BRN, LBRN	Branch never.
BSR, LBSR	Branch to subroutine.
BVC, LBVC	Branch if overflow clear.
BVS, LBVS	Branch if overflow set.

6809 MISCELLANEOUS INSTRUCTIONS

Mnemonic	Description
CWAI	Clear condition code register bits and wait for interrupt.
NOP	No operation.
JMP	Jump.
JSR	Jump to subroutine.
RTI	Return from interrupt.
RTS	Return from subroutine.
SEX	Sign extend B register into A register.
SWI, SWI2, SWI3	Software interrupts.
SYNC	Synchronize with interrupt line.

Text continued from page 98:

instructions and LEA (load effective address) instructions. The relative-branch instructions allow PCR (program counter relative) branching. When an 8-bit offset is used, control may be transferred anywhere within a 256-byte area. A 16-bit offset allows transfer of control anywhere in the entire 64 K-byte address space. The following are examples of the relative-branch instructions:

DECA	Decrement A Accumulator
BEQ CAT	If A = 0 then go to CAT (CAT is within ± 128 bytes)
INCA	Increment A Accumulator
LBEQ DOG	If A = 0 then go to DOG (DOG is within ± 32,768 bytes)

The LEA instructions work by calculating the effective address of an indexed instruction and storing it in the specified pointer register. This allows the programmer to use all the internal addressing hardware of the microprocessor. Below are some examples of the LEA instructions.

Instruction	Operation
LEAX 10,X	X + 10 → X
LEAY A,Y	Y + A → Y
LEAX D,Y	Y + D → X
LEAU −10,U	U − 10 → U
LEAX TABLE,PCR	(see text below)

Note how the registers may be incremented or decremented using the LEA instructions. In addition, registers may be used as offsets, as explained above. The program counter may be used as a pointer register with 8- or 16-bit signed offsets. As in relative addressing, the offset is added to the current contents of the program counter register to create the effective address.

The last example calculates the offset of TABLE and adds it to the current value of the program counter register. This value is then placed in the X register. Tables related to a particular routine will maintain the same relationship after the routine is moved, since addresses are calculated when the code is executed.

Position-independent code is not without disadvantages, the major being that it generally takes 5 to 10 percent more space than nonrelocatable code. In addition, PIC usually takes 5 to 10 percent more time to execute. Typically, PIC would be used for utility programs where the run-time addresses are dynamically determined. This eliminates the need for a linking loader to perform a relocation operation. Common examples of this type of code would be machine-language utilities such as graphic routines and subroutines called by BASIC programs.

The MC6809E has several very interesting hardware features also. Referring to the signal descriptions of figure 2, note that not only does the microprocessor have 16 address lines, 8 data lines, and an $R/\overline{W}$ (read/write) line, but there are several other control lines. The MC6809E is synchronized to the video-display circuit by the two clock inputs, E and Q. These two clocks control internal operation of the microprocessor. Figure 4 shows typical timing diagrams for bus operations.

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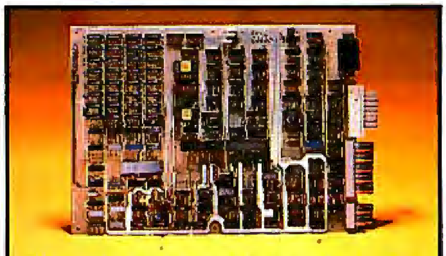
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Three interrupt control lines, $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, and $\overline{\text{IRQ}}$, allow peripherals to request (demand!) support. Each interrupt causes the microprocessor to retrieve a vector from a specific address and use it to begin executing instructions.

The Color Computer uses IRQ (interrupt request) and FIRQ (fast interrupt request) to support real-time clock input (driven by the horizontal and vertical sync signal from the VDG) and to auto-start read-only memory cartridges. The NMI (nonmaskable interrupt) input is reserved for use by the expansion port.

These interrupts function in different manners. The NMI cannot be disabled or postponed under software control and is useful in real-time interrupt-servicing disk transfers. The other two interrupts are maskable under software control. One is "faster" than the other in that a response to an FIRQ saves only the condition code register and the program counter on the stack. The other, IRQ, "stacks" all the registers, as does NMI. Separate interrupts were used for the PIAs (parallel interface adapters) to provide independent vector addresses for the service routines, thereby minimizing the software overhead.

The interrupt vectors in the Color Computer are mapped to the top of the BASIC ROM by the SAM chip. These vectors point to locations in programmable memory starting at address hexadecimal 100. On reset, the BASIC program stores jump instructions in these locations which point to the interrupt-service routines. Each jump call consists of 3 bytes: the jump extended op code (hexadecimal 7E) and the address of the routine. If a particular interrupt is not being used, all 3 bytes of its jump call would contain 00. See table 3 for a map of the interrupt-service addresses.

To define a jump call, program the 3 bytes with the required jump instruction. For example, if the SWI (software interrupt) service routine is located at hexadecimal 8000, the SWI jump call should be loaded with 7E 80 00. The following BASIC program would load the SWI jump call with this vector:

```
POKE 264,0
POKE 263,128
POKE 262,126
```

This example program defines the last byte of the jump call first, then the middle byte, then the first byte. This approach is required to prevent interrupt service until the jump call is completely defined. If the jump call was defined by starting with the first byte, an interrupt could be vectored to the wrong address. All interrupt-service routines should end with a hexadecimal 3B (Return from Interrupt op code) to restore the Color Computer to the proper state.

Two other MC6809E input-control signals used by the Color Computer are HALT and RESET. RESET is controlled by the pushbutton switch on the rear right-hand portion of the Color Computer. When the switch is pressed, RESET goes low to initiate a restart routine. The HALT input is connected to the expansion port. When HALT goes low, the MC6809E completes the current instruction, then releases the address, data, and R/$\overline{\text{W}}$ lines to the high-impedance state. This allows another device,

Text continued on page 110

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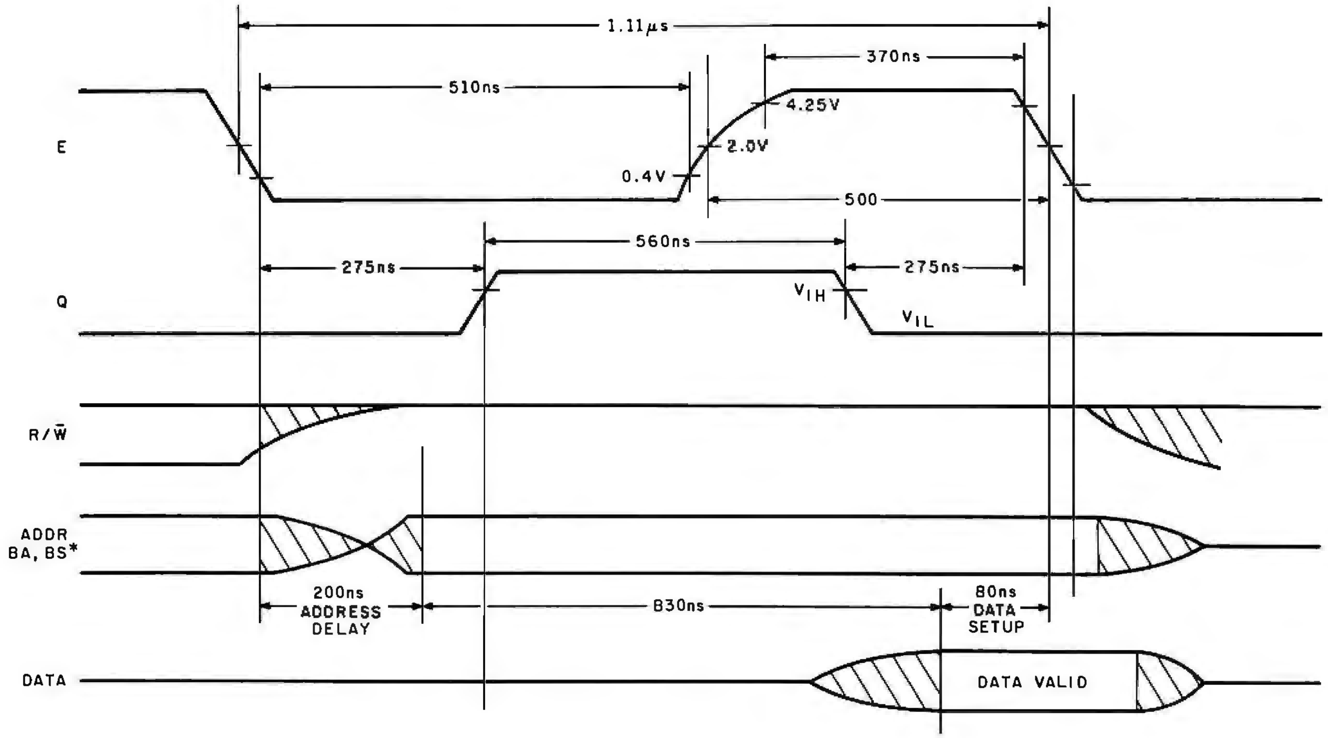

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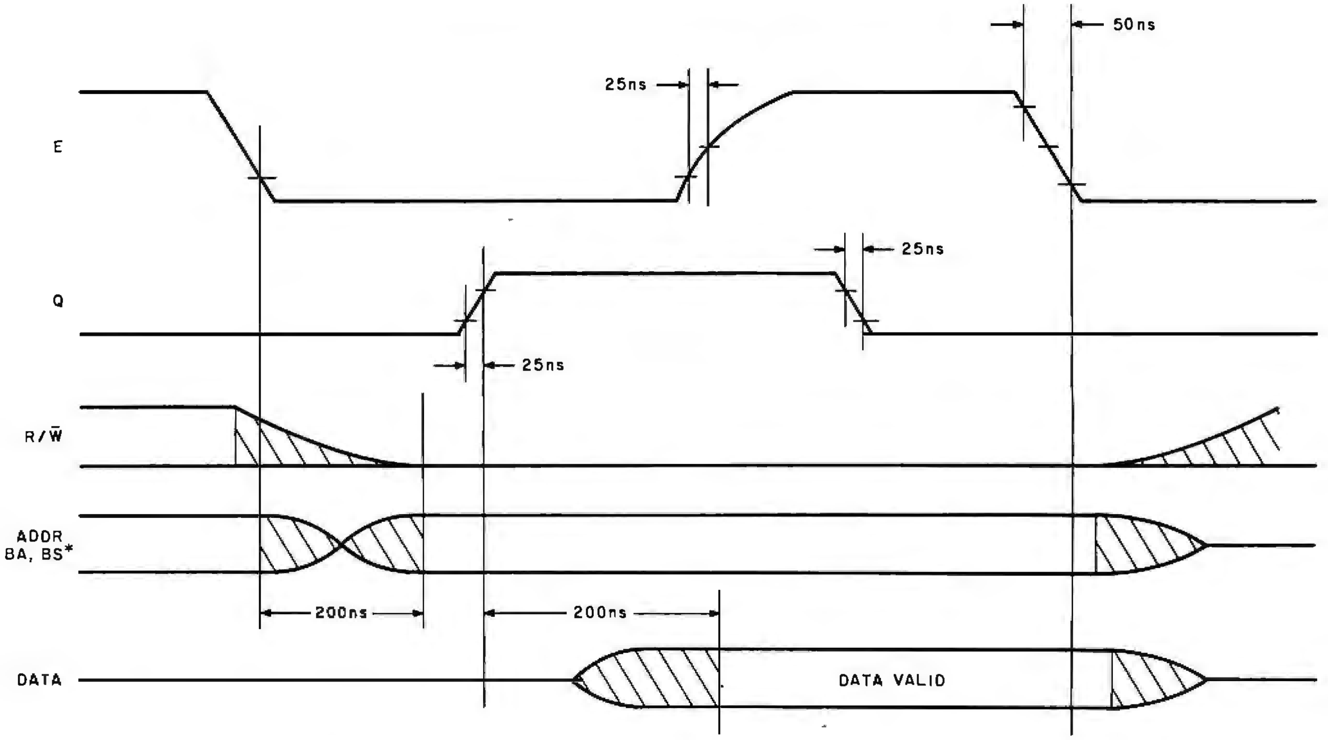

Figure 4: *Timing diagrams for 6809 bus operations. As with the 6800, both memory and peripherals are accessed in the same way and share the same address space. The complete instruction cycle for reads (figure 4a) and writes (figure 4b) is the same: approximately 1.1 μs.*

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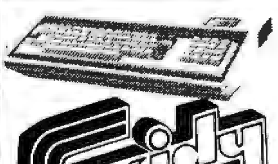

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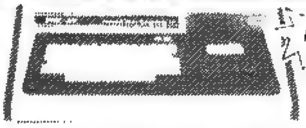

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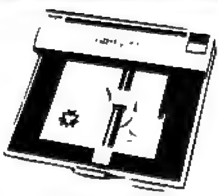

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Reset	FFFE	A027	none	direct call to restart
NMI	FFFC	0109	undefined	not used
SWI	FFFA	0106	undefined	not used
IRQ	FFF8	010C	A9B3	Extended BASIC uses 894C to update real-time clock.
FIRQ	FFF6	010F	A0F6	
SWI2	FFF4	0103	undefined	not used
SWI3	FFF2	0100	undefined	not used

Table 3: *Interrupt vectors for Color Computer BASIC. At the reception of an interrupt, control is transferred to a service routine via a call to an address stored near the top of the 64 K address space (occupied by the BASIC ROM). The address points to a 3-byte jump instruction (loaded into programmable memory when BASIC is initialized); that, in turn, points to an interrupt-handling routine.*

Bus Available Signal	Bus Status Signal	Machine State
low	low	Normal (running)
low	high	Synchronize Acknowledge
high	low	Interrupt Acknowledge
high	high	Halt/Bus-Grant Acknowledge

Table 4: *The four possible machine states. The Bus Available and Bus Status signals can be decoded to detect when the bus is not being used by the processor.*

Text continued from page 104:

such as a DMA (direct-memory access) controller, to control the bus.

Since the microprocessor is not halted until completion of the current instruction, the external bus controller has to wait 20 bus cycles before driving the bus. This delay is required because the longest execution time for an MC6809E instruction is 20 cycles for a CWAI instruction (see table 2).

This delay could have been minimized if the BA and BS lines were brought out to the expansion port. BA and BS (Bus Available and Bus Status) indicate one of four machine states. These four states and the BA and BS signal combinations are shown in table 4.

Of the four states, the *Halt/Bus-Grant Acknowledge* is the only one pertinent to the design of the Color Computer. The *Normal* state indicates that the microprocessor is executing code. The *Synchronize Acknowledge* state, which allows the processor to be synchronized to an external event, is not required in the Color Computer. Nor is the *Interrupt Acknowledge* state, which indicates that vector fetches are occurring.

Four other MC6809E signals were ignored by the Color Computer's designers: TSC, AVMA, BUSY, and LIC. TSC (Three State Control) is used to put the buses into the high-impedance state for cycle-stealing operations.

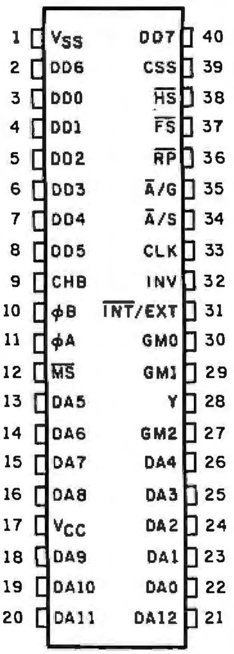

Figure 5: *Pin description of Motorola's MC6847 Video Display Generator. In concert with the Synchronous Address Multiplexer (see figure 6), this device interprets the contents of a block of memory to create a color display (using either an internal character generator or an external one). The output signal is converted to composite video by an MC1372, while a device built of discrete components modulates the signal to radio frequencies for reception on a standard television.*

This type of operation is typically used for DMA or dynamic-memory refresh and is not needed in the Color Computer.

AVMA, BUSY, and LIC are intended primarily for use in multiprocessor systems (which the Color Computer is not). AVMA (Advanced Valid Memory Access) is the signal indication that the processor will use the bus during the next cycle. The BUSY output provides the "indivisible" memory indication required for a "test and set" operation (operations of this type are required for efficient multiprocessor support on a common bus). LIC (Last Instruction Cycle) indicates that the first byte of an op code will be latched at the end of the present bus cycle.

The MC6809E was the best choice of the microprocessors available for use when the Color Computer was designed. The external clock inputs allow the microprocessor to be synchronized to the video display to allow interleaved memory accesses. In addition, the power of the MC6809E instruction set allows the efficient graphics drivers supported by the Extended BASIC.

The Video Display and the Memory Controller

The "Color" in Color Computer comes from the MC6847 Video Display Generator. This device can display information stored in memory using a variety of alphanumeric, semigraphic, and graphic modes. To understand how it works, refer to the signal description shown in figure 5. Normally the address lines DA0 thru DA12 would be connected to a block of programmable memory (usually static devices such as MCM2114s) shared with the microprocessor. Depending on the mode selected, the VDG would read the memory and, taking

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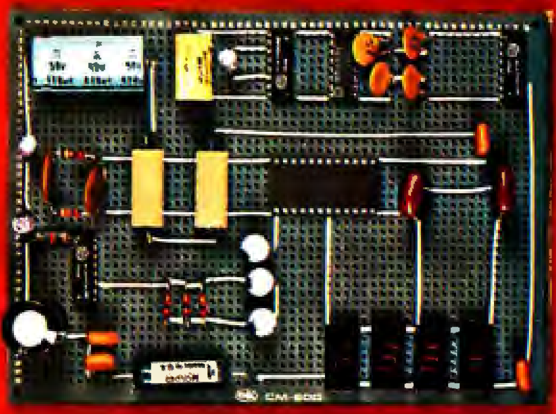

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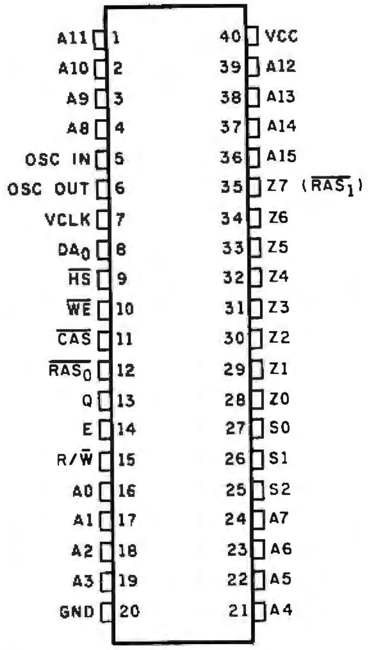

Figure 6: *Pin description of Motorola's MC6883 Synchronous Address Multiplexer. This device provides the complex timing signals required by the microprocessor and for refresh of dynamic memories, as well as multiplexing addresses going into the memories. The various programmable modes of the video-display generator are provided for so that the SAM can help to refresh the video display. (This occurs during the portions of instruction cycles that the processor does not access memory.)*

the information off its data lines (DD0 thru DD7), it would format and shift out video information to its companion part (the MC1372 Color Television Modulator) to be transmitted to a TV receiver.

This method of using the part is fine, but it has a few drawbacks. First, there needs to be a way to allow the microprocessor to write its output data to memory. This means that there must be three-state buffers between the microprocessor bus and the VDG bus (and logic to control them). A control pin on the VDG, Memory Select (MS), must be used to put the VDG's address lines in the high-impedance state when the processor accesses the memory.

One side effect of this is that the VDG shift registers will be filled with the data from its data bus as usual, except that the address lines are under the control of the microprocessor, and so the data that gets sent out on the video lines is incorrect. This results in "sparkles" of random color on the TV screen and can be annoying when you are trying to move your TIE fighter out of enemy gunsights!

Second, there is only one block of memory for the VDG to "look" at. In trying to implement computer animation, it would be nice to allow the microprocessor to draw one picture while another is being displayed. Then you would simply swap memory pages and, voilà, the horse moves! You can't do this with the system outlined above unless you resort to fancy hardware.

Of course, both of these problems can be overcome. We have seen it done with an entire board full of TTL (transistor-transistor logic) packages but this is expensive and not for the faint of heart. Fortunately, these problems have a solution in the form of another LSI device from—you guessed it—Motorola. The MC6883 SAM (Synchronous Address Multiplexer) is a 40-pin TTL part that marries the MC6809E and the MC6847 to some dynamic programmable memory.

SAM, the Synchronous Address Multiplexer

The little jewel called the SAM should really interest computer experimenters. In the first place, it provides the clock signals needed by the microprocessor. The E and Q clocks are derived from the 14.31818 MHz crystal—they are normally 895 kHz—but this can be changed, as we will see. Secondly, the SAM also provides RAS (row-address strobe) and CAS (column-address strobe) signals for dynamic-memory refresh. As anyone who has tried to design a dynamic-memory board can tell you, it isn't easy; and one of the hardest things is deriving RAS and CAS and hiding the refresh cycle from the processor. The SAM does it all and could do it even without a VDG. A complete memory board could be designed around this device even if you didn't want a video display. A signal description of the MC6883 is given in figure 6.

To conserve the number of pins on a dynamic-memory circuit the address is multiplexed in 6-bit pieces (7 bits for 16 K-bit devices). The SAM takes all the microprocessor address lines, multiplexes them to the memory, and controls RAS, CAS, and WE (Write Enable). A typical read cycle is shown in figure 7.

The microprocessor puts out an address to read a location in the dynamic memory. The SAM splits this address into the row address and the column address. First the row address is presented to the memory on the output

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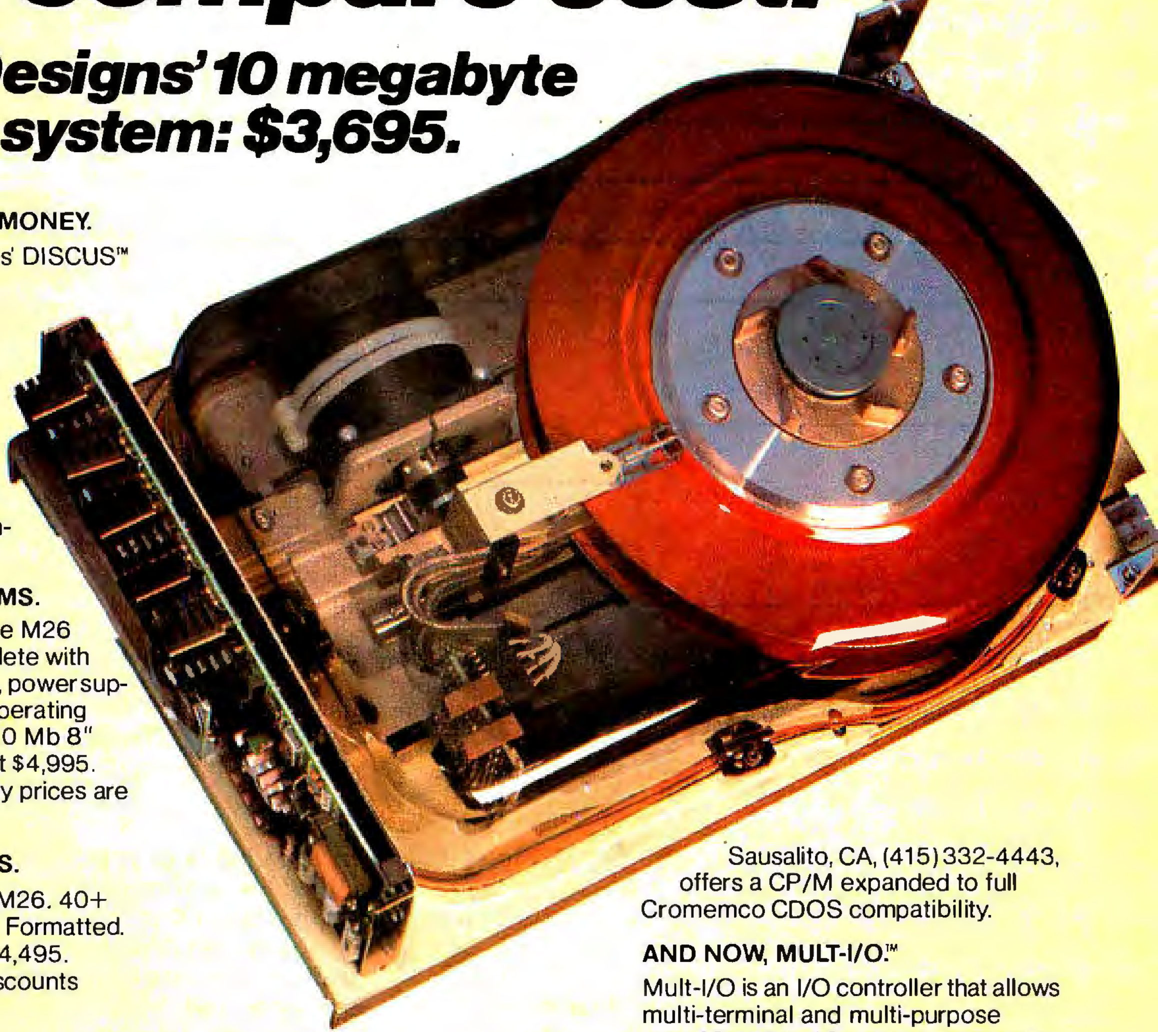

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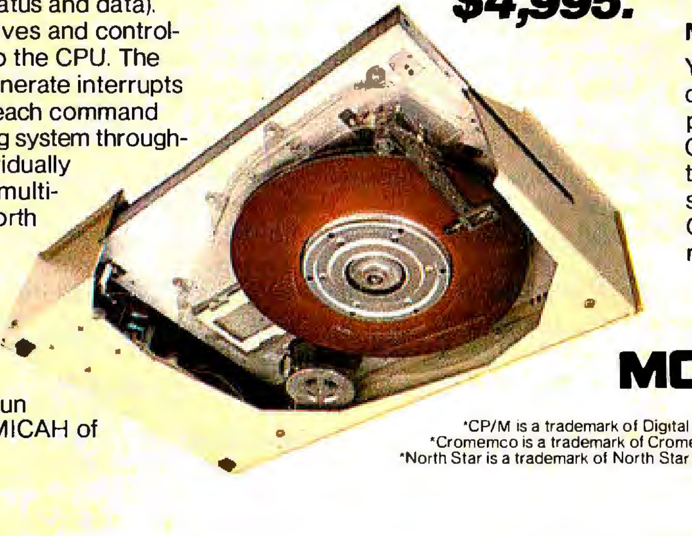

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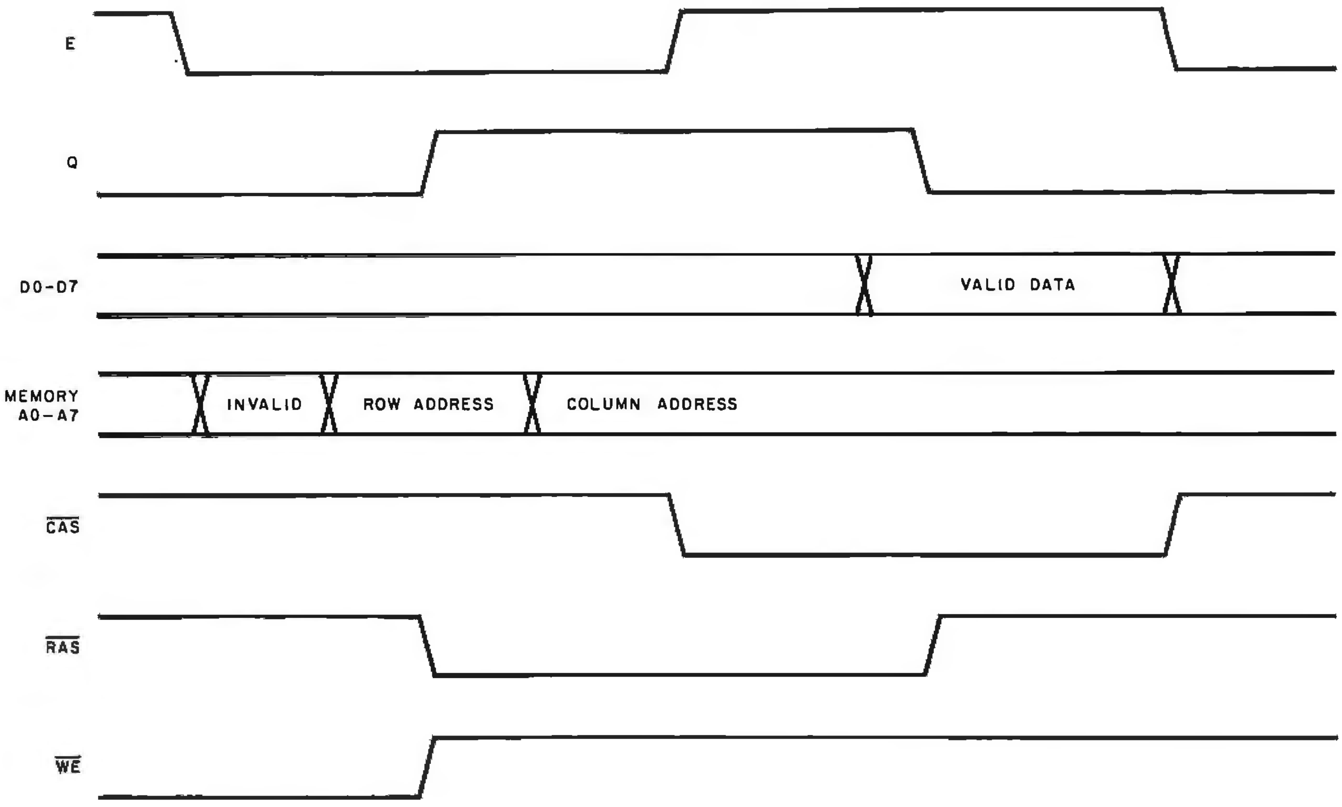

Figure 7: *Typical read cycle of 4116-type dynamic memory circuits. To reduce the number of pins required, the memory device interprets the address being accessed as two sets of 7 bits that come at different times over the same set of pins. The memory cells of each device are arranged in an array, and the two sets of bits define a* row address *and a* column address. *When a set of address bits is valid, either the CAS (column-address strobe) or the RAS (row-address strobe) signal is sent to latch in the respective portion of the address.*

lines Z0 thru Z5, and the falling edge of RAS causes the memory to latch this part of the address into internal decoders. The SAM then puts out the column address and drops CAS. This causes the memory device to latch the column address and decodes the location in the internal memory array. The memory's stored data is then put on the data-output lines and through a buffer to the microprocessor.

Now, what about refreshing? Dynamic-memory circuits are made of small capacitor cells and, unless they are refreshed, the charge that represents the stored information will bleed off in a very short time. The memories are constructed such that merely accessing all the row addresses every 2 ms will keep the data alive. Usually this is done with counters that need only count from 0 to 63 (0 to 127 for 16 K-bit devices). The trick is to hide this from the microprocessor.

In the MC6809E, this is possible because the microprocessor needs to access memory only during the time that the E clock is high, so all that must be done is to refresh the memories when E is low. The SAM also does this little chore.

There are two differences between a system that uses 4 K-bit circuits and one that uses 16 K-bit devices. First, the MCM4116 integrated circuits have an extra address line which must be connected to the Z6 output of the SAM. Second, the refresh counters in the SAM must be programmed to put out 128 refresh addresses for the MCM4116s instead of the 64 needed for the MCM4027s. The SAM has to be programmed to do this. How this is done will be detailed later.

In the Color Computer, the change is simple. There are only two jumpers that need to be switched to select either 4 K-bit or 16 K-bit memory devices. One of these connects the seventh address line, and one is connected to a PIA input line. Upon reset, the BASIC interpreter reads this bit and sets up the SAM for the type of memory indicated. That's all there is to it.

So what does all this have to do with the VDG? Since the VDG needs to be able to read memory to refresh the video screen, the SAM takes care of this, also. The address lines of the VDG are not connected at all in this system. Rather, the SAM is programmed into the same mode as the VDG and duplicates the timing of the VDG's address bus, except that it accesses memory to refresh the VDG during the E low time (so that the VDG accesses are transparent to the microprocessor). Since there is no possibility of a bus fight between the processor and the VDG, there is no need to deny the VDG access to the memory and the screen remains glitchless.

The full timing is shown in figure 8. The SAM usually provides memories with the address needed to access the data for the VDG to output as video. During the active display time (one frame of video) these addresses automatically refresh the memory devices. During the vertical retrace time, the SAM puts out refresh addresses. The microprocessor can access the memory at any time E is high and is therefore not affected.

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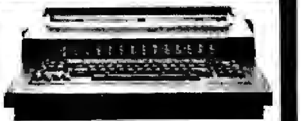

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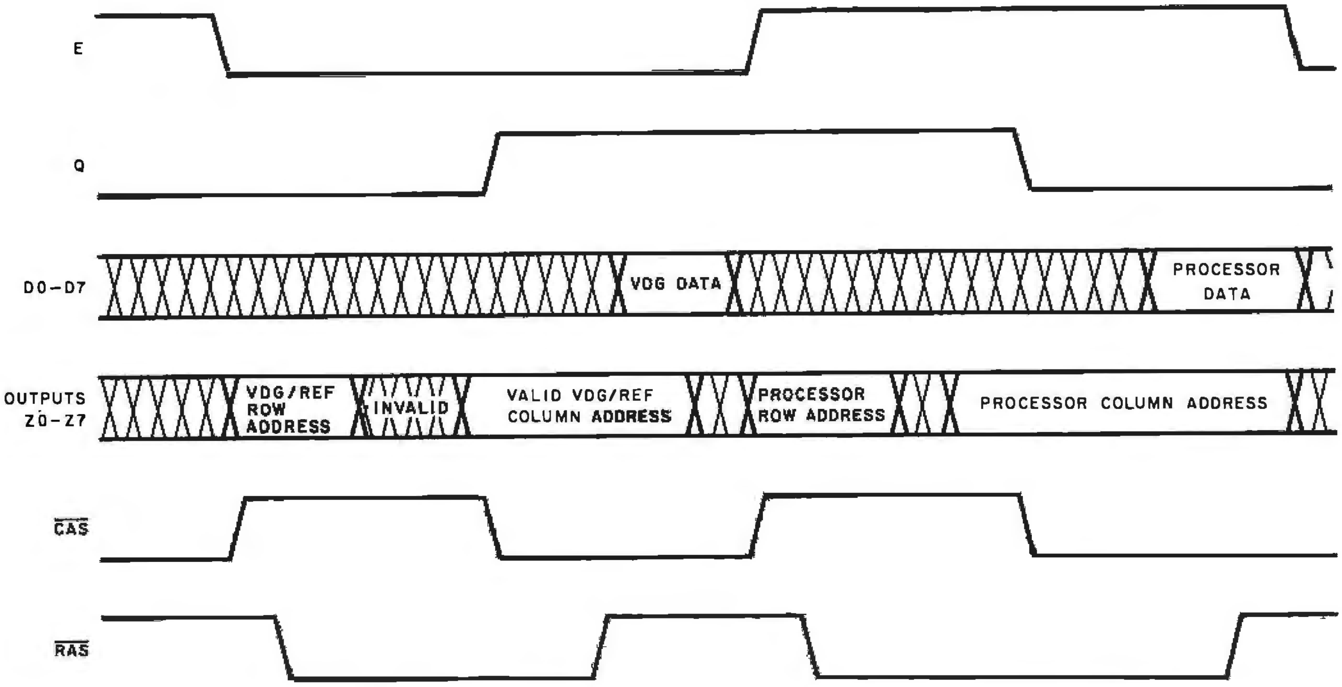

Figure 8: *Diagram of a typical dynamic-memory refresh cycle. The SAM provides every dynamic memory with a signal on each row address, as required, to refresh the data contained within.*

The VDG supports one alphanumeric mode, two semigraphic modes, and eight full graphic modes.

Programming the VDG

The VDG has 5 mode-control pins that determine how the address lines behave and how the data that is obtained from the memory is to be interpreted. In this system, these lines are connected to lines PB3 thru PB7 of PIA2. The data-output register for this device is located at address hexadecimal FF22. The microprocessor can write directly to this port to select the VDG mode. In fact, Extended Color BASIC has a statement, PMODE, to do just this.

The VDG has one alphanumeric mode (using its internal character generator or an external one), two semigraphic modes, and eight full-graphic modes. The modes and the way the mode-control pins must be programmed are shown in table 5.

The alphanumeric mode is the one used by BASIC to print on the screen. The VDG sequentially reads 512 bytes from memory for each TV frame. The data is interpreted as character codes, with the first byte corresponding to the top left corner ("home" position). There are 16 rows of 32 characters for a total of 512 characters on the screen. The character code is given in table 6.

Lowercase characters are displayed as inverted (light characters on a dark background). This is done by tying bit 6 (DD6) of the VDG to the INVERT pin. Because this bit is set in all lowercase numbers, they are inverted.

To support the SET and RESET commands in Radio Shack's Level I BASIC, data line DD7 on the VDG is connected to the alpha/semigraphic pin $(\overline{A}/S)$. Whenever this bit is set, the VDG will interpret the data in the manner shown in table 5, under the semigraphic-4 mode. Instead of displaying a character, a colored block that is divided into four smaller blocks is displayed. The code in the byte read from memory determines which pattern of blocks is shown and what color it is. Using the smaller element within the block as a pixel, this gives a grid of 64 by 32 blocks, which are the dimensions of the SET and RESET commands. The other semigraphic mode is similar to this, but each large block is divided into six blocks (instead of four) and has a choice of two sets of four colors, controlled by the CSS (Color Set Select) pin. (Refer to the semigraphic-6 mode in table 5.)

The remaining eight modes are of the bit-mapped graphic type. They require 1, 1.5, 2, 3, or 6 K bytes of memory, depending on the mode. Basically, the data in memory is interpreted as pixels. In the four-color modes (1-C, 2-C, 3-C, and 6-C), each pixel is represented by 2 bits, selecting one of four colors. The set of colors is selectable by the CSS pin. In the two-color modes (1-R, 2-R, 3-R, and 6-R), each bit is mapped one-to-one on the screen. If the bit is set, the pixel is colored, and if it is not set, the pixel is black. The color set can be changed so the pixel can be either buff or green; color sets are controlled by the CSS pin. The resolution of these modes varies from 64 by 64 to 256 by 192 pixels horizontal and vertical respectively.

To use these graphic modes, you simply program the VDG by writing the mode code into the PIA output register, and write to the "screen memory" addresses. The only problem is that the VDG's address lines are not connected to any memory. As mentioned before, the SAM provides the addresses and the VDG interprets the data from the memory, so the SAM must be programmed to be in the same mode as the VDG in order to get a mean-

Text continued on page 120

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MODES	VDG PINS									COLOR			TV SCREEN	VDG DATA BUS
	$\overline{\text{MS}}$	$\overline{\text{A}}$/G	$\overline{\text{A}}$/S	$\overline{\text{INT}}$/EXT	GM2	GM1	GM0	CSS	INV	Character Color	Background	Border	Display Mode	
The alphanumeric internal mode uses an internal character generator which contains the following 5 dot by 7 dot characters: @ABCDEFGHIJKLMNOPQRSTUVWXYZ[\ ] ↑ ← SP !"#$%&'()* + , – /0123456789:;< = > ?. The 6 bit ASCII code leaves 2 bits free and these may be externally connected to the mode pins ($\overline{\text{A}}$/G, $\overline{\text{A}}$/S, $\overline{\text{INT}}$/EXT. GM2, GM1, GM0, CSS or INV).	1	0	0	0	X	X	X	0 1	0 1 0 1	Green Black Orange Black	Black Green Black Orange	Black Black	32 characters across 16 characters down	E_1 E_0 A_5 A_4 A_3 A_2 A_1 A_0 extra ASCII code
The alphanumeric external mode uses an external character generator as well as a row counter. Thus, custom character fonts are graphic symbol sets with up to 256 different 8 dot by 12 dot "characters" that may be displayed.	1	0	0	0	X	X	X	0 1	0 1 0 1	Green Black Orange Black	Black Green Black Orange	Black Black	32 characters across 16 characters down	one row of custom characters
The semigraphic-4 mode uses an internal "coarse graphics" generator in which a rectangle (8 dots by 12 dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by 3 bits.	1	0	1	0	X	X	X	X	X	Lx C2 C1 C0 0 X X X 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	Color Black Green Yellow Blue Red Buff Cyan Magenta Orange	Black	64 display elements across 32 display elements down	X C_2 C_1 C_0 L_3 L_2 L_1 L_0
The semigraphic-6 mode is similar to the semigraphic-4 mode with the following differences: the 8 dot by 12 dot rectangle is divided into six equal parts. Color is determined by the 2 remaining bits.	1	0	1	1	X	X	X	0 1	X	Lx C1 C0 0 X X 1 0 0 1 0 1 1 1 0 1 1 1 0 X X 1 0 0 1 0 1 1 1 0 1 1 1	Color Black Green Yellow Blue Red Black Buff Cyan Magenta Orange	Black	64 display elements across 48 display elements down	C_1 C_0 L_5 L_4 L_3 L_2 L_1 L_0
The graphic 1-C mode uses a maximum of 1024 bytes of display memory in which one pair of bits specifies one picture element.	1	1	X	X	0	0	0	0 1	X	C1 C0 0 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1	Color Green Yellow Blue Red Buff Cyan Magenta Orange	Green or Buff	64 display elements across 64 display elements down	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0
The graphic 1-R mode uses a maximum of 1024 bytes of display memory in which one bit specifies one picture element.	1	1	X	X	0	0	1	0 1	X	Lx 0 1 0 1	Color Black Green Black Buff	Green or Buff	128 display elements across 64 display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0
The graphic 2-C mode uses a maximum of 2048 bytes of display memory in which one pair of bits specifies one picture element.	1	1	X	X	0	1	0	0 1	X	Same color as graphic 1-C mode		Green or Buff	128 display elements across 64 display elements down	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0
The graphic 2-R mode uses a maximum of 1536 bytes of display memory in which one bit specifies one picture element.	1	1	X	X	0	1	1	0 1	X	Same color as graphic 1-R mode		Green or Buff	128 display elements across 96 display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0
The graphic 3-C mode uses a maximum of 3072 bytes of display memory in which one pair of bytes specifies one picture element.	1	1	X	X	1	0	0	0 1	X	Same color as graphic 1-C mode		Green or Buff	128 display elements across 96 display elements down	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0
The graphic 3-R mode uses a maximum of 3072 bytes of display memory in which one bit specifies one picture element.	1	1	X	X	1	0	1	0 1	X	Same color as graphic 1-R mode		Green or Buff	128 display elements across 192 display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0
The graphic 6-C mode uses a maximum of 6144 bytes of display memory in which one pair of bits specifies one picture element.	1	1	X	X	1	1	0	0 1	X	Same color as graphic 1-C mode		Green or Buff	128 display elements across 192 display elements down	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0
The graphic 6-R mode uses a maximum of 6144 bytes of display memory in which one bit specifies one picture element.	1	1	X	X	1	1	1	0 1	X	Same color as graphic 1-R mode		Green or Buff	256 display elements across 192 display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0

Table 5: *Video Display Generator modes.*

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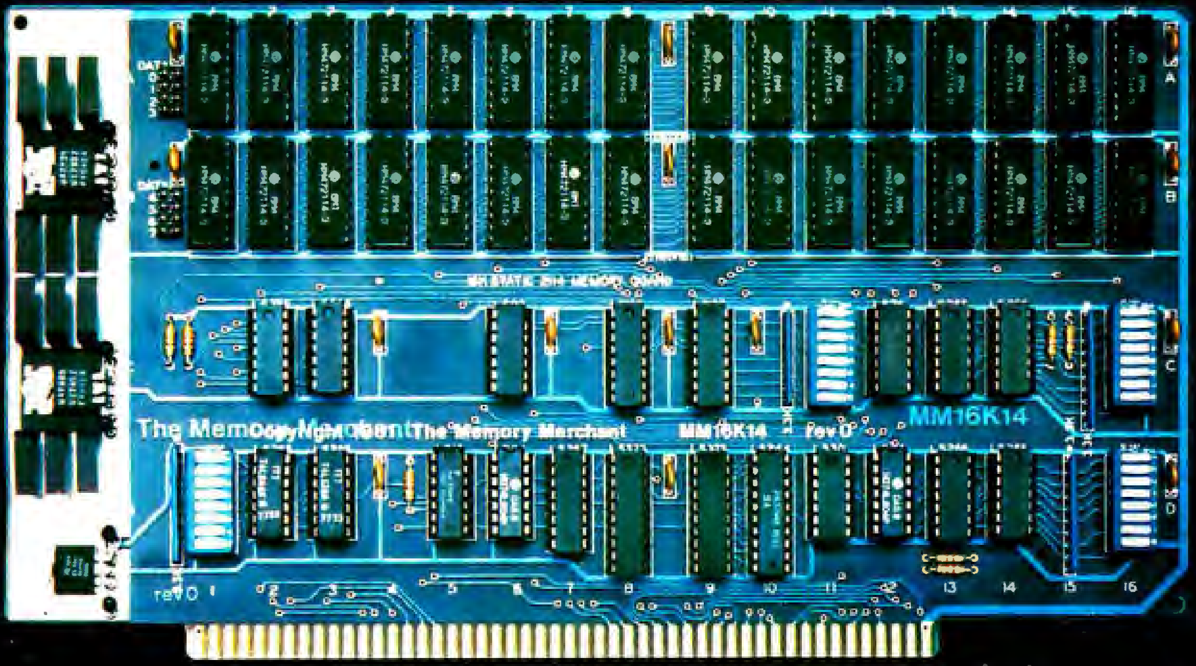

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1	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	←
2		!	"	#	$	%	&	'	(	)	*	+	,	–	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	←
6		!	"	#	$	%	&	'	(	)	*	+	,	–	.	/
7	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?

Table 6: *Codes for the characters stored in the VDG's internal character generator. The lower section contains inverse-video characters, dark characters on a light background.*

Text continued from page 116:

ingful display.

Programming the SAM

With a SAM in the system, the memory map is pretty much fixed. The SAM directly decodes the addresses from the processor to access memory, and provides device selects for the rest of the sytem on the S0 thru S2 pins. These pins are decoded by a 3-to-8 decoder (74LS138) to get the active-low select signals for the rest of the system. Refer to the memory map shown in figure 9.

The reset vector and interrupt vectors at the top of the map are mapped from hexadecimal FFF2 thru FFFF to BFF2 thru BFFF. This allows these vectors to be stored in the 8 K-byte BASIC ROM beginning at address hexadecimal A000. The addresses of the two PIAs, the second ROM, and the off-board ROM cartridges are also shown in figure 9.

The block of addresses from hexadecimal FFC0 to FFDF are the locations of the SAM registers. The SAM is programmed and its various options selected by writing to these locations. The data is immaterial since the data bus is not connected to the SAM. Each register bit has two unique locations, an even location and an odd one. Writing to the even location will clear the register bit. Writing to the odd location will set the bit. By encoding the bits, and accessing the appropriate locations, the SAM can be programmed.

The memory map in figure 9 shows the modes and the locations associated with each. S stands for set and C for clear in the diagram. The programmable attributes include:

- •VDG mode—mode of address lines during VDG refresh time.
- •Display offset—the base address of the memory used by the VDG is specified here. This is the address of the pixel in the upper left-hand corner of the screen in graphic mode. Programmable in ½ K pages.
- •Memory size—4 K-bit, 16 K-bit or 64 K-bit dynamic memories or a full map of static memory and I/O.
- •Microprocessor clock rate—can be set for 0.8, 1.8 MHz or address-dependent rate.
- •Page—allows two 32 K-byte memory pages between hexadecimal 0000 and 7FFF.

The VDG mode bits in the SAM must be programmed to match the mode selected for the VDG on its mode pins. Table 7 shows the correspondence between the SAM and the VDG modes. If the two modes do not agree, interesting results can be obtained. Some of these "mixed" modes include graphics mixed with alphanumerics.

The VDG address offset specifies where the SAM should start the address counters. Figure 10 shows the address sent by the SAM as a function of this offset. This allows the VDG display to be "paged" through memory in 512-byte pages, allowing fast page swapping for animation, etc. On reset, BASIC will set the offset to hexadecimal 400 so all the screen output of the BASIC interpreter is at locations hexadecimal 400 thru 5FF. Try POKEing to these locations to use the alphanumeric and semigraphic modes.

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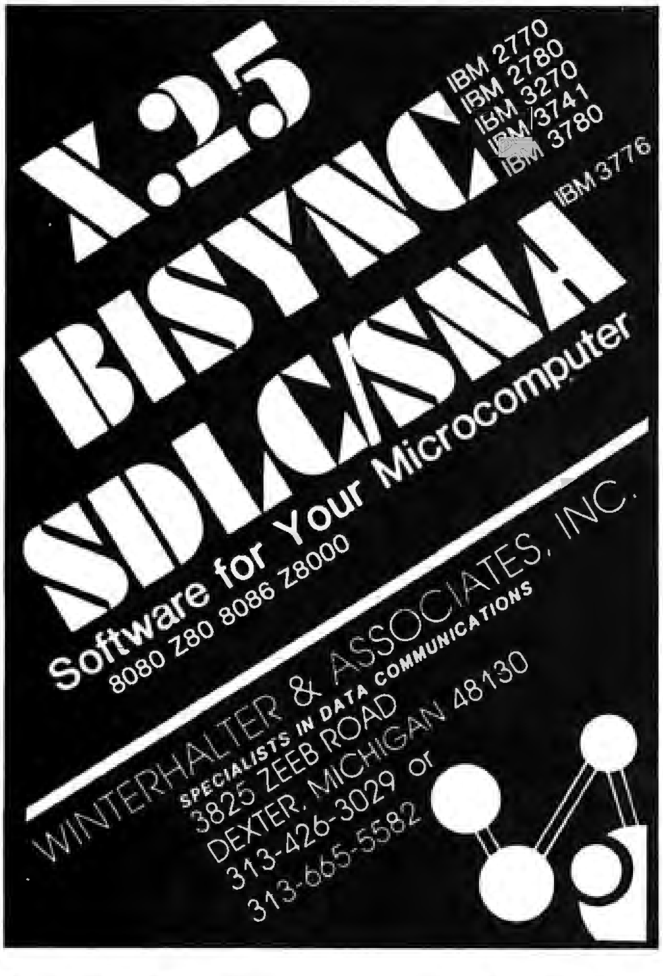
Text continued on page 124



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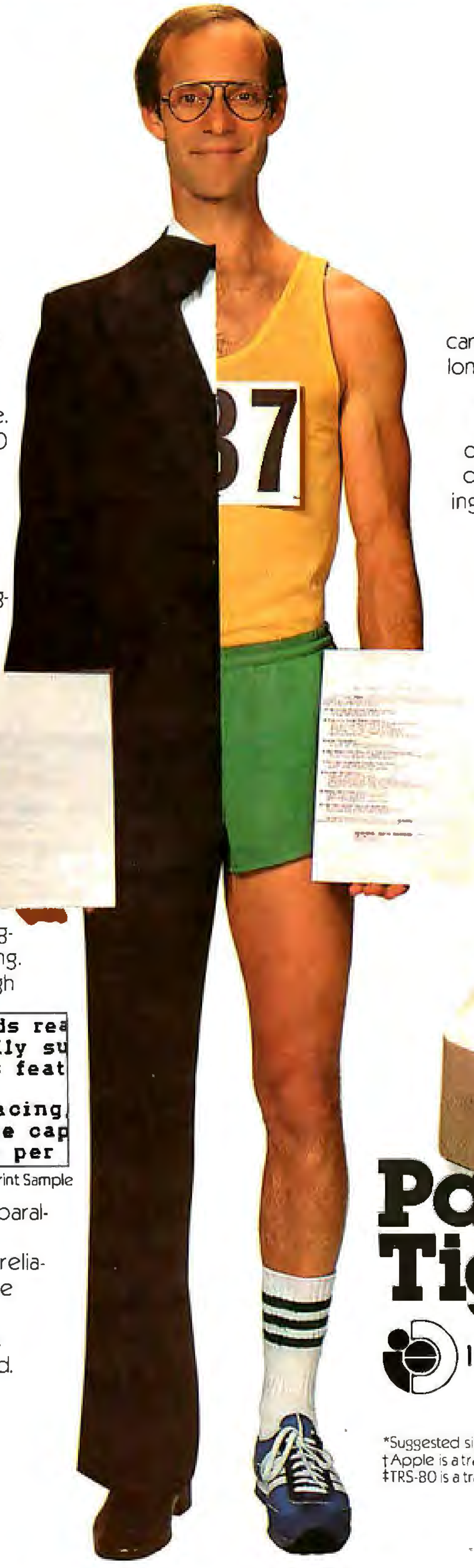

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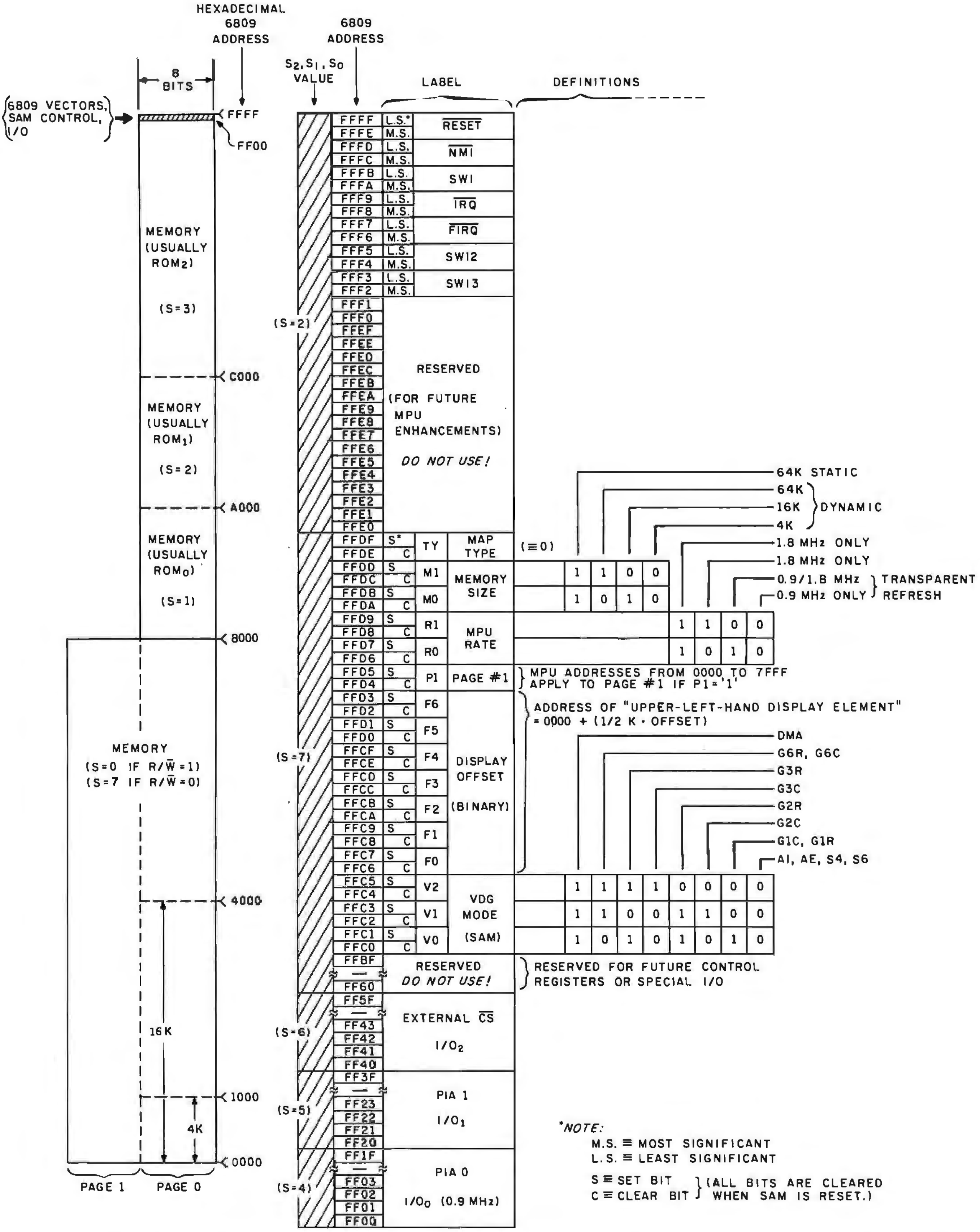

Figure 9: *Memory map of the Color Computer address space. The general division of addresses is provided at the left, while the SAM programming registers and the processor-interrupt vectors are expanded at the right.*

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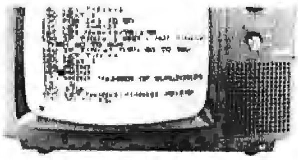

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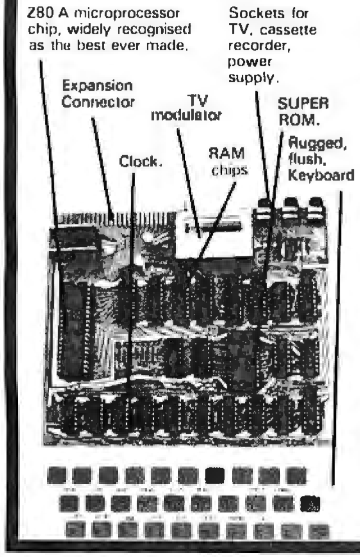

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Mode	Video Display Generator Signals					Synchronous Address Multiplexer Signals		
	G/$\overline{A}$	GM2	GM1	GM0 EXT/$\overline{I}$	CSS	V_2	V_1	V_0
Internal alphanumeric	0	X	X	0	x	0	0	0
External alphanumeric	0	X	X	1	X	0	0	0
Semigraphic-4	0	X	X	0	X	0	0	0
Semigraphic-6	0	X	X	1	X	0	0	0
Full graphic 1-C	1	0	0	0	X	0	0	1
Full graphic 1-R	1	0	0	1	X	0	0	1
Full graphic 2-C	1	0	1	0	X	0	1	0
Full graphic 2-R	1	0	1	1	X	0	1	1
Full graphic 3-C	1	1	0	0	X	1	0	0
Full graphic 3-R	1	1	0	1	X	1	0	1
Full graphic 6-C	1	1	1	0	X	1	1	0
Full graphic 6-R	1	1	1	1	X	1	1	0
Direct memory access	X	X	X	X	X	1	1	1

Table 7: *Mode correspondence between the SAM and the VDG.*

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
F_6	F_5	F_4	F_3	F_2	F_1	F_0	0	0	0	0	0	0	0	0	0
MSB															LSB

Figure 10: *Mapping of the video-display refresh address. The SAM uses a 7-bit offset to determine the start of video-display memory. This allows the use of 512-byte "pages" for display refreshing, making it possible to page through memory to create fast animation effects, etc.*

Text continued from page 120:

graphics and can also allocate more memory for multiple pages, up to eight. It provides graphic operations, such as LINE, DRAW, and CIRCLE, that are fast enough to allow the programming of real-time games using the joysticks as controllers.

Memory type is self-explanatory. The SAM must be programmed for the type of memory devices used in the system to produce the correct timing signals. If 16 K-bit circuits (MCM4116 or the equivalent) are used, pin 35 can be used for RAS1. This is needed to select a second bank of devices to provide 32 K bytes of memory. One way to do this on the Color Computer is to piggyback a second set of eight MCM4116s on top of the existing integrated circuits, paralleling all the pins except for the RAS pin. When this is jumpered to pin 35 on the SAM, the system then has 32 K bytes of user-programmable memory.

The microprocessor clock rate is also programmable. There are three modes, as shown in figure 9. In mode 0, the clock rate is fixed at one-sixteenth the crystal frequency. In this case, that is 895 kHz. Mode 2 gives a fixed rate of one-eighth the crystal frequency, or 1.8 MHz. This can be used with an MC68B09E, a 2 MHz version of the microprocessor. However, there are no memory or VDG addresses output in this mode, so don't use it.

Mode 1 is the most interesting. It gives a dual-rate clock of 895 kHz or 1.8 MHz depending on the address used in the bus cycle. When the processor accesses addresses from hexadecimal 0000 to 7FFF and FF00 to FF1F, the lower rate is used, allowing for slower memory and peripherals. When all other addresses are accessed, the processor runs at 1.8 MHz. Using fast ROMs will almost double the speed of the system because a majority of the microprocessor's memory references are to fetch op codes. If you want to try this, execute the following BASIC statement:

```
POKE 65495,0
```

This will set bit R0 of the microprocessor rate register at location hexadecimal FFD7 and put the SAM into the dual-rate mode. If your microprocessor can run at the higher speed (a pretty good bet), you will see the changing-color cursor flashing about twice as fast as normal. Your BASIC programs will now run about twice as fast, too. There is one problem, though — don't try to use the SOUND, CLOAD, or CSAVE statements in this mode. The PIA used by these statements is at location hexadecimal FF20 and it will probably not run at the higher speed.

The other two registers do not apply to the Color Computer. The Map Type bit chooses a mixed programmable/read-only type of system such as the Color Computer or a fully programmable system such as a disk-based one. The Page bit allows two 32 K-byte pages of memory to be accessed between locations hexadecimal 0000 and 7FFF. This can't be done on this system.

Keyboard Scanning

The keyboard is configured as an 8 by 7 matrix of keys. The Color Computer uses a software routine to encode the keyboard in a manner similar to that of the TRS-80 Model I. This is done by shifting a 0 through the B port of PIA IC8. The B port drives the 8 rows of the keyboard; the 7 columns are connected to the A port of IC8. The A port has internal pull-up resistors that provide a logic 1 level unless a key is depressed. When the shifted 0 occurs on the row of the closed key contact, the low level is passed to port A. By repeating the scanning procedure several times, debounced inputs are recognized.

If you need to monitor the keyboard during a program, a function (INKEY$) is provided. The BASIC statement

```
A$ = INKEY$
```

will return a character if a key is closed when the function is called. An example use of this function would be to monitor the keyboard during a "Tank" game for direction

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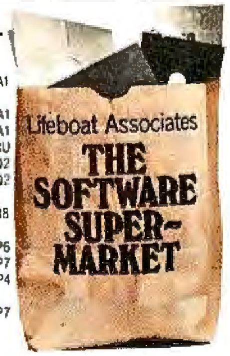

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keys and a "Fire" key. This would allow you to play a "Tank" game without having a set of joysticks.

Digital-to-Analog Converter

The D/A (digital-to-analog) converter allows the Color Computer to send analog waveforms. These signals are used for the cassette output, sound to the video modulator, and as a reference signal for A/D (analog-to-digital) conversion.

Six of the eight port A lines are configured as outputs and buffered to drive a resistive adder network for analog signal generation, as shown in figure 11. The resultant analog signal ranges from 0 V to +5 V in 78 mV steps.

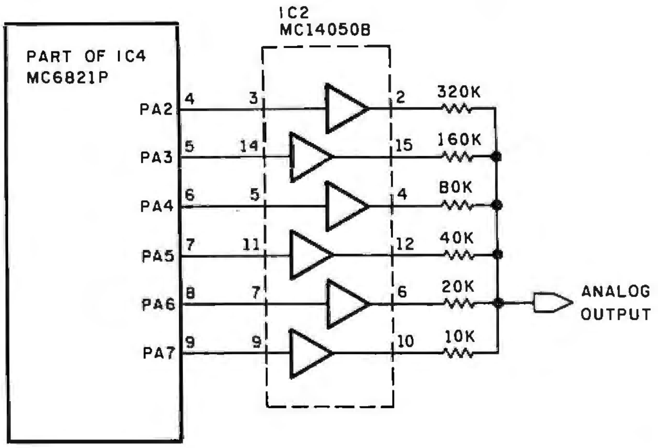

Figure 11: *Schematic diagram of the Color Computer's digital-to-analog converter. In a rather simple scheme, the output lines of a parallel port drive a resistive adding network to provide conversion. The resulting analog signals are used for recording on a cassette, providing the video modulator with sound, and also as part of the analog-to-digital converter.*

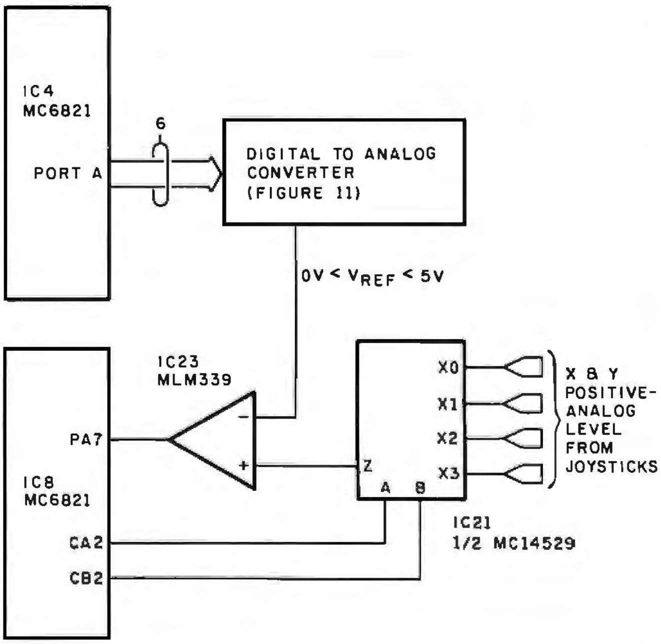

Figure 12: *Diagram for the analog-to-digital converter circuit. Also used as the joystick interface, this circuit applies the successive-approximation method (see figure 13) to change analog signals to digital form.*

This type of converter is accurate to ±½ the least significant bit, or in this case ±39 mV.

Cassette Port

The Color Computer has a cassette port which connects to a low-cost recorder. Motor-control capability is included that allows the cassette recorder to be started or stopped as required. The motor can be turned on and off with the statements MOTOR ON and MOTOR OFF. This allows the user to fast-forward or rewind tapes without having to unplug connections to the Color Computer.

Data is output to the recorder from the D/A converter. If an oscilloscope is connected to the data-output line, pin 5 of the cassette jack, an 800 mV 1500 bps signal will be seen.

When data is loaded from the cassette recorder, the playback signal can be routed to the modulator sound input in a manner that allows you to monitor the cassette signal via the speaker of a television set. This is done with the AUDIO ON and AUDIO OFF statements.

The cassette data-output can be used for an analog output level because the D/A converter can be controlled by a user program. The motor-control relay can be used to control loads up to 6 V DC at 500 mA.

Joystick Interface

Two joystick ports are provided which allow full *x*,*y* directional control. Each joystick has a pushbutton for use with games (eg: paddle control for the Pinball game). Each joystick consists of two potentiometers, each connected across +5 V and ground. The wiper of each potentiometer is connected to the input of an analog multiplexer controlled by PIA IC8. The voltage level from each of the four potentiometers is routed to the A/D converter to get a digital value for the position. This value will range between 0 and decimal 63. The JOYSTK(j) function returns the digital value of the joystick position.

Analog voltage levels from the joysticks are digitized using a successive-approximation technique. This is one of the more popular methods of A/D conversion. The 6-bit D/A converter is used in a feedback loop to generate a known analog signal to which the unknown analog joystick input is compared. This technique is not as fast as a flash converter, nor is it as slow as a binary counter.

Figure 12 shows the block diagram for the successive-approximation converter circuit. Figure 13 shows a flowchart for this approach. The D/A converter inputs are controlled by the microprocessor to form a successive-approximation register. The analog output is compared to the analog joystick input by the MLM339 comparator whose output is monitored by the MC6809E.

At the start of a conversion the MSB (most significant bit) of the D/A converter is turned on by the microprocessor, producing an output equal to half the full-scale value. This output is compared to the analog input and if it is greater than the joystick voltage, the microprocessor turns the MSB off. However, if the D/A output is less than the joystick voltage, the MSB remains on.

Following the trial of the MSB, the next most significant bit is turned on and again the comparison is made

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between the converter's output and the joystick voltage. The same criteria apply and this bit is either kept on or turned off. This procedure of testing each bit continues four more times until the 6 bits of the D/A converter have been set to the proper level.

Once the conversion is complete the microprocessor reads the joystick output by reading port A of PIA IC4. The internal structure of port A allows a read of the port to sample the output logic levels. Now the Color Computer has the digital value for the joystick voltage. The time necessary to do this conversion is constant and does not vary with the analog voltage level.

Note that the Color Computer has an on-board A/D converter that accepts a signal between +5 V and ground and can digitize it with less than a 40 mV error. This means you can use the appropriate joystick inputs to monitor various analog voltages. The switch inputs are connected to the PIA (the left switch to IC8 pin 3, PA1; and the right switch to IC8 pin 2, PA0). You can write a progam to monitor these bits for use with external devices. Figure 14 shows the connectors for the joysticks (which are not shown in the TRS-80 Color Computer Operation Manual).

RS-232 Interface

An RS-232 interface is also provided. This allows you to connect all manner of devices to the Color Computer. The standard RS-232 Transmit Data, Receive Data, and Carrier Detect signals are provided. This is the fundamental signal subset used by most devices. Tandy sells an off-the-shelf line of printers and a modem that are readily usable.

Expansion Port

The expansion port provides the capability to interface almost anything to the Color Computer. Table 8 lists the pins and their functions. Note that the entire address bus is brought out. There is also a decode-defeat pin which disables the 74LS138 that decodes ROMs and peripherals. This allows the expansion port to redefine the memory map. For instance, a flip-flop could be toggled to remove the BASIC and Extended BASIC ROMs from the memory map and replace them with programmable memory. A disk-controller board could also contain 48 K bytes of memory to fill the system from address hexadecimal 0000 to FF60.

The Vector Graphic company makes a wire-wrap prototype board (part number 4609) that fits the expansion connector of the Color Computer. This allows you to build your own peripheral boards. We are working on an interface to the General Instrument "Cricket" sound generator. The output from this circuit can be routed to the video modulator through a pin on the expansion connector. If you want, you can also build your own game

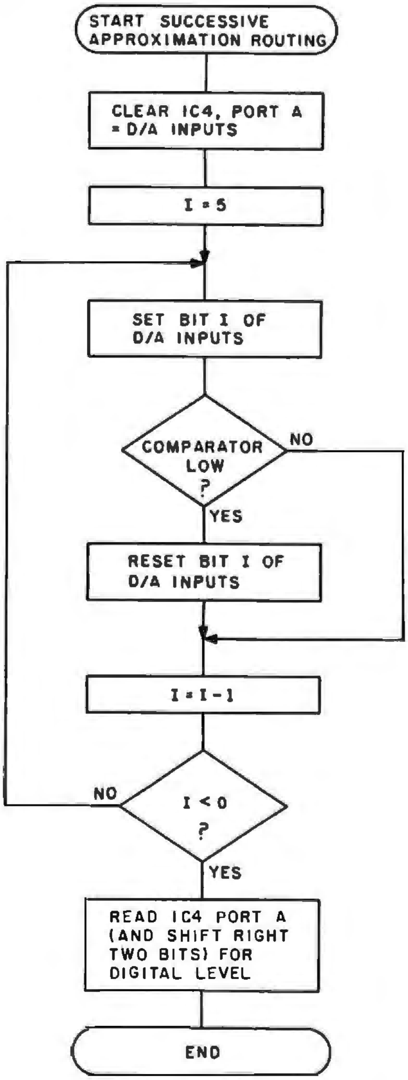

Figure 13: *Flowchart of the successive-approximation algorithm used by the Color Computer.*

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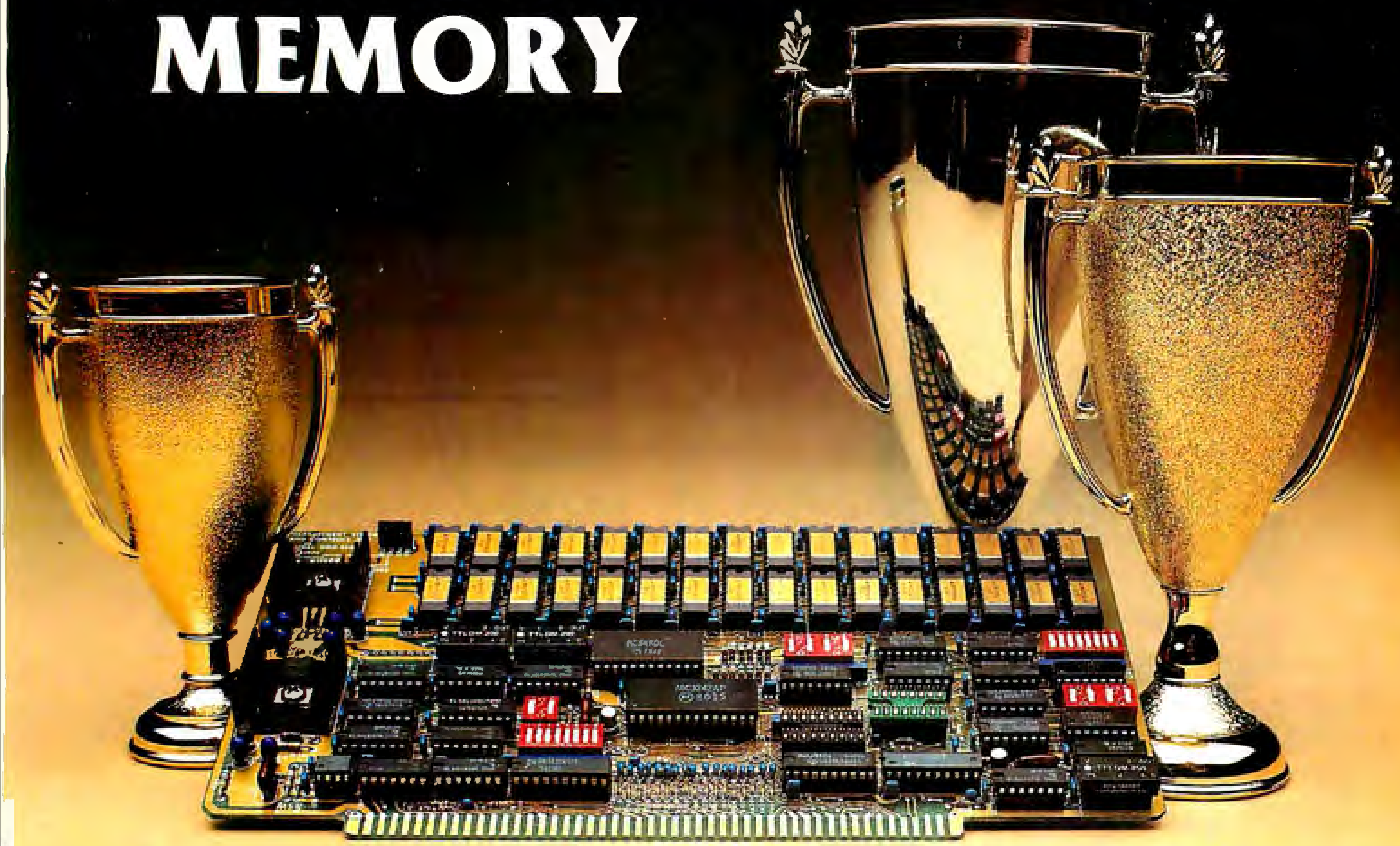

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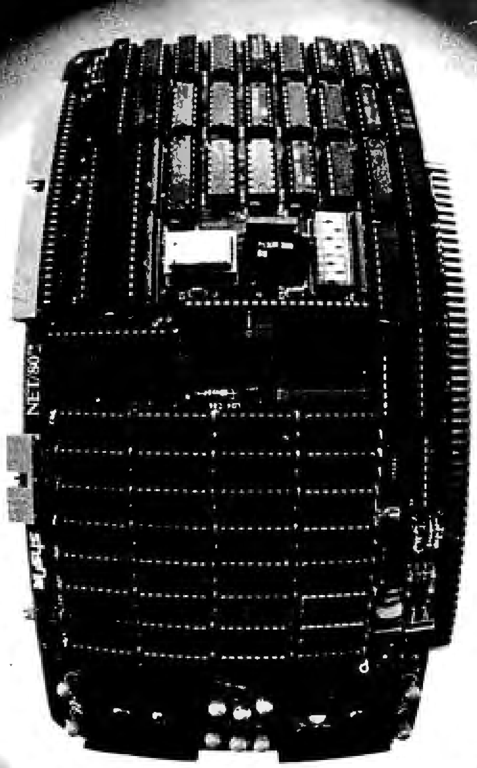

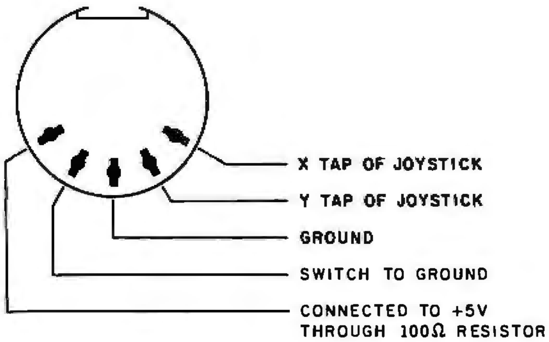

Figure 14: *Pin designations of the Color Computer joystick connectors. The connectors will mate with a standard 5-pin DIN plug, and any signal within the A/D converter's range may be monitored under program control.*

Expansion Port Pin Description

pin	function	pin	function
1	−12 V	2	+12 V
3	HALT	4	Nonmaskable Interrupt
5	RESET	6	E
7	Q	8	CB1 of IC4
9	+5 V	10	D0
11	D1	12	D2
13	D3	14	D4
15	D5	16	D6
17	D7	18	R/$\overline{W}$
19	A0	20	A1
21	A2	22	A3
23	A4	24	A5
25	A6	26	A7
27	A8	28	A9
29	A10	30	A11
31	A12	32	C000 thru FEFF
33	Ground	34	Ground
35	Analog In	36	FF40 thru FF5F, CS
37	A13	38	A14
39	A15	40	Decode Defeat

Table 8: *Signals available at the expansion port.*

cartridges. If you want them to auto-start like the Tandy cartridges, connect pins 7 and 8 together. This runs the Q clock into the CB1 input of PIA IC4, causing an FIRQ interrupt. The FIRQ interrupt-service routine jumps to hexadecimal C000 and starts execution. There is also a device select on pin 32 that is decoded from hexadecimal C000 to FEFF.

Summary

We have tried to completely describe the architecture of the Color Computer and deduce the reasoning behind the design trade-offs. Tandy certainly is to be complimented on the amount of "bang for the buck"—every part is fully used and several innovative design ideas are evident. We believe that the Color Computer has the capability to surpass the Model I in sales.

In a later article we will take a detailed look at the Extended BASIC and discuss its capabilities. We are currently implementing several popular video games in BASIC. Once the algorithms are proven, we plan to convert them to machine language to increase the speed, although with the power of the Extended BASIC we may not have to. ■

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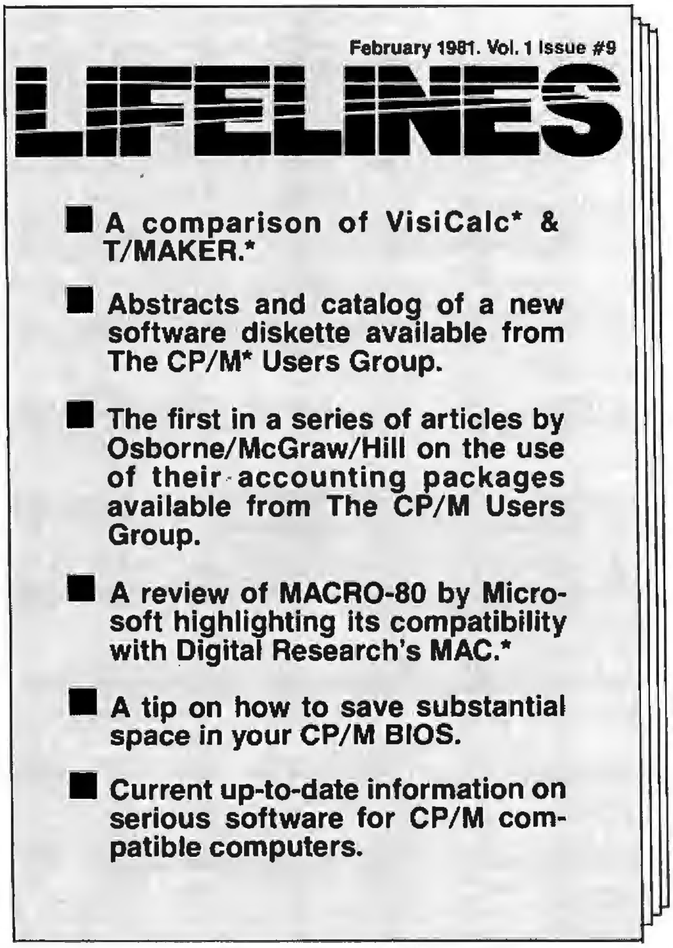

February 1981. Vol. 1 Issue #9

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What Is Good Documentation?

Jim Howard
150 Ramona Place
Camarillo CA 93010

As more and more people discover the joys of owning a microprocessor the need for good documentation will continue to grow. Information will be needed at all levels, from detailed hardware and software documentation to descriptions of which buttons to push to play your favorite game.

Who will provide this information? The simple answer is that those who know will tell those who don't know. It sounds simple, but it's not. Everywhere, complaints are made about documentation—"inadequate," "erroneous," "over my head," "bad or nonexistent," and so on. All too often, companies market excellent systems with poor or sketchy documentation, resulting in unhappy customers and unsatisfactory sales.

It's a common mistake to believe that because somebody is an expert in a subject, he can explain it to others. For example, it's assumed that a professor who knows a subject inside and out can pass on this information to students. However, whether he can or cannot depends on something else besides his knowledge of the subject. It depends on his ability to put himself in the place of the users, the students, to begin where *they* are, using their language and their knowledge level. (Of course, if there is a failure to communicate, it is the students who fail, not the professor!)

The microprocessor industry is a classic example of the communication problem. Aside from a few shining lights, microprocessor literature suffers from a bad case of "the jargons." The problem was not as serious while the technology was being pursued by only a few hobbyists, who like to work things out for themselves. Now that the public is becoming involved in large numbers, the information must adapt to the customer, not the other way around.

Aside from a few shining lights, microprocessor literature suffers from a bad case of "the jargons."

Many could undoubtedly do a better job of communicating if they followed a few principles. But doing this requires conscious dedication. And, of course, it requires principles. Those principles are what this article is about.

To translate the jargon of the expert into terms meaningful to the rest of the world, we need an *interpreter*. Such an interpreter is similar to the compiler or interpreter used in computers, which translates the source language into one the machine understands. In both cases, the source language is provided by the computer expert. The machine is the user in one case, the public in the other.

Information Design

The interpreter we require can best be referred to as *information design*. This term is better than the common term "technical writing," in that it indicates what really is required—conscious, step-by-step design. Writing is just one aspect of presenting understandable information. In fact, technical writing is similar to writing code for a computer program. If the planning and structure are sound, the writing almost takes care of itself.

There are many aspects of information design, not all of which can be

Information Design Principles

- **Content** *defines the* breadth *and* depth *of the material in a document, and is best specified by a* topic diagram. *Consistency and uniformity of treatment are revealed by such a diagram: One topic should not be treated in great detail and others of equal importance hardly mentioned. The breadth and depth should fit users' needs—all relevant material included, no unnecessary redundancies, and sufficient detail to allow users to understand the explanation or perform the job.*
- **Organization** *gives shape and direction. The users always know where they are, where they have been, and where they are going.* Indexes *and* headings *make the organization visible to users, so that information is located easily and quickly. Material is grouped and sequenced to flow logically and naturally from one topic to another. A* top-down *approach is used, to provide an overall structure before confusing users with details.* Introductions *and* summaries *tie pieces together both forward and backward, and reinforce for long-term memory.*
- **Format** *makes the information understandable through language and illustrations.* Language *speaks to one half of the brain—the verbal, linear side. Simple vocabulary and short, direct sentences make for ease of understanding.* Illustrations *speak to the other half of the brain—the nonverbal, spatial side. Illustrations are most effective when they are near the relevant text and are keyed to it through call-outs and highlights. Working together, words and illustrations present the whole "picture" as neither can alone.*

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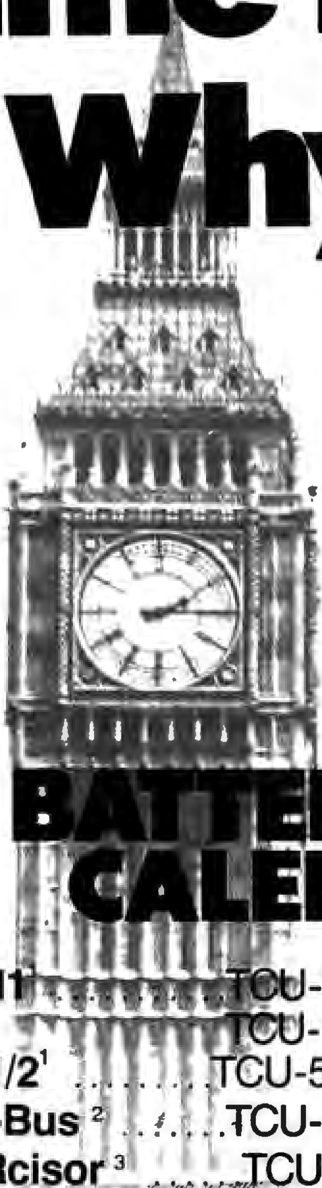

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covered here. What *is* necessary is that a few key principles are made clear.

The basic objective of information design is *usability*. Whatever the user intends to do—write a program, assemble a piece of hardware, learn how a system works—the documentation must serve this purpose.

Although this may sound trivial, if you're writing a technical document, it's surprising how easy it is to lose sight of this overall requirement after page 1. The presentation can become an ego trip without your realizing it. On the other hand, it's hard to go wrong if you consistently keep the usability objective in mind.

How do we determine if a document is usable? Whatever the type of document—operator's manual, maintenance procedure, reference manual, training program—it has some *purpose*. Its purpose may be to explain a concept, describe the operation of a piece of equipment, or guide a person through an assembly procedure.

To be usable, the document must take the users from a state of incomplete knowledge about some subject to a condition of more complete knowledge. If it's a procedure, the information must guide the users through the task. In any case, the document must take them from "here" to "there."

That's what information design does: It starts where the users are and builds step by step. The information designer first asks who the users are. Then he puts himself in their place and asks, "What will they understand, with their experience? What is their technical knowledge and vocabulary? How can they best be helped?"

Next, he builds step by step. He breaks up complicated subjects into simpler parts. He leads the users gradually into new territory, helping them make their own discoveries. With each step their confidence grows and they want to learn and do more. At the end, the users know they have succeeded—and, therefore, so has the information designer.

The Elements of Information Design

If we are going to start where the users are and build step by step, we need a plan of action. We need to decide:

- what information to include in the document
- how to organize it
- how to present it so it's understandable

We'll discuss these aspects under the headings of Content, Organization, and Format.

Content

The *content* of a document is the specific technical material contained in it. This should be carefully defined by boundary lines set down by the information designer.

Content really has two aspects: what information is included (*breadth*) and what is its level of detail (*depth*). A simple example will illustrate the important difference between breadth and depth: An operator's manual for a computer system might tell you to "remove and replace the printer's print wheel as necessary." The subject of print wheel replacement is thus "covered" in the manual; that is, in terms of breadth, it is part of the content. However, the lack of "how to" details may make this information of little use to many

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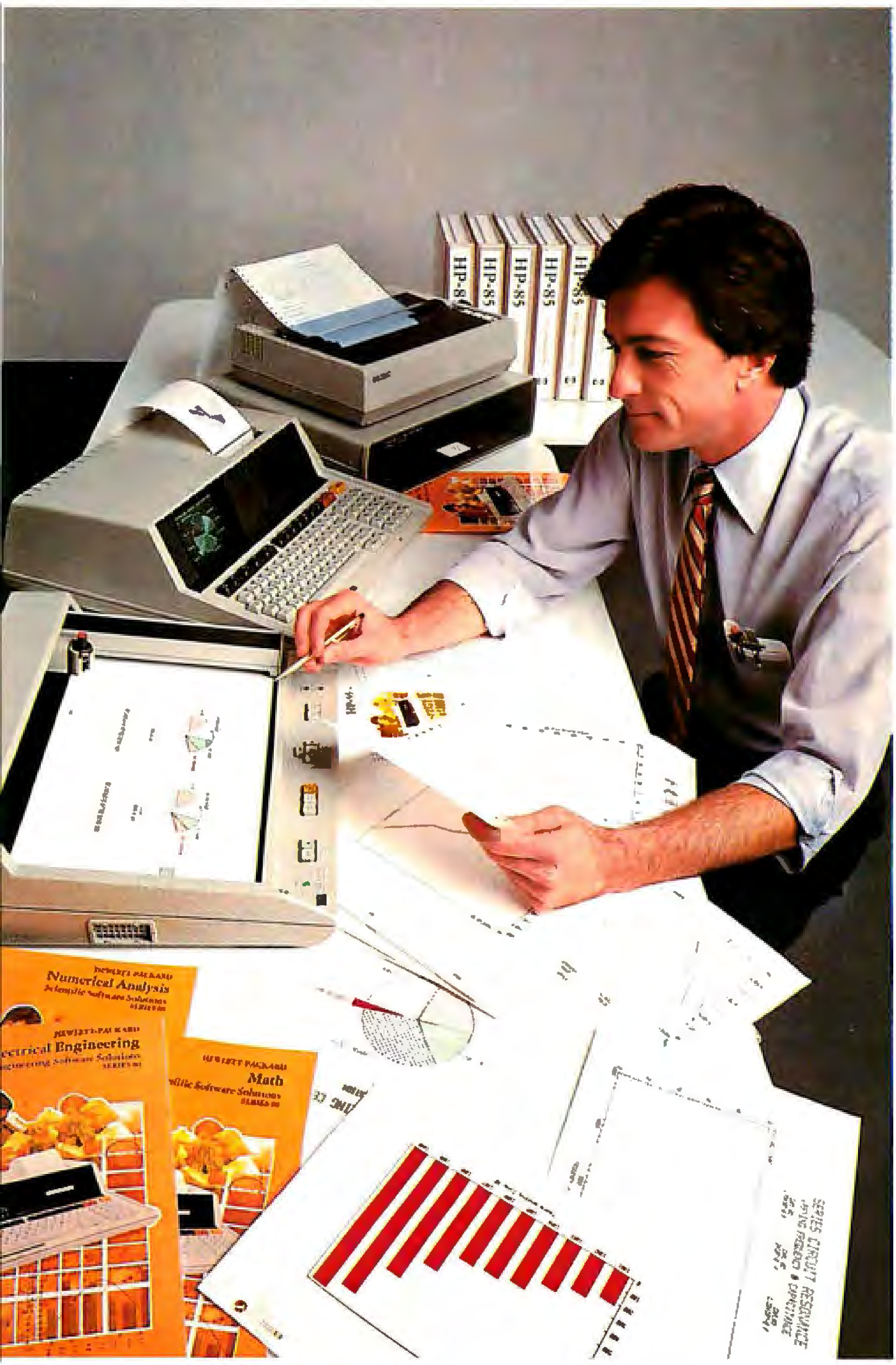

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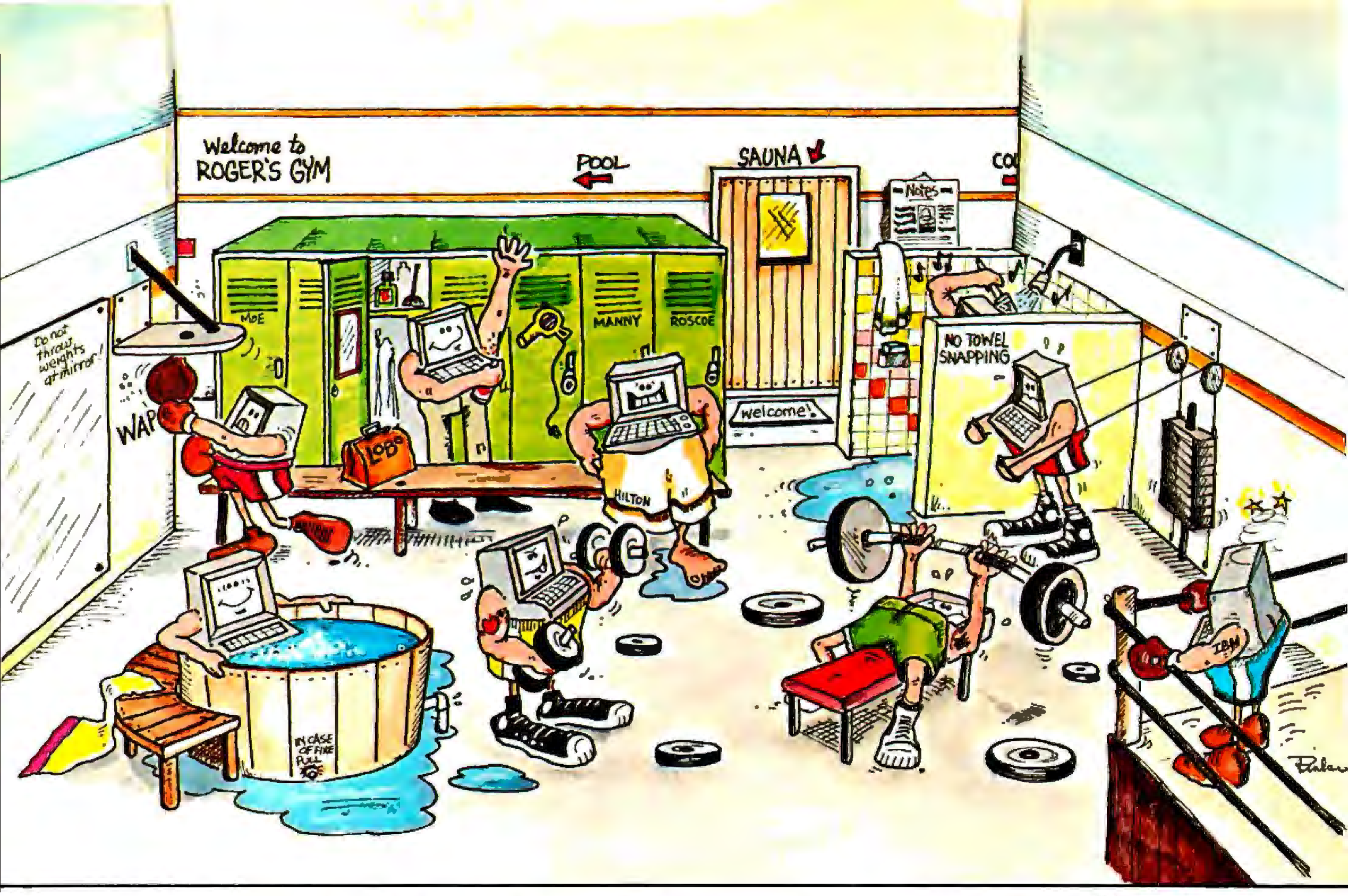

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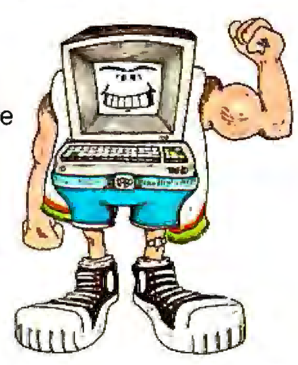

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printer users. Thus the proper *depth* of information is *not* part of the content.

A good tool to help a writer of documentation analyze breadth and depth is a *topic diagram* (figure 1), which is an arrangement of topics in boxes at different levels, with lines joining related topics. It serves a purpose similar to that of an outline, but provides an easier visual check on such elements as breadth, depth, and consistency of treatment.

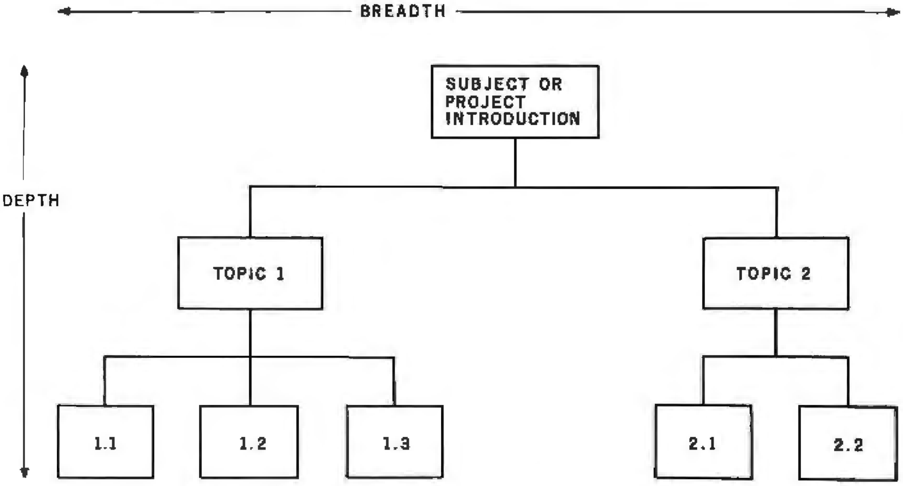


Figure 1: *A* topic diagram *is a useful tool for determining the* breadth, depth *and* consistency *of a piece of writing. Although similar in content to an outline, the topic diagram provides a clearer visual check on how topics are handled. As shown, topics 1 and 2 are major topics at the same level. Neither is a subtopic of the other and both will be treated equally when the writing is done. Subtopics represent breakdowns of each major topic. As additional topics and subtopics are added the diagram can extend downward and to the left and right.*

In figure 1, topics 1 and 2 are major topics at the same level in the diagram. They might be two major components of a system, or groups of software, or procedures. Neither is a subtopic of the other and they will be treated equally in the presentation.

Subtopics are shown under each major topic: 1.1, 1.2, 1.3 under topic 1, and 2.1 and 2.2 under topic 2. These represent breakdowns of each major topic. The diagram can continue on down to further depths of subdivision and can also be extended to the left and right as additional topics are added at a given level.

We can see that the breadth of the topic diagram, particularly at the major topic level, tends to indicate the breadth of content. The depth of the diagram indicates the depth of content. While this should not be considered an infallible guide, it is useful in preliminary planning.

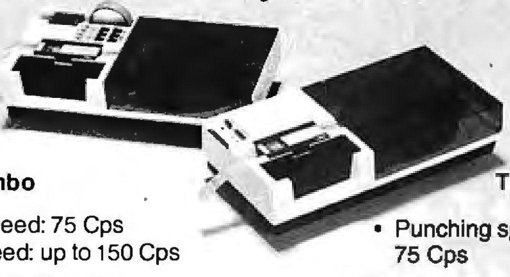
Another use of a topic diagram is that it gives an idea of *consistency* of coverage. A glance at figure 1 will tell the writer if topics at the same level are being treated with some consistency in how they are subdivided, or if one topic is being pursued to greater levels of detail than others. Without such a guide, it's easy to cover one topic in great detail and give other topics at the same level only token treatment or overlook them completely.

Definition of content is as important for what is *not* included as for what *is*. Many technical documents include irrelevant information. This can be particularly annoying in procedural documents, when users are trying to accomplish an exacting task. They want to get on with it, but are continually being interrupted with extraneous remarks that belong in some other part of the document or should be left out entirely.

Figure 2 shows a topic diagram for this article. As you can see, in addition to defining content, such a diagram shows a preliminary organization or structure.

Organization

To proceed step by step, we need to know where we are going and a route to get there. In other words, we need structure, or *organization*. Informa-



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tion must be grouped, sequenced, and related in order to be understood. Otherwise, it is merely a jumble of disordered facts or ideas—a "shopping list." If we had to learn everything by rote memory from shopping lists, we'd be in big trouble. Once a good structure is established, all kinds of details can be hung on it and they will be understood and remembered.

Organization is also what makes information in a document easily *accessible.* Accessibility depends on both the overall structure of the document and how this structure is made visible to the user through indexing and headings. If information is organized properly, the user will be able to turn quickly to the information he wants. Once there, he will be able to continue with a minimum of routing to other parts of the document.

The importance of structure or organization can be illustrated by a very simple example—a telephone book. Have you ever stopped to think how useless a telephone book would be if the names were listed randomly rather than alphabetically? The important aspects of structure or organization include indexing and headings, grouping and sequencing, routing, and introductions and reviews.

Indexing and Headings

Indexing and headings are the means by which the organization of the document is made easily visible to users. A writer may actually have a good organization, but if it is not clear to users, it will not really have served its purpose.

Indexing as used here includes both the standard type of index found at the end of a document and the table of contents. The index should be set up with the idea that users will sometimes look for items alphabetically, as in a dictionary. Many items that are too small or too specific to be included in the table of contents are made accessible with a good index.

Often a table of contents can be usefully constructed in two parts: an overall table in front and more detailed tables with each major section of the document. This avoids an unwieldy table up front. Figure 3 provides an example of a two-part table of contents. The main table (on the left in the figure) would appear in the front of the document. Each major section would start with its own table of contents (on the right in figure 3) showing the more detailed headings and subheadings in the section.

A consistent set of *headings* serves to make information accessible. Headings also help users remember

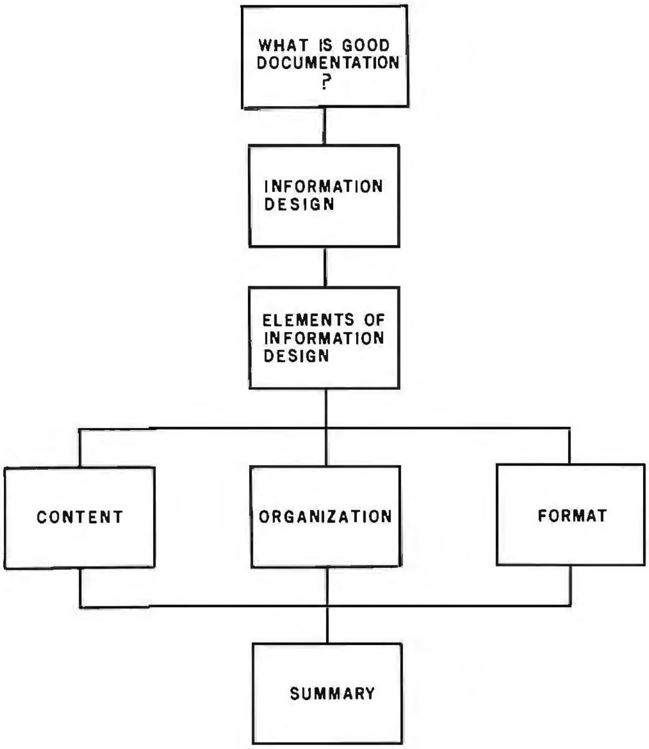

Figure 2: *A topic diagram written for this article.*

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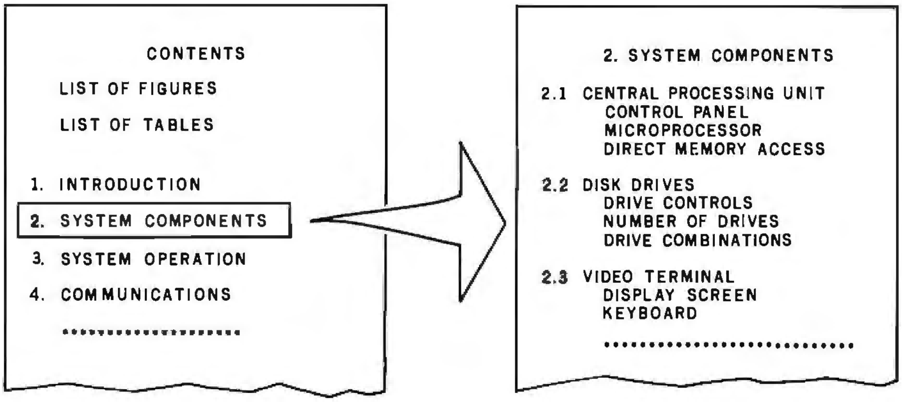
REQUEST & KRAM are trade marks of United Software of America where they are, which is just as important. Thus high-level headings should be repeated frequently, for example as a running head at the top of each page. Having the relevant headings always in front of the user makes the structure visible, and details are then assimilated more easily.

Grouping and Sequencing

The overall organization of the document is established by how the content material is grouped and sequenced. Again, the topic diagram is useful during the planning stages in making visible the planned organization of the document.

Whether the document is procedural or descriptive, grouping of the topics should be based on a logical pattern and the relevance of different items. For example, procedural tasks normally performed together (such as the various steps required to start up a computer system) should be grouped together. In a system description, the individual descriptions of system components would normally be grouped together, as in the example table of contents shown in figure 3.



CONTENTS
LIST OF FIGURES
LIST OF TABLES
1. INTRODUCTION
2. SYSTEM COMPONENTS
3. SYSTEM OPERATION
4. COMMUNICATIONS
....

2. SYSTEM COMPONENTS
2.1 CENTRAL PROCESSING UNIT
    CONTROL PANEL
    MICROPROCESSOR
    DIRECT MEMORY ACCESS
2.2 DISK DRIVES
    DRIVE CONTROLS
    NUMBER OF DRIVES
    DRIVE COMBINATIONS
2.3 VIDEO TERMINAL
    DISPLAY SCREEN
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....

Figure 3: *An example of a two-part table of contents. By using an overall table in the front of the document, and a more detailed table later, an initial unwieldy table is avoided where a user would be subjected to unwanted detail.*

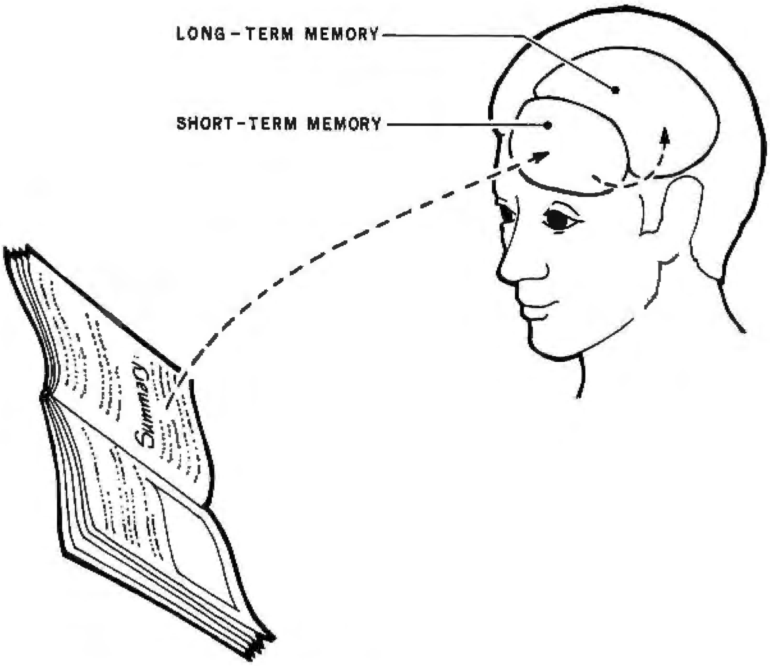

Figure 4: *Summaries and long-term memory. In the human brain, memory is divided into short-term memory and long-term memory. Although the capacity of long-term memory is large, all information must first pass through a short-term memory. When writing, the inclusion of summaries, reviews, and question-and-answer sections is an effective way of passing information into long-term memory.*

Sequencing is one of the most critical parts of the structure. The user is being led step by step from the known to the unknown, from the simple to the complex. Here the *top-down* structuring principle frequently used in writing computer programs also applies. The sequence should begin at the top and give the readers the big picture before engulfing them with details. It is not unusual to begin reading a document and find yourself up to your ears in technical details before you really know what's going on.

Most equipment operations and human activities have a natural or normal sequence that should be preserved in the documentation. For example, you normally gather together all the tools and supplies required for an activity before starting; therefore, this information should logically precede the activity description. It is disconcerting to have to stop in the middle of a task and run to the hardware store to buy some item.

Routing

Once you start using a document it is inconvenient to have to refer to other parts of the document, or to other documents. The more often you are routed, and the more pages you have to thumb through to get there, the less useful the document. On the other hand, if all information is repeated at each point of need, a bulky document can result. Obviously, judgment is required in weighing these trade-offs. For example, you wouldn't want to tell a user how to solder a particular type of joint every time it came up—you would set aside a special section for this purpose. However, if a safety precaution applies to a number of different tasks in the document, it is better to accept the redundancy and repeat the precaution.

Introductions and Reviews

A general rule is to prepare users for what is coming and to remind them of where they have been. Proceeding through a document, users may forget where they are, forget what has gone before—and decide they didn't really want to learn this anyway. Information should be

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designed to help users relate backward and forward and recognize and retain key points along the way.

Further, readers need introductory instructions to help them find and use information. For example, the numbering schemes for tasks or illustrations, the use of safety symbols, notes, cautions, and warnings, and the treatment of information about tools and supplies should be briefly explained. If these instructions are backed up by consistent information presentation (see **Format** section), users will quickly learn what to expect, no matter where they are in the document.

Simple reviews at key points reinforce information and help users retain it in memory. Human memory, to put it simply, consists of two parts, "short-term" and "long-term." Whereas capacity is very limited in STM (short-term memory), the capacity of LTM (long-term memory) is large indeed. The catch is that information can get to LTM only through STM. Summaries and reviews and question-and-answer sessions are effective ways of establishing information firmly in LTM. This important concept is illustrated in figure 4.

Format

Format usually has the rather narrow meaning of "physical layout of the page." Here the term is meant also to include the rules that govern text and illustrations—that is, how information is presented on a page.

The general rule is that language and illustrations should work together. Each is an effective way of presenting certain kinds of information, and relatively ineffective for other kinds. When combined properly, they form a powerful presentation technique.

People will readily admit that pictures can do things that words cannot and vice versa. And yet it is surprising how often we find ourselves reading words, words, words, when a visual or two would have helped the presentation considerably. Many ideas become clearer with an illustra-

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tion, and some kinds of information can hardly be communicated at all without one. If you want to tell someone what something looks like, show a diagram or a photograph.

It is known that the left and right sides of the brain are quite different. For most people, the left side is dominant and works mostly with linear, sequential logic (like a computer). It is also the verbal side and controls *language*.

The right side specializes in images, music, *pictures*—it deals in spatial and visual concepts, in contrast to the linear, verbal left brain. Schools, with their traditional emphasis on verbal skills, have tended to neglect the right side of the brain. People who are less adept with their left brain have suffered as a result. Einstein, for example, was a poor student in language, but had a great ability to visualize (see figure 5).

The ideal combination is words and pictures working together, each doing what it does best. In a procedure, for example, words can tell readers what to do and how to do it; pictures can tell them what it looks

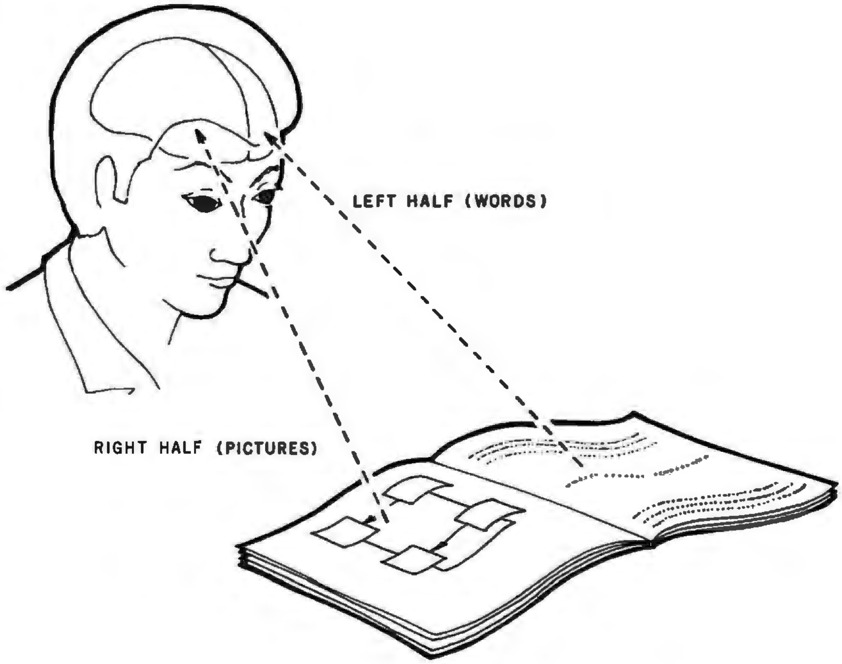

Figure 5: *The left and right sides of the human brain are very different. In most humans, the left side, which works mostly with linear and sequential logic, is dominant. The left side also controls verbal communications. The right side of the brain deals in spatial, visual, and more holistic concepts. One of the best ways of imparting information to the reader is through a combination of both words and pictures, thus enabling the reader to use both sides of the brain.*

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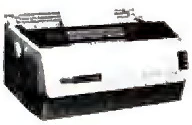

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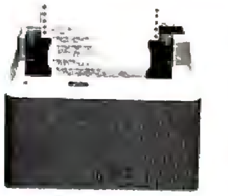

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like and where it is. For descriptive material, words and diagrams will do a good job of explaining and describing, *provided* they are working together. When you decide to use pictures to communicate with readers, follow the flow through step by step. Don't be content with offering an occasional "amazement diagram" and a "see figure so-and-so." You can perhaps wake up the right half of the reader's brain this way, but to get it working with the left half as a unit—whole-brain learning—make the words and pictures work together.

Here are some guidelines on how to do this, discussed under the following headings: keying text to illustrations, positioning text and illustrations, and limiting information density.

Keying Text to Illustrations

The mutual reinforcement of text and illustrations can be strengthened by keying the text to the illustration. This can be done by a liberal use of highlights and call-outs, which are "talked to" in the text.

For complicated diagrams, an indexing system can be used. An example of this common technique is shown in figure 6. Three parts of an electrical unit are designated A, B, and C in the picture on the right. These same letters are used in the text on the left to refer to these specific parts. This method can be used with fairly complex diagrams without confusing the reader. The alphabetical or numerical symbols take up little room on the diagram and can be ordered (for example, clockwise in figure 6) to make it easy to locate any symbol.

Highlights and call-outs help the user zero in on the main items of interest in a picture. A heavy outline or shading or color, together with a call-out of the item of interest, can make the text and illustration mutually support each other and help the user relate illustration to text.

Consistent, standard nomenclature should be used in linking text to illustration, and indeed throughout the document. Information becomes less accessible and less understandable if the same item is referred to by different names.

Positioning Text and Illustrations

Because the text and related pictures should work together, they should be positioned close together. Ideally, the user should be able to work back and forth between text and illustration without having to turn a page. While this ideal is sometimes impractical, it is usually possible to keep the illustration close to the relevant text. For important, frequently referenced figures, foldouts are sometimes the answer.

Limiting Information Density

Information is like food. If readers eat too fast, or too much at one time, they get indigestion. If information is presented too fast or in too large doses, readers will get confused. This is because of the limited capacity of short-term memory. Therefore, like food, information must be broken up into "bite-size" pieces to be digestible.

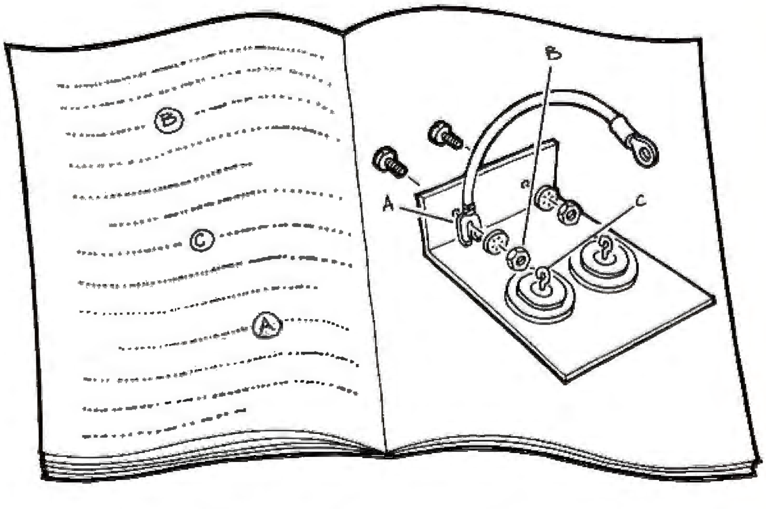

Figure 6: *Keying text to illustrations. The mutual reinforcement of text and illustrations (as shown in figure 5) can be strengthened by keying the text to the illustrations through the use of highlights and call-outs which are "talked to" in the text.*

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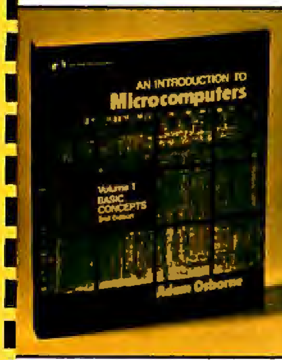

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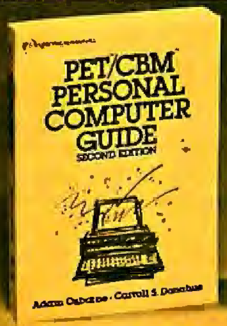

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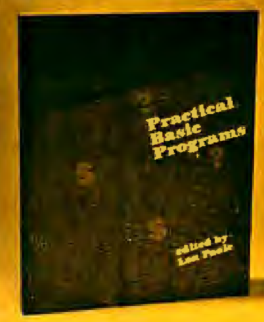

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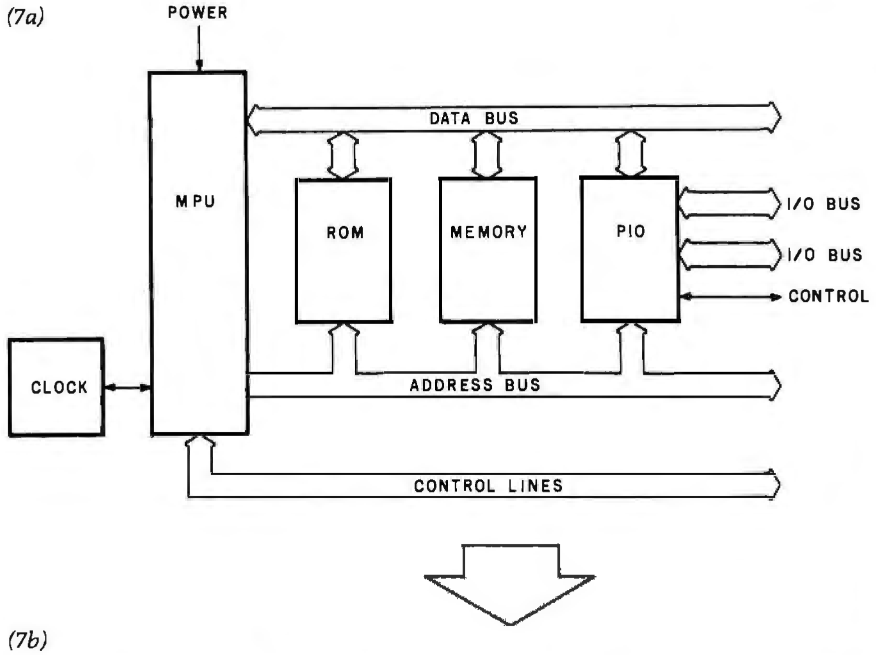
Good format does this.

Language should be simple and direct. Only words the reader understands should be used, with new words explained as they are introduced. Explanations are easier to read and understand if sentences are short and simple, and if words have few syllables.

Illustrations should not be cluttered with unnecessary information. If they are too "busy," pictures become confusing and are less useful. To avoid a profusion of details, illustrations can be used in a progression from simple to more complex. This is related to top-down sequencing. An initial overall figure can give the "big picture," which is easy to understand and serves as a beginning structure for proceeding to more detailed illustrations. In forming such progressions, it's important to preserve the relative locations of the parts of whatever is being pictured. For example, if a simple block diagram of a microprocessor leads off the series, subsequent more detailed diagrams and schematics should show the various parts of the blocks in the same relative positions as the original block. An example is shown in figure 7. Note that the lower detailed diagram preserves the relative positions, established by the upper figure, of the major parts of the system.

Earlier we said that microprocessor literature is suffering from a bad case of "the jargons." However, you'll see by now that there is much more to good documentation than avoiding jargon. You probably have had the experience of reading something and finding that it was very difficult to follow, even though you seemed to understand all the words. In this case, the author managed to avoid technical terminology but failed in other important areas. Good technical documentation requires a highly disciplined approach, and that approach is provided by information design. Those who adopt a go-as-you-please approach may score a success now and then, but it will be by accident. They have no way of knowing whether they have really reached their audience. In many cases they have not.■



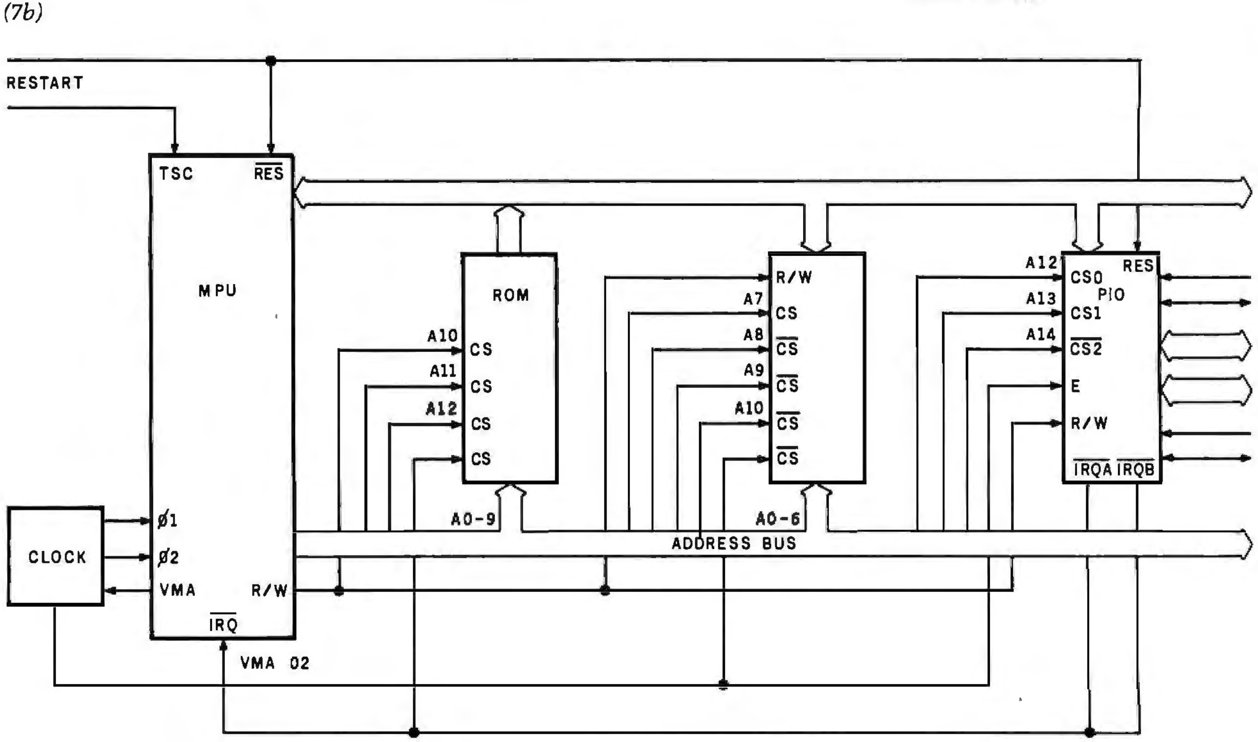


Figure 7: *To avoid reader confusion, illustrations should be used in a progression from less detail to more. An initial block diagram (7a) can give the overall picture before going into greater detail (7b). When forming these progressions, it's important to keep parts in the same relative positions.*

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MicroAge

Computing the Determinant of a Matrix

Brian Flynn, 1704 Drewlaine Dr, Vienna VA 22180

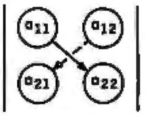
Matrix inversion is often used in solving sets of simultaneous equations and in performing multiple linear-regression analysis. But what determines whether or not a matrix can be inverted? The answer is its determinant does. More specifically, if the determinant of a matrix is 0, the matrix is singular and can't be inverted.

A Radio Shack Level II BASIC program for calculating the determinant of a matrix is presented here. The algorithm uses the upper-triangular technique and switches rows, when necessary, to insure that the determinant is always calculated, within the limits of the computing capability of the TRS-80 Model I.

A matrix is a rectangular array of numbers or variables (usually displayed in brackets). A square matrix is two-dimensional with as many rows as columns. A characteristic of a square matrix is its determinant. Determinants are defined only for square matrices, just as only square matrices are invertible. Unlike a matrix, a determinant is written as an unbracketed, single number—a lone, lorn creature such as 5, 0.03, or −1. The symbol for a determinant is sometimes *det*, but more often two parallel vertical lines: | |. (This latter symbol is also used for absolute value. The circumstance in which | | appears determines whether it means absolute value or determinant.)

It's relatively easy to calculate a second-order determinant, that is, the determinant of a second-order (2 by 2) matrix: tally the product of the principal diagonal elements and subtract from this the product of the off diagonal elements. The principal diagonal is the imaginary line segment running from the "northwest" corner to the "southeast" corner of the matrix. The off diagonal, on the other hand, is the one which connects the "northeast" and "southwest" corners. The process of calculating a second-order determinant is illustrated in table 1.

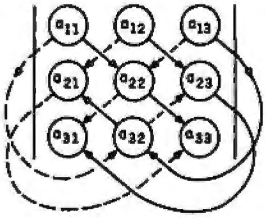
Tallying a third-order (3 by 3) determinant is a bit more difficult than tallying one of the second order. If the elements of the matrix are not too unwieldy, however, the calculation can still be made by hand without much trouble. This is shown in table 2. But for matrices of order four and higher, the business of determining the



$$= a_{11}a_{22} - a_{12}a_{21}$$

$$\begin{vmatrix} 2 & 5 \\ 3 & 9 \end{vmatrix} = 2 \cdot 9 - 5 \cdot 3 = 18 - 15 = 3$$

Table 1: *The general method for evaluating a 2 by 2 matrix and an example. The elements of the principal or major diagonal are multiplied ($a_{11}a_{22}$), as are the elements of the off or minor diagonal ($a_{12}a_{21}$). Then the product of the off diagonal is subtracted from the product of the principal diagonal.*



$$= a_{11}a_{22}a_{33} + a_{12}a_{23}a_{31} + a_{13}a_{32}a_{21} - a_{11}a_{32}a_{23} - a_{12}a_{21}a_{33} - a_{13}a_{22}a_{31}$$

$$\begin{vmatrix} 5 & 2 & 4 \\ 1 & 3 & 7 \\ 6 & 8 & 9 \end{vmatrix} = 5 \cdot 3 \cdot 9 + 2 \cdot 7 \cdot 6 + 4 \cdot 8 \cdot 1 - 5 \cdot 8 \cdot 7 - 2 \cdot 1 \cdot 9 - 4 \cdot 3 \cdot 6$$

$$= -119$$

Table 2: *The method for evaluating a third-order determinant is an extension of the method used for second-order determinants. Note that plus signs are associated with the three products formed by solid lines, and minus signs are associated with the three products formed by dashed lines.*

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^{TM}CPM is a trademark of Digital Research determinant can get really complicated. Indeed, calculating a fourth-order determinant one time by hand, using the popular Laplace expansion, is usually sufficient to elicit the plea, "Isn't there an easier way?"

Fortunately, there is. The upper-triangular method is a straightforward, computer-compatible technique for tallying a determinant of any order. The process, illustrated in table 3, is in two steps:

- Transform the matrix so all of the elements below the principal diagonal are 0s, using elementary row operations. Anticipate division by 0, and switch rows of the matrix to avoid it.
- Calculate the product of all elements along the transformed principal diagonal. This product is the determinant.

If you ever determine to determine the determinant of a matrix, I hope you find the upper-triangular method useful. ■

$$\begin{vmatrix} 4 & 2 & 3 \\ 8 & 4 & 1 \\ 2 & 9 & 6 \end{vmatrix}$$

STEP 1. TRANSFORM THE ELEMENTS OF THE LOWER TRIANGLE INTO 0s: TRANSFORM THE 8 INTO 0 BY MULTIPLYING THE ELEMENTS OF ROW #1 BY -2 THEN ADDING THEM TO THE CORRESPONDING ELEMENTS OF ROW #2.

$$= \begin{vmatrix} 4 & 2 & 3 \\ 0 & 0 & -5 \\ \textcircled{2} & 9 & 6 \end{vmatrix}$$

TRANSFORM THE CIRCLED 2 INTO 0 BY ADDING -1/2 TIMES ROW #1 TO ROW #3.

$$= \begin{vmatrix} 4 & 2 & 3 \\ 0 & 0 & -5 \\ 0 & 8 & 4.5 \end{vmatrix}$$

TRANSFORM THE 8 INTO 0. IF THE ABOVE PATTERN WERE FOLLOWED, -8/0 TIMES ROW #2 WOULD BE ADDED TO ROW #3. TO AVOID DIVISION BY 0, SWITCH ROWS 2 AND 3. THIS CHANGES THE ARITHMETIC SIGN OF THE DETERMINANT (LINE 4060 OF THE PROGRAM).

$$= - \begin{vmatrix} 4 & 2 & 3 \\ 0 & 8 & 4.5 \\ 0 & 0 & -5 \end{vmatrix}$$

STEP 1 IS NOW FINISHED SINCE THE ELEMENTS OF THE LOWER TRIANGLE ARE ALL 0s.

STEP 2. TALLY THE PRODUCT OF ALL ELEMENTS ALONG THE PRINCIPAL DIAGONAL.

$$\text{DETERMINANT} = -[4 \cdot 8 \cdot (-5)] = 160$$

Table 3: *The upper-triangular method for evaluating higher-order determinants consists of two steps: first, transform the elements of the lower triangle into 0s, then find the product of the principal diagonal.*

Listing 1: *The program for determining the determinant of a matrix.*

```
  10  REM CALCULATING THE DETERMINANT OF A
      MATRIX
  20  REM UPPER TRIANGULAR METHOD
  30  REM BRIAN J. FLYNN; FALL 1980
  40  REM MOD 1: INITIALIZE & ENTER DATA
  50  GOSUB 1000
  60  REM MOD 2: CALCULATE DETERMINANT
  70  GOSUB 2000
  80  REM MOD 3: PRINT DETERMINANT
  90  GOSUB 3000
 100  GOTO 9999
1000  REM MODULE 1
1010  REM VARIABLES
1020      REM    C = USED IN TRANSFORMING
          MATRIX
1030      REM   DT = DETERMINANT
1040      REM HOLD = USED IN SWITCHING ROWS
1050      REM    K = ORDER OF THE MATRIX
1060      REM SIGN = +1 OR -1
1070      REM    X = MATRIX
1080  REM INITIALIZE
1090      DEFDBL C,D,H,X:SIGN=1:DT=1:CLS
1100      PRINT "THIS PROGRAM COMPUTES THE
          DETERMINANT OF A MATRIX."
1110      PRINT:INPUT "HOW MANY ROWS (COLUMNS)
          ARE IN YOUR MATRIX";K
1120      DIM X(K,K)
1130  REM ENTER DATA
1140      FOR I=1 TO K
1150      CLS:PRINT "PLEASE ENTER DATA."
1160      PRINT"ROW #";I;":"
1170      FOR J=1 TO K
1180      PRINT"COL #";J:INPUT X(I,J)
1190      NEXT J,I
1200  RETURN
2000  REM MODULE 2
2010  REM CHECK FOR 1ST-ORDER DETERMINANT
2020      IF K=1 THEN DT=X(1,1):GOTO 2180
2030  REM FILL LOWER TRIANGLE WITH 0 s
2040      FOR L=1 TO K-1
2050      FOR I=L TO K-1
2060      REM AVOID DIVISION BY 0
2070      IF X(L,L)=0 THEN GOSUB 4000
2080      IF DT=0 THEN 2180
2090      C=X(I+1,L)/X(L,L)
2100      FOR J=1 TO K
2110      X(I+1,J)=X(I+1,J)-X(L,J)*C
2120      NEXT J,I,L
2130  REM TALLY PRODUCT OF PRINCIPAL DIAGONAL
      ELEMENTS
2140      FOR I=1 TO K
2150      DT=DT*X(I, I)
2160      NEXT I
2170      DT=DT*SIGN
2180  RETURN
3000  REM MODULE 3
3010      PRINT"DETERMINANT = ";DT
3020  RETURN
4000  REM SUBROUTINE: SWITCH ROWS
4010      FOR M=L+1 TO K
4020      IF X(M,L)=0 THEN 4070
4030      FOR Q=1 TO K
4040      HOLD=X(L,Q):X(L,Q)=X(M,Q):X(M,Q)=HOLD
4050      NEXT Q
4060      SIGN = -SIGN:GOTO 4100
4070      NEXT M
4080      REM DETERMINANT = 0
4090      DT=0
4100  RETURN
9999  END
```

Languages Forum

A Coding Sheet for FORTH

John O Bumgarner, 17370 Hawkins La
Morgan Hill CA 95037

FORTH is a new programming language to most people, and, while it has many advantages over other languages, it does have an unconventional appearance. FORTH is not an intrinsically difficult language, but the unfamiliar appearance, the use of a last-in-first-out stack for parameter passing, and a unique approach to problem solving require you to reorient your thinking a bit.

When I was learning FORTH, I often used to stop and sketch the appearance of the parameter stack as I defined a "word" (portion of a program) to help me get everything in place at the right time. It helped me, the novice FORTH programmer, to have a graphic representation of what the parameter stack looked like at each step. Later, I needed to document programs, so I expanded my sketchy method and made a proper FORTH-style coding sheet that provided the graphic parameter-stack representation.

The need for documentation never seems to go away, so I still use the coding sheet regularly.

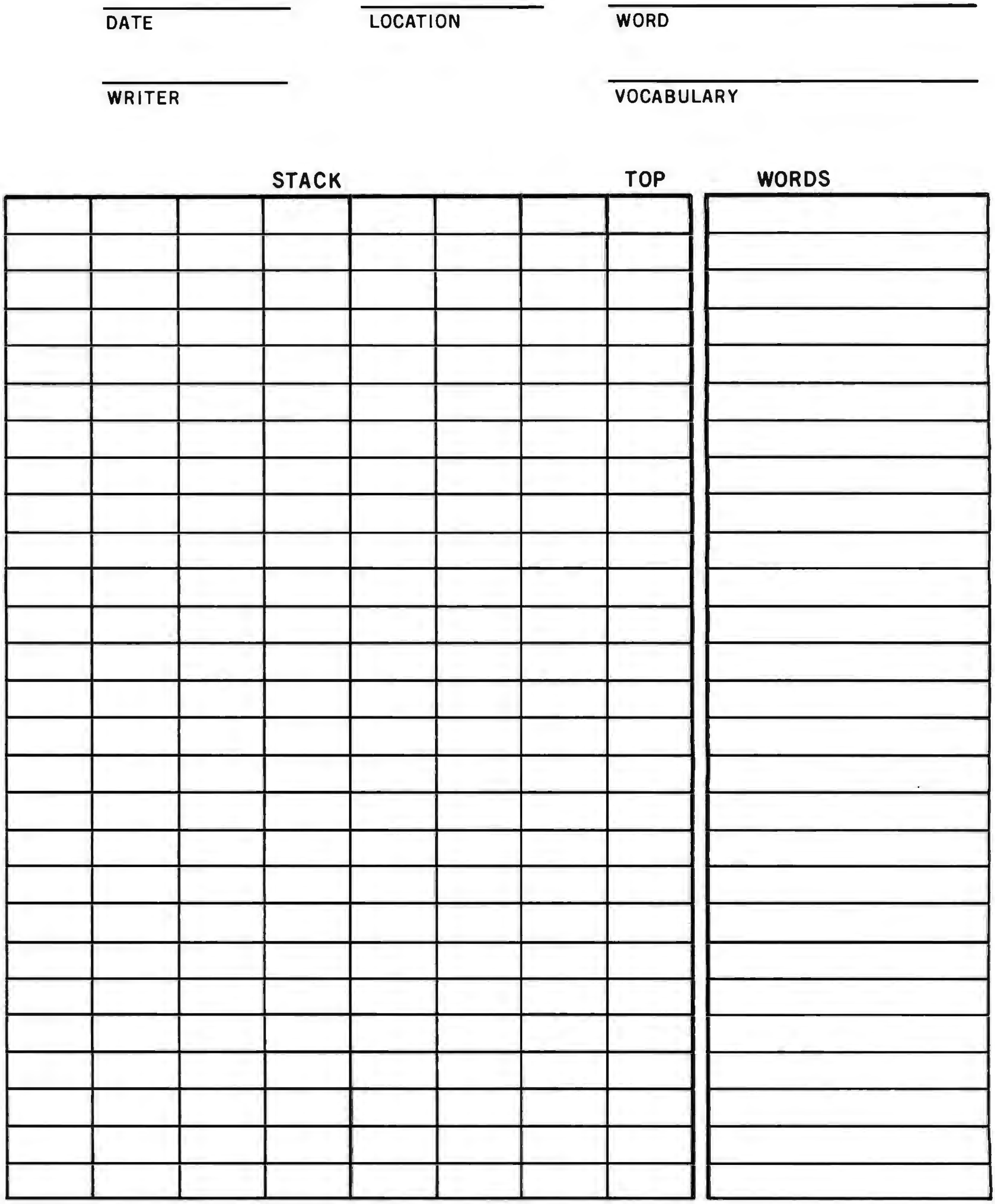
Now, while I rarely need help visualizing the stack, the need for documentation never seems to go away, and so I still use the coding sheet regularly. It has occurred to me that other FORTH programmers, new or otherwise, would find it useful too.

The coding sheet is shown full-sized in figure 1 and is meant to be copied for use by the reader. The form is deliberately simple to make it as flexible as possible. I have tried to strike a balance between the size of the spaces for words, the size of the spaces for stack items, and the number of stack items.

In actual practice, eight stack items on the form are sufficient because most FORTH words do not manipulate the stack outside of the range of the normal stack operators (which work from three to six words deep). In fact, a rule of thumb for good FORTH programming dictates that, if you get in a situation with the parameter stack that cannot be handled by normal stack operators, you are doing something wrong. You should stop and examine your methods to see how you can avoid the problem. In my experience, this is true; a better way results from a little thought, and it usually is simpler, to boot!

The space for words used in the definition is left a bit wide, as it is common to put short phrases on one line. This not only saves space but also allows frequently used short phrases such as fetching from or storing to a

Text continued on page 162



DATE

LOCATION

WORD

WRITER

VOCABULARY

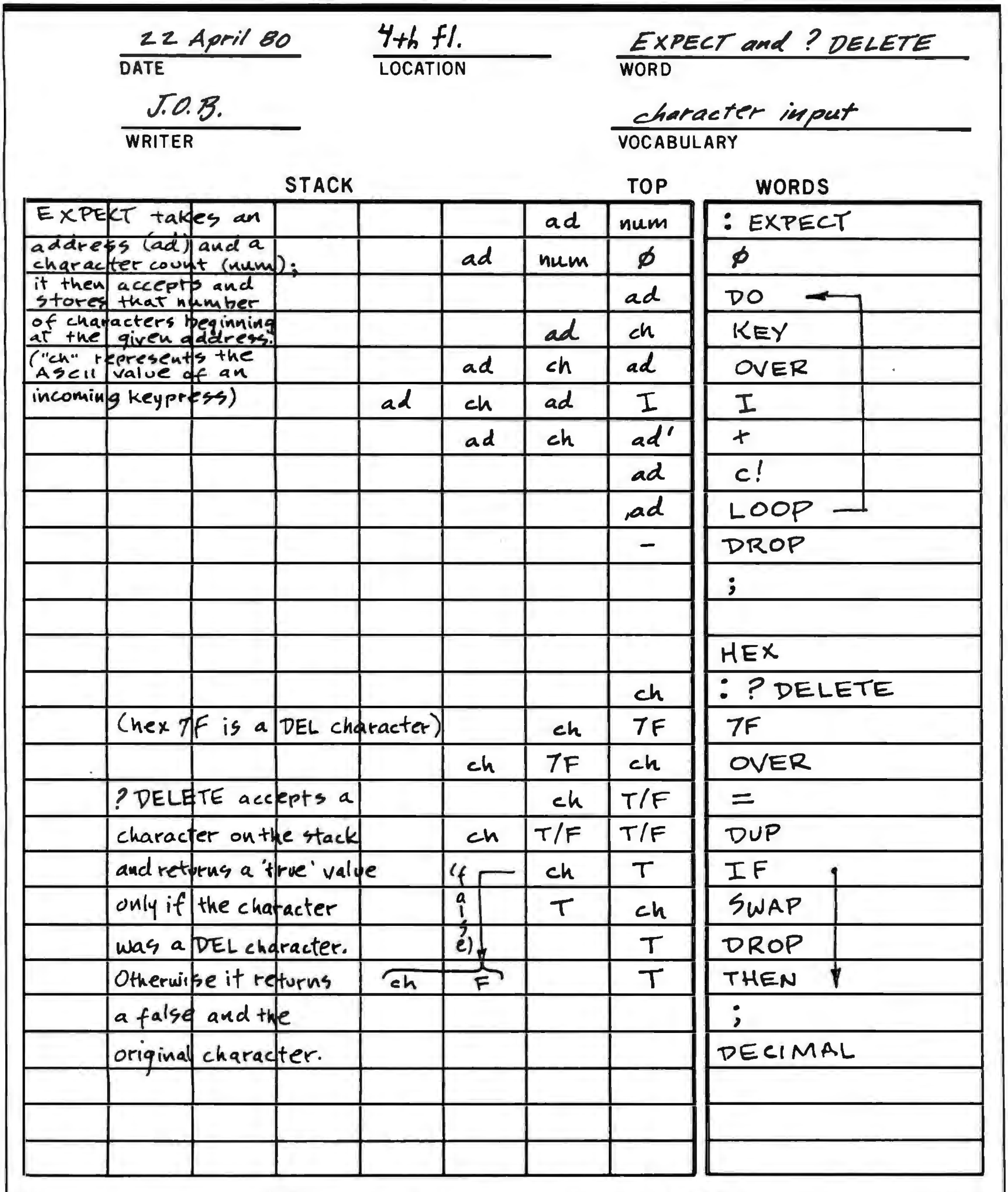
STACK

TOP

WORDS

J.O.B.80

Figure 1: *A coding sheet for FORTH used to show the effect of words in a FORTH definition on the parameter stack.*



22 April 80
DATE

4th fl.
LOCATION

EXPECT and ?DELETE
WORD

J.O.B.
WRITER

character input
VOCABULARY

STACK							TOP	WORDS
EXPECT takes an						ad	num	: EXPECT
address (ad) and a character count (num);					ad	num	0	0
it then accepts and stores that number							ad	DO
of characters beginning at the given address.						ad	ch	KEY
("ch" represents the ASCII value of an					ad	ch	ad	OVER
incoming keypress)				ad	ch	ad	I	I
					ad	ch	ad'	+
							ad	c!
							ad	LOOP
							–	DROP
								;
								HEX
							ch	: ?DELETE
	(hex 7F is a DEL character)					ch	7F	7F
					ch	7F	ch	OVER
	?DELETE accepts a					ch	T/F	=
	character on the stack				ch	T/F	T/F	DUP
	and returns a 'true' value				(f	ch	T	IF
	only if the character				als	T	ch	SWAP
	was a DEL character.				e)		T	DROP
	Otherwise it returns			ch	F		T	THEN
	a false and the							;
	original character.							DECIMAL

Table 1: *An example using the FORTH coding sheet. In this example and that of table 2, FORTH words or phrases are listed in the rightmost column, reading from top to bottom. The stack area on the same line represents zero or more parameters on the parameter stack after the word or phrase has been executed; the rightmost entry in the stack area is always the top-of-stack, with entries below it on the stack listed to the left. A dash represents an empty stack. "T/F" represents a flag of either true (nonzero value) or false (zero value) pushed to top-of-stack as the result of some comparison operation. Arrows represent the flow of control due to either a loop construct or the outcome of an IF construct. Note that, in the definition of { ?DELETE }, the stack exits the definition with two values on the stack if the comparison made evaluates as false, but only one value if the comparison is true. See listing 1 for details.*

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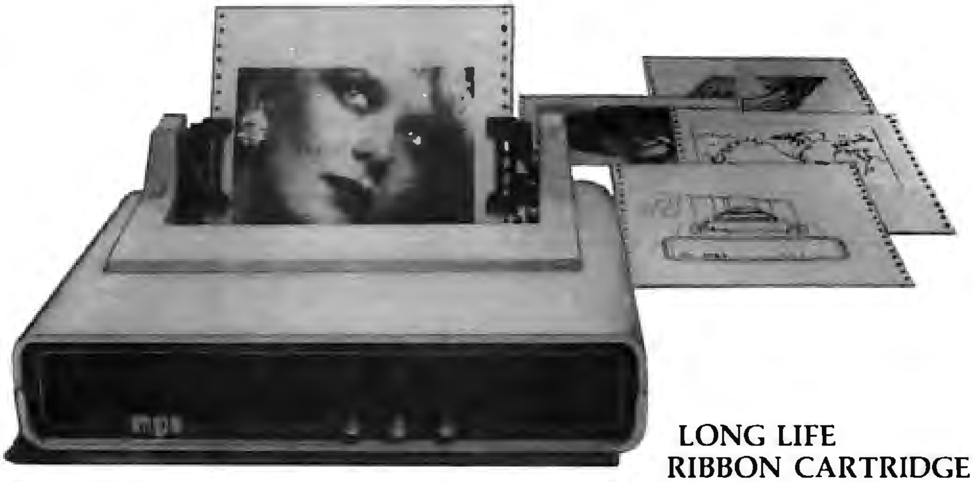

QUALITY

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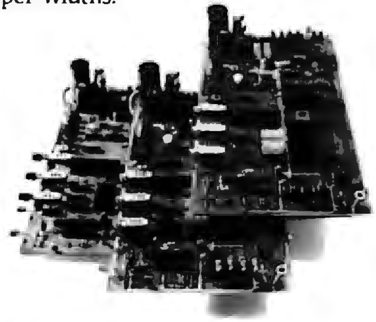

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VERSATILITY

The 88G prints a full upper and lower case 96 character ASCII set with a crisp, clear 7x7 matrix in 80, 96, or 132 column formats. For text processing and correspondence applications, an 11x7, 80 column serif style matrix can be selected by switch or software command. The dual tractor/pressure-feed paper drive system allows the user to choose either pin-feed, roll, or single sheet papers up to 9.5 inches wide.

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23 APR. 80
DATE

4th fl.
LOCATION

COUNTER
WORD

J. O. B.
WRITER

DATA - INPUT
VOCABULARY

STACK							TOP	WORDS
			setup	an accumulator			–	0 VARIABLE NEGATIVE
			setup	another one			–	0 VARIABLE NON-NEG
			the name of this routine				–	: COUNTER
							0	0
			clear the			0	$addr_1$	NEGATIVE
			accumulators				–	!
							0	0
						0	$addr_2$	NON-NEG
							–	!
							–	BEGIN
FETCH pushes a number (num) to top-of-stack							num	FETCH
						num	num	DUP
					num	num	0	0
true	if num < 0					num	T/F	<
							num	IF FALSE
						num	1	1
		true	part		num	1	$addr_1$	NEGATIVE
							num	+!
							num	ELSE
						num	1	1
		false	part		num	1	$addr_2$	NON-NEG
							num	+!
							num	THEN
test	for end condition (num=0)						T/F	0=
loop	until	true					–	UNTIL
								;

Table 2: *Another example using the FORTH coding sheet. See listing 1 for details.*

Solution \sō-ˈlü-shŭn\ n[ME,fr.MF,fr.L solution-] 1a: An answer to a problem.

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---

[1] Reg.TM, Digital Research

Listing 1: *A block of FORTH code. The FORTH words EXPECT , { ?DELETE } , and COUNTER are explained on the coding sheets in tables 1 and 2.*

```
( Character and data input words)

( EXPECT accepts n ch's putting them at given address)
( Use:    address  n  EXPECT  )
: EXPECT       0 DO    KEY  OVER    I  +  C!    LOOP    DROP  ;
HEX        ( change base to HEX for the following word)
( ?DELETE returns only T if given ch. is a DEL  )
( otherwise it returns the given ch. and a F on the top)
: ?DELETE        7F  OVER  =  DUP    IF  SWAP  DROP    THEN  ;
DECIMAL
0  VARIABLE  NEGATIVE       0  VARIABLE  NON-NEG
( COUNTER counts the number of negative and non-negative)
(       numbers and exits if given a zero. FETCH supplies #'s)
: COUNTER       0  NEGATIVE  !    0  NON-NEG  !       BEGIN
     FETCH  DUP  0  <     IF  1  NEGATIVE  +!    ELSE  1  NON-NEG   +!
     THEN  0=  UNTIL  ;
```

Text continued from page 155:

variable to read better. Such condensed definitions are also useful to keep as documentation. (See table 2.)

[*Editor's note: I have used John's sheet and found it very helpful in the design and documentation of FORTH words. I like to indent my entries in the "WORDS" column to show* if...then...else *constructs and loops. I have also been working with a similar diagram that allows a line to run across the long dimension on a page; this gives me more room for indenting FORTH words and documenting what they do....*GW]

Listing 1 is an example of a typical FORTH block of code. If it were part of a bigger listing, there would be three such blocks on one page and the page would be called a *triad*. If you wanted to see this block or edit it at your terminal, you would type { 123 LIST }. [*The braces are not part of the FORTH phrase, but are the standard BYTE delimiters that isolate FORTH words that include punctuation and FORTH phrases from the surrounding text....*GW]

The FORTH coding sheets show the detailed structure of each of the three words defined in block 123. The coding sheets in tables 1 and 2 show the words in great detail.

I hope that this coding sheet is of use to fellow FORTH enthusiasts. It certainly helped me learn FORTH, and allows me to produce clear documentation. ■

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Technological advances have added video and game terminals, and robots, to the ranks of terminal devices. Other areas of interest are the telecommunications networks for voice and data plus long-distance private networks, local area networks, instrumentation, and data bases. Terminals can be electrically, acoustically, or optically connected to these networks.

The first sessions sponsored by the Terminals Committee will be held at the 1981 International Communications Conference this June. Papers will be read on recent advances in terminals and the impact of communications systems on terminals. Topics being considered for the 1981 and 1982 workshops include office-automation terminals, graphics communications, plus speech-processing and game terminals. For more information, contact Fritz Froehlich, Bell Laboratories, Rm 1D622, Holmdel NJ 07733, (201) 949-4990.

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A Beginner's Guide to Spectral Analysis, Part 2

Mark Zimmermann
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In Part 1 of this article, I introduced some of the ideas behind the Fourier transform in one dimension. Here, I will try to extend those ideas to two-dimensional space. I will introduce a few of the many uses of two-dimensional spectral analysis, with particular emphasis on image processing. The main computer program that accompanies this article (see listing 1) is a 6502 assembly-language program that performs a two-dimensional transformation on a 25- by 40-pixel image. The program is specifically adapted to run on the Commodore PET microcomputer with 8 K bytes of programmable memory, but it should be a reasonably straightforward process to modify the code to work on other comparable machines. Several floating-point arithmetic routines are used from the PET's BASIC ROM (read-only memory); a table is included that describes what each routine does, so that it may be replaced by your own arithmetical procedures if necessary.

Components of Waves

As you will recall, the whole notion of Fourier, or spectral, analysis is to take a signal that is, for example, a function of time, and resolve it into its *components* (ie: the various frequencies that make up the whole). A chord played on a piano may produce a sound that is very complicated when plotted on an oscilloscope screen, but when the chord is Fourier analyzed, the individual notes (component frequencies) stand out.

It is mathematically possible to express any reasonable function as a sum of sines and cosines of various frequencies. The mathematical recipe for finding how much of each sine and cosine went into making the original signal is a fairly simple process that is discussed in many books (see references on page 198). Instead of going into the math here, however, I'd rather discuss the "feel" of Fourier transforming, with the objective of helping you develop some instincts about what a transform should look like and what it means.

Any reasonable function may be expressed as a sum of sines and cosines of various frequencies.

Figure 1 on page 168 shows several pairs of graphs. In each pair, the graph on the left represents a function of time. It could be showing, for instance, the difference between normal atmospheric pressure and the instantaneous pressure in a passing sound wave.

The graph on the right shows the Fourier transform (a function of frequency) of the graph on the left. It plots the amount of the components needed *at each frequency* to make the left-hand graph. The amount of sine wave is shown as a dashed line; the amount of cosine wave is a solid line. The horizontal axis runs from zero frequency (where it's intercepted by the vertical axis) to high frequencies. If the amount graphed on the right goes negative, it simply means that the original signal needs to have some amount of the function −sine or −cosine added to it. In other words, the original signal contained some sine waves that were 180° out-of-phase with the standard sine wave (so there's nothing special or mysterious about having a negative amount of a given frequency component).

What kind of insights can you get by examining the graphs in figure 1? First, it's clear that any function of time which is symmetric with respect to the $t=0$ (*vertical*) axis is made up only of cosine waves, and any function that is asymmetric with respect to $t=0$ is made of only sines. Every cosine wave is symmetric about the origin of time, so a sum of cosines should certainly be symmetric; every sine wave is asymmetric. A function that is neither perfectly symmetric nor perfectly asymmetric requires both sines and cosines in its constituent frequencies.

A second fact which becomes apparent from a study of figure 1 is that functions of time which have some *net area* (area between the curve and the horizontal axis) always have some amount of component with zero frequency plotted in their transforms. A zero-frequency wave doesn't wave at all; it's a constant number as time goes by, like cosine(0). Contrariwise,

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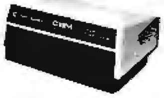

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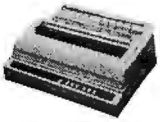

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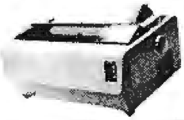

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if a function of time has no net area, if it is positive just as much as it is negative, then its Fourier transform has no zero-frequency component. This component, in fact, is just the average value of that signal.

Let's examine several specific pairs of graphs. The transform of a square pulse (figure 1a) contains a number of low-frequency cosines (to build up the area under the pulse and create the flat-topped sections which obviously change little with time), but in addition, a fair amount of high-frequency cosine energy is required to make the square pulse. A triangular pulse of the same area has similar low-frequency requirements, but needs fewer higher-frequency waves (see figure 1b). A Gaussian (bell-shaped) curve requires very little high-frequency contribution to make its smooth function of time (see figure 1c).

This correlation between "abruptness" and high frequencies in the Fourier transform is, in fact, quite general. Functions that change abruptly with time, like the square wave, or that have a lot of fine detail (the sharp edges), are not composed only of low-frequency, slowly changing waves; the jumps require a lot of high frequencies to define them. As a square wave becomes narrower and narrower, more and more high frequencies are necessary: a falling body's thud, if replayed at a high enough speed, can sound like an abrupt gunshot. Signals that don't have sudden jumps, like those represented in the triangular graph, can be made using fewer high-frequency components, but the sharp corners where the slope of the triangle's sides changes still require high-frequency sinusoids. Smooth curves like the Gaussian, where there isn't much detail, require the least amount of high frequencies.

Finally, look at the graphs in figures 1e thru 1h. The functions of time (on the left) all show some sort of *periodic* behavior. Their transforms all reveal this by a peak at or near the frequency of oscillation. The more cycles of oscillation that the temporal function goes through, the sharper the peak in *frequency space*. This effect is not just mathematical—you can hear it. A heavily damped bell that rings for very few cycles produces an abrupt note

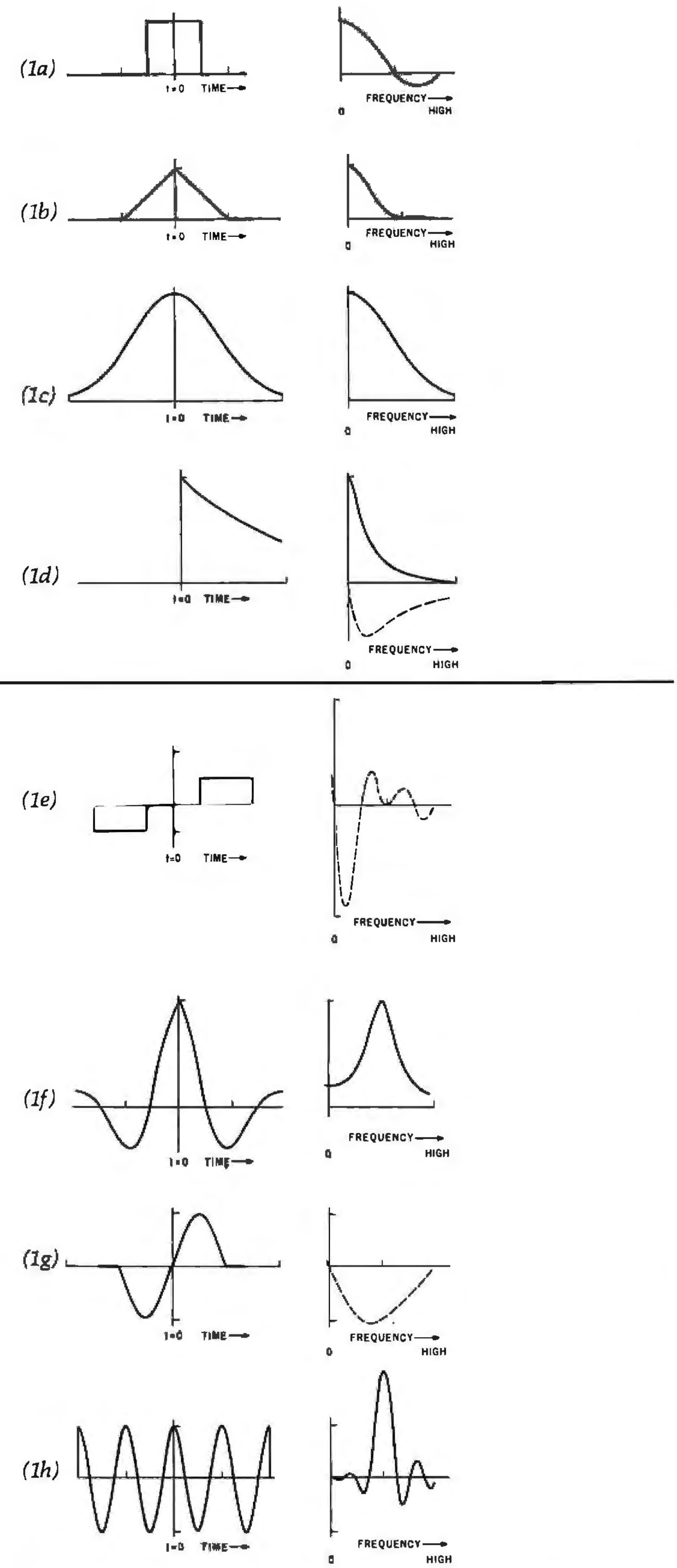

Figure 1: *Graphs on the right (functions of frequency) plot Fourier transforms for the specific functions on the left (functions of time), indicating the amount of each component frequency present in the original. Abrupt changes with respect to time (figures 1a thru 1d) are reflected in the transforms by the presence of higher-frequency energy. Graphs of functions exhibiting periodicity (figures 1e thru 1h) produce peaks centered on the frequency of this oscillation in the associated transform.*

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Listing 1: *The 6502 machine-language program 2DFT performs two-dimensional Fourier transform of images on the Commodore PET's video display. SINTAB is a table of sin (x) for x=0, π/20, 2π/20,...,thru 19π/20, in PET floating-point notation (5 bytes per number). Numbers may be scaled up or down for normalization; one good choice is to divide each sine by the square root of 32. ROWSXFRMD is a table of transformed rows from the screen, beginning with row 0, frequency 0, real (cosine) transform, then row 0, frequency 0, imaginary (sine) transform, then row 0, frequency 1, real transform, then imaginary, and so on, ending with row 24, frequency 20, imaginary transform.*

```
      DOROWS:  LDA #18            ;enter here to transform rows of screen data
               STA ROWCOUNT       ;do 24+1 rows (all of them)
               LDA #C0
               STA ROW0           ;point to bottom row of screen
               LDA #83
               STA ROW0+1
               LDA #FB
               STA ANS0           ;point to bottom of answer area for storage
               LDA #1F
               STA ANS0+1
       LOOP1:  JSR ROWTRANSFORM
               DEC ROWCOUNT
               BMI DONE           ;DONE = RTS instruction, to return to BASIC control
               SEC
               LDA ROW0
               SBC #28            ;back up to prior row (40 elements/row)
               STA ROW0
               BCS OVER1
               DEC ROW0+1
       OVER1:  JMP LOOP1
        DONE:  RTS

ROWTRANSFORM:  LDA #64            ;number in FREQ is 5 times frequency (5 bytes/number)
       LOOP2:  STA FREQ           ;initially set to maximum frequency...count down to 0
               LDA #C3
               STA POINT          ;set pointer for sine (imaginary part) transform
               JSR ONEFREQ
               JSR STOREIT
               LDA #91
               STA POINT          ;set pointer for cosine (real) transform
               JSR ONEFREQ
               JSR STOREIT
               LDA FREQ
               SEC
               SBC #5             ;decrement frequency being analyzed for
               BPL LOOP2          ;do all frequencies 0-20 inclusive
               RTS

     STOREIT:  LDX ANS0
               LDY ANS0+1         ;setup for PET utility subroutine
               JSR DAA6           ;store P at X+256Y
               LDA ANS0
               SEC
               SBC #5             ;move answer pointer back to a free space
               STA ANS0
               BCS OVER2
               DEC ANS0+1
       OVER2:  RTS
     ONEFREQ:  LDA #27
               STA COLNUM         ;set column counter to maximum = 39
               LDX #5
               LDA #0
       LOOP3:  STA MYACC-1,X      ;MYACC is 5 adjacent page zero.locations
               DEX                ;clear them out here
               BNE LOOP3
         TOP:  LDY COLNUM
               LDA (ROW0),Y       ;get screen character at current row & column
               TAY
               LDA #0
               JSR D278           ;convert integer 256A+Y to floating in P
               LDY #STABPG        ;point to page of sine table
               LDA POINT          ;256STABPG+POINT points to a sine to be multiplied in
               JSR D8FD           ;(sine)*P is calculated and stored in P
               LDY #0
               LDA #MYACC         ;point to MYACC, my accumulator's 5 bytes
               JSR D73C           ;(MYACC)+P is put into P
               LDY #0
               LDX #MYACC
               JSR DAA6           ;(P) gets rounded & transferred to 256Y+X (my acc.)
               DEC COLNUM
               BMI DONE           ;quit when all columns done
               LDA POINT
               SEC
               SBC FREQ           ;move pointer a distance FREQ through table
               BCS OVER3
               ADC #C8            ;work modulo 200, to stay on table
       OVER3:  STA POINT
               JMP TOP
```

Listing 1 continued on page 174

without a well-defined musical pitch. A tuning fork that rings for thousands of cycles makes a clear, precise tone.

Contemplation of some graphs of Fourier-transform function-pairs can lead to a number of other useful insights. The illustrations in figure 1 were adapted from Ron Bracewell's excellent book, *The Fourier Transform and Its Applications* (see references), which is worth looking at for further inspiration.

Adding a Dimension

Many signals, like sound, or light from a star, are essentially one-dimensional, and the techniques discussed above and in the earlier part of this article are immediately applicable to them. But there are other, extremely interesting signals which are two, three, or more dimensional when they arrive. Rather simple extensions of the concepts involved in one-dimensional spectral analysis will allow multidimensional signals to be transformed, analyzed, and manipulated. I'll discuss the two-dimensional case because problems with more dimensions can be attacked by completely analogous methods.

What function does a two-dimensional Fourier transform serve? For one thing, it can help solve many three-dimensional problems which have translational symmetry; that is, problems in which one of the three spatial dimensions can be trivially factored out. An obvious example is a system like a coaxial cable, or a cylindrical waveguide, where everything looks the same as you move along the length of the device. Two-dimensional Fourier transforms can give the electrical characteristics of such systems. To some extent, problems involving thin layers like the Earth's atmosphere can be dealt with using two-dimensional transforms.

If that were all, a few people might play around with two-dimensional spectral analysis, but it wouldn't be a huge industry. However, there's another class of problems that are of overpowering interest. These problems are in the field of imaging, or remote sensing. Ever since evolution came up with the first rudimentary eye-spots, creatures have been using electromagnetic radiation to probe their environments. With the development of lenses that form a two-

Text continued on page 178

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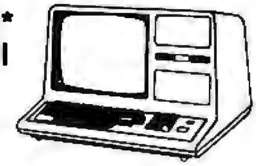

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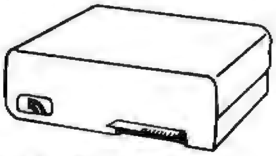

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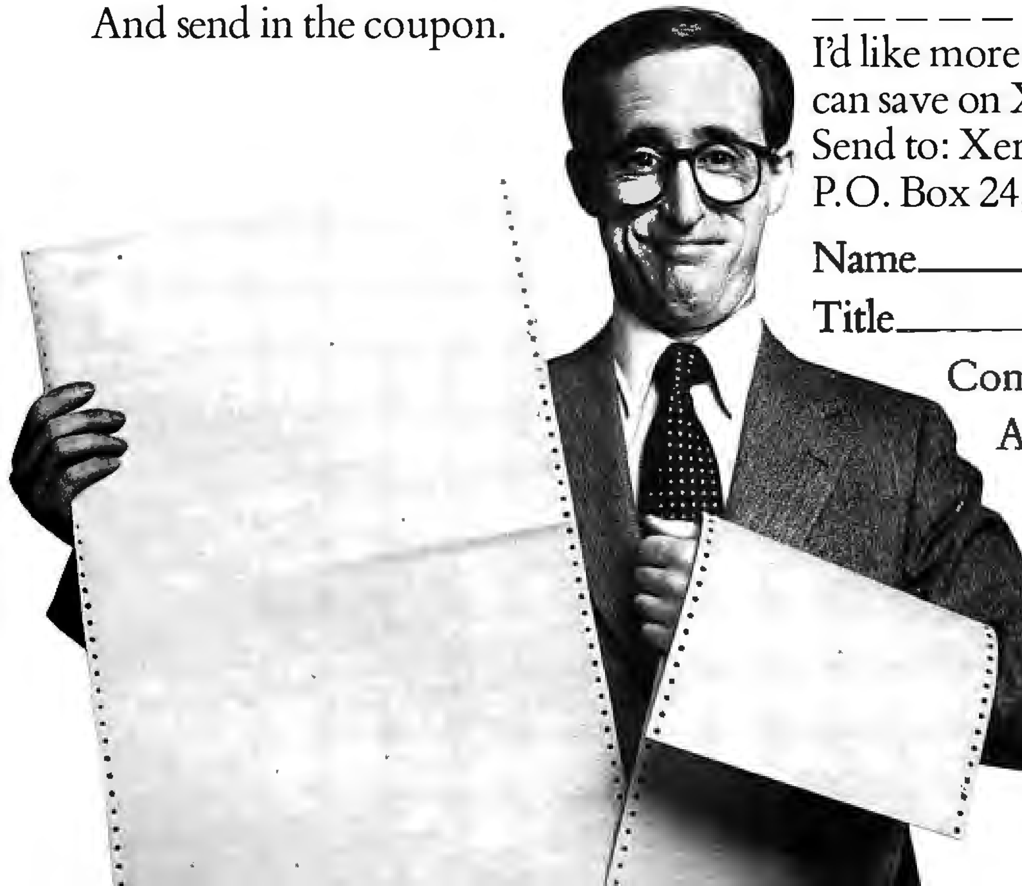
Circle 99 on inquiry card.

Listing 1 continued:

```
DOCOLS:  LDA #14            ;enter here to transform and display 20*2 columns
         STA COLNUM
 LOOP4:  LDA #3C            ;60/5=12 is maximum frequency which can be shown
         STA FREQ           ;begin at 12 and do frequencies through -12
         JSR FTC&D          ;fourier transform column & display
         DEC COLNUM
         BPL LOOP4
         RTS                ;when finished, go back to BASIC control

 FTC&D:  LDA COLNUM
         CLC
         ADC #D3
         STA RDISP          ;point to screen address of right-hand column to
         LDA #83            ;be displayed (zero at center)
         STA RDISP+1
         LDA #13
         SEC
         SBC COLNUM
         STA LDISP          ;point to left-hand display column
         LDA #80            ;(column 20 is only displayed on right...see below)
         STA LDISP+1
         LDA COLNUM
         ASL A
         STA ADRS           ;temporary storage for multiplication 10*COLNUM
         ASL A
         ASL A
         ADC ADR$           ;now we have 10*COLNUM
         ADC #2E            ;and now accumulator points to low byte of the real
         STA STASH          ;part of the last ROWSXFRMD table entry for this column
 LOOP5:  STA ADRS
         LDA #1F            ;high part of end of ROWSXFRMD table  address in 8K PET
         STA ADRS+1
         LDA #91
         STA POINT          ;pointer set for cosine transform of real part of data
         JSR COLXFRM        ;returns answer in MYACC and in P
         LDX #5
 LOOP6:  LDA MYACC-1,X
         STA COSACC-1,X     ;transfer answer to COSACC on page zero, 5 bytes
         DEX
         BNE LOOP6
         LDA #1F
         STA ADRS+1         ;reset data pointer before doing sine transform
         LDA STASH          ;stash holds result of low byte address calculation
         CLC
         ADC #5             ;add 5 to get to point to imaginary part of data
         STA ADRS           ;there is never a carry
         LDA #C3
         STA POINT          ;point setup for sine transform of imag. data
         JSR COLXFRM
         LDY #0
         LDA # COSACC
         JSR D95E           ;transfer COSACC to S
         JSR D728           ;calculate S-P and leave result in P
         JSR DADE           ;copy P to S
         LDA #0
         STA SGNCOMPR       ;set sign comparison (address BE) to +
         LDA B0             ;must call PET subroutine with (B0) in A
         JSR D900           ;(P)*(S)=(P)**2 is calculated and left in P
         LDY #0
         LDX # COSACC
         JSR DAA6           ;transfer P to COSACC
         LDA #1F
         STA ADRS+1
         LDA STASH
         STA ADRS           ;point to real data again
         LDA #C3
         STA POINT          ;setup for sine transform of real data
         JSR COLXFRM
         LDX #5
 LOOP7:  LDA MYACC-1,X
         STA SINACC-1,X     ;transfer answer to SINACC on page zero
         DEX
         BNE LOOP7
         LDA #1F
         STA ADRS+1
         LDA STASH
         CLC
         ADC #5
         STA ADRS           ;point to imaginary data
         LDA #91
         STA POINT          ;and do cosine transform
         JSR COLXFRM
         LDY #0
         LDA # SINACC
         JSR D73C           ;add (SINACC)+(P) and store in P
         JSR DADE           ;copy P to S
         LDA #0
         STA SGNCOMPR
```

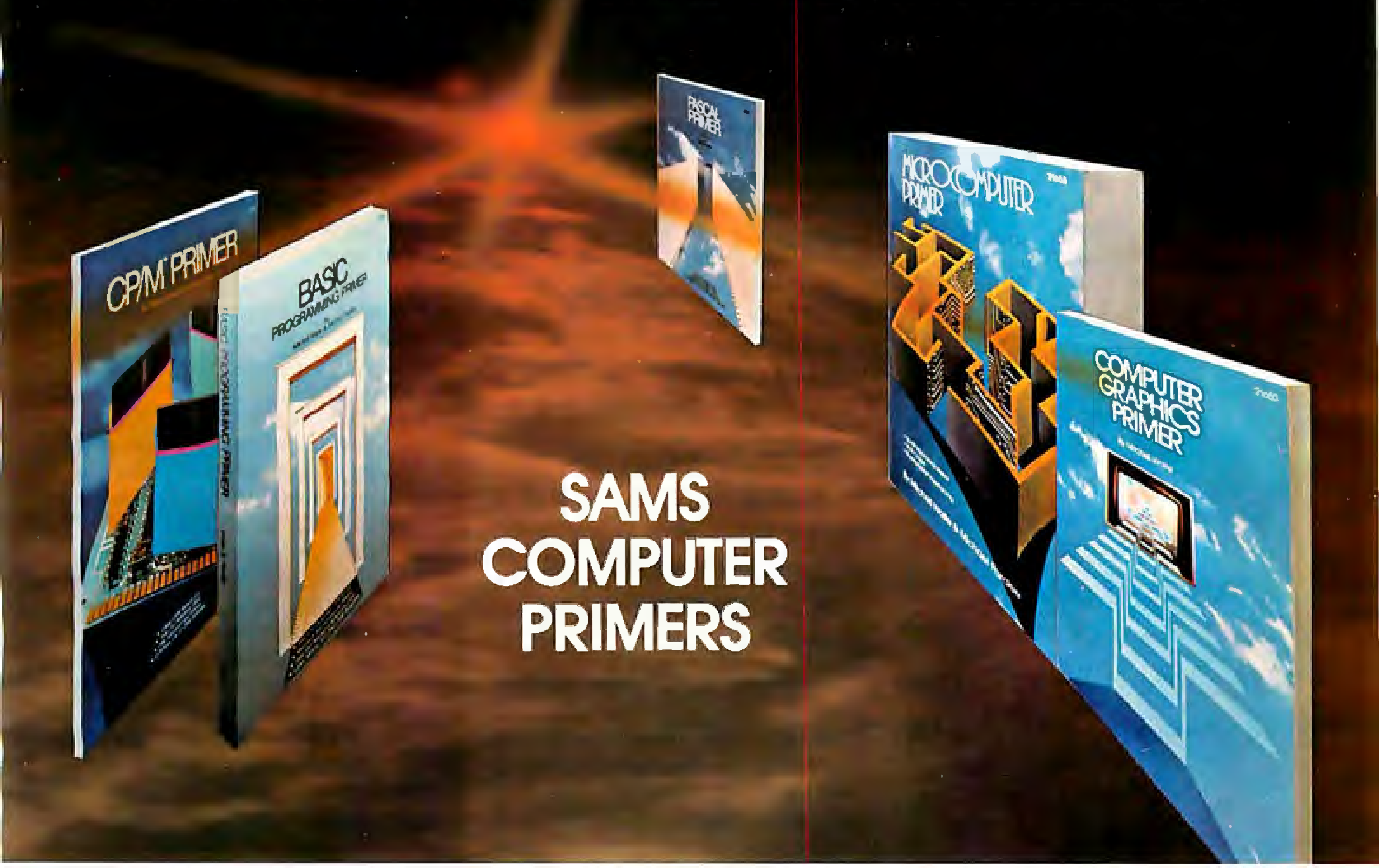
Listing 1 continued on page 176



Listing 1 continued:

```
           LDA B0
           JSR D900          ;square of P is now in P
           LDY #0
           LDA #COSACC
           JSR D73C          ;(COSACC)+(P) is in P
           JSR DE24          ;SQR(P)...now we have fourier amplitude to be plotted!
           LDA  B0           ;must avoid overflow, so check exponent of answer
           CMP #89
           BCS LIMITER       ;take branch if result is bigger than 255
           JSR D0A7          ;convert P to an integer in B3,B4
           LDA B4            ;but B3 is zero, by limiting process
           JMP OVERLTD
LIMITER:   LDA #FF           ;replace overflow by 255
OVERLTD:   LDY #0
           STA (RDISP),Y     ;display it on the screen!!--first, right column
           TAX
           LDA RDISP
           SEC
           SBC #28           ;subtract 40 to point to previous row
           STA RDISP
           BCS OVER4
           DEC RDISP+1
  OVER4:   LDA COLNUM
           CMP #14           ;check column number, and don't plot column
           BEQ OVER5         ;number 20 (no room on screen!)
           TXA
           STA (LDISP),Y     ;plot result in left column here
           LDA LDISP
           CLC
           ADC #28           ;add 40 for next row
           STA LDISP
           BCC OVER5
           INC LDISP+1
  OVER5:   LDA FREQ
           CMP #C4           ;see if we've reached frequency of -12 yet...
           BEQ DONE2
           SEC
           SBC #5            ;decrement frequency
           STA FREQ
           LDA STASH
           JMP LOOP5         ;go back and do it again at new frequency
  DONE2:   RTS
COLXFRM:   LDA #0
           LDX #5
  LOOP8:   STA MYACC-1,X     ;clear out MYACC's 5 bytes
           DEX
           BNE LOOP8
           LDA #19
           STA ROWNUM        ;initialize counter of rows
  LOOP9:   LDY ADRS+1
           LDA ADRS
           JSR DA74          ;transfer column member pointed to by ADRS to P
           LDY #STABPG       ;point to sine table page
           LDA POINT
           JSR D8FD          ;(sine)*P in P
           LDY #0
           LDA #MYACC
           JSR D73C          ;(MYACC)+(P) in P
           LDY #0
           LDX #MYACC
           JSR DAA6          ;(P) to MYACC
           DEC ROWNUM
           BEQ DONE2         ;return when all 25 are done
           LDA POINT
           SEC
           LDX FREQ
           BMI NEGFREQ       ;must handle movement of pointer carefully
           SBC FREQ
           BCS OVER6
           ADC #C8           ;work modulo 200, stay in table
  OVER6:   STA POINT
           JMP NXTADR
NEGFREQ:   SBC #C8           ;for FREQ less than zero, this section
           CMP FREQ          ;moves pointer while staying within table
           BCC OVER7
           SBC FREQ
           JMP OVER6
  OVER7:   LDA POINT
           SEC
           SBC FREQ
           JMP OVER6
 NXTADR: . LDA ADRS
           SEC
           SBC #D2           ;back up 210 to previous column member
           STA ADRS
           BCS OVER8
           DEC ADRS+1
  OVER8:   JMP LOOP9
```

SHORTEN THE JOURNEY TO KNOWLEDGE.



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Text continued from page 170:

dimensional image on the retina, remote sensing took a giant step forward.

When conditions are good, the images that develop on photographic plates or inside vidicons (television-camera tubes) can be used just as they are. But often, noise or other interference makes the original image low-quality. When astronomers look up, or spy satellites look down, they want to squeeze every possible bit of information out of their sensors, to "milk" every photon. That's one major reason for all the progress in image analysis and two-dimensional signal processing that has been made in the past few decades.

Advantages of transforming a visual image into the frequency domain overcome all the limitations of the photographic medium.

The advantages of transforming a picture into the frequency domain, where the elements of the image that vary periodically are gathered and grouped together, are numerous, just as were the advantages of analyzing a one-dimensional signal in frequency space (as discussed last month in Part 1). By working digitally inside a computer, you overcome all the limitations of the photographic medium. It's easy to enhance or mute contrasts, to intensify edges of objects (high-spatial frequencies) or to take out distracting large-scale brightness variations (low-spatial frequencies). The wonderful images that come back from NASA's planetary probes are automatically processed by these kinds of techniques before anyone sees them.

If, after all this build-up, you're expecting to hear that the two-dimensional Fourier transform is an arcane, incomprehensible mathematical process, I'm sorry, but I have to disappoint you. To take a two-dimensional transform, you merely need to choose a pair of perpendicular coordinate axes (x and y). First do a one-dimensional Fourier transform in the x direction, and then do a one-dimensional transform on the result of that, in the y direction. That's all there is to it!

The 2DFT Program

The 6502 assembly-language program in listing 1 performs two-dimensional Fourier transforms. The program takes as its input data the contents of the Commodore PET microcomputer's video-display screen: 1000 numbers, arranged in 25 rows of 40 integers, each one in the range 0 thru 255. The results of the transformation are displayed on the screen. Only the amplitude of the transform is shown; all phase information (whether the wave is sine, cosine, or a mixture) is suppressed.

I'd like to take a little time now to describe how the program works, and the choices and compromises I had to make in implementing it. This discussion should help you if you need to adapt 2DFT to run on a different microcomputer, and it should also be a useful starting point for modifications and improvements of my program. After the discussion, I'll return to the uses of the program, the insights that you can achieve by playing around with it, and the fascinating topic of holography, and how to do it with this program.

First, concerning the fundamental algorithm used to do the transforms: as mentioned above, a true two-dimensional Fourier transform results after you perform separate one-dimensional transformations on each row of a matrix, and then perform separate one-dimensional transformations on each resulting column of data. 2DFT does that. The routine DOROWS finds the amount of cosine phase necessary at each frequency, as well as the amount of sine. Those numbers are stored in memory for each row. Then, the routine DOCOLS does the same thing for each column of stored half-transformed data, and puts the amplitude of each resulting frequency-space point onto the screen. The amplitude is simply the square root of the sum of the squares of the cosine component and the sine component (like finding the hypotenuse of a right triangle).

To do the one-dimensional row and column transformations, DOROWS and DOCOLS call subroutines ROWTRANSFORM and COL-

Software for the Apple II and Apple II Plus*


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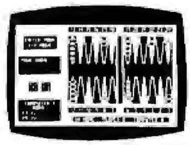

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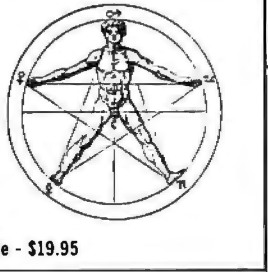

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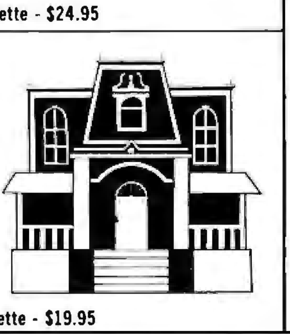

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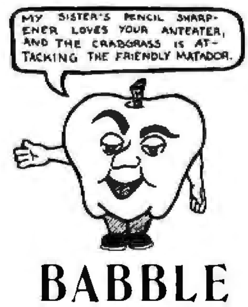

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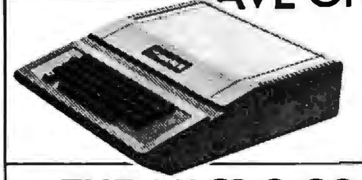

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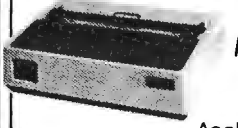

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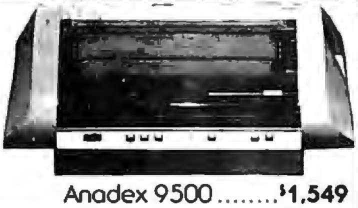

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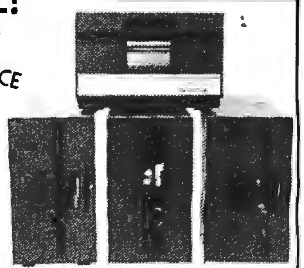

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XFRM, respectively. These simply use the old, classical, straightforward method of calculating a Fourier transform — no fast-Fourier-transform subtleties!

I've avoided talking about the mathematical mechanism for moving from ordinary space to the frequency domain in these articles so far, because there are ample technical references which explain such matters in great detail, and because the calculation tends to get in the way of the real substance of the subject, especially in an introduction such as this one. Here, let me just say that the transforms are accomplished by multiplying each row (or column) element by a sinusoidally varying factor, and adding up the results of those multiplications at each frequency. To find out how much cosine phase at frequency f is in a given row, multiply each row element $r(x)$ by $\cos(2\pi fx)$ and sum those products for the whole length of the row. The amount of sine wave is found by multiplying $r(x)$ by $\sin(2\pi fx)$ and summing those results. You can unite the cosines and sines into a set of complex numbers, with the cosines making the real parts and the sines the imaginary parts. Then, usual complex-number algebra helps keep track of how to add and subtract components during the transformation process.

S	P	Contents	S = e	P = − π/2
B8	B0	exponent + 80	82	81
B9	B1	fractions MSB	AD	C9
BA	B2	frac. byte 2	F8	0F
BB	B3	frac. byte 3	54	DA
BC	B4	fraction LSB	59	A2
BD	B5	sign	00	FF
BE		sign comparison	FF	
BF		roundoff byte	00	

Note: +, −, *, /, and ↑ must be called with S in B8 thru BD, sign comparison set to (B5) XOR (BD), and (B0) in A

0000	USR(P)
CED6	S OR P
CED9	S AND P
D264	FRE(P)
D285	POS(P)
D349	STR$
D5C4	CHR$
D5D8	LEFT$
D604	RIGHT$
D60F	MID$
D654	LEN
D663	ASC
D685	VAL
D6E6	PEEK
D728	S − P
D73C	JSR D95E, then S + P
D73F	S + P
D7AC	normalize P
D8BF	LOG(P)
D8FD	JSR D95E, then S * P
D900	S * P
D95E	[A + 100Y]→S, separating sign, set sign comparison, return with (B0) in A
D9E4	S / P
DA74	[A + 100Y]→P, separating sign
DAA6	roundoff(P)→[X + 100Y], merging sign
DACE	S→P
DADE	P→S, with rounding
DAE1	P→S, without rounding
DAED	roundoff(P)
DAFD	SGN(P)→A
DB0B	SGN(P)
DB2A	ABS(P)
DB9E	INT(P)
DE24	SQR(P)
DE2E	S ↑ P
DEA0	EXP(P)
DF45	RND(P)
DF9E	COS(P)
DFA5	SIN(P)
DFEE	TAN(P)
E048	ATN(P)

Conversions: D0A7 P→integer in B3,B4 [100B3 + B4]
D278 integer in A,Y [100A + Y] → P

Constants in floating (merged sign) notation:

E024	1/4
DDE3	1/2
E01A	π/2
CDBC	π
E01F	2π

Table 1: *Entry points for Commodore PET ROM functions, including floating-point subroutines that are utilized directly by the author's program.*

None of this is anything for a nonmathematically inclined person to worry about; it's just a recipe for the machine to follow in order to crank out the answers. There's no more need to follow the details of the process than there is to follow the details of how your pocket calculator computes exponentials or logarithms. In ten or twenty years, as the power of computers grows and their cost shrinks, there will probably be single-keyword instructions to perform Fourier transforms, just as most machines now have EXP and LOG routines available. Some people will still work with the nitty-gritty, low-level algorithms and procedures, just as some engineers work with individual transistors today. But most human work will be done using higher-level languages, where it's easier to invent new concepts and prove theorems. Machines will handle the low-level dirty work.

Besides the specific algorithm I chose to use, some other important decisions went into the design of 2DFT. First, to avoid all danger of arithmetic overflow and underflow, I use floating-point procedures except at the final stage where the results of the transformation are displayed. At that point, the floating numbers are converted into fixed-point integers and any results greater than 255 are truncated to equal 255. (There are never any negative results because the square root of the sum of the squares is always positive or zero.)

To save program space and avoid the headaches of writing my own routines, I call the floating-point procedures in the PET's BASIC ROM. Table 1 is a list of hexadecimal addresses of the entry points to these routines, and includes short descriptions of what each routine does and how to call it. (Driven by my need for machine-language floating-point capabilities, I found the locations of these subprograms, and I don't think that there can be anything wrong with PET owners using the subroutines in their programs, as I've done. I should also note, however, that Commodore and Microsoft may change the addresses given in table 1 in future production of PETs and other machines.)

A second important choice that was made in the design of 2DFT was

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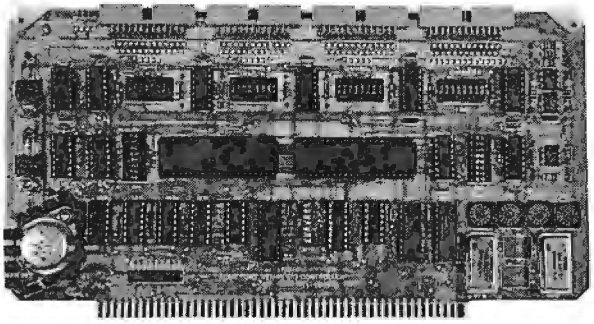

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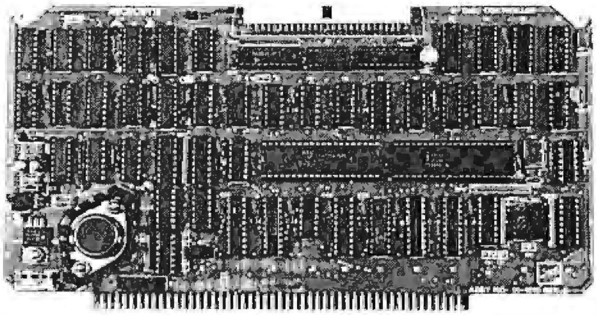

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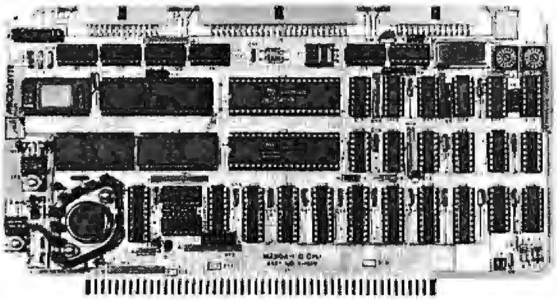

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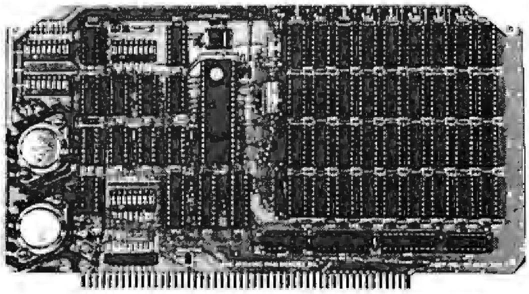

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to use the same scales for the horizontal and vertical axes in the Fourier transform. This is not as obvious a choice as it might seem. Because the video display screen isn't square, it might seem to be better to squeeze the vertical scale, so that as many high frequencies could be plotted in the vertical direction as are plotted horizontally. The resulting distortion would be perfectly acceptable mathematically, but it would make the pictures harder to look at and might be responsible for some mistaken notions on the part of naive viewers. Additionally, choosing different scales for horizontal and vertical transformations would require the use of a different set of sines and cosines for each dimension.

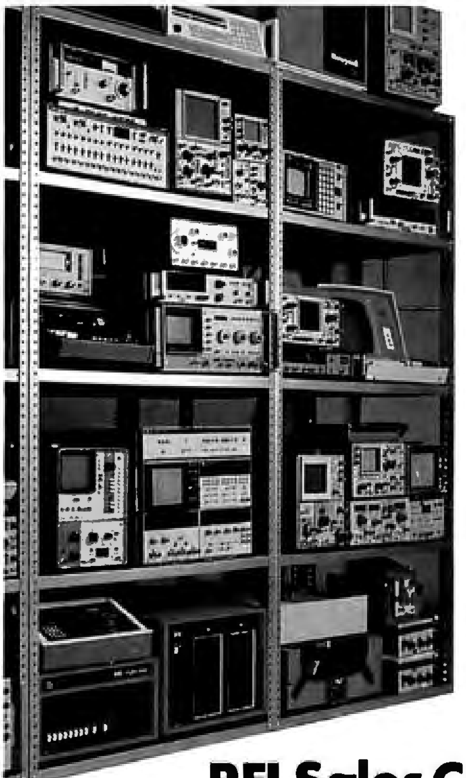
I chose instead to make the scales in the frequency domain equal. The required sines and cosines are stored in a table (on PET memory page STABPG, in listing 1); a pointer moves through the table, allowing the transformation subroutines to read off the trigonometric functions with a minimum amount of computational overhead. The effect of making the scales equal in both directions is that instead of using a 25- by 40-pixel (picture-element) screen, the program is really transforming a 40 by 40 image. The extra 15 rows are presumed to be filled with zeroes before every transformation. After transforming, the high frequencies that fall outside the bounds of the video screen are not calculated. (This is not a devastating loss; as you may have heard, you can cut off and throw away part of a hologram and still reconstruct the whole original image from the remaining fragment. The only cost is a loss of resolution and sharpness in the reconstructed image. More on this later.)

The third significant choice I made in writing 2DFT was to display the amplitude of the Fourier transform: the square root of the sum of the squares of the sine and cosine components. A photographic plate has a sensitivity that is proportional to the light energy which falls in any given area. Taking the square root adds mathematical complexity and computational time to the transformation process. On the other hand, the square-root operation makes it a lot easier to look at and interpret the transform results on the video screen. It prevents almost all overflows because any number between 0 and 65,535 is mapped into the range 0 to 255 automatically. The cost in time is an additional 10% or so, which is acceptable for the benefits that result. Finally, the nonlinearity of the square root turns out not to interfere much with the holographic process, in my experiments.

The video-character generator used in the PET is capable of storing a number between 0 and 255 in each of the thousand screen locations, but for human viewing, this kind of a display isn't very good. In the BASIC driver program which calls and controls 2DFT, I've included short routines to convert the screen contents to and from a "density plot," where each pixel on the display is filled with a character with brightness propor-

Listing 2: *This program calls 2DFT and helps translate its results to a form more easily viewed by a human. A picture can be drawn on the screen, using the usual cursor-control characters. Hitting the exclamation-mark key turns the picture into a form that 2DFT can read, where each cell has in it a number (from 0 thru 255) proportional to the magnitude of the image at that cell. The quote key turns the numbers back into a "density plot" where the brightness of each cell is proportional to its magnitude.*

```
  5    REM**POKE 135,6 BEFORE RUNNING TO PROTECT MACHINE-LANGUAGE 2DFT PROGRAM
 10    DATA 32,58,59,103,106,118,225,245,244,229,160:FOR I=1 TO 10:READ G%:NEXT
 20    PRINT "HIT -RETURN- TO TRANSFORM SCREEN"
 30    PRINT "     -QUOTES- TO MAKE DENSITY PLOT"
 40    PRINT "     -  !   - TO TURN DENSITY TO NUMBERS"
100    GET A$:IF A$="" GOTO 100
110    I=ASC(A$):IF I=13 GOTO 200
120    IF I=34 GOTO 800
130    IF I=33 GOTO 900
140    PRINT A$;:GOTO 100
200    SYS(1536):SYS(1713):GOTO 100
800    FOR I=32768 TO 33767:A=PEEK(I):POKE I,G%(A/25):NEXT:GOTO 100
900    FOR I=32768 TO 33767:A=PEEK(I):B=10:FOR J=0 TO 9:IF A-G%(J) THEN B=J:J=9
910    NEXT:POKE I,25*B:NEXT:GOTO 100
920    REM**POKE 135,32 WHEN FINISHED TO REGAIN ACCESSIBILITY TO ALL MEMORY
```



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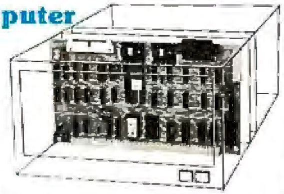

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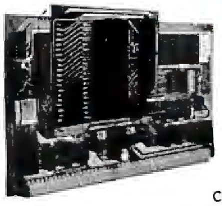

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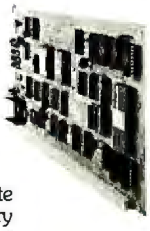

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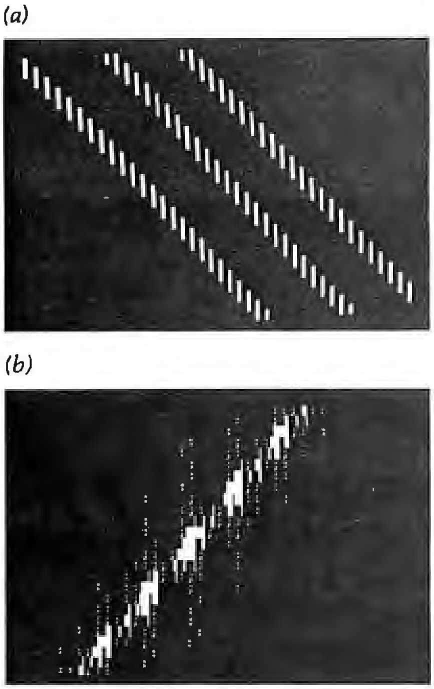


Photo 1: *Photo 1a shows a simple image of low-frequency components present along the length of the stripes. Perpendicular to the stripes, strong periodicity occurs at frequencies that are multiples of the spacing frequency. The resulting transform is shown in photo 1b.*

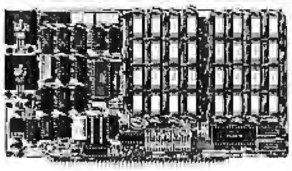
tional to the number formerly stored in that cell (see listing 2). The density-plot display uses only eleven distinct symbols, so it's as if the 8 bits stored in each screen location have been truncated to about 3½ bits. The loss of precision is not severe, and the density plots are much easier to look at and understand than the raw data.

Experimenting with 2DFT

As I have implemented it, the 2DFT program takes about 4 minutes to do a single complete two-dimensional Fourier transform of the contents of the PET's screen and display the results. (It runs faster if the input data contains many zeroes, since the floating-point multiplication routine in the PET knows how to multiply by zero quite rapidly!) The columns of the answers are plotted as soon as they are calculated. After a computation, 5250 bytes of PET memory are left containing the results of the row transformations in floating-point notation (5 bytes per number). Because the input data was a set of strictly real numbers, fifty of the sine components are always exactly zero (two zeroes per row), and so there are 1000 independent numbers in memory—precisely as many independent numbers as there were cells on the screen. This is not coincidental; the Fourier-transformation process "conserves information," so it had to turn out that way.

For your first experiments, and to confirm that the program is working correctly, I recommend that you transform simple pictures. A good test is a picture made up of parallel stripes (see photo 1). The picture, like a picket fence, has only low-frequency components present in the direction along the length of the stripes. Perpendicular to the stripes, there is a strong periodicity, at frequencies which are multiples of the fundamental spacing frequency. Logically, the transform should be a series of bright spots running along a line perpendicular to the original stripes.

Another good test is to transform a sharp spike—a picture with only one cell illuminated. Such a sharp point is made up of equal amounts of sine waves at all frequencies and in all directions. Thus, the result of transforming a spike should be a



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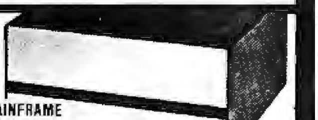

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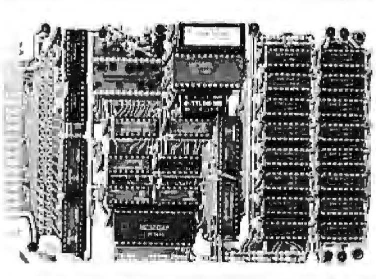

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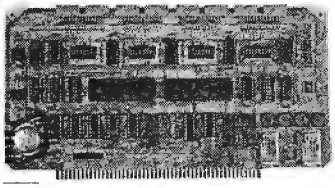

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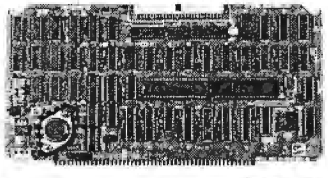

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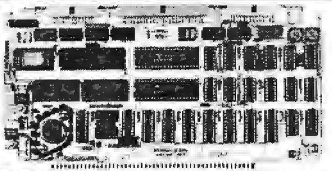

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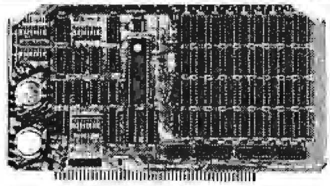

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screen with equal intensities in every cell.

One of the first things that you should discover when experimenting with 2DFT is that the absolute location of a picture on the screen doesn't matter. Shifting a picture changes the phases of the sines and cosines that go into making that image, but it does not change the amplitude of the frequency spectrum of that picture. Because only the amplitude and not the phase is displayed, two pictures which differ only by some shift should give the same transforms. (This insensitivity to shifts is one reason for the usefulness of Fourier transforms in pattern-recognition problems!)

Another thing to notice about 2DFT is the relative overall intensity of a picture and its transform. This intensity, of course, is somewhat arbitrary, since by multiplying each element of the transform's sine table by some constant, the whole transformed picture gets multiplied by the square of that constant. (The constant shows up squared because the sine table is used two times, once to transform the rows and once for the columns.)

If none of the transformed image was lost because of the nonsquare screen, it would be possible to adjust the constant that multiplies the sine table so that the sum of the squares of the pixels *before* a transform equals the sum of the squares *after* transforming. The multipler is 1/SQR(L), where L is the length of a side of the square screen.

In my implementation of 2DFT, I tried multiplying every element of the sine table by 1/SQR(32) and have found it to work well. Thirty-two is a reasonable mean value between the length of a row and the length of a column. The exact choice of the constant isn't critical unless you want to be able to read off quantative mathematical transformation results. For experimental purposes, any value that keeps the picture elements from growing too bright or too dim is acceptable.

An obvious quality of the transfor-

mations produced by 2DFT is that they are symmetric about a cell near the center of the video screen. The cell around which everything seems to revolve is the (0,0) cell, the center of the frequency domain. It contains the sum of all of the cells in the untransformed picture multiplied by any factors that were chosen for the sine table. It's also the cell which is most likely to suffer from an overflow problem because all of the pixels in each original image were positive numbers and add together to make a large zero-frequency total. (2DFT displays overflows as a character of maximum brightness, for the number 255.) The rest of the transformed image is symmetric about the central cell, in the sense that each cell contains the same number as the cell an equal distance away on the opposite side of the middle.

This follows mathematically from the fact that the original image was entirely real, with no imaginary (complex-number) part. You can think of it as just a convention, if you like; to avoid sharp edges which might cut off parts of a picture, we have plotted "negative frequencies" as if they had the same energy as the corresponding positive frequencies.

It works out then that you can think of the opposite edges of the screen as being joined, so that something moving off the screen at the right-hand side comes in automatically at the left edge. (Between the top and bottom edges, there are 15 unseen lines, however, in order to make the imaginary screen square.) Because there are an even number of columns, one column on each side of the central (zero) column is not duplicated. That column is plotted as the rightmost one on the screen.

It's a good idea to take some time now to draw pictures on the screen, transform them, and try to develop some instincts about what the transforms tend to look like. Many of the results from one-dimensional Fourier analysis carry over to two dimensions. For example, we noted that an

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CBS *DMA*	395	40	A,F,K
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SELECTOR IV *Micro Ap, Inc.*	395	25	A,C,G,K
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BASIC COMPILER *Microsoft*	350	25	A,F,L
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PASCAL/MT+ *MT Microsystems*	250	30	A

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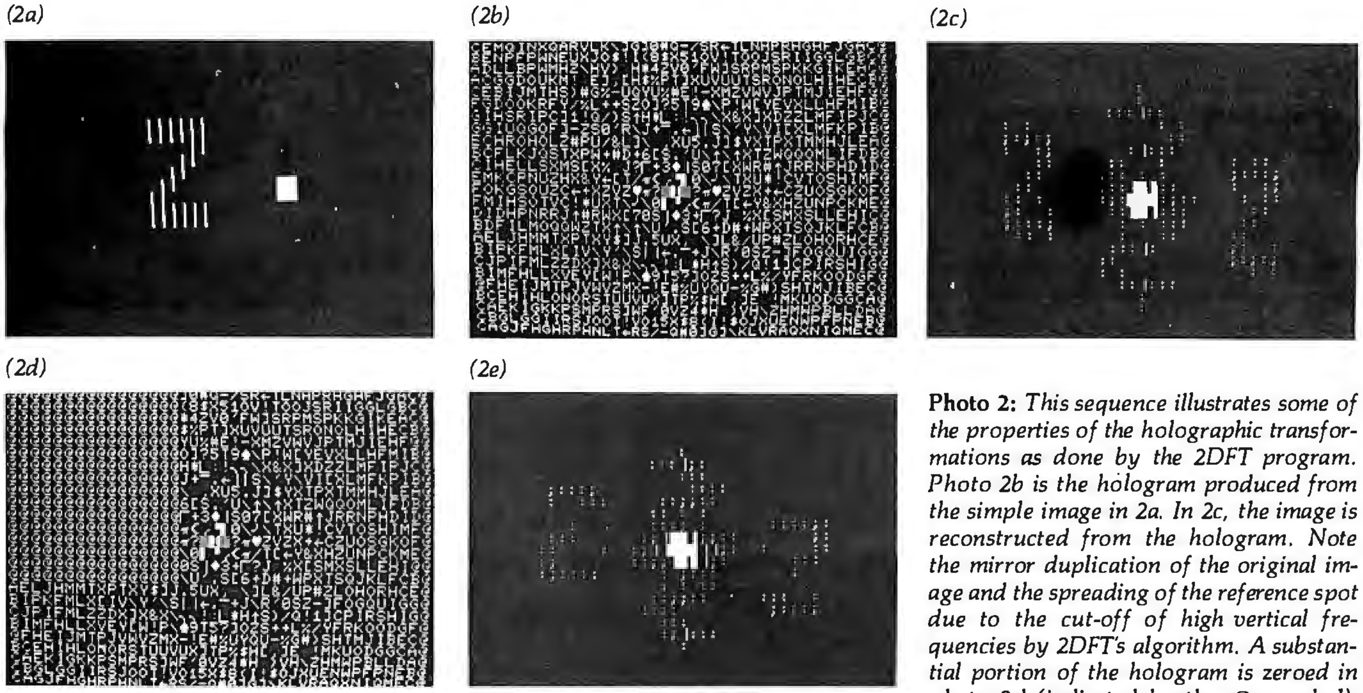

(2a) (2b) (2c)

(2d) (2e)

Photo 2: *This sequence illustrates some of the properties of the holographic transformations as done by the 2DFT program. Photo 2b is the hologram produced from the simple image in 2a. In 2c, the image is reconstructed from the hologram. Note the mirror duplication of the original image and the spreading of the reference spot due to the cut-off of high vertical frequencies by 2DFT's algorithm. A substantial portion of the hologram is zeroed in photo 2d (indicated by the @ symbol), giving the reconstructed image in photo 2e. This reconstruction is fainter and "noisier" than photo 2c, but no part of the overall image is missing.*

image with very fine detail (sharp spikes or narrow lines) in one dimension requires many high-frequency sinusoidal waves to define it; the same is true for two-dimensional pictures. A picture that repeats only a few times across the screen width will have strong low-frequency components in it (components that show up in frequency space near the central zero-frequency cell), while a picture that repeats many times across the screen will have strong components at the higher frequency of repetition. (In your experiments, don't forget that you're not seeing the highest vertical frequencies, which fall outside the screen's height.)

You should realize that even though the program uses horizontal and vertical axes to do the mathematical transform, those axes are artificial and not part of the initial or final picture. So, if you're looking at an image which has strong structure trending along a line from northwest to southeast, feel free to tilt your head and define your own personal axes in such a way as to make the image and its transform easier to think about.

Holography and Very-Long-Baseline Interferometry

One of the most exciting and valuable developments of technology in the past thirty years has been that of holography. *Holograms* can store information at densities far greater than normal photography, and with far better immunity to noise and loss of data from scratches, dust, etc on the film. An equally exciting develop-

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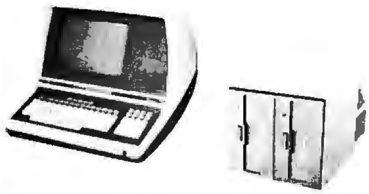

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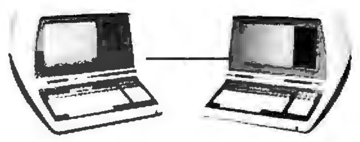
DUAL PROCESSOR



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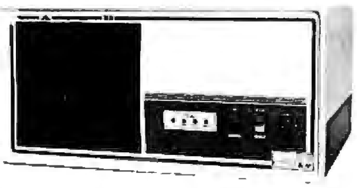

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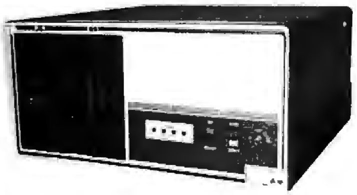

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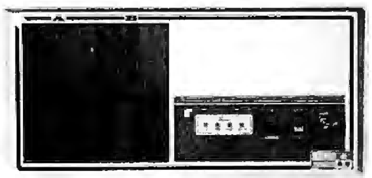

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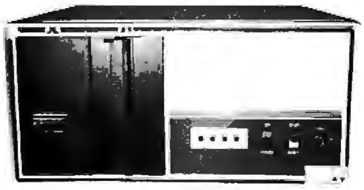

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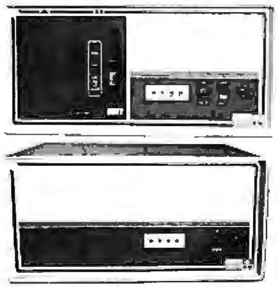

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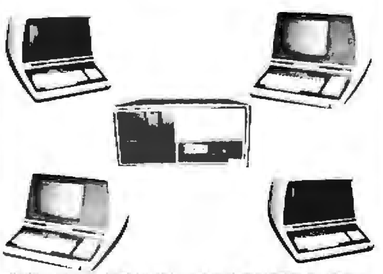

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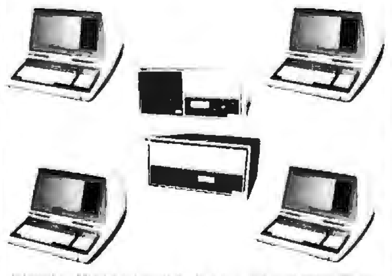

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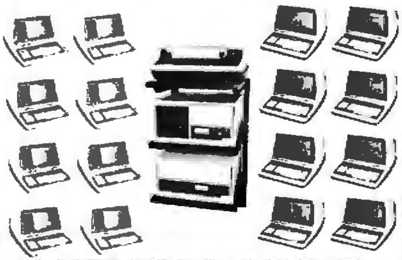

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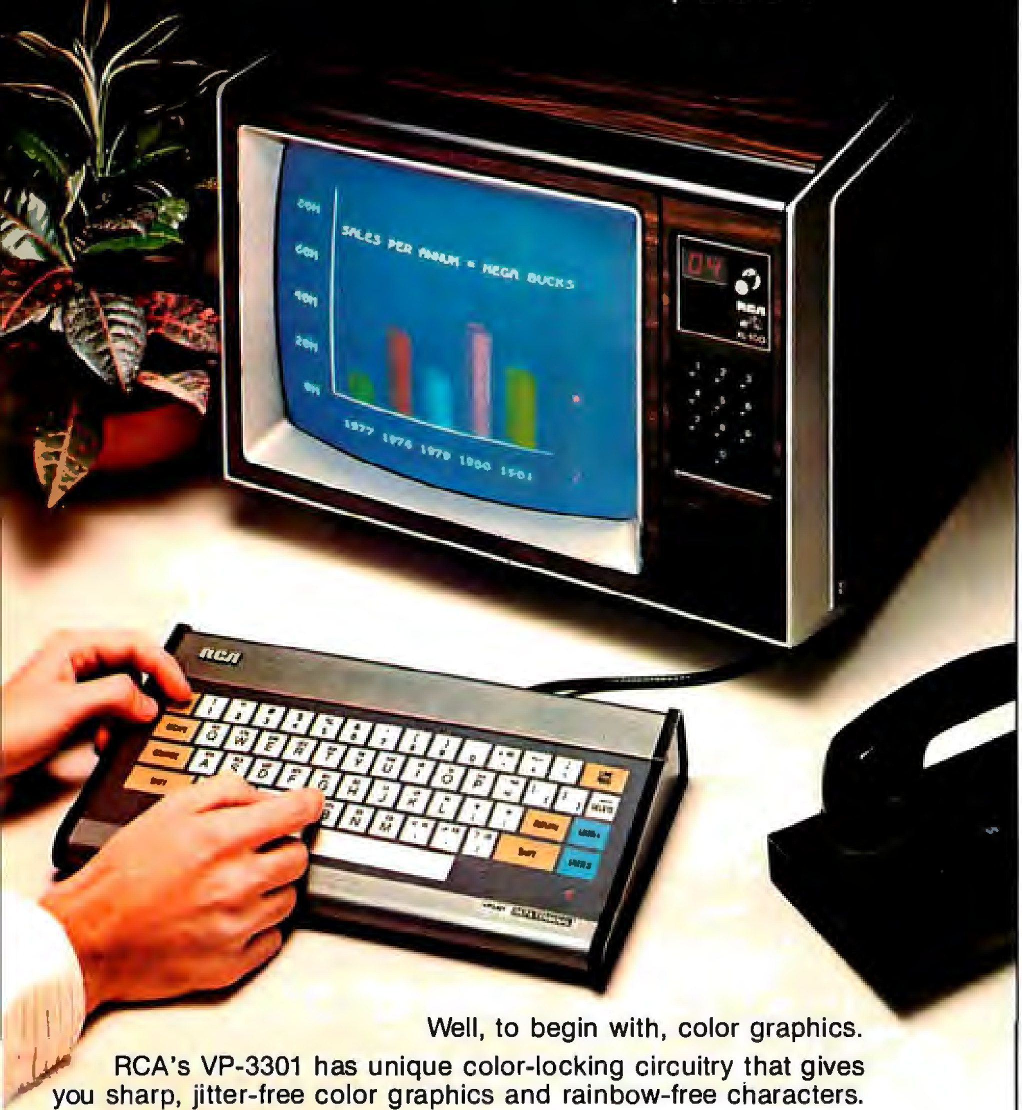

ment in modern astronomy has been the discovery of what's called very-long-baseline interferometry, or VLBI. In a VLBI observation, radio telescopes thousands of kilometers apart look at the same object. The signals which they receive are combined, and by this combination, give a resolving power equal to that of a single telescope as large as the separation between receivers—a telescope as large as the Earth, in some cases!

Even working at wavelengths very long compared to optical light, VLBI techniques enable astronomers to see objects that are hundreds or thousands of times smaller than the largest optical telescopes can resolve. The vast increase in astronomical information-gathering capability has produced new insights during the last few years concerning the structure of distant galaxies and the early history of the universe.

Both holography and VLBI rely on the same secret: the two-dimensional Fourier transform. Using the 2DFT program presented here, it's easy to make and reconstruct one type of hologram, the "Fourier-transform hologram," which is most useful for storing and retrieving two-dimensional information. (Holograms to record three-dimensional objects work on similar principles. See some of the references for more information.) It's also easy to use this program package to experiment with and learn about some of the interferometry problems that radio astronomers face.

Briefly, the results of a very-long-baseline-interferometry observation consist of a map of the object in the sky—a map not in the usual sense, but of the frequency domain. As the Earth's rotation moves the radio-telescope antennas relative to the stars, the signals that the telescopes receive sample different points in the Fourier-transformed plane. With enough observations, using enough antennas, reasonably complete coverage of this transformed map can be achieved.

The big problem in VLBI is to deduce what the astronomical object looks like before transforming. If information about the relative phases of points in the frequency domain were available, it would be possible to unambiguously invert the observations and produce a picture of the object.

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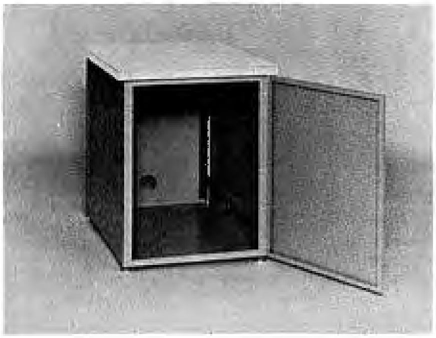

The secret of holography and its sophisticated ability to retain information is the two-dimensional Fourier transform.

Unfortunately, VLBI can't (as of today) produce enough phase information. The astronomers have to look at an image in Fourier-transformed space which contains only amplitude information, just like the image that the 2DFT program produces. In some cases, it's not too hard to guess what the object that produced that transform looked like, but observers often must fall back on model making and try to fit the simplest reasonable approximation they can think of to the data. This is a tough subject, but an important one. A lot of research is going on now in an attempt to find better solutions.

Fourier-transform holography is also a subject for vigorous current research. One reason for the interest is that holograms could possibly provide huge, ultra-fast memories for computer systems. Ordinary microfilm is a very inefficient way to record data. It fails to take advantage of the information-storage ability of high-resolution photographic film, and if the bit density is pushed up, the microfilm technique becomes unacceptably vulnerable to film defects, dust particles, etc. Conventional photographic methods are too highly localized for each bit that is written—it's like trying to transmit information over a noisy phone line without a decent error-detection and correction code!

A hologram, on the other hand, shares many of the best properties of sophisticated error-preventing techniques. Each bit of the original record is spread out over the entire holographic image. A speck of dust can't clobber a particular bit; all it can do is add a slight overall noise to the recovered analog signal, and even that noise can be entirely removed by a simple digitizing process. If half of a photograph is cut off and thrown away, half of the picture is lost forever. If half of a hologram is removed, the *whole* picture is still there! The sharpness of the picture is reduced, but no particular region is lost at all.

How can a hologram work? Photographic film records only the intensity, not the phase, of the light that hits it. The secret is simple: put a phase reference into the original object that is being holographed! This phase reference is just a bright, pointlike spot in the original. When transformed, the bright spot by itself turns into a constant signal over the whole frequency versus space plane because (as mentioned above) a sharp spike is made up of equal amounts of sinusoids at all frequencies.

This constant background signal provides a reference against which the sines and cosines of the other parts of the original object can interfere, constructively and destructively. The background provides the reference phase; the rest of the Fourier-transformed image adds and subtracts relative to that background, and so an intensity recording (as on a photographic plate) includes enough phase information to allow the original image to be reconstructed.

The reconstruction algorithm is simple: just do another Fourier transform of the hologram to return to ordinary space! Mathematically, if phase information is recorded, the operation of Fourier transforming is its own inverse, like the operation of inverting is for numbers. The reconstructed image comes back twice, symmetrically situated about the central zero-frequency spike, but it's easy to mask off one of the two images if necessary.

The 2DFT program is quite capable of taking simple holograms and reconstructing them. Because the transformation is done on a 40 by 40 grid, but only the central 25 rows of forty elements are kept and displayed, some of the high vertical frequencies in the original image will be lost. (That explains the vertical spreading of some of the reconstructions, especially noticeable in the central region.) It's best not to try to recover images with too much fine detail. If the original is made of lines at least two cells thick, it usually comes back quite recognizably.

Note that the bright pointlike spot that provides the reference phase should be brighter than the rest of the original image being transformed; otherwise, the rest of the image tends to act as a (poor) reference phase for

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the bright spot. Also note that some errors come in due to overflow and truncation, as only 8 bits of the hologram are recorded on the display. If you want to, you can turn the holographic display of numbers into a density-plot image for inspection—but the resulting truncation to about 3½ bits means still more noise in the reconstructed image.

It's quite educational to delete a few points (or a sizable fraction) of the hologram, and still see the entire original picture be reconstructed from the remaining fragment. (It may be desirable to change the density-plotting gray-scale factors in some cases, as the image reconstructed from a partially removed hologram is fainter than the usual result.) These are only a few suggestions—try inventing experiments of your own!

A final word about very-long-baseline interferometry: if it is known that the astronomical object under observation contains a bright, pointlike source in or near itself, it is possible to completely reconstruct a map of the original source. The bright spot acts as a phase reference for the radio astronomers. In fact, what they're reconstructing is just a Fourier-transform hologram—but on a galactic scale!

Further Work

After a program is written, it's always possible (and sometimes profitable) to go back and see how it could have been done differently, and perhaps better. The 2DFT program is no exception; I have several ideas for improvements and modifications, some of which you may wish to try. First, now that I know not to be afraid of cutting off parts of the holographic image, I've wondered whether a 64- by 64-cell transform would be the best step up. Since the dimensions are powers of two, it would be possible to use the fast-Fourier-transform algorithm and save time by at least a factor of 6 (the logarithm of 64 to the base 2) over the slow method. I also think that it might be worthwhile to use fewer bits during the transform, since overflows haven't been as deadly as I feared before starting the project. Perhaps integer arithmetic with 1 or 2 bytes for the numbers would work; it would certainly save space and time over the 5-byte floating-point methods that are used by the PET's firmware algorithms. (BASIC integer operations on the PET are actually done almost entirely in floating-point arithmetic; the only benefit of integers that I know of is to save memory in large arrays.)

I've seen comments about 1-bit Fourier transforms in some references. If that is a reasonable technique, you could use the ¼-cell graphics capabilities of the PET screen to display 50- by 80-pixel transformed images.

Finally, there must be a better way to find the amplitude of the transformed data than to take the square root of the sum of the squares of the sine and cosine parts. (The PET's floating-point square-root algorithm simply raises the argument to the ½ power, by taking a logarithm, multiplying, and exponentiating. It's not overly fast!) Perhaps a little table lookup could get a fast square root with sufficient accuracy for display purposes.

There are surely other improvements to be made on 2DFT. But as it is, it has provided me with a powerful learning tool. I've developed a more intuitive understanding of holography and the Fourier-transform process than I ever had before...and it's been fun! I hope you enjoy it as much. ■

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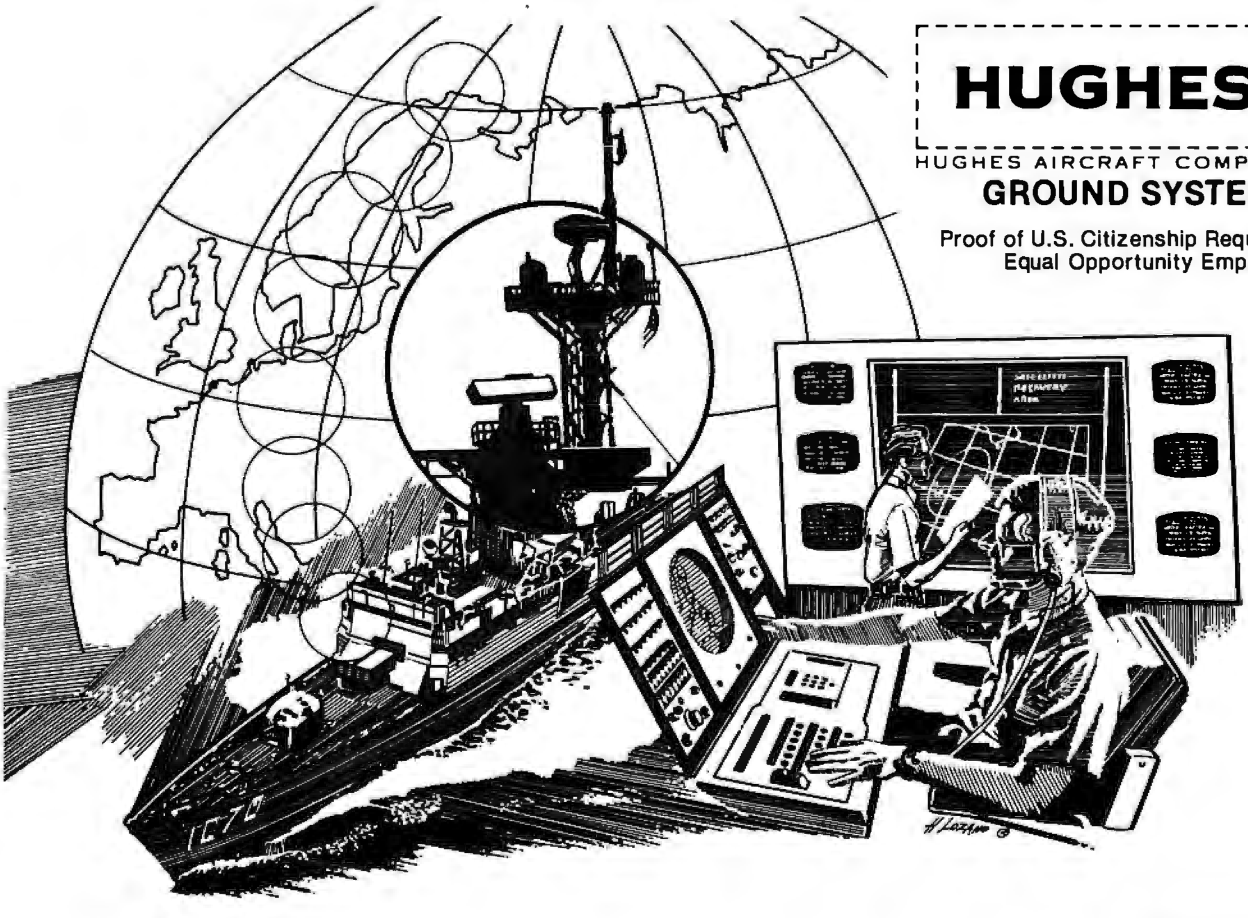

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"It looks like too much trouble": Most of the things you'll need to do are easy and make sense. After a while, they will become so natural that you'll wonder how you ever did without them.

"I don't have the time to spare—I'm on a tight deadline": You have time to debug, don't you? And you have time to fix that bug that appears six months after you wrote the program. Actually, the techniques of design (which include structured programming during the program design and implementation) take up less time due to decreased time in testing, debugging, and maintenance. In fact, what you're doing is spending more time in design (doing it right) and less time in testing and debugging (finding and fixing what you didn't do right the first time).

"It takes all the fun (or mystery) out of programming": This is a difficult question to answer because there's an element of truth in it. But what do you mean by "fun"? If you mean surprises or adventure, you're right—there's less of that because you know more of what is going to happen before you start coding; on the other hand, there's less frustrating debugging. There's less exultation when a program *finally* works—but there's also quite a bit of pride in the knowledge that it will *stay* working. Proper design takes some of the mystery out of programming. Programming becomes a skill, but it is *designing* that becomes the art.

Finally, if you are programming for a living, haphazard programming may be "fun," but can you *afford* such fun? Untraceable bugs and unreliable programs decrease your productivity and your effectiveness. Can you and your company afford that?

Some Design Tools

The following briefly describes three design tools that have been available for at least five years. *Data flow diagrams* (DFDs) are usually used on large projects, although they can help clarify your thinking on simpler ones. They force you to clarify what information is being manipulated and how it "flows" through the project. On a level of design several steps closer to coding, *structure*

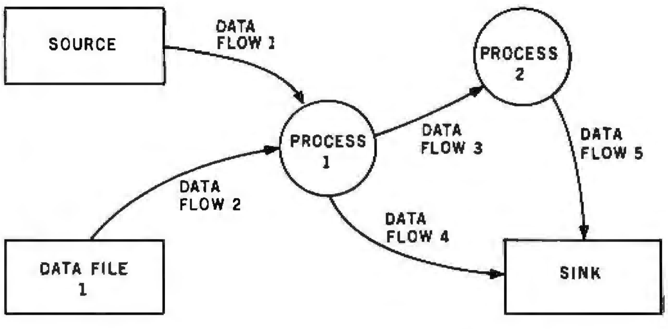

Figure 2: *An example of a data flow diagram (DFD). The circles represent processes (or actions) we are interested in within a system. The boxes represent external systems. The parallel lines represent data files (often called* data stores*), and the lines represent groupings of data that are transformed by the process.*

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charts are hierarchical models of a system that emphasize the tasks and subtasks to be performed and the data that passes among them. Finally, on the lowest level of design before coding, *structured pseudocode* is an informal English-like coding that allows you to experiment with implementing the logic of a program without being bothered with the narrow grammar of a particular computer language. Although I'll give an example and a short explanation of each method, you should refer to some of the books described at the end of this editorial for further details.

An example of a *data flow diagram* is given in figure 2. The circles represent processes we are interested in (actions being performed, *not* states of the system), and the arrows represent some grouping of data that is being transferred from one activity to another. The rectangular boxes represent other systems that interact with our systems but that are not of interest to us. If the arrows lead out of these boxes, they are called *sources*; if the arrows lead in, they are called *sinks*. The two parallel lines represent data files (also called "data stores") that store information for later use; depending on the file, arrows may go in both directions.

Data flow diagrams are usually used in groups, with one diagram representing the interaction of the system with external systems (one circle interacting with several boxes) and each of the other diagrams representing one circle from a "higher" diagram. For example, figure 3a shows an overview DFD of (a simplified version) the interaction between the BYTE editorial department and the rest of the world. Figure 3b shows an expansion of the single circle in figure 3a. Further data flow diagrams can be used (if needed) to subdivide a given process.

When a set of DFDs covers several levels, the circles in the subordinate diagram reflect the identity of the parent circle. For example, the processes (circles) in a diagram representing process 1 of figure 3b ("log in and schedule manuscripts") would be numbered 1.1, 1.2, 1.3, and so on; similarly, subordinate processes of 1.3 would be labeled 1.3.1, 1.3.2, 1.3.3, and so on.

A data flow diagram is useful only when it meets certain criteria. Although I can't give all the dos and don'ts, the following points are helpful: First, take care that circles represent *meaningful* data transformations and arrows represent *meaningful* collections of data. For example, "read card deck" is not a meaningful transformation, but "classify incoming orders" is.

Second, with one exception, the inputs and outputs to a given diagram must be the same as those for the single process the diagram represents in the next higher diagram. This rule makes sense, and checking diagrams for compliance often alerts you to some data flow you've ignored. The one exception to this rule is that arrows for rejected data on one level are not shown in the next higher level (for example, see "manuscripts with no name or return address" coming out of process 1 in figure 3b); the reason for this convention is to avoid cluttering up the diagrams.

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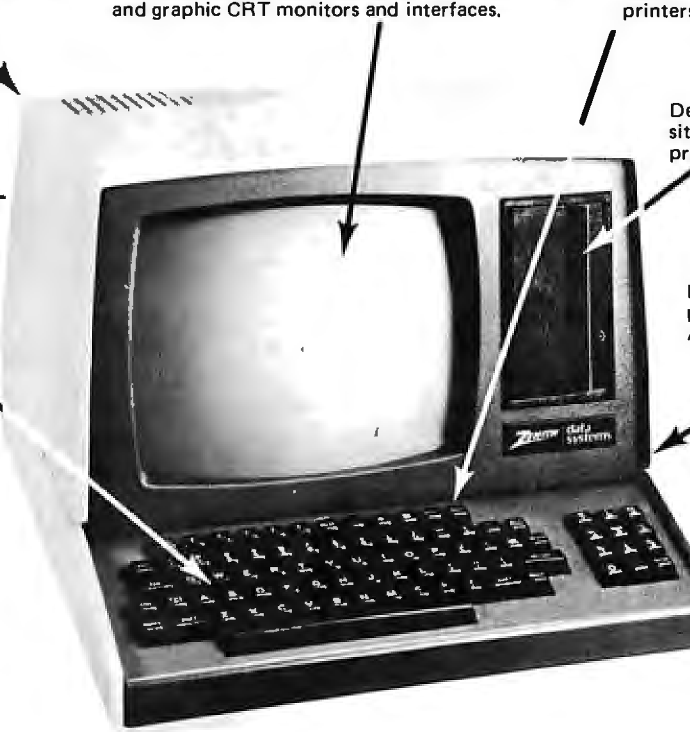

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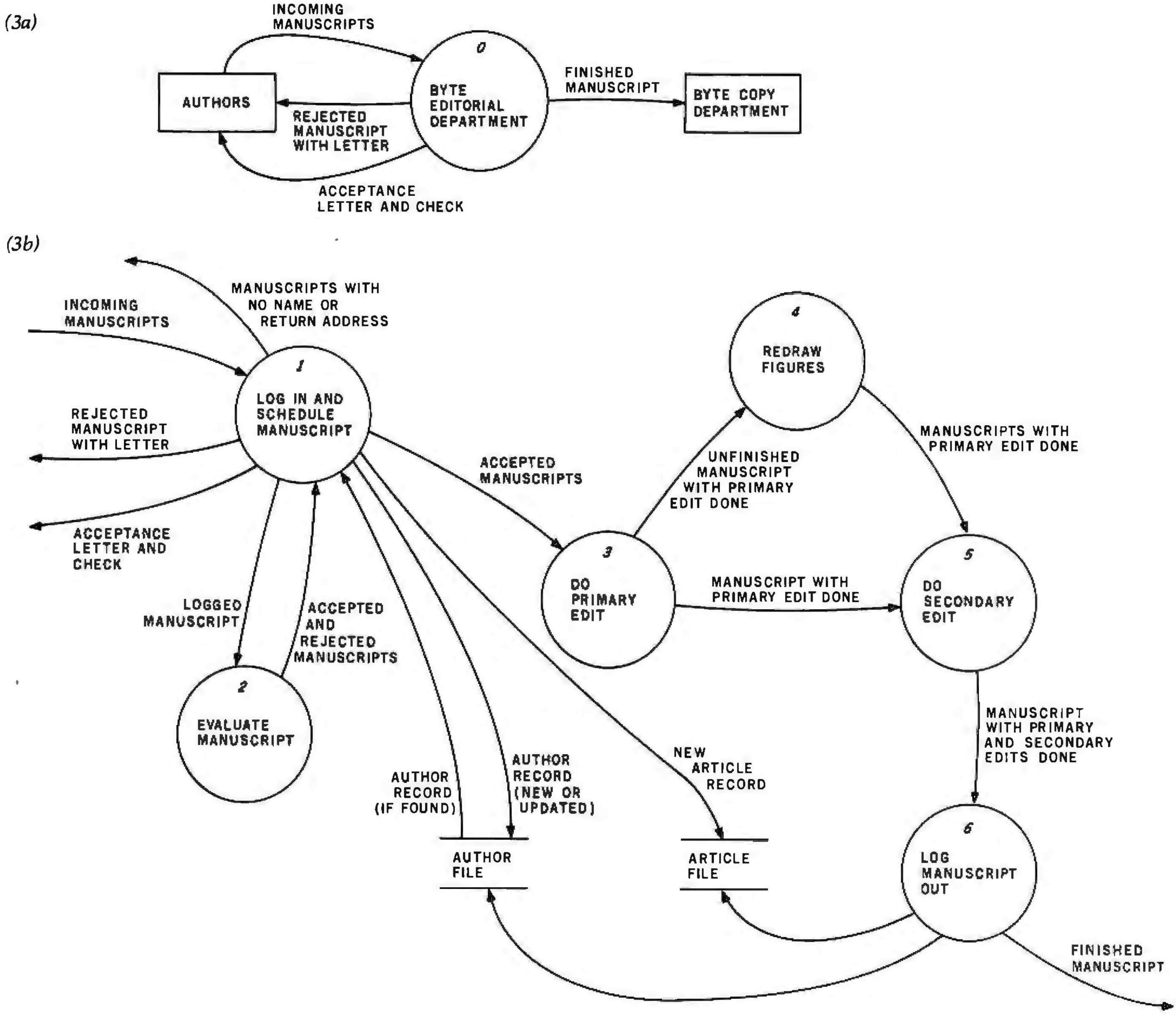

Figure 3: *Overview and detailed data flow diagrams. Figure 3a shows an overview data flow diagram of the interaction of the BYTE editorial office with the rest of the world. Figure 3b is a detailed data flow diagram showing the workings of circle 0 in figure 3a. (The system shown has been simplified for purposes of illustration.)*

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Third, data flow diagrams should show the logical flow of data, not its physical flow in an existing system—*a DFD is not a flowchart.* For example, circle 1 in figure 3b should not be labeled "Karen," even though she logs all incoming manuscripts.

In conclusion, the data flow diagram is a planning tool used in the early stages of design. It can clarify the flow of data in either an existing or a proposed system. You'll probably draft many versions of a data flow diagram before you arrive at a satisfactory version—this is a normal and unavoidable consequence of your increased understanding of the system and the improvements you are making in its design.

It's particularly important to use data flow diagrams when you are working for someone other than yourself (for example, a partner or client) because DFDs give you an easily understood document from which the other person can contribute *at an early stage in the design process.* This early feedback can often prevent costly backtracking in the later stages of system implementation.

The Structure Chart

Structure charts are used later in the design process, when you know what a system (or program) is to do but want to organize the design and interaction of modules. Structure charts can be used to design either a single program or a system of programs; if you are designing a system, a finished structure chart will suggest logical ways in which to group the modules of the system into programs.

In a structure chart (see figure 4), rectangular boxes represent modules that perform a given action. The organization of the modules is determined by the arrows interconnecting them; the one being pointed to is *used by* the one doing the pointing to carry out its task. The modules communicate in much the same way as people do in a military hierarchy: the higher (calling) modules are organizers, sending orders to the ones below; the lower (called) modules are workers, performing their tasks (often calling modules that they command) and reporting back to their superiors. However, in this situation, it is the data that is transmitted up and down between modules. The structure chart records this movement. The arrow that begins with an outline circle represents data being passed (eg: an employee record, a part number), and an arrow beginning with a filled-in circle represents a logical flag (eg: transaction-valid or invalid-account-number flag).

Figure 5 is an example of a structure chart at work. The task being illustrated (top box) is the writing of an (imaginary) order for a final article payment to a BYTE author. Note that the data can pass both up and down, depending on the situation, but that logical flags almost always pass yes/no-type control information *up* to a calling module. The vertical lines on the box "get valid article record" (in the second row of figure 5) indicate that it is a library module that can be used as is from an existing library of routines.

A structure chart shows the subdivision of a system into modules, the hierarchy of those modules, and the data that passes among them. It does *not* imply anything about the method used to implement a module, nor does it imply a left-to-right execution sequence for modules on the same row. Again, the main benefit of structure charts is the clarity of design they produce. Creating the structure chart forces you to be precise about what needs to be done. Once completed, the structure chart gives you the opportunity to find logical design flaws and to check for overall completeness. As with the data flow diagram, you'll probably write several versions of the structure chart before you get one that will satisfy you; but, in doing so, you'll create a design that will lead to a much better system or program.

Structured Pseudocode

Structured pseudocode is used only after you've passed the boundary from system design to program design. By the time you're ready to use structured pseudocode, you have already specified the function of the program and some of its implementation details. Writing structured pseudocode is like writing a program for an imaginary machine that understands English-like phrases; it is a "test run" for the real thing, coding the actual program in the strict grammar of BASIC, FORTRAN, or some other computer language. Structured pseudocode tells *what* is to be done, the *order* it is done in, and *how* it is done. Once the structured pseudocode has been written, studied, and rewritten to your satisfaction, you can easily code your computer program from the pseudocode.

Listing 1 gives a short example. The hypothetical task is to find the lump-sum payment for an article from a lookup table, given the classification number of the desired article (which is the key field of the lookup table). We'll assume that the lookup table has two fields, a classification number and a payment amount, and that a sequential search of the table is made to find the appropriate line.

Listing 1 shows what's being done more clearly than an equivalent BASIC (or even Pascal) program because it's not concerned with rigorously expressing the algorithm in the narrow (and therefore less meaningful) grammar of the computer language. Still, since the pseudocode follows (or should be written to follow) the style of the target language, writing the actual program is simply a matter of expanding the lines of pseudocodes to take care of all the necessary details. For more information on con-

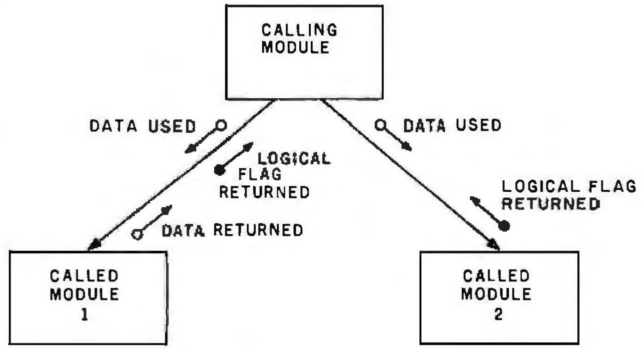

Figure 4: *An example of a structure chart. The boxes represent modules that perform specified actions, with the higher boxes pointing to the subordinate boxes that they use. An arrow with an outline circle represents a grouping of data, while an arrow with a filled circle represents a logical flag that transmits the results of some yes/no-type evaluation.*

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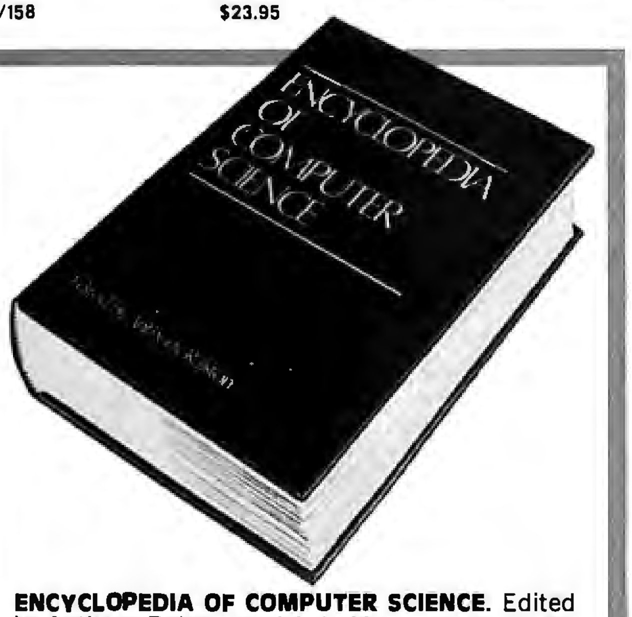

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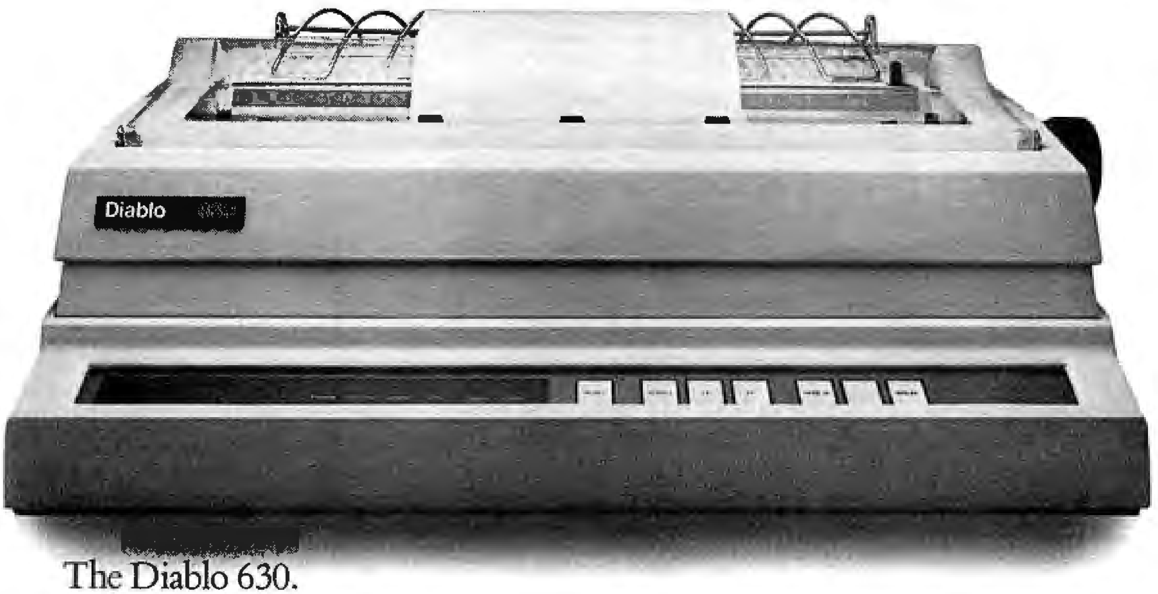

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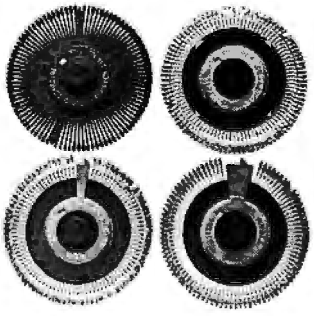

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At this point I'd like to break my earlier promise and say a few good words about structured programming, which is the design philosophy behind structured pseudocode. Structured programming asserts that any program can be written as a combination of three programming structures: a sequence of events, one of two events chosen by the value of a condition (the *if...then...else* construct), and an event repeated as long as a condition is true (the *while...do* construct). Structured programming goes hand-in-hand with *top-down design* (also called *programming by stepwise refinement*), which says that you solve a programming problem by breaking it into subproblems and continually subdivide these subproblems until each one can be easily coded. This process results in manageable, modular programs that are easy to understand, debug, modify, and maintain. The importance of such advantages cannot be overemphasized, especially if you program for a living.

Some Good Books

You will find the following books helpful if you're interested in structured programming, program design, or system design. The first books deal primarily with structured programming and program design, while the latter ones go deeper into long-range design.

Programming Proverbs by Henry F Ledgard (Hayden Book Company, Rochelle Park NJ, 1975): This is a friendly, but thorough, folk classic on methodical programming. It contains 26 proverbs with examples and some additional material on top-down design, and it can be read and understood by almost everyone with some programming experience. The languages used in the examples are ALGOL 60 and PL/I. The author, along with several coauthors, has tailored the same material for different books that emphasize FORTRAN, COBOL, BASIC, and Pascal. The titles are: *FORTRAN (or COBOL or BASIC or Pascal) with Style: Programming Proverbs.* All are published by Hayden Book Company.

The Elements of Programming Style, Second Edition by Brian W Kernighan and P J Plauger (McGraw-Hill, New York NY, 1978): Written in the style of Strunk and White's *Elements of Style* (the English language style book), it is slightly more formal and not as folksy as *Programming Proverbs.* It covers its material more methodically than *Programming Proverbs* does.

A Collection of Programming Problems and Techniques, by H A Maurer and M R Williams (Prentice-Hall, Englewood Cliffs NJ, 1972): I've always enjoyed leafing through this book because of all the tidbits of information it possesses. It includes such diverse information as the Ackermann function, algorithms involved with reverse Polish notation, and information on generating magic squares and solving simultaneous equations by the Gauss-Seidel method. An excellent book for problem ideas if you're teaching programming or need a short, nontrivial problem to illustrate a point.

Software Debugging for Microcomputers, by Robert C Bruce (Reston Publishing Co, Reston VA, 1980):

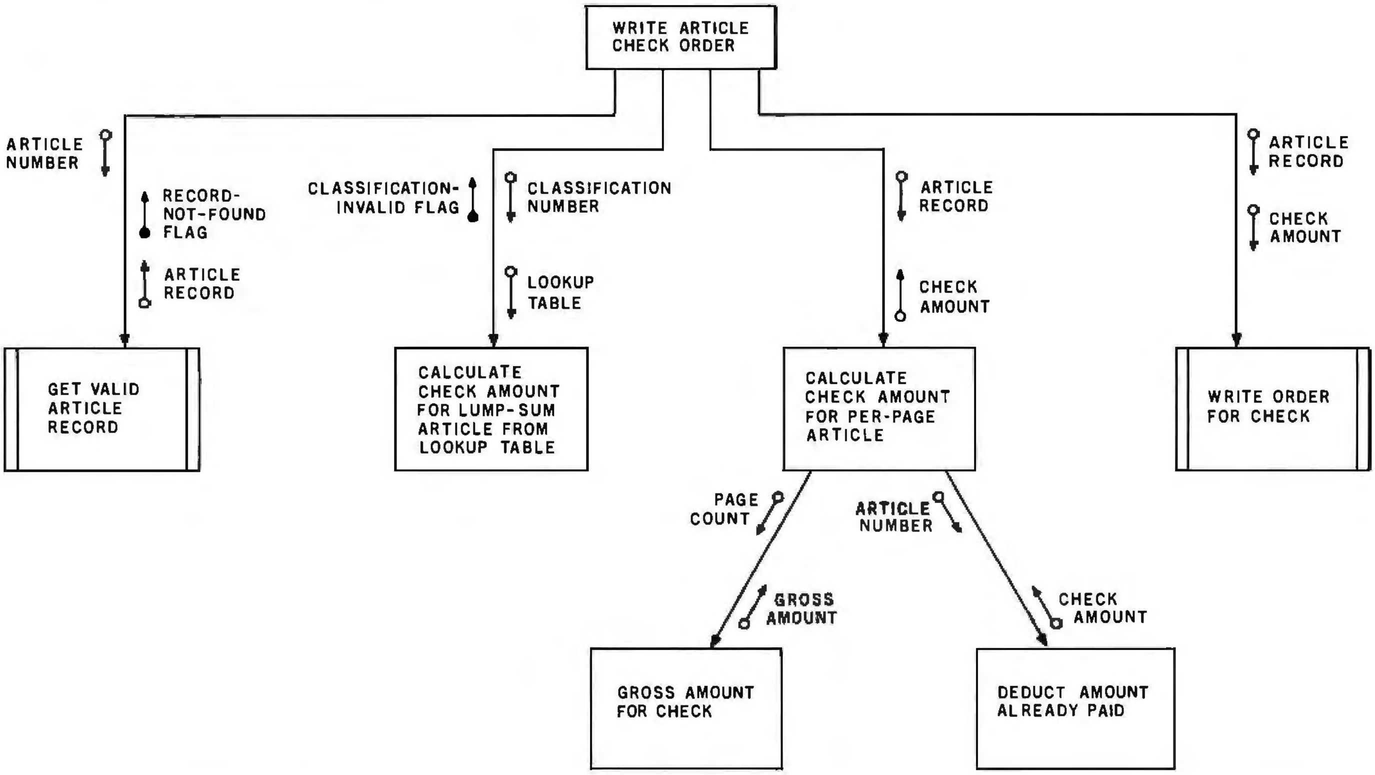


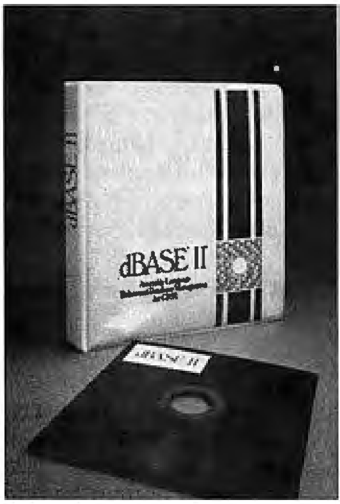
Figure 5: *Another example of a structure chart. The (hypothetical) action illustrated is the generation of an order for a check for final payment to a BYTE author for an article. The vertical bars on the first and last boxes in the middle row represent predefined modules that can be used in different situations.*

dBASE™ II vs. the Bilge Pumps.

by Hal Pawluk

We all know that bilge pumps suck.

And by now, we've found out—the hard way—that a lot of software seems to work the same way.



So I got pretty excited when I ran across **dBASE II**, an assembly-language relational Database Management System for CP/M. It works! And even a rank beginner like myself got it up and running the first time I sat down with it.

If you're looking for software to deal with your data, too, here are some tips that will help:

Tip #1: Database Management vs. File Handling:

Any list or collection of data is, loosely, a data base, but most of those "data base management" articles in the buzzbooks are really about file handling programs for specific applications. A real Database Management System gives you data and program independence (no reprogramming when data changes), eliminates data duplication and makes it easy to turn data into information.

Tip #2: Assembly Language vs. BASIC:

This one's easy: if you're setting up a DBMS, you're going to be doing a lot of sorting, and Basic sorts are s-l-o-w. Run a benchmark on a Basic system like S*-IV against a relational DBMS like **dBASE II** and you'll see what I mean. (But watch it: I've also seen one extremely slow assembly-language file management system.)

Tip #3: Relational vs. Hierarchal & Network DBMS.

CODASYL-like hierarchal and network systems, around since the 1960's, are being phased out on the big machines so why get stuck with an old-fashioned system for your micro? A relational DBMS like **dBASE II** eliminates the predefined sets, pointers and complex data structures of a CODASYL-type DBMS. And you don't need to be a programmer to use it.

dBASE II vs. everything else.

dBASE II really impressed me.

Written in assembly language (with no need for a host language), it handles up to 65,000 records (up to 32 fields and 1000 bytes each), stores numeric data as packed strings so there are no round-off errors, has a super-fast multiple-key sort, and supports ISAM based on B* trees.

You can use it interactively with English-like commands (DISPLAY 10 PRODUCTS), or program it (so when you've set up the formats, your secretary can do the work). Its report generator and user-definable full screen operations mean that you can even use your existing forms.

And if all this makes your mouth water, but you've already got all your data on a disk, that's okay: **dBASE II** reads your ASCII files and adds the data to its own database.

Right now, I'm using **dBASE II** with my word processor for budgeting, scheduling and preparing reports for my clients.

Next come job costing, time billing and accounting.

An Unheard-of Money-Back Guarantee.

dBASE II is the first software I've seen with a full money-back guarantee.

To check it out, just send $700 (plus tax in California) to Ashton-Tate, 3600 Wilshire Blvd., Suite 1510, Los Angeles, CA 90010. (213) 666-4409. Test **dBASE II** doing your jobs on your computer for 30 days. If, for some strange reason, you don't want to keep it, send it back and they'll refund your money.

No questions asked.

They know you don't need your bilge pumped.

Ashton-Tate

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Although this book has little to do with structured programming or design, I mention it because of its thorough treatment of debugging techniques. If you're interested in such debugging techniques as forcing, block debugging, snapshots, and patching, you should read this book.

Listing 1: *Structured pseudocode for a routine to find a value from a lookup table. The lookup table contains two fields, classification-number and check-amount, and this routine finds the appropriate check-amount by matching a given classification number to the classification numbers in the table. A sequential search is used, starting at the top of the table. If a classification-number match is made, the check-amount needed is the check-amount entry in the same line, and the error-flag (for the information of the calling routine) is cleared. If no match is made, check-amount is set to zero and the error-flag is set.*

```
while not-at-end-of-file and match-not-found
  compare classification number of current line with classification
  number sought
  if the two are equal
      check-amount sought is check-amount field in current line
    else
      add 1 to table-index
    endif
endwhile
if no-match-found
    set error-flag
  else
    check-amount = 0
    clear error-flag
endif
return (to calling routine)
```

Program Design: Programming Techniques, Volume I, edited by Blaise W Liffick (BYTE Books, Peterborough NH, 1978): This book contains new material and articles reprinted from BYTE. Subjects include "Top-Down Modular Programming;" "Some Words About Program Structure" (both by Albert D Hearn); "Applied Structured Programming" (by me); "Decision Tables: How to Plan Your Programs" (by Thomas G Bohon), and several other helpful articles. My only regret is that several articles include what are called 'Warnier-Orr diagrams," a program design technique I do not recommend.

A Primer on Structured Program Design, by Gary L Richardson, Charles W Butler, and John D Tomlinson (Petrocelli Books, New York NY, 1980): This book covers structured programming and program design, but it also touches on the larger elements of system design. One nice feature is that it briefly lists several different design tools in order to help you choose the one you like best.

Classics in Software Engineering, edited by Edward Nash Yourdon (Yourdon Press, New York NY, 1979): I cannot say enough good things about this book. It is a compilation of all the pivotal papers in the fields of structured programming (both theory and practice), program and system design, and other related fields. Not only is it extremely convenient to have these articles gathered together, it's also the only way most people will ever see them (since many of the articles appeared in the proceedings of computer conferences as many as 15 years ago). By reading the articles (and the excellent introduc-

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tions to each article, written by Mr Yourdon), you can see how the key ideas in the field formed and grew. The highly theoretical article, "Flow Diagrams, Turing Machines, and Languages with Only Two Formation Rules," by C Bohm and G Jacopini, contains the theoretical rigorous proof that *any* program can be written using only sequence, choice (*if...then...else*), and iteration (*while...do*). Although I don't have the room to list all the articles in this 424-page book (most of which are remarkable in some way), I must mention "The Humble Programmer," by Edsger Dijkstra; "Revolution in Programming: An Overview," by Daniel McCracken, and the monumental "Structured Programming with go to Statements," by Donald Knuth.

The Practical Guide to Structured Systems Design, by Meilir Page-Jones (Yourdon Press, New York NY, 1980): This is a very readable book explaining the latest design techniques. I enjoyed reading it, and I referred to it constantly while writing this editorial. It covers the three techniques discussed above, as well as several I didn't have room for (the concept of a "data dictionary," for one), and it is greatly enhanced by the inclusion of a complete case study of a system designed using the methods given in the book. The book concentrates on the *design* process and talks only briefly of structured programming and program design. Also, it presents much the same material as the next two books (which come before it chronologically), with a slight reduction in complexity and a slight increase in readability. I recommend that you read this book first.

Structured Analysis and System Specification by Tom DeMarco (Prentice-Hall, Englewood Cliffs NJ, 1979): This book covers much the same material as the preceding book, but it treats the subjects covered more rigorously and a bit more formally. It also addresses the special problem of modeling and designing very large systems that don't yet exist.

Structured Design: Fundamentals of a Discipline of Computer Program and Systems Design, by Edward Yourdon and Larry C Constantine (Prentice-Hall, Englewood Cliffs NJ, 1979): This book is the parent of the two just described (the first publication of this book was in 1975, and the authors of all three books come from the same school of design). Because it was written to describe its design techniqes for the first time, the notation used is a bit cluttered (compared to the streamlined design used in the last two books), but this book is easily the most comprehensive and the most theoretical; it attacks the problem of program design on the broadest level. Particularly important are the ideas of *coupling* and *cohesion* among program modules, each of which have separate chapters in the book.

Conclusions

If I had to give you one word to associate with the concept of design, that word would be *forethought*. Design *is* forethought—it's as simple as that. Few people would say that they program without forethought, but programming at the keyboard (or with a coding sheet) without design is the same as playing the piano without sheet music— more improvisation than rendition. So the question is no longer, "Is this really necessary?" It's "can you afford not to?"■

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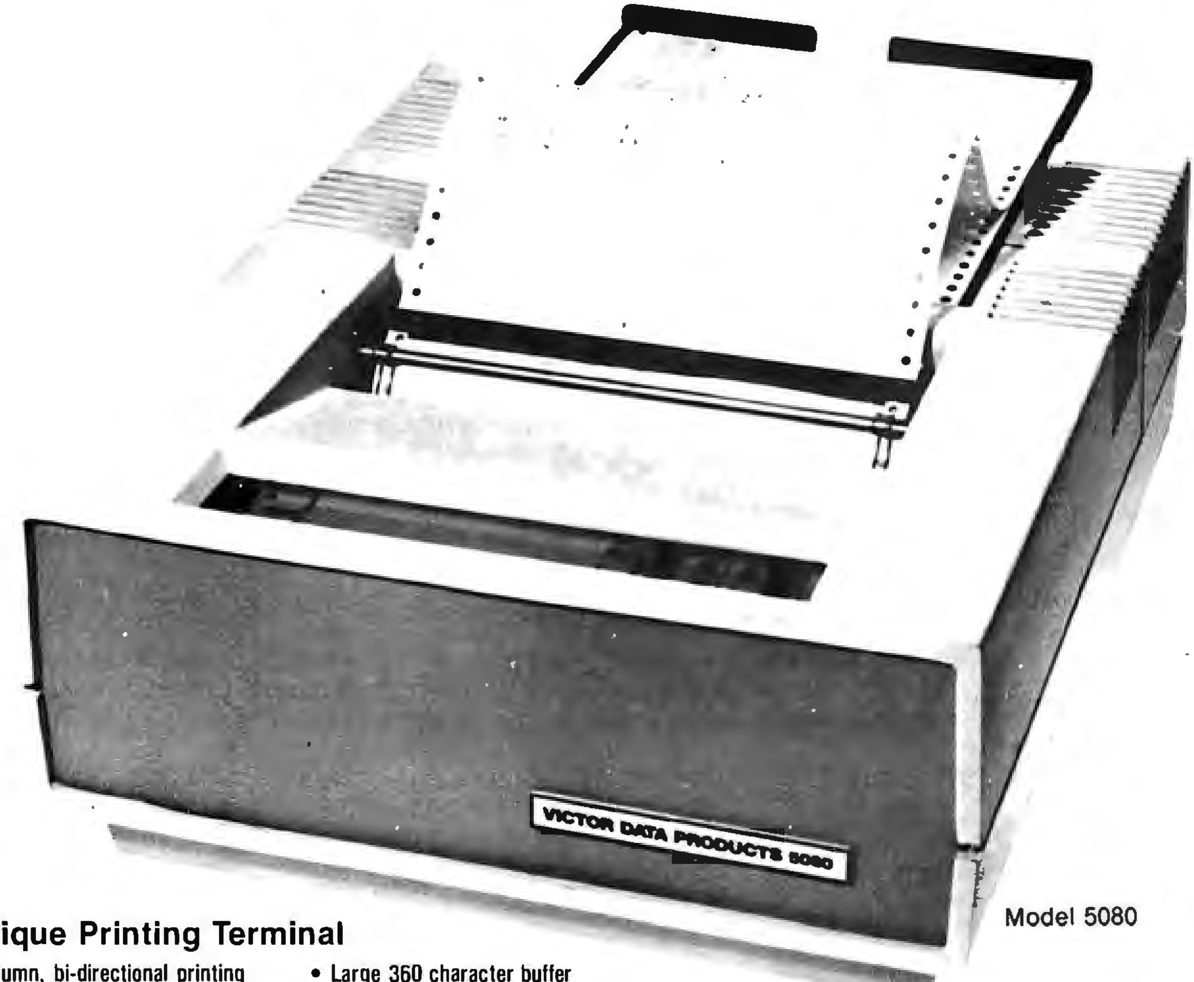

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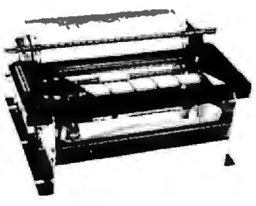

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DATALINE

Daniel S Hunt, 829 Presidio Dr, Costa Mesa CA 92626

There is a certain pleasure in writing assembly-language subroutines for my Microsoft BASIC system; however, the dismal tedium involved in hand-converting object code into BASIC data statements is unmatched.

There are alternatives: one method is to put the object code into a data file and read it into memory for execution by the program. The disadvantage with this method is that one must keep a separate file for what is in essence a subroutine. Besides, the file may be lost in a backup operation or during insouciant copying of the BASIC code to another disk.

My solution for this problem was to write DATALINE. DATALINE is a BASIC program that takes freshly assembled object code and moves it into DATA statements so that the code can be integrated with the BASIC mainline source code.

This program assumes that you are able to move object code into a memory area protected from BASIC. If you do not have the ability to move blocks of object code in this way, the concatenation routine can be joined with an algorithm to read a .COM file character by character.

To use DATALINE, load the object code into an area protected from BASIC. The program will prompt you for the load address, length of the program in 64-byte segments, a file name, and a starting line number. It peeks the object code byte by byte and concatenates a string conversion of each byte to a line composed of line number, " DATA ", plus appropriate spaces and commas between each byte value. Eight bytes are put on each data line. The line is filed serially, and it appears to BASIC to be a program file saved in "A" mode. You can merge the data lines with your BASIC program by using the MBASIC MERGE command.

This program includes one of my most used library routines. This is a procedure that takes a hexadecimal-value input at the keyboard and converts it to decimal representation which can be used in PEEK and POKE statements. As the MBASIC 5.1 interpreter is intolerant of integer overflow, the conversion is to single-precision floating-point base 10, rather than integer. While integer conversion is possible, the extra speed gained in the exercise is not worth the extra code or the increased complexity.

If your BASIC is an older version of Microsoft, merely reduce the length of the variable names where your interpreter rejects one here.

Listing 1: *Written in Microsoft BASIC, this short routine takes the drudgery out of writing assembly-language subroutines for BASIC programs. The program rewrites object code as BASIC DATA statements, as shown in listing 2.*

```
10 REM *** MBASIC DATALINE WRITER ***
100 '
110 '------------------------------------------------------------------------
120 '        Written by Daniel S. Hunt, April 25, 1980
130 '             MBASIC 5.1 INTERPRETER / Sol-20
140 '------------------------------------------------------------------------
150 WIDTH 64
160 PERSE = &HCOD5 : 'SOLOS CLEAR SCREEN CALL
170 CALL PERSE:PRINT:PRINT
180 PRINT "--- MACHINE CODE / DATA LINE WRITER ---":PRINT
190 INPUT "Enter hex base address of oject code ",HXIN$
200     GOSUB 350 :' CONVERT HEX STRING TO REAL DEC.
210     DBASE = BASETEN
220 INPUT "Routine length in 64-byte segments ",PAGES :
        LENGTH = PAGES * 64
230 INPUT "Enter name of data statement file ",DFILE$
240     OPEN "0",1,DFILE$
250 INPUT "Enter line number of starting data statement ",LNUM
260 LASTBYTE = DBASE + (LENGTH -1)
280 GOSUB 570 :'CREATE DATA LINES
290 CLOSE
310 '
320 '
330 REM --- CONVERTS HEX INPUT STRING TO DECIMAL ---
340 '
350   CUME = 0
360   HDAT$ = "0123456789ABCDEF"
370   CHARPOS% = LEN(HXIN$)
380   FOR I% = 1 TO LEN(HXIN$)
390     ADDER =0
400     FOR J% = 1 TO LEN(HDAT$)
410       IF MID$(HXIN$,I%,1) = MID$(HDAT$,J%,1)THEN
            ADDER = J% - 1
```

Listing 1 continued on page 218

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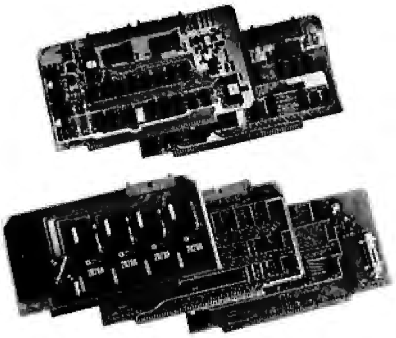

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Listing 1 continued:

```
420      NEXT
430      ' { CASE CHARPOS% OF }
440        IF CHARPOS% = 4 THEN
             CUME = CUME + (ADDER * 4096)
450        IF CHARPOS% = 3 THEN
             CUME = CUME + (ADDER * 256)
460        IF CHARPOS% = 2 THEN
             CUME = CUME + (ADDER *  16)
470        IF CHARPOS% = 1 THEN
             CUME = CUME + ADDER
480      ' { END CASE }
490      CHARPOS% = CHARPOS% - 1
500    NEXT
510    BASETEN = CUME
520   RETURN
530 '
540 '
550 '---CONVERTS OBJECT CODE TO BASIC DATA LINES---
560 '
570   FOR I = DBASE TO LASTBYTE STEP 8
580    LNUM$ = STR$(LNUM) + " "
590    DATL$ = LNUM$ + "DATA "
600     FOR J = 0 TO 7
610        BYTE = PEEK(I+J)
620 '
630        IF J = 7 THEN
             BYTE$ = STR$(BYTE)
            ELSE
             BYTE$ = STR$(BYTE) +"" + CHR$(44) + ""
640 '
650        DATL$ = DATL$ + BYTE$
660     NEXT
670     PRINT DATL$ :' TO CRT
680     PRINT #1, DATL$ :' TO FILE
690     LNUM = LNUM + 10
700   NEXT
710   RETURN
999   END
```

Listing 2: *A "verification run" of DATALINE in a CP/M operating-system environment shows that assembly-language object code is converted into DATA statements for embedding in a BASIC program.*

```
A>asm qtab.aax
CP/M ASSEMBLER — VER 1.0

            ; ROUTINE TO INITIALIZE TAB STOPS ON QUME
            ;
            ;         ASEG
            ;****** DECLARATIONS ***********
9000 =        CACHE      EQU          9000H    ; ROUTINE ORIGIN
00F8 =        SERSTAT    EQU           0F8H
00F9 =        SERDAT     EQU           0F9H
0040 =        SDR        EQU            40H
0080 =        STBE       EQU            80H
001B =        ESC        EQU            27D
0020 =        SPC        EQU            32D
000D =        CR         EQU            13D
000A =        LF         EQU            10D
0009 =        HT         EQU            09H
0001 =        ONE        EQU            01H
000F =        SI         EQU            15D
000E =        SO         EQU            14D
000A =        NUMTBS     EQU            10D
              ;
9000                     ORG          CACHE
            ;
            ;BEGIN MAIN PROGRAM**********************
            INIT:
9000 210000          LXI    H,0000H     ;ZERO REGISTER SO THAT
9003 39              DAD    SP          ;VALUE PASSED TO H = SPC
                                        SETTING
9004 226890          SHLD   OLDSTK      ;SAVE OLD STACK POINTER
                                        ADDRESS
```

Listing 2 continued on page 222

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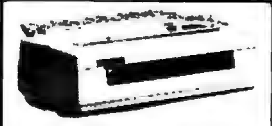

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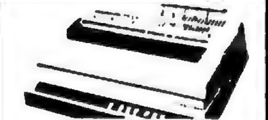

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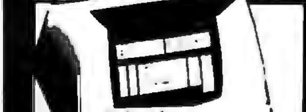

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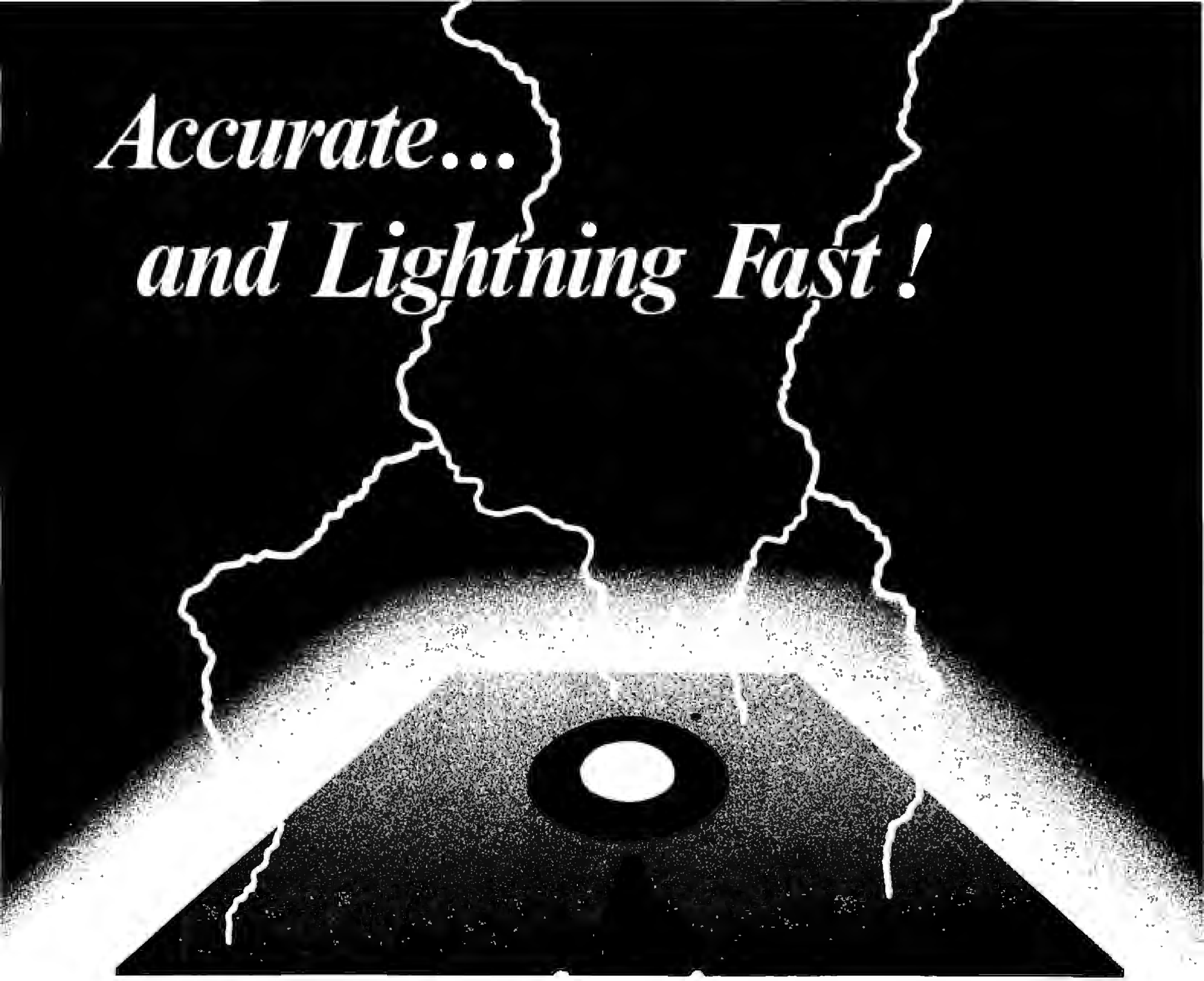

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900A 215190      LXI     H,PMODE     ;THIS PUTS QUME IN PRO-
                                     GRAM MODE
900D CD4190      CALL    SCAN        ;READ SERIES LINE AND SEND
                                     IT
            ;
            TAB0:  ;ACTUAL MESSAGE LOAD BEGINS HERE
9010 B7          ORA     A           ;CLEAR FLAGS
9011 1E0A        MVI     E,NUMTBS    ;SETS FOR CARRIAGE WIDTH
            TAB1:
9013 215790      LXI     H,TAB8SP
9016 CD4190      CALL    SCAN
9019 216090      LXI     H,SETTAB
901C CD4190      CALL


A>asm qtab.aaz
CP/M ASSEMBLER — VER 1.0

907A
003H USE FACTOR
END OF ASSEMBLY

A>type qtab.hex
:109000002100003922689031 7A90215190CD419011
:10901000B71E0A215790CD4190216090CD41901DFF
:10902000C21390215490CD4190216390CD41903155
:109030006890C30000DBF8E680CA3590C979D3F99F
:10904000C9B77EFE24C84FCD3590CD3D9023C34196
:109050009 01B0E241B0F242020202020202024C1
:069060001B31240D0A245F
:0090000070

A>ddt qtab.hex
SID VERS 1.4
NEXT  PC   END
9066  9000  677F
#g0


A>b:
B>basic dataline
BASIC Rev. 5.1
[CP/M Version]
Copyright 1977, 78, 79, 80 (C) by Microsoft

Created: 14-Jan-80
5595 Bytes free

---MACHINE CODE / DATA LINE WRITER---

Enter hex base address of object code 9000
Routine length in 64-byte segments 2
Enter name of data statement file bytes.dat
Enter line number of starting data statement 5000
   5000 DATA 33, 0, 0, 57, 34, 104, 144, 49
   5010 DATA 122, 144, 33, 81, 144, 205, 65, 144
   5020 DATA 183, 30, 10, 33, 87, 144, 205, 65
   5030 DATA 144, 33, 96, 144, 205, 65, 144, 29
   5040 DATA 194, 19, 144, 33, 84, 144, 205, 65
   5050 DATA 144, 33, 99, 144, 205, 65, 144, 49
   5060 DATA 104, 144, 195, 0, 0, 219, 248, 230
   5070 DATA 128, 202, 53, 144, 201, 121, 211, 249
   5080 DATA 201, 183, 126, 254, 36, 200, 79, 205
   5090 DATA 53, 144, 205, 61, 144, 35, 195, 65
   5100 DATA 144, 27, 14, 36, 27, 15, 36, 32
   5110 DATA 32, 32, 32, 32, 32, 32, 32, 36
   5120 DATA 27, 49, 36, 13, 10, 36, 0, 0
   5130 DATA 0, 0, 0, 0, 0, 0, 0, 0
   5140 DATA 0, 0, 0, 0, 0, 0, 0, 0
   5150 DATA 0, 0, 0, 0, 0, 0, 0, 0
Ok■
```

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Technical Forum

Addition and Subtraction: The 1802 Versus the Z80

Stephen Merrin, 4470 NW Alpha Pl, Apt 6, Corvallis OR 97330

Binary arithmetic is inherently simple because it involves only 0s and 1s. But recently, while I was trying to understand the instruction sets of two very different microprocessors, the 1802 and the Z80, I became confused when examining addition and subtraction operations. The confusion arose primarily over the notion of "borrow" in subtraction.

When you perform multiple-byte additions and subtractions, instructions like ADD WITH CARRY and SUBTRACT WITH BORROW (CARRY) are needed. In the *1802 User Manual* the instruction SUBTRACT MEMORY WITH BORROW is defined as performing the following:

$$D - M(R(X)) - (NOT\ DF) \rightarrow DF,D$$

Here, 8-bit arithmetic is being performed. DF is the borrow (carry) bit and M(R(X)) and D are 8-bit operands. On the other hand, in the Z80, you have the instruction SBC s, SUBTRACT WITH CARRY, which accomplishes:

$$A \leftarrow A - s - CY$$

This operation involves the 8-bit operands A and s, and CY is the borrow (carry) bit.

If you are a programmer at the assembly- or machine-language level, you are aware that ambiguity in the description of the instruction set cannot be tolerated. You need to know such things as: Is the 1802 DF bit 0 or 1 if the result of subtracting two positive numbers is negative? Is the Z80 flag CY 0 or 1 if the result of subtracting two positive numbers is negative? (Oddly enough, even though CY and DF serve the same purpose in both microprocessors, the answer for the 1802 is opposite that of the Z80.)

My objective for this exercise was to explain to myself exactly what was happening at the bit level during these addition and subtraction operations. I also wanted to formulate a simple model of the operation. As it turned out, in the 1802, all addition and subtraction operations are very neatly and cleanly lumped into one category. In the Z80, however, the picture is not so simple. While the Z80 has a large and powerful instruction set which I prefer to that of the 1802, the 1802 has a certain elegant simplicity.

What I wanted to do was to first set up a model for binary addition and subtraction, without reference to any particular processor, then show how the 1802 and Z80 addition and subtraction operations could be interpreted in terms of my model. I wanted my model to reflect the inherent simplicity that I ascribed to binary arithmetic.

In addition to 8-bit arithmetic operations, the Z80 also allows for 16-bit and even 4-bit operations, the latter being used in BCD (binary-coded decimal) manipulations (the half-carry flag H is the analog of the other carry flag CY). In the 1802, except for incrementing and decrementing the 16-bit registers R(N), all arithmetic operations use 8-bit operands. In my model, I am concerned only with 8-bit operations and how they can be used to implement multiple-byte additions and subtractions.

A unified model for addition and subtraction is possible because a subtraction operation can actually be viewed as an addition operation. Addition and subtraction can be accomplished with the same hardware, provided there are circuits to do complementation.

Let X and Y be 8-bit quantities. $\overline{Y}$ will denote the one's complement of Y ($\overline{Y}$ is again an 8-bit quantity, obtained by replacing each 1 with a 0 and each 0 with a 1). Let c_i and c_o denote 1-bit values, called respectively "carry in" and "carry out." In my general model, all 8-bit additions and subtractions take the form:

$$X + Y + c_i \rightarrow c_o, SUM$$

Here, *SUM* is the 8-bit quantity resulting from the addition of X, Y, and c_i. If a carry is generated, then $c_o = 1$; otherwise $c_o = 0$. This is shown in figure 1.

For single-precision (1-byte) additions and subtractions, $c_i = 0$ for addition and $c_i = 1$ for subtraction. For multiple-byte operations, c_i will take on the value of c_o generated in the last performed operation. The results of an addition or subtraction will be in two's complement form. The 8-bit quantity $\overline{Y}+1$ (and throw away the carry, if there is one) is the two's complement of Y.

If you wish to add X and Y, you do $X+Y+c_i$ with $c_i=0$; if you wish to compute the difference $X-Y$, you do $X+\overline{Y}+c_i$ with $c_i=1$ (ie: add the two's complement of Y to X). Thus, as advertised, both the sum and difference of X and Y can be regarded as taking the form of an addition. The distinction is that, for subtraction, c_i has a different value and the one's complement $\overline{Y}$ is used. Some examples are shown in figure 2.

The following is how multiple-byte sums are done. Suppose we have $X = X_m, X_{m-1} \ldots X_1$ (an m-byte sequence) and $Y = Y_m, Y_{m-1} \ldots Y_1$, where each X_k and Y_k is 8 bits. Let's say that you want to compute the multiple-byte sum $X+Y$. You first perform $X_1+Y_1+c_i$ with $c_i=0$. Then do

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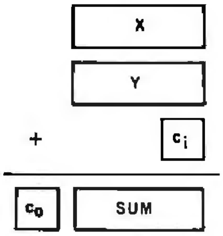

Figure 1: *A pictorial model of the addition of X, Y, and* c_i *to give* SUM *and the carry bit* c_o.

$X_2+Y_2+c_i$ where $c_i=c_o$ of the previous sum. And so forth until you finally do $X_m+Y_m+c_i$, with $c_i=c_o$ resulting from the immediately preceding sum of X_{m-1} and Y_{m-1}.

Multiple-byte subtractions are similar. Again, suppose X and Y are given as above, but now you want to compute the multiple-byte difference $X-Y$. First, perform $X_1+\overline{Y}_1+c_i$ with $c_i=1$. Next do $X_2+\overline{Y}_2+c_i$ with $c_i=c_o$ of the preceding sum; and so on until you finally do $X_m+\overline{Y}_m+c_i$ with $c_i=c_o$ resulting from the immediately preceding sum of X_{m-1} and $\overline{Y}_{m-1}$. Notice that $X-Y$ is computed by adding the two's complement of Y to X in a multiple-byte fashion.

Let me summarize the addition/subtraction model I have just presented. Whether you choose to add or subtract, or whether you want multiple-byte or single-byte operations, in all cases the fundamental operation is a sum of the form $X+Y+c_i \rightarrow c_o$, *SUM*.

```
          X=5
          Y=6
       Find X+Y
       00000101    X
       00000110    Y
   +          0    ci
   ------------
       00001011    X+Y
       Co=0

          X=5
          Y=6
       Find X-Y
       00000101    X
       11111001    Y̅
   +          1    ci
   ------------
       11111111    X-Y
       Co=0

          X=6
          Y=5
       Find X-Y
       00000110    X
       11111010    Y̅
   +          1    ci
   ------------
       00000001    X-Y
       Co=1
```

Figure 2: *Some examples of a unified model for binary addition and subtraction.* c_i *and* c_o *are 1-bit values called "carry in" and "carry out." If a carry is generated by the addition of X and Y, then* $c_o = 1$; *otherwise* $c_o = 0$.

The 1802 processor fits this model perfectly. In the 1802, both c_i and c_o correspond to the 1-bit register DF. Just before the addition or subtraction operation is performed, DF is the c_i. Just after the operation, DF is loaded with c_o. (Incidentally, table 1 is a complete list of the 1802 arithmetic operations.) WITH CARRY and WITH BORROW operations take c_i to be whatever value that currently resides in DF (ie: c_i is determined by c_o of the previous operation). Otherwise, as discussed in my model, c_i must be 0 for an addition and 1 for a subtraction operation.

Table 1 is important for two reasons. First, it reveals exactly what each operation does. $(D+\overline{M(R(X))}+DF \rightarrow DF,D$ is much clearer than $D-M(R(X))-(NOT\ DF)\rightarrow DF,D.)$ Second, it is obvious that, without exception, each addition and subtraction operation has the form $X+Y+c_i \rightarrow c_o$,SUM. This last fact is no accident, since (presumably) the same hardware is used for all operations.

In the Z80, the 1-bit carry flag CY serves the same function as the DF flag does in the 1802. In contrast with the 1802, where the DF bit corresponds exactly with the model's c_i and c_o, there is a distinction in the Z80 between an addition and a subtraction as far as the role of the CY is concerned. Consider this example that points out this distinction. Is the computation $5-3$ the same as $5+(-3)$? That is, in the Z80, is there any difference in the outcome between the assembly-language sequences (LD A,05 SUB 03) and (LD A,05 ADD FD)? (FD is the two's complement representation of -3, written in hexadecimal.) While the end result is 02 in A for both computations, the final value of CY is not the same. When you do $5-3$, CY=0. When you do $5+(-3)$, CY=1. If you do analogous operations in the 1802, DF=1 in both cases. How do you make sense out of all this?

Table 2 describes what occurs within the Z80 in terms of my model. Four classes of operations are shown in the table: add, add with carry, subtract, and subtract with carry. X and Y are arbitrary 8-bit operands within the

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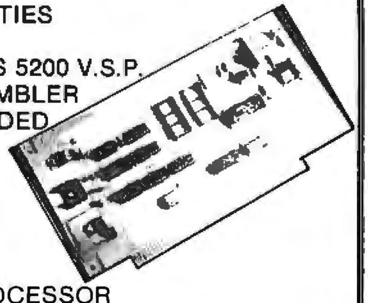

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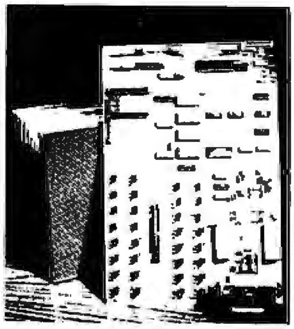

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.0039mf	.13	.11	.08
.0047mf	13	.11	08
.0056mf	.13	.11	.08
.0068mf	.13	.11	.08
.0082mf	.13	.11	.08
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.022mf	.14	.12	.09
.027mf	.14	.12	.09
.033mf	.14	.12	.09
.039mf	.15	.13	.10
.047mf	.15	.13	.10
.056mf	.16	.13	.10
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.082mf	.17	.14	.11
.1mf	.18	.15	.12
.12mf	.20	.17	.14
.15mf	.22	18	.15
.18mf	.24	.20	.16
.22mf	.26	.22	.17
.27mf	.30	.25	.20
.33mf	.33	.28	.23
.39mf	.37	.31	.25
.47mf	.40	.34	.30

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20	200	2K	20K	200K	2M
22	220	2.2K	22K	220K	2.2M
24	240	2.4K	24K	240K	2.4M
27	270	2.7K	27K	270K	2.7M
30	300	3K	30K	300K	3M
33	330	3.3K	33K	330K	3.3M
36	360	3.6K	36K	360K	3.6M
39	390	3.9K	39K	390K	3.9M
43	430	4.3K	43K	430K	4.3M
47	470	4.7K	47K	470K	4.7M
51	510	5.1K	51K	510K	5.1M
56	560	5.6K	56K	560K	5.6M
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68	680	6.8K	68K	680K	
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79L12	TO92	.65
79L15	TO92	.65
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7812P	TO220	1.20
7815P	TO220	1.20
7905P	TO220	1.25
7912P	TO220	1.25
7915P	TO220	1.25
7805K	TO3	1.50
7812K	TO3	1.50
7815K	TO3	1.50
7905K	TO3	1.60
7912K	TO3	1.60
7915K	TO3	1 60
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.33mf	35v	.35	.30	.26
.47mf	35v	.35	.30	.26
.68mf	35v	.35	.30	.26
1mf	35v	.35	.30	.26
1.5mf	35v	.45	.39	.33
2.2mf	35v	.45	.39	.33
3.3mf	35v	.50	.42	.36
4.7mf	25v	.50	.42	.36
4.7mf	35v	.65	.56	.44
6.8mf	35v	.65	.56	.44
10mf	25v	.85	.72	.61
10mf	35v	1.19	1.00	.84
15mf	25v	1.30	1.09	.92
22mf	25v	1.30	1.09	.92
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74100	99
74104	85
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4021	1 10
4022	.75
4023	35
4024	.85
4025	.35
4026	1.45
4027	.50
4028	.75
4029	1.15
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4041	1.15
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4047	1.35
4048	.99
4049	.50
4050	.50
4051	1.10
4052	1.10
4053	.85
4060	1.39
4066	.39
4068	.35
4069	.35
4070	.39
4071	.39
4072	.39
4073	.39
4075	.39
4076	1.15
4077	.39
4078	.35
4081	.35
4082	.35
4093	.95
4503	.85
4508	2.95
4510	.89
4511	89
4512	1.10
4514	2.55
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	Operation Code	Operands Used That Match the Formula:				
Operation		X	+	Y	+	$c_i \rightarrow c_o$,SUM
ADD	F4	M(R(X))	+	D	+	0→DF,D
ADD IMMEDIATE	FC	M(R(P))	+	D	+	0→DF,D
ADD WITH CARRY	74	M(R(X))	+	D	+	DF→DF,D
ADD WITH CARRY IMMEDIATE	7C	M(R(P))	+	D	+	DF→DF,D
SUBTRACT D	F5	M(R(X))	+	$\overline{D}$	+	1→DF,D
SUBTRACT D IMMEDIATE	FD	M(R(P))	+	$\overline{D}$	+	1→DF,D
SUBTRACT D WITH BORROW	75	M(R(X))	+	$\overline{D}$	+	DF→DF,D
SUBTRACT D WITH BORROW IMMEDIATE	7D	M(R(P))	+	$\overline{D}$	+	DF→DF,D
SUBTRACT MEMORY	F7	D	+	$\overline{M(R(X))}$	+	1→DF,D
SUBTRACT MEMORY IMMEDIATE	FF	D	+	$\overline{M(R(P))}$	+	1→DF,D
SUBTRACT MEMORY WITH BORROW	77	D	+	$\overline{M(R(X))}$	+	DF→DF,D
SUBTRACT MEMORY WITH BORROW IMMEDIATE	7F	D	+	$\overline{M(R(P))}$	+	DF→DF,D

Table 1: *Arithmetic operations of the 1802 microprocessor.*

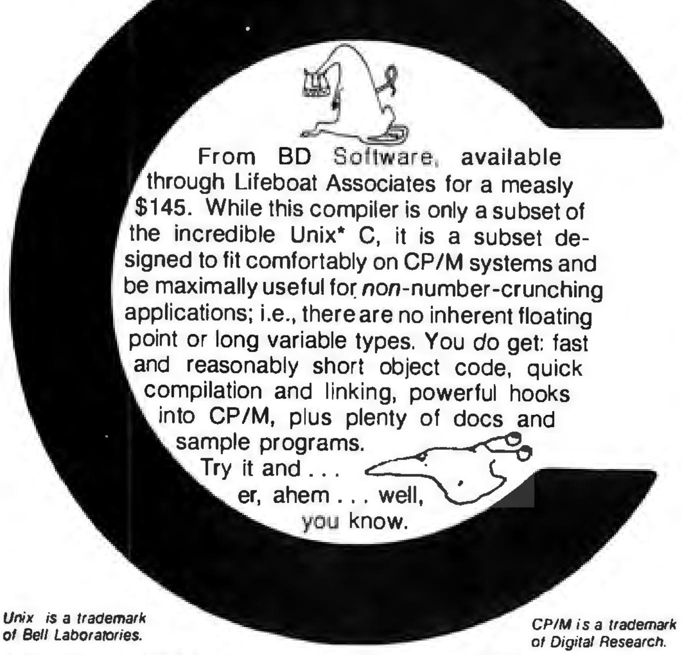
Operation performed	X + Y	X + Y with carry	X − Y	X − Y with carry
Equivalent sequence of steps taken within the Z80 to perform the given operation	$CY \leftarrow 0$ $c_i \leftarrow CY$ $SUM = X + Y + c_i$ $CY \leftarrow c_o$	$c_i \leftarrow CY$ $SUM = X + Y + c_i$ $CY \leftarrow c_o$	$CY \leftarrow 0$ $c_i \leftarrow \overline{CY}$ $SUM = X + \overline{Y} + c_i$ $CY \leftarrow \overline{c_o}$	$c_i \leftarrow \overline{CY}$ $SUM = X + \overline{Y} + c_i$ $CY \leftarrow \overline{c_o}$

Table 2: *Addition and subtraction operations in the Z80 microprocessor.*

Z80. Notice that the "with carry" operations (ADC, SBC) are distinguished from the others only in that CY is not initially zeroed. The peculiar feature of table 2 (in comparison with table 1) is that, when doing a subtraction, the CY bit is complemented beforehand to obtain c_i. Following the operation, c_o is complemented to yield the final value for CY. This explains why 5−3 and 5+(−3) are not equivalent in the Z80 (as far as the end result of CY is concerned). When the operation performed is a subtraction, CY takes on the complement of c_o.

As an illustration of the importance of the above considerations, suppose that you want to compute $X-Y$ (where X and Y are 8-bit positive values). Then you want to branch according to whether the result is negative or positive. In the 1802, DF=1 means that the result was positive, and a branch is made based on the value of DF. Suppose in the Z80 you wish to branch according to CY (the branching could also be done according to the sign bit; however, there are cases when using CY is more convenient, such as a shift operation that follows a subtraction). The problem is not so straightforward now, because in the Z80, it is crucial to know whether or not $X-Y$ was computed using a subtraction operation. If so, flag CY=0 means the result was positive. ■

Technical Forum is a feature intended as an interactive dialog on the technology of personal computing. The subject matter is open-ended, and the intent is to foster discussion and communication among readers of BYTE. We ask that all correspondents supply their full names and addresses to be printed with their commentaries. We also ask that correspondents supply their telephone numbers, which will not be printed.



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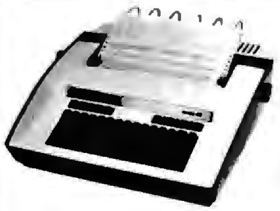

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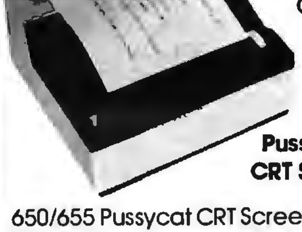

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You have probably played the popular Hunt the Wumpus game (in BASIC) on a microcomputer system. Now, you can hunt him on your HP-41C. This version of Hunt the Wumpus has all the excitement of the big game, including the ability to throw gas cans, get snatched by bats, or fall into a pit. You'll also be warned when the Wumpus, a pit, or bats are near.

The program will easily fit into an unexpanded HP-41C. With added memory modules and a bit of experimentation, many refinements are possible.

Playing the Game

After entering the program as shown in listing 1 (on page 232), set the following:

- SIZE 018 (eighteen registers are used)
- FIX 0
- Enter the register data as shown in table 1
- ASN WUMP XEQ (assigns program to XEQ key)
- Put HP-41C in USER mode
- Press XEQ

At this point, you will be prompted with "SHOOT?" Enter your choice, YES or NO (you will automatically be in the ALPHA mode), and press RUN. You will be asked which room you wish to enter. Continue until you win or lose. Happy hunting! ■

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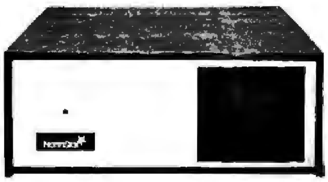

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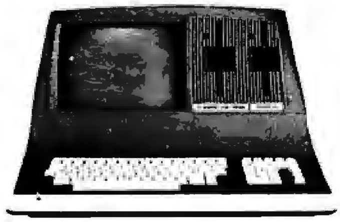

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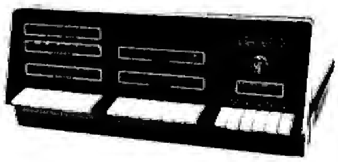

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Circle 148 on inquiry card.

Register	Contents	Comments
R0	–	Your location, generated randomly
R1	2345	Room layouts, enter these values in ALPHA mode
R2	158 10	
R3	1467	
R4	1357	
R5	124 10	
R6	3789	
R7	3469	
R8	269 10	
R9	678 10	
R10	2589	
R11	3	Number of cans of gas, generated by program
R12	seed	Used for random number generation 0<s<1
R13	–	Wumpus position
R14	–	Bat positions (all generated randomly)
R15	–	Pit position
R16	YES	Enter letters in ALPHA mode; used for string comparison
R17	NO	Enter letters in ALPHA mode; used for string comparison

Table 1: *Register data used in the Hunt the Wumpus game for the HP-41C. A dash indicates data that varies from game to game. See the text for details on using the program.*

Listing 1: *Hunt the Wumpus for the HP-41C programmable calculator.*

```
01♦LBL "WUMP"
02 3
03 STO 11
04 XEQ 01
05 STO 13
06 XEQ 01
07 STO 14
08 XEQ 01
09 STO 15
10♦LBL 00
11 XEQ 01
12 RCL 13
13 X=Y?
14 GTO 00
15 X<>Y
16 STO 00
17♦LBL 09
18 XEQ 03
19 GTO 02
20 GTO 14
21♦LBL 01
22 RCL 12
23 PI
24 +
25 21
26 *
27 FRC
28 STO 12
29 10
30 *
31 INT
32 1
33 +
34 RTN
35♦LBL 02
36 RCL 13
37 XEQ 06
38 X<=Y?
39 GTO 05
40 "WUMPUS NEAR"
41 AVIEW
42♦LBL 05
43 RCL 14
44 XEQ 06
45 X<=Y?
46 GTO 07
47 "BATS NEAR"
48 AVIEW
49♦LBL 07
50 RCL 15
51 XEQ 06
52 X<=Y?
53 GTO 14
54 "PIT NEAR"
55 AVIEW
56 GTO 14
57♦LBL 06
58 RCL 00
59 -
60 ABS
61 3
62 RTN
63♦LBL 03
64 RCL 00
65 "YOU ARE IN ROOM"
66 "├ NO:"
67 ARCL X
68 AVIEW
69 PSE
70 PSE
71 RTN
72♦LBL 14
73 "GOT"
74 ARCL 11
75 "├ CANS"
76 AVIEW
77 PSE
78 "SHOOT?"
79 ARCL 16
80 "├"
81 ARCL 17
82 AVIEW
83 PSE
84 AON
85 STOP
86 ASTO X
87 AOFF
88 RCL 16
89 X=Y?
90 GTO 08
91 XEQ 13
92 STOP
93 STO 00
94♦LBL 04
95 RCL 00
96 RCL 14
97 -
98 X=0?
99 GTO 11
100 RCL 00
101 RCL 15
102 -
103 X=0?
104 GTO 12
105 GTO 09
106♦LBL 11
107 XEQ 01
108 STO 00
109 "SNATCHED TO:"
110 ARCL 00
111 AVIEW
112 GTO 09
113♦LBL 12
114 "FELL IN"
115 AVIEW
116 STOP
117♦LBL 13
118 "TO ROOM:"
119 ARCL IND 00
120 AVIEW
121 PSE
122 RTN
123♦LBL 08
124 1
125 ST- 11
126 XEQ 13
127 STOP
128 STO 00
129 RCL 13
130 -
131 X=0?
132 GTO 10
133 RCL 11
134 X=0?
135 GTO 15
136 "MISSED"
137 AVIEW
138 GTO 09
139♦LBL 10
140 "GOT HIM"
141 AVIEW
142 BEEP
143 STOP
144♦LBL 15
145 "LOST"
146 AVIEW
147 TONE 1
148 END
```

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Build a Simple Video Switch

Richard C Hallgren, Department of Biomechanics,
College of Osteopathic Medicine, Michigan State University,
East Lansing MI 48824

Although I know that there are many sophisticated ways of building a video switch, I am hard pressed to think of one that is easier to build, as inexpensive, or works as reliably as mine. In the process of building a CAI (computer-aided instruction) system, I needed a logic-controlled device to switch video to a video display at appropriate times. Because I had to transfer the video signal without excessive attenuation, I knew that the switch required a series impedance of less than 50 ohms at 10 MHz.

Motorola Semiconductor manufactures a quad bilateral switch (MC14016B) that is able to transfer frequencies up to 54 MHz, but the series resistance of each switch is in the neighborhood of 300 ohms. As I considered other alternatives, it occurred to me that if I took two of the devices and connected all eight of the switches in parallel, the series impedance would be approximately 37.5 ohms.

Figure 1 shows the schematic diagram of the video switch. Dropping the control line to ground opens the switch, and raising the control line to +5 V closes the switch. Since the units are bilateral, it doesn't matter which line is the input or output. I have used the switch in this form for over a year, and it has performed so well that there hasn't been a need to replace it with a more elegant design. ■

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- Quiescent current = 0.5 nA/package typical at 5 VDC
- Low crosstalk between switches — 80 dB typical at 1.0 MHz
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- Supply voltage range = 3.0 VDC to 18 VDC
- Transmits frequencies up to 54 MHz at 5 VDC
- Linearized transfer characteristics
- Low noise — $12 nV/\sqrt{Cycle}$, f > 1 kHz typical
- Pin-for-pin replacement for CD4016, CD4066

Maximum Ratings (voltage referenced to V_{SS})

Rating	Symbol	Value	Unit
DC supply voltage	V_{DD}	−0.5 to +18	VDC
Input voltage—all inputs	V_{in}	−0.5 to V_{DD} + 0.5	VDC
DC current drain per pin	1	10	mADC
Operating temperature range AL device CL/CP device	T_A	 −55 to +125 −40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

Table 1: *Technical data for the MC14016B.*

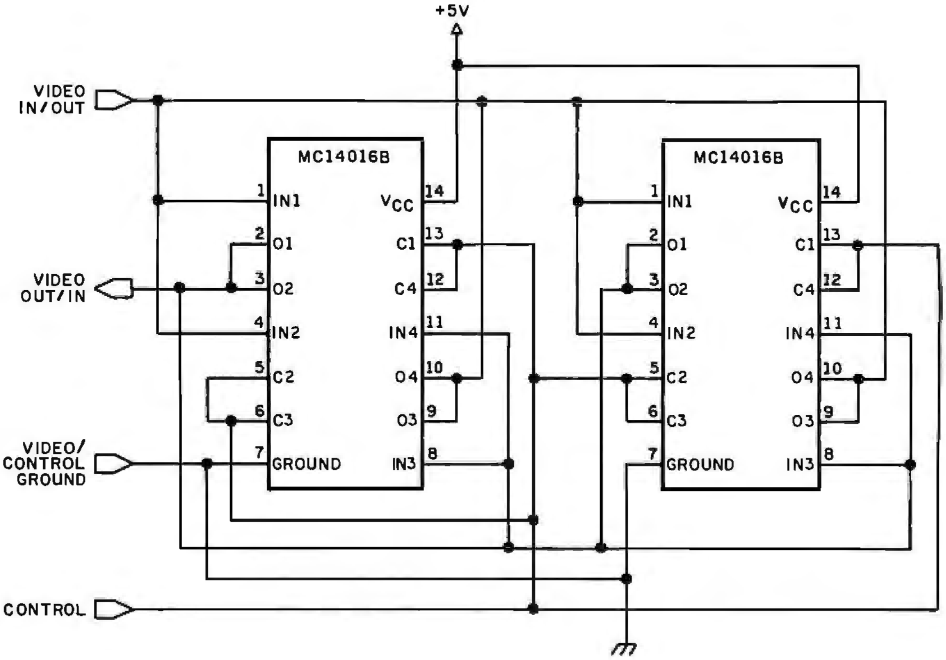

Figure 1: *Schematic diagram of a simple video switch. The MC14016B integrated circuit is a Quad Analog Switch/Quad Multiplexer manufactured by Motorola Semiconductor.*

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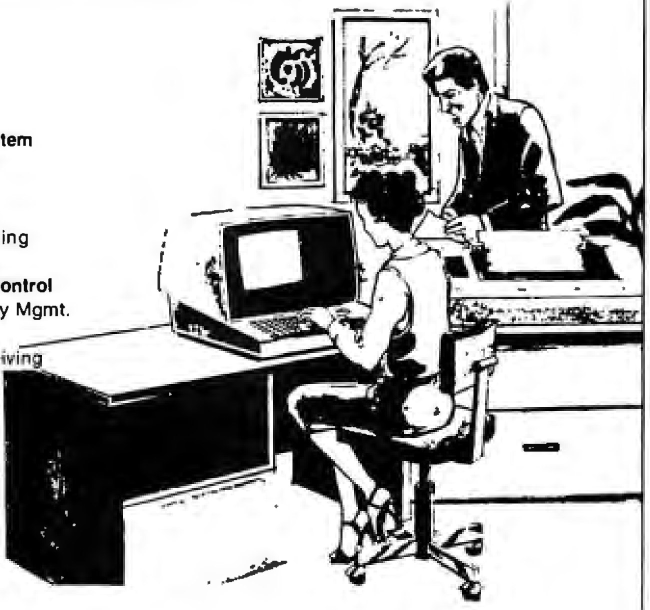

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Software Addressing Modes for the 8080

Dragan Bozinovic
25 Wood St Apt 810
Toronto, Ontario M4Y 2P9 Canada

If you have ever had to write a nontrivial program in Intel 8080 assembler, you probably missed the convenience of more sophisticated addressing modes such as indexed, indirect, and relative addressing. You may have also wished that you had an easy way to access data stored below the top of the stack.

Let's briefly review what Intel 8080 hardware offers in the area of addressing, along with suggestions for improvement:

1. *Direct addressing:* All 3-byte instructions are direct, with the absolute address stored in the last 2 bytes of the instruction. If you do not have a relocating assembler and loader, you must specify absolute starting addresses in your subroutines. This will force you to reassemble them whenever you have to change addresses. It would be convenient to have relative addressing instead, which would specify the displacement (positive or negative) of the referenced address relative to the address of the referencing instruction. Assemblers can easily calculate these displacements for you. All addresses in your subroutine will be independent of its starting location, allowing you to move the object code anywhere in memory. Relative addressing tends to confuse beginners, but they soon find that it is worth the effort to overcome the initial confusion.
2. *Implicit addressing:* Most instructions can reference the byte pointed to by the "data counter" (register pair HL), while a few accumulator-oriented instructions can use other registers as data counters. A nicer arrangement would be one in which any memory location could serve as a data counter, freeing the processor registers for more useful work. This is where indirect addressing comes in.
3. *Stack pointer addressing:* You can readily access the last 2 bytes stored in the stack, but if you think about retrieving bytes stored previously you may get a headache.
4. *Immediate data:* The instruction itself contains the data byte instead of an address.

What can software do to enhance the choice of addressing modes? If you're not overly concerned about execution speed, you may use software routines to create the illusion of having any addressing mode you desire. You will also need a few bytes of programmable (writable) memory.

How does it work? Just CALL the routine implementing the particular addressing mode, followed immediately by the instruction to be executed using that mode. That instruction will not be executed as is, but will provide the operation code and information necessary for EA (effective address) calculation. Instructions that are to be executed by hardware will be formed in programmable memory. After execution, control returns to the instruction following the pseudo-instruction unless it was a successful CALL or JMP. None of the registers are changed unless they are modified by the instruction to be executed.

Listing 1 contains detailed specifications of each routine and its source code. Concerning the programming conventions used, it may be noted that routines were developed using the Intel MAC80 assembler, which has only one location counter ($). To define data storage close to the routines that use it, and still separate it physically into programmable memory, three predefined labels, PROG, DATA, and TEMP, are used to keep track of the addresses.

The basic idea behind the approach described here is that of covering hardware by a layer of software routines, creating an illusion of a machine that is easier to program. In fact, this is the concept behind the creation of a virtual machine. It can be expanded far beyond the basic addressing modes, particularly in the area of I/O (input/output) handling. This approach was developed to hide peripheral devices from the programmer, but the application to addressing modes is likely to be better understood by a wider circle of programmers. ■

Listing 1 and text box on pages 238 and 240.

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Listing 1: *Sophisticated addressing modes may be emulated on an Intel 8080 microprocessor with the use of these subroutines. They are passed values interpreted as pseudo-code, each setting up the proper absolute addresses, freeing the programmer from the bind of limited addressing. Similar routines could easily be developed for other processors.*

```
Location  Object    Label        Operation  Operand
          Code
A0DC                             ORG        PROG
A0DC                RELAT:
A0DC      E3                     XTHL
A0DD      F5                     PUSH       PSW
A0DE      D5                     PUSH       D
A0DF      CD27A1                 CALL       EMSUB
A0E2      2B                     DCX        H
A0E3      2B                     DCX        H
A0E4      2B                     DCX        H
A0E5      C31DA1                 JMP        EMEND
000C                LENGTH       SET        $-RELAT
A0E8                PROG         SET        $.
                    ;
A0E8                             ORG        PROG
A0E8                SPNDX:
A0E8      E3                     XTHL
A0E9      F5                     PUSH       PSW
A0EA      D5                     PUSH       D
A0EB      EB                     XCHG
A0EC      210600                 LXI        H,6
A0EF      39                     DAD        SP
A0F0      EB                     XCHG
A0F1      D5                     PUSH       D
A0F2      C319A1                 JMP        EM1
000D                LENGTH       SET        $-SPNDX
A0F5                PROG         SET        $
                    ;
A0F5                             ORG        PROG
A0F5                SPDEX:
A0F5      E3                     XTHL
A0F6      F5                     PUSH       PSW
A0F7      D5                     PUSH       D
A0F8      E5                     PUSH       H
A0F9      210800                 LXI        H,8
A0FC      39                     DAD        SP
A0FD      E3                     XTHL
A0FE      CD39A1                 CALL       EMS1B
A101      E1                     POP        H
A102      C31DA1                 JMP        EMEND
0010                LENGTH       SET        $-SPDEX
A105                PROG         SET        $

A105                INDRX:
A105      E3                     XTHL
A106      F5                     PUSH       PSW
A107      D5                     PUSH       D
A108      E5                     PUSH       H
A109      EB                     XCHG
A10A      5E                     MOV        E,M
A10B      23                     INX        H
A10C      56                     MOV        D,M
A10D      EB                     XCHG
A10E      E3                     XTHL
A10F      C319A1                 JMP        EM1
000D                LENGTH       SET        $-INDRX
A112                PROG         SET        $
                    ;
A112                             ORG        PROG
A112                INDEX:
A112      E3                     XTHL
A113      F5                     PUSH       PSW
A114      D5                     PUSH       D
A115      D5                     PUSH       D
A116      C319A1                 JMP        EM1
0007                LENGTH       SET        $-INDEX
A119                PROG         SET        $
A119                             ORG        PROG
A119                EM1:
A119      CD27A1                 CALL       EMSUB
A11C      E1                     POP        H
A11D                EMEND:
A11D      19                     DAD        D
A11E      22F167                 SHLD       EMINS + 1
A121      D1                     POP        D
A122      F1                     POP        PSW
A123      E1                     POP        H
A124      C3F0B7                 JMP        EMINS
                    ;
A127                EMSUB:
A127      7E                     MOV        A,M
A128      32F0B7                 STA        EMINS
A128      23                     INX        H
A12C      5E                     MOV        E,M
A12D      23                     INX        H
A12E      56                     MOV        D,M
A12F                EMSBR:
A12F      3E                     DB         03EH
A130      C3                     DB         0C3H
A131      32F387                 STA        EMRTN
A134      23                     INX        H
A135      22F4B7                 SHLD       EMRTN + 1
A138      C9                     RET
A139                EMS1B:
A139      7E                     MOV        A,M
A13A      32F0B7                 STA        EMINS
A13D      C32FA1                 JMP        EMSBR
0027                LENGTH       SET        $-EM1
A140                PROG         SET        $
B7F0                             ORG        TEMP
B7F0                EMINS:       DS         3
B7F3                EMRTN:       DS         3
B800                             ORG        DATA
B800                DATA         SET        $
```

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Interface Specifications

Family: *EMUL*

Routines: *RELAT, INDEX, INDRX, SPNDX, SPDEX.*

Purpose: *This family of routines EMULates several addressing modes not implemented by Intel 8080 hardware.*

Description: *Routines consist of separate CALLable prefixes of code, common subroutine (EMSUB), and final processing routine (EMEND), grouped under the name EMUL (see listing 1). Prefixes of unnecessary routines may be removed. All routines share a common temporary data area defined in EMUL. In this work area two instructions are constructed and executed:*

1. *Instruction to be emulated*
2. *Return jump*

CALLing interface basic description:

```
        CALL   entry-point
        op     address-parameter
```

The instruction to be emulated is one of Intel 8080's 3-byte instructions: LDA, STA, LHLD, SHLD, LXI, JMP's and CALLs. Any other instruction is illegal and will produce incorrect results. Return is made after the emulated instruction (except for JMP and CALL). The instruction is not executed as coded, but serves as an argument to emulation routines. The value expected in the address field of the emulated instruction and the method of forming EA as well as eventual additional parameters are all described for each routine. Some of the routines are redundant and can be simulated by others from this family. Users will have to decide which to use depending on the concern for programming convenience, calling sequence storage requirements, and execution speed. If applicable, alternate ways of accomplishing each effect are given under the description of each routine.

Side Effects: *The current stack is used three to four words deep and restored before return. None of the processor registers are changed (including PSW) unless modified by the emulated instruction.*

Routine: *RELAT*

Purpose: *This routine is provided to facilitate writing of PIC (position-independent code). It emulates addressing relative to PC (program counter).*

Use: *If you are writing a module that must be capable of executing anywhere in memory you may reference a label in the same module as follows:*

```
CALL  RELAT
op    label-$     ; $ being the current location
                    counter value
```

The displacement label-$ will be added to the content of PC to form the effective address and the instruction will be executed. The only precondition is to have RELAT code or JMP to it on the fixed absolute address known at assembly time.

Routine: *INDEX*

Purpose: *This routine emulates addressing relative to the content of the register pair DE. Effective address is formed as:*

$$EA = (DE) + displacement$$

Displacement is taken from the address field of the emulated instruction and can be either positive or negative.

Routine: *INDRX*

Purpose: *This routine emulates addressing relative to content of the word pointed to by register pair DE. Effective address is formed as:*

$$EA = ((DE)) + displacement$$

Calling sequence:

```
        LXI     D,address
        CALL    INDRX
```

is equivalent to:

```
        LHLD    address
        XCHG
        CALL    INDEX
```

Routine: *SPNDX*

Purpose: *Sometimes you may wish to access not the top word of the current stack (using POP, XTHL, or PUSH), but a previously stored word or byte. This may be accomplished by calling this routine if the position of the desired word or byte relative to the top of the stack is known at assembly time. The word that is referenced by POP is accessed using an offset of zero (low byte zero, high byte one). The offset is found in the address field of the instruction to be emulated. It is not and cannot be checked against the current depth of the stack. The SP content is not changed.*

Routine: *SPDEX*

Purpose: *This routine has the same purpose as SPNDX, but the offset is found in register pair DE instead of the address field of the following instruction. This permits the offset to be dynamically changed, even if the program is to be ROM (read-only memory) resident. The calling sequence of this routine is different from the general model. It is:*

```
        LXI    D,offset  ; or equivalent
        CALL   SPDEX
        DB     op-code   ; octal or hex
```

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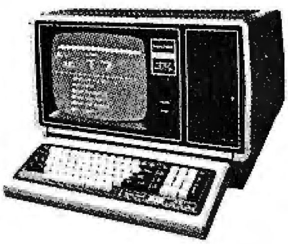

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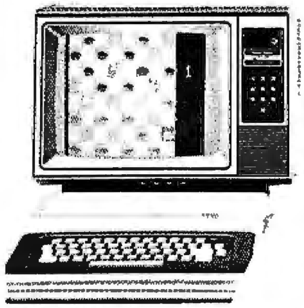

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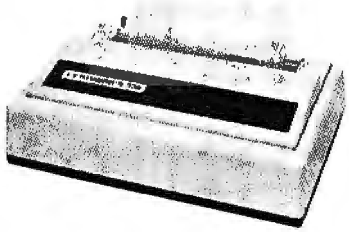

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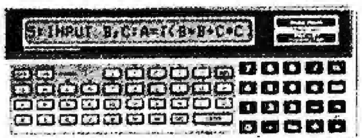

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The law gives the author exclusive rights to copy the work and to transfer ownership rights, including sale and leasing arrangements. Piracy is punishable by fines, civil damages, or criminal penalties. Work does not have to be registered with the Copyright Office to be protected; it is protected once it is in "any tangible medium of expression."

Before the passage of this law, the copyright status of computer software was unclear.

First 68000 System Introduced: S-100-bus personal-computer users can now step up to the most powerful 16-bit microprocessor—the Motorola MC68000. Management Analysis & Control Inc, 3530 C Street NE, Auburn WA 98002, is the first manufacturer to announce a 68000-based personal-computer system. Its new processor card will sell for $2095. (That's more than I paid for my entire S-100 cabinet and contents!) As yet, no software has been announced.

Shugart Offers 5-Megabyte Hard-Disk System For Under $2000: If you're looking for a hard-disk system and can do some minimal interfacing, you'll be interested in Shugart Associates' special deal, called the "Success Kit." The kit is really an evaluation offer for OEMs considering the design of a Shugart hard-disk drive into their computer systems; however, there are no restrictions on the offer, hence anyone can buy just one Success Kit. For $1950 you can get an SA1002 8-inch, 5-megabyte Winchester-technology drive, an SA1400 intelligent controller, cables, and documentation. The controller provides backup on single- or double-sided floppy-disk drives. For more information, call (800) 824-7888; in California (800) 852-7777 (operator 12).

FCC Grants Apple and Heath Extensions: The FCC has granted Apple Computer Inc and Heath Company a 3-month extension on compliance with the January 1, 1981 deadline for RF (radio-frequency) radiation regulations. Each unit now carries a label warning that the equipment can interfere with radio and television reception and that the user is responsible for correcting it.

This is the second extension of the original July 1980 deadline given the companies by the FCC. Both contended that more time was needed to make the necessary product changes.

AT&T Plans Home-Video Data Base: AT&T has disclosed that it is about to begin a year-long test of an electronic telephone directory. The test will involve 700 color-video terminals in homes and businesses throughout Austin, Texas. The terminals will be connected to telephone lines and used to access white- and Yellow-Pages listings. Users will also be able to store personal information.

A similar test involving eighty-three participants was conducted earlier in Albany, Texas; it involved black-and-white terminals. AT&T is conducting another test with the Knight-Ridder Newspaper group, in Coral Gables, Florida. That system includes news reports, home banking, and a home-shopping service.

If these tests are successful, it will be three to four years before the system is widely available.

Japanese Sales Of US-Made Personal Computers Drop Sharply: *Feedback From Fujitsu*, a Japanese computer-industry newsletter, reports that the sales of US-made personal computers in that country have dropped sharply. It says that until recently, Tandy/Radio Shack, Commodore, and Apple manufactured over 90% of the 6000 to 7000 personal computers sold monthly in Japan. However, their share of the market has fallen to 20% as Hitachi, NEC (Nippon Electric Company), and Sharp have moved into the manufacture and sale of personal computers.

Apple and Tandy have formed joint ventures with Japanese concerns in an attempt to combat these inroads on US sales. Commodore is reportedly studying a similar move.

Japanese Establishing Foothold In US Personal Computing: The Japanese presence is being felt in the American personal-computer market. For example, all 142 Computerland stores will soon carry Japanese personal computers. Computerland is currently negotiating with Casio, NEC, Panasonic, and Hitachi. Several other distributors are flirting with Japanese personal computers. Apple, TI (Texas Instruments), and Atari appear to be the primary losers of valuable showroom space.

Terminals To Replace Phone Directories: The French government is preparing to launch a bold effort to give every telephone subscriber in France a mini-video terminal. Initially it will provide on-line telephone directories. The terminal will have a 7- to 8-inch diagonal screen with 24 lines of 40 characters each, solid-state keyboard, and a modem to send data at 75 bps (bits per second) and receive at 1200 bps. The PTT (Postal Telephone and Telegraph Authority) expects the terminal to cost $75 to $100. Over the next ten years, the PTT expects to procure more than 30 million terminals at a cost of $3 billion, which it estimates is less than the cost of printed directories and directory-assistance operators.

More Hobby Robotics Activities: Add these developments to previously listed sources of robotics information.

The United States Robotics Society, Palo Alto, California, is resuming publication of its *ROVOX* newsletter. Membership is $20 per year. The Computerworld Store, Van Nuys, California, has published the *Robotics Catalog*. Also, the International Institute of

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"Critical path" network analysis program for scheduling manpower, dollars and time to maximize productivity.

An interactive project management program that runs under CP/M and can relate together different skills, hourly pay rates and projects to maximize efficiency. MILESTONE could be used to track paper flow, build a computer, check a salesman's performance, or build a bridge. MILESTONE can be used by exeutives, engineers, managers, and small businessmen to:

- Find the critical tasks which can't be delayed.
- Discover which tasks are not time critical.
- See how manpower and expenses vary versus time.
- Investigate tradeoffs between manpower, dollars and time.
- Communicate plans to others using a printed project schedule.
- Change details of the project and immediately see the results on the screen.

Requires 48K RAM and CP/M. Also available for Apple UCSD Pascal or UCSD Pascal Operating Systems.
Formats: 8, NS, MP, CDOS, SB, TRS2, APPL

SPECIAL INTRODUCTORY PRICE: $295. until April 1, 1981
Manual alone - $30.

DATEBOOK™ - $295. Manual alone $25.

- Replaces your office appointment calendar
- Searches for openings that fit time of day, day of week & day of year constraints
- Appointments made, modified or cancelled by a few key strokes
- Copies of day's appointments can be quickly printed
- Schedule appointments 4 months in advance - plus.

Requires CP/M or UCSD Pascal and 48K RAM
Formats: 8, NS, MP, CDOS, SB, APPL, TRS2

TEXTWRITER III™ - $125. Manual alone - $25.

Requires CP/M, NorthStar DOS, or MDOS
Formats: 8, NS MP, TRS2

REPORT WRITER™ - $150. Manual alone - $25.

Mini-word and arithmetic calculation processor designed to generate reports with ledger of figures and numeric calculations. Built-in calculator functions end calculator to paper errors. Saves data. Reports can be printed as often as desired. Changes in data can be easily entered and saved. "Cause and Effect" analysis easily computed using Recalculate function.
Requires CP/M, Microsoft Basic and 48K RAM
Formats: 8, NS, MP, SB, TRS2, CDOS

MAGIC WAND™ - $395. Manual alone - $35.

Word Processing System

- Full screen text editing
- Full text formatting commands
- Merging with external data files
- Variables
- Conditional commands
- True proportional printing

Specify disk format, terminal and printer.

MAGIC MENU™

Turns Magic Wand into a turnkey system. Allows move from EDIT to PRINT, backup of files or disks, system status, etc. from menu without returning to CP/M 2.x
Requires 56K RAM, CP/M and Magic Wand.
Regular Price - $95

SPECIAL INTRODUCTORY PRICE: $45. when purchased with Magic Wand.
Formats: 8, NS, MP, SB, TRS2, APPL

PASCAL/M™. $225. Manual alone - $20.

CP/M™ compatible language for 8080/Z80 CPUs, supports full Jensen & Wirth plus 45 extensions to Standard Pascal including Random access files & 16 bit BCD real type. **NOW INCLUDES** symbolic debugger which features trapping on stores, examining and changing variables and tracing of program execution.

SPECIAL OFFER:
PASCAL/M DEMO DISK - $20.

Includes demo disk and manual.

PASCAL/M for 8086/88 - $270.

Manual alone - $20.

All features of Pascal/M for the 8086 and 8088 processors running under the 8086/88 version of CP/M.

Requires CP/M & 64K RAM   Formats: 8, NS, CDOS, APPL, TRS2

TRANS 86™ - $125. Manual alone - $20.

8086/88 Translator for existing 8080/Z80 programs. The new source code can be easily edited and assembled using ACT II to produce hex code which can be executed by 8086/88. Emphasizes the extensions and features available in the 8086/88.

Requires CP/M and 32K RAM
Formats: 8, NS CDOS, APPL

ACT I™ - $125. Manual alone - $15.

CP/M compatible macro assembler for Z80, 8080/85, 6502 & 6800.
One assembler that supports all major 8 bit micros. ACT features include full macro capabilities, comprehensive pseudo-ops, link-file structures, cross reference map, and algebraic expression processor. Requires 24K RAM & CP/M.

ACT II - $175. Manual alone - $20.

CP/M 2.x compatible cross assembler for 8086/88

ACT III - $125. Manual alone - $20.

CP/M 2.x compatible cross assembler for 6809.

ACT I and ACT II together - $225.

Formats: 8, NS, CDOS, MP/M, TRS2, APPL

PEARL™ The application software generator

Pearl asks questions that a programmer would have to answer to code the system. You answer the questions & Pearl uses built-in logic to construct both subroutines & mainline programs. The system then compiles & executes your program code.

- Level 1: For Personal Computing - $130.
- Level 2: The Business Assistant - $350.
- Level 3: Advanced Software Development - $650.

Manuals alone - $25. each
Requires CP/M and CBASIC2.   Formats: 8, NS, MP, SB, TRS2

CBASIC2™ - $120.

Industry standard intermediate code compiler with run-time interpreter. Features include chaining, integer & external precision arithmetic.

ULTRASORT-II™ - $175.

The sort/merge/select utility for CBASIC2 written in assembly language. Can be loaded by CBASIC during run-time; also can be used as a stand-alone utility.

FABS™ - $175. Manual alone - $20.

Fast Access Btree Structure. Key sequential multi-path balanced tree structure. Faster than ISAM. Can be loaded by Cbasic2 during run-time; also can be used as stand-alone utility. Also supports Microsoft Basic Compiler and S-Basic.

Requires CP/M and CBASIC2, Microsoft Basic Compiler or S-Basic
Formats: 8, NS, MP, SB, TRS2, CDOS

COPYWRITER™ $395. Manual alone - $35.

A powerful CP/M Word Processing System which includes a fast screen editor and is exceptionally easy to learn and use. Copywriter supports both vertical and horizontal scrolling for 132 column printers. File size is limited only by disk size. The print formating program allows control over output word processing files, and permits the insertion of variable data into form letters. Full proportional printing is also supported.

COPYWRITER+ $595. Manual alone - $35.

All of the above plus an integrated mailing list system which can select any range of zip codes for printing; select which fields to fill into merge; select by title, position or department within a company. Output can sort for bulk mailings by state and zip codes.
Copywriter Screen Editor alone - $195.

COPYPROOF™ - $295. Manual alone - $35.

Copywriter version of Spellguard.

DICTION I™ - $95.

22,000 dictionary words not included in Copyproof or Spellguard. Compatible with any word processor using Spellguard.

DICTION II - $195.

40,000 more words not included in Diction I, Copyproof or Spellguard.

Requires 54K RAM & CP/M. Formats: 8, NS

SPELLGUARD™ - $295. Manual alone - $20.

20,000+ word dictionary containing commonly used words that find spelling & typographical errors in text files. Allows review of mis-matched words & speedy search routine.
Proofs at 10,000 words/min.
Requires CP/M, 48K RAM & Magic Wand, WordStar™ or Spellbinder™
Formats: 8, NS, MP, SB, TRS2, CDOS

S-BASIC™ - $295. Manual alone $25.

Produces chainable, relocatable native code.

- ★ Fully defined user functions & procedures
- ★ Local & global variables
- ★ Single & double precision floating point
- ★ Fixed point packed BCD
- ★ Integer, string & character data types
- ★ Packed binary disk storage

Requires CP/M and 40K RAM   Formats: 8, NS, MP, SB, APPL

SELECTOR IV™ - $550. Manual alone - $25.

A totally self-contained CP/M Data Base System providing complete data, procedural, query, and report definition functions. Allows records to be managed on a one-for-one basis, as well as in 'batch' mode where several files can communicate with each other in a variety of ways. Includes multiple 'key fields'. Requires 54K RAM, CP/M and CBASIC2

Formats: 8, NS, MP, SB, APPL

MICROSTAT™

Powerful statistical analysis package.
Includes data management sub-system for editing, sorting, ranking, logging, data file transfers PLUS eleven data transformations (e.g. linear, reciprocal, exponential, etc.)

- Frequency distributions
- Multiple regression
- Time series
- Crosstabs/Chi-Square
- Factorials, permutations, combinations
- Scatterplots
- ANOVA (one and two-way)

Requires 48K RAM

CP/M-CBASIC2 version - $250.
CP/M - Microsoft Basic 80 version - $250.
NorthStar Basic version - $250.
Manual alone - $25.

Formats: 8, NS

FORMAT CODES: 8 (8" single density IBM soft-sectored) NS (NorthStar DD) MP (Micropolis Mod II/Vector MZ) SB (Superbrain 3.0) CDOS (8" Cromemco CDOS) TRS2 (TRS-80 Mod II) APPL (Apple II)

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For shipping add $5. in US; $10. outside US per package California residents add appropriate state sales tax Terms: Prepaid check, M/C or VISA or in US COD (UPS) Dealer inquiries invited Prices quoted do not include dealer installation & training Prices effective until May 1, 1981

Circle 156 on inquiry card.

Robots in Pelahatchie, Mississippi, has resumed publication of its quarterly newsletter.

Wristwatch-Sized Computer Proposed: Ten years ago, who would have conceived of the table-top computer or, better yet, the pocket computer? Yet they are realities today. Current dreams envision something much smaller: the November 1980 *Computer* carried a detailed proposal by Stephen Kearney for a computer to be worn on your wrist. Kearney has overcome the I/O (input/output) problem with a clearly thought out display and keyboard. The LCD (liquid-crystal display) is 27 characters by 8 lines (for a total of 216 characters), with uppercase, lowercase, and special characters, in a space 1⅞ by 3 inches. The unit has a 9-key keyboard capable of upper- and lowercase alphanumerics and special characters. The keyboard measures ⅞ inch by 2 inches.

Which Computer Is The Fastest?: *Datamation* recently conducted a survey to determine which computers are the fastest in production. The measurement used was KOPS (thousands of operations per second). This was felt to be a better measure than MIPS (millions of instructions per second). The top three were: Cray-1 (800,000 KOPS), CDC Cyber 205 (800,000 KOPS), and CDC 7600 (10,000 KOPS). The fastest IBM computer was the IBM 1088 (2X) with 1160 KOPS.

The KOPS rating is determined by measuring how long it takes the computer to execute a prescribed mix of programs; the measurement ignores I/O and operating-system considerations. As such, KOPS measures only processor speed and not system speed.

Smart Wheelchair Shown: The Rehabilitation Engineering Center of the Veterans Administration Hospital, Palo Alto, California, has demonstrated a prototype microprocessor-controlled wheelchair for severely incapacitated persons. Using autofocus ultrasonic-ranging detectors aimed at the head, a person can direct the wheelchair's movements by moving his head. Sensors are included to detect objects in the chair's path and to gauge distance to walls so that the chair can track a wall at a fixed distance. Cruise control is provided so that the user can relax until a change in velocity is wanted. The developers expect this unit to add only $100 to $200 to the cost of a standard wheelchair.

Flat-Panel Display Update: There are over 2 million video terminals in use. It's expected that yearly shipments will top the million-unit level by the mid-1980s. However, they have some big disadvantages. They're bulky, they waste a lot of desk space, consume too much power, annoy users with reflected light, and are damaged easily.

More than a dozen companies are developing flat-panel displays. Some are already in production. Most successful are the plasma displays. LCD and ELD (electroluminescent displays) are also being developed.

The Japanese are working on flat-panel displays. Fujitsu, Hitachi, Matsushita, and Seiko Denki have all produced plasma and LCD prototypes. Hycom Corporation, a US subsidiary of Sharp, has developed an ELD for the US Army in portable battlefield terminals. Exxon Corporation, through its Kylex and Electrophoretic Information Display divisions, is also developing flat displays. Kylex is already producing an 8-line LCD panel, and it is rumored that this will soon be expanded.

There is no doubt that by the end of the decade flat-panel displays will dominate the terminal- and television-display markets. They will offer low power consumption, high daylight visibility, and the shock resistance necessary to make the true portable computer and intelligent terminal a reality.

Can A Computer Have Worms? Several years ago rumor had it that an enterprising computer hacker had gained access to a DOD computer from a remote terminal. Once inside, he entered a program that rewrote its data into all of the computer's memory, destroying the computer's software and data base. In other words, the program was like the shapeless monster from the classic science-fiction thriller, *The Blob*.

Now, from Xerox's Palo Alto (California) Research Center, comes the "Worm." The Worm is a series of programs that wiggles through a computer network at will, copying itself into inactive systems in the network. The Worm coordinates the operation of all the computer systems in the network. It delegates tasks to unused machines and coordinates the operation of machines in the network. Any complex computations are handled by harnessing multiple processors.

The Worm is still in the experimental stage. As such, it may be the precursor of much more powerful autonomous programs that, like the Blob, could take over and control entire networks.

Computer Contest To Aid The Handicapped: The National Science Foundation, Johns Hopkins University, and Radio Shack have announced a nationwide competition for computer aids for the physically or mentally handicapped. (See "National Search to Aid the Handicapped Through Personal Computers," page 316.) The grand prize is $10,000, with runner-up prizes of equipment and money. There are several incentives to encourage participation, including separate entry categories for students, amateurs, and professionals. For more information, contact Personal Computers for the Handicapped, Johns Hopkins University, POB 670, Laurel MD 20810.

Robot Destroys Itself: An experimental robot at the University of Florida went out of control, destroying itself before a graduate student could press its cutoff button. The robot's arm was driven into its supporting body, ripping its shoulder off.

Xerox Introduces First Ethernet System: Xerox has been talking about Ethernet for two years, and I have reported on its progress many times. Finally, it has introduced the first system hardware. Called the Xerox System 8000, it allows users to create, file, print, and distribute documents and data to any and all users on the system. It allows many types of office equipment to be linked into an integrated local system via coaxial cable, and the system can be tied in to other external networks.

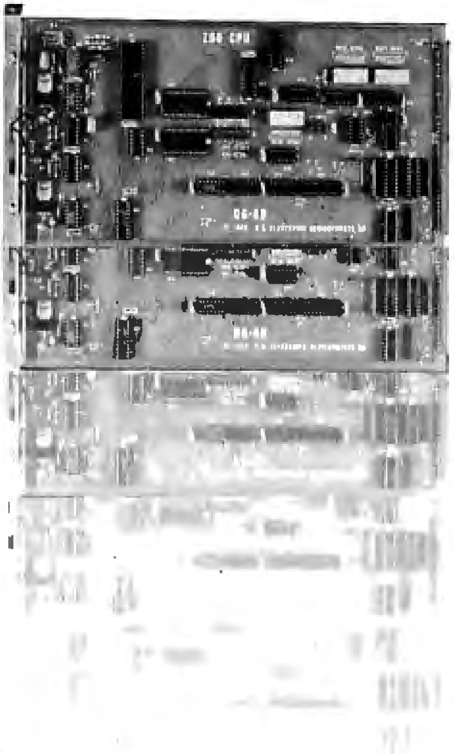
Without a doubt, many manufacturers will introduce hardware and software interfaces for the Ethernet system. IBM, Wang, Exxon, AT&T, and M/A-COM are working on their own local network systems.

IBM Opens Retail Stores: Philadelphia and Baltimore are the sites of IBM's two new storefront sales outlets. Several more are planned.

The stores carry typewriters, copiers, word processors, small-business computers, and supplies. IBM is following in the footsteps of

TOMORROW'S answers for the H8® TODAY!

DG Electronic Developments provides the only enhancements to put the Heath® H8 ahead ***TODAY*** while maintaining its high standards, broad flexibility and high reliability.

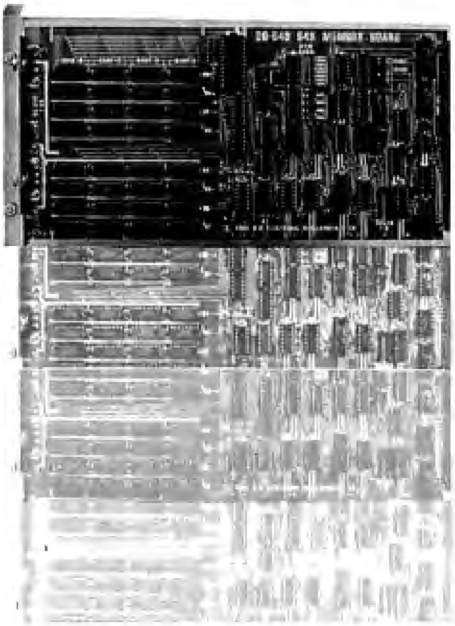


DG-80 (Z80® Based CPU)

The DG-80 offers the **BEST** foundation for the H8 to build on for the future. Compare the DG-80 to your current Heath® 8080 CPU and see the advantages of the DG-80's superior speed and flexibility. The Z80 gives twice the processing speed coupled with twice the instruction set making your H8 a truly professional microsystem. DG-80 aids the efficient writing of utility programs, user routines, sub-routines and use of assemblers.
DG-80 $249. (Documentation only $25.)

DG-FP8/ADP4 (DG80 Front Panel Monitor)

The DG-FP8/ADP4 firmware/hardware package brings the world of standardization to your H8. The FP8/ADP4 allows the full use of currently available "STANDARD" CPM software, with 4 MHz operation. You can still use your HDOS and all its related software, by simply putting a disk in your drive. The DG firmware package gives you use of the full 64K of RAM available on the 64D or 64D5. The FP8/ADP4 firmware also offers many extras including hexadecimal OR split octal display; simplification of register and memory contents display; and the full use of all Z80 registers (more than twice the number of registers in the 8080). Plus, the unique front-panel single-step feature is maintained to aid in software troubleshooting.
DG-FP8 $69.95. DG-ADP4 $19.95. Purchased together $79.95.
(Documentation only — source code not included $15.)



DG-64D (64K RAM Memory Board)

The DG-64D is **THE BEST** memory board available for the H8! Along with the DG-80 CPU, the 64D gives a full 64K of addressable memory. Its built-in flexibility ensures future compatibility. Multi-user configurations can be achieved accessing up to eight 64D's on line with the hardware/software bank select features. Memory contents are maintained and protected during extended wait states by asynchronous refresh.
DG-64D priced from $333 (0K) to $529 (64K). (Documentation only $15.)

DG-64D5 (5-Volt Power Supply 64K RAM)

The DG-64D5 memory board offers the **ultimate** in low power consumption for the H8 computer! The 64D5 is primarily designed for use with the Heath Color Graphics board. In addition to offering **ALL** of the features of the standard 64D, the 64D5 utilizes **single-supply** 5-volt-only dynamic RAMs and allows the use of extended wait states.
Priced from $333 (0K) to $799 (64K). (Documentation only $15.)
Chip Sets (8-4517 dynamic RAMS) $150.

CP/M (Standard V2.2 Disk Operating System)

The final component for the **"STANDARD"** H8 system is Digital Research's CP/M® V2.2. Our full line of H8 enhancements in combination with CP/M gives the user unparalleled flexibility and puts thousands of CP/M software programs at your fingertips.
CPM V2.2 $130. (Documentation only $25.)

All products supplied with complete documentation.

Please call or write for additional information.

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Ordering Information: Products listed available from DG Electronic Developments Co., P.O. Box 1124, 1827 South Armstrong, Denison, Tx. 75020. Check, Money Order, VISA or MasterCard accepted. Phone orders (charge only) call (214) 465-7805. No COD's. Freight prepaid. Allow 3 weeks for personal checks to clear. Texas residents add 5%. Foreign orders add 30%. Prices subject to change without notice.

DEC, even though DEC closed two of its retail outlets and has put a halt to its retail expansion.

In a related development, Hewlett-Packard has entered into an agreement to sell its HP-1000L small-business computer through ABC Computers Inc's 350 retail outlets.

Programmer Fined For Copying Software: A Mobile County, Alabama, circuit court has fined a programmer $50,000 for copying his former employer's software and using it in a competing business he started. A jury decided that a theft had occurred, even though nothing material was taken. The prosecution maintained that the former employee could not have re-created the identical programs in such a short period of time. The defense said he had done so. The programmer plans to appeal.

Personal Computing On Corporate Machines: Federal auditors discovered over 200 government employees at the Sandia Nuclear Weapons Research Center in Albuquerque, New Mexico, using the facility's Control Data Corporation systems for personal use. Sources report that 456 unauthorized files were located, including several hundred games such as *Star Trek* and *Adventure*, as well as poetry, jokes, personal letters, a beer-can collection catalog, and bowling-team rosters. One employee was caught helping local gamblers run a bookmaking operation.

Does Computer Crime Pay? It certainly does... according to Paul Nolan, supervisory special agent in the FBI's White Collar Crime Section. He estimates that non-computer-aided embezzlement averages $23,000 per occurrence, while computer-aided embezzlement averages $430,000. By the way, bank robbers average only $3000.

Volume Production For 64 K-Bit Memories: Within two months, suppliers will start shipping the new 64 K-bit programmable memories to manufacturers and distributors. Prices will be in the $25 to $30 range; they'll drop under $20 in July. Fifteen suppliers have announced devices, although some of the specification sheets are tentative.

It's not yet clear when personal-computer manufacturers will start using the 64 K-bit chips in place of 16 K-bit circuits. Many will stick with the 16 K-bit device until the 64 K units show a significant price drop.

Intel has let it be known that its 64 K-bit memories will use redundant bits for increased yield, the same technique used by IBM and Western Electric in their in-house circuits. Intel uses a "ROM-fuse" technique (an internal programmable read-only-memory) to decode addresses and replace one or more defective cells.

Ada Status Report: It is estimated that the DOD (Department of Defense) uses over 500 general-purpose computer languages and that $3 billion is spent each year for software development, whose control is a nightmare. That's what led the DOD to subsidize the Ada language project. The department wants Ada to be its only language.

In 1975, a DOD group undertook the task of evaluating twenty-three existing languages to find a standard language. None were found suitable. In mid-1978, the group invited specification recommendations from around the world and sponsored a competition among seventeen organizations. The Green language (later dubbed Ada), developed by Cii Honeywell Bull (a French subsidiary of Honeywell), emerged the winner. Initial specifications were released in mid-1979 and refined and completed by mid-1980.

A fully functional Ada compiler for the entire language is expected to be available next year. Many private and educational institutions are currently developing Ada compilers, including Carnegie-Mellon University and the University of Karlsruhe, West Germany. Other schools studying various aspects of Ada include Stanford, Harvard, MIT, and the Universities of Texas, Massachusetts, Southern California, Pennsylvania, York (England), Tokyo, London, and the Technical University of Denmark.

The DOD has requested that the Ada compiler run on the DEC (Digital Equipment Corporation) VAX11/780 and produce code for the VAX, the DEC PDP-11, and the military AN/GYK-12.

A number of institutions already have "Little Ada" compilers running, and it's likely that we'll see a "Tiny Ada" implementation for 8080/Z80 systems by year's end.

Ohio Scientific Sold: Ohio Scientific Inc (OSI), one of the early pioneers in personal-computing systems, has been purchased for an undisclosed sum by M/A-COM Inc of Burlington, Massachusetts. M/A-COM manufactures business communications equipment. OSI had sales of $14.8 million for the 10-month period ending October 1980. Mike Cheiky, OSI founder, will remain as vice-president of development. In all likelihood OSI will move away from personal computing and into the small-business market.

Random Rumors: Apple is rumored to be frantically working on a 16-bit computer system using the Motorola 68000.... Sony and Canon are about to introduce computers using the Motorola 6809 8-bit microprocessor.... Radio Shack may introduce a disk system for the TRS-80 Color Computer system.... According to insiders, Texas Instruments will soon have a low-cost system and a Viewdata-type terminal. TI is concerned over Radio Shack's growing domination of the consumer communications market.... Experts predict that Radio Shack will have 40,000 people hooked up to data bases through their equipment by year end....

The Apple III appears to be designed to accept one of the new 5¼-inch Winchester hard disks in place of its 5¼-inch floppy-disk drives.... Informed sources say that Zilog is at last shipping fully functional Z8000s. Reportedly, the first four versions had some op codes that did not execute correctly.... Sony and Matsushita are expected to introduce portable microcomputer products that fit into your briefcase. They are intended for electronic mail and database access applications. (See "The Panasonic and Quasar Hand-Held Computers," by Gregg Williams and Rick Meyer January 1981 BYTE, page 34.) ...Expect a CP/M-like operating system for Atari's 800 personal computer.... Okidata will unveil a 35 cps overlapping dot-matrix printer for under $1000 at the National Computer Convention in May....

MAIL: I receive a large number of letters each month as a result of this column. If you write to me and wish a response, please include a self-addressed, stamped envelope

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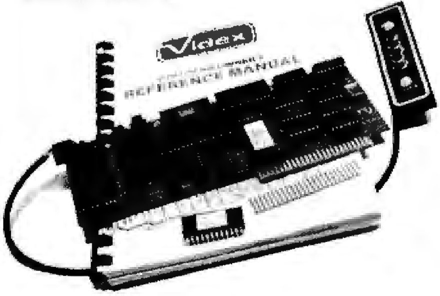
The Text Solution for APPLE II®

Now APPLE II® Owners Can Solve Text Problems With VIDEOTERM 80 Column by 24 Line Video Display Utilizing 7 X 9 Dot Character Matrix

Perhaps the most annoying shortcoming of the Apple II® is its limitation of displaying only 40 columns by 24 lines of text, all in uppercase. At last, Apple II® owners have a reliable, trouble-free answer to their text display problem. VIDEOTERM generates a full 80 columns by 24 lines of text, in upper and lower case. Twice the number of characters as the standard Apple II® display. And by utilizing a 7 by 9 character matrix, lower case letters have true descenders. But this is only the start.

VIDEOTERM, MANUAL, SWITCHPLATE



VIDEOTERM

BASICs VIDEOTERM lists BASIC programs, both Integer and Applesoft, using the entire 80 columns. Without splitting keywords. Full editing capabilities are offered using the ESCape key sequences for cursor movement. With provision for stop/start text scrolling utilizing the standard Control-S entry. And simultaneous on-screen display of text being printed.

Pascal Installation of VIDEOTERM in slot 3 provides Pascal immediate control of the display since Pascal recognizes the board as a standard video display terminal and treats it as such. No changes are needed to Pascal's MISC.INFO or GOTOXY files, although customization directions are provided. All cursor control characters are identical to standard Pascal defaults.

Other Boards The new Microsoft Softcard* is supported. So is the popular D. C. Hayes Micromodem II*, utilizing customized PROM firmware available from VIDEX. The powerful EasyWriter* Professional Word Processing System and other word processors are now compatible with VIDEOTERM. Or use the Mountain Hardware ROMWriter* (or other PROM programmer) to generate your own custom character sets. Naturally, VIDEOTERM conforms to all Apple OEM guidelines, assurance that you will have no conflicts with current or future Apple II* expansion boards.

Advanced Hardware Design VIDEOTERM's on-board asynchronous crystal clock ensures flicker-free character display. Only the size of the Pascal Language card, VIDEOTERM utilizes CMOS and low power consumption ICs, ensuring cool, reliable operation. All ICs are fully socketed for easy maintenance. Add to that 2K of on-board RAM, 50 or 60 Hz operation, and provision of power and input connectors for a light pen. Problems are designed out, not in.

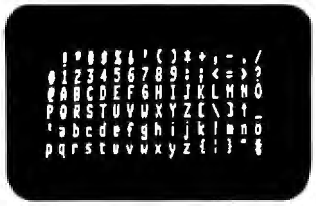
Available Options The entire display may be altered to inverse video, displaying black characters on a white field. PROMs containing alternate character sets and graphic symbols are available from Videx. A switchplate option allows you to use the same video monitor for either the VIDEOTERM or the standard Apple II* display, instantly changing displays by flipping a single toggle switch. The switchplate assembly inserts into one of the rear cut-outs in the Apple II* case so that the toggle switch is readily accessible. And the Videx KEYBOARD ENHANCER can be installed, allowing upper and lower case character entry directly from your Apple II* keyboard.

Firmware 1K of on-board ROM firmware controls all operation of the VIDEOTERM. No machine language patches are needed for normal VIDEOTERM use.

Firmware Version 2.0

Characters	7 x 9 matrix	Display	24 x 80 (full descenders)
Options	7 x 12 matrix option; Alternate user definable character set option; Inverse video option.		18 x 80 (7 x 12 matrix with full descenders)

7X12 MATRIX
18X80 OPTIONAL



7X9 MATRIX
24X80 STANDARD

Want to know more? Contact your local Apple dealer today for a demonstration. VIDEOTERM is available through your local dealer or direct from Videx in Corvallis, Oregon. Or send for the VIDEOTERM Owners Reference Manual and deduct the amount if you decide to purchase. Upgrade your Apple II* to full terminal capabilities for half the cost of a terminal. VIDEOTERM. At last.

Apple II* is a trademark of Apple Computer Inc.
ROMWriter* is a trademark of Mountain Hardware Inc.
Micromodem II* is a trademark of D. C. Hayes Associates Inc.
Softcard* is a trademark of Microsoft
EasyWriter* is a trademark of Information Unlimited Software Inc

PRICE:

• VIDEOTERM includes manual	$345
• SWITCHPLATE	$ 19
• MANUAL refund with purchase	$ 19
• 7 x 12 CHARACTER SET	$ 39
• MICROMODEM FIRMWARE	$ 25

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introducing the

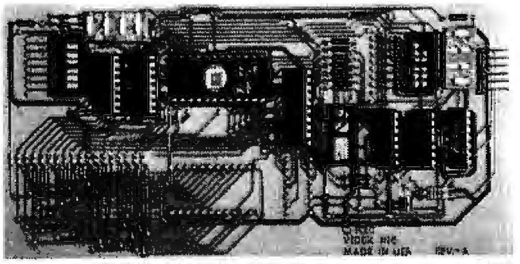
KEYBOARD & DISPLAY ENHANCER

- *PUT THE SHIFT AND SHIFT LOCK BACK WHERE IT BELONGS*
- *SEE REAL UPPER AND lower CASE ON THE SCREEN*
- *ACCESS ALL YOUR KEYBOARD ASCII CHARACTERS*

Videx has the perfect companion for your word processor software: the **KEYBOARD AND DISPLAY ENHANCER**. Install the enhancer in your APPLE II and be typing in lower case just like a typewriter. If you want an upper case character, use the SHIFT key or the CTRL key for shift lock. Not only that, but you see upper and lower case on the screen as you type. Perfectly compatible with Apple Writer and other word processors like, for example, Super-Text.

If you want to program in BASIC, just put it back into the alpha lock mode; and you have the original keyboard back with a few improvements. Now you can enter those elusive 9 characters directly from the keyboard, or require the Control key to be pressed with the RESET to prevent accidental resets.

KEYBOARD AND DISPLAY ENHANCER is recommended for use with all revisions of the APPLE II. It includes 6 ICs, and EPROM and dip-switches mounted on a PC board, and a jumper cable. Easy installation, meaning no soldering or cutting traces. Alternate default modes are dip-switch selectable. You can even remap the keyboard, selecting an alternate character set, for custom applications.



PRICE

• KDE-700 (REV. 7 or greater)	$129.
• KDE-000 (REV. 6 or less)	$129.

Apple II* is a trademark of Apple Computer, Inc.

Videx

VIDEX
897 N.W. Grant Avenue
Corvallis, Oregon 97330
Phone (503) 758-0521

VISA

Software Received

Apple II, PET, and TRS-80

B-1 Nuclear Bomber, historical strategy game for the Apple, PET, and TRS-80. Cassette, $14.95. Avalon Hill Game Company, 4517 Harford Rd, Baltimore MD 21214.

Planet Miners, strategy game for the Apple, PET, and TRS-80 (three versions sold together). Cassette, $14.95. Avalon Hill Game Company (see above).

TRS-80

Disk Editor/Assembler, line editor and relocatable machine-language assembler for the TRS-80. Floppy disk, $99.95. Radio Shack, 1 Tandy Ctr, Fort Worth TX 76102.

FORTRAN, programming language and utilities for the TRS-80. Floppy disk, $99.95. Radio Shack (see above).

Lost Ship Adventure, Adventure program for the TRS-80. Cassette, $14.95. The Programmer's Guild, POB 66, Peterborough NH 03458.

Profile, general-purpose data base and report writer for the TRS-80. Floppy disk, $79.95. Radio Shack (see above).

Real Estate Volume II, mortgage analysis program for the TRS-80. Cassette, $29.95. Radio Shack (see above).

Scripsit, word-processing package for the TRS-80. Floppy disk, $99.95. Radio Shack (see above).

Standard & Poor's Stockpak and Portfolio Management System, stock-analysis program for the TRS-80. Floppy disk, $49.95. Radio Shack (see above).

Star Trek 4.0, action game for the TRS-80. Cassette, $14.95. The Programmer's Guild (see above).

Superdisk, collection of utility programs for the TRS-80. Floppy disk, $49.95. The Programmer's Guild (see above).

VisiCalc, numerical computation and forecasting tool for the TRS-80. Floppy disk $99.95. Radio Shack (see above).

Texas Instruments 99/4

Early Learning Fun, educational activity for children for the TI 99/4. Floppy disk, $30. Texas Instruments, 13500 N Central Expy, Dallas TX 75231.

Personal Record Keeping, computer-based filing system for the TI 99/4. Program cartridge, $50. Texas Instruments (see above).

Speech Editor, speech synthesis aid for the TI 99/4. Program cartridge, $45. Texas Instruments (see above).

Other Computers

Nevada COBOL, version of the COBOL language for CP/M systems. Eight-inch floppy disk, $99.95. Ellis Computing, 1480 17th Ave, San Francisco CA 94122.

This is a list of software packages that have been received by BYTE Publications during the past month. The list is correct to the best of our knowledge, but it is not meant to be a full description of the product or the forms in which the product is available. In particular, some packages may be sold for several machines or in both cassette and floppy-disk format; the product listed here is the version received by BYTE Publications.

This is an all-inclusive list that makes no comment on the quality or usefulness of the software listed. We regret that we cannot review every software package we receive. Instead, this list is meant to be a monthly acknowledgment of these packages and the companies that sent them. Companies sending software packages must include the suggested list price of the packages and (where appropriate) the alternate forms in which they are available.

MULTI-USER OASIS HAS THE FEATURES PROS DEMAND. READ WHY.

(THEN COMPARE.)

Computer experts (the pros) usually have big computer experience. That's why when they shop system software for Z80 micros, they look for the big system features they're used to. And that's why they like Multi-User OASIS. You will too.

DATA INTEGRITY: FILE & AUTOMATIC RECORD LOCKING

The biggest challenge for any multi-user system is co-ordinating requests from several users to change the same record at the same time.

Without proper co-ordination, the confusion and problems of inaccurate or even destroyed data can be staggering.

Our File and Automatic Record Locking features solve these problems.

For example: normally all users can view a particular record at the same time. But, if that record is being updated by one user, automatic record locking will deny all other users access to the record until the up-date is completed. So records are always accurate, up-to-date and integrity is assured.

Pros demand file & automatic record locking. OASIS has it.

SYSTEM SECURITY: LOGON, PASSWORD & USER ACCOUNTING

Controlling who gets on your system and what they do once they're on it is the essence of system security.

Without this control, unauthorized users could access your programs and data and do what they like. A frightening prospect isn't it?

And multi-users can multiply the problem.

But with the Logon, Password and Privilege Level features of Multi-User OASIS, a system manager can specify for each user which programs and files may be accessed—and for what purpose.

Security is further enhanced by User Accounting—a feature that lets you keep a history of which user has been logged on, when and for how long.

Pros insist on these security features. OASIS has them.

EFFICIENCY: RE-ENTRANT BASIC

A multi-user system is often not even practical on computers limited to 64K memory.

OASIS Re-entrant BASIC makes it practical.

How?

Because all users use a single run-time BASIC module, to execute their compiled programs, less memory is needed. Even if you have more than 64K, your pay-off is cost saving and more efficient use of all the memory you have available—because it services more users.

Sound like a pro feature? It is. And OASIS has it.

AND LOTS MORE...

Multi-User OASIS supports as many as 16 terminals and can run in as little as 56K memory. Or, with bank switching, as much as 784K.

Multi-Tasking lets each user run more than one job at the same time.

And there's our BASIC—a compiler, interpreter and debugger all in one. An OASIS exclusive.

Still more: Editor; Hard & Floppy Disk Support; Keyed (ISAM), Direct & Sequential Files; Mail-Box; Scheduler; Spooler; all from OASIS.

Our documentation is recognized as some of the best, most extensive, in the industry. And, of course, there's plenty of application software.

Put it all together and it's easy to see why the real pros like OASIS. Join them. Send your order today.

OASIS

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OASIS IS AVAILABLE FOR

SYSTEMS: Altos; Compucorp; Cromemco; Delta Products; Digital Group; Digital Microsystems; Dynabyte; Godbout; IBC; Index; Intersystems; North Star; Onyx; SD Systems; TRS 80 Mod II; Vector Graphic; Vorimex.

CONTROLLERS: Bell Controls; Cameo; Corvus; Konan; **Micromation;** Micropolis; Tarbell; Teletek; Thinkertoys; X Comp

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free Application Software Directory.

PLEASE SEND ME:

Product	Price with Manual	Manual Only
OPERATING SYSTEM (Includes: EXEC Language; File Management; User Accounting; Device Drivers; Print Spooler; General Text Editor; etc.) SINGLE-USER MULTI-USER	 $150 350	 $17.50 17.50
BASIC COMPILER/ INTERPRETER/DEBUGGER	100	15.00
RE-ENTRANT BASIC COMPILER/INTERPRETER/ DEBUGGER	150	15.00
DEVELOPMENT PACKAGE (Macro Assembler; Linkage Editor; Debugger)	150	25.00
TEXT EDITOR & SCRIPT PROCESSOR	150	15.00
DIAGNOSTIC & CONVERSION UTILITIES (Memory Test; Assembly Language; Converters; File Recovery; Disk Test; File Copy from other OS; etc.)	100	15.00
COMMUNICATIONS PACKAGE (Terminal Emulator; File Send & Receive)	100	15.00
PACKAGE PRICE (All of Above) SINGLE-USER MULTI-USER	 500 850	 60.00 60.00
FILE SORT	100	15.00
COBOL-ANSI '74	750	35.00

Order OASIS from:

Phase One Systems, Inc.
7700 Edgewater Drive, Suite 830
Oakland, CA 94621
Telephone (415) 562-8085
TWX 910-366-7139

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Expiration Date__________
Signature__________

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■ *OS-9 Level One* runs on systems without memory management hardware having up to 56K memory.

☐ OS-9 Level Two $495* ☐ Level One $195

BASIC09™ PROGRAMMING LANGUAGE SYSTEM

Extended BASIC language compiler/interpreter with integrated text editor and debug package. Runs standard BASIC programs *or* minimally-modified PASCAL programs.

■ Permits multiple named program modules having local variables and identifiers. Modules are reentrant, position independent and ROMable.

■ Additional control statements for structured programming: IF ... THEN ... ELSE, FOR ... NEXT, REPEAT ... UNTIL, WHILE ... DO, LOOP ... ENDLOOP, EXITIF ... ENDEXIT.

■ Allows user-defined data types and complex data structures. Five built-in data types: byte, integer, 9 digit floating-point, string and boolean.

■ Runs under OS-9™ Level One or Level Two. ☐ $195*

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■ Interactive Assembler ■ Macro Text Editor

■ Interactive Debugger

BASIC09 and OS-9 are trademarks of Microware® and Motorola. UNIX is a trademark of Bell Laboratories.* Most software is available on ROM or diskette in versions for many popular 6809 computers. Contact Microware® for specific availability.

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5. On back (legs only)—50 Yds.
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7. Surface dive—underwater swim—20 Ft.
8. Disrobe—float with clothes—5 mins.
9. Long shallow dive.
10. Running front dive.
11. 10-minute swim.

Anybody who's taken a Red Cross swim course knows how tough it can be. There's a good reason.

We believe drowning is a serious business.

Last year alone, we taught 2,589,203 Americans not to drown—in the seven different swim courses we offer all across the country. (Incidentally, most of the teaching—as with almost everything American Red Cross does—is done by dedicated volunteers.)

A good many of the youngsters not only are learning to keep *themselves* safe. Thousands upon thousands of them are learning to become lifesavers.

And the life they save—may be your own.

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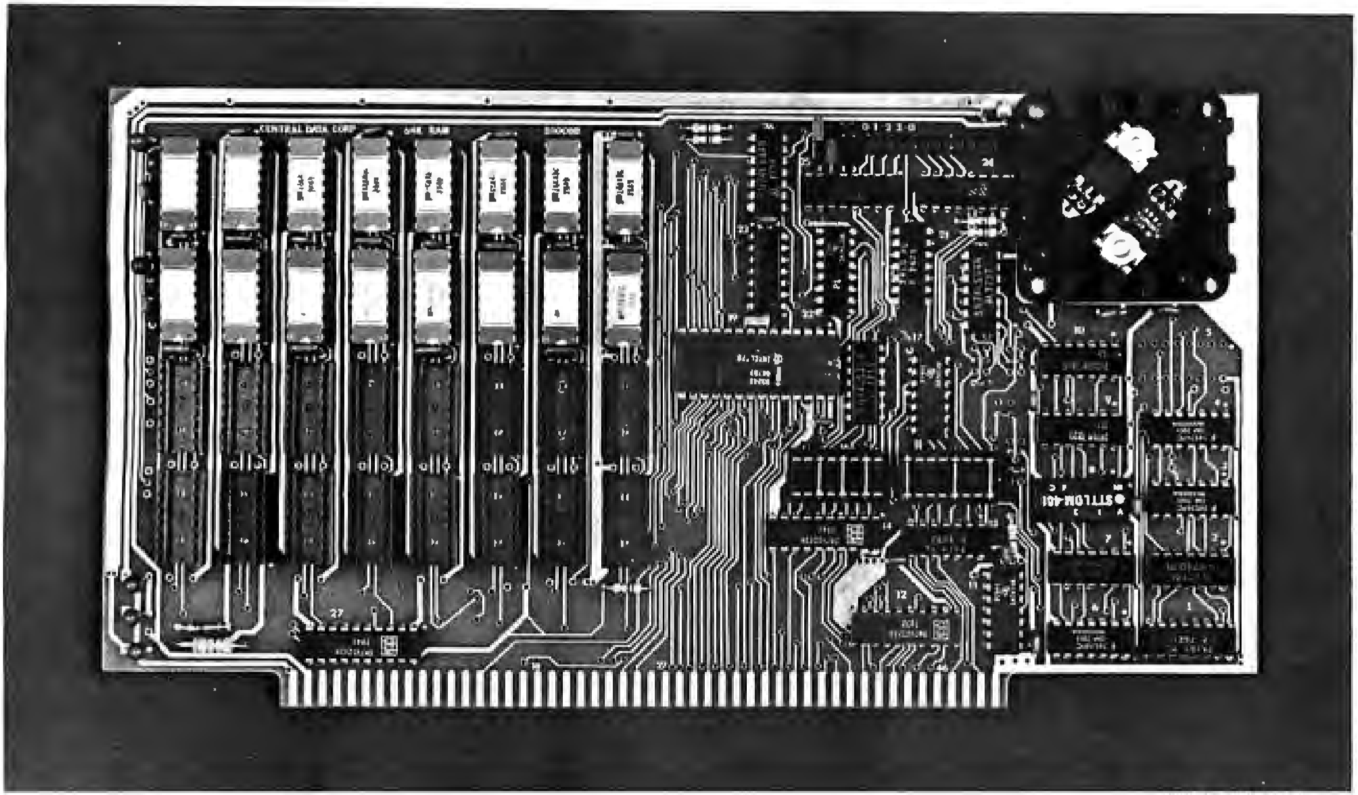

32K Board Pictured Above

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16K—$249	$259
32K—$375	$395
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We have now been shipping our 2MHz dynamic RAM boards for over two years. Hundreds of 4MHz boards have been going out every month since early 1979. Our reliability is proven in the thousands of systems which contain our board. Many quality-minded systems houses across the country and overseas are using our boards for their equipment.

Our prices still beat all. Despite rising 16K memory chip prices (at least from reputable suppliers), Central Data continues to give you the best buy in memory today. Nobody offers a board with a capacity of 64K, assembled, tested, and guaranteed for a full year at the price we do.

Deselect around PROMs. Our boards have the important deselect feature which lets you overlap any fixed memory in your system with no interference.

Our features make the board easily used and expanded. You address our boards on 16K boundaries with mini-jumps (small shorting plugs that slide over wire-wrap pins) near the top of the board for easy access. If you want to expand your board after you have purchased it, all that you need to do is add memory. We can supply you with expansion packages ($150-2MHz, $160-4MHz) which include eight RAMs that you can depend on as well as two mini-jumps for addressing. And of course, our board **never** generates wait states.

Low power consumption keeps your computer running cool and reliable. The total power consumption of our 16K board is typically less than 4 watts (+8V @ 300ma, +16V @ 150ma and −16V @ 20ma). Boards with additional memory typically increase power consumption only 1 watt per 16K!

Standard S-100 Interface. Our board is designed to interface with any standard S-100 CPU. All of the timing of the board is independent of the processor chip, and the board is set up for different processors by changing two plugs on the board.

Call or write us today. That will guarantee a fast response with more information on the board. Or make an order — you'll probably have the board in two weeks! **If you're interested, also ask for a catalog on our Z8000 16-bit processor board designed for the MULTIBUS.** All of these products are available to your local dealer, also.

Central Data Corporation, 713 Edgebrook Drive, PO Box 2530, Station A, Champaign, IL 61820. (217) 359-8010

Central Data

Circle 162 on inquiry card.

Books Received

Basic Computer Programs for Business, Volume I, Charles D Sternberg. Rochelle Park NJ: Hayden Book Company Inc, 1980; 25 by 20 cm, 264 pages; softcover, ISBN 0-8104-5162-X, $9.95.

Basic FORTRAN, James S Coan. Rochelle Park NJ: Hayden Book Company Inc, 1980; 15.5 by 23 cm, 248 pages, softcover, ISBN 0-8104-5168-9, $8.95.

Communicating with Microcomputers, Ian H Witten. London, England: Academic Press Inc Ltd, 1980; 15.5 by 23 cm, 164 pages, hardcover, ISBN 0-12-760750-1, $18; softcover, ISBN 0-12-760752-8, $10.50.

Computers and Programming Guide for Scientists and Engineers, second edition, Donald D Spencer. Indianapolis IN: Howard W Sams & Company Inc, 1980; 14 by 22 cm, 463 pages, softcover, ISBN 0-672-21693-0, $15.95.

The Computer in the School: Tutor, Tool, Tutee, Robert Taylor, editor. New York: Teachers College Press, 1980; 15.5 by 23.5 cm, 274 pages, softcover, ISBN 0-8077-2611-7, $14.95.

Computer/Law Journal, Volume II, Number 2, Jay Becker, editor. Los Angeles CA: Center for Computer/Law, 1980; 17.5 by 25.5 cm, 469 pages, softcover, ISSN 0164-8756, $16.

Designs of VMOS Circuits with Experiments, Robert T Stone and Howard M Berlin. Indianapolis IN: Howard W Sams & Company Inc, 1980; 14 by 22 cm, 174 pages, softcover, ISBN 0-672-21686-8, $10.95.

A Guide to FCC Equipment Authorizations, Willmar K Roberts. New Smyrna Beach FL: Willmar K Roberts, 4637 Van Kleeck Dr, 1980; 21.5 by 27.5 cm, 142 pages, softcover, ISBN none, $24.50 in North America, $29.50 elsewhere.

Introduction to Pascal, Including UCSD Pascal, Rodney Zaks. Berkeley CA: Sybex, 1980; 18 by 23 cm, 421 pages, softcover, ISBN 0-89588-050-4, $12.95.

Introduction to TRS-80 Level II BASIC and Computer Programming, Michael P Zabinski, PhD. Englewood Cliffs NJ: Prentice-Hall Inc, 1980; 22.5 by 29 cm, 186 pages, hardcover ISBN 0-13-499970-3, $14.95; softcover, ISBN 0-13-499962-2, $10.95.

Micromatics, Steven K Roberts. Elmwood CT: Scelbi Publications, 1980; 22 by 29 cm, 190 pages, hardcover, ISBN none, $19.95.

Modern Microprocessor System Design, Daniel R McGlynn. Somerset NJ: John Wiley & Sons, 1980; 22.5 by 29 cm, 295 pages, hardcover, ISBN 0471-06492-0, $21.95.

The Nature of Computation: An Introduction to Computer Science, Ira Pohl and Alan Shaw. Rockville MD: Computer Science Press Inc, 1981; 16 by 23.5 cm, 397 pages, hardcover, ISBN 0-914894-12-9, $16.95.

Owning Your Home Computer, Robert L Perry. New York: Everest House, 1980; 19 by 25.5 cm, 224 pages, softcover, ISBN 0-89696-093-5, $10.95.

Personal Computers Handbook, Walter H Buchsbaum, Sc D. Indianapolis IN: Howard W Sams & Company Inc, 1980; 14 by 22 cm, 286 pages, softcover, ISBN 0-672-21724-4, $11.95. ■

This is a list of books received at BYTE Publications during this past month. Although the list is not meant to be exhaustive, its purpose is to acquaint BYTE readers with recently published titles in computer science and related fields. We regret that we cannot review or comment on all the books we receive; instead, this list is meant to be a monthly acknowledgment of these books and the publishers who sent them.

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- FORM 2106 EMPLOYEE BUSINESS EXPENSE

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- FORM 1040 (LONG FORM)
- FORM 1040A (SHORT FORM)
- FORM 2106 EMPLOYEE BUSINESS EXPENSE
- FORM 2440 DISABILITY INCOME EXCLUSION
- FORM 2441 CREDIT FOR CHILD AND DEPENDENT CARE EXPENSES
- FORMS 3903 MOVING EXPENSE ADJUSTMENT
- FORM 4797 SUPPLEMENTAL SCHEDULE OF GAINS AND LOSSES
- SCHEDULE A ITEMIZED DEDUCTIONS
- SCHEDULE B INTEREST AND DIVIDENDS
- SCHEDULE C PROFIT (OR LOSS) FROM BUSINESS OR PROFESSION
- SCHEDULE D CAPITAL GAINS AND LOSSES
- SCHEDULE E SUPPLEMENTAL INCOME SCHEDULE
- SCHEDULE G INCOME AVERAGING
- SCHEDULES R & RP-CREDIT FOR THE ELDERLY
- SCHEDULE SE-COMPUTATION OF SOCIAL SECURITY SELF-EMPLOYMENT TAX
- SCHEDULE TC TAX COMPUTATION
- OUTPUT TO VIDEO OR LINE PRINTER
- FORMATS FOR TRACTOR FEED OR INDIVIDUAL FORM FEED PRINTERS
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☐ MODEL II PROFESSIONAL INCOME TAX PAC C ($199.95)

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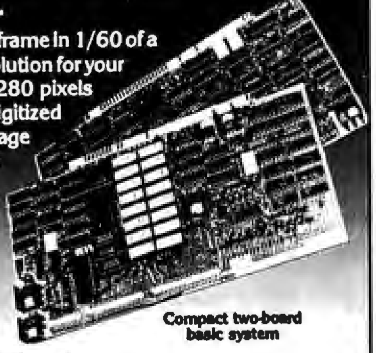
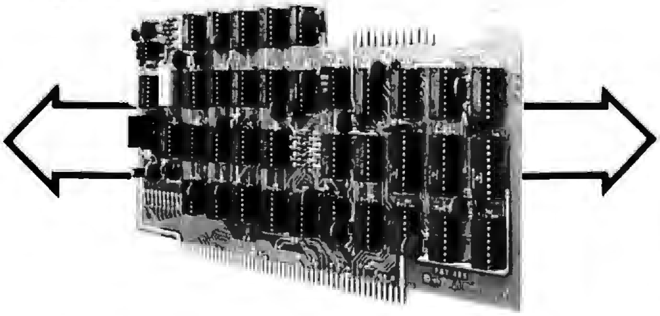


Compact two-board basic system

240x256 Digitized image, 16 levels

480x512 Computer-generated



Ask BYTE

Conducted by Steve Ciarcia

Modem Modification

Dear Steve,

I read "A Build-It-Yourself Modem for Under $50" (August 1980 BYTE, page 22) with great interest, as I do so many of your articles. Can the circuitry be modified easily to provide either *originate* or *answer* operation at the flick of a switch? From your article, it seems that the only difference between the originate and answer modes is the value of two capacitors in both the modulator and demodulator. If the values of these capacitors are switch-selected, then the modem could be either an originate- or an answer-only unit, as desired.

I have an uneasy feeling about several aspects of this scheme. Since you say that the capacitances are critical, will the switch capacitances cause trouble? Secondly, will the variable potentiometer settings be unique to each mode of operation, thus necessitating separate potentiometers for each switch setting?

It seems much more appealing to get expanded capability by buying a few additional components than by buying another complete set of components for both the modulator and demodulator.

Jonathan K Davis

An originate/answer modem is more complicated to build than it might seem at first. While, in theory at least, the answer functions can be added to the design by changing a few capacitors and resistors, the logistics of doing this presents a problem. The wires necessary to add these components and connect them through switches act like an antenna. Due to the high impedances in the circuit, it would probably become "swamped" with noise and cease reliable operation.

The only effective way to connect these components is through CMOS (complementary metal-oxide semiconductor) switches such as the 4052 dual 1-of-4 analog multiplexer, which are mounted close to the modem board. Separate potentiometer settings for answer and originate modes are necessary as well. If done as a printed circuit, the result is a more complicated and expensive board.

I won't tell you that simply installing components with a switch will not work, but I hesitate to suggest it. Success depends on your construction abilities.

As for the kit mentioned in the article, many experimenters seem to be purchasing two kits at once (they are still available). Apparently they intend to change a few components on the second board to make it "answer."

Also, instead of two speakers and two rubber

In "Ask BYTE," Steve Ciarcia answers questions on any area of microcomputing. The most representative questions received each month will be answered and published. Do you have a nagging problem? Send your inquiry to:

Ask BYTE
c/o Steve Ciarcia
POB 582
Glastonbury CT 06033

If you are a subscriber to The Source, send your questions by electronic mail or chat with Steve (TCE317) directly. Due to the high volume of inquiries, personal replies will be given as time permits. Please enclose a self-addressed, stamped envelope, and be sure to include "Ask BYTE" in the address.

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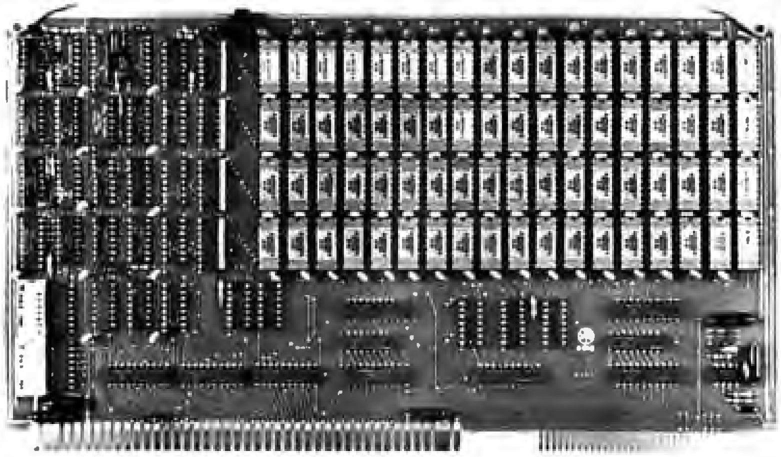

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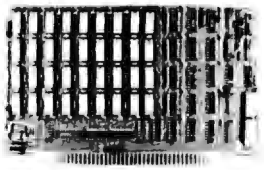

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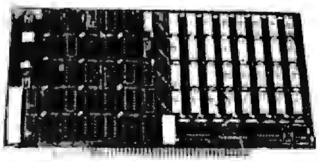
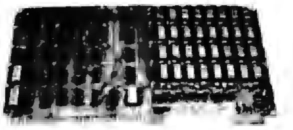


CI-S100 — 16KB to 64KB. Transparent hidden refresh. No wait states at 4 Mhz. Compatible with Alpha Micro and all Major 8080, 8085 and Z80 Based S100 Systems. Expandable to 512K bytes thru Bank Selections. **64K x 8 $750.00.**



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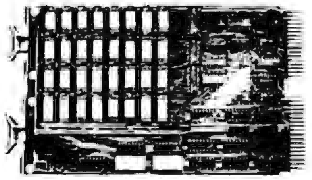

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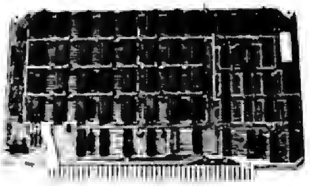

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Circle 168 on inquiry card.

*cushions in the coupler kit, MicroMint is shipping (at no extra cost) a ceramic microphone in place of one speaker. Even though I designed the prototype using an 8-ohm speaker as the "mike," the ceramic unit is far more reliable....*Steve

Communications

Dear Steve,

I am working on converting your biphase encoding/decoding circuits to use 8- instead of 4-bit words. (See "Hand-Held Remote Control for Your Computerized Home," July 1980 BYTE, page 22.) This approach looks promising, but I am not sure which communications medium I should use the circuits for. Radio is a possibility, but I really don't like the idea of having its interference. Infrared also looks good, but I am not sure about achieving long-range communications with it. To the best of my knowledge, the same holds true for ultrasonics. Can you suggest a particular system?

Also, in figure 3 of your article, there is a note next to the FSK OUTPUT saying that it can be connected to figure 5's input; however, figure 5 has two inputs labeled audio input modulation, plus and minus. Why?

Arthur Allen Gleckler

Any of the systems you list will work. For the most part, ultrasonics and infrared communication are limited to use in one room. If the experience of model-airplane builders is worth anything, 49 MHz radio control may be your best bet. Interference presents less of a problem if you use the "smarts" available with a microprocessor. Perhaps you should require that, for any command to be acted upon, it must be received correctly with a synchronization word before and after the command.

There are many coding schemes that insure you don't lose data. Rather than sending a single bit, you could send the same bit eight successive times. This makes for slow but reliable reception. Heathkit sells a variety of radio-control equipment that is adaptable to the task.

*Finally, in figure 5, the plus (+) lead would be connected to the biphase output of figure 3 and the minus (−) lead would be connected to ground....*Steve

BSR X-10

Dear Steve,

I read with interest your article "Computerize a Home." (See the January 1980 BYTE, page 28.)

Can you suggest references or other aids for pursuing the option of directly synthesizing the command-console waveform and transmitting it directly onto the AC line? This approach may be useful in an application for which I'm developing a product.

Jim Konsevich

It so happens that the cover article of the September 1980 issue of Radio Electronics *is about the BSR X-10. The article fully describes how to synthesize waveforms for direct injection into the AC line. It also has schematics of the command console and typical receivers. It should be just what you need.*

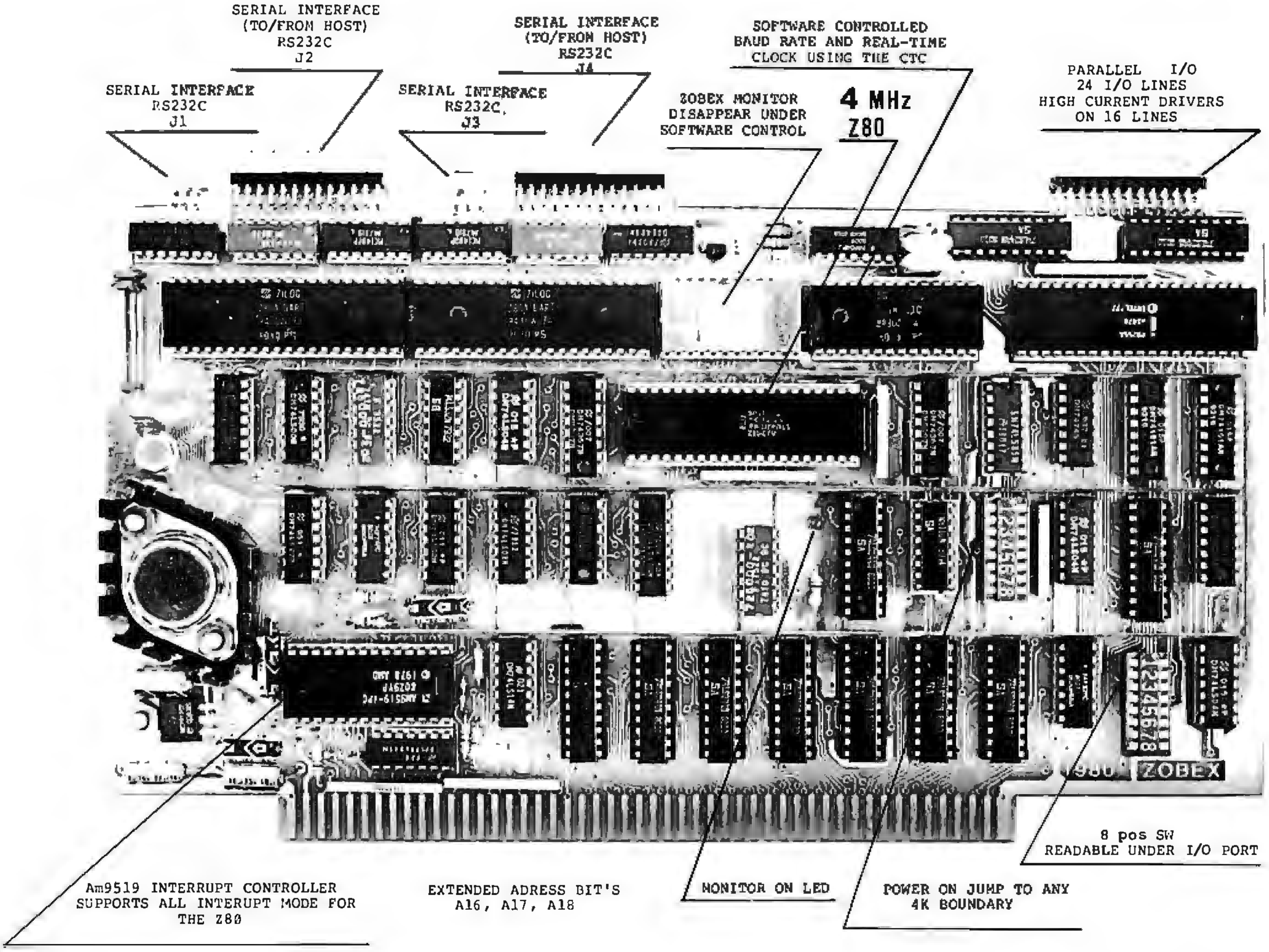
*By the way, I wrote the article....*Steve

Reference Needed

Dear Steve,

In your article "Computer-Controlled Security for Your Home" (January 1979 BYTE, page 56) you indicate an MM5369 in figure 4. I cannot find any reference or cross-reference for this device. It looks like an interesting unit; where can I get one and who manufactures it?

James Bush



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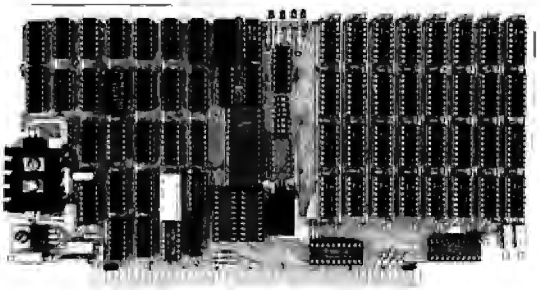

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Radio Shack sells the MM5369 as part number 276-1769, for $2.89. Radio Shack calls it an oscillator/divider. Be aware that the +12 V and ground-pin connections were listed incorrectly in the power-connection table. Pin 8 is the ground and pin 2 is +12 V.... **Steve**

Character Descension

Dear Steve,

I own a Radio Shack TRS-80 Level II with 16 K bytes of memory, and I have installed an uppercase/lowercase kit.

If you have seen a system with this kit, you probably noticed that the lowercase letters p, q, and y do not descend below the line. Actually, they are the same size as the uppercase letters. This can be irritating. To cure this, the character generator must be changed, but I have yet to find a compatible device to replace the old one. It must have the same characters (graphics, etc) and of course, the new p, q, and y. Please tell me where I can get such a device and its approximate cost?

Mark T Cruse

Apparently the device that you want is made by Motorola, but is proprietary to Radio Shack. The standard MCM6670 installed in TRS-80s is only available in quantities of 5000 or greater. There is the preprogrammed MCM6674 that is available, but it is a 5 by 7 matrix. Try ordering a new character generator directly from Radio Shack. I do not see any 5 by 9 dot-matrix 18-pin horizontal-scan character generators in the Motorola data manuals that would be applicable.

I asked a few non-Radio Shack TRS-80 dealers about this, and some expect to eventually carry it. All the new TRS-80s have a revised character generator installed, even though the descenders cannot be used without the uppercase/lowercase option.... **Steve**

Home Control

Dear Steve,

I work in software development for a videotext/electronic publishing concern. Hardware is not my area of expertise; however, I have done some minimal automation of my home, including a humidity-controlled bathroom fan. I anticipate using a computer-controlled BSR X-10, but mine will be different from yours. (See "Computerize a Home," January 1980 BYTE, page 28.) I plan to have my ultrasonic controller run through the computer to the X-10 unit. I hope to talk to the X-10 unit through an optoisolator that would replace the microphone in the unit.

The same technique can be applied to any remotely controllable consumer device. It avoids the potential conflicts between the various ultrasonic and infrared control methods used in televisions, turntables, cassette decks, and other products. In the future, a videodisk, a Telidon videotex terminal, and an electronic-music library will join the list of controlled devices. There will be an ultrasonic receiver in each room. To complement the computer control, each device will retain its local controls.

I am working on a computer-controllable preamplifier for my stereo, incorporating reed-switch relays and a voltage-controlled amplifier. Crown has a unit on the market, but it's a little too expensive. The preamplifier will lower its output by 20 dB whenever the telephone or the door is answered, etc.

I hope to stay with a single-board computer for the simple scheduling and control functions, but I have not yet calculated my memory requirements. I'm considering an SD Systems Z80 starter kit with an addi-

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- No restrictions to record size other than available RAM memory size.
- Instantaneous data record inquiry on indexed data records.
- Capable of selecting on any field or multiple fields with multiple selection criteria (fields do not have to be keyed).
- Mathematical manipulation of numeric data fields (add, subtract, multiply and divide).
- Capable of collecting information from multiple data files and generating a new data file or report.
- All menu driven.
- Capable of abstracting data from other programs written in other languages.
- Available now (off the shelf).

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Mike Ketcham, systems consultant and programmer for Management Information Systems: "FMS-80 allows me the flexibility of quickly creating programs for user applications. It is flexible, in that data can be entered in a form that the secretary recognizes and generates reports that the manager requires. Also, the user-definable menus allow me to actually generate a menu from which the user can select, creating a true turnkey system." **Tom Niccoli**, Partner, Computerland of Phoenix: "FMS-80 is flexible enough to acquire data from an application program that was previously written and allowed me to generate the reports that my customer needed. It closed the deal for me. Considering its capability, FMS-80 is one of the most cost-effective application programs available today."

If you're continuously asked to do applications programming, and you don't have the time to do it in Basic, consider FMS-80. For additional information on FMS-80, contact

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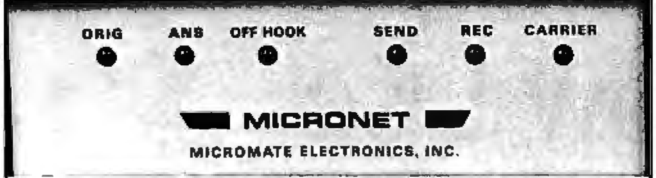

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Ask BYTE

tional memory and I/O (input/output) board. Am I too optimistic?

I plan to loosely couple the control computer to a more general-purpose computer, for advanced scheduling and control functions (perhaps including voice recognition). The general-purpose machine will be used as a programming terminal for work I do at home; I currently use a TI Silent 700. Whatever I get, it must have good graphics, because I want to use it as a Telidon terminal until the real thing gets to market. Incidentally, why are high-speed modems so expensive?

Putting intelligence into home applicances can make them more useful, as you so aptly demonstrate in your column. Putting that same intelligence behind a hand-held controller would offer still more advantages. I've had a lot of fun considering the human engineering aspects of a single hand-held controller wielding so much power.

Ian Smith

I appreciate your activities. I have been attempting a similar effort during the past year and a half. The BUSY BOX was specifically designed because I was getting tired of expensive hard-wired AC control. I started out with a single-board computer, but it has evolved into a 26 K-byte mainframe with sixteen I/O ports and many of the interfaces presented in my articles during the past year. It's quite possible to use a single-board computer, but you may find, as I did, that a larger unit accommodating a combination of assembly-language and BASIC programming is necessary. BASIC makes report generation much easier.

I too have been thinking of hand-held master controllers. I have a few designs and will probably have more articles on this subject in the near future. If you get something working in the meantime, let me know.

High-speed modems must pack a lot of information into a limited bandwidth and recover this information, often in noisy environments. The high cost is a function of the increased circuit complexity necessary to accomplish this feat. I wish you luck in your venture.

...**Steve** ■

And then there were none.

The list of already extinct animals grows . . . the great auk, the Texas gray wolf, the Badlands bighorn, the sea mink, the passenger pigeon . . .
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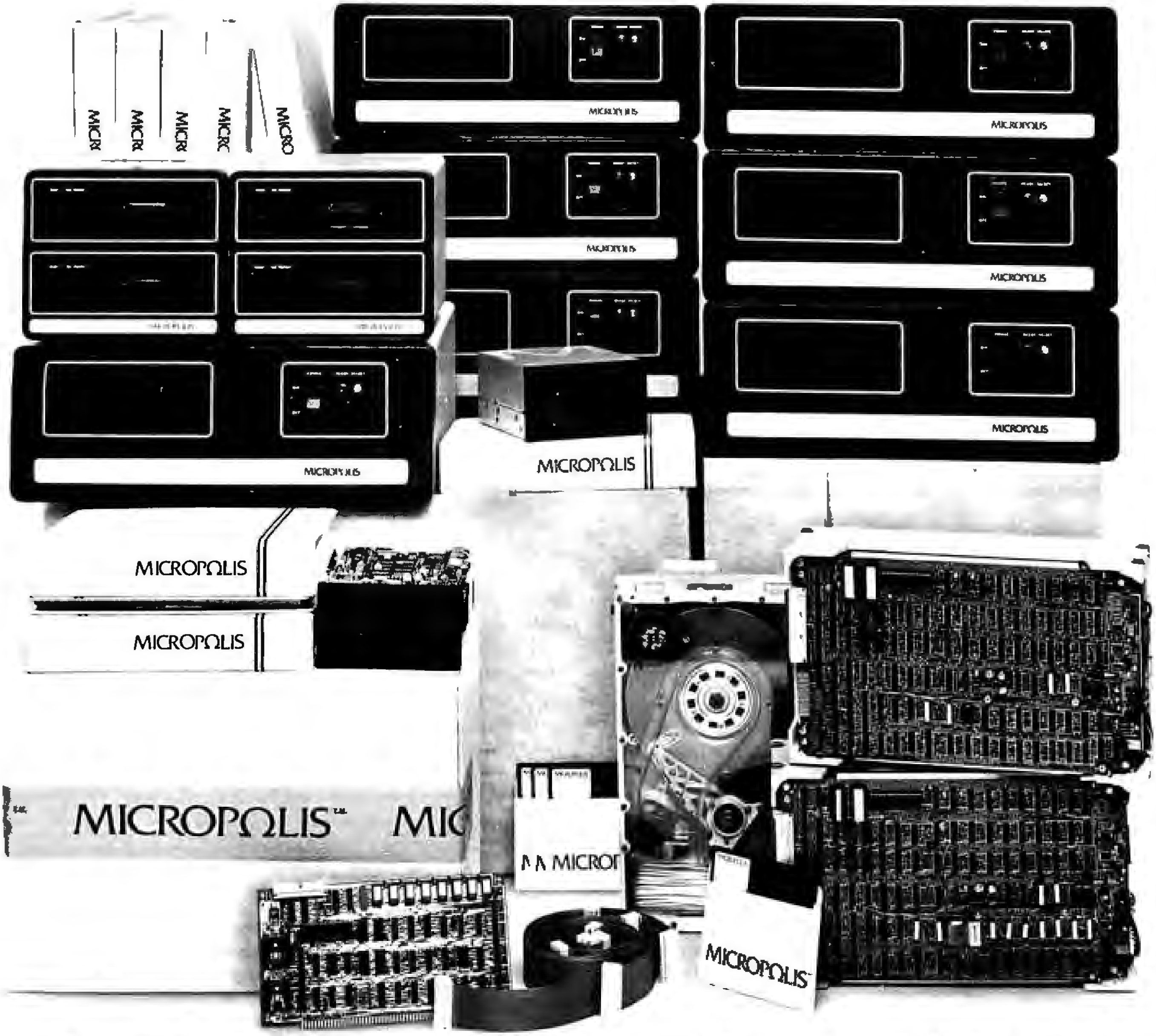

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A Simple Approach to Data Smoothing

Fred Ruckdeschel and Janice A Krinsky
c/o BYTE
POB 372
Hancock NH 03449

Existing trends in data may not be visible because they are masked by statistical fluctuations.

The storage and processing of data has become a major activity in modern society. Computers have created an increasing demand for data because of their highly organized storage and retrieval facilities. Computers have also provided a means for rapidly transforming data into a format that emphasizes particular aspects of the underlying information. *Data* and *information* as used in this context are not synonymous terms. The word *data* refers to sets of numbers. *Information* is the knowledge that may be derived from those numbers.

Data appears in many forms. For example, a person interested in stocks may have a history of daily quotations for a particular company. A businessman may have a weekly sales record for each item in his inventory. A hospital administrator may have a record of emergency admittances. A scientist may have a table of results from a series of experimental measurements. All these types of data, when plotted against time (or another *independent variable*), may contain information regarding trends. However, existing trends in the data may not be visible because they are masked by statistical fluctuations, which are often a component of any real-world measurement.

Month	1978 Sales Volume
January	3279
February	2421
March	4864
April	3629
May	3180
June	4744
July	6181
August	3653
September	3418
October	1722
November	1235
December	2408

Table 1: *1978 sales data for a hypothetical company. The figures indicate that the product being sold has an obvious seasonal appeal.*

The importance of somehow removing the "noise" (or statistical fluctuation) from the data may be seen by using a simple example. Consider the monthly sales-volume data for a new business or product as shown in table 1. The data clearly indicates that the sales generally peak in the summer, with a slump in late autumn. Plotting the data, as shown in figure 1, demonstrates the basic seasonal nature of the sales volume. If this data were to be used to supply information regarding the number of units that should be ready for sale for July of the next year, several factors would have to be taken into account, the first of which is the "noise" in the data.

As the sales are assumed to have started in January 1978, there is no previous history that can be used to directly measure the noise by a monthly comparison. Thus the noise must be extracted using the data given. If there is no reason to expect sales to be *statistically* much different during the next year, we can use the smoothed results for 1978 to predict 1979. If the raw data value of 6181 units were prepared for July 1979, there is a chance for that number to be too high, with a corresponding penalty to be paid (eg: bank interest) for maintaining the inventory. Thus, a more realistic estimate is required.

Predicting Future Performance

One approach to obtaining sales estimates is to assume a functional form for the average sales-volume behavior and perform a regression. One mathematical form which might be tried is:

$$S(t) = A + B \times \sin\{\ 2\pi(t+t_0)/12\ \} \qquad (1)$$

where $t=1$ represents January, $t=2$ represents February, and so on. A regression using $S(t)$ could be performed that minimizes the sum of the squares of the differences between the true values and the ones eventually calculated using $S(t)$. The regressed coefficients would then be A, B, and t_0, and the desired estimate for July 1979 is then $S(7)$.

There are two practical considerations that make this approach less than ideal for the average businessman. First, though the form of $S(t)$ given above may be appropriate, it is simply a guess. Second, few businessmen have the knowledge, facilities, or inclination for doing

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HEARTS 1.5 (Available for all computers) Price: $14.95 Cassette/$18.95 Diskette

An exciting and entertaining computer version of this popular card game. Hearts is a trick-oriented game in which the purpose is not to take any hearts or the queen of spades. Play against two computer opponents who are armed with hard-to-beat playing strategies.

STUD POKER (ATARI only) Price: $11.95 Cassette/$15.95 Diskette

This is the classic gambler's card game. The computer deals the cards one at a time and you (and the computer) bet on what you see. The computer does not cheat and usually bets the odds. However, it sometimes bluffs! Also included is a five card draw poker betting practice program. This package will run on a 16K ATARI. Color, graphics, sound.

POKER PARTY (Available for all computers) Price: $17.95 Cassette/$21.95 Diskette

POKER PARTY is a draw poker simulation based on the book, POKER, by Oswald Jacoby. This is the most comprehensive version available for microcomputers. The party consists of yourself and six other (computer) players. Each of these players (you will get to know them) has a different personality in the form of a varying propensity to bluff or fold under pressure. Practice with POKER PARTY before going to that expensive game tonight! Apple Cassette and diskette versions require a 32 K (or larger) Apple II.

VALDEZ (Available for all computers) Price: $14.95 Cassette/$18.95 Diskette

A simulation of supertanker navigation in the Prince William Sound and Valdez Narrows. The program uses an extensive 256X256 element radar map and employs physical models of ship response and tidal patterns. Chart your own course through ship and iceberg traffic. Any standard terminal may be used for display.

FLIGHT SIMULATOR (Available for all computers) Price: $17.95 Cassette/$21.95 Diskette

A realistic and extensive mathematical simulation of take-off, flight and landing. The program utilizes aerodynamic equations and the characteristics of a real airfoil. You can practice instrument approaches and navigation using radials and compass headings. The more advanced flyer can also perform loops, half-rolls and similar aerobatic maneuvers.

CRIBBAGE 2.0 (TRS-80 only) Price: $14.95 Cassette/$18.95 Diskette

This is a well-designed and nicely executed two-handed version of the classic card game, cribbage. It is an excellent program for the cribbage player in search of a worthy opponent as well as the beginner wishing to learn the game, in particular the scoring and jargon. The standard cribbage score board is continually shown at the top of the display (utilizing the TRS-80's graphics capabilities), with the cards shown underneath. The computer automatically scores and also announces the points using the traditional phrases.

CHESS MASTER (North Star and TRS-80 only) Price: $19.95 Cassette/$23.95 Diskette

This complete and very powerful program provides five levels of play. It includes castling, en passant captures and the promotion of pawns. Additionally, the board may be preset before the start of play, permitting the examination of "book" plays. To maximize execution speed, the program is written in assembly language (by SOFTWARE SPECIALISTS of California). Full graphics are employed in the TRS-80 version, and two widths of alphanumeric display are provided to accommodate North Star users.

STARTREK 3.2 (Available for all computers) Price: $ 9.95 Cassette/$13.95 Diskette

This is the classic Startrek simulation, but with several new features. For example, the Klingons now shoot at the Enterprise without warning while also attacking starbases in other quadrants. The Klingons also attack with both light and heavy cruisers and move when shot at! The situation is hectic when the Enterprise is besieged by three heavy cruisers and a starbase S.O.S. is received! The Klingons get even!

SPACE TILT (Apple only) Price: $10.95 Cassette/$14.95 Diskette

Use the game paddles to tilt the plane of the TV screen to "roll" a ball into a hole in the screen. Sound simple? Not when the hole gets smaller and smaller! A built-in timer allows you to measure your skill against others in this habit-forming action game.

GAMES PACK I (Available for all computers) Price: $9.95 Cassette/$13.95 Diskette

GAMES PACK I contains the classic computer games of BLACKJACK, LUNAR LANDER, CRAPS, HORSERACE, SWITCH and more. These games have been combined into one large program for ease in loading. They are individually accessed by a convenient menu.

GAMES PACK II (Available for all computers) Price: $9.95 Cassette/$13.95 Diskette

GAMES PACK II includes the games CRAZY EIGHTS, JOTTO, ACEY-DUCEY, LIFE, WUMPUS and others. As with GAMES PACK I, all the games are loaded as one program and are called from a menu.

Why pay $7.95 or more per program when you can buy a DYNACOMP collection for just $9.95?

NOMINOES JIGSAW (TRS-80 only) Price: $16.95 Cassette/$20.95 Diskette

NOMINOES JIGSAW is an intriguing and sophisticated graphical puzzle. The jigsaw consists of a 9 by 9 board partially filled with randomly chosen shapes (nominoes), of which there are 60 types. By knowing that the shapes must be legally connected, and by guessing the shape at each location, all the nominoes may be eventually deduced. Scoring is based on the number of guesses required and the difficulty of the board set-up.

MOVING MAZE (Apple only) Price: $10.95 Cassette/$14.95 Diskette

MOVING MAZE employs the games paddles to direct a puck from one side of a maze to the other. However, the maze is dynamically (and randomly) built and is continually being modified. The objective is to cross the maze without touching (or being hit by) a wall. Scoring is by an elapsed time indicator, and three levels of play are provided.

BLACK HOLE (Apple only) Price: $14.95 Cassette/$18.95 Diskette

This is an exciting graphical simulation of the problems involved in closely observing a black hole with a space probe. The object is to enter and maintain, for a prescribed time, an orbit close to a small black hole. This is to be achieved without coming so near the anomaly that the tidal stress destroys the probe. Control of the craft is realistically simulated using side jets for rotation and main thrusters for acceleration. This program employs Hi-Res graphics and is educational as well as challenging.

TEACHER'S PET I (Available for all computers) Price: $ 9.95 Cassette/$13.95 Diskette

This is the first of DYNACOMP's educational packages. Primarily intended for pre-school to grade 3, TEACHER'S PET provides the young student with counting practice, letter-word recognition and three levels of math skill exercises.

CRYSTALS (ATARI only) Price: $ 9.95 Cassette/$13.95 Diskette

A unique algorithm randomly produces fascinating graphics displays accompanied with tones which vary as the patterns are built. No two patterns are the same, and the combined effect of the sound and graphics are mesmerizing. CRYSTALS has been used in local stores to demonstrate the sound and color features of the Atari.

CRANSTON MANOR ADVENTURE (North Star only) Price: $19.95

At last! A comprehensive Adventure game for the North Star. CRANSTON MANOR ADVENTURE takes you into mysterious CRANSTON MANOR where you attempt to gather fabulous treasures. Lurking in the manor are wild animals and robots who will not give up the treasures without a fight. The number of rooms is greater and the associated descriptions are much more elaborate than the current popular series of Adventure programs, making this game the top in its class. Play can be stopped at any time and the status stored on diskette. Requires 32K.

NORTH STAR SOFTWARE EXCHANGE (NSSE) LIBRARY Price $9.95 Diskette

DYNACOMP now distributes the 20+ volume NSSE library. Most of these diskettes offer an outstanding value for the purchase price. Write for details regarding the contents of this library and quantity (four or more) purchases.

Availability

DYNACOMP software is supplied with complete documentation containing clear explanations and examples. Unless otherwise specified, all programs will run within 16K program memory space (ATARI requires 24K). Except where noted, programs are available on ATARI, PET, TRS-80 (Level II) and Apple (Applesoft) cassette and diskette as well as North Star single density (double density compatible) diskette. Additionally, most programs can be obtained on standard (IBM format) 8" CP/M floppy disks for systems running under MBASIC.

BUSINESS and UTILITIES

MAIL LIST II (Apple and North Star diskettes only) Price: $21.95

This many-featured program now includes full alphabetic and zip code sorting as well as file merging. Entries can be retrieved by user-defined code, client name or Zip Code. The printout format allows the use of standard size address labels. Each diskette can store more than 1100 entries (single density North Star or Apple DOS 3.2; over 2200 with double density North Star or Apple DOS 3.3)!

FORM LETTER SYSTEM (FLS) (Apple and North Star diskette only) Price: $17.95

FLS may be employed to generate individually addressed form letters. The user creates the address file and separately composes the letter. FLS will then print form letters using each address. FLS is completely compatible with MAIL LIST II, which may be used to manage your address files.

FLS and MAIL LIST II are available as a combined package for $37.95.

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An easy to use, line-oriented text editor which provides variable line widths and simple paragraph indexing. This text editor is ideally suited for composing letters and is quite capable of handling much larger jobs. Available for all computers.

PERSONAL FINANCE SYSTEM (ATARI only) Price: $34.95 Diskette

PFS is a single disk menu oriented system composed of 10 programs designed to organize and simplify your personal finances. Features include a 300 transaction capacity; fast access; 20 optional user codes; data retrieval by month, code or payee; optional printing of reports; checkbook balancing; bar graph plotting and more. Also provided on the diskette is ATARI DOS 2.

FINDIT (North Star only) Price: $19.95

This is a three-in-one program which maintains information accessible by keywords of three types. Personal (eg: last name), Commercial (eg: plumbers) and Reference (eg: magazine articles, record albums, etc). In addition to keyword searches, there are birthday, anniversary and appointment searches for the personal records and appointment searches for the commercial records. Reference records are accessed by a single keyword or by cross-referencing two or three keywords.

DFILE (North Star only) Price: $19.95

This handy program allows North Star users to maintain a specialized data base of all files and programs in the stack of disks which invariably accumulates. DFILE is easy to set up and use. It will organize your disks to provide efficient locating of the desired file or program.

COMPARE (North Star only) Price: $12.95

COMPARE is a single disk utility software package which compares two BASIC programs and displays the file sizes of the programs in bytes, the lengths in terms of the number of statement lines, and the line numbers at which various listed differences occur. COMPARE permits the user to examine versions of his software to verify which are the more current, and to clearly identify the changes made during development.

COMPRESS (North Star only) Price: $12.95

COMPRESS is a single-disk utility program which removes all unnecessary spaces and (optionally) REMark statements from North Star BASIC programs. The source file is processed one line at a time, thus permitting very large programs to be compressed using only a small amount of computer memory. File compressions of 20-30% are commonly achieved.

GRAFIX (TRS-80 only) Price: $12.95 Cassette/$16.95 Diskette

This unique program allows you to easily create graphics directly from the keyboard. You "draw" your figure using the program's extensive cursor controls. Once the figure is made, it is automatically appended to your BASIC program as a string variable. Draw a "happy face", call it H$ and then print it from your program using PRINT H$! This is a very easy way to create and save graphics.

TIDY (TRS-80 only) Price: $10.95 Cassette/$14.95 Diskette

TIDY is an assembly language program which allows you to renumber the lines in your BASIC programs. TIDY also removes unnecessary spaces and REMark statements. The result is a compacted BASIC program which uses much less memory space and executes significantly faster. Once loaded, TIDY remains in memory; you may load any number of BASIC programs without having to reload TIDY!

STATISTICS and ENGINEERING

DATA SMOOTHER (Not available for ATARI) Price: $14.95 Cassette/$18.95 Diskette

This special data smoothing program may be used to rapidly derive useful information from noisy business and engineering data which are equally spaced. The software features choice in degree and range of fit, as well as smoothed first and second derivative calculation. Also included is automatic plotting of the input data and smoothed results.

FOURIER ANALYZER (Available for all computers) Price: $14.95 Cassette/$18.95 Diskette

Use this program to examine the frequency spectra of limited duration signals. The program features automatic scaling and plotting of the input data and results. Practical applications include the analysis of complicated patterns in such fields as electronics, communications and business.

TFA (Transfer Function Analyzer) Price: $19.95 Cassette/$23.95 Diskette

This is a special software package which may be used to evaluate the transfer functions of systems such as hi-fi amplifiers and filters by examining their response to pulsed inputs. TFA is a major modification of FOURIER ANALYZER and contains an engineering oriented decibel versus log-frequency plot as well as data editing features. Whereas FOURIER ANALYZER is designed for educational and scientific use, TFA is an engineering tool. Available for all computers.

HARMONIC ANALYZER (Available for all computers) Price: $24.95 Cassette/$28.95 Diskette

HARMONIC ANALYZER was designed for the spectrum analysis of repetitive waveforms. Features include data file generation, editing and storage/retrieval as well as data and spectrum plotting. One particularly unique facility is that the input data need not be equally spaced or in order. The original data is sorted and a cubic spline interpolation is used to create the data file required by the FFT algorithm.

FOURIER ANALYZER, TFA and HARMONIC ANALYZER may be purchased together for a combined price of $44.95 (three cassettes) and $56.95 (three diskettes).

REGRESSION I (Available for all computers) Price: $19.95 Cassette/$23.95 Diskette

REGRESSION I is a unique and exceptionally versatile one-dimensional least squares "polynomial" curve fitting program. Features include very high accuracy; an automatic degree determination option; an extensive internal library of fitting functions; data editing; automatic data and curve plotting; a statistical analysis (eg: standard deviation, correlation coefficient, etc.) and much more. In addition, new fits may be tried without reentering the data. REGRESSION I is certainly the cornerstone program in any data analysis software library.

REGRESSION II (PARAFIT) (Available for all computers) Price: $19.95 Cassette/$23.95 Diskette

PARAFIT is designed to handle those cases in which the parameters are imbedded (possibly nonlinearly) in the fitting function. The user simply inserts the functional form, including the parameters (A(1), A(2), etc.) as one or more BASIC statement lines. Data and results may be manipulated and plotted as with REGRESSION I. Use REGRESSION I for polynomial fitting, and PARAFIT for those complicated functions.

MULTILINEAR REGRESSION (MLR) (Available for all computers) Price: $19.95 Cassette
$23.95 Diskette

MLR is a professional software package for analyzing data sets containing two or more linearly independent variables. Besides performing the basic regression calculation, this program also provides easy to use data entry, storage, retrieval and editing functions. In addition, the user may interrogate the solution by supplying values for the independent variables. The number of variables and data size is limited only by the available memory.

REGRESSION I, II and MULTILINEAR REGRESSION may be purchased together for $49.95 (three cassettes) or $61.95 (three diskettes).

BASIC SCIENTIFIC SUBROUTINES, Volume I (Not available for ATARI)

DYNACOMP is the exclusive distributor for the software keyed to the text *BASIC Scientific Subroutines, Volume I* by F. Ruckdeschel (see the BYTE/McGraw-Hill advertisement in BYTE magazine, January 1981). These subroutines have been assembled according to chapter. Included with each collection is a menu program which selects and demonstrates each subroutine.

Collection #1: Chapters 2 and 3: Data and function plotting, complex variables
Collection #2: Chapter 4: Matrix and vector operations
Collection #3. Chapters 5 and 6: Random number generators, series approximations
Price per collection: $14.95 Cassette/$18.95 Diskette

All three collections are available for $39.95 (three cassettes) and $49.95 (three diskettes).

Because the text is a vital part of the documentation, *BASIC Scientific Subroutines, Volume I* is available from DYNACOMP for $19.95 plus 75¢ postage and handling.

ROOTS (Available for all computers) Price $9.95 Cassette/$13.95 Diskette

In a nutshell, ROOTS simultaneously determines all the zeroes of a polynomial having real coefficients. There is no limit on the degree of the polynomial, and because the procedure is iterative, the accuracy is generally very good. No initial guesses are required as input, and the calculated roots are substituted back into the polynomial and the residuals displayed.

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*TRS-80 diskettes are not supplied with DOS or BASIC

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---

* *ATARI, PET, APPLE II, TRS-80, NORTH STAR, CP/M and IBM are registered trade names and/or trademarks*

Circle 176 on inquiry card.

Listing 1: *Listing of program for data smoothing. This program was written in North Star BASIC, version 6, release 4. To make the software portable to other machines, only a subset of the language was used. In most cases, only the statement delimiters, backslashes, need to be changed to colons, and certain commas changed to semicolons (in print statements) to get this program to operate in other BASICs (in particular, Microsoft BASIC).*

```
1 REM
2 REM
3 REM DATA SMOOTHING PROGRAM
4 REM
5 REM BY F.R. RUCKDESCHEL
6 REM
7 REM
8 REM
9 REM
10 DIM B(5,3),C(8,91),D(70),E(8)
11 REM DIMENSION OF D,Y AND Y1 MAY HAVE TO
12 REM INCREASED FOR LARGE SETS.
13 DIM U(8),V(8,12),W(12),Y(70),Y1(70)
14 PRINT
15 PRINT
16 PRINT 'DATA SMOOTHER FOR EQUALLY'
17 PRINT 'SPACED DATA SETS'
18 PRINT
19 PRINT
20 PRINT 'INPUT THE NUMBER OF'
21 PRINT 'DATA POINTS IN SET: ',
22 INPUT N4
23 PRINT
24 PRINT 'HOW MANY POINTS ARE'
25 PRINT 'TO BE AVERAGED OVER: ',
26 INPUT N3
27 PRINT
28 PRINT 'WHAT IS THE DESIRED LEVEL'
29 PRINT 'OF FIT (1,2,3,4,5): ',
30 INPUT N1
31 PRINT
32 PRINT 'WHAT IS THE DESIRED'
33 PRINT 'DERIVATIVE (0,1,2,3): ',
34 INPUT N2
35 REM CHECK FOR ERRORS
36 REM DETERMINE TABLE
37 GOSUB 169
38 REM CHECK ERROR CODES
39 GOSUB 193
40 PRINT
41 PRINT
42 IF E=0 THEN GOTO 50
43 PRINT '*** ERROR IN INPUT ***'
44 PRINT '    ERROR CODE',E
45 PRINT
46 PRINT 'RESTART'
47 PRINT
48 GOTO 20
49 REM IF THIS POINT PASSED, OK
50 PRINT
51 PRINT 'INPUT DATA AS PROMPTED:'
52 PRINT
53 FOR K=1 TO N4
54 PRINT K,TAB(6),
55 INPUT Y(K)
56 NEXT K
57 REM PLOT ABS VALUE OF DATA
58 PRINT
59 PRINT
60 FOR K=1 TO N4
61 D(K)=ABS(Y(K))
62 NEXT K
63 REM GO TO PLOTTING SUBROUTINE
64 GOSUB 472
65 REM GOTO SUPERVISOR SUBROUTINE
66 PRINT 'CALCULATING....."
67 PRINT
68 GOSUB 118
69 REM RESULTS READY FOR DISPLAY
70 PRINT
71 PRINT
72 PRINT 'THE SMOOTHED DATA IS: '
73 PRINT
74 FOR K=1 TO N4
75 PRINT K,TAB(6),Y1(K)
```

Listing 1 continued on page 266

such a regression. Thus, a more reasonable method might be to simply "eyeball" a curve through the data (as done by the dashed lines in figure 1). Using the dashed curve, the businessman would plan on having about 4800 units ready in July, instead of 6181.

The eyeballing method shown above has two clear deficiencies. The first obvious shortcoming is the assumption that the data of the next year, 1979, is a continuation of the data of the present year, 1978. This assumption is violated because the slopes of the curve at the January and December end points are not the same. However, this could be corrected graphically by a second freehand curve that would make sure that the tangent lines at January and December are parallel.

The second and more important deficiency is that there is uncertainty whether the smoothed value obtained for July 1979 is statistically correct, coupled with a lack of knowledge as to what the *expected* error might be. For example, a "better" analysis might show that the estimate is 4900 units with a standard deviation of 700 units. Thus, if 4900 units were on hand, there would be a 50% chance that all the orders could be filled. If 5600 (4900 plus one standard deviation) were available, the probability would become roughly 83%. With this type of information (that is, conclusions about data), the businessman can better plan his inventory.

In the following sections, a very simple technique is presented for data smoothing. This technique is based on the use of tables that are applied to adjust the value of a given data point according to the *weighted sum* of the values of surrounding data points. The smoothing criterion used is that of *least squares*, although it is applied in a manner not commonly taught in numerical analysis courses. As we will see, the method is amenable to pencil and paper calculations, but it is much more readily accomplished with a computer. A program to accomplish this, given in listing 1, is written in a nearly universal dialect of BASIC.

An important point is that the utility of the procedure is based on the assumption that the "noise" apparent in figure 1 is truly a random fluctuation *independent* of the signal (or month). In principle, it is possible for the month-to-month sales volume to be totally deterministic

Text continued on page 276

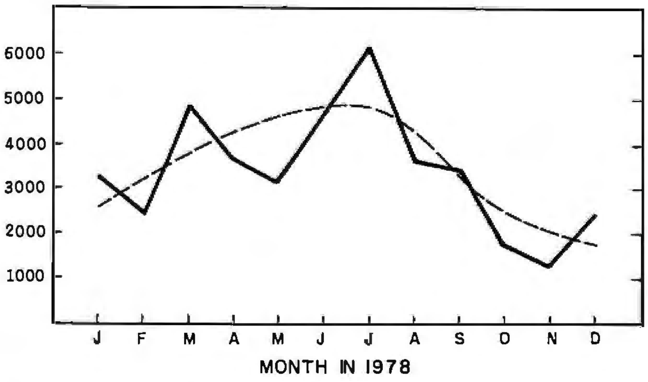

Figure 1: *Chart of sample data used in this article. The data plotted in this chart, drawn in a solid line, represents the sales of a hypothetical company for the months January through December 1978. The broken line is a human-drawn estimate of the ideal numbers that the given data roughly represents.*

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*Time estimates based on 4Mhz 8085 with 48K memory, CP/M 2.1 double density 8" floppy drive, 10,000-word text file.

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Listing 1 continued:

```
76 NEXT K
77 PRINT
78 GOSUB 535
79 PRINT 'THE STANDARD DEVIATION'
80 PRINT 'BETWEEN THE SMOOTHED AND'
81 PRINT 'UNSMOOTHED DATA SETS IS',
82 PRINT D
83 PRINT
84 GOSUB 535
85 REM PLOT ABSOLUTE VALUE OF RESULTS
86 FOR K=1 TO N4
87 D(K)=ABS(Y1(K))
88 NEXT K
89 REM GO TO PLOTTING SUBROUTINE
90 PRINT
91 PRINT
92 GOSUB 472
93 PRINT
94 PRINT
95 PRINT
96 END
97 REM ********************
98 REM DATA SMOOTHER SUPER-
99 REM VISOR SUBROUTINE
100 REM IT IS ASSUMED THAT
101 REM B,C,D,U,V,W,Y AND Y1
102 REM HAVE ALREADY BEEN
103 REM DIMENSIONED.
104 REM   B(5,3)
105 REM   C(8,91)
106 REM   D(N4+2*N3+2)
107 REM   U(8)
108 REM   V(8,12)
109 REM   W(12)
110 REM   Y(N4)
111 REM   Y1(N4)
112 REM IT IS ALSO ASSUMED THAT
113 REM THE INPUT DATA IS
114 REM AVAILABLE-
115 REM    N1,N2,N3,N4
116 REM    Y(K)
117 REM THE PROGRAM USES I AND J
118 I=N1
119 J=N2
120 REM THE OUTPUT IS Y1(K)
121 REM FIRST INITIALIZE Y1(K)
122 FOR K=1 TO N4
123 Y1(K)=0
124 NEXT K
125 REM DETERMINE THE TABLE
126 GOSUB 169
127 REM DETERMINE IF ERROR
128 GOSUB 197
129 REM ERROR ON E>0
130 IF E>0 THEN RETURN
131 REM OBTAIN COEFFICIENTS
132 REM      U(I),V(I,J)
133 REM      C(I,K)
134 GOSUB 225
135 REM SAVE THE SYMMETRY AND
136 REM NORMALIZING FACTORS
137 U=U(B(I,J))
138 A=(N3-1)/2
139 V=V(B(I,J),13-A)
140 REM GET WEIGHTS, W(K)
141 GOSUB 375
142 REM CREATE AUGMENTED
143 REM DATA VECTOR, D(K)
144 GOSUB 419
145 REM SMOOTH THE DATA VECTOR D(K)
146 REM THE DATA POSITION POINTER
147 REM IS M
148 FOR M=A+1 TO N4+A+1
149 GOSUB 439
150 Y1(M)=D
151 NEXT M
152 REM SHIFT Y1(M) DOWN
153 GOSUB 452
154 REM RESULT IS Y1(M)
155 REM GET STANDARD DEVIATION
156 GOSUB 459
157 REM RESULT IS D
158 PRINT
```

Listing 1 continued on page 268

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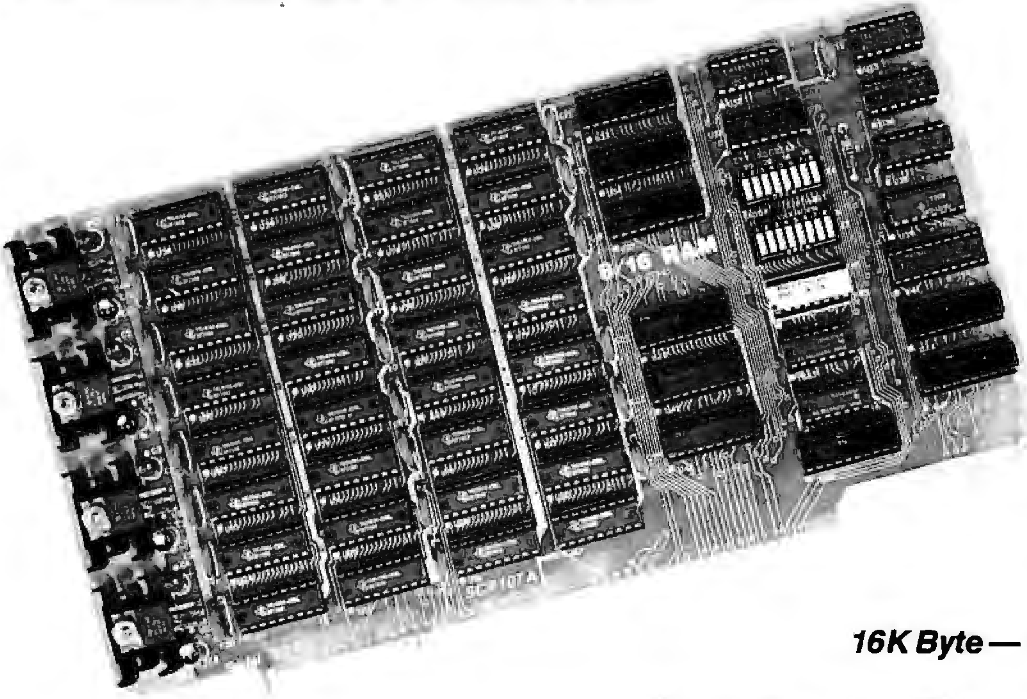
MEMORY PRODUCTS FOR THE 80'S



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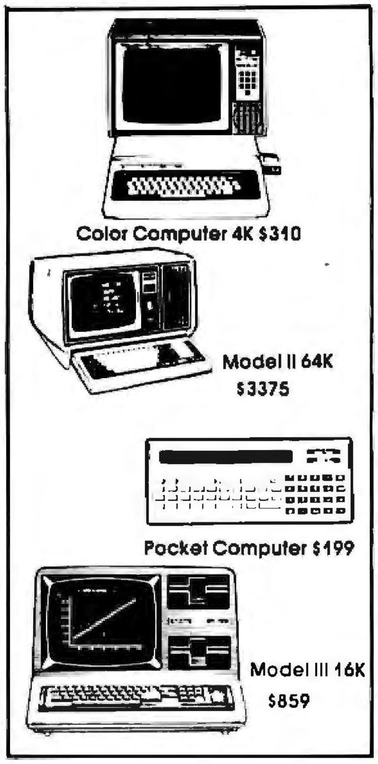
1114 Industry Drive, Seattle, WA. 98188
(206) 575-1830

Circle 180 on inquiry card.

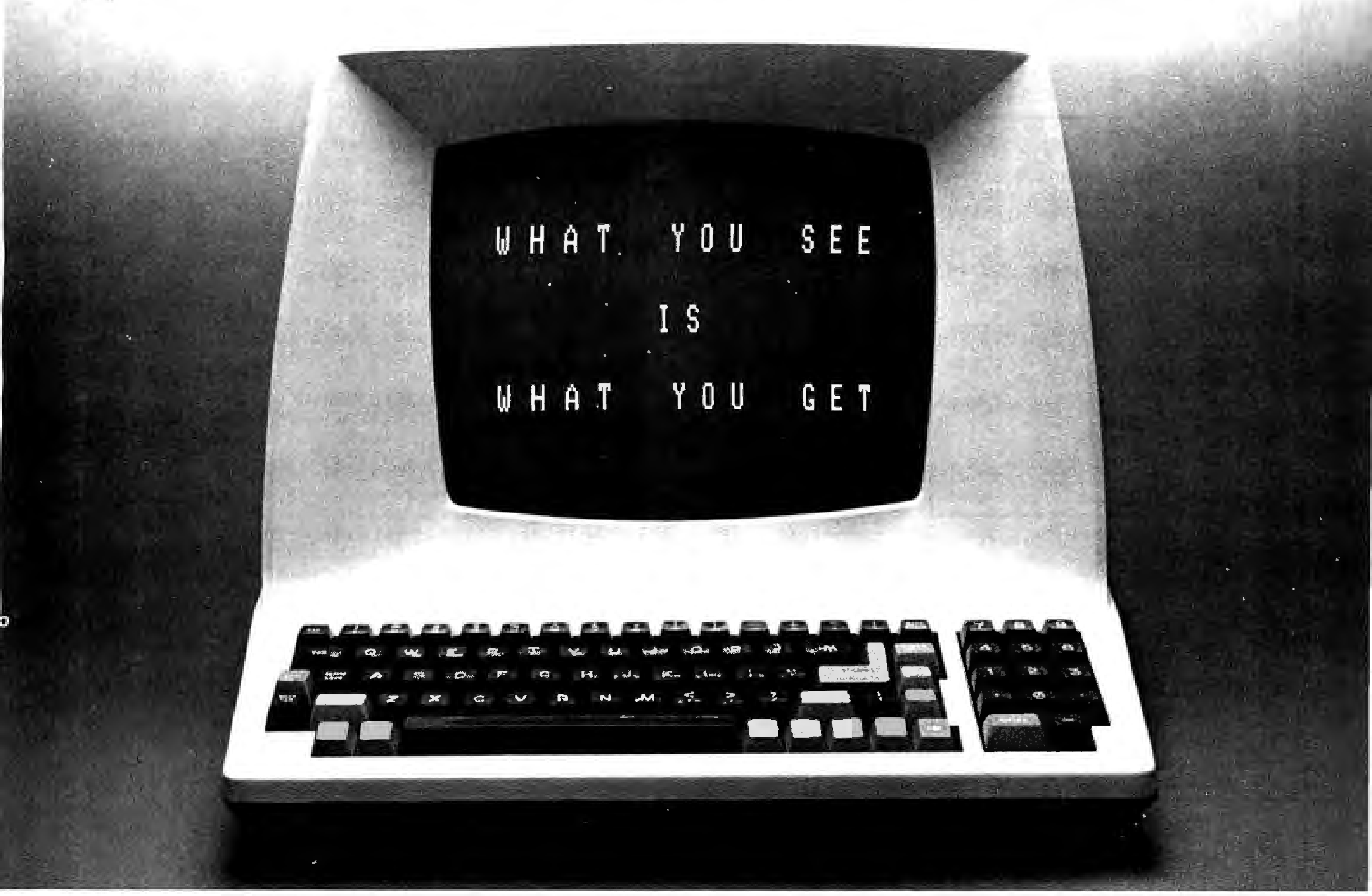


Listing 1 continued:

```
159 REM ********************
160 REM TABLE DECODE SUBROUTINE
161 REM THERE ARE 8 TABLES OF
162 REM COEFFICIENTS TO BE CHOSEN
163 REM ACCORDING TO THE DEGREE OF
164 REM FIT, I, AND THE DERIVATIVE
165 REM LEVEL, J. THE DECODING
166 REM ARRAY IS B(I,J).
167 REM NEW TABLES 12 AND 13
168 REM ARE MOVED TO 5 AND 3
169B(1,0)=5\B(1,1)=3\B(1,2)=0\B(1,3)=0\B(2,0)=1\B(2,1)=3
170B(2,2)=6\B(2,3)=0\B(3,0)=1\B(3,1)=4\B(3,2)=6\B(3,3)=8
171B(4,0)=2\B(4,1)=4\B(4,2)=7\B(4,3)=8\B(5,0)=2\B(5,1)=0
172B(5,2)=7\B(5,3)=0
173E(1)=5\E(2)=7\E(3)=3\E(4)=5\E(5)=3\E(6)=5\E(7)=5\E(8)=5
174 RETURN
175 REM *********************
176 REM ERROR CODING SUB.
177 REM E=0 - NO ERROR
178 REM E=1 - TOO FEW POINTS
179 REM E=2 - TOO MANY POINTS
180 REM E=3 - DERIVATIVE > FIT
181 REM       LEVEL
182 REM E=4 - FIT TOO HIGH
183 REM E=5 - DERIVATIVE TOO
184 REM       HIGH
185 REM E=6 - TABLE NOT AVAIL.
186 REM E=7 - NOT ENOUGH DATA
187 REM E=8 - ILLEGAL VALUE
188 REM N1=LEVEL OF FIT
189 REM N2=ORDER OF DERIVATIVE
190 REM N3=NO. OF DATA POINTS
191 REM    TO BE AVERAGED
192 REM N4=TOTAL DATA SET SIZE
193 E=0
194 IF B(N1,N2)=0 THEN E=6
195 IF N1<0 THEN E=8
196 IF N2>3 THEN E=5
197 IF N3<3 THEN E=1
198 IF N3>25 THEN E=2
199 IF N3<E(B(N1,N2)) THEN E=1
200 IF N2>N1 THEN E=3
201 IF N2<0 THEN E=8
202 IF INT (N3/2)=N3/2 THEN E=8
203 IF N3>N4 THEN E=7
204 IF N1>5 THEN E=4
205 RETURN
206 REM ********************
207 REM COEFFICIENT STORAGE SUB.
208 REM THE WEIGHTS ARE STORED IN
209 REM THE ARRAY C(I,K). THE IN-
210 REM DEX, I, REPRESENTS THE
211 REM TABLE NUMBER (1 TO 8).
212 REM THE INDEX, K, REPRESENTS
213 REM THE ELEMENT IN TABLE I.
214 REM THERE ARE UP TO 91 SUCH
215 REM ELEMENTS.
216 REM ALSO STORED ARE THE NORM-
217 REM ALIZING FACTORS, V(I,K),
218 REM WHERE K RANGES FROM 1 TO
219 REM 13. IN ADDITION, THE 8
220 REM SYMMETRY VALUES, U(I),
221 REM ARE ALSO INCLUDED.
222 REM NOTE THAT TABLES 12 (NOW 5)
223 REM AND 13 (NOW 3) ARE CALCULATED
224 REM ELSEWHERE.
225U(1)=1\U(2)=1\U(3)=-1\U(4)=-1\U(5)=1\U(6)=1\U(7)=1\U(8)=-1
226V(1,1)=5175\V(1,2)=805\V(1,3)=3059\V(1,4)=2261
227V(1,5)=323\V(1,6)=1105\V(1,7)=143\V(1,8)=429\V(1,9)=231
228V(1,10)=21\V(1,11)=35\V(2,1)=30015\V(2,2)=6555
229V(2,3)=260015\V(2,4)=7429\V(2,5)=4199\V(2,6)=46189
230V(2,7)=2431\V(2,8)=429\V(2,9)=429\V(2,10)=231
231V(4,1)=1776060\V(4,2)=197340\V(4,3)=3634092\V(4,4)=255816
232V(4,5)=23256\V(4,6)=334152\V(4,7)=24024\V(4,8)=5148
233V(4,9)=1188\V(4,10)=252\V(4,11)=12
234V(6,1)=26910\V(6,2)=17710\V(6,3)=33649\V(6,4)=6783
235V(6,5)=3876\V(6,6)=6188\V(6,7)=1001\V(6,8)=429\V(6,9)=462
236V(6,10)=42\V(6,11)=7\V(7,1)=4292145\V(7,2)=2812095
237V(7,3)=245157\V(7,4)=490314\V(7,5)=478686\V(7,6)=277134
238V(7,7)=160446\V(7,8)=16731\V(7,9)=4719\V(7,10)=99\V(7,11)=3
239V(8,1)=296010\V(8,2)=32890\V(8,3)=86526\V(8,4)=42636
240V(8,5)=3876\V(8,6)=7956\V(8,7)=572\V(8,8)=858\V(8,9)=198
241V(8,10)=6\V(8,11)=2
242FORK=1TO12\V(5,K)=27-2*K\V(3,13-K)=K*(K+1)*(2*K+1)/3\NEXTK
```

Listing 1 continued on page 270

Can your word processor pass this screen test?



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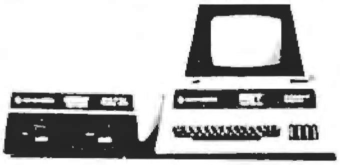

Listing 1 continued:

```
243FORK=1TO12\V(7,K)=12*V(7,K)\NEXTK
244C(1,1)=467\C(1,2)=462\C(1,3)=447\C(1,4)=422\C(1,5)=387
245C(1,6)=342\C(1,7)=287\C(1,8)=222\C(1,9)=147\C(1,10)=62
246C(1,11)=-33\C(1,12)=-138\C(1,13)=-253\C(1,14)=79\C(1,15)=78
247C(1,16)=75\C(1,17)=70\C(1,18)=63\C(1,19)=54\C(1,20)=43
248C(1,21)=30\C(1,22)=15\C(1,23)=-2\C(1,24)=-21\C(1,25)=-42
249C(1,26)=329\C(1,27)=324\C(1,28)=309\C(1,29)=284\C(1,30)=249
250C(1,31)=204\C(1,32)=149\C(1,33)=84\C(1,34)=9\C(1,35)=-76
251C(1,36)=-171\C(1,37)=269\C(1,38)=264\C(1,39)=249
252C(1,40)=224\C(1,41)=189\C(1,42)=144\C(1,43)=89\C(1,44)=24
253C(1,45)=-51\C(1,46)=-136\C(1,47)=43\C(1,48)=42\C(1,49)=39
254C(1,50)=34\C(1,51)=27\C(1,52)=18\C(1,53)=7\C(1,54)=-6
255C(1,55)=-21\C(1,56)=167\C(1,57)=162\C(1,58)=147\C(1,59)=122
256C(1,60)=87\C(1,61)=42\C(1,62)=-13\C(1,63)=-78\C(1,64)=25
257C(1,65)=24\C(1,66)=21\C(1,67)=16\C(1,68)=9\C(1,69)=0
258C(1,70)=-11\C(1,71)=89\C(1,72)=84\C(1,73)=69\C(1,74)=44
259C(1,75)=9\C(1,76)=-36\C(1,77)=59\C(1,78)=54\C(1,79)=39
260C(1,80)=14\C(1,81)=-21\C(1,82)=7\C(1,83)=6\C(1,84)=3
261C(1,85)=-2\C(1,86)=17\C(1,87)=12\C(1,88)=-3\C(2,1)=4253
262C(2,2)=4125\C(2,3)=3750\C(2,4)=3155\C(2,5)=2385\C(2,6)=1503
263C(2,7)=590\C(2,8)=-255\C(2,9)=-915\C(2,10)=-1255
264C(2,11)=-1122\C(2,12)=-345\C(2,13)=1265\C(2,14)=1011
265C(2,15)=975\C(2,16)=870\C(2,17)=705\C(2,18)=495\C(2,19)=261
266C(2,20)=30\C(2,21)=-165\C(2,22)=-285\C(2,23)=-285
267C(2,24)=-114\C(2,25)=285\C(2,26)=44003\C(2,27)=42120
268C(2,28)=36660\C(2,29)=28190\C(2,30)=17655\C(2,31)=6378
269C(2,32)=-3940\C(2,33)=-11220\C(2,34)=-13005\C(2,35)=-6460
270C(2,36)=11628\C(2,37)=1393\C(2,38)=1320\C(2,39)=1110
271C(2,40)=790\C(2,41)=405\C(2,42)=18\C(2,43)=-290
272C(2,44)=-420\C(2,45)=-255\C(2,46)=340\C(2,47)=883
273C(2,48)=825\C(2,49)=660\C(2,50)=415\C(2,51)=135
274C(2,52)=-117\C(2,53)=-260\C(2,54)=-195\C(2,55)=195
275C(2,56)=11063\C(2,57)=10125\C(2,58)=7500\C(2,59)=3755
276C(2,60)=-165\C(2,61)=-2937\C(2,62)=-2860\C(2,63)=2145
277C(2,64)=677\C(2,65)=600\C(2,66)=390\C(2,67)=110
278C(2,68)=-135\C(2,69)=-198\C(2,70)=110\C(2,71)=143
279C(2,72)=120\C(2,73)=60\C(2,74)=-10\C(2,75)=-45\C(2,76)=18
280C(2,77)=179\C(2,78)=135\C(2,79)=30\C(2,80)=-55\C(2,81)=15
281C(2,82)=131\C(2,83)=75\C(2,84)=-30\C(2,85)=5
282C(4,1)=0\C(4,2)=-8558\C(4,3)=-16649\C(4,4)=-23806
283C(4,5)=-29562\C(4,6)=-33450\C(4,7)=-35003\C(4,8)=-33754
284C(4,9)=-29236\C(4,10)=-20982\C(4,11)=-8525\C(4,12)=8602
285C(4,13)=30866\C(4,14)=0\C(4,15)=-1222\C(4,16)=-2365
286C(4,17)=-3350\C(4,18)=-4098\C(4,19)=-4530\C(4,20)=-4567
287C(4,21)=-4130\C(4,22)=-3140\C(4,23)=-1518\C(4,24)=815
288C(4,25)=3938\C(4,26)=0\C(4,27)=-29592\C(4,28)=-56881
289C(4,29)=-79564\C(4,30)=-95338\C(4,31)=-101900
290C(4,32)=-96947\C(4,33)=-78176\C(4,34)=-43284\C(4,35)=10032
291C(4,36)=84075\C(4,37)=0\C(4,38)=-2816\C(4,39)=-5363
292C(4,40)=-7372\C(4,41)=-8574\C(4,42)=-8700\C(4,43)=-7481
293C(4,44)=-4648\C(4,45)=68\C(4,46)=6936\C(4,47)=0
294C(4,48)=-358\C(4,49)=-673\C(4,50)=-902\C(4,51)=-1002
295C(4,52)=-930\C(4,53)=-643\C(4,54)=-98\C(4,55)=748\C(4,56)=0
296C(4,57)=-7506\C(4,58)=-13843\C(4,59)=-17842\C(4,60)=-18334
297C(4,61)=-14150\C(4,62)=-4121\C(4,63)=12922\C(4,64)=0
298C(4,65)=-832\C(4,66)=-1489\C(4,67)=-1796\C(4,68)=-1578
299C(4,69)=-660\C(4,70)=1133\C(4,71)=0\C(4,72)=-296
300C(4,73)=-503\C(4,74)=-532\C(4,75)=-294\C(4,76)=300
301C(4,77)=0\C(4,78)=-126\C(4,79)=-193\C(4,80)=-142\C(4,81)=86
302C(4,82)=0\C(4,83)=-58\C(4,84)=-67\C(4,85)=22\C(4,86)=0
303C(4,87)=-8\C(4,88)=1\C(6,1)=-52\C(6,2)=-51\C(6,3)=-48
304C(6,4)=-43\C(6,5)=-36\C(6,6)=-27\C(6,7)=-16\C(6,8)=-3
305C(6,9)=12\C(6,10)=29\C(6,11)=48\C(6,12)=69\C(6,13)=92
306C(6,14)=-44\C(6,15)=-43\C(6,16)=-40\C(6,17)=-35\C(6,18)=-28
307C(6,19)=-19\C(6,20)=-8\C(6,21)=5\C(6,22)=20\C(6,23)=37
308C(6,24)=56\C(6,25)=77\C(6,26)=-110\C(6,27)=-107\C(6,28)=-98
309C(6,29)=-83\C(6,30)=-62\C(6,31)=-35\C(6,32)=-2\C(6,33)=37
310C(6,34)=82\C(6,35)=133\C(6,36)=190\C(6,37)=-30\C(6,38)=-29
311C(6,39)=-26\C(6,40)=-21\C(6,41)=-14\C(6,42)=-5\C(6,43)=6
312C(6,44)=19\C(6,45)=34\C(6,46)=51\C(6,47)=-24\C(6,48)=-23
313C(6,49)=-20\C(6,50)=-15\C(6,51)=-8\C(6,52)=1\C(6,53)=12
314C(6,54)=25\C(6,55)=40\C(6,56)=-56\C(6,57)=-53\C(6,58)=-44
315C(6,59)=-29\C(6,60)=-8\C(6,61)=19\C(6,62)=52\C(6,63)=91
316C(6,64)=-14\C(6,65)=-13\C(6,66)=-10\C(6,67)=-5\C(6,68)=2
317C(6,69)=11\C(6,70)=22\C(6,71)=-10\C(6,72)=-9\C(6,73)=-6
318C(6,74)=-1\C(6,75)=6\C(6,76)=15\C(6,77)=-20\C(6,78)=-17
319C(6,79)=-8\C(6,80)=7\C(6,81)=28\C(6,82)=-4\C(6,83)=-3
320C(6,84)=0\C(6,85)=5\C(6,86)=-2\C(6,87)=-1\C(6,88)=2
321C(7,1)=-441870\C(7,2)=-418011\C(7,3)=-348429\C(7,4)=-239109
322C(7,5)=-100026\C(7,6)=54855\C(7,7)=207579\C(7,8)=336201
323C(7,9)=414786\C(7,10)=413409\C(7,11)=298155\C(7,12)=31119
324C(7,13)=-429594\C(7,14)=-373230\C(7,15)=-349401
325C(7,16)=-280275\C(7,17)=-172935\C(7,18)=-39186
326C(7,19)=104445\C(7,20)=236709\C(7,21)=331635\C(7,22)=358530
```

Listing 1 continued on page 272

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Winner of the software division of the *First International Man-Machine OTHELLO™ Tournament*, this version of the 200-year old game Reversi, features 27 levels of play and high-resolution color graphics. *07004, APPLE II tape, $29.95; 07009, APPLE II Disk, $34.95*

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Increase your BASIC programming speed and flexibility. Contains 9 useful subroutines: 1. REM Writer 2. PRINT Writer 3. POKE Writer 4. Hexadecimal Decimal Converter 5. Line Counter 6. Renumber 7. Append 8. Byte Counter 9. Slow List Stop List *03504, Apple II tape, $29.95*

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Automatically maintains a cross-reference listing of all your programs, their location by disk number, their function and use. Catalogs, lists and sorts programs *05203, TRS-80 Level II tape, $16.95; 05208, TRS-80 Level II Disk, $21.95*

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MAILING LIST (Tru-Data Software) Lists addresses, prints labels, allows for alterations and deletions, and has the capacity to make duplicate data file disks. Can only be used with version 1.5. *05713, Heath Disk, $49.95*

FINPLAN: A Financial Planning Program for Small Business (Montgomery) Allows you to enter data from a balance sheet into the program, to make assumptions about future growth of business, and to have the computer project results for up to a five-year period based on those assumptions. And if you change any data, the program revises all resulting data automatically. The disk version can only be used with TRSDOS Version 2.3. *05103, TRS-80 Level II tape, $69.95; 05108, TRS-80 Level II Disk Version, $74.95*

DATA MANAGER: A Data Base Management System and Mailing List (Lutus) Store information on a floppy disk, and retrieve it quickly and easily by specific names, or by category. *04909, Apple II Disk Version, $49.95*

MCAP: A Microcomputer Circuit Analysis Program (Savon) Performs a linear voltage, impedance, or transfer impedance analysis of an electronic circuit. *04501, PET; 04503, TRS-80 Level II; 04504, Apple II; each tape $24.95; 04513, Heathkit Zenith Disk, $29.95*

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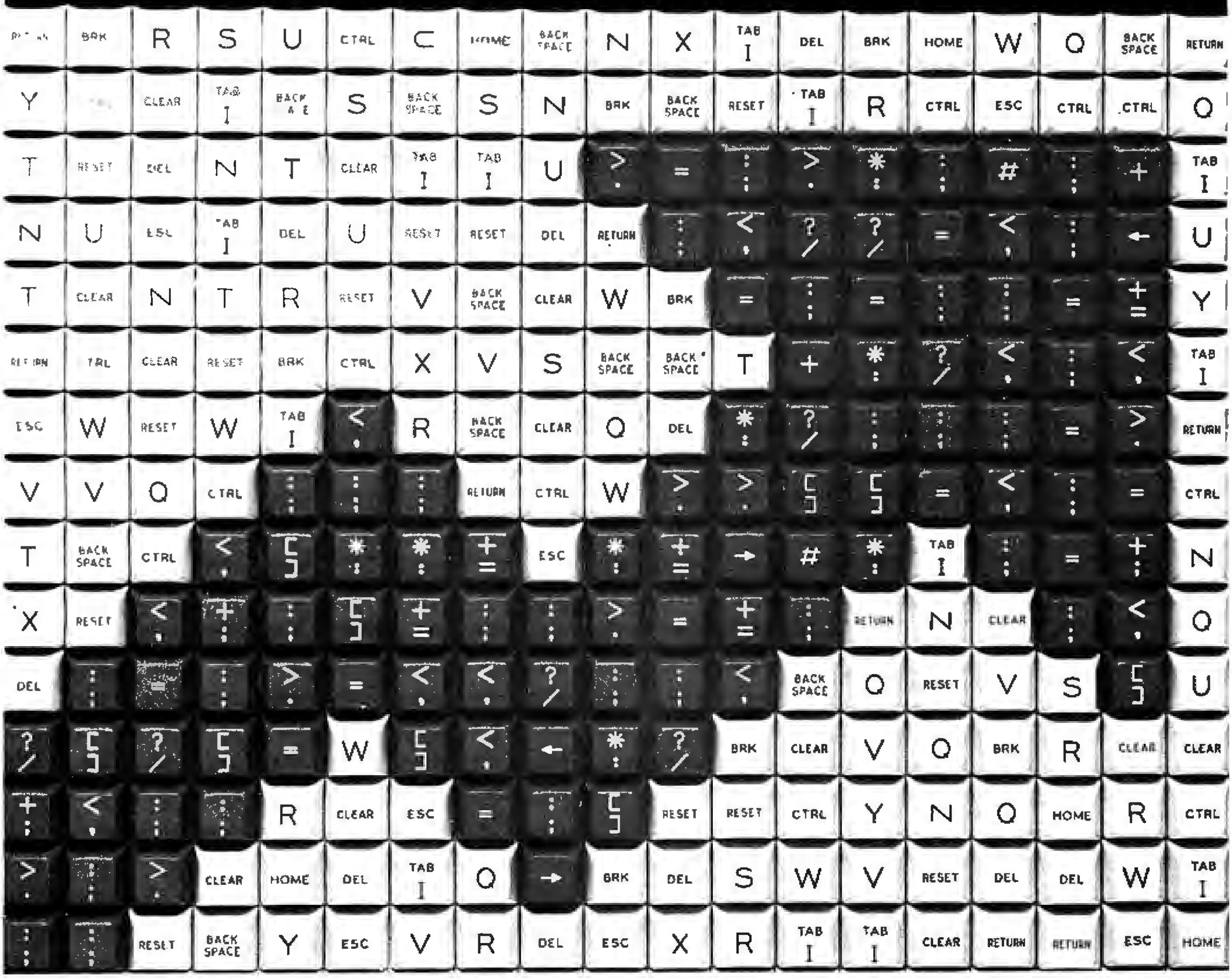
Listing 1 continued:

```
327C(7,23)=281979\C(7,24)=61845\C(7,25)=-346731\C(7,26)=-42966
328C(7,27)=-39672\C(7,28)=-30183\C(7,29)=-15678\C(7,30)=1878
329C(7,31)=19734\C(7,32)=34353\C(7,33)=41412\C(7,34)=35802
330C(7,35)=11628\C(7,36)=-37791\C(7,37)=-116820
331C(7,38)=-105864\C(7,39)=-74601\C(7,40)=-27846\C(7,41)=26376
332C(7,42)=76830\C(7,43)=109071\C(7,44)=105444\C(7,45)=45084
333C(7,46)=-96084\C(7,47)=-160740\C(7,48)=-141873
334C(7,49)=-88749\C(7,50)=-11799\C(7,51)=71592\C(7,52)=137085
335C(7,53)=153387\C(7,54)=82251\C(7,55)=-121524
336C(7,56)=-137340\C(7,57)=-116577\C(7,58)=-59253
337C(7,59)=19737\C(7,60)=95568\C(7,61)=133485\C(7,62)=88803
338C(7,63)=-93093\C(7,64)=-124740\C(7,65)=-99528
339C(7,66)=-32043\C(7,67)=53262\C(7,68)=115632\C(7,69)=98010
340C(7,70)=-72963\C(7,71)=-22230\C(7,72)=-15912\C(7,73)=117
341C(7,74)=17082\C(7,75)=20358\C(7,76)=-10530\C(7,77)=-12210
342C(7,78)=-6963\C(7,79)=4983\C(7,80)=12243\C(7,81)=-4158
343C(7,82)=-630\C(7,83)=-171\C(7,84)=603\C(7,85)=-117
344C(7,86)=-90\C(7,87)=48\C(7,88)=-3\C(8,1)=0\C(8,2)=77
345C(8,3)=149\C(8,4)=211\C(8,5)=258\C(8,6)=285\C(8,7)=287
346C(8,8)=259\C(8,9)=196\C(8,10)=93\C(8,11)=-55\C(8,12)=-253
347C(8,13)=-506\C(8,14)=0\C(8,15)=13\C(8,16)=25\C(8,17)=35
348C(8,18)=42\C(8,19)=45\C(8,20)=43\C(8,21)=35\C(8,22)=20
349C(8,23)=-3\C(8,24)=-35\C(8,25)=-77\C(8,26)=0\C(8,27)=54
350C(8,28)=103\C(8,29)=142\C(8,30)=166\C(8,31)=170\C(8,32)=149
351C(8,33)=98\C(8,34)=12\C(8,35)=-114\C(8,36)=-285\C(8,37)=0
352C(8,38)=44\C(8,39)=83\C(8,40)=112\C(8,41)=126\C(8,42)=120
353C(8,43)=89\C(8,44)=28\C(8,45)=-68\C(8,46)=-204\C(8,47)=0
354C(8,48)=7\C(8,49)=13\C(8,50)=17\C(8,51)=18\C(8,52)=15
355C(8,53)=7\C(8,54)=-7\C(8,55)=-28\C(8,56)=0\C(8,57)=27
356C(8,58)=49\C(8,59)=61\C(8,60)=58\C(8,61)=35\C(8,62)=-13
357C(8,63)=-91\C(8,64)=0\C(8,65)=4\C(8,66)=7\C(8,67)=8
358C(8,68)=6\C(8,69)=0\C(8,70)=-11\C(8,71)=0\C(8,72)=14
359C(8,73)=23\C(8,74)=22\C(8,75)=6\C(8,76)=-30\C(8,77)=0
360C(8,78)=9\C(8,79)=13\C(8,80)=7\C(8,81)=-14\C(8,82)=0
361C(8,83)=1\C(8,84)=1\C(8,85)=-1\C(8,86)=0\C(8,87)=2
362C(8,88)=-1
363 RETURN
364 REM ********************
365 REM WEIGHTS SUBROUTINE
366 REM N3=NO. OF DATA POINTS
367 REM     TO BE AVERAGED OVER
368 REM B(I,J)=THE TABLE NUMBER
369 REM THE TABLE IS STRUNG
370 REM OUT STARTING WITH THE
371 REM 25 POINT SET WHICH, AS
372 REM IT IS IS SYMMETRICAL,
373 REM IS REDUCED TO 13 ELE-
374 REM MENTS.
375 IF B(I,J)=5 THEN GOSUB 397
376 IF B(I,J)=3 THEN GOSUB 407
377 IF B(I,J)=5 THEN RETURN
378 IF B(I,J)=3 THEN RETURN
379 L=12
380 K=1
381 FOR K1=0 TO L
382 W(K1)=C(B(I,J),K)
383 K=K+1
384 NEXT K1
385 REM TABLE IS READ IN
386 REM SEQUENCE UNTIL THE
387 REM RIGHT SET IS FOUND.
388 IF A=L THEN RETURN
389 L=L-1
390 GOTO 381
391 REM ********************
392 REM TABLE 12 (5) SUBROUTINE
393 REM THIS TABLE IS FOR THE
394 REM LINEAR LEAST SQUARES
395 REM SMOOTHING AND IS
396 REM ONLY A MOVING AVERAGE.
397 FOR K=0 TO 12
398 W(K)=1
399 NEXT K
400 RETURN
401 REM ********************
402 REM TABLE 13 (3) SUBROUTINE
403 REM THIS TABLE IS FOR
404 REM LINEAR LEAST SQUARES
405 REM FIRST DERIVATIVE
406 REM SMOOTHING.
407 FOR K=0 TO 12
408 W(K)=-K
409 NEXT K
410 RETURN
411 REM ********************
412 REM DATA VECTOR SUB.
```

Listing 1 continued on page 274

KEYS TO PRODUCTIVITY



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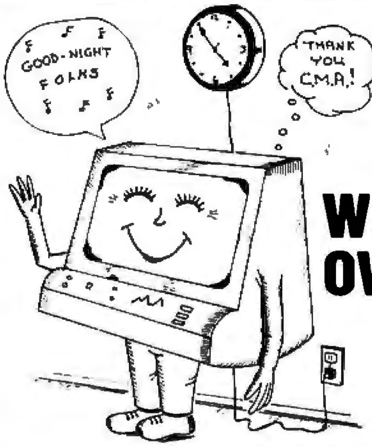

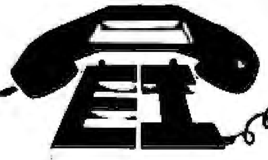

Listing 1 continued:

```
413 REM THE INPUT DATA, Y(K),
414 REM ARE CONVERTED TO A
415 REM DATA VECTOR WHICH IS
416 REM AUGMENTED BY ZEROES ON
417 REM BOTH THE LEFT AND
418 REM RIGHT.
419 FOR K=0 TO A
420 D(K)=0
421 D(K+N4+A+1)=0
422 NEXT K
423 FOR K=1 TO N4
424 D(K+A)=Y(K)
425 NEXT K
426 RETURN
427 REM ********************
428 REM CONVOLUTION SUBROUTINE
429 REM THIS ROUTINE SMOOTHS THE
430 REM DATA POINT M USING THE
431 REM SURROUNDING N3 DATA POINTS.
432 REM THE WEIGHTING FUNCTION IS
433 REM W(I), AND THE DATA D(K).
434 REM THE SYMMETRY IN WEIGHTING
435 REM IS GIVEN IN U.
436 REM THE RESULT IS D.
437 REM THE RESULT IS NORMALIZED
438 REM USING V.
439 D=0
440 D=D+W(0)*D(M)
441 FOR K=1 TO A
442 D=D+W(K)*(U*D(M+K)+D(M-K))
443 NEXT K
444 D=D/V
445 RETURN
446 REM ********************
447 REM DATA SHIFT SUB.
448 REM THE SHIFTED AND
449 REM SMOOTHED DATA SET
450 REM IS D(K). THE DESIRED
451 REM SMOOTHED SET IS Y1(K).
452 FOR K=1 TO N4
453 Y1(K)=Y1(K+A)
454 NEXT K
455 RETURN
456 REM ********************
457 REM STANDARD DEVIATION
458 REM SUBROUTINE
459 D=0
460 FOR K=1 TO N4
461 D=D+(Y(K)-Y1(K))*(Y(K)-Y1(K))
462 NEXT K
463 D=SQRT(D/(N4-I-.999999))
464 REM IF Y1(K) IS A DERIVATIVE
465 REM THEN CALCULATION IS NOT
466 REM APPLICABLE.
467 IF N2>0 THEN D=0
468 RETURN
469 REM ********************
470 REM PLOTTING SUBROUTINE
471 REM SHIFT DATA TO NON-NEGATIVE
472 PRINT
473 PRINT 'INPUT DESIRED PLOT WIDTH: ',
474 INPUT L
475 REM FIND MAX. DATA VALUE
476 C=0
477 FOR K=1 TO N4
478 IF C<D(K) THEN C=D(K)
479 NEXT K
480 REM DETERMINE PRINTING SCALE VALUE
481 A=L/C
482 PRINT
483 PRINT
484 PRINT'***** DATA PLOT (SCALED) *****'
485 PRINT
486 PRINT
487 PRINT 'MAXIMUM VALUE= ',C
488 PRINT
489 PRINT
490 REM GO TO AXIS PRINT SUBROUTINE
491 GOSUB 519
492 FOR K=1 TO N4
493 REM INSERT LINE FEED FOR AUTO SPACING
494 FOR P=1 TO (INT(0.6*L/N4))
495 PRINT':',TAB(L),':'
496 NEXT P
497 REM LOCATE DATUM POSITION
498 E2=A*D(K)
```

Listing 1 continued on page 276

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1.000-A
1 8432-A
1 8437-B
2 000 A
2 0971-A
2 4576-A
2.500-A
2.6657-B
2.9950-B
3 000-A
3 067-B
3.200-B
3 2768-A
3 500-B
3 579-B
4.000-B
4 1943-B
4 3426 B
4 4803 B
4.6103-B
4.6503 B
4 8303-B
4 9152-B
5 000-B
5 0688-B
5 1203-B
5.1850-B
5 1856-B

5.2428-B
5.610-B
5 7143-B
5.855-B
5.982-B
6.000-B
6 144-B
6.15030-B
6.29780-B
6.400-B
6.5536-B
6.72530-B
6.75840-B
6.9003-B
7.0063-B
7.0336-B
7.0916-B
7.1836-B
7.2588-B
8 000 B
8.0556-B
8.1416-B
8.1818-B
8.3303-B
8.4998 B
8 5766 B
8 6056-B
8.9608-B
8.9906-B
9.47208-B

9.9336-B
9.98408-B
9.98960-B
10.000-B
10.2458-B
10 4960 B
10.7755-B
10.8255-B
10 8386 B
11.1360-B
11.155-B
11.2186-B
11.2890 B
11.4776-B
11.6566-B
11.6816-B
12.440-B
14.3182 B
14.4308 B
15 000-B
15.4408-B
15 5066-B
16.000-B
16.3848-B
17 2248 B
17.2422-B
18.000 B
18.4320-B
19 4690-B
19.7508-B

20.000-B
20 4988-B
22 1184-B
22.6258-B
26 3556 B
26 5006 B
26 6706 B
27.000 B
27.0006 B
27 6506 B
28.4006-B
28 6276-B
28.7538-B
29 8758 B
29.9378-B
30.0648 B
30 3606-B
30 6258-B
30.8768-B
31.4378 B
31.7538-B
31 9008-B
32 000-B
33.2006-B
33.6258 B
34 5558 B
34.7538-B
34 9776-B
35 9256 B
36 006 B

36.2886-B
36.3536-B
37 9628-B
38.3768-B
38 4448-B
38 6258-B
38.9258 B
39 3128 B
39 5038-B
39 6668-B
39.7538-B
39.8768-B
39.9628-B
40.4448-B
40.5928-B
40.8128-B
40 8336-B
40 8758-B
40.8888-B
40.9258-B
41.0008-B
41.1666-B
41 3768-B
41.9378-B
42 0008 B
42 5836-B
42 6268-B
42.7006-B
42.7538-B
42 8148-B

42.8518-B
42.8768-B
42.9258 B
42.9628-B
43.0008-B
43.0378-B
43.0748-B
43.1858-B
43.2598-B
43 3338-B
43.3708-B
43.4078-B
43.4378-B
43.4448-B
43.5558-B
43.6298-B
43 6668-B
43.7778-B
43.8128-B
43.8148-B
43.8548-B
43 8888-B
43.9258-B
44.0008-B
44 0378-B
44.3768-B
44.7778-B
45.1256-B
46 3006-B
46.7006-B

46.8128 B
47.3768-B
47.8838 B
48 000-B
48 3006 B
48.6468 B
48 7006 B
48 8768 B
49 7006-B
49 7338-B
49.8128-B
50.2505 B
51 0556-B
51.3128-B
51.7778-B
51.8506 B
52 8128-B
56.7506-B
60 6006 B
60 7508 B
66 7506 B
70 4006 B
75.0005 B
90 8338-B
99.9668 B
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Listing 1 continued:

```
499 REM FORMATTED PRINT
500 IF E2>=1 THEN GOTO 503
501 PRINT"*",
502 GOTO 506
503 PRINT":",
504 PRINT TAB(E2),"*",
505 IF INT(E2)=L THEN GOTO 507
506 PRINT TAB(L),":",
507 PRINT
508 NEXT K
509 REM GO TO AXIS PRINT SUBROUTINE
510 GOSUB 519
511 PRINT
512 GOSUB 535
513 PRINT
514 PRINT
515 REM RETURN TO DATA SOURCE PROGRAM
516 RETURN
517 REM *********
518 REM AXIS PLOT
519 FOR K=1 TO L/5
520 PRINT"I----",
521 NEXT K
522 PRINT"I",
523 E4=(K-1)*5+1
524 IF E4=L+1 THEN PRINT
525 IF E4=L+1 THEN GOTO 532
526 E4=E4+1
527 IF E4>=L+1 THEN GOTO 530
528 PRINT"-",
529 GOTO 526
530 PRINT";"
531 REM RETURN TO MAIN PLOTTING PROGRAM
532  RETURN
533 REM ********************
534 REM PAUSE
535 PRINT "CONTINUE",
536 INPUT R4$
537 PRINT
538 RETURN
READY
```

Text continued from page 264:

(eg: a government contract) so that, depending on the situation, the next year's sales might be either exactly the same or drastically different. Thus data smoothing must be performed using some common sense concerning how to evaluate the results.

The Moving Average

This section presents the basic table-oriented algorithm; the following section provides the mathematical derivation of the table values for the linear least-squares case. Although the mathematics may appear complicated, especially for the parabolic, cubic, and higher fits, you will find the actual application of the results very simple.

The algorithm is conceptually identical to that of the *moving average.* In the calculation of the three-point moving average, the data point for the month of interest (using our example from table 1) is replaced by the average value of that data point and its two surrounding neighbors:

$$S(t) = \frac{Y(t-1)+Y(t)+Y(t+1)}{3} \tag{2}$$

In this notation, $S(t)$ is the smoothed value at position t and $Y(t)$ is the actual datum for position t. If a five-point moving average were used, the corresponding equation would be:

$$S(t) = \frac{Y(t-2)+Y(t-1)+Y(t)+Y(t+1)+Y(t+2)}{5} \tag{3}$$

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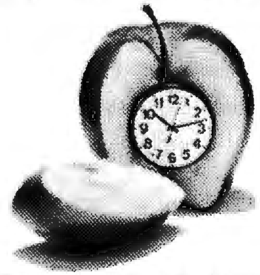

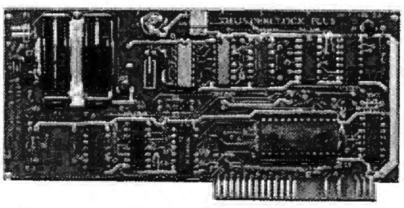

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sort	alphabetize by all or part of text line
col	arrange text in columns on page.
print	paginates text for hard copy.
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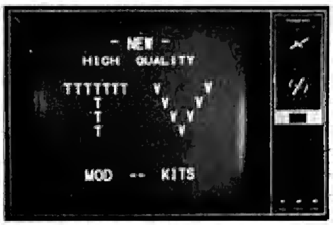

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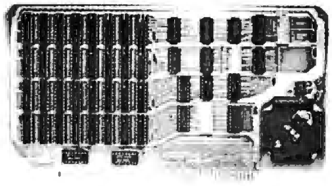

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Month	1978 Sales Volume	Three-Point Smoothing	Five-Point Smoothing
(November)	(1235)		
(December)	(2408)		
January	3279	2703	2842
February	2421	3521	3321
March	4864	3638	3475
April	3629	3891	3768
May	3180	3851	4520
June	4744	4702	4277
July	6181	4859	4235
August	3653	4417	3944
September	3418	2931	3242
October	1722	2125	2487
November	1235	1788	2412
December	2408	2307	2213
(January)	(3279)		
(February)	(2421)		
Standard Deviation:		719	994

Table 2: *1978 sales with three-point and five-point moving-average data smoothing. Note that extrapolated figures must be given for November and December 1977 and January and February 1979 in order for the smoothed versions to be calculated.*

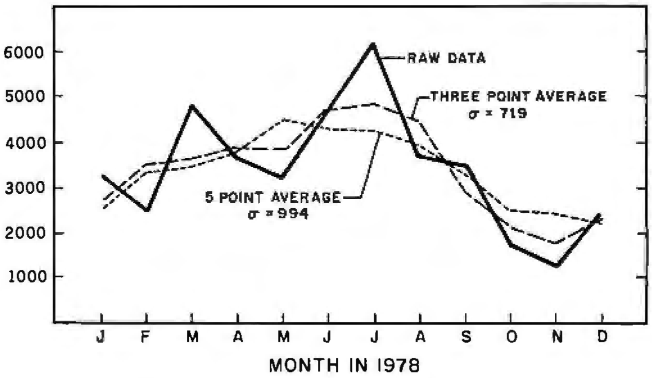

Figure 2: *Computation of a smoothed set of data using the moving-average method. The chart shows the raw data (solid line), the smoothed version using a three-point average (the dashed line) and the smoothed version using a five-point average (the dotted line). The Greek letter σ indicates the standard deviations for the respective graphs.*

Note that the number of points included in the average is odd. This is required to keep the smoothed points from being shifted in *phase*. Contrast this with the average of the two data points for June and July—the smoothed value would have to be plotted halfway between the two months.

The results of applying the three-point and five-point moving averages to the data shown in table 1 are given in table 2, and the results are plotted in figure 2. The assumption that the pattern will repeat is used to supply the extra data points required at either end of the data set.

This particular example demonstrates several general features of moving-average data smoothing. First, from figure 2, it is apparent that the moving average tends to smooth out extreme fluctuations in the data. Using a five-point average instead of a three-point one has a greater effect on limiting the range of variation. However, using a five-point average does not guarantee that a locally smoother curve will result, although the tendency will exist.

Note, for example, the region near May. The five-point average equally weights the values from the two-month periods on either side, which, in this case, contain two peaks (one in March and one in July). Thus, where there is a local *minimum* in the raw data, the five-point average gives a local *maximum*. This obvious weakness in the smoothing is due to the implied assumption that the five data points over which the averaging is performed should all be equally *weighted*; the July value is included with the May value with equal importance, even though the smoothed result is being calculated for May. As we will see later, nonuniform weighting may be used, partially avoiding this problem.

The second feature to note is that the three-point and five-point moving averages naturally give different results. For the smoothed July value, the three-point method gives an average of 4859, with a standard deviation of 719, while the five-point method gives an average of 4235, with a standard deviation of 994.

Which result is correct? The answer is probably neither. However, one result is likely to be more representative of the truth than the other. If reason exists for believing that correlation between monthly results extends only as far as one month on either side of a given month, then the three-month average is likely to be better. (That is, if the sales for the June and August time periods are expected to be the same as those for July, with the only difference being the "noise," then it is reasonable to average these three months, *or maybe more*. This is the case for, say, a five-month average. However, if the May and September sales are expected to represent a seasonal response different from the response that caused the July sales, then the average should be limited to a span of only three points. Such might be the case if the data in table 1 represented the sales of a seasonal item such as lawn mowers.

The conclusion is that the number of points used in the moving average (3, 5, 7, 9,...) should be dictated by some knowledge of the time frame associated with the underlying customer sales motivation (or, for physicists, the *physics*; for engineers, the *forcing function*). The span parameter in the moving-average and the weighted-averaging techniques to be discussed in the next section should generally be chosen based on some idea of the general trends that are the basis of the observed data. With this in mind, the moving-average calculation can then be used to refine the estimate in an intelligent manner. Only in this way can real *information* be derived from the data.

Least-Squares Data Smoothing

The simple moving-average calculation presented in the previous section is a special case of the general concept of weighted averages, which can be stated mathematically as follows:

$$S(t) = \sum_{i=-n}^{i=n} w(i)Y(t+i) \Big/ \sum_{i=-n}^{i=n} w(i) \tag{4}$$

$$= \frac{w(-n)Y(t-n)+\ldots+w(0)Y(t)+\ldots+w(n)Y(t+n)}{\sum_{i=-n}^{i=n} w(i)}$$

For the moving-average case we have $w(i)=1$ for all i.

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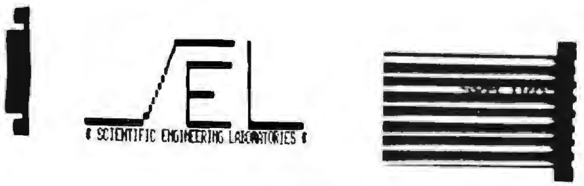

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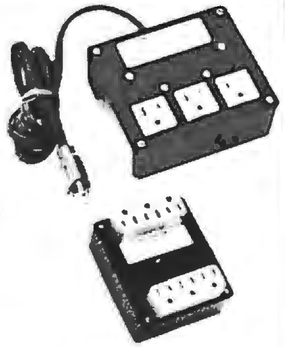

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INTEGER WEIGHTS W(i)

Index *i*	25	23	21	19	17	15	13	11	9	7	5	3
12	1											
11	1	1										
10	1	1	1									
9	1	1	1	1								
8	1	1	1	1	1							
7	1	1	1	1	1	1						
6	1	1	1	1	1	1	1					
5	1	1	1	1	1	1	1	1				
4	1	1	1	1	1	1	1	1	1			
3	1	1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1	1	1	1	
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1
−1	1	1	1	1	1	1	1	1	1	1	1	1
−2	1	1	1	1	1	1	1	1	1	1	1	
−3	1	1	1	1	1	1	1	1	1	1		
−4	1	1	1	1	1	1	1	1	1			
−5	1	1	1	1	1	1	1	1				
−6	1	1	1	1	1	1	1					
−7	1	1	1	1	1	1						
−8	1	1	1	1	1							
−9	1	1	1	1								
−10	1	1	1									
−11	1	1										
−12	1											
Normalizing factor, *N*	25	23	21	19	17	15	13	11	9	7	5	3

Table 3: *Weighting coefficient table for the moving-average method of data smoothing. This is a trivial case, but it clearly introduces the table concept.*

At this point, you should become familiar with the idea of tables of *weighting coefficients,* which are the *w(i)* terms in equation 4. Such a tabulation for moving averages is shown in table 3. Although this table is trivial, it demonstrates the concept of integer weighting coefficients as presented in an article by Savitzky and Golay. (See references.) In that article (and here as well), the weighting coefficients, *w(i)*, are integers, and the normalization *N* is performed after the multiplication/addition sequence:

$$S(t)=\frac{1}{N}\sum_{i=-n}^{i=+n} w(i)Y(t+i) \qquad (5)$$

For a given number of averaging points, the coefficients are easily found in the table, the summation performed, and the result then normalized (by dividing by, for the moving-average case, $N=2n+1$, the sum of all the *w(i)*s from $w(-n)$ to $w(n)$).

For the moving average, it is very obvious how the entries in table 3 were obtained. As an illustrative example, we will now derive the table entries for a linear (as opposed to parabolic, cubic, etc) least-squares smoothing.

Consider a set of data where there are $2n+1$ elements having coordinates (X_i, Y_i). Generally, the method of linear least-squares fitting leads to a "best fit" line having the equation:

$$Y(X)=mX+b \qquad (6)$$

The "best fit" criterion is to find values for *m* and *b* such that the sum of squares, *SS*, is a minimum:

$$SS=\sum_{i=-n}^{i=n}(Y(X_i)-Y_i)^2 \qquad (7)$$

The case we are considering is a little special in the sense that we are examining least-squares fitting with only an odd number of data points. The index range is not the usual $i=1$ to some positive value, but rather $i=-n$ to $i=n$.

The analytical solution to the desired parameters, *m* and *b*, may be found in any standard statistics text. For example, reference 2 presents the results in a particularly convenient form modified here:

$$m=\sum_{i=-n}^{i=n}(X_i-\overline{X})(Y_i-\overline{Y})/\sum_{i=-n}^{i=n}(X_i-\overline{X})^2 \qquad (8)$$

$$b=\overline{Y}-m\overline{X} \qquad (9)$$

In this notation, $\overline{X}$ and $\overline{Y}$ are simply the averages of X_i and Y_i :

$$\overline{X}=\sum_{i=-n}^{i=n} X_i/2n+1 \qquad (10)$$

$$\overline{Y}=\sum_{i=-n}^{i=n} Y_i/2n+1 \qquad (11)$$

The weighting coefficients we are looking for are implicitly contained in the above equations. This may be seen as follows.

We are interested in replacing the data point Y_0 with a "better" one as determined by the least-squares smoothing. This smoothed value is simply:

$$Y=mX_0+b=mX_0+\overline{Y}-m\overline{X} \qquad (12)$$

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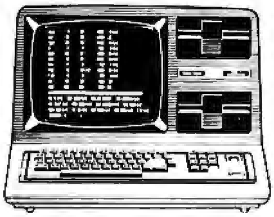

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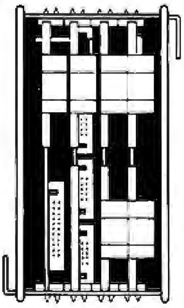

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	Index i	25	23	21	19	17	15	13	11	9	7	5	3
		Number of Averaging Points											
	12	12											
	11	11	11										
	10	10	10	10									
	9	9	9	9	9								
INTEGER	8	8	8	8	8	8							
	7	7	7	7	7	7	7						
	6	6	6	6	6	6	6	6					
	5	5	5	5	5	5	5	5	5				
	4	4	4	4	4	4	4	4	4	4			
	3	3	3	3	3	3	3	3	3	3	3		
	2	2	2	2	2	2	2	2	2	2	2	2	
	1	1	1	1	1	1	1	1	1	1	1	1	1
WEIGHTS	0	0	0	0	0	0	0	0	0	0	0	0	0
	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
	−2	−2	−2	−2	−2	−2	−2	−2	−2	−2	−2	−2	
	−3	−3	−3	−3	−3	−3	−3	−3	−3	−3	−3		
	−4	−4	−4	−4	−4	−4	−4	−4	−4	−4			
	−5	−5	−5	−5	−5	−5	−5	−5	−5				
	−6	−6	−6	−6	−6	−6	−6	−6					
	−7	−7	−7	−7	−7	−7	−7						
	−8	−8	−8	−8	−8	−8							
	−9	−9	−9	−9	−9								
	−10	−10	−10	−10									
	−11	−11	−11										
	−12	−12											
	Normalizing factor, N	1300	1012	770	570	408	280	182	110	60	28	10	2

Table 4: *Weighting-coefficient table for linear, least-squares, first-derivative data smoothing. The symmetry around $i=0$ allows this table to be cut in half when used in a computer program.*

Since the data points are equally spaced, it does no harm to redefine the X_i values. In particular, choose $X_i=i$. In that case, $X_0=0$ and $\overline{X}=0$, giving the smoothed value:

$$Y=\overline{Y}=\sum_{i=-n}^{i=n} Y_i/2n+1 = \frac{1}{2n+1}\sum_{i=-n}^{i=n} Y_i \qquad (13)$$

That is, the smoothed value obtained by the linear least-squares criterion is just the moving average! Thus table 3 gives the weighting coefficients for linear, least-squares data smoothing.

The analysis can be taken yet one more step. If we want the first derivative at $X_0=0$ of the function fitted to the $2n+1$ points centered at X_0, we have simply:

$$\left.\frac{dY}{dX}\right|_{X=X_0} = m \qquad (14)$$

Recalling that $\overline{X}=0$ and noting that $\Sigma X_i\overline{Y}$ is proportional to $\overline{X}\,\overline{Y}$, we get:

$$\left.\frac{dY}{dX}\right|_{X=X_0} = \sum_{i=-n}^{i=n} X_iY_i/\sum_{i=-n}^{i=n} X_i^2 \qquad (15)$$

Thus, the nonnormalized integer weighting coefficients for linear, least-squares, first-derivative data smoothing are:

$$W(i)=i \qquad (-n\le i\le n) \qquad (16)$$

$$\text{with} \quad N=\sum_{i=-n}^{i=n} i^2=\frac{n(n+1)(2n+1)}{3} \qquad (17)$$

The last two equations were used to generate table 4.

Two important characteristic features are apparent from table 4. The first is that the normalizing factor, N, is not simply a sum of the weighting factors in the corresponding column. That is true only for the moving average. Second, the table is symmetrical about the $i=0$ row. The weighting tables are exactly symmetrical or inversely symmetrical, thus making nearly half the entries redundant. This property may be used to save program space.

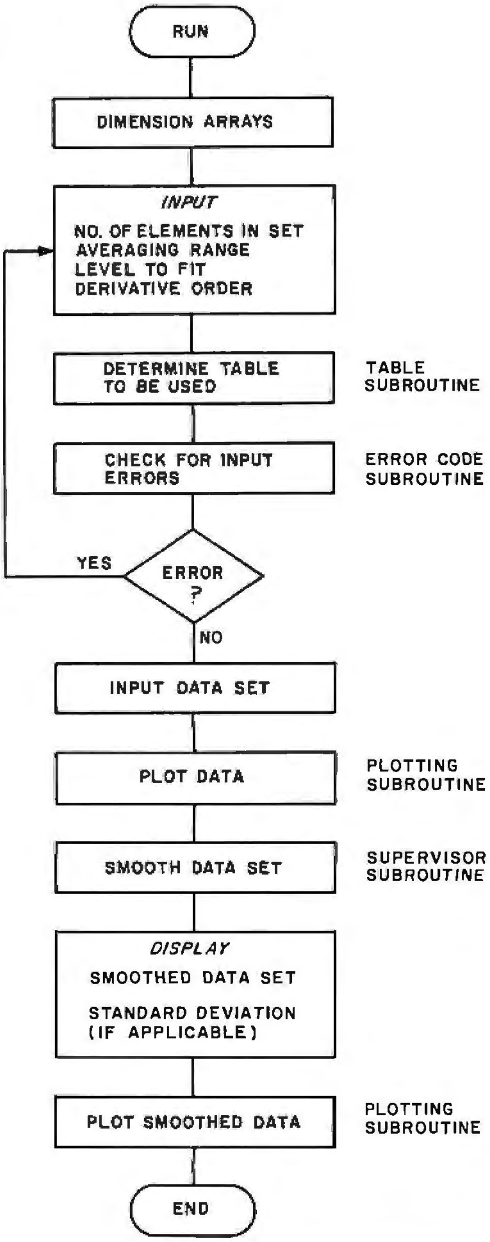

Figure 3: *Flowchart for the least-squares data-smoothing program given in listing 1. See figure 4 for the supervisor subroutine flowchart.*

Implementing the Algorithm

The algorithm represented by equation (5) may easily be implemented as a computer program that applies the appropriate table depending on the prompted inputs. The flowchart for such a program is shown in figure 3.

The program is laid out in modular (ie: subroutine) form. As shown in figure 3, the basic program flow is to input the smoothing parameters, check for errors in those parameters, and then input the data. The input data is

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then plotted, and control is subsequently passed to a generalized supervisor (or executive) program that performs the desired smoothing by calling in several other subroutines. (See figure 4.) The smoothed results are returned to the main program and are printed out along with the standard deviation between the original and smoothed data. In the case of derivative smoothing, which will be discussed later, the concept of standard deviation is not applicable, and 0 is printed. After the numerical display, the smoothed results are plotted.

The plotting routine properly deals with only nonnegative data. This restriction helps keep the program short and simple. If negative values are encountered, only the absolute values are plotted. This generally does not cause much confusion because the values themselves are also printed. The plot is only a convenience item.

The supervisor subroutine is interesting because it can be called by some other data-gathering program instead of the one outlined in figure 3. It requires the variables given in table 5a as input and returns the values given in table 5b.

Before entering the supervisor, the arrays must have already been dimensioned. The reason for this requirement is that in many BASIC interpreters an array cannot be dimensioned more than once. Since the supervisor subroutine may be called more than once, it therefore cannot contain DIM (dimension) statements.

The complete program is shown in listing 1. As can be seen from the listing, the subroutines indicated in figures 3 and 4 are clearly identified by liberal use of REM (remark) statements.

(5a)

N1: The level of fit (0,1,2,3,4,5).
N2: The order of the derivative (0,1,2,3).
N3: The number of points to be smoothed over (3,5,7,9,...25).
N4: The number of data points.
Y(K): The data array.

(5b)

E: The error code if an improper input was given.
Y1(K): The smoothed data (or derivative).
D: The standard deviation (if applicable).

Table 5: *Variables used in the supervisor subroutine that appears in the flowchart in figure 4. This subroutine is given in lines 98 thru 158 of listing 1.*

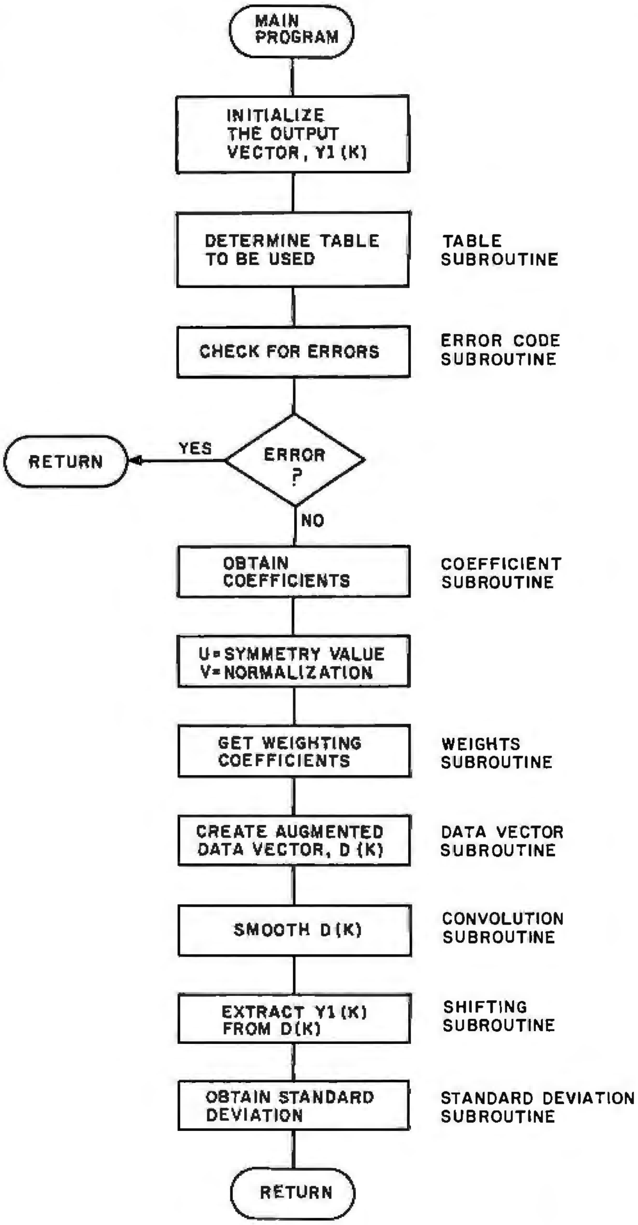
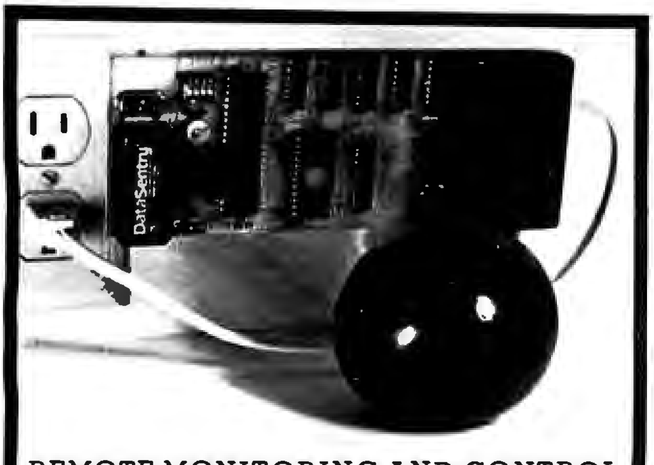


Figure 4: *Flowchart for the supervisor subroutine. The supervisor calls several other subroutines in order to perform the task of data smoothing. Note that the calling program, shown in figure 3, can be entirely replaced by a program that obtains the appropriate inputs and then calls this subroutine.*



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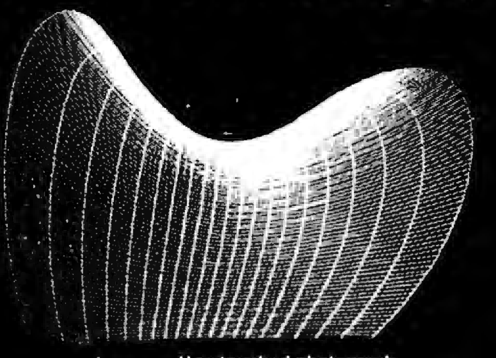

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A
B(I,J)
C(I,J)
D
D(I)
E
E(I)
E2
E4
I
J
K
K1
L

M
N1
N2
N3
N4
O
P
R4$
U
U(I)
V
V(I,J)
W(I)
Y(I)
Y1(I)

Table 6: *A table of variables used in the subroutines of listing 1. This table is used to prevent duplication of variable names when generating a new main program that uses the subroutines of listing 1.*

		Derivative			
		0	1	2	3
Level of Fit	1	Yes	Yes	No	No
	2	Yes	Yes	Yes	No
	3	Yes	Yes	Yes	Yes
	4	Yes	Yes	Yes	Yes
	5	Yes	No	Yes	No

Table 7: *Table of permitted data-smoothing operations with the program shown in listing 1. The derivative/level-of-fit combinations omitted were done to keep the program at a reasonable length.*

The smoothing parameters are stored as explicit arrays. It would have been more efficient to store this information in BASIC data statements. However, the supervisor (and the routines it calls) is meant to be a subroutine, and it is not good programming to use data statements in subroutines that may be called often. For example, if the main program and the subroutine both have data stored that way, how does the subroutine read the appropriate data and restore the data pointer to its proper location after repeated calls? The way the program shown in listing 1 is written, the main program (statements 1 thru 96) can be replaced by a user program without any change in the subroutines. If you want to replace the main program, keep in mind that the subroutines have variables that should not also be employed in the calling program without some caution. The subroutine variables list is shown in table 6.

Using the Program

As presented, the program may be used to smooth data over the range of fits and derivatives shown in table 7. As an example of how the program operates, we will now apply it to the sales-volume example discussed earlier.

Listing 2 shows a sample run in which a parabolic (ie: second level) fit was applied using a five-point average. Note that sixteen data points are necessary to do this, since we require an additional two points on either side of the point of interest. (These points can be deleted later.) The user inputs are underlined. If a "fatal" error in the parameter input sequence had been made, the error

Text continued on page 290

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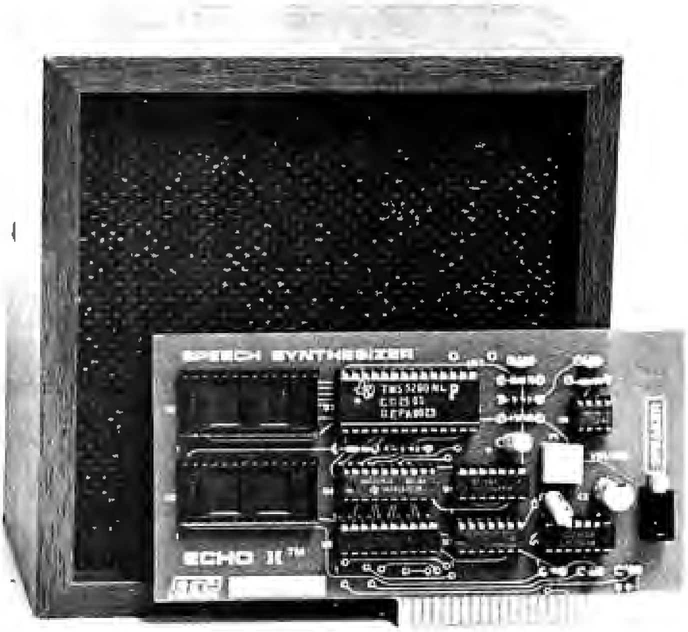

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Listing 2: *Sample run of data smoothing program, using data from table 1. In this listing, user input is underlined.*

```
RUN

DATA SMOOTHER FOR EQUALLY
SPACED DATA SETS


INPUT THE NUMBER OF
DATA POINTS IN SET: ?16

HOW MANY POINTS ARE
TO BE AVERAGED OVER: ?5

WHAT IS THE DESIRED LEVEL
OF FIT (1,2,3,4,5): ?2

WHAT IS THE DESIRED
DERIVATIVE (0,1,2,3): ?0

INPUT DATA AS PROMPTED:

 1     ?1235
 2     ?2408
 3     ?3279
 4     ?2421
 5     ?4864
 6     ?3629
 7     ?3180
 8     ?4744
 9     ?6181
 10    ?3653
 11    ?3418
 12    ?1722
 13    ?1235
 14    ?2408
 15    ?3279
 16    ?2421

INPUT DESIRED PLOT WIDTH: ?50


***** DATA PLOT (SCALED) *****


MAXIMUM VALUE=  6181


I----I----I----I----I----I----I----I----I----I----I
:                                                 :
:        *                                        :
:                                                 :
:                  *                              :
:                                                 :
:                         *                       :
:                                                 :
:                  *                              :
:                                                 :
:                                      *          :
:                                                 :
:                            *                    :
:                                                 :
:                        *                        :
:                                                 :
:                                     *           :
:                                                 :
:                                                 *
:                                                 :
:                            *                    :
:                                                 :
:                          *                      :
:                                                 :
:            *                                    :
:                                                 :
:        *                                        :
:                                                 :
:                  *                              :
:                                                 :
:                         *                       :
:                                                 :
:                  *                              :
I----I----I----I----I----I----I----I----I----I----I

CONTINUE?Y
```

```
CALCULATING.....





THE SMOOTHED DATA IS:

 1       1144.4
 2       2509.7429
 3       2725.5429
 4       3450.3429
 5       3883.1714
 6       3906.4571
 7       3468.6
 8       4889.5429
 9       5315.6286
 10      4511.1714
 11      2867.3714
 12      1912.2
 13      1441.8286
 14      2362.1429
 15      3142.4571
 16      2093.7429

CONTINUE?Y

THE STANDARD DEVIATION
BETWEEN THE SMOOTHED AND
UNSMOOTHED DATA SETS IS 589.8642

CONTINUE?Y



INPUT DESIRED PLOT WIDTH: ?50


***** DATA PLOT (SCALED) *****


MAXIMUM VALUE=  5315.6286


I----I----I----I----I----I----I----I----I----I----I
:                                                 :
:         *                                       :
:                                                 :
:                      *                          :
:                                                 :
:                        *                        :
:                                                 :
:                               *                 :
:                                                 :
:                                   *             :
:                                                 :
:                                   *             :
:                                                 :
:                               *                 :
:                                                 :
:                                            *    :
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:                                         *       :
:                                                 :
:                         *                       :
:                                                 :
:                *                                :
:                                                 :
:            *                                    :
:                                                 :
:                     *                           :
:                                                 :
:                            *                    :
:                                                 :
:                  *                              :
I----I----I----I----I----I----I----I----I----I----I

CONTINUE?
```

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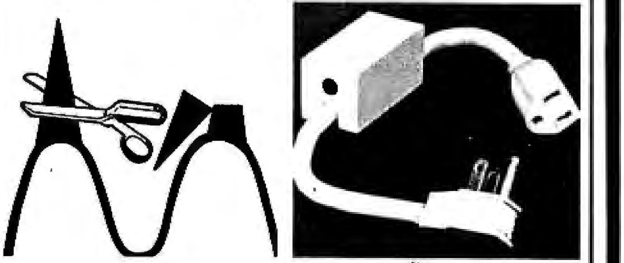

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Error Code	Explanation
0	No Error.
1	Number of data points to be averaged over is too small.
2	Number of data points to be averaged over is too large.
3	The order of the derivative is greater than the level of the fit, which gives a trivial (0) result.
4	The level of fit attempted is too high.
5	The order of the derivative attempted is too high.
6	The particular table required is not available in the program.
7	There is not enough data to do the smoothing requested.
8	An illegal or otherwise out-of-range parameter was given.

Table 8: *Table of error codes returned by a call to the supervisor subroutine.*

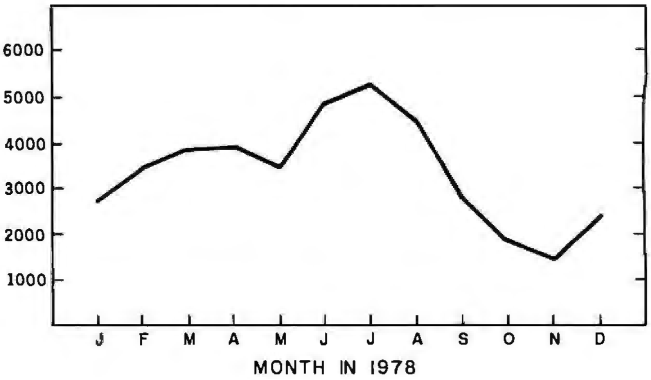

Figure 5: *Chart of smoothed sample data using five-point parabolic smoothing. This chart is identical to the one plotted in listing 2.*

Text continued from page 286:

would have been indicated according to the code in table 8.

As shown in listing 2, the program prompts for all the inputs. The user can then specify the plotting width for the terminal being used. Note that only absolute values are plotted. The program then performs the smoothing and calculates the standard deviation (when applicable). Finally, the routine plots the smoothed data.

The smoothed data for the sales-volume example has been replotted as shown in figure 5. Observe that the first two and last two of the sixteen input values have been discarded. If a seven-point average had been used, three points on either side of the desired results would have been dropped. Comparing figure 5 with figure 2, we see that the five-point parabolic smoothing looks much more "reasonable" than the three-point and five-point linear smoothing. The peak in July is apparent, as well as the dips in May and November. Recalling that the nominal purpose of the example was to better predict the July sales volume, we find the value to be 5316 units, with a standard deviation of 590. We expect that the standard deviation will be lower for the parabolic fit than for the corresponding linear fit, and it is.

Discarding points at the ends of the smoothed data set is necessary. The smoothing at each position uses data on either side. At the extremes of the data set there is missing information. The program supplies values (eg: 0) for this missing data. In general, if the number of data points averaged over is $N3$, then the number of data points that should be discarded at either end of the data list is $(N3-1)/2$.

Square-Wave Example

We will now look at the results of smoothing a very discontinuous function, the square wave. The purpose is to show the comparative effects of the various levels of fit on "smoothing" an abrupt transition.

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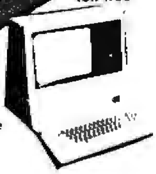

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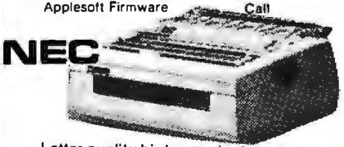

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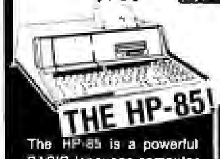

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Using a computer, the mechanics of data smoothing can be made fairly simple.

To electrical engineers, the multipoint averaging technique presented in this discussion is the equivalent of *nonrecursive digital filtering*. The way in which the calculation is applied is identical to *convolution*. According to one of the important theorems of Fourier transform theory, performing a discrete convolution on a "signal" (the data) is the same as frequency filtering. The shape of the frequency filter is simply the discrete Fourier transform of the weighting function.

Thus, every table of weighting coefficients can be converted to a corresponding set of filter coefficients. Usually, in electrical engineering one chooses the frequency filter response and *then* finds the convolution (ie: weighting) coefficients. In our case, we chose our coefficients according to a least-squares curve-fitting criterion first. However, the idea of frequency filtering is still valid.

The square wave is built of many spatial-frequency components. Filtering out some of the high-frequency components results in a less-than-abrupt square-wave transition. Figure 6a on page 294 shows the square-wave input data that was provided as an example to the program. The square wave is 1 unit high and 18 units wide. For clarity, lines have been drawn between the points plotted by the computer.

Figure 6b shows the effect of applying a linear (first level fit, zeroeth-order derivative) smoothing using nine averaging points. The effect is simple. Applying a parabolic fit leads to a more curious form. (See figure 6c.) The dashed parts of the "curve" indicate negative values. The overshoot effect is called *ringing*.

Going one step further and applying a quartic (fourth-order polynomial) smoothing, we get figure 6d. Note that the ringing has increased, but the standard deviation between the square wave and the quartic smooth version has decreased relative to the parabolic or linear case. There is more ringing but a better fit. The overshoot effect is related to the *Gibbs phenomenon*, which is a nonuniform convergence problem in Fourier transform theory.

The square wave may also be used to demonstrate derivative smoothing. (See figures 7a and 7b on page 298.) It might be argued that these curves are not very smooth: however, remember that the unsmoothed derivative is an infinite spike!

Figure 7a calls attention to an important point regarding derivatives. From figure 6b, we might have expected the linear smoothing of the first derivative to be just a step from 0 to 1/9 and back to 0 again, since the linearly smoothed function has a constant slope ramp on one side. However, the result shown in figure 7a resembles a parabola. The reason for the difference is that the derivative is not derived from the smoothed data. Rather, at each data point the derivative of the curve fitted over the nine-point interval surrounding that position is used. This is *not* the same as the slope between neighboring smoothed data points, a very important conceptual difference.

As you might expect, the situation for the second and third derivatives is even more complicated. Examination of those forms is left to you.

Conclusion

As indicated earlier, the mechanics of data smoothing can be made fairly simple given a computer that can execute the program provided. Running the program is easy. Choosing the appropriate fitting parameters and applying the results is much more difficult. The two main choices for fitting are the averaging range and the level of fit. The averaging range should be chosen based on an idea of the *true* correlation between the data points. If changes over a range of *N*3 are *not* expected, then an averaging range of that size is warranted.

Choosing the level of fit is more difficult. In the sales-volume example, the parabolic fit appeared better than the corresponding linear fit. However, that is a subjective judgment based largely on the feeling that the peak and two major dips observed in the data should appear in the smoothed curve. There is still no replacement for common sense! ■

REFERENCES

1. Savitzky A, and M J E Golay. "Smoothing and Differentiation of Data by Simplified Least Squares Procedures." *Analytical Chemistry*, Volume 36, Number 8, July 1964.
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3. Weast, R C and S M Selby. *Handbook of Tables for Mathematics, Third Edition*. Cleveland OH: Chemical Rubber Company, 1967.

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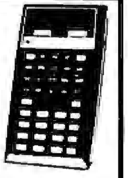

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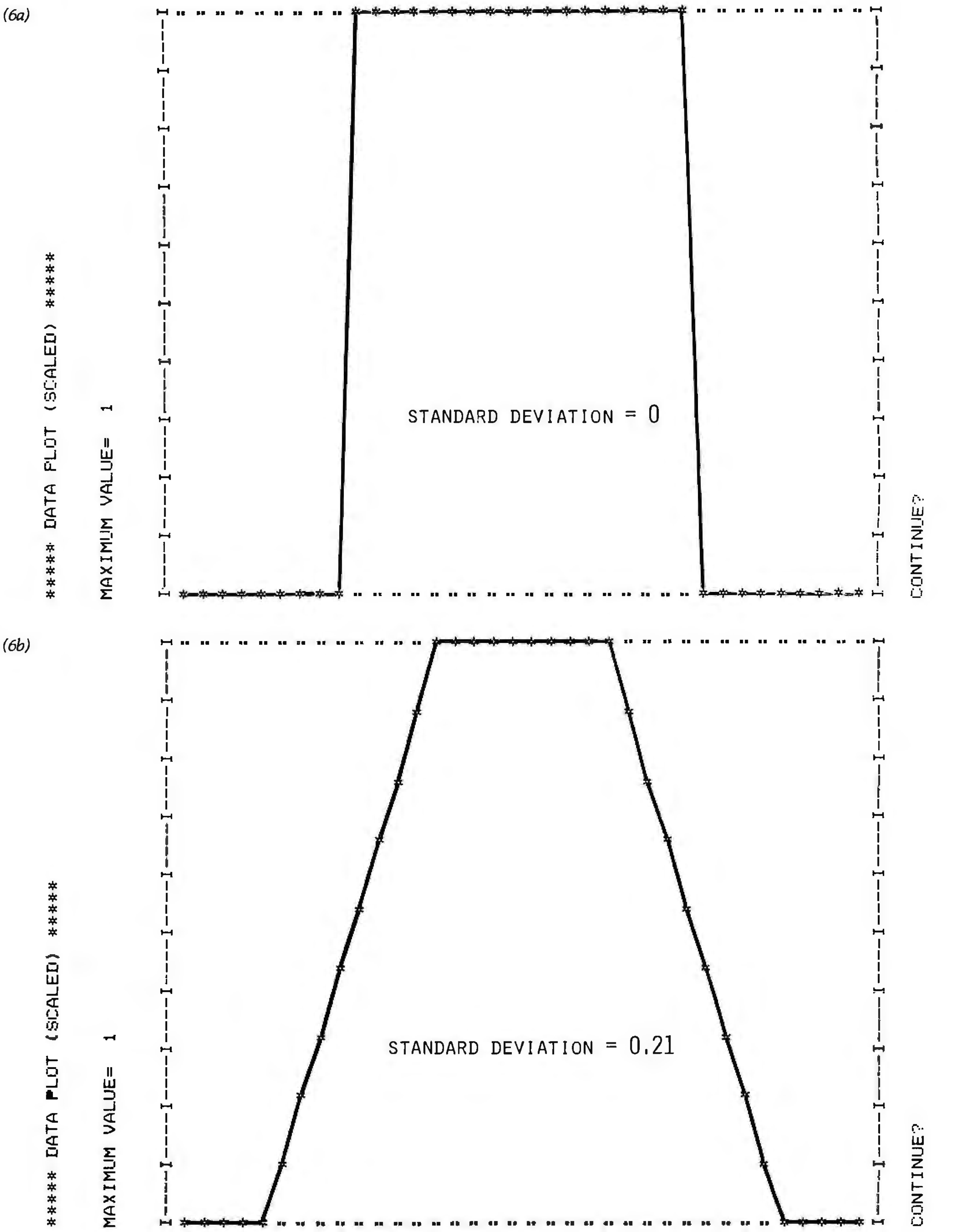

Figure 6: *Smoothing a square wave. The test square wave in figure 6a was smoothed in figures 6b thru 6d using a nine-point average. Figure 6b shows a linear smoothing. Figure 6c shows the results of a parabolic smoothing with a cubic smoothing giving the same results. Figure 6d shows the results of a quartic and quintic smoothing. In all figures, dashed lines denote negative values plotted here as positive. These figures and those of figure 7 were generated using the program given in listing 1.*

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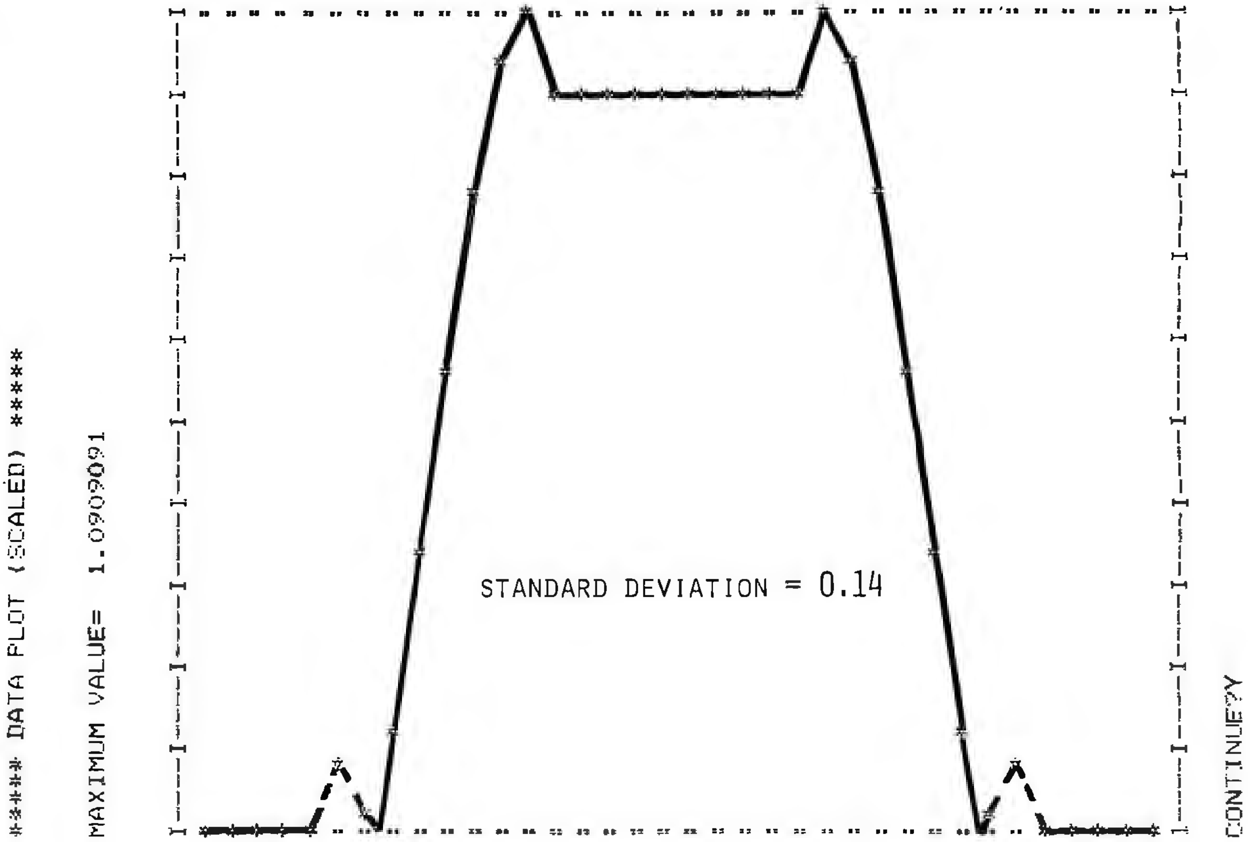

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MAXIMUM VALUE=  1.0909091
CONTINUE?Y
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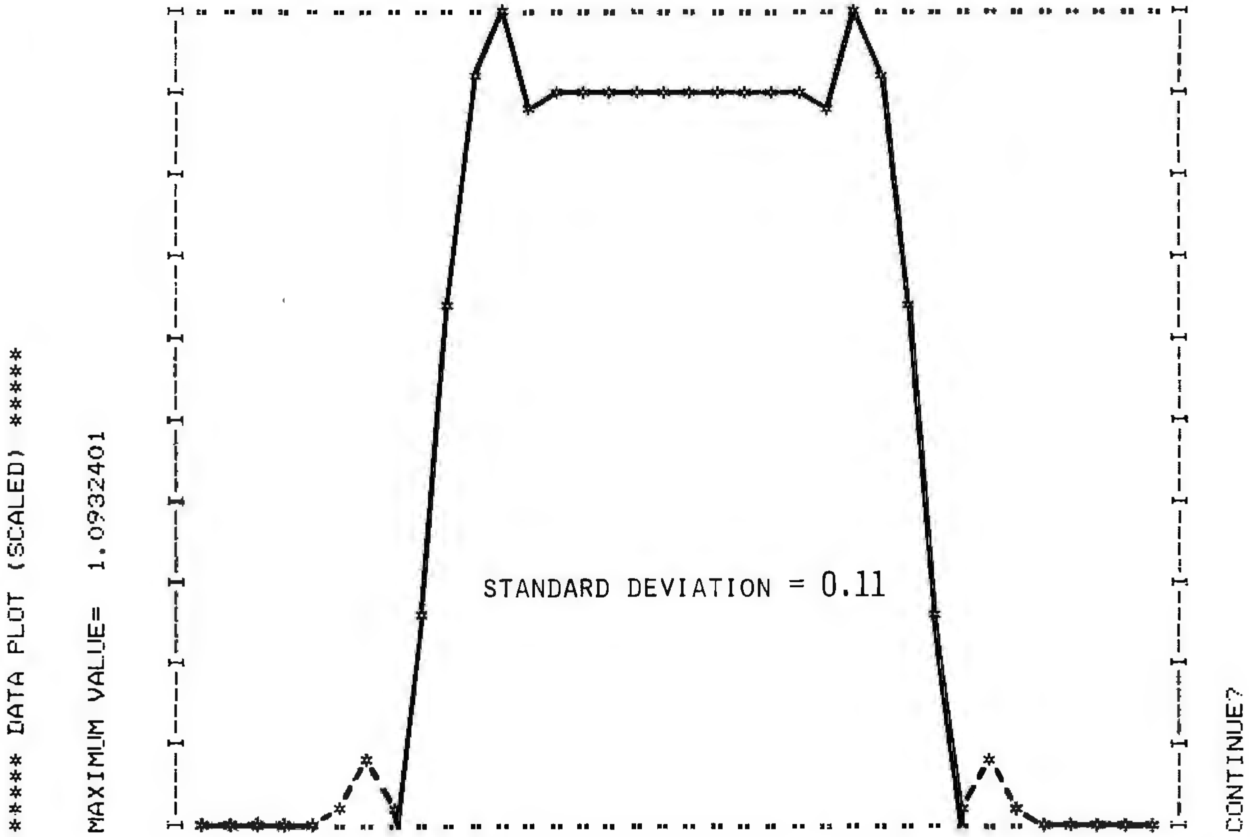
STANDARD DEVIATION = 0.14

(6d)



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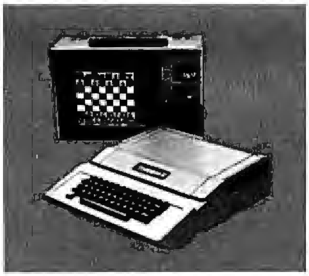

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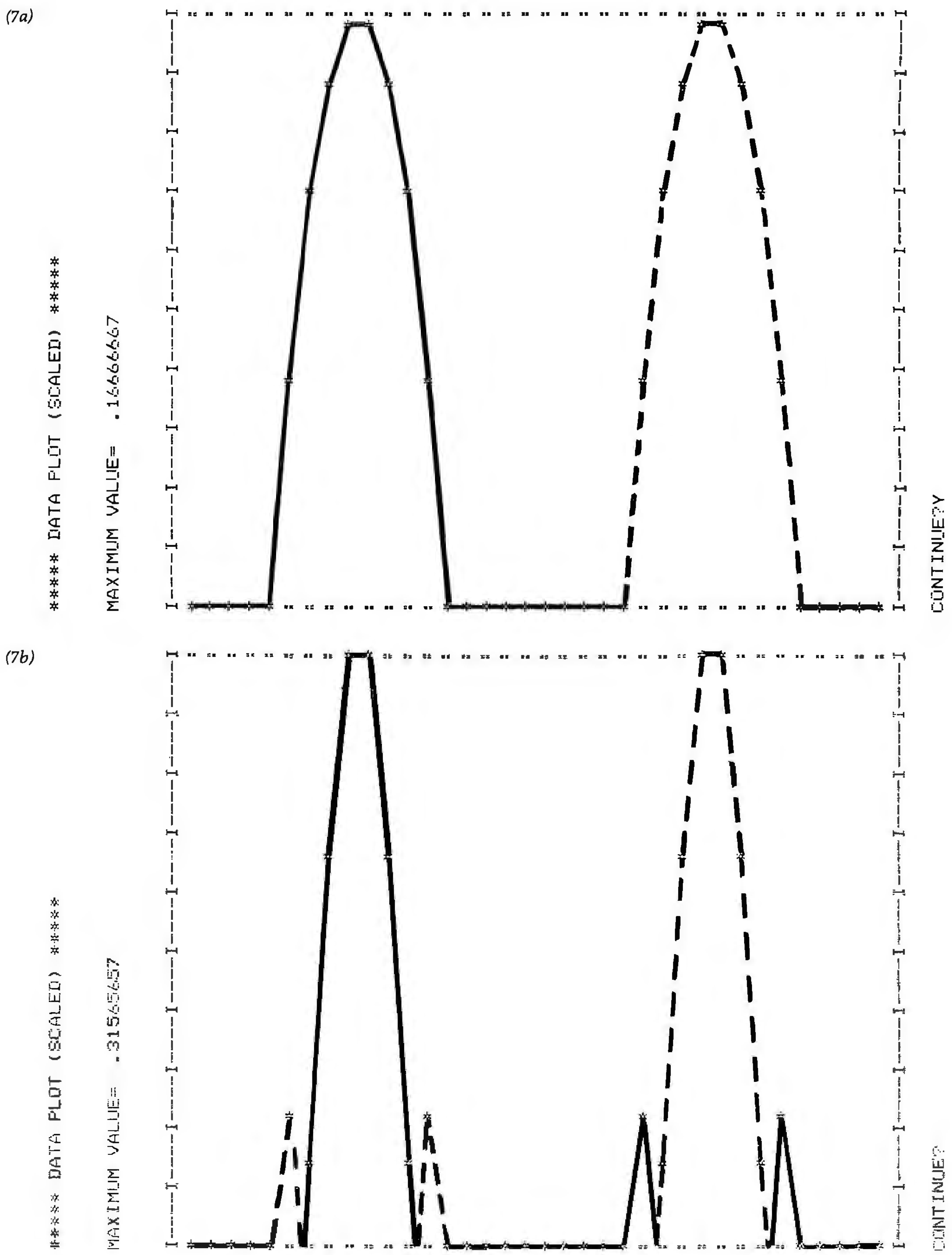

Figure 7: *Least-squares smoothed (nine-point) first derivatives of the square wave shown in figure 6a. Figure 7a shows the result for a linear and a parabolic first-derivative smoothing. (Both are the same.) Figure 7b shows the result for a cubic and quartic first-derivative smoothing.*

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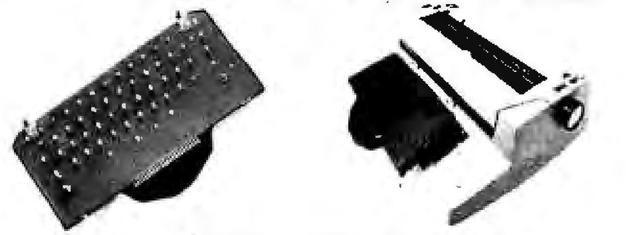

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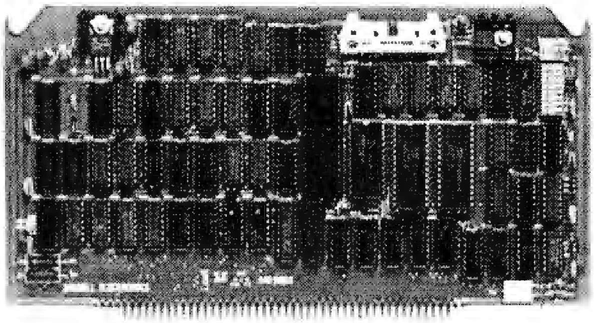

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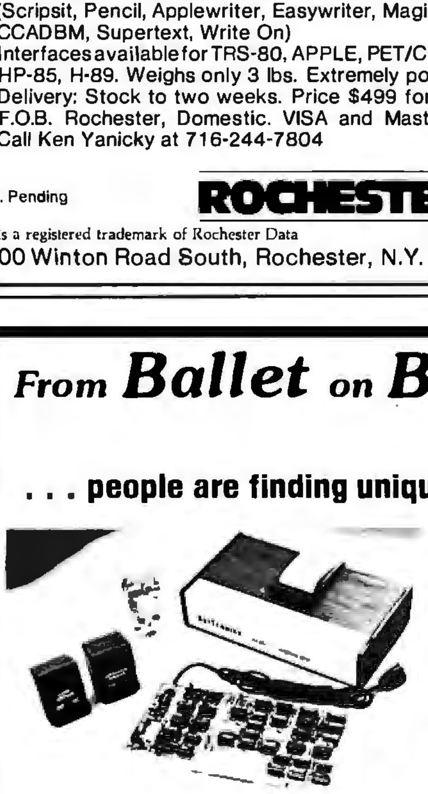

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The New Literacy:

Programming Languages as Languages

> *"To be a good programmer today is as much a privilege as it was to be a literate man in the sixteenth century."*
>
> *Andrei Ershov, USSR Academy of Sciences, Novosibirsk University*

Jon Handel
3 Gilmore Ct
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Many people would declare that Ershov is making an incongruous comparison: he compares the ability to read, a universally desirable trait, with the ability to program a computer, which fewer people deem to be a desirable trait. Stranger still, he compares reading, which is linked with the appreciation of literature and with the artistic use of language, to programming. Programming is the recording of arcane codes that make a computer perform some data manipulation. Such coding seems unconnected with art and language, yet he implies that it is. Consonant with this view, program-coding systems are called languages, but most people would find it difficult to specify any way in which a computer programming system merits the label *language*.

Some people are, in fact, hostile to the very idea that programming and programming languages have anything at all to do with creativity and language. Sometimes these people are confused between the computer and its human programmer, attributing programming to the computer rather than to human beings.

Programming languages *are* in fact languages in a meaningful sense of that word: they exhibit some of the complexity of form and function that natural languages do. Computer programming languages are much more than mere coding systems.

It is important that programming languages be recognized by lay people as languages. The ability to program computers, or at least to understand programming and computers in a general way, is important today, just as literacy was important in the sixteenth century. Those who lack the new literacy—computer literacy—will find increasing difficulty in participating effectively in political, professional, and business life. If you don't know what a computer can do, how can you decide whether we should sell them to the Soviets—or whether you should buy one to help around the house?

What a computer can do is greatly determined by its software—that is, by the programs it executes. The software is expressed in some programming language, and this is the subject to which we now turn.

To explore the nature of programming languages and examine the characteristics of natural language exhibited by programming languages, the term *language* must first be defined. A reasonable definition is that language consists of a set of symbols, sounds, and/or gestures, and a set of rules according to which these elements may be systematically combined to communicate an indefinite number and variety of thoughts and ideas. Usually, these symbols are combined into subunits called words, and these words are then combined into sentences.

Notice that the communication effected by a language need not be between people; it may also involve machines. A computer programming language is a language which is most often used for communication with computing machinery. The instrument of communication is a computer program, which is a detailed, step-by-step set of directions for the computer to follow. The purpose of a particular program can be practically anything from printing mathematical tables to controlling oil refineries.

Three computer programs in common languages will be examined. Following this is an examination of the communicative function of programming languages and the grammar of programming languages. The examples presented will show that programming languages are much more than mere coding systems. They exhibit structural patterns and concepts that are both complex and in some ways parallel to patterns and concepts of natural languages.

(The several computer languages discussed in this article represent only a small fraction of the existing languages. Jean Sammet of IBM compiled a list of 167 major languages, noting the existence of numerous dialects of some of these (*Communications of the ACM*, December 1976, page 655). In an earlier roster (*Communications of the ACM*, July 1972, page 601), Sammet presented a chronological chart of languages arranged by application area (eg: scientific computation, business data processing, experimental, etc). There are dotted, dashed, single, and double lines on the chart representing evolutionary changes from one language to another, as well as circles, squares, triangles, and three different type styles. The whole effect is that of a collapsed and tangled spiderweb. This complexity reflects the diversity of programming languages in use today.)

My sample programs deal with a specific problem. Imagine a computer user who wishes to calculate the reciprocals of some numbers. The user is sitting at a computer terminal and will use it to type in the numbers to the computer and receive the printout of the reciprocals. The programs illustrated will allow her or him to input a number X and have the computer print out the reciprocal of the number X, which is 1 divided by X. If the number X is 0, instead of printing the result of its computation, the program will print the message "Reciprocal of 0 does not exist."

BASIC Program

Listing 1 shows the reciprocal program coded in the BASIC language. When this program is typed into the computer as shown, and the command RUN is typed, the computer begins executing the program in the order of increasing line numbers. Line 10 instructs the machine to print the message in quotation marks exactly as it is written. The message reminds the user of what he will be expected to do. Line 20 causes the machine to print a question mark at the terminal and wait for the user to type in a number. Since the statement identifies the input as X, whatever number the user types will be placed in the variable X. The program can then use the number by referring to X.

In line 30, the program tests to see if X is equal to 0. If so, the computer does not execute the next statement in numerical order (line 40), but transfers control to line 70, as directed by the IF-THEN statement, and continues from there. Line 70 causes the printout of the message indicating that the reciprocal of 0 does not exist. Line 80, which is executed next, tells the computer that the program is over. The computer stops executing the program, and the user may restart it and enter a new number, or run a different program altogether.

If X does not equal 0, then the program continues from line 30 on to line 40. Line 40 performs a computation of the reciprocal of X. This value is placed in the variable Y. Subsequent references to Y will use this computed value.

Continuing with the sequence, line 50 prints the numerical value of Y. If the number typed in were 2, then Y would be printed as 0.5. Finally, line 60 causes the computer to stop executing the program. This line has essentially the same effect as the END statement in line 80.

> **It should be realized that even though programming languages are used for communication in many ways, they do not serve the same communicative functions as natural languages. Programming languages are used for communicating technical procedures in a precise fashion.**

ALGOL Program

Listing 2 shows the reciprocal program written in ALGOL 60. ALGOL 60 was created and formally defined in a report of an international committee which appeared in 1960. ALGOL 60 is important because its syntax was described using a formal notation. (See "An Introduction to BNF" by W D Maurer, BYTE, January 1979, page 116.) A different version of the language, ALGOL 68, appeared eight years later.

When execution begins, the first line of the program in listing 2 serves two distinct functions. The word BEGIN indicates the beginning of a program, and the phrase REAL X,Y declares that variables named X and Y will be used in the program. These two variables are to represent real numbers (ie: numbers that can have a decimal point and a decimal fraction part, for example, 0.5, 6.2, or 4).

On the next two lines, the PRINT and INPUT directives work in a similar manner to those in the BASIC program, although the syntax is slightly different.

The IF-THEN-ELSE structure on the succeeding lines is different from the IF-THEN encountered in BASIC. The intent is the same, but the structure is more complex. In the ALGOL program, if X is equal to 0, the clause following THEN is executed [PRINT ("RECIPROCAL OF 0 DOES NOT EXIST")]; otherwise, the compound statement following ELSE is executed. This compound statement is composed of the two statements Y:=1/X, which assigns the value of the reciprocal of X to Y, and PRINT(Y), which prints out the value of Y. These two statements are bracketed by the pair of words BEGIN and END. This bracketing allows the two statements to be treated syntactically as a single statement group. If X does not equal 0, it is this compound statement that is executed.

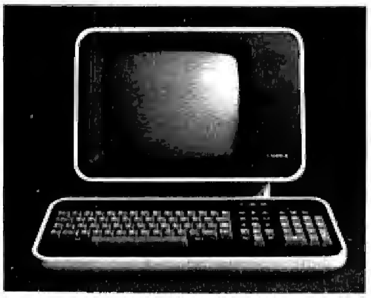
Finally, we encounter the second END statement, which is paired with the BEGIN at the beginning of the program. This indicates the end of the program; execution of the program terminates.

Notice that, in contrast to the BASIC program, the physical layout of the ALGOL program displays its logical structure. The indentation shows the functional grouping of individual statements. This indentation, and the associated BEGIN-END delimiters, are used to clarify the structure of ALGOL programs. [**Editor's note**: *Indentation is also used to clarify structure in other languages, such as Pascal. . . .* **RSS**]

Despite the differences between ALGOL and BASIC, one common characteristic of the two languages is that they are both similar to English and conventional algebra in the notation and verbs (eg: PRINT and INPUT) that they use. This similarity is not a characteristic of the language used for the third version of the reciprocal program, which makes extensive use of Greek letters and special symbols.

APL Program

The language of the third



Listing 1: *Reciprocal-determining program written in the BASIC language.*

```
10        PRINT "INPUT NUMBER FOR RECIPROCAL";
20        INPUT X
30        IF X=0 THEN GOTO 70
40        LET Y=1/X
50        PRINT Y
60        STOP
70        PRINT "RECIPROCAL OF 0 DOES NOT EXIST."
80        END
```

Listing 2: *Reciprocal program written in ALGOL.*

```
BEGIN REAL X,Y;
PRINT ("INPUT NUMBER FOR RECIPROCAL");
INPUT (X);
IF X=0 THEN
    PRINT ("RECIPROCAL OF 0 DOES NOT EXIST.")
ELSE
    BEGIN
    Y: =1/X;
    PRINT (Y)
    END
END
```

Listing 3: *Reciprocal program written as an APL function.*

```
          ∇ RECIPROCAL
(1)       ' INPUT NUMBER FOR RECIPROCAL'
(2)       → (0=X←□)/5
(3)       □ ←Y← ÷X
(4)       → 0
(5)       ' RECIPROCAL OF 0 DOES NOT EXIST.'
          ∇
```

reciprocal program is APL (A Programming Language), which was created by Dr Kenneth Iverson. The keys to its power are conciseness of notation and ability to deal with tables of data (arrays) as easily as with a single number. This conciseness can, however, make even a simple program difficult to read for the uninitiated.

Listing 3 shows our reciprocal routine written in APL. The first line, which is unnumbered, denotes the beginning of an APL function to be named RECIPROCAL. (Programs are called *functions* in APL. Once a function is entered into the computer, it is executed by typing its name, RECIPROCAL.) Execution proceeds starting with line 1.

Line 1 simply causes the computer to print the text that is within the single quotation marks.

Line 2 illustrates some of the complexity of the APL language. This line does two separate things. The characters X←□ cause input from the computer terminal to be placed in the variable X for subsequent use. These three characters do the same thing as the seven characters INPUT X (counting the space) do in BASIC.

Continuing on line 2, once X has been assigned the numeric value input from the terminal, the expression 0=X compares the value, now in X, against 0. If X is equal to 0, the expression produces the logical value 1; if X is not equal to 0, the expression produces the logical value 0.

This logical result of either 0 or 1 is still within the parentheses of line 2. The combination of this value (0 or 1) and the /5 to the right of the parentheses produces either a null vector or the value 5.

The arrow → at the left of line 2 is followed by the expression in parentheses, whose value is either the null vector or 5. The arrow is known as the *branch arrow*; to branch is to change the order of execution of program statements. The branch arrow does this as the GOTO statement does in BASIC. If the value following the arrow is 5, indicating that X is equal to 0, the arrow causes a branch to line 5. If the value is the null vector, indicating that X is not equal to 0, no branch at all is taken and execution proceeds to line 3 of the function.

In summary, line 2 performs the functions of the following two lines from the BASIC version of the program:

```
20 INPUT X
30 IF X=0 THEN GOTO 70
```

Line 3, which should be read from *right* to *left*, calculates the reciprocal of X (written in APL as ÷X), places this value in the variable Y, and then prints Y. This line functions as do the lines:

```
40 LET Y=1/X
50 PRINT Y
```

in the BASIC program.

Line 4 seems to direct a branch to line 0. Actually, →0 is an idiom that means branch out of the function entirely—in other words, stop the program.

Finally, line 5, which is only executed if X was found equal to 0 in line 2, directs the computer to print the text in quotation marks. After line 5 is executed, the computer encounters the ∇ symbol, which denotes the end of the program.

Uses of Programming Languages

Programming languages, like all languages, are used for communication in a variety of ways. Two broad classifications are communication between people and machines, and communication between people and people.

The way in which people use programming languages to communicate their desires to computers is self-evident. If the user desires computation of reciprocals, a program is written for this computation in a language understood by the particular computer at the programmer's disposal. It should then be entered into the machine. The aspect of communication is the same for more difficult tasks.

Programming languages are also used for communication between people. For example, since many programming projects involve more than one person, those involved must communicate. Naturally, much of this communication requires transmission of segments of the program being worked on.

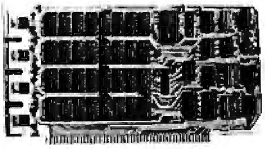
Another example of this type of communication is the publication in professional journals of algorithms expressed by programs. One of the most popular languages for such communication is ALGOL 60. The ALGOL 60 report, by defining a publication language differing slightly from the hardware representation, explicitly recognizes the two facets of programming language communication.

It should be realized that even though programming languages are used for communication in many ways, they do not serve the same communicative function as natural languages. Programming languages are used for communicating technical procedures in a precise fashion. Natural languages are not very well adapted to this type of communication. Indeed, natural languages, when used for communication of detailed instructions, are often augmented with charts, diagrams, pictures, and mathematical expressions.

Grammar and Syntax

The *noun* of a programming language is the *variable*, which is conceptually an object or storage cell capable of holding information. The primal variable, seen in the reciprocal programs, can hold only one number. There are two distinct directions in which this concept of variable may be extended: by allowing different *types* of data to be stored in the variable, or by allowing different *amounts* of data to be stored.

In most languages, if different types of data are to be stored in different variables, the variables themselves must possess the attribute of *data type*. This attribute is an identification that a particular variable can be used to store a particular type of data. Consider some of the data types offered by ALGOL 68 as shown in table 1. For example, to declare in an ALGOL 68 program that I and "class size" (a single variable; lowercase and spaces are okay) are to be variables capable of storing an integer; COST, to be capable of storing



a real number, and NAME, to be capable of storing a character string (such as "John Smith"); the programmer would use the following statements:

```
INT I, class size;
REAL COST;
STRING NAME;
```

The structure of these declarations is:

predicate-adjective subject

with an omitted linking verb. This structure is similar to the English structure:

subject **is** predicate-adjective

Data types are attributes of variables and are specified in the same way as an attribute of a noun in English. (The parallel is even stronger in Russian, since that language usually omits the linking verb in the present tense.) The names of the data types (INT, REAL, CHAR, STRING, and others) are adjectives in the grammar of ALGOL 68.

In addition to the four data types outlined above, ALGOL 68 offers a number of other data types, each of which is an extension of the concept of data type in a distinct direction. One class of data type that is of a particular interest is *reference-to modes*. (*Mode* means data type.)

Such modes can be viewed simply as the recognition of the difference between nouns and pronouns. A noun, in English, is a symbol for some person, place, or thing. A pronoun is a reference to a particular noun, termed the *referent* of the pronoun. With this distinction in mind, consider the following sequence of ALGOL 68 statements:

```
BEGIN
INT I,J;
I:=2;
J:=I+3;
END
```

This seems simple enough, but consider carefully the statement J: =I+3. What is being added here? The 3, certainly, is being used as it stands, but the I really is not. The I refers to a number (2 in this case) and it is actually this number that figures in the addition, 2+3. The constants 2 and 3 in this program are the nouns and the variables I and J are pronouns.

The declaration INT I,J is a shorthand: it does not signify that I and J are themselves of type INT, but that they are to *refer to* objects (ie: numbers) of type INT. The variables themselves are of mode (type) REF INT, meaning *reference to integer*. REF REAL, REF CHAR, REF STRING, etc are all possible. These different types of reference-to modes are analogous to pronouns of different genders and cases in human languages.

The distinction between variables and the values to which they point may strike you as pointless. Indeed, some languages—BASIC, APL—ignore the distinction. Others—ALGOL 68, Pascal—don't. Like genders and cases in Russian, *pointer* variables (a more common term than *reference-to*) can be a pain to learn, but once learned, a subtle and useful tool.

The concept of variable type or mode is only one way in which the concept of variable may be extended. Another extension is to remove the restriction that a variable hold only one item. Such variables must have some internal organization or structure to allow access to subsets of the stored data. One type of structured variable is the array.

In an array, all data items are of the same type (eg: all integers) and are arranged in a regular rectangular pattern. A one-dimensional array is called a vector or list; an example is:

95 78 99

This three-element vector could represent the final examination grades of three students; the first scored a 95, the second a 78, and the third a 99. Though all elements of the vector are integers, the programmer can just as easily work with a vector of real numbers, of characters, or of any particular type. To create this vector of integers for use in an ALGOL 68 program, use the following statements:

```
[1:3] INT GRADES;
GRADES:=(95,78,99);
```

The first statement declares GRADES to be a vector of integers, the elements of which are numbered from 1 to 3. The second statement assigns to GRADES the three grades 95, 78, and 99. It is clear that a vector is called a one-dimensional array because it is an array of numbers that extends in one direction only (mathematically, along one dimension).

An example of a two-dimensional array, or matrix, is:

$$\begin{array}{cccc} 96 & 95 & 98 & 95 \\ 67 & 83 & 72 & 78 \\ 97 & 95 & 99 & 99 \end{array}$$

Each row could correspond to the test grades of a particular student; thus, student number 1 scored a 96 on the first test, a 95 on the second, a 98 on the third, and a 95 on the final exam. A matrix is called a two-dimensional array because it extends along two directions, horizontal and vertical.

Higher-dimensional arrays are also possible, though clumsy to represent on the printed page. It is even possible in ALGOL 68 to have arrays of arrays, arrays of arrays of arrays, and so forth.

The concept of array is analogous to that of plurals in natural languages. At one stroke, a sentence such as *Cheshire cats always grin* makes a statement about all members of the set of Cheshire cats. Similarly, the expression Y: = GRADES − 5 subtracts 5 from all elements of GRADES at once, setting Y equal to (90,73,94).

There is also a parallel between array subscripting and prepositional phrases. Consider again the vector GRADES. To access the first element of GRADES by itself, the subscripts to the elements in GRADES must be assigned. In ALGOL 68, this is written GRADES [1].

GRADES [1] is the single number 95; it may be printed or used in calculations just like a single variable. The construction [1] may be viewed as a prepositional phrase, the brackets being the preposition, and the 1, its object. The preposition [ ] shows the relationship between the two nouns GRADES and 1. Interestingly, the way GRADES [1] is read aloud reflects this structure: "GRADES sub [meaning subscripted by] one."

Just as a noun cannot communicate much without verbs, a variable is useless without the verbs of programming languages, *operators* and *functions*. Operators are the symbols used in mathematics and programming languages to represent arithmetic and other operations. Thus, +, −, and * (multiplication) are all operators. In conventional notation, operators are placed between their operands (X+Y) if there are two, or in front of them (−X) if there is one.

Functions, on the other hand, precede and enclose their operands. For example, the function SQRT(X) in FORTRAN computes the square root of X. A function can have more than one operand. An example of this is the function MAX(X1, X2, X3, . . .), which selects the largest of its indefinitely many operands. The distinction between functions and operators is fundamentally one of notation; operators will be used in the examples presented here.

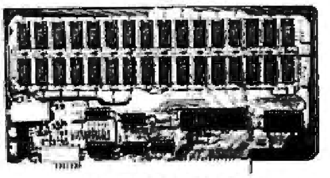
Operators change their actions depending on the data types of their operands. For instance, there are differences in the accuracy of addition of real operands and of integer operands, while addition of string operands is actually concatenation (eg: "John"+" Smith" yields "John Smith"). In general, ALGOL 68 actually allows total redefinition of operators based on the data types of their operands.

Operators can also change their actions depending on the structure of their operands. To use an operator with arrays and inhomogeneous structures, ALGOL 68 *requires* prior definition of the operator's actions, which allows a great deal of flexibility. In contrast to ALGOL 68, the APL language provides definitions such as "the addition of two arrays is the addition of their corresponding elements"; the programmer cannot redefine operators in APL. The PL/I language has a different solution; to add correspondingly named elements in two inhomogeneously structured variables, A and B, one uses:

```
C=A+B,BY NAME;
```

The keyword BY NAME functions as an adverb, modifying the + operator.

APL, in addition to functions (such as + and −, which most languages call operators) which act as simple verbs, also has operators, which act as *auxiliary* verbs. These operators (again, note the special meaning in APL) modify the results of regular functions in a systematic way. For example, + is the familiar addition function. Applied to two vectors, it yields the sum of corresponding elements (eg: 3 4 5 + 6 8 9 produces 9 12 14). The reduction operator, /, is an auxiliary verb. Juxtaposed, as +/, these



two form a new function, "plus-reduction," that operates on a single vector and produces the sum of its elements (eg: +/3 4 5 yields 12). The +/ function *reduces* its operand to a single number by addition.

These complex verbs, nouns, adjectives, adverbs, pronouns, and prepositions all fit into equally complex syntactic structures. As with English, there is a range of syntactic complexity; some languages, such as BASIC, have a very simple set of syntactic patterns. Other languages encompass some very complex and powerful syntactic structures.

Probably the simplest syntactic form is that of many BASIC statements, which may be characterized as:

imperative-verb object

Examples of this form are PRINT X, INPUT Y, and GOTO 200. The object may also be a verbal phrase, as in PRINT X+Y, in which the verb in the verbal is the + operator.

A few forms of greater complexity are found in BASIC. One of these is the IF-THEN statement, an example of which is:

```
IF X=3 THEN PRINT
   "X IS EQUAL TO 3."
```

This is a more complex form than the first for two reasons. First, it uses a conjunction-conjunctive adjective pair, IF and THEN; second, the phrase following THEN can be any BASIC statement. This makes the IF-THEN statement, in the terminology of English grammar, a complex sentence.

Syntactic patterns much more complex than these are found in ALGOL 60 and 68. An example from ALGOL 60 is the statement:

```
X:=2+(IF Y=1 THEN 3
      ELSE 6)
```

This statement assigns to X the value 5 (2+3) if Y is equal to 1, and the value 8 (2+6) if Y is not equal to 1. An IF-THEN-ELSE clause may be used wherever a noun (ie: numerical or character value) is required by the syntax of ALGOL 60. This freedom is restrictive compared to the rules of ALGOL 68; there, not only IF-THEN-ELSE statements can be used as clauses in place of nouns, but *any* valid statement can be so used.

Statements and phrases may be combined in ways such as:

```
k:=(INT i; read(i); i+1)
```

This statement declares the variable i to be of type INT, accepts a value for i as input from some device (possibly a computer terminal), calculates the value of i+1, and finally assigns this value to the variable k. One of the most impressive aspects of ALGOL 68 is that the labyrinthine syntax of the entire language is rigorously defined using a formal notation.

INT	integer
REAL	rational number [it may have a fractional component]
CHAR	character [a single character only]
STRING	string of characters [text string]

Table 1: *Data types which may be assigned to variables in the ALGOL 68 language.*

As has been implicit in the above discussion, the meaning of a statement (English or programming language) is often determined by the meaning of the individual words (such as *grin* or PRINT) and the syntactic operations which combine them. This is made light of by Lewis Carroll in his poem "Jabberwocky," which begins:

'Twas brillig, and the slithy toves
Did gyre and gimble in the wabe:
All mimsy were the borogoves,
And the mome raths outgrabe.

This verse is amusing because we understand the syntax, while the words, though suggestive, are meaningless.

In the realm of more standard language, there are constructions whose meaning is not simply a composition of individual word meanings. Such expressions are called idioms. A sentence like *The FBI kept tabs on Bill's unicorn* has nothing to do with actually sticking plastic tabs on a unicorn. And thinking about *The cat got his tongue* in such literal terms would lead to an anxiety attack.

In programming languages, too, there are idioms. In APL, there are the constructions →, →0, and →(null vector), all of which are idioms for special types of program branching. In ALGOL 68, there are operators such as +=: (plus and becomes). A+=:1 is equivalent to A=:A+1, and instructs the computer to take the value of A, add 1 to it, and store the result back into A. These are truly idioms, as their meanings cannot be derived directly from the meanings of their individual elements.

Good examples of expletives may be found in both ALGOL 68 and FORTRAN. In ALGOL 68, the SKIP statement is an expletive; it does nothing and is explicitly undefined. A similar example in FORTRAN is the CONTINUE statement, the execution of which also has no effect. In practice, CONTINUE is used in only one particular context, while SKIP is used in many different contexts.

While idioms, expletives, and syntax in general reveal the similarity between programming languages and natural languages on the level of the word and the sentence, there are also similarities on the level of the *paragraph* and the *document*. The paragraph in ALGOL 60 is the *block*, which is a sequence of statements beginning with BEGIN and variable declarations (REAL, INTEGER, etc), and ending with END. This is similar to a paragraph of English in several ways. It has a clearly marked beginning and end. It is required to state at the beginning the objects (variables) it will be working with, just as a good paragraph should declare its subject at the beginning. Finally, a good block deals with only one phase of the problem being solved by the program, just as a paragraph should deal with only one aspect of the idea being discussed.

The analogy between programming languages and natural languages at the level of whole documents is seen by comparing computer programs with books. Both usually have titles; some programming languages—APL and Pascal—actually require them. Many books have a dust-jacket blurb or preface to make the book easier to read and use. Good computer programs have comments written into the code for the same purpose.

You may be surprised to find paragraphs, idioms, expletives, and so forth in programming languages, if you have thought of them only as characteristics of natural language. Throughout this discussion, however, we have seen how closely programming languages parallel natural languages. Therefore, the existence of idioms and similar attributes in programming languages is a nearly predictable situation.

Importance of Similarity

Granting that programming languages are languages in the same sense as English or Mandarin, the question that follows is: does this make any difference to working programmers? Yes, it makes a great deal of difference, for it leads to the concept of programming style, with associated benefits.

The concept of programming style follows naturally. Just as English is a tool for which there are different uses and styles, so too are programming languages tools for which there are different uses and styles. Further, just as in English there are some writing styles that are superbly clear and efficient, while others are not, there are some programming styles that are more desirable than others. *Aesthetic* considerations indicate that a desirable style is a clear and concise one. But why should this interest the working programmer, who is just interested in doing a job, not in creating a work of art?

Too many programs are written today without consideration for later revisions that may be necessary. It is as though these programs will never be read or changed. The inevitable result of such a programming practice is programs that *do* need to be patched, altered, and debugged to make them work, and programs that are so incomprehensible that they can be changed to meet future requirements only with great difficulty. Worse, the result may be a program that works 99 times out of 100. On that hundredth time, the program may fail and produce incorrect results that are accepted as true. Or perhaps it will be obvious, as bank accounts are jumbled, an oil refinery burns, or a spacecraft explodes upon launch, that something is indeed amiss with the computer programs in use.

Working programs, programs that can be confidently (and even mathematically) labeled correct, are serious business in a society in which computers are performing more and more functions of ever greater importance. For this and other reasons related to the costs of debugging a poorly written program, structured programming (which advocates a clear and systematic approach to programming) has become popular.

Many programmers still do not write programs that work correctly the first time. There is still much to be done before good programming is nearly universal. However, better programming languages are being developed, more programmers are developing a clear and functional programming style, and more programs work the first time. ■

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3. Ledgard, H F. *Programming Proverbs.* Rochelle Park NJ: Hayden Book Co, 1975.
4. Naur, P (editor). "Revised Report on the Algorithmic Language ALGOL 60." *Communications of the ACM*, January 1963, pages 1 thru 17.

Event Queue

March 1981

March

Fairchild Education Center Courses, South San Jose CA. Bit-slice techniques, the 3870 microprocessor, and programming in Pascal are the courses offered by Fairchild during March. For details, contact Dr Dennis Lunder, Fairchild Education Center, M/S 43-4022, 133 Bernal Rd, South San Jose CA 95119, (408) 224-7095.

March-April

Courses from George Washington University, Washington DC. George Washington University has schedules and descriptions of many courses in computers and communications. For your copy, contact the Director, Continuing Engineering Education, George Washington University, Washington DC 20052, (800) 424-9773; in Washington DC (202) 676-6106.

March-September

Seminars from WPI, Worcester Polytechnic Institute, Worcester MA. A series of 2-day seminars covering data communications, microprocessors, and other topics of interest to data-processing professionals is offered by WPI. For a detailed brochure, write to the Office of Continuing Education, Worcester Polytechnic Institute, Worcester MA 01609, (617) 753-1411, attn: Ms Ginny Bazarian.

March-November

Advanced Data Processing Workshops, Deltak Inc, various cities throughout the US and Canada. These 5-day workshops are aimed at data-processing training managers responsible for the management and administration of data-processing training and involved in planning, monitoring, evaluating, and reporting to upper management on the status of the training. For a schedule of dates and locations, contact Deltak Inc, 1220 Kensington Rd, Oak Brook IL 60521, (312) 920-0700.

March 8-11

TI-MIX 1981, Marriott Hotel, New Orleans LA. This is a conference for Texas Instruments equipment users. Thirty-six sessions consisting of individual presentations, panel discussions, and workshops are planned. Two exhibit rooms featuring the latest computer equipment from Texas Instruments will be open. Contact TI-MIX, M/S 2200, POB 2909, Austin TX 78769, (512) 250-7151.

March 11-13

Business- and Personal-Computer Sales and Exposition and New York Business Show, Madison Square Garden, New York NY. For details, contact Produx 2000 Inc, POB 2000, Bala-Cynwyd PA 19004, (215) 457-2300.

March 14

The Fourth Annual PACS Computer Games Festival, LaSalle College Ballroom, Philadelphia PA. This event is sponsored by PACS

(Philadelphia Area Computer Society) and the LaSalle College Physics Department. Presentations on computer-aided learning will be featured. Contact Stephen A Longo, Physics Department, LaSalle College, Philadelphia PA 19141, (215) 951-1255.

March 17-20
The Fourteenth Annual Simulation Symposium, Tampa FL. Papers describing digital discrete simulation and other techniques will be read. This symposium is a forum for the exchange of ideas and techniques in computer simulation. Contact Annual Simulation Symposium, POB 22621, Tampa FL 33622.

March 20
Digital Computer Association Annual Meeting, Pacifica Hotel, 6161 Centinela Blvd, Culver City CA. Cocktails, dinner, and the annual meeting are the features of this gathering. For more information, contact Mary Rich, 731 Bayonne St, El Segundo CA 90245.

March 23-25
Office Automation Conference, Albert Thomas Convention Center, Houston TX. This conference presents seminars on the concepts and the methods behind the latest office technologies and an exhibition of office equipment. Contact Office Automation Conference, POB 9659, Arlington VA 22209, (703) 558-3617.

March 24-27
Printemps Informatique, Palais des Congres, Paris, France. This is an electronic data-processing exhibition for computer OEMs (original equipment manufacturers). Additional information is available from Kallman Associates, 30 Journal Sq, Jersey City NJ 07306, (201) 653-3304.

March 24-26
The Southwest Semiconductor Exposition, Phoenix Civic Plaza Convention Center, Phoenix AZ. More than 140 equipment and materials makers will exhibit semiconductor, hybrid, and printed-circuit board production, processing, and test equipment. Contact Cartlidge & Associates Inc, 491 Macara Ave, Suite 1014, Sunnyvale CA 94086, (408) 245-6870.

March 31-April 2
Cincinnati Business Show, Cincinnati Convention-Exposition Center, Cincinnati OH. Office equipment and services, including automated systems, communications, computers, telephone systems, word processing, data processing, printing equipment, and other office supplies, will be featured. A program of business seminars is also scheduled. Contact Ray G Nemo, 5679 Creek Rd, Cincinnati OH 45242, (513) 531-5959.

April 1981

April 1-2
Communications in the Twenty-First Century, Philip Morris Operations Center, Richmond VA. This conference focuses on technological advances and their economic, political, social, and psychological implications. Elie Abel, Professor of Communications at Stanford University and Lord Briggs, provost of Worcester Col-

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April 1-3
Assuring Quality in Electronic Data Processing Applications, McCormick Inn Hotel, Chicago IL. The objective of this conference is to explain the methods, tools, and techniques that are valuable in improving the quality of computerized applications. Tutorials cover the areas of quality assurance; managing structured design; and designing, implementing, and enforcing application standards. Contact DPMA Quality Assurance Conference, 12611 Davan Dr, Silver Spring MD 20904, (301) 622-0066.

April 3-5
The Sixth West Coast Computer Faire, Civic Auditorium, San Francisco CA. The Faire, a major personal-computing event, has continually attracted larger and larger numbers of exhibitors and attendees. A full program of talks plus a large display of hardware and software are featured. For more information, contact Computer Faire, 333 Swett Rd, Woodside CA 94062, (415) 851-7075.

April 6-10
Tutorial Week—East, Orlando Marriott Inn, Orlando FL. Tutorials on VLSI (very large-scale integration) and microprocessors and graphics, software-engineering methodology and testing, and distributed computing and networks will be presented. For IEEE members, the cost is $400; for nonmembers, the cost is $475. Contact Tutorial Week—East, POB 639, Silver Spring MD 20901, (301) 439-7007.

April 7-8
Top Secrets '81, Pointe Resort, Phoenix AZ. Honeywell's annual computer security and privacy conference. Many author-

ities in the field of data security will discuss the business and legal impact of the latest incidents in computer crime and abuse. The conference fee is $500. Contact the Security Symposium Registrar, Honeywell Information Systems, M/S T-99-4, POB 6000, Phoenix AZ 85005, (800) 528-5343.

April 7-9
Computerized Office Equipment Expo, O'Hare Exposition Center, Rosemont IL. More than 200 exhibitors will feature their office equipment at this show. Executives and administrators from wholesale, retail, commercial, financial, and industrial establishments are invited, along with the general public. Contact Industrial & Scientific Conference Management Inc, 222 W Adams St, Chicago IL 60606, (312) 263-4866.

April 7-9
Electro/81, New York Coliseum and Sheraton Centre Hotel, New York NY. Electro/81 will feature computers and computer-related equipment, plus seminars on components, devices, and materials; computer communications; memories; office automation; speech; and more. Contact Electronic Conventions Inc, 999 N Sepulveda Blvd, Suite 410, El Segundo CA 90245, (800) 421-6816; in California (213) 772-2965.

April 13-16
The Fifteenth International Symposium on Minicomputers and Microcomputers, MIMI '81, Sheraton Hotel, Mexico City, Mexico. The scope of this symposium covers hardware, software, distributed processor architecture, computer networks, telecommunications, real-time applications, education, and more. Contact Ing. Jorge Gil, Academic Secretary, MIMI Symposium, IIMAS-UNAM, Apartado Postal 20-726, Mexico 20 D F, Mexico.

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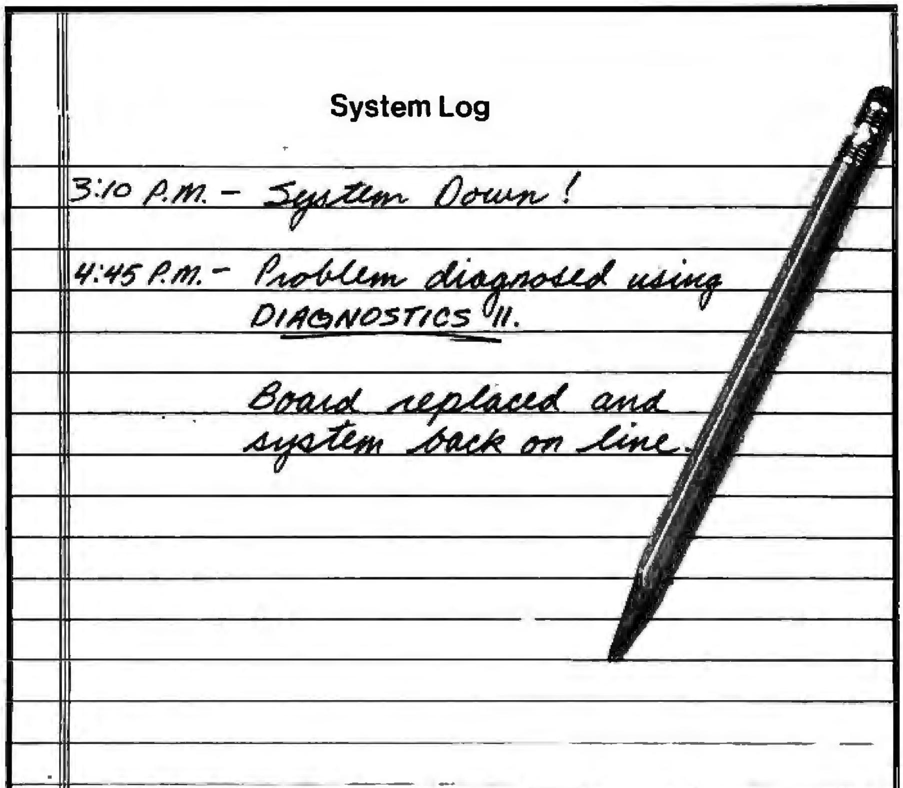

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May 1981

May 2

National Computer Problem-Solving Contest for Junior and Senior High School Students, throughout the US. Small teams of junior and senior high school students will compete for two hours on computer systems to solve five programming problems. Winners will be judged on whether their programs run properly using the test data supplied in the problem, are easy to read, logical, imaginative, and creative.

To receive a copy of the 1981 contest problems, local school directors should contact the University of Wisconsin—Parkside by April 4. Directors must agree to keep the problems confidential until the day of the contest. After that, any organization can use the problems to conduct their own contest. Local contest winners can enter the national and international contest. A national and worldwide ranking will be determined by a team of judges from the University of Wisconsin—Parkside. All interested schools or organizations can share the 1981 contest problems.

For additional information, write Dr Donald T Piele, Associate Professor of Mathematics, University of Wisconsin—Parkside, Kenosha WI 53141.

May 4-7

National Computer Conference, McCormick Pl, Chicago IL. Approximately 90,000 people are expected to attend the National Computer Conference (NCC) this year. The use of robots and artificial intelligence will be among the program sessions at the Personal-Computing Festival during the NCC. For the first time, personal-computing exhibits will join the rest of the conference in the main exhibit area. Over thirty technical sessions will be held. All major companies will be represented. Contact the American Federation of Information Processing Societies Inc, POB 9658, 1815 N Lynn St, Arlington VA 22209, (703) 558-3617.

May 11-13

The Thirty-First Electronic Components Conference, Colony Square Hotel, Atlanta GA. Papers on semiconductor-processing technology, optoelectronic devices, manufacturing technology, materials, hybrid microcircuits, discrete components, interconnections, reliability, and connectors will be read. Contact T G Grau, Bell Laboratories, Whippany Rd, Rm 3B-312, Whippany NJ 07981; or Electronics Industries Association, 2001 Eye St NW, Washington DC 20006.

May 14-16

The Tenth ASIS Mid-Year Meeting, Fort Lewis College, Durango CO. The American Society for Information Science's (ASIS) theme for this meeting is "Using Information." Among the topics to be addressed are user studies, decision making, organizational change, government, education, management, access to information, and designing information systems for use. For information, contact ASIS, 1010 16th St NW, Washington DC 20036, (202) 659-3644.

May 17-20

Expo '81, Loew's Anatole Hotel, Dallas TX. Expo '81 is a combination of exhibits and technical sessions. The exhibits cover everything from graphics systems to industrial computer-control systems. The technical ses-

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4010	.45	4040	.90	4511	.75	74C93	.95
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7417	.37	7495	.60	74191	1.20
7420	.17	7496	.60	74192	.79
7425	.35	74107	35	74193	.79
7426	.33	74121	.35	74194	.85
7427	.35	74122	.39	74195	.65
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74LS08	.38	74LS85	1.23	74LS163	.99	74LS266	.68
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74LS20	.26	74LS109	.49	74LS174	1.19	74LS298	1.24
74LS21	.30	74LS112	.48	74LS175	1.09	74LS352	1.59
74LS22	.34	74LS113	.48	74LS181	2.19	74LS353	1.59
74LS26	.40	74LS114	.55	74LS190	1.15	74LS363	1.39
74LS27	.35	74LS122	.55	74LS191	1.31	74LS365	.99
74LS28	.39	74LS123	.99	74LS192	.88	74LS366	.99
74LS30	.35	74LS125	.99	74LS193	.98	74LS367	.99
74LS32	.39	74LS126	.88	74LS194	1.80	74LS368	.99
74LS33	.54	74LS132	.69	74LS195	1.39	74LS373	1.85
74LS37	.78	74LS136	.58	74LS196	.82	74LS374	1.81
74LS38	.39	74LS138	.79	74LS197	.82	74LS377	1.48
74LS40	.25	74LS139	.79	74LS221	1.28	74LS385	1.90
74LS42	.79	74LS145	1.19	74LS240	1.89	74LS386	.65
74LS47	.78	74LS148	1.39	74LS241	1.89	74LS390	1.90
74LS48	.78	74LS151	.79	74LS242	1.89	74LS393	1.90
74LS51	.35	74LS153	.79	74LS243	1.89	74LS395	1.69
74LS54	.35	74LS154	2.39	74LS244	1.79	74LS670	2.20
74LS55	.32	74LS155	1.19	74LS245	2.89		

8080 SUPPORT

8212	2.75
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2708	450ns	1K × 8	5.95
2716	450ns	2K × 8	10.95
2732	450ns	4K × 8	29.95

PROMS

74S188	(82S23)	OC	32 × 8	4.75
74S287	(82S129)	TS	256 × 4	4.75
74S288	(82S123)	TS	32 × 8	4.75
74S387	(82S126)	OC	256 × 4	5.75
74S471		TS	256 × 8	18.75
74S472	(82S147)	TS	512 × 8	18.75
74S474	(82S141)	TS	512 × 8	19.95
74S570	(82S130)	OC	512 × 4	7.80
74S571	(82S131)	TS	512 × 4	7.80

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5 Position	1.02	8 Position	1.14
6 Position	1.06		

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7812T	.89	7912T	.99
7815T	.99	7915T	1.19
7824T	.99	7924T	1.19
7805K	1.39	7905K	1.49
7812K	1.39	7912K	1.49
78L05	.69	79L05	.79
78L12	.69	79L12	.79
78L15	.69	79L15	..79

IC SOCKETS

8 PIN	10/1.29
14 PIN	10/1.49
16 PIN	10/1.69
18 PIN	10/1.99
20 PIN	10/2.89
22 PIN	10/2.99
24 PIN	10/2.99
28 PIN	10/3.99
40 PIN	10/4.99

LINEAR

LM301V	.34	LM567V	1.29
LM309K	1.49	LM723	.49
LM311V	.64	LM741V	.29
LM317T	2.29	LM747	.79
LM323K	4.95	LM1310	1.90
LM324	.59	LM1414	1.59
LM339	.99	LM1458	.69
LM377	2.29	LM1488	1.39
LM380	1.29	LM1489	1.39
LM555V	.39	LM1800	1.99
LM556	.69	LM1889	2.49
LM565	.99	LM3900	.59
LM566V	1.49	75451V	.39

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BYTE's Bits

Missing References in Circuit Cellar

Three references were inadvertently omitted from Steve Ciarcia's Circuit Cellar article "Electromagnetic Interference" (January 1981 BYTE, page 48). The following books provide additional reading material for those interested in the topic:

1. Ott, Henry W. *Noise Reduction Techniques in Electronic Systems.* New York: John Wiley & Sons, 1976.
2. Jones, R W. *Electric Control Systems.* New York: John Wiley & Sons, 1953.
3. Shadowitz, Albert. *Electromagnetic Field.* New York: McGraw-Hill Book Company, 1974.

Noise Reduction Techniques in Electronic Systems was reviewed by J N Demas in the September 1980 BYTE, page 311. ■

Circle 233 on Inquiry card.

Clubs and Newsletters

Atari Club Newsletter

Each month the *Atari Computer Enthusiasts News* contains news, hints, and assistance for Atari owners and users. Most of the information is supplied by club members, but articles from all interested Atari users are welcomed. Contact the *Atari Computer Enthusiasts,* 3662 Vine Maple Dr, Eugene OR 97405.

TSUNAMI

The Sorcerer Users Newsletter Around Michigan (TSUNAMI) is a free, bimonthly newsletter for Exidy Sorcerer owners. The editorial focus is on advanced applications in a variety of languages. Recent issues have featured a 7-generation per second Life program and a Paper Tiger screen-printer program. Contact Joseph R Power, 124 Cedar St #5, East Lansing MI 48823, (517) 337-1049.

MENTAT

MENTAT is a brand-new publication probing professional and recreational uses of computers, plus fantasy and role-playing designs, games, and simulations. *MENTAT* is an Amateur Press Association member. If you are interested in contributing, send a self-addressed, stamped envelope to Bill Seligman, 667 Rugby Rd, Brooklyn NY 11230.

CPT Users Group Formed

An independent group for CPT word-processing system users has been formed. A quarterly newsletter covering word- and data-processing techniques and applications is published. The newsletter features a programming and problem clearinghouse, application notes, program reviews, a directory of software and support packages, and general-interest items. The group is not affiliated with the CPT Corporation. Contact Larry Matthews, c/o APB Inc, 919 Lindy Ct, Dayton OH 45415, (513) 890-9593.

Boston Computer Update

The *Boston Computer Update* is a bimonthly publication from the Boston Computer Society. It is free when you join the society; membership fees are $15 per year. Articles, news reports, and story ideas are welcomed. Members can place free classified ads for noncommercial items. For further details, contact the society at 3 Center Plz, Boston MA 02108, (617) 227-9178.■

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BYTE's Bits

National Search to Aid the Handicapped Through Personal Computers

Johns Hopkins University has announced a national search for ideas and inventions using personal computers and related technology to assist the handicapped. The National Science Foundation and the Radio Shack Division of the Tandy Corporation are cosponsoring the search.

The competition seeks ideas, devices, methods, and computer programs to help handicapped people overcome learning disabilities, employment difficulties, and barriers that prevent adapting to home and community settings. Categories that can be addressed include computer-based aids for the blind, deaf, and mentally retarded; for individuals with learning disabilities, neurological or neuromuscular conditions; and the orthopedically handicapped. One hundred awards will be made, including a $10,000 grand prize, and other prizes consisting of computer equipment and cash. Proceedings describing the winning entries will be published at the end of the contest. All participants will retain commercial rights to their entries.

Entries are being sought from computer specialists, high school and college students, and from all interested people. Orientation meetings are being scheduled at rehabilitation centers throughout the US to bring together potential inventors, handicapped individuals, and professionals in the habilitation/rehabilitation fields.

Contestants must prepare and submit their entries by June 30, 1981. To obtain additional information and a contest application, BYTE urges you to write to Personal Computing to Aid the Handicapped, Johns Hopkins University, POB 670, Laurel MD 20810, (301) 953-7100.■

Photo 1: *Personal computers can give the handicapped access to everyday activities. Here, a Johns Hopkins engineer demonstrates typing on a computer-aid electronic keyboard activated by a chin controller. The Johns Hopkins National Search for Applications of Personal Computing to Aid the Handicapped hopes to uncover similar applications.*

Computer Music: A Design Tutorial

Thomas P Orlofsky
8 Victoria Dr
Eatontown NJ 07724

The computational power necessary to synthesize high-quality, polyphonic computer music in real time exceeds the resources of the currently available microprocessors. Despite this discouraging observation, I decided early in the fall of 1978 to design a microprocessor-based music synthesizer. My goal was to discover just how successful I would be with a minimum system constructed from readily available parts. My self-imposed design constraints included an avoidance of special-purpose hardwired logic and an intention to stick with a byte-oriented architecture.

I hesitate to call the results of my efforts a music synthesizer. A more honest description might be a program-controlled, digital tone generator. Specifically, the design generates a predetermined sequence of sinusoidal waveforms in the manner of a player piano. A binary musical score or *command program* specifies the pitch and duration of each note. Each instruction in the command program selects between approximately 30,000 possible pitches from 0.1 Hz to 3 kHz, and selects between 255 possible durations from 10 ms to 2.55 seconds. This relatively fine time and frequency resolution permits quite sophisticated melodic articulations such as the slur, glissando, and vibrato. While the design provides memory for 341 notes or rests, this limitation is by no means essential.

About the Author

Tom Orlofsky is an employee of Bell Telephone Laboratories Inc. He works in systems engineering. His hobbies, in addition to application of home computers to music, include tennis, hiking, and skiing.

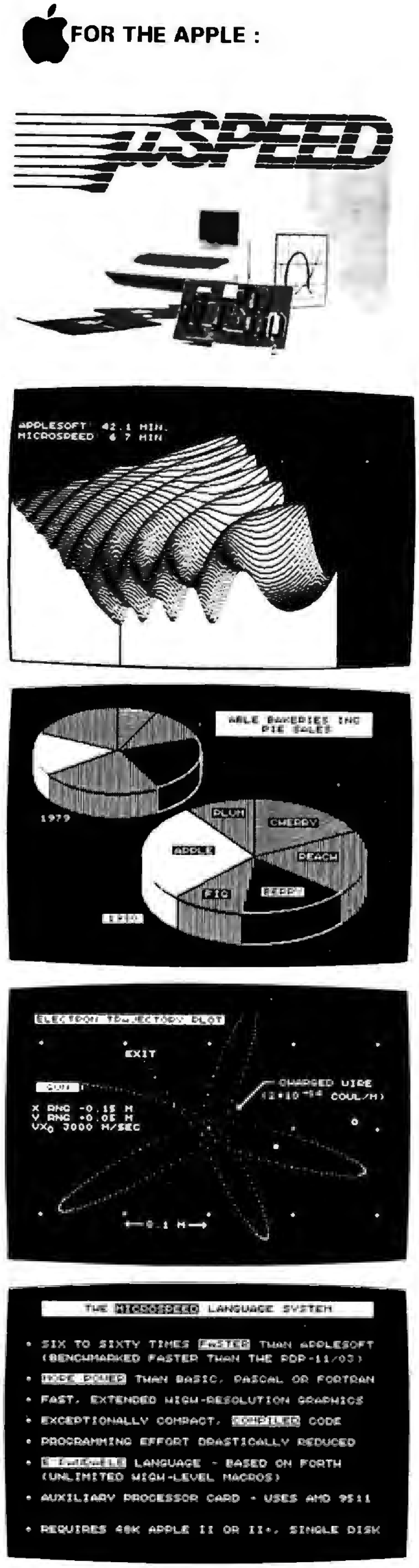
I will begin by discussing the frequency-synthesis method before diving into a more detailed description of the implementation in both hardware and software. Along the way, you will become familiar with the engineering trade-offs inherent in the design of a digital sound system. At the conclusion, some possible improvements and points of departure for your own experiments will be discussed.

Frequency-Synthesis Method

Frequency synthesis is the process of generating an output frequency bearing a mathematical relationship to some reference frequency. Digital synthesis differs from analog synthesis in that the waveform is constructed from a mathematical process rather than from modification of the energy storage of a physical system. Since the digital method is mathematical, the quality of the output signal is theoretically unlimited. In practice, however, the transformation from samples to smoothly changing voltages introduces noise that is independent of the precision of the mathematical calculation.

Figure 1 illustrates the method of digital-frequency synthesis used in the design. A complete sine wave is divided into 256 segments. The average amplitude of each segment is measured with 8-bit precision. These measurements, or *samples*, are stored in consecutive memory locations. Each sample specifies the amplitude of the waveform at a particular phase angle. Consequently, the address of a sample is equivalent to its phase. One way to vary the frequency of the constructed waveform is by varying the rate at which the samples are selected. However, a more practical procedure maintains a constant sampling rate and varies the phase increment between the samples. A larger phase increment has the effect of skipping some of the samples during a pass through the memory.

Observe that the phase of the current sample being selected is formed from the sum of the phase increment and the phase of the previous sample. Only the nine most significant bits of the phase register actually contribute to the address of the current sample. The addition of the phase and phase increment is performed modulo 2^{16}, and the overflow is equivalent to a



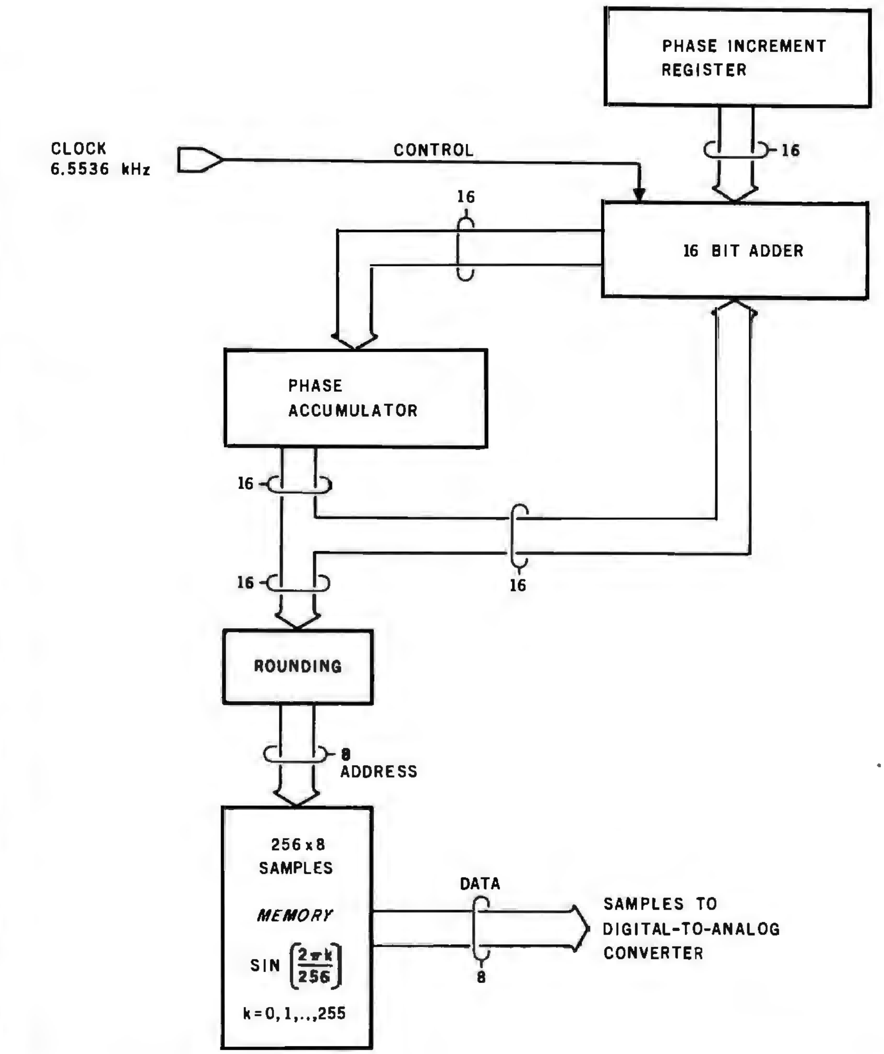


Figure 1: *Conceptual block diagram of the frequency-synthesis method. This scheme will produce one of 32,768 unique frequencies.*

phase shift of -2π.

As an illustrative exercise, assume a phase increment of 256, and that the addition is performed at a rate of 6.5536 kHz. Under these circumstances, the resultant set of addresses will select every sample once per cycle and produce a constructed waveform of frequency equal to (6.5536 kHz / 256) or 25.6 Hz. Now assume a phase increment of 257. In each cycle through the memory, one sample is skipped. However, one particular sample is skipped only once in 257 cycles. This shows that the second phase increment increases the frequency of the constructed waveform in such a way that the second waveform will complete 257 cycles in the time that the first completed 256 cycles. The new frequency is (6.5536 kHz × 257) / (256 × 256) or 25.7 Hz. This particular choice of sampling rate and register size provides a convenient frequency resolution of 0.1 Hz.

It is crucial to observe that the sampling rate is fixed and that the amplitude envelope of the selected samples determines the frequency of the constructed waveform. In other words, the average period of the constructed waveform is not constrained to be an integer multiple of the sampling period. This result of sampling theory follows from the elegant properties of sine waves in the frequency domain. Sampling theory also shows that perfect construction of the sine wave is theoretically possible with as few as two samples per cycle.

Critical Design Considerations

At this point, we judge that the sampling rate is by far the most critical design parameter. Increasing

Text continued on page 320

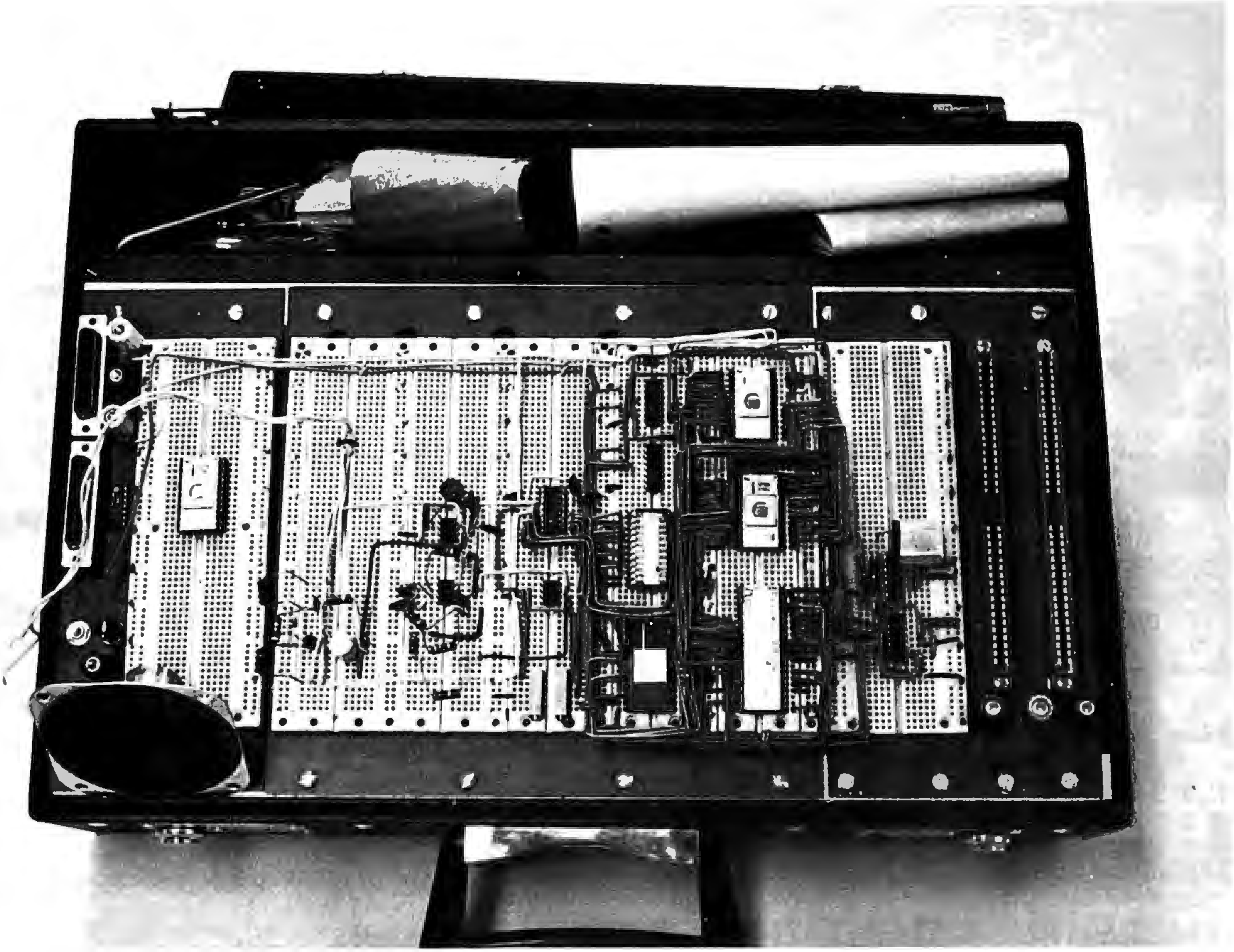


Photo 1: *The author's microprocessor computer music system implemented in a breadboard prototype suitcase. A 2½-inch speaker (lower left) provides audio output for demonstrations. Best results were obtained by patching into the power amplifier of a high-fidelity receiver.*

Text continued from page 318:

the sampling rate increases the audio bandwidth, but the sampling rate is limited by the rate at which the microprocessor system can deliver samples to the output port.

The method of waveform construction adds considerations to the issue of the sampling rate beyond those already mentioned. A digital-to-analog (D/A) converter transforms the samples into discrete voltage levels producing a sine wave with a staircase appearance. A low-pass filter smooths over the discontinuities by removing the so-called sampling harmonics. Unfortunately, a practical filter passes some of the sampling harmonics due to finite attenuation of frequency components in the rejection band. Therefore, the design must sacrifice some of the theoretical bandwidth of the synthesizer to achieve tones that are relatively free of audible distortion. The magnitude of the sacrifice is, of course, a function of your sensitivity to harmonic distortion. If you are to judge harmonic distortion by the advertised specifications of high-fidelity audio equipment, it is quite undesirable.

My choice of sampling at a rate of 6.5536 kHz represents a compromise. On one hand, the 150 microseconds or so of calculation time allows the microprocessor to execute a nontrivial program, yet the audio bandwidth encompasses the range of the fundamental frequency of most musical instruments. However, on the other hand, much of the bandwidth contains audible harmonic distortion.

Another important design consideration concerns the necessary precision and quantity of the stored samples. The difference between the stored value of a sample and the actual value of the sine function evaluated at the same phase introduces an error into the constructed waveform. This disturbance is known as *quantization noise*. The quantization noise associated with 256 8-bit samples has an average power that is about one percent of the average power of the sine wave. Therefore, in this particular design, the noise due to quantization is quite inaudible in comparison with the sampling harmonics that sneak through the filter.

Finally, the design must exhibit sufficient resolution between frequencies. You may have noticed in the illustrative example that the length of the phase accumulator determined the smallest possible frequency increment. Resolution of 0.1 Hz provides the potential of arbitrary tuning. Two tones 0.1 Hz apart in frequency played simultaneously beat together once every 10 seconds. Such mistuning is imperceptible under normal conditions. Another aspect is the granularity of pitch changes during a glissando. While 0.1 Hz might be sufficient for the casual listener, the granularity is audible under close scrutiny. Unfortunately, increased resolution for fixed-register length is purchased with decreased audio bandwidth, and the bandwidth cannot be spared.

Hardware

Now that the problems facing the designer are in perspective, the hardware design will be described so that you may digest the schematic diagram. Figure 2 provides an overview of the system implementation; figure 3 is the schematic diagram. The hardware is functionally divided between the microprocessor system and the analog signal conditioning. In addition to the Z80 processor, the microprocessor system includes 2 K bytes of erasable programmable read-only memory (EPROM) and two input/output (I/O) devices. An 8212 8-bit I/O port, hardwired into a simple output latch, serves as an interface to the D/A converter. A Z80 counter-timer circuit provides interval timing. The system includes no general-purpose programmable memory. The processor and counter-timer circuit serve as depositories for all dynamic information. A simple crystal oscillator generates the system clock signal, and a momentary push button allows the system to be reset. Sufficient device-select logic insures that two devices cannot be simultaneously enabled, regardless of the state of the machine. Finally, the system requires well-regulated external power supplies of +5, +12, and −12 V.

Although the 6 kHz sampling rate is quite demanding from the computational point of view, the rate is quite modest with respect to state-of-the-art conversion speeds. An inexpensive D/A converter such as the MC1408 proves to be quite sufficient. The active low-pass filter is a second-order Butterworth-type with a cutoff

at approximately 3 kHz. If you are interested in maximum tone purity, use a higher-order filter design. The filter output appropriately buffered and attenuated can be patched into the power amplifier section of a typical home audio system. As usual, precautions should be taken to insure signal compatibility. You might want to use a blocking capacitor to trap the DC voltage present in the output during rests.

Software

Now with the hardware out of the way, I can get down to the heart of system design, the software. The software is functionally divided between the *system program* and the *command program*. You can view the system program as a special-purpose operating system that not only performs the frequency synthesis, but also interprets the command program. The command program is essentially a musical score in a form understandable by the system program. Since the command program resides in its own memory device,

Text continued on page 324

Number	Type	+5 V	GND	−12 V	+12 V
IC1	Z80-CPU	11	29		
IC2	Z80-CTC	24	5		
IC3	2708	24	12		19
IC4	2708	24	12		19
IC5	8212	24	12		
IC6	74LS32	14	7		
IC7	74LS74	14	7		
IC8	74LS04	14	7		
IC9	74LS04	14	7		
IC10	MC1408	13	2	3	
IC11	741			4	7
IC12	741			4	7
IC13	741			4	7

Power Wiring Table for Figure 3

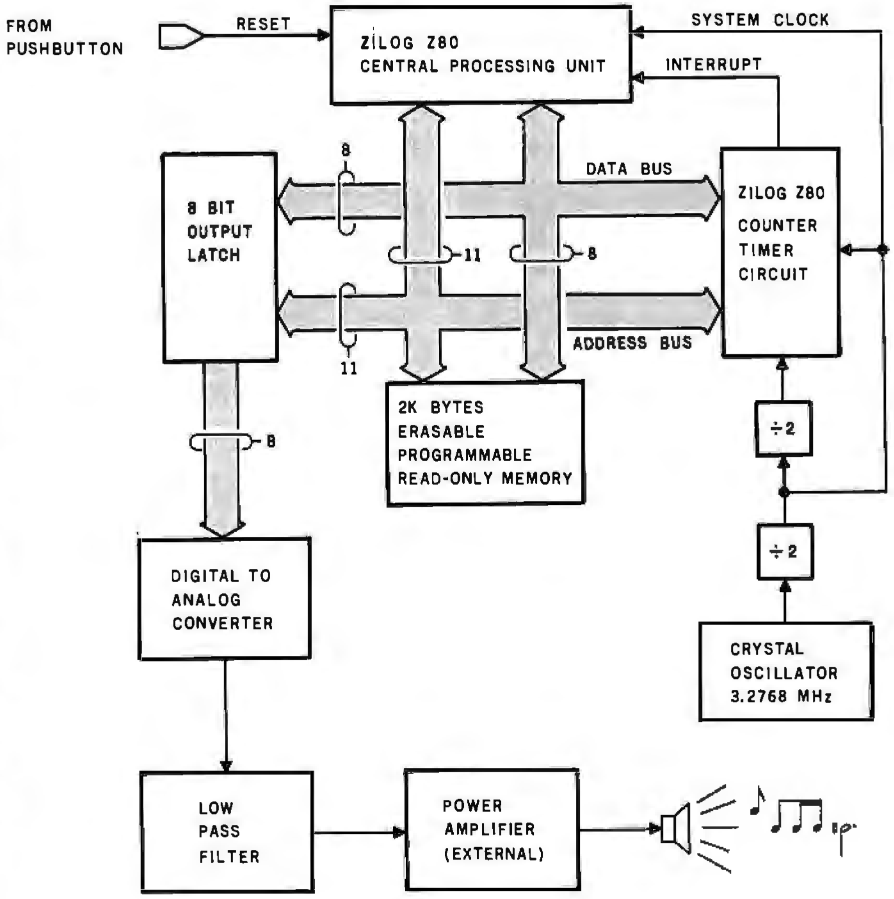


Figure 2: *Functional overview of the hardware organization and signal flow.*

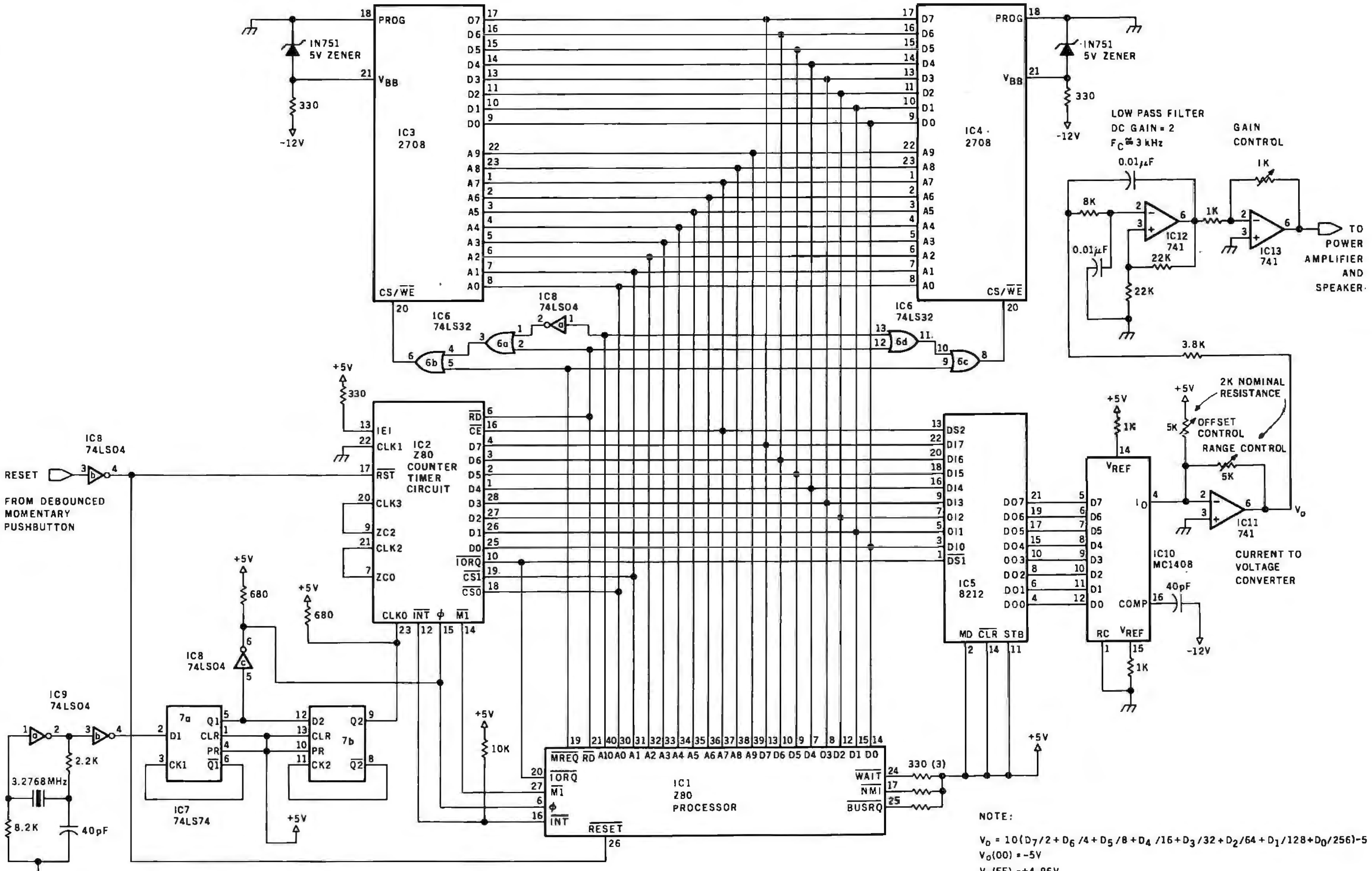


Figure 3: *Schematic diagram for the microprocessor-controlled music system. The design is self-contained except for power and the final audio-output stage. Efficient use of registers within the primary microprocessor eliminates the need for general-purpose memory.*

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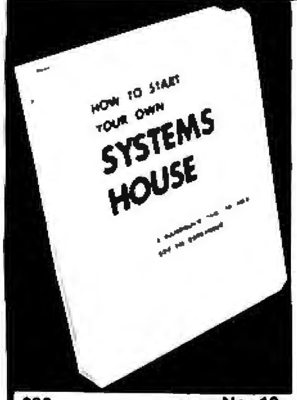

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HOW TO START YOUR OWN SYSTEMS HOUSE
6th edition, March 1980

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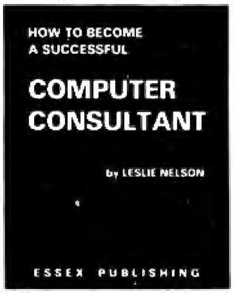

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by Leslie Nelson, 2nd revised edition, Jan 1981

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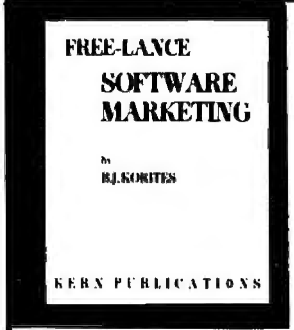

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.		
.		
.		
.		
03FF		
0400	Command Program	IC3
.		
.		
.		
.		
.		
07FF		
08FF		
.		Nonexistent
.		
.		
.		
.		
.		
FFFF		

Table 1: *Memory map for the software of listings 1 and 2.*

Text continued from page 322:

you can play a new song by simply substituting one memory chip for another.

Figure 4 provides the algorithmic flow of the system program. Upon reset, the system program initializes registers within the Z80 processor and counter-timer circuit, reads the first command, calculates the first sample, and halts. The remainder of the program, contained entirely within one interrupt-service routine, executes once per sampling period in response to interrupt requests from the counter-timer circuit. As the samples are generated, the counter-timer circuit clicks them off in a down counter. The processor polls the down counter during every sampling period and branches to the new-tone procedure when the counter reaches zero. The new-tone procedure fetches the next command and updates the registers accordingly. When the new-tone procedure reaches an end of file, it performs an unconditional branch to the beginning of the command program.

Three bytes make up a command. The system program loads the first byte, the note duration, into the down counter within the counter-timer circuit. Bytes 2 and 3 contain the pitch information or phase increment. Observe that a phase increment with a value of zero results in a stream of constant samples, a DC signal or rest.

Hexadecimal Address	Device
00	Counter-Timer
.	Circuit (CTC)
.	
03	
04	
.	
.	Nonexistent
.	
7F	
80	8212 Latch
81	
.	
.	Nonexistent
.	
FF	

Table 2: *I/O port map of the hardware of figure 3.*

In general, the system program completes the sample calculation with time to spare. However, during the command fetch, the processor delays acknowledgment of the next sample interrupt for a fraction of the sampling period. Basically, the processor steals some extra time for housekeeping. Fortunately, the postponement of one sample among thousands is inaudible. If you are familiar with the Z80, then you should have minimal difficulty in deciphering the details of the system program provided in listing 1.

The command program example shown in listing 2 performs the measure of music pictured in figure 5. A macroassembler facilitates generation of the command program. User-defined symbols for notes of the equally tempered scale (see text box) and common note durations eliminate the need to edit numbers. A note macroinstruction, which defines the data structure, reduces each command to a single line of code. The programmer can generate the command program quite efficiently by defining nested macroinstructions that specify repeated rhythms or articulations. Nevertheless, the process is quite tedious.

You may wonder why it is necessary to use sixteen bits to distinguish between twenty-four or so pitch symbols. The answer is that it is not strictly necessary, but immense tonal flexibility can be gained. First of all, you can specify the sliding-note effects mentioned earlier. Second, you are not locked into the equally

Text continued on page 331

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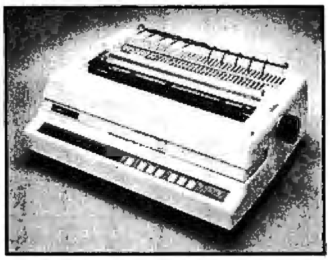

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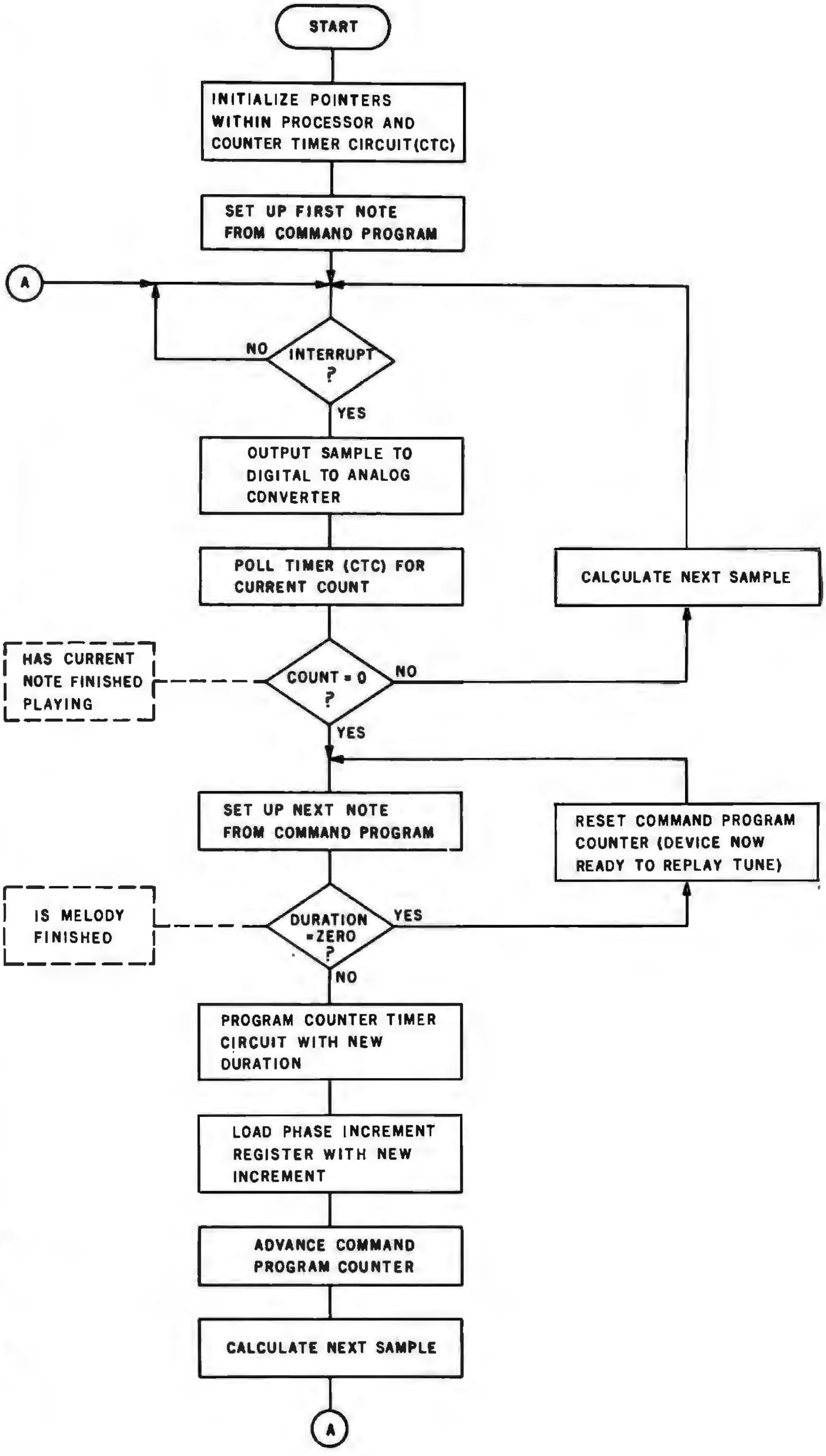

Figure 4: *Flowchart of the system program. The system program, executed in real time, performs the frequency synthesis and interprets the binary musical score contained in the command program.*

Listing 1: *The system program written in Z80 assembly language. See comment lines for details.*

```
                   ;***************************************************
                   ;
                   ;        TONE  SYNTHESIZER                 WRITTEN BY
                   ;        SYSTEM PROGRAM                    TOM ORLOFSKY
                   ;                                          12-8-78
                   ;
                   ;        THIS PROGRAM IS WRITTEN FOR  A Z80 MICRPRO-
                   ;CESSOR SYSTEM CONSISTING OF A Z80-CPU, Z80-CTC,
                   ;2K PROM, 8212 USED AS AN OUTPUT LATCH,  8 BIT DAC,
                   ;AND ANALOG SIGNAL CONDITIONING.  THIS PROGRAM WHICH
                   ;RESIDES  IN THE FIRST 1K OF MEMORY GENERATES
                   ;SINUSOIDAL SAMPLES AT APPROX. 6 KHZ.  THE  PITCH
                   ;AND DURATION OF EACH SINUSIOD OR TONE IS SELECTED BY
                   ;THE COMMAND PROGRAM WHICH RESIDES IN THE SECOND 1K
                   ;OF MEMORY.  THE SYSTEM PROGRAM EXECUTES THE INSTRUC-
                   ;TIONS PROVIDED BY THE COMMAND PROGRAM SEQUENTIALLY.
                   ;        INTERRUPTS FROM CHANNEL 0 OF THE CTC DRIVE
                   ;THE SYSTEM  PROGRAM.  CHANNELS 2 & 3 OF THE CTC
                   ;ARE USED TO TIME TONE DURATION. THE SYSTEM PROGRAM
                   ;POLLS CH3  FOR A TIME OUT CONDITION.
                   ;
                   ;REGISTER USE:
                   ;        HL:     CONTAINS THE PHASE
                   ;        BC:     CONTAINS THE PHASE INCREMENT
                   ;        DE:     CONTAINS THE SAMPLE ADDRESS
                   ;        IX:     COMMAND PROGRAM COUNTER
                   ;        AF':    CONTAINS THE CONTROL  CODE FOR CTC CH3
                   ;        A:      CONTAINS THE NEXT SAMPLE WHEN THE CPU
                   ;                IS HALTED
                   ;CTC CHANNEL USE:
                   ;        CHO:    DETERMINES THE SAMPLING PERIOD
                   ;                (250 T CYCLES)
                   ;        CH2:    DEVIDE BY TEMPO SCALING FACTOR
                   ;        CH3:    TIMES NOTE DURATION  (CLOCKED BY CH2)
                   ;
                   ;
                            LIST    NOGEN    ;SUPPRESS PRINTING OF
                   ;                          MACRO-EXPANSIONS
                   ;***************************************************
                   ;
                   ;                SYMBOL DEFINITION
                   ;
                   ;***************************************************
       (0003)      CH3      EQU     03H      ;ADDRESS OF CTC CH3
       (0002)      CH2      EQU     02H      ;ADDRESS OF CTC CH2
       (0000)      CHO      EQU     OOH      ;ADDRESS OF CTC CHO
       (0000)      BASE     EQU     OH       ;DISPLACEMENT FOR IX REG ADD
       (0080)      DAC      EQU     8OH      ;ADDRESS OF DAC BUFFERED
                   ;                          BY 8212
                   ;***************************************************
                   ;
                   ;                MACRO  DEFINITION
                   ;
                   ;        THE MACRO FACILITATES EDITING THE SAMPLES
                   ;
                   ;***************************************************
                   DATA:    MACRO   #A,#B,#C,#D,#E,#F,#G,#H
                            DB      #A
                            DB      #B
                            DB      #C
                            DB      #D
                            DB      #E
                            DB      #F
                            DB      #G
                            DB      #H
                            MEND
                   ;***************************************************
                   ;
                   ;                INITIALIZATION PROCEDURE
                   ;
                   ;***************************************************
0000                        ORG     OH
0000   210000      INIT:    LD      HL,OH    ;INIT PHASE REGISTER
0003   DD210004             LD      IX,400H  ;INIT COMMAND PROGRAM COUNTER
0007   3E01                 LD      A,1H     ;INIT INTERRUPT REGISTER
0009   ED47                 LD      I,A
000B   3E00                 LD      A,OH     ;LOAD CTC INTERRUPT VECTOR
000D   D300                 OUT     CHO,A
000F   ED5E                 IM2              ;INTERRUPT MODE 2
0011   310002               LD      SP,0200H;INIT SP TO FAKE STAK
0014   3E57                 LD      A,57H    ;INIT CTC CHANNEL 3
```

Listing 1 continued on page 328

Listing 1 continued:

```
                ;                 ***CONTROL WORD DESCRIPTION***
                ;                 BIT 7=0 :INTERRUPT DISABLE
                ;                     6=1 :COUNTER MODE
                ;                     5=0 :DON'T CARE
                ;                     4=1 :TRIGGER ON RISING EDGE
                ;                     3=0 :DON'T CARE
                ;                     2=1 :TIME CONSTANT FOLLOWS
                ;                     1=1 :RESET CHANNEL
                ;                     0=1 :CONTROL CHANNEL WRITE
0016  08                  EX      AF,AF'   ;SAVE CONTROL WORD
0017  DD7E00              LD      A,(IX+BASE);FETCH FIRST DURATION
001A  08                  EX      AF,AF'   ;GET CONTROL WORD
001B  D303                OUT     CH3,A    ;OUTPUT CONTROL WORD
001D  08                  EX      AF,AF'   ;SAVE CONTROL WORD
001E  D303                OUT     CH3,A    ;OUTPUT TIME CONSTANT
0020  3E57                LD      A,57H    ;INIT CTC CH2 SAME
                ;                          EXCEPT FOR TIME CONSTANT
0022  D302                OUT     CH2,A    ;OUTPUT CONTROL WORD
0024  3E40                LD      A,64D    ;TEMPO SCALING FACTOR
0026  D302                OUT     CH2,A    ;OUTPUT TIME CONSTANT
0028  DD23                INC     IX       ;INCREMENT COMMAND PC
002A  DD4E00              LD      C,(IX+BASE);INIT PHASE INC REG
002D  DD23                INC     IX       ;INCREMENT COMMAND PC
002F  DD4600              LD      B,(IX+BASE);MOST SIGNIFICANT BYTE
0032  DD23                INC     IX       ;INCREMENT COMMAND PC
0034  110002              LD      DE,200H  ;INIT SAMPLE ADDRESS REG
0037  3ED7                LD      A,0D7H   ;INIT CTC CH0 SAME AS CH3
0039  D300                OUT     CH0,A    ;EXCEPT ENABLE INTERRUPTS
003B  3E7D                LD      A,125D   ;AND DIFFERENT TIME CONSTANT
003D  D300                OUT     CH0,A    ;OUTPUT TIME CONSTANT
003F  1A                  LD      A,(DE)   ;LOAD A WITH FIRST  SAMPLE
0040  FB                  EI               ;ENABLE INTERRUPTS
0041  76        HOLD:     HALT             ;WAIT HERE FOR ALL INTERRUPTS
                ;******************************************************
                ;
                ;                 INTERRUPT SERVICE ROUTINE
                ;
                ;******************************************************
0042                      ORG     100H
0100  0201                DW      INTRPT   ;ADDRESS FOR INDIRECT JUMP
                ;                          TO  INTERRUPT SERVICE ROUTINE
                ;                          THE INTERRUPT VECTOR PRO-
                ;                          VIDED BY THE CTC POINTS HERE
0102  D380      INTRPT:   OUT     DAC,A    ;OUTPUT SAMPLE TO DAC
0104  09                  ADD     HL,BC    ;INCREMENT PHASE REG
                ;                          ROUND OFF UPPER 9 BITS OF
                ;                          PHASE REG TO 8 BITS AND
                ;                          USE THESE AS LOWER 8 BITS
                ;                          OF SAMPLE ADDRESS
0105  5C                  LD      E,H
0106  CB7D                BIT     7,L      ;IF 1 THEN ROUND UP
0108  CA0C01              JP      Z,NEXT   ;IF 0 THEN ROUND DOWN
010B  1C                  INC     E        ;ROUND UP
010C  DB03      NEXT:     IN      A,CH3    ;POLL CTC CHANNEL 3
010E  D601                SUB     A,1H     ;TEST FOR VALUE 1
0110  CA1701              JP      Z,NEW    ;1 MEANS CHANGE TO NEXT TONE
0113  1A                  LD      A,(DE)   ;CONTINUE PRESENT TONE
                ;                          LOAD A WITH NEXT SAMPLE
0114  FB                  EI               ;ENABLE INTERRUPTS
0115  ED4D                RETI             ;RETURN FROM INTERRUPT
                ;***************NEXT TONE PROCEDURE*******************
0117  DD7E00    NEW:      LD      A,(IX+BASE);FETCH NEW DURATION
011A  C600                ADD     A,0H     ;TEST FOR VALUE 0
                ;                          IF ZERO JUMP TO BEGINNING
                ;                          ELSE CONTINUE SONG
011C  C22601    TEST:     JP      NZ,ANOTHR
011F  DD210004            LD      IX,400H  ;COMMAND PROGRAM STARTS 400H
0123  C31701              JP      NEW
0126  08        ANOTHR:   EX      AF,AF'   ;LOAD CTC CH3 WITH NEW DURATION
0127  D303                OUT     CH3,A    ;OUTPUT CONTROL WORD
0129  08                  EX      AF,AF'   ;SAVE CONTROL WORD
012A  D303                OUT     CH3,A    ;OUTPUT NEW TIME CONSTANT
012C  DD23                INC     IX       ;INCREMENT COMMAND PC
                ;                          UPDATE PHASE INCREMENT REG
012E  DD4E00              LD      C,(IX+BASE);FETCH LOWER BYTE
0131  DD23                INC     IX       ;INCREMENT COMMAND PC
0133  DD4600              LD      B,(IX+BASE);FETCH UPPER BYTE
0136  DD23                INC     IX       ;INCREMENT COMMAND PC
0138  1A                  LD      A,(DE)   ;LOAD A WITH NEXT SAMPLE
                ;                          NEW PITCH WILL BECOME
                ;                          EFFECTIVE ON THE NEXT
                ;                          SAMPLE
0139  FB                  EI               ;ENABLE INTERRUPTS
013A  ED4D                RETI             ;RETURN FROM INTERRUPT
                ;******************************************************
                ;
                ;                 DEFINE FAKE STAK
                ;
                ;         SINCE THERE IS NO WRITABLE MEMORY THE CPU
                ;         WILL NOT BE ABLE TO STORE THE RETURN ADDRESS
                ;         OF THE INTERRUPTED INSTRUCTION.  IT MUST BE
                ;         PROVIDED IN READ ONLY MEMORY.
                ;
```

Listing 1 continued:

```
                   ;*****************************************************
013C                       ORG     1FEH
01FE  4100                 DW      HOLD     ;ADDRESS OF THE HALT
                   ;                         INSTRUCTION
                   ;*****************************************************
                   ;
                   ;               SINUSOIDAL SAMPLES
                   ;       256 8 BIT SAMPLES OVER 360 DEGREES
                   ;       PRINTING OF THE OBJECT CODE IS SUPPRESSED
                   ;       NUMBERS ARE LISTED IN DECIMAL.
                   ;
                   ;*****************************************************
0200                       DATA    128D,131D,134D,137D,141D,144D,147D,150D
0208                       DATA    153D,156D,159D,162D,165D,168D,171D,174D
0210                       DATA    177D,180D,183D,186D,188D,191D,194D,196D
0218                       DATA    199D,202D,204D,207D,209D,212D,214D,216D
0220                       DATA    219D,221D,223D,225D,227D,229D,231D,233D
0228                       DATA    234D,236D,238D,239D,241D,242D,244D,245D
0230                       DATA    246D,247D,249D,250D,250D,251D,252D,253D
0238                       DATA    254D,254D,255D,255D,255D,255D,255D,255D
0240                       DATA    255D,255D,255D,255D,255D,255D,255D,254D
0248                       DATA    254D,253D,252D,251D,250D,250D,249D,247D
0250                       DATA    246D,245D,244D,242D,241D,239D,238D,236D
0258                       DATA    234D,233D,231D,229D,227D,225D,223D,221D
0260                       DATA    219D,216D,214D,212D,209D,207D,204D,202D
0268                       DATA    199D,196D,194D,191D,188D,186D,183D,180D
0270                       DATA    177D,174D,171D,168D,165D,162D,159D,156D
0278                       DATA    153D,150D,147D,144D,141D,137D,134D,131D
0280                       DATA    128D,125D,122D,119D,115D,112D,109D,106D
0288                       DATA    103D,100D,097D,094D,091D,088D,085D,082D
0290                       DATA    079D,076D,073D,070D,068D,065D,062D,060D
0298                       DATA    057D,054D,052D,049D,047D,044D,042D,040D
02A0                       DATA    037D,035D,033D,031D,029D,027D,025D,023D
02A8                       DATA    022D,020D,018D,017D,015D,014D,012D,011D
02B0                       DATA    010D,009D,007D,006D,006D,005D,004D,003D
02B8                       DATA    002D,002D,001D,001D,001D,000D,000D,000D
02C0                       DATA    000D,000D,000D,000D,001D,001D,001D,002D
02C8                       DATA    002D,003D,004D,005D,006D,006D,007D,009D
02D0                       DATA    010D,011D,012D,014D,015D,017D,018D,020D
02D8                       DATA    022D,023D,025D,027D,029D,031D,033D,035D
02E0                       DATA    037D,040D,042D,044D,047D,049D,052D,054D
02E8                       DATA    057D,060D,062D,065D,068D,070D,073D,076D
02F0                       DATA    079D,082D,085D,088D,091D,094D,097D,100D
02F8                       DATA    103D,106D,109D,112D,115D,119D,122D,125D

Errors             0
```

Listing 2: *A command program example making use of a macroassembler. The score of this music is given in figure 5.*

```
                   ;****************************************************
                   ;
                   ;       TONE SYNTHESIZER          WRITTEN BY
                   ;       COMMAND PROGRAM           TOM ORLOFSKY
                   ;       EXAMPLE                   12-8-78
                   ;
                   ;       THE COMMAND PROGRAM IS A REPRESENTATION OF
                   ;A  MUSICAL SCORE IN OBJECT CODE EXECUTABLE BY THE
                   ;SYSTEM PROGRAM.  THE FIRST BYTE IS THE NOTE DURA-
                   ;TION AND CAN HAVE VALUE 2H,3H, . . . ,FFH.  THE
                   ;SYSTEM PROGRAM INTERPRETS A ZERO NOTE DURATION AS
                   ;AN UNCONDITIONAL REPEAT.  THE FOLLOWING TWO BYTES
                   ;CONTAIN THE PITCH INFORMATION AND CAN HAVE VALUE
                   ;1H,2H, . . .,800H.  VALUES >800H CAUSE ALIASING
                   ;AND VALUE ZERO CAUSES A DC OUTPUT OR APPARENT
                   ;REST.
                   ;       SYMBOLS FOR TWO OCTAVES OF THE EQUALLY
                   ;TEMPERED SCALE AND COMMON NOTE DURATIONS SIMPLIFY
                   ;THE TRANSLATION PROCESS.  THE NOTE DURATIONS ARE
                   ;SET AT A TEMPO OF APPROXIMATELY 96 QUARTER NOTES
                   ;PER MINUTE.  OTHER NOTE DURATIONS CAN BE CONSTRUCTED
                   ;WITH EXPRESSIONS.  OTHER TEMPOS REQUIRE
                   ;MODIFICATION OF THE TEMPO SCALING FACTOR IN THE
                   ;SYSTEM PROGRAM.
                   ;****************************************************
                   ;
                   ;****************************************************
                   ;
                   ;       SYMBOL DEFINITION
                   ;
                   ;****************************************************
                   ;                         DEFINE NOTE DURATIONS
(0002)             .128    EQU     2D        ;128TH NOTE
(0004)             .64     EQU     4D        ;64TH NOTE
(0008)             .32     EQU     8D        ;32ND NOTE
(0010)             .16     EQU     16D       ;16TH NOTE
(0020)             .8      EQU     32D       ;8TH NOTE
(0040)             .4      EQU     64D       ;QUARTER NOTE
```

Listing 2 continued on page 330

Listing 2 continued:

```
          (0080)        0040 .2       EQU      128D      ;HALF NOTE
          (0100)        0041 .1       EQU      256D      ;WHOLE NOTE
          (0000)        0042 REST     EQU      0D
                        0043 ;                           DEFINE PITCHS
          (0898)        0044 A01      EQU      2200D
          (091B)        0045 AS01     EQU      2331D     ;        FORM XXNN
          (091B)        0046 BF01     EQU      AS01      ;XX=LOCATION OF THE NOTE
          (09A5)        0047 B01      EQU      2469D     ;   WITHIN THE OCTAVE
          (0A38)        0048 C01      EQU      2616D     ;EXAMPLE: AF=A FLAT
          (0AD4)        0049 CS01     EQU      2772D
          (0AD4)        0050 DF01     EQU      CS01      ;NN=LOCATION OF THE OCTAVE
          (0B79)        0051 D01      EQU      2937D     ;EXAMPLE: 0=OCTAVE
          (0C27)        0052 DS01     EQU      3111D     ;CONTAINING MIDDLE C
          (0C27)        0053 EF01     EQU      DS01      ;EXAMPLE: 01=OCTAVE BELOW 0
          (0CE0)        0054 E01      EQU      3296D
          (0DA4)        0055 F01      EQU      3492D     ;CONVERT TO HZ. BY MULTYPLYING
          (0E74)        0056 FS01     EQU      3700D     ;BY 0.1 HZ.
          (0E74)        0057 GF01     EQU      FS01
          (0F50)        0058 G01      EQU      3920D
          (1038)        0059 GS01     EQU      4152D
          (1038)        0060 AF01     EQU      GS01
          (1130)        0061 A0       EQU      4400D
          (1236)        0062 AS0      EQU      4662D
          (1236)        0063 BF0      EQU      AS0
          (134B)        0064 B0       EQU      4939D
          (1471)        0065 C0       EQU      5233D
          (15A8)        0066 CS0      EQU      5544D
          (15A8)        0067 DF0      EQU      CS0
          (16F1)        0068 D0       EQU      5873D
          (184F)        0069 DS0      EQU      6223D
          (184F)        0070 EF0      EQU      DS0
          (19C1)        0071 E0       EQU      6593D
          (1B49)        0072 F0       EQU      6985D
          (1CE8)        0073 FS0      EQU      7400D
          (1CE8)        0074 GF0      EQU      FS0
          (1EA0)        0075 G0       EQU      7840D
          (2072)        0076 GS0      EQU      8306D
          (2072)        0077 AF0      EQU      GS0
                        0079 ;
                        0080 ;**************************************************
                        0081 ;
                        0082 ;                 MACRO  DEFINITION
                        0083 ;
                        0084 ;        MACRO N (NOTE) FACILITATES EDITING OF
                        0085 ;        COMMAND PROGRAMS AND DEFINES THE DATA
                        0086 ;        STRUCTURE
                        0087 ;
                        0088 ;**************************************************
                        0089 N:       MACRO    #TIME,#PITCH
                        0090          DB       #TIME
                        0091          DW       #PITCH
                        0092          MEND
                        0094 ;**************************************************
                        0095 ;
                        0096 ;                 COMMAND  PROGRAM
                        0097 ;
                        0098 ;        TRANSLATION OF THE MEASURE OF FIGURE 5
                        0099 ;
                        0100 ;**************************************************
0000                    0101          ORG      0H
0000                    0102 M1       N        .4,C0
0000      40            0103+         DB       .4
0001      7114          0104+         DW       C0
0003                    0105          N        .64,REST
0003      04            0106+         DB       .64
0004      0000          0107+         DW       REST
0006                    0108          N        .4-.64,C0
0006      3C            0109+         DB       .4-.64
0007      7114          0110+         DW       C0
0009                    0111          N        .64,REST
0009      04            0112+         DB       .64
000A      0000          0113+         DW       REST
000C                    0114          N        .4-.64,C0
000C      3C            0115+         DB       .4-.64
000D      7114          0116+         DW       C0
000F                    0117          N        .8,B0
000F      20            0118+         DB       .8
0010      4B13          0119+         DW       B0
0012                    0120          N        .8,A0
0012      20            0121+         DB       .8
0013      3011          0122+         DW       A0
0015                    0123          N        .8,G01
0015      20            0124+         DB       .8
0016      500F          0125+         DW       G01
0018                    0126          N        .8,F01
0018      20            0127+         DB       .8
0019      A40D          0128+         DW       F01
001B                    0129          N        .4,G01
001B      40            0130+         DB       .4
001C      500F          0131+         DW       G01
001E                    0132          N        .8,REST
001E      20            0133+         DB       .8
001F      0000          0134+         DW       REST
```

Listing 2 continued on page 331

Text continued from page 325:

tempered scale, but can experiment with other scale temperings. It is necessary to choose between the benefits of such flexibility and the value of considerable data compression possible in a table-lookup approach.

Listing 2 continued:

```
0021                  0135      N       .8,C0
0021   20             0136+     DB      .8
0022   7114           0137+     DW      C0
0024                  0138      N       .8,B0
0024   20             0139+     DB      .8
0025   4B13           0140+     DW      B0
0027                  0141      N       .8,C0
0027   20             0142+     DB      .8
0028   7114           0143+     DW      C0
002A   00             0144      DB      0H
002B   (0000)         0145      END

Errors                0
```

System Enhancements

Once you gain confidence in the methods of music synthesis, you may wish to add features or otherwise improve the system. For instance, you may decide to generate a second melodic line, or voice, using the system. Careful analysis of the instruction-execution cycles in the system described in this article show that sufficient computing time is available to generate a second voice.

The second voice may be synthesized along with the first, using the remaining registers in the control microprocessor and counter-timer microprocessor. As the last step in the synthesis, the separate samples should be summed and then scaled by a factor of 0.5.

Control of dynamics (amplitude) of the music is made possible by the addition of a programmable reference voltage for the signal converter. Four bits (a nybble) may be added to each note specification to select between sixteen possible dynamic levels.

If you are satisfied with the single voice, you may decide to improve the command interpreter instead. A good place to start is to add commands such as change tempo, branch conditionally, and halt.

If you are willing to try distributed processing, you can develop a command interpreter of practically unlimited capability. One microprocessor can be dedicated to the task of note synthesis, while another processor can handle the interpretation of commands and note specifications.

In a system that uses distributed processing, the command processor, unencumbered with calculations of samples, has time to execute complex routines during the intervals between processing of commands. A parallel system architecture could enable more exact control over individual waveform samples. For example, a parallel processor could modulate the signal on a sample-by-sample basis, creating attack and decay envelopes or frequency-modulated timbres.

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Figure 5: *One measure that has been translated into the command program example provided in listing 2.*

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processors become available, those of us that synthesize music as a hobby will use them in our circuit designs. And since systems built for hobby use do not have to be compatible with any previous equipment, we are free to use the best ideas currently available. ■

> *Use of equally tempered tuning makes it possible to play music in any diatonic scale on a keyboard instrument without having to change the tuning of the instrument. By international convention, the note A4 (second space on the treble clef) is defined to have the frequency of 440.0 Hz. Since raising a pitch by one octave is the same as doubling the frequency, we can calculate the frequency of A in any octave quite easily by multiplying and dividing by the appropriate power of 2.*
>
> *In equally tempered tuning, the octave is divided into twelve notes; each pair of adjacent notes is separated by an interval called a semitone. The ratio of frequencies between the adjacent notes is equal to the twelfth root of 2, or*
>
> $$f_{k+1} / f_k = 2^{1/12}$$
>
> *Using these relationships, it is easy to calculate the frequency of any arbitrary note.*

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2. Osborne, A, J Kane, R Rector, and S Jacobson, *Z80 Programming for Logic Design*, Osborne/McGraw-Hill, Berkeley CA, 1978.
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4. Tierney, J, C M Rader, and B Gold, "A Digital Frequency Synthesizer," *IEEE Transactions Audio and Electroacoustics*, March 1971, pages 43 thru 57.
5. *Z80-CPU Technical Manual*, Zilog Inc, Cupertino CA, 1977.
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Constellation I: An Astronomy Program

Howard Berenbon, 2681 Peterboro, West Bloomfield MI 48033

Here is an educational program for those interested in astronomy. It displays ten of the most well-known constellations and gives a multiple-choice test to see if you've been paying attention.

Constellation I (see listing 1) is written in BASIC and will run on many computers, including the Radio Shack TRS-80 Model I Levels I and II and SwTPC 6800. It requires roughly 4 K bytes of memory.

Operation

After running the program, you can review the constellations by entering a 1. You can enter a 0 to take the test. If you choose to review the constellations (highly suggested before taking the test), enter another number from 1 thru 10. For each number entry, a constellation will be displayed using asterisks as stars, along with its name (see listing 2). The constellations may be reviewed in or out of sequence and for any length of time.

When you review the tenth constellation, you again have a choice of taking or not taking the test. Enter a 0 if you are ready. Otherwise, you can continue reviewing.

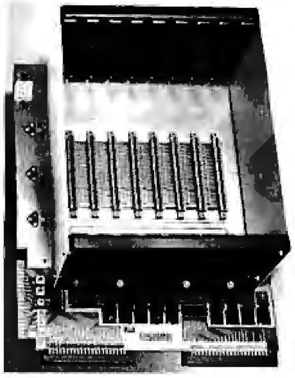
The test consists of ten multiple-choice questions. A constellation is displayed with four possible answers. Enter the number (1 thru 4) of the name that corresponds to the constellation. The program will advance to the

Text continued on page 335

Listing 1: *Constellation I, a program for learning ten constellations. This program requires only 4 K bytes of memory and will run without modification in many BASIC systems.*

```
5 PRINT'CONSTELLATION I'
10 PRINT'COPYRIGHT (C) 1979 BY HOWARD BERENBON'
20 PRINT
30 PRINT'THIS PROGRAM DISPLAYS 10 CONSTELLATIONS AND'
35 PRINT'GIVES A MULTIPLE CHOICE TEST.'
40 PRINT
45 FORI=1TO10
50 A(I)=0
55 NEXTI
100 INPUT'1-REVIEW, 0-TEST';A
110 IFA=0THEN3000
118 PRINT
120 PRINT'ENTER #1-10'
125 INPUTB
130 ONBGOTO2400,2430,2460,2500,2530,2560,2600,2630,2660,2700
200 PRINT'CASSIOPEIA'
220 PRINTTAB(12);'x'
230 PRINTTAB(26);'x'
240 PRINT'     x              x'
250 PRINTTAB(33);'x'
260 RETURN
300 PRINT'LEO'
320 PRINTTAB(30);'x'
330 PRINT'                         x          x'
340 PRINTTAB(23);'x'
350 PRINT'           x                 x'
360 PRINT'   x       x                 x'
370 RETURN
400 PRINT'URSA MAJOR'
415 PRINTTAB(32);'x'
420 PRINT
430 PRINT'      x      x        x            x'
440 PRINT'x                          x'
450 RETURN
500 PRINT'CEPHEUS'
520 PRINTTAB(21);'x'
530 PRINT
540 PRINT'         x'
550 PRINT
560 PRINTTAB(23);'x'
570 PRINT'             x'
580 PRINT
590 PRINT
600 PRINTTAB(24);'x'
610 RETURN
```

Listing 1 continued on page 334

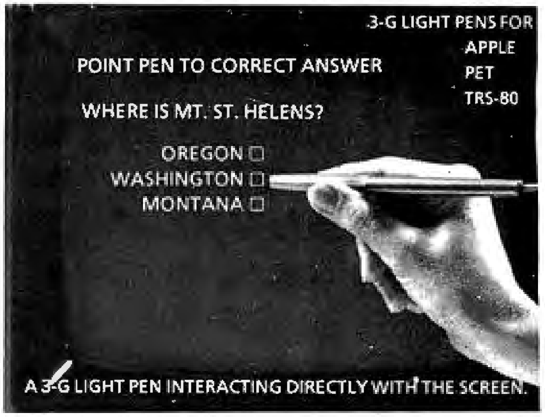


Listing 1 continued:

```
700 PRINT"GEMINI"
720 PRINT"              *        *"
730 PRINT
740 PRINT
750 PRINTTAB(14);"*"
760 PRINT"               *        *"
770 PRINT
780 PRINT"              *          *"
790 PRINT"          *                  *"
795 RETURN
800 PRINT"CORONA BOREALIS"
820 PRINT"                            *"
830 PRINT"               *              *"
840 PRINT"                *           *"
850 PRINT"                   *    *"
860 RETURN
900 PRINT"SAGITTARIUS"
920 PRINT"           *       *"
930 PRINT"                      *         *"
940 PRINTTAB(12);"*"
950 PRINT
960 PRINT"                                     *"
970 PRINT"                                           *"
980 PRINT"                                  *"
990 RETURN
1000 PRINT"LYRA"
1020 PRINT"                        *"
1030 PRINT"                    *"
1040 PRINT"               *"
1060 PRINT
1070 PRINT"                  *"
1080 PRINT"             *"
1090 RETURN
1200 PRINT"AURIGA"
1220 PRINT"                              *"
1230 PRINT"                    *"
1240 PRINT"                                   *"
1250 PRINT
1260 PRINT"              *"
1270 PRINT"                        *"
1280 RETURN
1400 PRINT"CYGNUS"
1420 PRINT"                   *"
1430 PRINT"                               *"
1440 PRINT"                       *"
1450 PRINT"              *"
1470 PRINTTAB(29);"*"
1480 PRINTTAB(32);"*"
1490 PRINTTAB(35);"*"
1500 RETURN
2400 GOSUB200
2410 GOTO118
2430 GOSUB300
2440 GOTO118
2460 GOSUB400
2470 GOTO118
2500 GOSUB500
2510 GOTO118
2530 GOSUB700
2540 GOTO118
2560 GOSUB800
2570 GOTO118
2600 GOSUB900
2610 GOTO118
2630 GOSUB1000
2640 GOTO118
2660 GOSUB1200
2670 GOTO118
2700 GOSUB1400
2710 GOTO100
3000 P=0
3010 PRINT"MULTIPLE CHOICE TEST"
3020 PRINT"ENTER CORRECT ANSWER (#1-4)"
3030 PRINT
3040 PRINT"1)"
3050 GOSUB320
3060 PRINT"(1) LEO"
3070 PRINT"(2) BOOTES"
3080 PRINT"(3) LYRA"
3090 PRINT"(4) LYNX"
3100 GOSUB5050
3110 IFC=1GOSUB5000:A(1)=10
3130 PRINT"2)"
3150 GOSUB520
3170 PRINT"(1) PROCYON"
3180 PRINT"(2) AURIGA"
3190 PRINT"(3) CEPHEUS"
3200 PRINT"(4) ORION"
3210 GOSUB5050
3220 IFC=3GOSUB5000:A(2)=10
3230 PRINT"3)"
3240 GOSUB1220
3260 PRINT"(1) LEO"
3270 PRINT"(2) AURIGA"
3280 PRINT"(3) GEMINI"
3290 PRINT"(4) HYDRA"
3300 GOSUB5050
3310 IFC=2GOSUB5000:A(3)=10
3320 PRINT"4)"
3340 GOSUB720
```

Listing 1 continued:

```
3350 PRINT'(1) LEO'
3360 PRINT'(2) CRUX'
3370 PRINT'(3) CANOPUS'
3380 PRINT'(4) GEMINI'
3390 GOSUB5050
3400 IFC=4GOSUB5000:A(4)=10
3410 PRINT'5)'
3420 GOSUB220
3440 PRINT'(1) AURIGA'
3450 PRINT'(2) LYNX'
3460 PRINT'(3) CASSIOPEIA'
3470 PRINT'(4) LYRA'
3480 GOSUB5050
3490 IFC=3GOSUB5000:A(5)=10
3500 PRINT'6)'
3510 GOSUB820
3520 PRINT'(1) LEO'
3540 PRINT'(2) CYGNUS'
3560 PRINT'(3) CORONA BOREALIS'
3570 PRINT'(4) CEPHEUS'
3580 GOSUB5050
3590 IFC=3GOSUB5000:A(6)=10
3600 PRINT'7)'
3610 GOSUB1020
3620 PRINT'(1) LYRA'
3640 PRINT'(2) LEO'
3650 PRINT'(3) ORION'
3660 PRINT'(4) CETUS'
3670 GOSUB5050
3680 IFC=1GOSUB5000:A(7)=10
3700 PRINT'8)'
3710 GOSUB920
3720 PRINT'(1) CRUX'
3740 PRINT'(2) CETUS'
3750 PRINT'(3) DRACO'
3760 PRINT'(4) SAGITTARIUS'
3770 GOSUB5050
3780 IFC=4GOSUB5000:A(8)=10
3800 PRINT'9)'
3810 GOSUB415
3820 PRINT'(1) LYRA'
3840 PRINT'(2) URSA MAJOR'
3850 PRINT'(3) CRUX'
3860 PRINT'(4) VIRGO'
3870 GOSUB5050
3880 IFC=2GOSUB5000:A(9)=10
3900 PRINT'10)'
3910 GOSUB1420
3920 PRINT'(1) CYGNUS'
3930 PRINT'(2) LEPUS'
3940 PRINT'(3) PERSEUS'
3950 PRINT'(4) TAURUS'
3960 GOSUB5050
3970 IFC=1GOSUB5000:A(10)=10
3980 PRINT
3985 PRINT'POINTS PER QUESTION'
3990 PRINT
4000 PRINT'1=";A(1);"  2=";A(2);"  3=";A(3);"  4=";A(4);"  5=";A(5)
4010 PRINT"6=";A(6);"  7=";A(7);"  8=";A(8);"  9=";A(9);"  10=";A(10)
4020 PRINT
4030 PRINT'SCORE IS %";P
4040 END
5000 P=P+10
5005 PRINT'CORRECT'
5010 RETURN
5050 INPUT"(1-4)";C
5060 RETURN
```



Listing 2: *A sample run of Constellation I showing the review phase.*

```
1
CASSIOPEIA
            *
                           *
     *              *
                                  *

ENTER #1-10
?


2
LEO
                               *
                         *          *
                        *
            *                *
   *        *                *

ENTER #1-10
?


10
CYGNUS
                    *
                                *
                        *
               *
                              *
                                 *
                                    *
1-REVIEW, 0-TEST?
```

Listing 3: *Part of the ten-question test given by Constellation I. The bottom part of the listing shows the points for each question and the final score.*

```
1-REVIEW, 0-TEST? 0
MULTIPLE CHOICE TEST
ENTER CORRECT ANSWER (#1-4)

1)
                               *
                         *          *
                        *
           *                 *
   *       *                 *
(1) LEO
(2) BOOTES
(3) LYRA
(4) LYNX
(1-4)? 1






POINTS PER QUESTION

1= 10    2= 10    3= 10    4= 10    5= 10
6= 10    7= 10    8= 10    9= 10    10= 10
SCORE IS % 100
READY
>
```

Text continued from page 333:

next question. After all questions are answered, a list of points per question is displayed along with your percent score (see listing 3).

You'll be surprised how much you have learned about the constellations. Next time you are stargazing, keep an eye out for Cassiopeia (it's near Andromeda). You won't have trouble recognizing it, if you have been doing your homework.■

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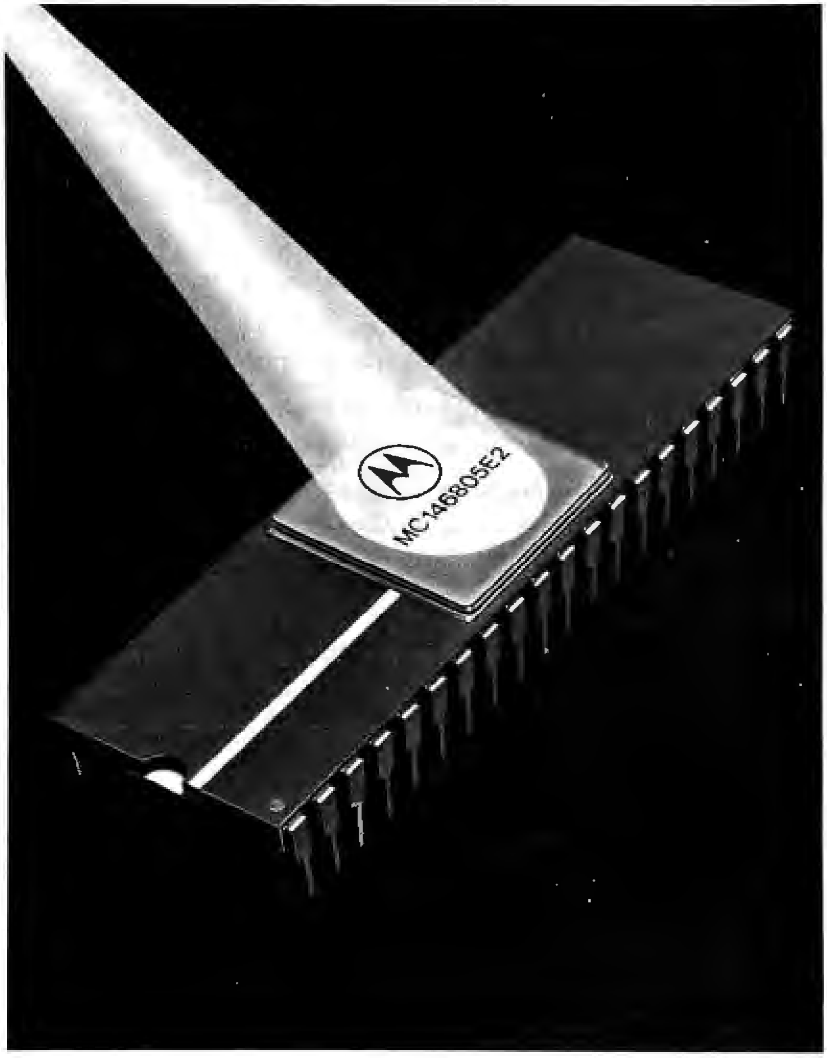
SYSTEMS

CMOS Processor from Motorola



The MC146805E2 is an 8-bit CMOS microprocessor with a set of 61 instructions similar to the MC6800's. There's a set of bit-manipulation instructions to allow any bit in programmable memory or any I/O (input/output) line to be set or cleared with a single instruction. The device requires only 20 mW at 1 MHz and less than 1 mW in the standby mode. The supply-voltage range is 3 to 6 V DC. The unit includes an 8-bit timer with a software-programmable 7-bit prescaler, 112 bytes of programmable memory, and a clock generator. The multiplexed bus has an 8 K-byte addressing range. A 2 K-byte CMOS ROM is available. The processor is priced at $45 in unit quantities. Contact Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin TX 78721.

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8088-Based Board for the S-100

The CP88 is a 5 MHz 8088-based microprocessor board designed for the S-100-bus system. It features 1-megabyte address space, 64 K I/O addresses, an instruction set with full 16-bit mathematics and extensive string-handling capabilities, a 3 K-byte EPROM, provision for 1 K bytes of programmable memory, memory addressing in the top 4 K bytes of address space, and the ability to disable memory space. The memory-access time is 450 ns. The CP88 has switch-selectable 5 to 8 MHz clock rates and spare sockets for breadboarding. The CP88 is available as a bare board only. It comes with documentation for $59.95 from Microfuture, POB 5951, San Jose CA 95150, (408) 249-0560.

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DTC's Microcomputer

The DTC Micro 210 contains 64 K bytes of programmable memory, a 2 K phantom ROM (read-only memory), an 8085A-2 microprocessor, and four RS-232C asynchronous interface ports. The unit employs two BASF 5-inch floppy-disk drives having 300 K bytes of storage. The operating systems available with the Micro 210 are compatible with DTC's other microcomputers. Single- and multiuser systems are available. Applications software can be written under CP/M, DTC's Multi-User Business BASIC, or DTC's version of Microsoft BASIC. The price for the Micro 210 is $3295 from DTC, 590 Division St, Campbell CA 95008, (408) 378-1112.

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Where Do New Products Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. The information is printed more or less as a first-in first-out queue, subject to occasional priority modifications. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

What's New?

PERIPHERALS

Music Filter

The Music Sweetener is a low-pass filter designed to enhance Software Affair's Orchestra-80 and other commercial and homebrew D/A (digital-to-analog) converter music synthesizers that do not already have a filter. The unit attenuates the unwanted high-frequency sampling noise better than a stereo system's treble tone control. It is designed for use in four-part music synthesis on most microcomputers. The device is inserted between the music peripheral and the audio amplifier. The Music Sweetener is $39.95, plus $2 shipping, from Newtech Computer Systems Inc, 230 Clinton St, Brooklyn NY 11201, (212) 625-6220.

Circle 403 on inquiry card

Apple II Printer

IMP2-Apple is an impact printer designed for the Apple II. It provides lowercase characters, single-command printer functions, and is compatible with the Pascal operating system. Priced at $895, the printer is equipped with friction and tractor feed to handle single sheets, roll paper, and fanfold forms. The unit can print 80, 96, or 132 columns at 1 line per second. The 7 by 7 dot matrix has a standard 96-character ASCII (American Standard Code for Information Interchange) set; special character sets are optional. IMP2-Apple can handle user-defined and high-resolution graphics under software control. Contact Axiom Corporation, 5932 San Fernando Rd, Glendale CA 91202, (213) 245-9244.

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Vision for Your Microcomputer

Microtex Corporation has developed an image-processing subsystem that allows microprocessors to be used in the gray-scale data acquisition from Reticon line-scan and matrix cameras. The Microtex 6400 device acquires 8-bit (256 gray level) data at 1 or 2.5 MHz, and provides all power, control, and clock signals to the Reticon camera. A board designed for the Digital Equipment Corporation LSI-11 family of microprocessors, the 6400-A has a general-purpose interface for use with many other 16-bit microprocessors. An optional video processor will allow the user to see real-time data from the 256 by 256 matrix camera at approximately 30 frames per second.

The basic 6400 system includes the camera-control logic, an external synchronization input that initiates the scan, an 8-bit A/D (analog-to-digital) converter, 64 K bytes of programmable memory, and the Q-bus interface, which contains all the registers for software control of the subsystem. The 6400-A costs $4595 for the 1 MHz version and $4895 for the 2.5 MHz version. For more information, contact Microtex Corporation 80 Trowbridge St, Cambridge MA 02138, (617) 491-2874.

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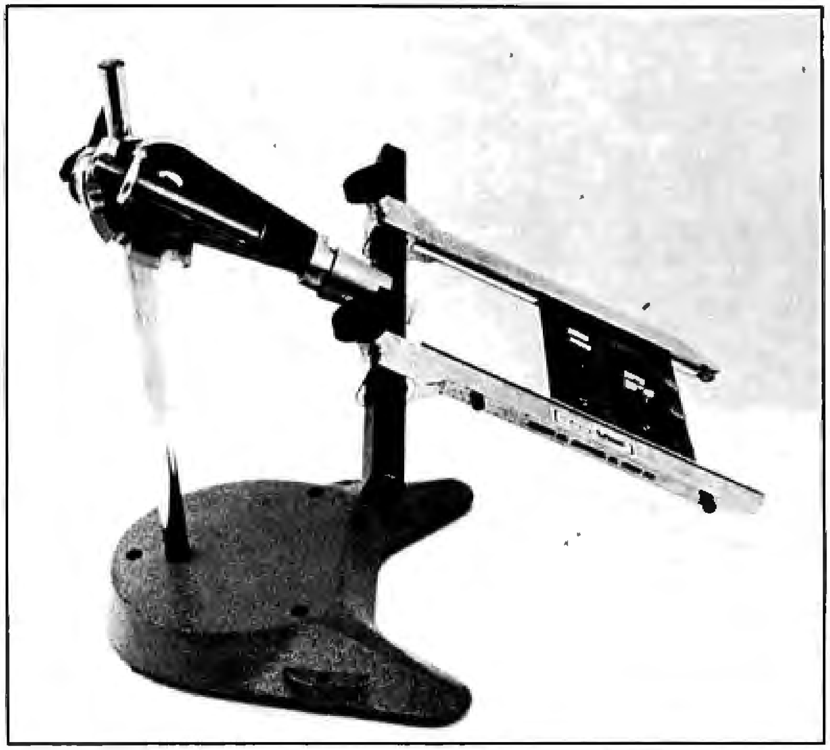

Circuit-Board Holder

The Model 333 circuit-board holder from PanaVise Products Inc features an 8-position rotating adjustment, indexing at 45° increments, and 6 lock positions in the vertical plane, allowing a 10-inch height adjustment. With cross-bars available up to 30 inches in length, the holder can support circuit boards up to 28 inches wide. Extra arms can be added. It is built onto a pre-drilled cast-iron base for stability and easy mounting. Contact PanaVise Products Inc, 2850 E 29th St, Long Beach CA 90806, (213) 595-7621.

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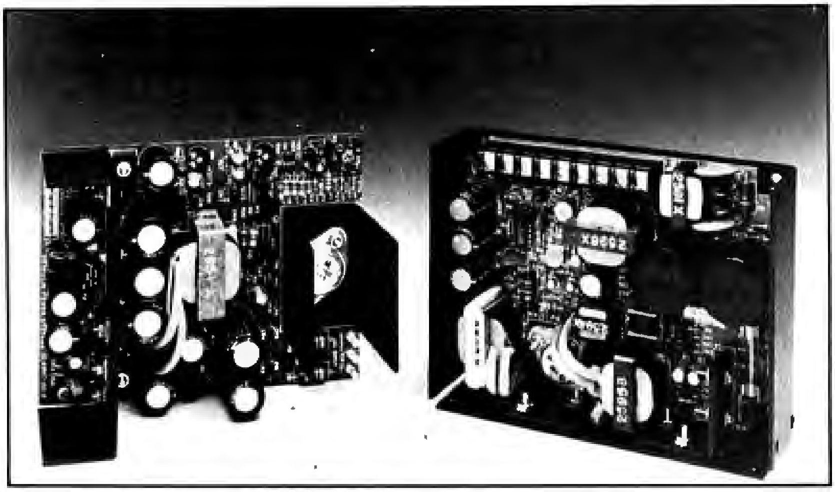
What's New?

PERIPHERALS

40 and 60 W Switching DC Power Supplies



Sierracin/Power Systems has developed a series of 40 and 60 W open-frame switching DC power supplies. The 5A and 5B series, 40 and 60 W respectively, come in single- and multiple-output versions. The single-output models 5A5 and 5B5 deliver 5 V at 7 A and 12 A at full load. Prices for these models are $45 and $75 respectively. The 40 W multiple-output 5AXMP delivers 5 V at 4 A, ± 12 V at 0.5 A, -5 V at 0.5 A, and + 15 V at 1.0 A for $59. The 60 W multiple-output 5BXMP delivers 5 V at 7 A, + 12 V at 1.5 A, -12 V at 0.5 A, and -5 V at 0.25 A for $89. For complete details, contact Sierracin/ Power Systems, 20500 Plummer St, Chatsworth CA 91311, (800) 423-5569; in California (213) 998-9873.

Circle 412 on inquiry card

DIP-85 Printer

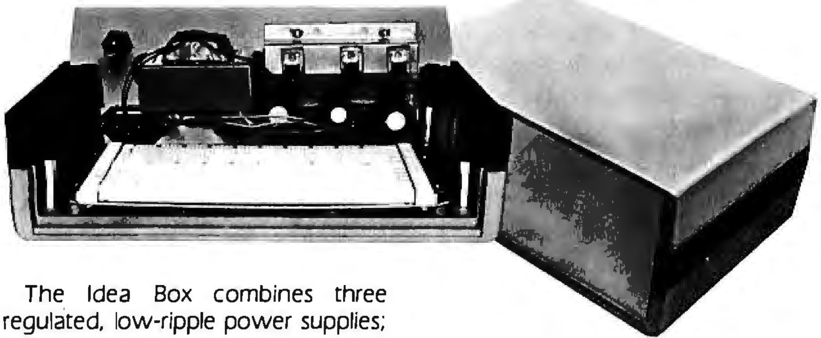
The DIP-85 impact printer features a 7 by 7 or 14 by 7 dot matrix, 6 character sizes, 100 cps (characters per second) bidirectional print speed, tractor or friction paper feed, and a ribbon cartridge. It has variable line density and continuous form-length controls. The printer has a high-resolution graphic capability and can provide plotting, video-display graphics, illustrations, and special-effects symbols. The unit has data rates up to 9600 bps, parallel and serial RS-232C ports, and a 1 K-byte buffer. With a 96-character ASCII (American Standard Code for Information Interchange) set, the DIP-85 is capable of uppercase and lowercase printing at 80, 96, or 132 characters per line on standard-sized paper. Paper feed is at the rate of 10 lines per second. Operator control includes power, select/ deselect, line feed, top of form, self-test, and variable vertical-tab setting. The DIP-85 is priced at $625 in quantities of 100. For more information, contact DIP Inc, 745 Atlantic Ave, Boston MA 02111, (617) 482-4214.

Circle 413 on inquiry card

What's New?

PERIPHERALS

Idea Box for Experimenters



The Idea Box combines three regulated, low-ripple power supplies; a choice of a solderless breadboard, a pre-etched, pre-drilled printed-circuit board, or a blank foil board. This combination allows easy construction of a prototype or a built-once-only device. The Idea Box is priced from $149.95. The circuit cards and printed-circuit layout pads are available individually from $4.95 to $44.95. Contact Global Specialties Corporation, 70 Fulton Ter, New Haven CT 06509, (203) 624-3103.

Circle 407 on inquiry card

Interface the Apple II to Centronics-Type Printers

The Model 7728 Centronics Printer Interface makes the Apple II compatible with printers using Centronics-type parallel interfaces, such as the Okidata Microline 80, the Microtek MT-80P, the MPI 88T, and Centronics printers. A 256-byte ROM (read-only memory) provides driver firmware and controls character output to the printer. The 7728 supports the interrupt daisy chain with arbitration logic, including jumper-selectable IRQ generation, and it provides direct-memory-access daisy-chain pass-through. The printer interface includes an 8-bit data output bus, four status inputs, data strobe and acknowledge handshake signals, and a printer-reset signal. The 7728 comes assembled and tested, with documentation, for $119.95. Cables for different printers are available from the manufacturer. Contact California Computer Systems, 250 Caribbean Dr, Sunnyvale CA 94086, (408) 734-5811.

Circle 408 on inquiry card

Five-Inch Hard-Disk Drive

Tandon Magnetics Corporation has a family of hard-disk drives that can store 3.19 to 11.5 megabytes. The TM 600 family of 5-inch Winchester-type hard-disk drives contains one-, two-, and three-platter models. These drives feature a track-to-track access time of 3 ms and an average access time of 168 ms. Recording density is 7690 bits per inch and rotating speed is 3600 rpm (revolutions per minute). Tandon offers two interfaces, the S and the T versions. The S version is compatible with higher-capacity drives, and the T version is compatible with Tandon's TM 100 floppy-disk drives. The T version allows the TM 600 series to run in a daisy chain with the TM 100-4 floppy-disk drive. This permits 11.5 megabytes of fixed-disk storage in a daisy chain with 3 megabytes of floppy-disk storage.

The three-platter TM 603E offers a capacity of 11.5 unformatted megabytes with 230 cylinders. The TM 602E is a two-platter unit offering 7.66 megabytes of storage with 230 cylinders. The two-platter TM 602 model stores 6.38 megabytes, and the TM 603 delivers 9.57 megabytes with three platters. Up to four TM 600s can be daisy-chained on a single bus. The TM 600 family is priced in the $1400 to $1600 range. Contact Tandon Magnetics Corporation, 9333 Oso Ave, Chatsworth CA 91311, (213) 993-6644.

Circle 409 on inquiry card

80 by 24 Video Display for the Apple II

The Full-View 80 is an 80-column by 24-line uppercase and lowercase plug-in video-display card for the Apple II. Under keyboard or program control, Full-View 80 permits user selection of 80- or 40-column graphics on the same monitor. Four character generators are offered. One is a 7 by 9 dot-character font. Two are user-programmable EPROM (erasable programmable read-only memory) types that contain line-drawing graphics; one has 127 characters and the other 255 characters. The fourth is a 5 by 7 dot matrix to permit 80-column display on low-performance monitors. The Full-View 80 works with Apple Pascal, Microsoft's SoftCard, the Hayes Microcomputer Products Micromodem, the Apple Communications Card, and all Apple peripherals. A 2 K-byte ROM provides keyboard editing, cursor control, tabbing, and scrolling. Seven other keyboard-function keys are provided. The firmware incorporates Pascal and BASIC protocols. A real-time nonmaskable interrupt clock can be software-enabled to permit timing of programs in background mode. A read-screen capability, a blank-screen function, and a light-pen connector with firmware support are provided. When the keyboard is shift-locked, the cursor blinks. The price is $395 from Bit 3 Computer Corporation, 1890 Huron St, St Paul MN 55113, (612) 926-6997.

Circle 410 on inquiry card

240 lpm Thermal Printer/Plotter

Printer Systems Corporation's TH 240 is an 80-column thermal printer that prints 240 lpm (lines per minute). This speed permits copying a 24-line video display in less than 6 seconds. The 240 has an optional plotting mode that produces 70 by 560 dots per inch resolution. The TH 240 is priced at $1395 for the alphanumeric version and $1595 for the alphanumeric-plus-plotting version. For details, contact Printer Systems Corporation, 1 W Deer Park Rd, Suite 104, Gaithersburg MD 20760, (301) 840-1070.

Circle 411 on inquiry card

What's New?

MISCELLANEOUS

Dual-Output DC Power Supplies

The 200 series dual-output DC power supplies from Power General include thirteen models with outputs of ±5 VDC, ±12 VDC, or ±15 VDC with output currents from ±50 mA to ±500 mA. Other specifications include: input voltage range 105 to 125 VAC; input frequency 50 to 440 Hz; output-voltage accuracy ±1%; line regulation ±0.05%; load regulation ±0.1%; ripple and noise 1 mV RMS; transient recovery time 50 μs; breakdown voltage 1500 VAC; and an operating temperature range of −25°C to +71°C. Prices range from $49 to $109. Contact Power General, 152 Will Dr, Canton MA 02021, (617) 828-6216.

Circle 417 on inquiry card

Let This Program Write Your Programs

PEARL Level 3 is an automatic systems generator. PEARL allows you to respond to on-screen menus and prompts to define a desired program. PEARL uses this input to generate error-free source code in BASIC and to produce desired applications software. It can also create complex multiple-file applications programs. The program lets you describe performance requirements, then turn the linear programming over to PEARL. PEARL 3 enables you to create programs for menu selection, file update and edit, reports, editing control data, file reorganization, and general report writing. It can define and cross-index elements between multiple files within a single system, define reports using data from multiple files, extend the standard program menu, define the interrelationships between data elements in different files, post journal files to a master file, provide extended report generation, and support multiple index keys for a file. PEARL 3 is priced at $650, PEARL 2 for $350, and PEARL 1 for $130. PEARL 1 and 2 are for beginning and intermediate programmers. Contact CPU, POB 12892, Salem OR 97309, (503) 370-8653.

Circle 418 on inquiry card

Mostek Announces a 64 K-Byte Dynamic Programmable Memory

The MK4164 is a series of 64 K-byte programmable memories featuring polysilicon lines instead of diffused bit lines for a 50% signal increase to the sense amplifier. By relocating the bit lines to a different level, the distance between adjacent capacitors is reduced to 3 microns. This space savings permits an increase of the storage-capacitor size to 75% of the total cell area. To increase the density from 16 to 64 K bits, the device uses 512 sense amplifiers. The MK4164s feature an internal refresh counter. Another refresh feature permits the output to be held valid indefinitely by holding $\overline{\text{CAS}}$ (column address strobe) active low. The series features single +5 V supply operation, maximum power of 300 mW (20 mW standby), and 150 ns access time. The MK4164-15 has a 325 ns cycle time. The price for the MK4164-20 in 100-piece lots is $59.99. For complete details on the MK4164s, contact Mostek Corporation, 1215 W Crosby Rd, Carrollton TX 75006, (214) 323-6000.

Circle 419 on inquiry card

Built-In Foreign Languages

The ML-32 multi-language system offers users the ability to select sets of 32 different languages, resident in the system, and display these languages simultaneously on the screen or have them printed. The system offers multilanguage communications in a word-processing package. Black-and-white graphics are included with color graphics provided in the CML-32. The ML-32 can interface with any host computer system. The screen displays 34 lines of 80 characters on a high-resolution monitor. There are 80 programmable function keys on the keyboard. The system can also utilize floppy-disk drives, cassette tape players, and hard-disk drives. RS-232C, IEEE, and IBM 3270 input/output ports are provided. The languages in the system include English, Greek, Arabic, Hebrew, Russian, Japanese, Chinese, German, French, Italian, Welsh, Dutch, Norwegian, Swedish, Turkish, Spanish, Latin, Icelandic, Hungarian, Albanian, Bulgarian, and Portuguese. The price for the ML-32 is $17,500, and the CML-32 is priced at $26,000. For more information, contact Michael Root at Computer Systems Consultants Inc, 225 Main St, Chelmsford MA 01863, (617) 251-8561.

Circle 420 on inquiry card

What's New?

MISCELLANEOUS

Hayden Books Brochure

Hayden Book Company Inc's new brochure lists books on computer science, electricity and electronics, engineering, mathematics, and other special interests. It is available free upon request from the Hayden Book Company Inc, 50 Essex St, Rochelle Park NJ 07662, (800) 827-3777, ext 302.

Circle 421 on inquiry card

Basic Electricity Course from Heathkit/Zenith

The EE-3100 Basic Electricity Course, from Heathkit/Zenith Educational Systems, is designed for the self-starter. If you wish to expand your knowledge of basic electronics, this course will serve as your introduction to Ohm's Law, power, series and parallel circuits, electromagnetism, types of current, motors, generators, and meters. The course is written in a programmed-instruction format, and includes two audio cassettes. It is costs $29.95. Contact Heathkit/Zenith Educational Systems, Department 350-540, Benton Harbor MI 49022, (616) 982-3210.

Circle 422 on inquiry card

Graphics Coprocessor Integrated Circuits

EFCIS, a subsidiary of Thomson-CSF, has introduced two graphics devices. The EF 9365 (512 by 512 pixels) and the EF 9366 (512 by 256 pixels) graphics processors can directly execute high-level-language descriptors by means of vector-descriptor files. The on-chip vector generator allows a writing speed of more than 500 meters per second on a 51 cm (21-inch) screen. The devices generate all the timing signals required for interfacing with video displays. The circuits contain a 96-character ASCII (American Standard Code for Information Interchange) generator. They also have light-pen registers and controls, three types of interrupt requests, and TTL-LS I/O ports. For additional details, contact EFCIS at 23, rue de Courcelles, B.P.96.08, 75362, Paris, Cedex 08, France.

Circle 423 on inquiry card

High-Speed 16 K-Byte ROM Challenges Bipolar PROMs

Synertek has announced the SY3316 MOS (metal-oxide semiconductor) 2048 by 8 high-speed ROM (read-only memory) that can replace bipolar PROMs (programmable read-only memories) in many applications. The device features a maximum access time of 80 ns. It is fully compatible with 16 K-byte PROMs. The SY3316 is compatible with TTL (transistor-transistor logic) on all inputs and outputs and operates on a single +5 V power supply. It includes three-state outputs. The device uses static circuitry and operates asynchronously. The three circuit-selects are mask programmable so that high, low, or undecided active states are possible. Eight ROMs can be connected without needing external decoding. In quantities of 250, the device is priced at $56. For more information, contact Synertek, 3001 Stender Way, Santa Clara CA 95051, (408) 988-5623. Circle 424 on inquiry card

Intel's EEPROM

Intel Corporation has introduced an electrically erasable programmable read-only memory (EEPROM). The 2816 is a 16 K-bit nonvolatile memory that is byte-erasable with an access time of 250 ns. Users can erase, read, and write on the device without removing it from the computer. The 2816 erases and writes by causing electrons to tunnel across a thin layer of silicon dioxide. At 125°C, the 2816 will retain data for at least 20 years. The circuit is fully static and it needs no refreshing. Erasing and writing requires the application of a 21 V pulse for 10 ms. Any of the 2 K bytes of the 2816 can be erased and rewritten in 20 ms. Separate chip-enable and output-enable pins permit 2-line control of the unit, which eliminates contention between addresses and data on multiplexed bus lines. It is pin-for-pin compatible with the 2716 ultraviolet EPROM and plug-compatible with 2732 and 2764 EPROMs. The 2816 costs $120 in 100-piece lots. Contact Intel Corporation, 3065 Bowers Ave, Santa Clara CA 95051, (408) 987-6742.

Circle 425 on inquiry card

Color Computer from Commodore

VIC 20 (video interface computer) is a color computer priced under $300. It connects to any television set or monitor and provides 5 K bytes of memory. VIC 20 features color, sound, programmable function keys, memory expansion to 32 K bytes, PET BASIC, expansion ports, a 22-character by 23-line screen display, high-resolution graphics, graphics character set, joystick, paddles, light pen, and plug-in memory and program cartridges. VIC system peripherals include a cassette-tape drive, a floppy-disk drive, and a printer. The computer uses the 6502 microprocessor and the VIC (video interface chip), which incorporates programmable memory, ROM (read-only memory), and video-control circuitry on the same integrated circuit. Contact Commodore Business Machines Inc, 950 Rittenhouse Rd, Norristown PA 19403, (215) 666-7950.

Circle 426 on inquiry card

Check Spelling with Spellguard

Spellguard is a program to check spelling in documents prepared with word processors and text editors. A 10,000-word document (20 pages) can be checked for spelling and typographical errors in under one minute. Spelling is checked using a dictionary supplied with the Spellguard package. The dictionary contains the 20,000 most-commonly used words in English and can be expanded. The dictionary size is limited only by disk-file size. One feature of Spellguard is the ability to create multiple dictionaries. Spellguard also contains a self-diagnostic feature for protection. Spellguard works with most CP/M-based word processors, including WordStar, Magic Wand, Electric Pencil, and Spellbinder. The program requires an 8080-, 8085A-, or Z80-based system, at least 32 K bytes of programmable memory, one 8-inch floppy-disk drive, and CP/M 1.4 or a later version. Spellguard has a suggested retail price of $295; a manual is available for $15. Contact Innovative Software Applications, 915 Timothy Ln, Menlo Park CA 94025, (415) 326-0805.

Circle 427 on inquiry card

What's New?

SOFTWARE

UCSD Pascal for the Sprint 68

Wintek has the UCSD Pascal compiler available for its Sprint 68 microcomputer. The package includes an interactive operating system, Pascal compiler, screen-oriented editor, macroassembler, linker, p-code interpreter, and a library of utilities. The price for the package is $675 from Wintek Corporation, 1801 South St, Lafayette IN 47905, (317) 742-8428.

Circle 429 on inquiry card

Duel-N-Droids

Duel-N-Droids is a sound and graphics game program for the TRS-80 Model I Level II. It features two sword-wielding androids that clash with each other in both practice and tournament duels. Each player controls his androids with four letter keys, causing it to maintain defense, back off, or attack. Each win moves the rank of the player's android up one level on the game scale. In practice duels, the player manually controls one android while the computer controls the other. In tournament duels, the machine controls both androids, using the skills instilled by the player during practice sessions. The program is priced at $14.95 for cassette versions and $20.95 on floppy disks. Contact Acorn Software Products Inc, 634 North Carolina Ave SE, Washington DC 20003, (202) 544-4259.

Circle 430 on inquiry card

Alpha Micro FIG-FORTH

Version 3.2 of μA/FORTH is available for Alpha Micro systems. This version is aligned with the 1978 standard of the FORTH International Standards Team. It allows complete access to Alpha Micro's AMOS operating system. It implements full-length names up to 31 characters, checks code at compile-time with error reporting, and contains string-handling routines and a string-search editor. A FORTH assembler is included. FORTH words (commands) may be created from previously defined words, and even the original words supplied with the system can be redefined. It comes on an AMS format floppy disk and includes all source code, an editor, an assembler, and a string package. It costs $130 from Professional Management Services, 724 Arastradero Rd, Suite 109, Palo Alto CA 94306, (408) 252-2218.

Circle 431 on inquiry card

Apple II Curve Fitter

Curve Fitter allows you to select an appropriate mathematical curve to fit your experimental results. Methods include scaling and transformations, averaging, smoothing, interpolation, least-squares fitting, and interpolation of unknown values from the fitted curve. Using an optional A/D (analog-to-digital) converter, data can be entered directly from instruments. Curve Fitter is compatible with VisiChart. Curve Fitter runs on a 48 K-byte Apple II with Applesoft in ROM (read-only memory). It is available on floppy disk with a 29-page manual for $35. The manual is available separately for $5. Contact Paul K Warme, Interactive Microware Inc, POB 771, State College PA 16801, (814) 238-8294.

Circle 428 on inquiry card

UniFLEX Operating System

UniFLEX is a multitasking, multiuser operating system. Several users can run different programs simultaneously, and one user can run several programs at a time. Users must log in with a password before being permitted to use the system. UniFLEX supports a hierarchical file system allowing file sizes up to 1 gigabyte (ie: 1 billion bytes) and disk capacities of over 8 gigabytes. All system I/O is device-independent. Any combination of interrupt-driven devices can be attached to the system. Intertask communication is supported, and task swapping can occur. The basic UniFLEX system includes the operating system, approximately 50 system utilities, a text editor, macroassembler, and system-configuration programs. System maintenance is also available. Software that runs under this system includes a C compiler, Pascal, word processors, a debug package, and BASIC. UniFLEX is available for 6809 and 68000 systems. The price is $450 for the 6809 version. Contact Technical Systems Consultants Inc, POB 2570, 1208 Kent Ave, West Lafayette IN 47906, (317) 463-2502.

Circle 432 on inquiry card

FORTRAN and COBOL for the Apple II with the SoftCard

The Apple II can now have FORTRAN and COBOL thanks to Microsoft Consumer Products. Both languages run under the CP/M operating system and are designed to be used with Microsoft's SoftCard. FORTRAN-80 can compile several hundred statements per minute in a single pass. The FORTRAN compiler creates true Z80 machine code and supports double-precision, integer X4 and integer X1 data types. The FORTRAN-80 package includes the compiler, a linking loader, and a user's manual. It also requires 48 K bytes of memory and a floppy-disk drive. The suggested price is $195.

COBOL-80 includes sequential, line-sequential, relative, and indexed-sequential data files. Program chaining with parameter passing allows systems control from within COBOL applications. The program supports String, Unstring, Compute, Search, Perform, and Varying/Until verbs; abbreviated and compound conditions; ASCII (American Standard Code for Information Interchange), packed and binary data formats; run-time assignment of file names; full Copy facility; and packed-decimal data format. The COBOL-80 package includes the compiler, linking loader, macroassembler, library manager, cross-reference assembler, and documentation. It runs on the Apple II with SoftCard, 48 K bytes of programmable memory, and two disk drives. The suggested price is $750. For complete details, contact Microsoft Consumer Products, 400 108th Ave NE, Suite 200, Bellevue WA 98004, (206) 454-1315.

Circle 433 on inquiry card

Remote Batch Terminal Emulator

The Remote Batch Terminal Emulator, RBTE, allows Z80 systems to emulate an IBM 3780, 2780, 2770, 3741, or 2968 remote batch terminal. It provides the ability to transfer data files to and from mainframe computers or other remote batch terminals. Data rates up to 19.2 kbps (thousand bits per second) can be set. IBM bisynchronous protocol, hardware diagnostics, dynamic terminal configuration, on-line communication trace, attended and unattended operation, and user-customization are featured. The RBTE runs under CP/M, OASIS, and other special operating systems for Z80 microcomputers. It is designed for TRS-80, Cromemco, North Star, Onyx, Gnat, Vector Graphic, Ithaca Intersystems, and other Z80 microcomputer systems. Versions are available for 8086, Z8000, and 68000 microprocessor-based systems. Software to emulate X.25 protocol is also available. The price for the RBTE is $500 for a single-use license. The operator manual and the programmer manual are available for $25 and $15, respectively. For complete details, contact Winterhalter and Associates Inc, 3825 Zeeb Rd, Dexter MI 48130, (313) 665-5582.

Circle 434 on inquiry card

This Program Moves Files Through VisiCalc

VU #3 is a utility program for Personal Software's calculating and bookkeeping program VisiCalc. VU #3 allows the user to enter data into VisiCalc from any program by inserting data into an array defined by VU #3. The program can transfer data generated from VisiCalc into any of the user's programs through another array as defined in the instructions. VU #3 runs on the Apple II. It is available from Progressive Software, POB 273, Plymouth Meeting PA 19462.

Circle 435 on inquiry card

Wordbank for the TRS-80 Model II

The Wordbank is a word-processing program for writing letters, reports, manuals, or other documents on a one-time or repetitive basis. Up to 7500 document lines are available; lines may be added, changed, or deleted; page control is user-assigned or automatic; and automatic line numbering and pagination are included. Wordbank requires a TRS-80 Model II with 64 K bytes of programmable memory, one floppy-disk drive, and a printer. Wordbank is available from Taranto and Associates Inc, POB 6073, 121 B Paul Dr, San Rafael CA 94903, (415) 472-2670, for $149.95.

Circle 436 on inquiry card

Pascal Data Base Written in UCSD Pascal

The Pascal Database can be used for mailing lists, accounting, inventory, job estimates, sales analysis, and property management. The data base can update, search, and traverse data-base files; sort on multiple fields; and maintain records in several sorted orders. There is user-programmable screen formatting and automatic indexing of information at data entry. Users can define file, record, and field names. Reports can also generated. The Pascal Database for the Apple II costs $400, and it is available from Arizona Computer Systems Inc, POB 125, Jerome AZ 86331, (602) 634-7301.

Circle 437 on inquiry card

General Ledger System for Prodigy Computers

Prodigy Systems has a small-business accounting package with a general-ledger program for its computers. Features include a user-defined chart of accounts, current balances, audit trail, and the ability to produce comparative statements. The system allows users to format their own reports. The reports include account charts, general ledger, trial balance, income statements, balance sheets, and transaction proof listings. The general-ledger system includes accounts receivable, accounts payable, and payroll packages. Contact Prodigy Systems Inc, 497 Lincoln Hwy, Iselin NJ 08830, (201) 283-2000.

Circle 438 on inquiry card

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INTEGRATED CIRCUITS

7400TTL	
7400N	19
7402N	20
7404N	25
7409N	27
7410N	25
7414N	70
7420N	25
7422N	.39
7430N	.25
7442N	.58
7445N	.82
7447N	.63
7448N	.77
7450N	.25
7474N	35
7475N	.49
7485N	.88
7489N	1.70
7490N	.43
7492N	.43
7493N	43
7495N	.69
74100N	1.35
74107N	.35
74121N	.34
74123N	59
74125N	45
74145N	.77
74150N	1.20
74151N	.69
74154N	1 25
74157N	.69
74161N	.87
74162N	.85
74163N	.87
74174N	.89
74175N	.85
74190N	1.15
74192N	.87
74193N	.85
74221N	1.25
74298N	1.65
74365N	.75
74366N	.75
74367N	75
74LS00 TTL	
74LS00N	29
74LS02N	29
74LS04N	.35
74LS05N	.25
74LS08N	35
74LS10N	35
74LS13N	.55
74LS14N	1.00
74LS20N	.35
74LS22N	.35
74LS28N	35
74LS30N	35
74LS33N	60
74LS38N	50
74LS74N	.45
74LS75N	65
74LS90N	.60
74LS93N	.75
74LS95N	1.00
74LS107N	.45
74LS112N	.45
74LS113N	.45
74LS132N	.89
74LS136N	.50
74LS151N	.75
74LS155N	79
74LS157N	1 10
74LS162N	1.10
74LS163N	1.10
74LS174N	1.15
74LS190N	1.25
74LS221N	1.25
74LS258N	1.00
74LS367N	89
LINEAR	
CA3045	.90
CA3046	1.10
CA3081	1 80
CA3082	1.90
CA3089	3.40
LM301AN/AH	.35
LM305H	.87
LM307N	.35
LM308N	1.00
LM309K	1.25
LM311H/N	.90
LM317T	1.65
LM317K	3 75
LM318	1.50

LM320K-5	1 35
LM320K-12	1.35
LM320K-15	1 35
LM320T-5	.95
LM320T-8	.95
LM320T-12	.95
LM320T-15	.95
LM323K-5	5 95
LM324N	1 00
LM339N	1.00
LM340K-5	1.35
LM340K-8	1 35
LM340K-12	1.35
LM340K-15	1 35
LM340K-24	1.35
LM340T-5	85
LM340T-8	.85
LM340T-12	.85
LM340T-15	.85
LM340T-18	.85
LM340T-24	85
LM350	5 50
LM377	2.95
LM379	5.00
LM380N	1.00
LM381	1.60
LM382	1 60
LM709H	.59
LM723H/N	50
LM733N	.85
LM741CH	.35
LM741N	.38
LM747H/N	.75
LM748N	.50
LM1303N	1.75
LM1304	1.10
LM1305	1.27
LM1307	2.00
LM1310	1.95
LM1458	.55
LM1812	7.50
LM1889	3.00
LM2111	1.75
LM2902	2.25
LM3900N	60
LM3905	1.75
LM3909N	.95
MC1458V	.55
NE550N	1.35
NE555V	.39
NE556A	.85
NE565A	1.00
NE566V	1.50
NE567V	1.00
NE5708	4.75
78L05	60
78L08	60
78M05	85
75108	1.75
75491CN	.50
75492CN	.55
75494CN	89
A to D CONVERTER	
80388	4.50
8700CJ	13.95
8701CN	22 00
8750CJ	13.95
LD130	9.95
9400CJV/F	7 40
ICL7103	9.50
ICL7107	14 25
CMOS	
CD4000	25
CD4001	.35
CD4002	.35
CD4006	1.10
CD4007	35
CD4008	1.20
CD4009	.45
CD4010	.45
CD4011	.35
CD4012	28
CD4013	.47
CD4014	1.25
CD4015	1.00
CD4016	.55
CD4017	1.05
CD4018	.94
CD4019	.45
CD4020	1.02
CD4021	1.35
CD4022	1.10
CD4023	.28
CD4024	.75
CD4025	.28

CD4026	2 50
CD4027	.66
CD4028	.85
CD4029	1 35
CD4030	.45
CD4035	1 00
CD4040	1 35
CD4042	.85
CD4043	.85
CD4044	.85
CD4046	1 67
CD4049	.45
CD4050	.50
CD4051	1 13
CD4060	1 42
CD4066	71
CD4068	.40
CD4069	.40
CD4070	50
CD4071	45
CD4072	45
CD4073	45
CD4075	45
CD4076	1 45
CD4078	40
CD4081	35
CD4082	35
CD4116	.47
CD4490	5.50
CD4507	1.00
CD4508	2.85
CD4510	1.00
CD4511	.96
CD4515	2.52
CD4516	1 10
CD4518	1.50
CD4520	1.02
CD4527	1 51
CD4528	1.60
CD4553	3.50
CD4566	2.45
CD4583	2 35
CD4585	1 10
CD40192	3.00
74C00	35
74C04	40
74C10	35
74C14	.89
74C20	35
74C30	35
74C48	1 95
74C74	65
74C76	1 25
74C90	1.25
74C93	1 25
74C154	3 50
74C160	2 75
74C175	1.35
74C192	1 65
74C221	1.80
74C905	8 00
74C906	75
74C914	1.95
74C922	5 00
74C923	5 50
74C925	7 50
74C926	6 95
74C927	6 95
INTERFACE	
8095	.65
8096	.65
8097	.65
8098	65
8T09	1 25
8T10	4.50
8T13	3.00
8T20	5.50
8T23	3 10
8T24	3.50
8T25	3.20
8T26	1.69
8T28	2.75
8T97	1.69
8T98	1.69
MOS/MEMORY RAM	
2101-1	3.85
2102-1	.95
2102AL-4	1.45
2102AN-2L	1.65
2104A-4	4.95
2107B-4	3 75
2111-1	3.75
2112-2	3.95
2114	3.75
2114L 300ns	4.25

2114L 450ns	4 00
4116 200ns	4 50
8x4116 200ns	26 95
MM5262	40
MM5280	3.00
MM5320	9.95
MM5330	5.94
PD411D-3	4.00
PD411D-4	5 00
P5101L	8 95
4200A	9.95
82S25	2.90
91L02A	1.50
HD0165-5	6.95
MM57100	4.50
GIAY38500-1	9.95
MCM6571A	9.95
9368	3.50
4100	10 00
416	16 00
CLOCKS	
MM5311	5.50
MM5312	3.90
MM5314	3.90
MM5369	2 10
MM5841	14.45
MM5865	7 95
CT7010	8 95
CT7015	8.95
MM5375AA/N	3.90
MM5375AG/N	4 90
7205	16.50
7207	7.50
7208	15.95
7209	4.95
DS0026CN	3.75
DS0056CN	3.75
MM53104	2.50
MICROPROCESSOR	
6502	10.95
6504	9.95
6522	9.95
6800	6.95
6802	11.95
6820	4 95
6850	5.95
8080A	3.95
8085	12.95
8086	75.00
Z80	9.95
Z80A	11.95
8212	2.90
8214	3.95
8216	2.90
8224	3.45
8228	4.95
8251	6.95
8253	15.00
8255	5.75
8257	10.95
8259	14.95
1802CP plas.	13 95
1802DP plas.	17.95
1861P	9.50
CDP1802CD	28.95
CDP1802D	35.00
CDP1816P	7.95
UART/FIFO	
AY5-1013	5.50
AY5-1014	7.50
3341	6.95
PROM	
1702A	4.95
2708	6.10
2716T1	18.00
2716 5 Volt	10.50
8/2716 5 Volt	89.00
2732	29.50
2758	19.50
8741A	55.00
8748	55.00
8748-8	55 00
8755A	55 00
N82S23	2.95
N82S123	6.50
N82S126	3.75
N82S129	8.50
N82S131	8.50
N82S136	8.75
N82S137	8.75
DM8577	2.90
8223	2.90

CONNECTORS	
30pin edge	2.50
44 pin edge	2.75
86pin edge	4.00
100pin edge	4.50
100 pin edge WW	5.25

IC SOCKETS

Solder Tin	Low Profile		
PIN	1UP	PIN	1UP
8	.15	22	.30
14	.14	24	.35
16	.16	28	.42
18	27	36	58
20	29	40	57

2 level 14 pin ww 20

WIRE WRAP LEVEL 3

PIN		PIN	
14	.46	24	.93
16	.49	28	1.00
18	.67	40	1 59

CRYSTALS	
1 MHz	4 50
2 MHz	4 50
4 MHz	4.25
5 MHz	4.25
10 MHz	4.25
18 MHz	3.90
20 MHz	3.90
32 MHz	3.90
32768 Hz	4 00
1.8432 MHz	4 50
3.5795 MHz	1 20
2.0100 MHz	1.95
2.097152 MHz	4.50
2.4576 MHz	4.50
3.2768 MHz	4.50
5.0688 MHz	4 50
6.185 MHz	4 50
5.7143 MHz	4.50
6.5536 MHz	4.50
14.31818 MHz	4.25
18.432 MHz	4 50
22.1184 MHz	4 50
KEYBOARD ENCODERS	
AY5-2376	$12.50
AY5-3600	17.95
AY5-9100	10.50
AY5-9200	16.50
74C922	5.50
74C923	5.50
HD0165-5	6.95
AY5-9400	10.50
D Connectors RS232	
DB25P	3.62
DB25S	5.20
Cover	1.67
DE9S	1.95
DA15P	2.10
DA15S	3.10
Complete Set	9.50
Hickok 3½ Digit LED multimeter	89.95
Stopwatch Kit	26.95
Auto Clock Kit	17.95
Digital Clock Kit	14.95
6K/1 8K Eprom Kit (less PROMS)	$89.00
Motherboard	$39.00
Extender Board	$15.00
RESISTORS ¼ watt 5%	
10 per type	.03
25 per type	025
100 per type	015
1000 per type	.012
350 piece pack 5 per type	6.75
½ watt 5% per type	.05
Televideo Terminal	
Model 912	$785.00
Model 920	$885.00
TinyBasic Experimenters Kit	$10.00

KEYBOARDS	
56 key ASCII keyboard kit	$67.50
Fully assembled	77.50
53 key ASCII keyboard kit	60.00
Fully assembled	70.00
Enclosure Plastic	14.95
Metal Enclosure	29.95
LEDS	
Red TO18	.15
Green, Yellow TO18	.20
Jumbo Red	.20
Green, Orange, Yellow Jumbo	25
Cliplite LED Mounting Clips (specify red, amber, green, yellow, clear)	8/$1.25

CONTINENTAL SPECIALTIES in stock
Complete line of breadboard test equip.

MAX-100 8 digit Freq. Ctr.	$149.95

OK WIRE WRAP TOOLS in stock

Portable Multimeter	$18.00

Complete line of AP Products in stock.

SPECIAL PRODUCTS	
MM5865 Stopwatch Timer with 10pg. spec	9.00
PC board	7.50
Switches Mom. Pushbutton	27
3 pos slide	.25
Encoder HD0165-5	6.95
Paratronics	
Model 10 Trigger Expander Kit	$229.00
Model 150 Bus Grabber Kit	$369.00
Clock Calendar Kit	$23.95
2.5 MHz Frequency Counter Kit	$37.50
30 MHz Frequency Counter Kit	$47.75
TRANSFORMERS	
6V 300 ma	3 25
12 Volt 300ma transformer	1 25
12 6VCT 600 ma	3.75
12V 250 ma wall plug	2.95
12V CT250 ma wall plug	3.75
24V CT 100 ma	3.95
10V 1 2 amp wall plug	4 85
12V 6 amp	12 95
12V 500 ma wall plug	4 75
12V 1 amp wall plug	6 50
10/15 VAC 8/16 VA wallplug	9.75

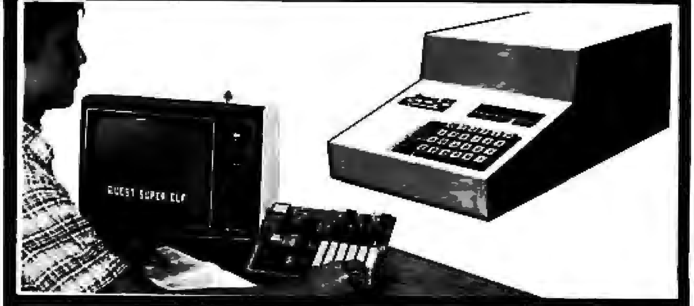
DISPLAY LEDS

MAN1	CA	270	2.90
MAN3	CC	125	39
MAN72/74	CA/CA	.300	1.00
DL704	CC	.300	1.25
DL707/DL707R	CA	.300	1.00
DL727/728	CA/CC	.500	1.90
DL747/750	CA/CC	600	1.95
FND359	CC	357	.70
FND500/507	CC/CA	500	1 35
FND503/510	CC/CA	.500	.90
FND800/807	CC/CA	800	2.20
3 digit Bubble			.60
10 digit display			1.25
7520 Clairex photocells			.39
TIL311 Hex			9.50
MAN3640	CC	.30	1.10
MAN4610	CA	40	1.20
MAN4640	CC	40	1.20
MAN4710	CA	40	95
MAN4740	CC	40	1.20
MAN6640	CC	56	2 95
MAN6710	CA	.60	1.35
MAN6740	CC	.60	1.35

MA1002A, C, E	8.95
MA1012A	8.95
102P3 transformer	2.25
MA1012A Transformer	2.25
DIP Switches	
4-position	$ .95
5-position	1.00
6-position	1.00
7-position	1.00
8-position	1.05

Complete line of Hobby-Blox solderless breadboards in stock.

IC Starter Pack	$5.95
Discrete Component Starter Pack	$8.57



RCA Cosmac 1802 Super Elf Computer $106.95

Compare features before you decide to buy any other computer. There is no other computer on the market today that has all the desirable benefits of the Super Elf for so little money. The Super Elf is a **small** single board computer that does many **big** things. It is an excellent computer for training and for learning programming with its machine language and yet it is easily **expanded with additional memory, Full Basic, ASCII Keyboards, video character generation, etc.**

Before you buy another small computer, see if it includes the following features: ROM monitor; State and Mode displays; Single step; Optional address displays; Power Supply; Audio Amplifier and Speaker; Fully socketed for all IC's; Real cost of in warranty repairs; Full documentation.

The **Super Elf** includes a **ROM** monitor for program loading, editing and execution with **SINGLE STEP for program debugging** which is not included in others at the same price. With **SINGLE STEP** you can see the microprocessor chip operating with the **unique Quest** address and data bus displays **before, during** and **after** executing instructions. Also, CPU mode and instruction cycle are decoded and displayed on 8 LED indicators.

An RCA 1861 **video graphics** chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a **speaker system** included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

A 24 key **HEX keyboard** includes 16 HEX keys plus **load, reset, run, wait, input, memory protect, monitor select** and **single step**. Large, on board displays provide output and optional **high and low address**. There is a 44 pin standard connector slot for PC cards and a 50 pin connector slot for the Quest Super Expansion Board. Power supply and sockets for **all** IC's are included in the price plus a detailed 127 pg. instruction manual which now includes over 40 pgs. of software info. including a series of lessons to help get you started and a music program and graphics target game. Many schools and universities are using the Super Elf as a course of study. OEM's use it for training and R&D.

Remember, other computers only offer Super Elf features at additional cost or not at all. **Compare before you buy. Super Elf Kit $106.95, High address option $8.95, Low address option $9.95. Custom Cabinet** with drilled and labelled plexiglass front panel **$24.95.** All metal Expansion Cabinet, painted and silk screened, with room for 5 S-100 boards and power supply **$57.00. NiCad Battery Memory Saver Kit $6.95.** All kits and options also completely assembled and tested.

Questdata, a software publication for 1802 computer users is available by subscription for $12.00 per 12 issues. Single issues $1.50. Issues 1-12 bound $16.50.

Tiny Basic Cassette **$10.00,** on ROM **$38.00,** original Elf kit board **$14.95. 1802 software;** Moews Video Graphics **$3.50.** Games and Music **$3.00,** Chip 8 Interpreter **$5.50.**

Super Expansion Board with Cassette Interface $89.95

This is truly an astounding value! This board has been designed to allow **you** to decide how you want it optioned. **The Super Expansion Board comes with 4K of low power RAM** fully addressable anywhere in 64K with built-in memory protect and a **cassette interface.** Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the **Super Elf.** The board includes slots for up to 6K of **EPROM** (2708, 2758, 2716 or TI 2716) and is **fully socketed.** EPROM can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/editor and error checking multi file cassette read/write software, (relocatable cassette file) another exclusive from Quest. It includes register save and readout, block move capability and video graphics driver with blinking cursor. Break points can be used with the register save feature to isolate program bugs quickly, then follow with single step. If you have the **Super Expansion Board** and **Super Monitor** the monitor is up and running at the push of a button.

Other on board options include **Parallel Input and Output Ports with full handshake.** They allow easy connection of an ASCII keyboard to the input port. **RS 232 and 20 ma Current Loop** for teletype or other device are on board and if you need more memory there are two **S-100** slots for static RAM or video boards. Also a 1K Super Monitor version 2 with video driver for full capability display with Tiny Basic and a video interface board. **Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50. A 50 pin connector set** with ribbon cable is available at $15.25 for easy connection between the **Super Elf** and the **Super Expansion Board.**

Power Supply Kit for the complete system (see Multi-volt Power Supply).

Quest Super Basic V5.0

A new enhanced version of **Super Basic** now available. Quest was the first company worldwide to ship a full size Basic for 1802 Systems. A complete function **Super Basic** by **Ron Cenker** including floating point capability with scientific notation (number range $\pm .17E^{38}$), 32 bit integer ±2 billion; multi dim arrays, string arrays; string manipulation; cassette I/O; save and load, basic, data and machine language programs; and over 75 statements, functions and operations.

New improved faster version including **renumber** and essentially **unlimited variables.** Also, an exclusive user expandable command library.

Serial and Parallel I/O included.

Super Basic on Cassette $55.00.

Ohio Scientific Computers

CIP Series 2 **$455.00.** Like an Apple at less than half the price! CIPMF Series 2 **$1199.00.** Minifloppy version with additional RAM/ROM. Complete software and peripherals available. Send for free brochure.

Elf II Adapter Kit $24.95

Plugs into Elf II providing Super Elf 44 and 50 pin plus S-100 bus expansion. (With Super Expansion). High and low address displays, state and mode LED's optional **$18.00.**

Gremlin Color Video Kit $69.95

32 x 16 alpha/numerics and graphics; up to 8 colors with 6847 chip; 1K RAM at E000. Plugs into Super Elf 44 pin bus. No high res. graphics. On board RF Modulator Kit $4.95

Super Color S-100 Video Kit $129.95

Expandable to 256 x 192 high resolution color graphics. 6847 with all display modes computer controlled. Memory mapped. 1K RAM expandable to 6K. S-100 bus 1802, 8080, 8085, Z80 etc.

Dealers: Send for excellent pricing/margin program.

1802 16K Dynamic RAM Kit $149.00

Expandable to 32K. Hidden refresh w/clocks up to 4 MHz w/no wait states. Addl. 16K RAM **$63.00**

Tiny Basic Extended on Cassette (added commands include Stringy, Array, Cassette I/O etc.)	**$15.00**
S-100 4-Slot Expansion	**$ 9.95**
Super Monitor VI.I Source Listing	**$15.00**
Editor Assembler (Requires minimum of 4K for E/A plus user source)	**$25.00**
1802 Tiny Basic Source listing	**$19.00**
Super Monitor V2.0/2.1 Source Listing	**$20.00**

PROM Eraser

assembled. 25 PROM capacity **$37.50** (with timer **$69.50**). 6 PROM capacity OSHA/UL version **$69.50** (with timer **$94.50**).

Z80 Microcomputer

16 bit I/O, 2 MHz clock, 2K RAM, ROM Breadboard space. Excellent for control. Bare Board **$28.50.** Full Kit **$99.00.** Monitor **$20.00.** Power Supply Kit **$35.00. Tiny Basic $30.00**

S-100 Computer Boards

8K Static Godbout Econo IIA Kit	149.00
16K Static Godbout Econo XIV Kit	269.00
24K Static Godbout Econo XX-24 Kit	414.00
32K Static Godbout Econo XX-32 Kit	537.00
16K Dynamic RAM Kit	289.00
32K Dynamic RAM Kit	328.00
64K Dynamic RAM Kit	399.00
Video Interface Kit	$139.00

80 IC Update Master Manual $39.00

Comp. IC data selector, 2700 pg. master reference guide. Over 51,000 cross references. Free update service through 1980. Domestic postage $3.50.

Modem Kit $60.00

State of the art, orig., answer. No tuning necessary. 103 compatible 300 baud. Inexpensive acoustic coupler plans included. Bd. only $17.00.

LRC 7000+Printer $389.00

40/20 column dot matrix impact, std. paper. Interface all personal computers.

64/40/32/20 version **$405.00.** Optional cables available.

LRC 7000 printer interface cable for Super Elf with software **$35.00**

NiCad Battery Fixer/Charger Kit

Opens shorted cells that won't hold a charge and then charges them up, all in one kit w/full parts and instructions. **$7.95**

Rockwell AIM 65 Computer

6502 based single board with full ASCII keyboard and 20 column thermal printer. 20 char. alphanumeric display, ROM monitor, fully expandable. **$405.00.** 4K version **$450.00.** 4K Assembler **$85.00,** 8K Basic Interpreter **$100.00.**

Special small power supply for AIM65 assem. in frame **$54.00.** Complete AIM65 in thin briefcase with power supply **$499.00.** Molded plastic enclosure to fit both AIM65 and power supply **$47.50.** Special Package Price: 4K AIM, 8K Basic, power supply, cabinet **$625.00.**

AIM65/KIM/VIM/Super Elf 44 pin expansion board; 3 female and 1 male bus. Board plus 3 connectors **$22.95.**

60 Hz Crystal Time Base Kit $4.40

Converts digital clocks from AC line frequency to crystal time base. Outstanding accuracy.

Video Modulator Kit $9.95

Convert TV set into a high quality monitor w/o affecting usage. Comp. kit w/full instruc.

Multi-volt Computer Power Supply

8v 5 amp, ±18v .5 amp, 5v 1.5 amp, −5v .5 amp, 12v .5 amp, −12v option. ±5v, ±12v are regulated. Basic Kit **$29.95.** Kit with chassis and all hardware **$43.95.** Add **$4.00** shipping. Kit of hardware **$14.00.** Woodgrain case **$10.00.** $1.50 shipping.

TERMS: $5.00 min. order U.S. Funds. Calif residents add 6% tax.
$10.00 min. BankAmericard and Master Charge accepted. $1.00 insurance optional.
Postage: Add 5%. C.O.D. $10.00 min. order.

FREE: Send for your copy of our NEW 1980 QUEST CATALOG. Include 48¢ stamp.

Circle 81 on inquiry card.

PUBLICATIONS

BYTE Books Brings You Two Books from Steve Ciarcia

Ciarcia's Circuit Cellar, Volume II, is a collection of articles from BYTE. The book tells you about microcomputers and how you can use them in various environments. Construction projects show you how to build a computer-controlled home-security system, computerize home appliances, make an inexpensive joystick, send digital information over a light beam, and explore the Intel 8086 microprocessor system-design kit. Each project is presented in such a way that even beginners should have little trouble making and enjoying these useful devices. Ciarcia's Circuit Cellar, Volume II, costs $11.95.

Build Your Own Z80 Computer is for the engineer, computer technician, student, and anyone interested in building his or her own computer. The computer is based on the Zilog Z80 microprocessor. Each computer subsystem (ie: I/O, serial interface, keyboard, memory, etc) is fully explained and supported by proven design and testing information. The board contains a 2 K-byte operating system, serial and parallel ports, hexadecimal display, and audio-cassette mass storage, with expansion to include a video terminal. You can modify this system to meet your individual needs. All required components are readily available and have been selected to allow simple system checkout. This book costs $15.95. Both books by Steve Ciarcia are published by BYTE Books, 70 Main St, Peterborough NH 03458, (800) 258-5420; in New Hampshire (603) 924-9281.

Circle 439 on inquiry card

Microcomputer and Minicomputer Supplies

Daily Business Products Inc's 68-page catalog features supplies and accessories for all microcomputers, minicomputers, and word-processing systems. For a free copy, contact Daily Business Products Inc, 464 New York Ave, Huntington NY 11743, (800) 645-5332; in New York (212) 594-8065.

Circle 440 on inquiry card

1981 Radio Shack Catalog

Radio Shack's 1981 catalog is available free at Radio Shack stores and dealers. The catalog features computer and stereo equipment, toys and electronic games, plus parts and accessories for home entertainment, or hobbyists and experimenters. The TRS-80 Pocket Computer, the Color Computer, the Model III system, six new stereo receivers, five cassette tape decks, twelve new telephone products, home-alarm systems, and thirteen new electronic calculators are among the items in the catalog.

Circle 441 on inquiry card

Datapro Directory of Small Computers

This guide is designed to help data-processing professionals and managers locate, compare, and evaluate small-computer systems, software, peripherals, services, and the companies that manufacture and distribute them. This directory service is updated monthly. More than 200 microcomputer systems are reported on, with each report giving a summary of current models, memory size, base price, primary uses, popular options, principal applications, and more. The reports have details on hardware specifications, such as the processor used, memory, display, keyboard, direct-access storage, printers, data communications, and I/O electronics. Software information covers languages, operating systems, database-management systems, and applications programs. An applications index, a section on advice and guidelines on purchasing, a listing of over 16,000 companies, and sections on computer concepts, user ratings, and user groups are included. The subscription rate is $330. Each subscription to the Datapro Directory of Small Computers includes two volumes, 12 monthly supplements, 12 monthly newsletters, and use of a telephone-inquiry service. Contact Datapro Research Corporation, 1805 Underwood Blvd, Delran NJ 08075, (609) 764-0100.

Circle 442 on inquiry card

Time-Sharing and Remote-Computing Services Report

Details on 117 remote-computing services, including results of a user survey, are available in this report from Datapro Research Corporation. All About Time-Sharing and Remote Computing Services gives you the name of the service, areas currently served, type of computer, number of simultaneous users, conversational and batch terminals supported, programming languages, principal applications, and pricing information. A listing of vendors is included. The report provides a discussion of user benefits and disadvantages, a guide for evaluation and selection of remote-computing services, and an index of application programs and user programming aids. The report is available for $15 per copy from Datapro Research Corporation, 1805 Underwood Blvd, Delran NJ 08075, (609) 764-0100.

Circle 443 on inquiry card

Packaging and Breadboarding Materials Brochure

A brochure from Vector Electronic Company Inc describes 109 electronic packaging and breadboarding products available at electronic and personal-computer component stores. Highlighted are microcomputer interface boards, Vector products, motherboards, cases, tools, wiring terminals, and kits. A price list is included. Contact Vector Electronic Company Inc, 12460 Gladstone Ave, Sylmar CA 91342, (213) 365-9661.

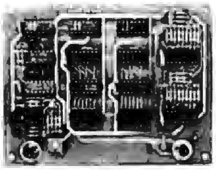
Circle 444 on inquiry card

SDK-85 Experiments

The 8085 Microprocessor—Fundamentals and Applications: 76 Control Experiments with the Intel SDK-85, by Dr Howard Boyet is available from MTI, 14 E 8th St, New York NY 10003, (212) 473-4947. Other books from MTI describe hands-on experiments with the 8080, 8085, and 8048 microprocessors.

Circle 445 on inquiry card

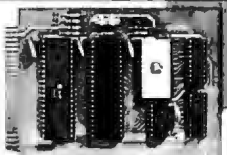
A-D & D-A CONVERTER



JBE A-D & D-A Converter can be used with any system having parallel ports • Interfaces with JBE Parallel I/O Card • D-A conversion time — 5 μs • A-D conversion time — 20 μs • Uses JBE 5V power supply • Parallel inputs & outputs include 8 data bits, strobe lines & latches • Analog inputs & outputs are medium impedance 0 to 5 volt range.

79-287 ASSM. $79.95
Bare Board $29.95 Kit $59.95

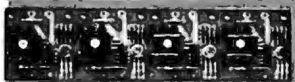
6502 MICROCOMPUTER



This control computer has: • 1024 bytes RAM (two 2114s) • 2048 bytes EPROM (2716) • Uses one 6522 VIA (comp. doc. incl.) • Interfaces with JBE Solid State Switches & A-D & D-A Converter • Uses JBE 5V power supply • 2716 EPROM available separately (2716 can be programmed with an Apple II & JBE EPROM Programmer & Parallel Interface) • 50 pin connector included in kit & assm.

80-153 ASSM. $110.95
Bare Board $24.95 Kit $ 89.95

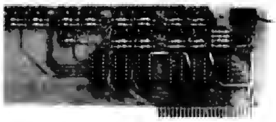
SOLID STATE SWITCH



Your computer can control power to your printer, lights, stereo & any 120VAC appliances up to 720 watts (6 amps at 120VAC). Input 3 to 15VDC • 2-14MA TTL compatible • Isolation — 1500V • Non zero crossing • Comes in 1 or 4 channel version • Includes doc. for interfacing with Dimmer Control.

79-282-1 ASSM. $13.95
Bare Board $6.95 Kit $10.95
79-282-4 ASSM. $49.95
Bare Board $24.95 Kit $39.95

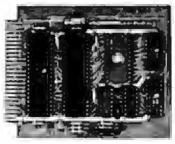
APPLE II DISPLAY BOARD



80-144 ASSM. $49.95
Bare Board $25.95 Kit $42.95

• Has run-stop, single step switch • Has 16 address LEDs, 8 data LEDs & 1 RDY LED • All lines are buffered.

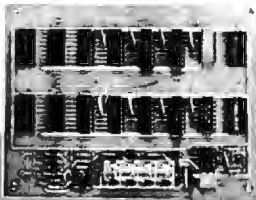
Z80 MICROCOMPUTER



JBE is announcing a single board dedicated computer designed for control functions. It features: • A Z80 Microprocessor software compatible with the Z80, 8080 & 8085 Microprocessors • Uses a Z80 PIO chip for I/O which has 2 independent 8 bit bidirectional peripheral interface ports with handshake & data transfer control • Uses one 2716 EPROM (2K) & two 2114 RAM memories (1K) • Single 5V power supply at 300MA req. • Clock frequency is 2MHz, RC controlled • Board comes with complete doc. • 50 pin connector is included • 2716 EPROM available separately.

80-280 ASSM. $129.95
Bare Board $29.95 Kit $119.95

DIMMER CONTROL



JBE Dimmer Control features: • 4 channels • 256 brightness levels • On-board power supply • Four 8 bit parallel input ports • Interfaces with JBE Solid State Switch & Apple II Parallel Interface.

80-146 ASSM. $89.95
Bare Board $25.95 Kit $79.95

POWER SUPPLIES

• Use wall transformers for safety • Protected against short circuit and thermal breakdown.

5 VOLT POWER SUPPLY

Rated at 5V 500MA • Operates JBE A-D & D-A Converter, Z80 & 6502 Microcomputers, 8085 & 8088 Microcomputers.

80-160 ASSM. $20.95
Bare Board $8.95 Kit $16.95

± 12 VOLT POWER SUPPLY

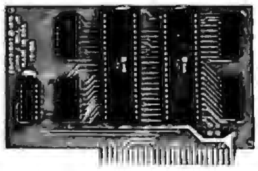
Rated at ± 12V 120MA • Can be used as a single 24V power supply • Ideally suited to OP-AMP experiments.

80-161 ASSM. $22.95
Bare Board $8.95 Kit $18.95

ICS

6502	$9.95
6522	$9.95
Z80	$9.95
Z80 PIO	$9.95
2716 5V	$19.95

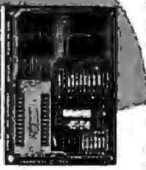
6522 APPLE II INTERFACE



• Interfaces printers, synthesizers, keyboards, JBE A-D & D-A Converter & Solid State Switches • Has handshaking logic, two 6522 VIAs & a 74LS74 for timing. Inputs & outputs are TTL compatible.

79-295 ASSM. $69.95
Bare Board $22.95 Kit $59.95

2716 EPROM PROGRAMMER



JBE 2716 EPROM Programmer was designed to program 5V 2716 EPROMS • It can also read 2716s. It interfaces to the Apple II using JBE Parallel I/O Card & four ribbon cable connectors • An LED indicates when power is being applied to the EPROM • A textool zero insertion force socket is used for the EPROM • Comes with complete doc. for writing and reading in the Apple II or Apple II+ • Cables available separately.

80-244 ASSM. $49.95
Bare Board $24.95 Kit $39.95

BARE BOARDS

APPLE II EXTENDER BOARD

3½" x 2½". Price includes 50 pin Apple Connector.

80-143 $12.95

8085 3 CHIP SYSTEM

State-of-the-art system using an 8085, 8156 & either an 8355 or 8755 • Instruction set 100% upward compatible with 8080A.

Bare Board $24.95

8088 5 CHIP SYSTEM

An 8086 family microcomputer system using an 8088 CPU, 8284, 8155, 8755A & an 8185.

Bare Board $29.95

CRT CONTROLLER

This intelligent CRT Controller is based on an 8085A Microprocessor & an 8275 Integrated CRT Controller. It features: • 25 lines, 80 characters/line • 5x7 dot matrix • Upper case only • Two 2716s • Serial Interface RS232 & TTL • Baud rates of 110, 150, 300, 600, 1200, 2400, 4800 & 9600 • Keyboard scanning system • Req's. unencoded keyboard • Uses +5V & ±12V power supplies.

Bare Board $39.95

50 pin connector	$5.95
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SN7480N	59	SN74196N	.85
SN7481N	1.10	SN74197N	.85
SN7482N	1.10	SN74198N	1.39
SN7483N	55	SN74199N	1.39
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CD4071	35	74C164	2 39
CD4072	35	74C173	2 59
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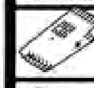
Proto Clips



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- Male, female, and children's voices
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- MICROBUS™ compatible

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- Symtex X-10 $349 00
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- NEW! Z-80 Softcard for APPLE CPM 2.2 & M BASIC 5.0 $325 00
- NEW! California Micro Products Keypad for APPLE $175 00

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2. RTR Stock Market Analysis – Hi-Res, TrendLines, etc $109 95
3. "Star Cruiser" – Apple II version of the number one arcade game, "Galaxy" $29 95
4. "Both Barrels" – Hi-Res simulation of Western Gunfight and Skeet Shooting. Same author as Nasir $29 95
5. "AppleTax Planner Package" $74 95
6. "New-DOS Tool Kit" $64 95
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MICROSOFT 16K ON A PLUG-IN CARD. $175

[illegible]

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[illegible]	55 00	Counseling Procedures	35 00	**Add-On Memory**	
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SINGLE BOARD COMPUTER SELECTION GUIDE

BOARD	PROCESSOR	ACP PRICE	ENCLOSURE	BOARD	PROCESSOR	ACP PRICE	ENCLOSURE
KIM-1	6502	169 00	Add 29 95	SC-SBC100	Z80	[illegible]	N/A
SYM-1	6502	239 00	Add 39 95	AIM 65	6502	[illegible]	Add 49 95
Cromemco	Z80	409 00	N/A	Cosmac Vip	1802	[illegible]	Inc

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TENNIS	ADVENTURE	SUB BATTLE
GOLF	CHECKERS	ARMOR BATTLE
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- Bank to select port address in software selectable
- Any 16K block can be made bank independent
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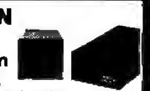
California Computer Systems

FLOPPY DISK CONTROLLER $400.

Z80 CPU BOARD $300.

TRS80 ADD-ON

The VISTA V-80 Disk Drive System



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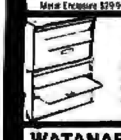

Siemens FDD 120-8 (2) VISTA Floppy Controller (S-100), Case, Power Supply & Cable CP/M Disk Operating System Assembled & Tested Walnut Wood Sides **$1499.00**

★ CHECK OUR FLOPPY DISK PRICING ON THIS PAGE ★

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Max pen speed 50 mm/sec, resolution .10 mm typically, 05 mm built in character generator sizes and 4 degrees of rotation, absolute draw, relative draw, alpha printing done with simple commands. **$1195.00**

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TAKE 10% OFF!

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SD200 Computer System w/64K	–	7995.00

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9602	Card Cage	75.00
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9604	Power Supply	275.00
9605	DC Input Power Supply	325.00
9610	Utility Proto Board	39.00
9611	Arith. Proc/Memory Module	495.00
9612	Buffered Utility Proto Board	49.00
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9620	16 Channel Parallel I/O Module	295.00
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9629A	32K Static RAM 200ns	895.00
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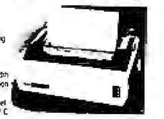

- 25 CPS printspeed
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- 130 printable columns
- 1/120 inch min. char. spacing
- 1/48 inch min. line spacing
- 1000 msec. return time
- 40 msec. line feed time
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- Multistrike fabric/black ribbon
- 96 print characters
- Standard 96 character wheel
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★ On board 2708 ★ 2708 included (450ns.)
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2517V	1.49	2529	1.49
2524V	1.49	2533	1.49

6502 SUPPORT CHIPS

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6522 Mult.	11.95
6530-002,003,004,005.	21.95
6532	19.95
6551	19.95

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2708 450 ns	6.25
2708-6 650 ns.	7.50
1702A	4.95
2732	74.95
2716-5V	14.95
2716-5V, 12V.	19.95
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4702	14.95
WD1941	9.95
COM 5016	16.95

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AY5-3600	13.75
HD0165	9.95
74C922	9.95
74C923	9.95

STATIC RAMS

SALE 2102 .89

	1-24	25-99	100
21L02 450ns	1.30	1.25	[illegible]
21L02 250ns	1.59	1.55	1.55
2111	3.75	3.65	3.55
2112-1	2.95	2.65	2.65
2101-1	2.90	2.70	2.55
2114L-250ns (4045)	6.90	5.95	5.50
2114L-450ns. (4045)	5.50	5.25	4.75
4044 250 ns	8.95	7.50	6.90
4044 450ns.	5.95	5.95	4.75
EMM4200A	9.75	8.75	7.95
EMM4402	7.95	7.25	6.25
AMD9140/41	10.95	10.25	9.25
AMD9130/31	12.95	11.95	10.25
1101	1.55	1.75	1.25
P2125/93425 (45ns)	9.95	8.35	8.25
6518 1K x 1 CMOS	7.95	7.95	7.25
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93415	9.95	9.95	8.50
TMS4046	11.95	10.95	10.50

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416/4116 16K (16 Pin)	8.75
Set of 8 416's	49.95
4115 8K (16 Pin)	6.95
4050 4K x 1 (18 Pin)	4.95
4060 4K x 1 (22 Pin)	4.95
4096 4K x 1 (16 Pin)	3.95
2104 4K x 1 (16 Pin)	4.75
4027 4K x 1 (16 Pin)	4.95

64K RAMS $159.95

5261	1.95	1103	1.95
5262	1.95	4008L	4.95
5270	4.95	6605	7.95
5280	4.95	6604	4.95
5290	12.45	6002	1.50

SOCKETS

# Pins	Lo-Pro Snapstrip	Wire Wrap 3 Level Tin	Wire Wrap 3 Level Gold
8	15	[illegible]	.45
14	19	36	59
16	20	38	62
18	24	59	84
20	29	69	99
22	24	79	1.10
24	38	85	1.20
28	43	1.10	1.49
36	58	1.25	1.69
40	60	1.40	[illegible]

ZERO INSERTION FORCE

16 Pin $5.50 24 Pin $7.50 40 Pin $10.25

LED READOUTS

Part No	Size	Color	Description	Price
DL704	300	Red	Comm Cathode	.99
DL707	300	Red	Comm Anode	.99
FND357	357	Red	Comm Cathode	.99
[illegible]	500	Red	Comm Cathode (+1)	.99
FND503 (500)	500	Red	Comm Cathode	.99
FND507 (510)	500	Red	Comm Anode	.99
FND508	500	Red	Comm Anode (+1)	.99
FND530	500	Green	Comm Cathode	1.49
FND550	500	Orange	Comm Cathode	1.49
FND800 (800)	800	Red	Comm Cathode	1.75
FND807 (810)	800	Red	Comm Anode	1.75
HP5082-7340	400	Red	4 x 7 Hexadecimal	20.95
HP5082-7300	400	Red	4 x 7 Sgl Digit Ampl	18.95
HP5082-7731	300	Red	Comm Anode	.75
TIL305	-	Red	Array 5 x 7	7.95
TIL308	270	Red	Numerical Display	16.95
TIL309	270	Red	Numerical Display	9.95
TIL311	270	Red	4 x 7 Hexadecimal	10.95
MAN2A	320	Red	Array	5.95
[illegible]	270	Red	Alpha Numeric	4.95
XAN3061	300	Red	Comm Anode Right DP	1.75
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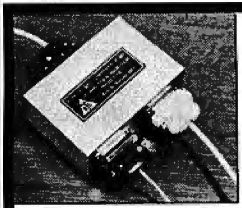

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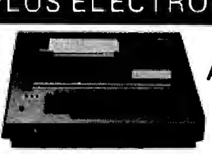

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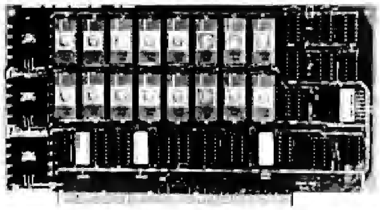

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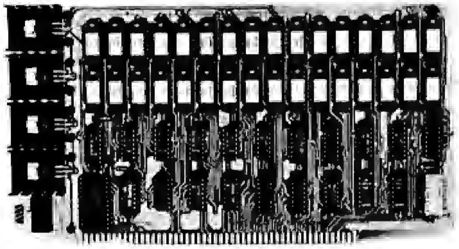

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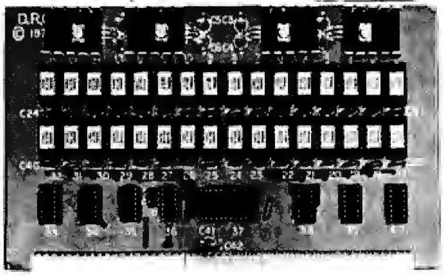

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page
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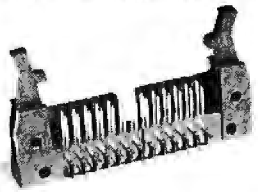
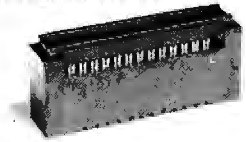


Pins	PC Mounting		Wire Wrap	
10	IDH10SR	.80	IDH10WR	1.75
20	IDH20SR	1.25	IDH20WR	2.75
26	IDH26SR	1.85	IDH26WR	3.60
34	IDS34SR	2.15	IDH34WR	4.15
40	IDH40SR	2.50	IDH40WR	4.90
50	IDH50SR	3.15	IDH50WR	6.15

EJECTOR EARS .25 EACH

CARD EDGE CONNECTORS

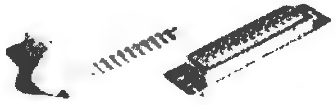


Pins	Part No.	
10	IDE10	3.25
20	IDE20	3.50
26	IDE26	4.05
34	IDE34	4.85
40	IDE40	5.65
50	IDE50	5.90

RIBBON CABLE

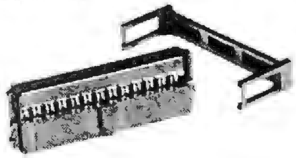
Conductors:	Solid Color		Color Coded	
	10 ft.	100 ft.	10 ft.	100 ft.
10	2.90	17.00	4.00	30.00
14	3.40	23.80	5.00	42.00
16	3.70	27.20	5.60	48.00
20	4.40	34.00	7.00	60.00
24	5.00	40.80	8.00	72.00
26	5.40	44.20	8.60	78.00
34	6.80	57.80	11.00	102.00
40	7.80	68.00	13.00	120.00
50	9.50	85.00	16.00	150.00

25 PIN "D" CONNECTORS



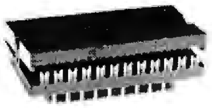
Style	Part #	
SOLDER STYLE		
Male	DB25P	.2.25
Female	DB255	3.00
Hood	DB25C	1.10
INSULATION DISPLACEMENT		
Male	IDC25P	4.95
Female	IDC255	5.25
Hood	IDC25C	1.35

SOCKETS



Pins	Part No.		Stain Relief
10	IDS10	1.25	.25
20	IDS20	2.02	.25
26	IDS26	2.65	.25
34	IDS34	3.50	.25
40	IDS40	4.05	.25
50	IDS50	5.06	.25

CABLE PLUGS



Pins	Part No.	
14	IDP14	1.25
16	IDP16	1.40
24	IDP24	2.25
40	IDP40	3.65

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Length	100/Bag	500/Bag	1K/Bag
2.5"	$1.25	$3.58	$ 6.19
3.0"	1.30	3.86	6.78
3.5"	1.37	4.15	7.37
4.0"	1.42	4.44	7.94
4.5"	1.48	4.74	8.54
5.0"	1.54	5.04	9.13
5.5"	1.58	5.38	9.72
6.0"	1.65	5.66	10.31
6.5"	$1.92	$6.44	$11.81
7.0"	1.99	6.76	12.44
7.5"	2.08	7.07	13.09
8.0"	2.14	7.38	13.73
8.5"	2.18	7.69	14.36
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9.5"	2.30	8.32	15.65
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500	3"	100	5½"
500	3½"	250	6"
500	4"	100	6½"
250	4½"	100	7"

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500	3½"	500	5½"
500	4"	500	6"

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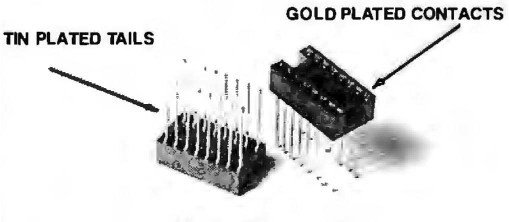

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20	21	.87	18.27
22	19	.94	17.86
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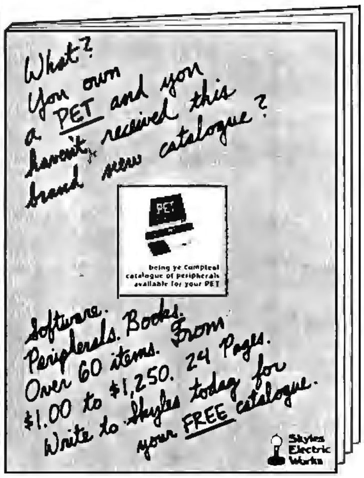

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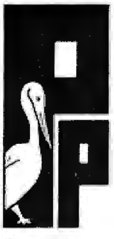

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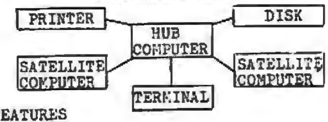

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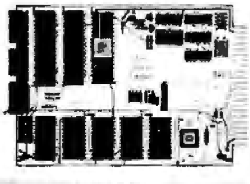

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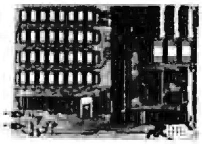

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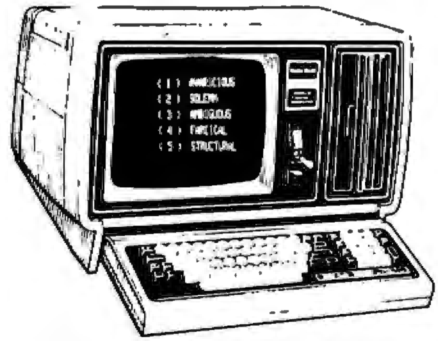

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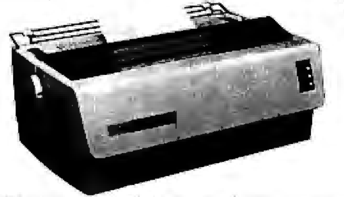

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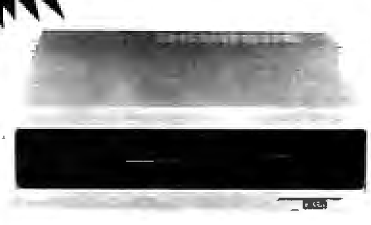

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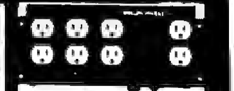

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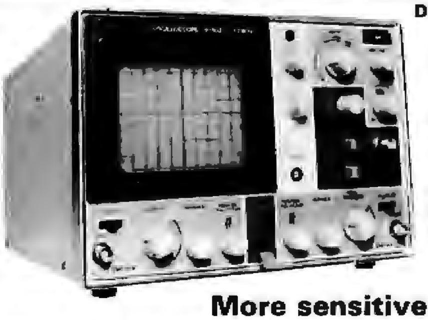

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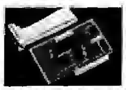

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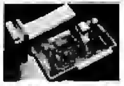

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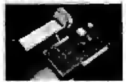

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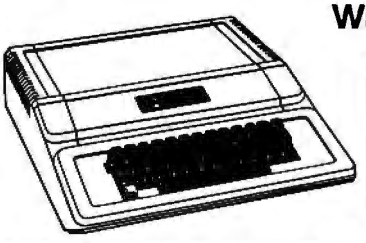

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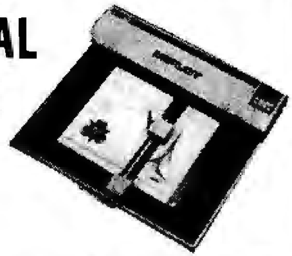

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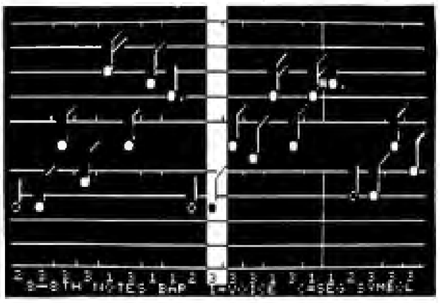

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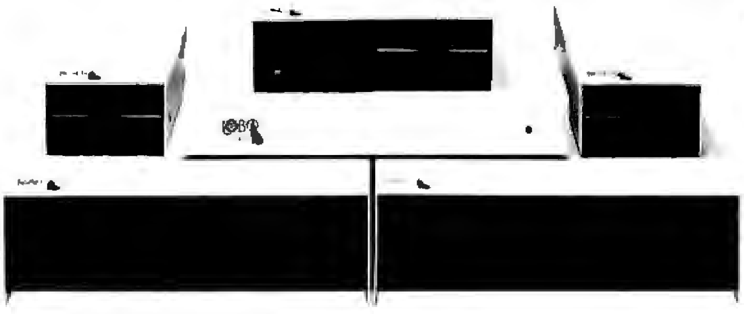

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CB-1A 8080 Processor Board. 2K of PROM 256 BYTE RAM power on/rest Vector Jump Parallel port with status. Kit $146.00 PCBD ... $31.95

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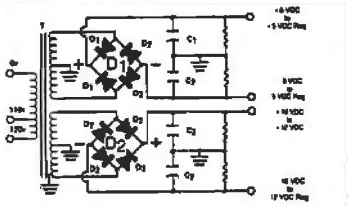

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T_1	1	0V, 110V, 120V	2 × 7.5A	2 × 2.5A	—	3¾" × 3⅝" × 3⅛"	21.95
T_2	2	0V, 110V, 120V	2 × 12.5A	2 × 3.5A	—	3¾" × 4⅜" × 3⅛"	27.95
T_3	3	0V, 110V, 120V	2 × 9A	2 × 2.5A	2 × 2.5A	3¾" × 4⅜" × 3⅛"	29.95
T_4	4	0V, 110V, 120V	2 × 4A	(28V, CT)	48V, CT, @3A	3¾" × 3⅝" × 3⅛"	22.95
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POWER SUPPLY KITS (OPEN FRAME WITH BASE PLATE, 3 HRS. ASSY. TIME)

ITEM	USED FOR	@ + 8 Vdc	@ − 9 Vdc	@ + 16 Vdc	@ − 16 Vdc	@ + 28 Vdc	SIZE W × D × J	UNIT PRICE
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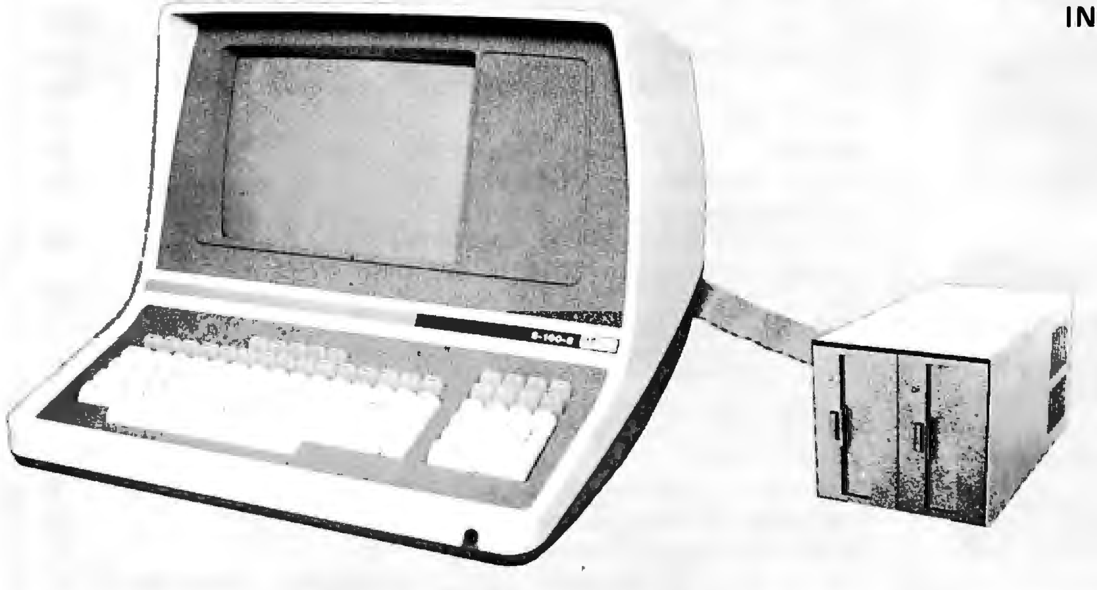

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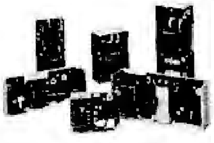

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S-100 CARD EXTENDER

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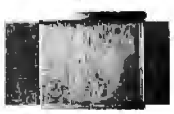
(Gold Contacts)

As long as there is a price war, we will fight your battle. Compare at your local Dept. store and buy U$ MICRO.



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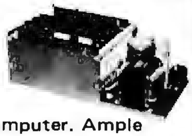

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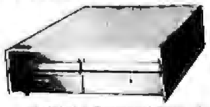


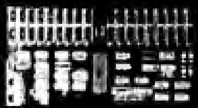
2 SHUGART 801R
POWER SUPPLY

If this looks like a Lobo Drive System, don't be fooled. Just because it looks like one, works like one, smells like one, and tastes like one (?) doesn't mean It has to cost like one!

EXPANDABLE RAM

★SPECIAL★SPECIAL★SPECIAL★

This is the best all around 64K board you can buy. If after you see it, you don't agree return for full refund. Bank Select by extended address lines or I.O. 40H.



★$389.00 A&T★

S-100 POWER

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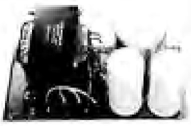
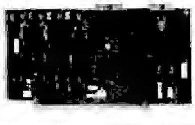
Simple Brute Force!
S-100 Power Supply,
30A @ +8V,
6A @ +16V,
6A @ –16V,
PC Board Design.



Z-80 CPU (KIT)



The first time this world popular CPU offered in Kit. 2 serial, 3 parallel, CTC, EProm Z-80 at 4 mhz. Software buad rate, etc. (less Prom & cable) **$212.00**

12 SLOT MOTHER

We have connectors and power supply too. Start your system with quality components. Terminated.

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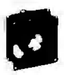

3-1/8"

4-5/8"

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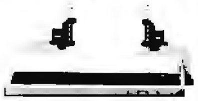
4116s

$3.75

Expansion 16K Dynamic RAMs for Apple, TRS-80 S-100 systems. T.I., Mostek Intel, Call for manufacturer.

200 NS

DIP-80 $399.00



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200 NS

TMS-4044
MM-5257
INTEL 2147

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2716s **$9.50** (450 NS)
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SN7409N	.29
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SN7440N	.20
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SN7443N	1.10
SN7444N	1.10
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SN7473N	.35
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SN7485N	.89
SN7486N	.35
SN7489N	1.75
SN7490N	.49
SN7491N	.59
SN7492N	.45
SN7493N	.45
SN7494N	.69
SN7495N	.69
SN7496N	.69
SN7497N	3.00
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SN74107N	.35
SN74109N	.39
SN74116N	1.95
SN74121N	.39
SN74122N	.55
SN74123N	.59
SN74125N	.49
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SN74143N	3.49
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SN74198N	1.49
SN74199N	1.49
SN74221N	1.25
SN74251N	.99
SN74276N	1.95
SN74279N	.79
SN74283N	1.49
SN74284N	3.95
SN74285N	3.95
SN74365N	.69
SN74366N	.69
SN74367N	.69
SN74368N	.69
SN74390N	1.49
SN74393N	1.49

74LS

74LS00	.29
74LS01	.29
74LS02	.29
74LS03	.29
74LS04	.35
74LS05	.35
74LS08	.29
74LS09	.35
74LS10	.29
74LS11	.75
74LS12	.35
74LS13	.59
74LS14	.99
74LS15	.35
74LS20	.29
74LS21	.35
74LS22	.35
74LS26	.35
74LS27	.35
74LS28	.35
74LS30	.29
74LS32	.35
74LS33	.59
74LS37	.45
74LS38	.49
74LS40	.35
74LS42	.89
74LS47	.89
74LS48	1.15
74LS49	1.15
74LS51	.29
74LS54	.29
74LS55	.29
74LS73	.45
74LS74	.45
74LS75	.59
74LS76	.45
74LS78	.49
74LS83	.89
74LS85	1.25
74LS86	.45
74LS90	.59
74LS92	.75
74LS93	.75
74LS95	.99
74LS96	1.15
74LS107	.45
74LS109	.45
74LS112	.45
74LS113	.49
74LS114	.49
74LS122	.89
74LS123	1.25
74LS125	.89
74LS126	.55
74LS132	.99
74LS133	.89
74LS136	.49
74LS138	.89
74LS139	.89
74LS151	.89
74LS153	.89
74LS154	1.75
74LS155	1.19
74LS156	1.19
74LS157	.89
74LS158	.99
74LS160	1.15
74LS161	1.15
74LS162	1.15
74LS163	1.15
74LS164	1.25
74LS165	1.25
74LS168	1.19
74LS169	1.19
74LS170	2.49
74LS173	1.39
74LS174	.99
74LS175	.99
74LS181	2.95
74LS190	1.25
74LS191	1.25
74LS192	1.15
74LS193	1.15
74LS194	1.15
74LS195	1.15
74LS197	1.19
74LS221	1.19
74LS240	1.95
74LS241	1.95
74LS242	1.95
74LS243	1.95
74LS244	1.95
74LS245	2.95
74LS247	1.19
74LS248	1.19
74LS249	1.19
74LS251	1.49
74LS253	.99
74LS257	.89
74LS258	.99
74LS260	.69
74LS266	.69
74LS273	1.95
74LS279	.75
74LS283	1.09
74LS290	.99
74LS293	.99
74LS298	1.25
74LS352	1.29
74LS353	1.29
74LS365	.75
74LS366	.75
74LS367	.75
74LS368	.75
74LS373	1.95
74LS374	1.95
74LS375	.89
74LS386	.69
74LS393	2.49
74LS399	2.49
74LS670	2.49
81LS95	1.95
81LS97	1.95

74S

74S00	.50
74S02	.50
74S03	.50
74S04	.55
74S05	.55
74S08	.50
74S09	.50
74S10	.50
74S11	.50
74S15	.50
74S20	.50
74S22	.50
74S30	.50
74S32	.55
74S40	.55
74S51	.50
74S64	.50
74S65	.50
74S74	.79
74S86	.79
74S112	.79
74S113	.79
74S114	.79
74S133	.55
74S134	.69
74S135	1.19
74S136	1.75
74S138	1.35
74S139	1.35
74S140	1.15
74S151	1.35
74S153	1.35
74S157	1.35
74S158	1.35
74S174	1.59
74S175	1.59
74S188	4.95
74S194	1.95
74S195	1.95
74S196	3.95
74S240	2.95
74S241	2.95
74S242	3.25
74S243	3.25
74S244	3.25
74S251	1.45
74S253	1.45
74S257	1.35
74S258	1.35
74S260	.79
74S280	2.95
74S287*	4.95
74S288*	4.95
74S373	3.49
74S374	3.49
74S387*	5.95
74S471*	19.95
74S472*	19.95
74S473*	19.95
74S474*	21.95
74S475*	21.95
74S570*	7.95
74S571*	7.95
74S572*	19.95
74S573*	19.95
74S940	3.15
74S941	3.15

* LIMITED AVAILABILITY ON THESE PROMS

CA—LINEAR

CA3013H	2.15
CA3023H	3.25
CA3039H	1.35
CA3046N	1.30
CA3059N	3.25
CA3060N	3.25
CA3080H	1.25
CA3081N	2.00
CA3082N	2.00
CA3083N	1.60
CA3086N	.85
CA3089N	3.75
CA3096N	3.95
CA3130H	1.39
CA3140H	1.25
CA3160H	1.25
CA3401N	.59
CA3600N	3.50

CD—CMOS

CD4000	.39
CD4001	.39
CD4002	.39
CD4006	1.19
CD4007	.25
CD4009	.49
CD4010	.49
CD4011	.39
CD4012	.25
CD4013	.49
CD4014	1.39
CD4015	1.19
CD4016	.59
CD4017	1.19
CD4018	.99
CD4019	.49
CD4020	1.19
CD4021	1.39
CD4022	1.19
CD4023	.29
CD4024	.79
CD4025	.23
CD4026	2.95
CD4027	.69
CD4028	.89
CD4029	1.49
CD4030	.49
CD4035	.99
CD4040	1.49
CD4041	1.49
CD4042	.99
CD4043	.89
CD4044	.89
CD4046	1.79
CD4047	2.50
CD4048	1.35
CD4049	.49
CD4050	.69
CD4051	1.19
CD4052	1.19
CD4053	1.19
CD4056	2.95
CD4059	9.95
CD4060	1.49
CD4066	.79
CD4068	.39
CD4069	.45
CD4070	.55
CD4071	.49
CD4072	.49
CD4073	.39
CD4075	.39
CD4076	1.39
CD4081	.39
CD4082	.39
CD4093	.99
CD4098	2.49
CD4506	.75
CD4507	.99
CD4508	3.95
CD4510	1.39
CD4511	1.29
CD4514	3.95
CD4515	2.95
CD4516	1.49
CD4518	1.79
CD4519	.89
CD4520	1.29
CD4526	1.79
CD4528	1.79
CD4529	1.95
CD4543	2.79
CD4562	11.95
CD4566	2.79
CD4583	2.49
CD4723	1.95
CD4724	1.95
MC14409	14.95
MC14410	14.95
MC14411	14.95
MC14412	11.95
MC14419	4.95
MC14433	13.95

LITRONIX DISPLAY SALE

LIMITED OFFER!!!

WHILE THEY LAST!!!

DL-4500
DL-4507
DL-4520A
DL-4120A

DL-2300
DLG-2535

DL-4509

DL-6500
DL-6530

DL-3130

MULTI DIGIT REFLECTOR ARRAYS FOR CLOCKS

PART NUMBER	CHAR HT (IN.)	POLARITY	DESCRIPTION	LIGHT OUTPUT (MCD) TYP	LIGHT OUTPUT (MCD) MIN	LIGHT OUTPUT (MCD) @mA	FORWARD VOLTAGE SEGMENT (V) I_F = 20mA TYP	FORWARD VOLTAGE SEGMENT (V) I_F = 20mA MAX	CONTINUOUS FORWARD CURRENT PER SEGMENT (mA) MAX	PRICE
DL-4500 (Red) DL-4507 (Red)	.50	C.C. MPX	4 Digit 7 Segment With Colon And Auxiliary Indicators	.8	.5 1.0	10	1.7	2.0	30	2.49 2.49
DLO-4507 (orng) DLG-4507 (grn) DL-4520A (red)		C.C. non MPX		.8	.5					4.95 4.95 2.49
DL-4120A (red)	1.0	C.C. non MPX		1.5	1		3.4	4.0		4.95

MULTI DIGIT REFLECTOR ARRAYS

DL-2300 (Red)	.30	C.C. MPX	7 Seg. 2 Digit D.P. Right	.35	1.5	20	1.7	2.0	30	.99
DLG-2535 (green)	.50	C.A. MPX	8 Seg. 2 Digit		2.5	20		3.5	35	1.49
DL-4509 (Red)	.50	C.C. MPX	8 Seg. 4 Digit D.P. Right	.8	.5	10	1.7	2.0	30	2.49
DL-6500 (Red)	.50	C.C. MPX	7 Seg. 6 Digit D.P. Right	.8	.5	10	1.7	2.0	30	2.95
DL-6530 (Red)	.50	C.A. MPX	7 Seg. 6 Digit D.P. Right	.8	.5	10	1.7	2.0	30	2.95
DL-3130 (Red)	1.0	C.A. MPX	7 Seg. 3 Digit D.P. Right	1.5	1.0	10	3.4	4.0	30	3.95

DISCRETE LEDS

XC556R	.200"	red	5/$1
XC556G	.200"	green	4/$1
XC556Y	.200"	yellow	4/$1
XC556C	.200"	clear	4/$1
XC22R	.200"	red	5/$1
XC22G	.200"	green	4/$1
XC22Y	.200"	yellow	4/$1
MV10B	.170"	red	4/$1
MV50	.085"	red	6/$1
XC209R	.125"	red	5/$1
XC209G	.125"	green	4/$1
XC209Y	.125"	yellow	4/$1
XC526R	.185"	red	5/$1
XC526G	.185"	green	4/$1
XC526Y	.185"	yellow	4/$1
XC526C	.185"	clear	4/$1
XC111R	.190"	red	5/$1
XC111G	.190"	green	4/$1
XC111Y	.190"	yellow	4/$1
XC111C	.190"	clear	4/$1

XC114 RED LED, METAL MTG. HDW. 1.8" LEADS

RL-2 . . $.39 ea. or 3/$1.00

DISPLAY LEDS

C.A. — Common Anode

C.C. — Common Cathode

Type	Polarity	Ht	Price	Type	Polarity	Ht	Price
MAN 1	C.A.—red	.270	2.95	DLG507	C.A.—green	.500	1.25
MAN 2	5x7 D.M.—red	.300	4.95	DL704	C.C.—red	.300	1.25
MAN 3	C.C.—red	.125	.25	DL707	C.A.—red	.300	1.25
MAN 52	C.A.—green	.300	1.25	DL728	C.C.—red	.500	1.49
MAN 54	C.C.—green	.300	1.25	DL741	C.A.—red	.600	1.25
MAN 71	C.A.—red	.300	.75	DL746	C.A.—red ± 1	.630	1.49
MAN 72	C.A.—red	.300	.75	DL747	C.A.—red	.600	1.49
MAN 74	C.C.—red	.300	1.25	DL750	C.C.—red	.600	1.49
MAN82	C.A.—yellow	.300	.49	DLD847	C.A.—orange	.800	1.49
MAN 84	C.C.—yellow	.300	.99	DLO850	C.C.—orange	.800	1.49
MAN 3620	C.A.—orange	.300	.49	DL33B	C.C.—red	.110	.35
MAN 3630	C.A.—orange ± 1	.300	.99	FND358	C.C. ± 1	.357	.99
MAN 3640	C.C.—orange	.300	.99	FND359	C.C.	.357	.75
MAN 4610	C.A.—orange	.400	.99	FND503	C.C. (FND500)	.500	.99
MAN 6610	C.A.—orange—DD	.560	.99	FND507	C.A. (FND510)	.500	.99
MAN 6630	C.A.—orange ± 1	.560	.99	HDSP-3401	C.A.—red	.800	1.50
MAN 6640	C.C.—orange—DD	.560	.99	HDSP-3403	C.C.—red	.800	1.50
MAN 6650	C.C.—orange ± 1	.560	.99	5082-7751	C.A.,R.H.D.—red	.430	1.25
MAN 6660	C.A.—orange	.560	.99	5082-7760	C.C.,R.H.D.—red	.430	1.75
MAN 6710	C.A.—red—DD	.560	.99	5082-7300	4x7sgl.dig. RHD	.600	22.00
MAN 6750	C.C.—red ± 1	.560	.99	5082-7302	4x7sgl. dig. LHD	.600	22.00
MAN 6780	C.C.—red	.560	.99	5082-7304	Overnge. char.(±1)	.600	19.95
DLD304	C.C.—orange	.300	1.25	4N28	Photo XsistorOpto-Isol.		.99
DLD307	C.A.—orange	.300	1.25	LIT-1	Photo Xsistor Opto-Isol.		.69
DLG500	C.C.—green	.500	1.25	MOC3010	Optically Isol. Triac Driver		1.25

POTENTIOMETERS

$2.95 each

2 Watt @ 70°C ± 10%
7/8" Slotted Shaft
Linear Taper
Meets Mil-R-94

Part No.		
CMU 1021	RV4NAY SD - 102A	1K
CMU 5021	RV4NAY SD - 502A	5K
CMU 1031	RV4NAY SD - 103A	10K
CMU 2531	RV4NAY SD - 253A	25K
CMU 5031	RV4NAY SD - 503A	50K
CMU 1041	RV4NAY SD - 104A	100K
CMU 1052	RV4NAY SD - 105A	1Meg

$1.35 each

3/4 Watt @ 70°C
15 turn pot. Linear taper. Printed circuit mount.

Part No.	Part No.	Part No.
830P- 50ohm	830P- 5K	830P-100K
830P-100ohm	830P-10K	830P-200K
830P-500ohm	830P-20K	830P-500K
830P-1K	830P-50K	830P-1Meg
830P-2K		

LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100
8 pin LP	.17	.16	.15
14 pin LP	.20	.19	.18
16 pin LP	.22	.21	.20
18 pin LP	.29	.28	.27
20 pin LP	.34	.32	.30
22 pin LP	.37	.36	.35
24 pin LP	.38	.37	.36
28 pin LP	.45	.44	.43
36 pin LP	.60	.59	.58
40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100
14 pin ST	.27	.25	.24
16 pin ST	.30	.27	.25
18 pin ST	.35	.32	.30
24 pin ST	.49	.45	.42
28 pin ST	.99	.90	.81
36 pin ST	1.39	1.26	1.15
40 pin ST	1.59	1.45	1.30

SOLDERTAIL (GOLD) STANDARD

	1-24	25-49	50-100
8 pin SG	.39	.35	.31
14 pin SG	.49	.45	.41
16 pin SG	.54	.49	.44
18 pin SG	.59	.53	.48
24 pin SG	.79	.75	.69
28 pin SG	1.10	1.00	.90
36 pin SG	1.65	1.40	1.26
40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100
8 pin WW	.59	.54	.49
10 pin WW	.69	.63	.58
14 pin WW	.79	.73	.67
16 pin WW	.85	.77	.70
18 pin WW	.99	.90	.81
20pin WW	1.19	1.08	.99
22 pin WW	1.49	1.35	1.23
24 pin WW	1.39	1.26	1.14
28 pin WW	1.69	1.53	1.38
36 pin WW	2.19	1.99	1.79
40 pin WW	2.29	2.09	1.89

1/4 WATT RESISTOR ASSORTMENTS – 5%

ASST. 1	5ea.	10 Ohm 12 Ohm 15 Ohm 18 Dhm 22 Ohm 27 Ohm 33 Ohm 39 Ohm 47 Ohm 56 Ohm	50pcs.	$1.95
ASST. 2	5ea.	68 Ohm 82 Ohm 100 Ohm 120 Ohm 150 Ohm 180 Ohm 220 Ohm 270 Dhm 330 Ohm 390 Ohm	50pcs.	$1.95
ASST. 3	5ea.	470 Dhm 560 Ohm 680 Ohm 820 Ohm 1K 1.2K 1.5K 1.8K 2.2K 2.7K	50pcs.	$1.95
ASST. 4	5ea.	3.3K 3.9K 4.7K 5.6K 6.8K 8.2K 10K 12K 15K 18K	50pcs.	$1.95
ASST. 5	5ea.	22K 27K 33K 39K 47K 56K 68K 82K 100K 120K	50pcs.	$1.95
ASST. 6	5ea.	150K 180K 220K 270K 330K 390K 470K 560K 680K 820K	50pcs.	$1.95
ASST. 7	5ea.	1M 1.2M 1.5M 1.8M 2.2M 2.7M 3.3M 3.9M 4.7M 5.6M	50pcs.	$1.95
ASST. 8R		Includes Resistor Assts. 1-7 (350 pcs.)		$10.95 ea.

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INTERSIL

Part No.	Function	Price
7045IPI	CMOS Precision Timer	14.95
7045EV/Kit*	Stopwatch Chip, XTL	22.95
7106CPL	3½ Digit A/D (LCD Drive)	16.95
7106EV/Kit*	IC, Circuit Board, Display	34.95
7107CPL	3½ Digit A/D (LED Drive)	15.95
7107EV/Kit*	IC, Circuit Board, Display	28.95
7116CPL	3½ Digit A/D LCD Dis. HLD.	18.95
7117CPL	3½ Digit A/D LED Dis. HLD.	17.95
7201IDR	Low Battery Volt Indicator	2.25
7205IPG	CMOS LED Stopwatch/Timer	12.95
7205EV/Kit*	Stopwatch Chip, XTL	19.95
7206CJPE	Tone Generator	5.15
7206CEV/Kit*	Tone Generator Chip, XTL	9.95
7207AIPD	Oscillator Controller	6.50
7207AEV/Kit*	Freq. Counter Chip, XTL	11.10
7208IPI	Seven Decade Counter	17.95
7209IPA	Clock Generator	3.95
7215IPG	4 Func. CMOS Stopwatch CKT	13.95
7215EV/Kit*	4 Func. Stopwatch Chip, XTL	19.95
7216AIJI	8-Digit Univ. Counter C.A.	32.00
7216CIJI	8-Digit Freq. Counter C.A.	26.95
7216DIPI	8-Digit Freq. Counter C.C.	21.95
7217IJI	4-Digit LED Up/Down Counter	12.95
7218CIJI	8-Digit Univ. LED Drive	10.95
7224IPL	LCD 4½ Digit Up Counter DRI	11.25
7226AIJL	8-Digit Univ. Counter	31.95
7226AEV/Kit*	5 Function Counter Chip, XTL	74.95
7240IJE	CMOS Bin Prog. Timer/Counter	4.95
7242IJA	CMOS Divide-by-256 RC Timer	2.05
7250IJE	CMOS BCD Prog. Timer/Counter	6.00
7260IJE	CMOS BCD Prog. Timer/Counter	5.25
7555IPA	CMOS 555 Timer (8 pin)	1.45
7556IPD	CMOS 556 Timer (14 pin)	2.20
7611BCPA	CMOS Op Amp Comparator 5MV	2.25
7612BCPA	CMOS Op Amp Ext. Cmvr. 5MV	2.95
7621BCPA	CMOS Dual Op Amp Comp. 5MV	3.95
7631CCPE	CMOS Tri Op Amp Comp. 10MV	5.35
7641CCPD	CMOS Quad Op Amp Comp. 10MV	7.50
7642CCPD	CMOS Quad Op Amp Comp. 10MV	7.50
7660CPA	Voltage Converter	2.95
8069CCQ	50ppm Band—GAP Volt Ref. Diode	2.50
8211CPA	Volt Ref/Indicator	2.50
8212CPA	Volt Ref/Indicator	2.50

* INTERSIL'S EVALUATION KITS

74C

74C00	.39
74C02	.39
74C04	.39
74C08	.39
74C10	.39
74C14	.75
74C20	.39
74C30	.39
74C42	1.39
74C48	1.95
74C73	.79
74C74	.79
74C85	1.95
74C86	.99
74C89	6.95
74C90	1.29
74C93	1.29
74C95	1.59
74C106	.75
74C107	1.89
74C151	2.95
74C154	3.95
74C157	2.25
74C160	1.69
74C161	1.60
74C162	1.49
74C163	1.69
74C164	1.59
74C173	1.39
74C174	1.39
74C175	1.39
74C192	1.69
74C193	1.69
74C195	1.59
74C221	1.95
74C240	2.25
74C244	2.25
74C373	2.49
74C374	2.59
74C901	.89
74C903	1.15
74C911	10.95
74C912	10.95
74C915	1.69
74C917	10.95
74C922	5.49
74C923	5.75
74C925	7.50
74C926	7.50
80C95	.79
80C97	.79

LINEAR

LH0002CN	6.85
LM10CLH	4.50
LM11CLH	4.75
LH0070-0H	6.05
TL071CP	.79
TL072CP	1.39
TL074CN	2.49
LH0082CD	35.80
TL082CP	1.19
TL084CN	2.19
LH0094CD	36.80
LM300H	.99
LM301CN	.35
LM302H	1.95
LM304H	1.95
LM305H	.99
LM307CN	.45
LM308CN	1.00
LM309H	1.95
LM309K	1.25
LM310CN	1.75
LM311H	.90
LM312H	2.49
LM317MP	1.15
LM317T	1.75
LM317K	3.95
LM318CN	1.95
LM319N	1.95
LM320K-5	1.35
LM320K-12	1.35
LM320K-15	1.35
LM320T-5	1.25
LM320T-12	1.25
LM320T-15	1.25
LM323K-5	5.95
LM324N	.99
LM329DZ	.65
LM331N	3.95
LM334Z	1.30
LM335Z	1.40
LM336Z	1.75
LM337T	1.95
LM337MP	1.15
LM338K	6.95
LM339N	.99
LM340K-5	1.35
LM340K-12	1.35
LM340K-15	1.35
LM340T-5	1.25
LM340T-12	1.25
LM340T-15	1.25
LM341P-5	.75
LM341P-12	.75
LM341P-15	.75
LM342P-5	.69
LM342P-12	.69
LM342P-15	.69
LM348N	1.25
LM350K	5.75
LF351N	.60
LF353N	1.00
LF355N	1.10
LF356N	1.10
LM358N	1.00
LM359N	1.79
LM370N	4.49
LM373N	3.25
LM377N	2.95
LM380N	1.25
LM381N	1.95
LM382N	1.79
LM384N	1.95
LM386N-3	1.29
LM387N	1.45
LM389N	1.35
LM392N	.69
LF398N	4.00
LM399H	5.00
TL494CN	4.49
TL496CP	1.75
NE510A	6.00
NE529A	4.95
NE531H	3.95
NE536H	6.00
NE540H	6.00
NE544N	4.95
NE550A	1.30
NE555V	.39
LM556N	.99
NE564N	3.95
LM565N	1.25
LM566CN	1.95
LM567V	1.25
NE570N	4.95
LM702H	.79
LM703CN	.89
LM709N	.29
LM710N	.79
LM711N	.79
LM723N	.69
LM733N	1.00
LM739N	1.19
LM741CN	.35
MC1741SCG	3.00
LM747N	.79
LM748N	.59
LM1014N	2.75
LM1310N	1.95
LM1458CN	.59
LM1488N	1.25
LM1489N	1.25
LM1496N	1.95
LM1556V	1.75
LM1800N	2.95
LM1877N-9	3.25
LM1889N	3.20
LM1896N	1.75
LM2002T	1.49
LM2877P	2.05
LM2878P	2.25
LM2896P-1	2.25
LM3189N	2.95
LM3900N	.69
LM3905CN	1.25
LM3909N	1.15
LM3914N	3.95
LM3915N	3.95
LM3916N	3.95
RC4136N	1.25
RC4151NB	3.95
RC4194TK	5.95
RC4195TK	5.49
KB4428	4.25
KB4429	5.95
LM4500A	3.25
ICL8038B	4.95
LM13080N	1.29
LM13600N	1.49
75138N	1.95
75450N	.89
75451CN	.39

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

Value	1-9	10-99	100+	Value	1-9	10-99	100+
10 pf	.08	.06	.05	.001µF	.08	.06	.05
22 pf	.06	.06	.05	.0047µF	.08	.06	.05
47 pf	.06	.06	.05	.01µF	.08	.06	.05
100 pf	.08	.06	.05	.022µF	.09	.07	.06
220 pf	.06	.06	.05	.047µF	.09	.07	.06
470 pf	.06	.06	.05	.1µF	.15	.12	.10

100 VOLT MYLAR FILM CAPACITORS

.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022mf	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+20% DIPPED TANTALUMS (Solid) CAPACITORS

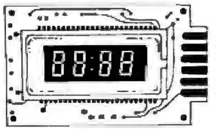
.1/35V	.39	.34	.29	1.5/35V	.41	.37	.29
.15/35V	.39	.34	.29	2.2/35V	.51	.45	.34
.22/35V	.39	.34	.29	3.3/25V	.53	.47	.37
.33/35V	.39	.34	.29	4.7/25V	.63	.56	.45
.47/35V	.39	.34	.29	6.8/25V	.79	.69	.55
.68/35V	.39	.34	.29	15/25V	1.39	1.25	.95
1.0/35V	.39	.34	.29	22/6V	.79	.69	.55

MINI. ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead				Radial Lead			
.47/50V	.16	.14	.10	.47/25V	.15	.13	.12
1.0/50V	.19	.16	.12	.47/50V	.16	.14	.13
3.3/50V	.17	.16	.11	1.0/16V	.15	.13	.12
4.7/25V	.18	.15	.11	1.0/25V	.16	.14	.13
10/25V	.18	.15	.11	1.0/50V	.17	.15	.14
10/50V	.19	.16	.12	4.7/16V	.15	.13	.12
22/25V	.19	.16	.12	4.7/25V	.16	.14	.13
22/50V	.24	.20	.18	4.7/50V	.17	.15	.14
47/25V	.25	.21	.19	10/16V	.15	.13	.12
47/50V	.29	.25	.23	10/25V	.16	.14	.13
100/25V	.28	.24	.22	10/50V	.17	.15	.14
100/50V	.41	.37	.34	47/50V	.25	.21	.19
220/25V	.39	.34	.33	100/16V	.21	.17	.14
220/50V	.49	.45	.41	100/25V	.25	.23	.21
470/25V	.54	.49	.45	100/50V	.37	.34	.31
1000/16V	.79	.69	.61	220/16V	.25	.21	.19
2200/16V	.89	.79	.69	470/25V	.35	.31	.27

Circle 328 on inquiry card.

National Semiconductor Clock Modules



12VDC
AUTOMOTIVE/
INSTRUMENT
CLOCK

APPLICATIONS:
- In-dash auto clocks
- After-market auto/RV clocks
- Aircraft-marine clks.
- 12VDC oper. instru.
- Portable/battery powered instrumnts.

Features: Bright 0.3" green display. Internal crystal time-base. ± 0.5 sec./day accur. Auto. display brightness control logic. Display color filterable to blue, blue-green, green & yellow. Complete—just add switches and lens.

MA 1003 Module $16.95

MA1023 .7" Low Cost Digital LED Clock Module	8.95
MA1026 .7" Dig. LED Alarm Clock/Thermometer	18.95
MA5036 .3" Low Cost Digital LED Clock/Timer	6.95
MA1002 .5" LED Display Dig. Clock & Xformer	9.95

National Semiconductor

RAM SALE

MM5290N-4 (MK4116/UPD416) . . **$4.95 each**
16K DYNAMIC RAM (250NS)
(8 EACH $39.95) (100 EACH $450.00/lot)

MM5290J-2 (MK4116/UPD416) . . **$6.95 each**
16K DYNAMIC RAM (150NS)
(8 EACH $49.95) (100 EACH $550.00/lot)

MM5298J-3A .... **$3.25 each**
8K DYNAMIC RAM (LOW HALF OF MM5290J) 200NS
(8 EACH $23.95) (100 EACH $250.00/lot)

MM2114-3 .... **$5.95 each**
4K STATIC RAM (300NS)
(8 EACH $43.95) (100 EACH $450.00/lot)

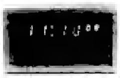
MM2114L-3 .... **$6.25 each**
4K STATIC RAM (LOW POWER 300NS)
(8 EACH $44.95) (100 EACH $475.00/lot)

EPROM Erasing Lamp

- Erases 2708, 2716, 1702A, 5203Q, 5204Q, etc.
- Erases up to 4 chips within 20 minutes.
- Maintains constant exposure distance of one inch.
- Special conductive foam liner eliminates static build-up.
- Built-in safety lock to prevent UV exposure.
- Compact — only 7-5/8" x 2-7/8" x 2"
- Complete with holding tray for 4 chips.

UVS-11E $79.95

Jumbo 6-Digit Clock Kit



- Four .630"ht. and two .300"ht. common anode displays
- Uses MM5314 clock chip
- Switches for hours, minutes and hold functions
- Hours easily viewable to 30 feet
- Simulated walnut case
- 115VAC operation
- 12 or 24 hour operation
- Includes all components, case and wall transformer
- Size: 6¾" x 3-1/8" x 1¾"

JE747 .... $29.95

6-Digit Clock Kit

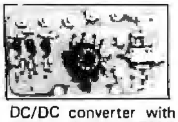
- Bright .300 ht. comm. cathode display
- Uses MM5314 clock chip
- Switches for hours, minutes and hold modes
- Hrs. easily viewable to 20 ft.
- Simulated walnut case
- 115 VAC operation
- 12 or 24 hr. operation
- Incl. all components, case & wall transformer
- Size: 6¾" x 3-1/8" x 1¾"

JE701 .... $19.95

Regulated Power Supply

Uses LM309K. Heat sink provided. PC board construction. Provides a solid 1 amp @ 5 volts. Can supply up to ±5V, ±9V and ±12V with JE205 Adapter. Includes components, hardware and instructions. Size: 3½" x 5" x 2"H

JE200 .... $14.95



ADAPTER BOARD —Adapts to JE200— ±5V, ±9V and ±12V

DC/DC converter with +5V input. Toriodal hi-speed switching XFMR. Short circuit protection. PC board construction. Piggy-back to JE 200 board. Size: 3½" x 2" x 9/16"H

JE205 .... $12.95

MICROPROCESSOR COMPONENTS

8080A/8080A SUPPORT DEVICES

INS8080A	CPU	6.50
DP8212	8-Bit Input/Output	3.25
DP8214	Priority Interrupt Control	5.95
DP8216	Bi-Directional Bus Driver	3.49
DP8224	Clock Generator/Driver	[illegible]
DP8226	Bus Driver	[illegible]
DP8228	System Controller/Bus Driver	4.95
DP8238	System Controller	5.95
INS8243	I/O Expander for 48 Series	9.95
INS8250	Asynchronous Comm. Element	16.95
DP8251	Prog. Comm. I/O (USART)	7.95
DP8253	Prog. Interval Timer	14.95
DP8255	Prog. Peripheral I/O (PPI)	9.95
DP8257	Prog. DMA Control	19.95
DP8259	Prog. Interrupt Control	14.95
DP8275	Prog. CRT Controller	49.95
DP8279	Prog. Keyboard/Display Interface	19.95
DP8300	Octal Bus Receiver	6.95
DP8303	System Timing Element	6.95
DP8304	8-Bit Bi-Directional Receiver	3.95
DP8307	8-Bit Bi-Directional Receiver	3.95
DP8308	8-Bit Bi-Directional Receiver	3.95

6800/6800 SUPPORT DEVICES

MC6800	MPU	14.95
MC6802CP	MPU with Clock and RAM	[illegible]
MC6810API	128x8 Static RAM	4.95
MC6821	Peripheral Inter. Adapt (MC6820)	[illegible]
MC6828	Priority Interrupt Controller	10.95
MC6830L8	1024x8-Bit ROM (MC68A30-8)	14.95
MC6850	Asynchronous Comm. Adapter	4.95
MC6852	Synchronous Serial Data Adapter	5.95
MC6860	0-600bps Digital MODEM	10.95
MC6862	2400bps Modulator	12.95
MC6880A	Quad 3-State Bus. Trans. (MC8T26)	2.25

MICROPROCESSOR CHIPS

Z80 (780C)	CPU (MK3880N) (2MHz)	13.95
Z80A (780-1)	CPU (MK3880N-4) (4MHz)	15.95
CDP1802	CPU	19.95
2650	MPU	16.95
IDM2901ADC	CPU—4-Bit Slice (Com. Temp. Grade)	19.95
MCS6502	MPU w/Clock (65K Bytes Memory)	11.95
INS8035N-6	MPU - 8-Bit (6MHz)	16.95
INS8039N-6	CPU - Sgl. Chip 8-Bit (128 bytes RAM)	19.95
INS8040N-6	CPU (256 Bytes RAM)	24.95
INS8070N	CPU—64 Bytes RAM	24.95
INS8073N	CPU w/Basic Micro Interpreter	29.95
P8085	CPU	19.95
TMS9900	CPU—16-Bit	29.95
TMS9900JL	MPU—16-Bit	49.95

SHIFT REGISTERS

MM500H	Dual 25-Bit Dynamic	.50
MM503H	Dual 50-Bit Dynamic	.50
MM506H	Dual 100-Bit Static	.50
MM510H	Dual 64-Bit Accumulator	.50
MM1402	256-Bit Dynamic	1.95
MM5013	1024-Bit Dynamic/Accumulator	1.95
MM5016H	500/512-Bit Dynamic	.89
MM5034N	Octal 80-Bit	9.95
MM5035N	Octal 80-Bit	9.95
2504V (1404A)	1024-Bit Dynamic	3.95
2518N	Hex 32-Bit Static	4.95
2522V	Dual 132-Bit Static	2.95
2524V	512-Bit Dynamic	.99
2525V	1024-Bit Dynamic	2.95
2527V	Dual 256-Bit Static	2.95
2528V	Dual 250-Bit Static	4.00
2529V	Dual 240-Bit Static	4.00
2532N	Quad 80-Bit Static	2.95
3341PC	Fifo (Dual 40)	6.95

DATA ACQUISITION

AF100-1CN	Universal Active Filter 2.5%	8.95
AF121-1CJ	Touch Tone Low Pass Filter	19.95
AF122-1CJ	Touch Tone Low Pass Filter	19.95
LM308AH	Super Gain Op Amp	1.00
LM334Z	Constant Current Source	1.20
LM335Z	Temperature Transducer	1.40
LF356N	JFET Input Op Amp	1.10
LF398N	Sample & Hold Amplifiers	3.95
LM399H	Temp. Comp. Prec. Ref. (.5ppm/C°)	4.95
ADC0804LCN	8-Bit A/D Converter (1 LSB)	4.95
DAC0806LCN	8-Bit D/A Converter (0.78% Lin.)	2.25

DATA ACQUISITION (CONTINUED)

ADC0809CCN	8-Bit A/D Converter (8-Ch. Multi.)	5.75
ADC0817CCN	8-Bit A/D Converter (16-Ch. Multi.)	10.95
DAC1000LCN	10-Bit D/A Conv. Micro. Comp. (0.05%)	13.95
DAC1008LCN	10-Bit D/A Conv. Micro. Comp. (0.20%)	8.95
DAC1020LCN	10-Bit D/A Converter (0.05% Lin.)	8.49
DAC1022LCN	10-Bit D/A Converter (0.20% Lin.)	5.95
DAC1222LCN	12-Bit D/A Converter (0.20% Lin.)	9.95
CD4051N	8-Channel Multiplexer	1.19
AY-5-1013	30K BAUD UART	5.95

RAM'S

1101	256x1 Static	1.49
1103	1024x1 Dynamic	.99
2101 (8101)	256x4 Static	3.95
2102	1024x1 Static	1.75
21L02	1024x1 Static	1.95
2111 (8111)	256x4 Static	3.95
2112	256x4 Static MOS	4.95
2114	1024x4 Static 450ns	5.95
2114L	1024x4 Static 450ns Low Power	6.95
2114-3	1024x4 Static 300ns	7.49
2114L-3	1024x4 Static 300ns Low Power	7.95
2117	16,384x1 Dynamic 350ns (housemarked)	4.95
4116 (UPD416)	16K Dynamic 250ns	4.95
MM2147J	4096x1 Fast 70ns	19.95
5101	256x4 Static	7.95
MM5261	1024x1 Dynamic Fully Decoded	.99
MM5262	2Kx1 Dynamic	.25
MM5280/2107	4096x1 Dynamic	4.95
MM5290J-2 (4116)	16K Dynamic 150ns (UPD416)	6.95
MM5298J-3A	8K Dyn. 200ns (lower ½ of MM5290J)	4.95
7489	16x4 Static	1.75
UPD414/MK4027	4K Dynamic 16-pin	4.95
TMS4044-45NL	4K Static	14.95
TMS4045	1024x4 Static	14.96

PROMS/EPROMS

1702A	2K UV Erasable PROM	5.95
2708	8K EPROM	9.95
TMS2716	16K EPROM (-5V, +5V, +12V)	19.95
2716 Intel (2516) TI	16K EPROM (Single +5V)	17.95
2732 Intel (2532) TI	32K EPROM	49.95
2758	8K EPROM (450ns) (Single +5V)	7.95
5203	2048 PROM	14.95
82S23 (74S188)	32x8 PROM (Open Collector)	4.95
82S115	4096 Bipolar PROM	19.95
82S123 (74S288)	32x8 Tri-State Bipolar PROM	4.95
82S185	8K PROM	29.95

ROM'S

2513 (2140)	Character Generator (Upper Case)	9.95
2513 (3021)	Character Generator (Lower Case)	9.95
2516N	Character Generator	10.95
MM5230N	2048-Bit Read Only Memory	1.95

NMOS READ ONLY MEMORIES

MCM6571P	128x9x7 ASCII Shifted w/Greek	13.50
MCM6574P	128x9x7 Math Symbol & Pictures	13.50
MCM6575P	128x9x7 Alpha Control Char Gen.	13.50

MICROPROCESSOR MANUALS

M-Z80	User Manual	7.50
M-CDP1802	User Manual	7.50
M-2650	User Manual	5.00

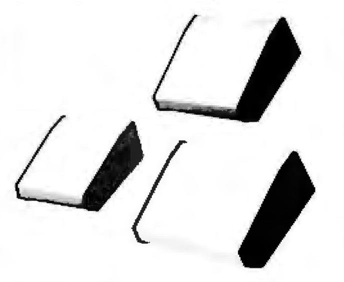
SPECIAL FUNCTION

DS0025CN	Dual MOS Clock Driver (5MZ)	3.50
DS0026CN	Dual MOS Clock Driver (5MZ)	1.95
INS1771N-1	Floppy Disc Controller	24.95
INS2651N	Communication Chip	19.95
MM58167N	Microprocessor Real Time Clock	8.95
MM58174N	Microprocessor Compatible Clock	11.95
COP402N	Microcontroller with 64-Digit RAM and Direct LED Drive	6.95
COP404MN	Microcontroller with 64-Digit RAM & Direct LED Drive w/N Buss Int.	[illegible]
COP470N	32-Seg. VAC Fluor. Driver (20-pin pkg.)	3.25

TELEPHONE/KEYBOARD CHIPS

AY-5-9100	Push Button Telephone Dialer	14.95
AY-5-9200	Repertory Dialer	14.95
AY-5-9500	CMOS Clock Generator	4.95
AY-5-2376	Keyboard Encoder (88 keys)	11.95
HD0165-5	Keyboard Encoder (16 keys)	7.95
74C922	Keyboard Encoder (16 keys)	5.49
74C923	Keyboard Encoder (20 keys)	5.75
MM53190N	Push Button Pulse Dialer	7.95
MM57499N	96/144-Key Serial Keyboard Encoder	8.95

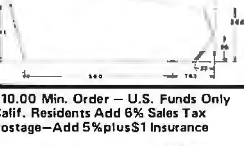
DESIGNERS' SERIES
Blank Desk-Top Electronic Enclosures



- High strength epoxy molded end pieces in mocha brown finish.
- Sliding rear/bottom panel for service and component accessibility.
- Top/bottom panels .080 thk alum. Alodine type 1200 finish (gold tint color) for best paint adhesion after modification.
- Vented top and bottom panels for cooling efficiency.
- Rigid construction provides unlimited applications.

CONSTRUCTION:

The "DTE" Blank Desk Top Electronic Enclosures are designed to blend and complement today's modern computer equipment and can be used in both industrial and home. The end pieces are precision molded with an internal slot (all around) to accept both top and bottom panels. The panels are then fastened to ¼" thick tabs inside the end pieces to provide maximum rigidity to the enclosure. For ease of equipment servicing, the rear/bottom panel slides back on slotted tracks while the rest of the enclosure remains intact. Different panel widths may be used while maintaining a common profile outline. The molded end pieces can also be painted to match any panel color scheme.



Enclosure Model No.	Panel Width	PRICE
DTE-8	8.00"	$29.95
DTE-11	10.65"	$32.95
DTE-14	14.00"	$34.95

$10.00 Min. Order — U.S. Funds Only
Calif. Residents Add 6% Sales Tax
Postage—Add 5% plus $1 Insurance

Spec Sheets — 25¢
Send 41¢ Postage for your
FREE 1981 JAMECO CATALOG

NEW 1981 CATALOG

Jameco ELECTRONICS

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ORDERS
WELCOME
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1355 SHOREWAY ROAD, BELMONT, CA 94002
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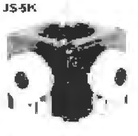
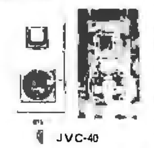
3/81

JOYSTICKS



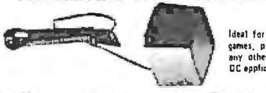
JS-5K



JVC-40

JS-5K	5K Linear Taper Pots	$5.25
JS-100K	100K Linear Taper Pots	$4.95
JVC-40	40K (2) Video Controller in case . . .	$5.95

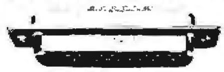
AC and DC Wall Transformers



Ideal for use with clocks, games, power supplies or any other type of AC or DC application

Part No.	Input	Output	Price
AC 250	117V/60Hz	12 VAC 250mA	$3.95
AC 500	117V/60Hz	12 VAC 500mA	$4.95
AC1000	117V/60Hz	12 VAC 1 amp	$5.95
DV9200	117V/60Hz	9 VDC 200mA	$3.25
DC 900	120V/60Hz	9 VDC 500mA	$3.95

CONNECTORS



DB25P	D-Subminiature Plug	$2.95
DB25S	D-Subminiature Socket	$3.50
DB51226	Cover for DB25P/S	$1.75
22/44SE	P.C. Edge (22/44 Pin)	$2.95
UG88/U	BNC Plug	$1.79
UG89/U	BNC Jack	$3.79
UG175/U	UHF Adapter	$ .49
SO239	UHF Panel Recp.	$1.29
PL258	UHF Adapter	$1.60
PL259	UHF Plug	$1.60
UG260/U	BNC Plug	$1.79
UG1094/U	BNC Bulkhead Recp.	$1.29

TRS-80
16K Conversion Kit

Expand your 4K TRS-80 System to 16K.
Kit comes complete with:
★ 8 ea. MM5290 (UPD416/4116) 16K Dyn. Rams (*NS)
★ Documentation for Conversion

TRS-16K2 *150NS **$49.95**
TRS-16K4 *250NS **$39.95**

JE610 ASCII
Encoded Keyboard Kit

The JE610 ASCII Keyboard Kit can be interfaced into most any computer system. The kit comes complete with an industrial grade keyboard switch assembly (62-keys), IC's, sockets, connector, electronic components and a double-sided printed wiring board. The keyboard assembly requires +5V @ 150mA and −12V @ 10 mA for operation. Features: 60 keys generate the 126 characters, upper and lower case ASCII set. Fully buffered. Two user-define keys provided for custom applications. Caps lock for upper-case-only alpha characters. Utilizes a 2376 (40-pin) encoder read-only memory chip. Outputs directly compatible with TTL/DTL or MOS logic arrays. Easy interfacing with a 16-pin dip or 18-pin edgeconnector. Size: 3½"H x 14½"W x 8¾"D

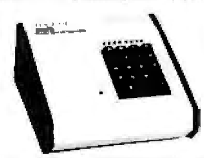
JE610/DTE-AK (as pictured above) . . . **$124.95**

JE610 Kit 62-Key Keyboard, PC Board, & Components (no case). . . . **$ 79.95**

K62 62-Key Keyboard (Keyboard only) . . . **$ 34.95**

DTE-AK (case only — 3¼"Hx11"Wx8¾"D) **$ 49.95**

JE600
Hexadecimal Encoder Kit



FULL 8-BIT
LATCHED OUTPUT
19-KEY KEYBOARD

The JE600 Encoder Keyboard Kit provides two separate hexadecimal digits produced from sequential key entries to allow direct programming for 8-bit microprocessor or 8-bit memory circuits. Three additional keys are provided for user operations with one having a bistable output available. The outputs are latched and monitored with 9 LED readouts. Also included is a key entry strobe. Features: Full 8-bit latched output for microprocessor use. Three user-define keys with one being bistable operation. Debounce circuit provided for all 19 keys. 9 LED readouts to verify entries. Easy interfacing with standard 16-pin IC connector. Only +5VDC required for operation. Size: 3½"H x 8¼"W x 8¾"D

JE600/DTE-HK (as pictured above) **$99.95**

JE600 Kit 19-Key Hexadec. Keyboard, PC Board & Cmpnts. (no case) . . **$59.95**

K19 19-Key Keyboard (Keyboard only) **$14.95**

DTE-HK (case only — 3½"Hx8¼"Wx8¾"D) **$44.95**

Circle 328 on inquiry card.

QT
COMPUTER
SYSTEMS
INC.

15620 South Inglewood Avenue
Lawndale, California 90260
(213) 970-0952

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1-800-421-5150
(CONTINENTAL U.S. ONLY)
(EXCEPT CALIFORNIA)

Retail Store Open
10:00 A.M. to 6:00 P.M.
Daily **Except** Sunday

QT CATALOG NOW AVAILABLE

QT SYSTEM +

The QT System+ is designed for both businessmen and engineers in accordance with latest IEEE standards. Among other functions, it can be used for accounting and word processing, as well as a variety of scientific applications. The system will soon be available with MP/M® to allow multi-user, multi-tasking operations. This means, for example, that an engineer could be working on scientific applications in the lab while an accountant is writing payroll checks in the office. QT also offers a full line of business and applications software, ranging from a business package to word processing.

Technical specifications: 4MHz Z-80A CPU • Dbl-sided, dbl-den. 5¼" & 8" floppy disk controller (handles both drives simultaneously) • Includes televideo terminal • Two 8" dbl-den., sgl. or dual sided disk drives, expandable to 4 floppy drives • CP/M® 2.2 included • 64K RAM, expandable per your requirements • Comes complete in single mainframe • EPROM/ROM in any combination to 8K • Two RS232C serial I/O ports • Two parallel I/O ports • Hard disk compatible • Real time clock • Std. 2K monitor program & disk routines included on ROM • Power-on/Reset jump to monitor program • 2716 (5V) EPROM programmer (software incl. on monitor ROM; ext. 25.5V @ 50ma req.) • Uses Z-80A CPU vectored interrupts • Assembled, tested & burned in at factory • Documentation included.

SYSTEM + I (1MB+)

SYS+SS Computer System with 8" Single Sided Drives (801R) without Terminal

A&T (6 slot)	$3495.00
A&T (8 slot)	$3595.00
A&T (12 slot)	$3695.00

With Terminal Add $900.00

SYSTEM + II (2MB+)

SYS+DS Computer System with 8" Dual-Sided Drives (Qume DT-8) without Terminal

A&T (6 slot)	$4195.00
A&T (8 slot)	$4295.00
A&T (12 slot)	$4395.00

With Terminal Add $900.00

MINI-SYSTEM + I (½MB+)

Computer System with 5¼" Single Sided Drives (uses B-51 Disk Drives) No Terminal

A&T (6 slot)	$2495.00
A&T (8 slot)	$2595.00
A&T (12 slot)	$2695.00

MINI-SYSTEM + II (1MB+)

Computer System with 5¼" Double Sided Drives (uses B-52 Disk Drives) No Terminal

A&T (6 slot)	$2795.00
A&T (8 slot)	$2895.00
A&T (12 slot)	$2995.00

S-100 PRODUCTS

Double Density - Cal Comp Sys

5¼" or 8" disk controller with free CP/M 2.2

CCS-2422A A&T	$374.95

SALE

SBC-100-SD Systems

2.5 MHz Z80 CPU with serial & parallel I/O ports

SDS-SBC100K Kit	$280.00
SDS-SBC100AT A&T	$350.00

SBC-200 - SD Systems

4 MHz Z80 CPU with serial & parallel I/O ports

SDS-SBC200K Kit	$348.00
SDS-SBC200AT A&T	$408.00

SALE

CB2 - S.S.M.

2 or 4 MHz switchable Z80 CPU with RAM, ROM & I/O

SSM-CB2K Kit	$200.00
SSM-CB2AT A&T	$275.00

2810 Z-80 CPU - Cal Comp Sys

2 or 4 MHz Z80A CPU w/serial I/O port

CCS-2810 A&T	$275.00

Expando RAM II - SD Systems

4 MHz RAM board expandable from 16K to 256K

SDS-RAM216K 16K kit	$289.95
SDS-RAM216AT 16K A&T	$339.95
SDS-RAM232K 32K kit	$329.95
SDS-RAM232AT 32K A&T	$379.95
SDS-RAM248K 48K kit	$369.95
SDS-RAM248AT 48K A&T	$419.95
SDS-RAM264K 64K kit	$409.95
SDS-RAM264K 64K A&T	$459.95

PROM-100 - SD Systems

2708, 2716, 2732, 2758 & 2516 EPROM programmer

SDS-PROM-100K kit	$220.00
SDS-PROM-100AT A&T	$275.00

I/O-4 - S.S.M.

2 serial I/O ports plus 2 parallel I/O ports

SSM-I04K kit	$179.95
SSM-I04AT A&T	$259.95
SSM-I04BB Bare board	$ 35.00

Versafloppy II - SD Systems

New double density controller for both 8" & 5¼"

SDS-VF2K kit	$385.00
SDS-VF2AT A&T	$450.00

VDB-8024 - SD Systems

80 x 24 I/O mapped video board with keyboard I/O

SDS-VDBK kit	$406.00
SDS-VDBAT A&T	$475.00

VB3 - S.S.M.

80 x 24 x 48 memory mapped with graphics

SSM-VB3-4mhzK kit, 4 MHz	$399.95
SSM-VB3-4mhzAT A&T, 4 MHz	$464.95
SSM-VB3-4mhzUPG 80 x 48 upgrade, 4 MHz	$ 89.00

T1 Active Terminator

SSM-T1K kit	$ 34.00
SSM-T1AT A&T	$ 64.00

VB2 I/O Mapped Video Interface

SSM-VB2K kit	$160.00
SSM-VB2AT A&T	$210.00

XB1 Extender Board

SSM-XB1K kit (with Connector)	$ 22.00
SSM-XB1AT Assembled & tested	$ 30.00

Z-80 STARTER KIT - SD Systems

Z-80 computer with RAM, ROM, I/O & keyboard

SDS-Z80K kit	$374.00
SDS-Z80AT A&T	$454.00

ITHACA AUDIO REV 2.0 Z-80 BD

Bare Board	**$35.00 each**

10 for $300.00

SEALS ELECTRONICS 32K STATIC BD

Uses TMS-4044 or 5257L	**$35.00 each**

QT MEMORY EXPANSION KITS

TRS-80 • APPLE • EXIDY

4116 200 ns	8 for $32.00
2716 (5V-450 ns)	$ 9.00
2716 (5 & 12V-450 ns)	$ 9.00
2732 (5V)	$40.00
2114L 300 ns	8 for $36.00
	100 - $3.50 ea.

PARTS

MICROPROCESSORS

Z80 (2MHz)	$10.95
Z80A (4MHz)	$12.95
6502	$11.25
6800	$12.50
6802	$18.00
8035	$20.00
8080A	$ 3.50
8085A	$20.00
8086-4	$60.00
8088	$60.00
8748	$60.00
TMS 9900 JL	$29.95

8080A SUPPORT

8212	$ 3.50
8214	$ 4.50
8216	$ 2.95
8224	$ 4.00
8228	$ 6.00
8238	$ 6.00
8243	$ 5.00
8251	$ 7.00
8253	$19.00
8253-5	$20.25
8255	$ 6.25
8257	$17.95
8257-5	$19.00
8259	$19.95
8275	$69.95
8279	$17.50
8279-5	$18.00
8295	$16.50

KEYBOARD CHIPS

AY5-2376	$13.75
AY5-3600	$13.75

BAUD RATE GENERATORS

MC14411	$11.00
1.8432 XTAL	$ 4.95

DISK CONTROLLER

1771B01	$24.95
1791A01(CER)	$37.95

EPROMS

1702A	$ 4.95
2708	$ 6.25
2516 (5V)	$18.00
2716 (5V)	$13.50
2716 (5 & 12V)	$13.50
2758	$19.95
2532	$55.00
2732	$55.00

USRT

S2350	$ 7.95

MISCELLANEOUS OTHER COMPONENTS

N8T20	$ 3.25
N8T26	$ 2.50
N8T97	$ 2.00
N8T98	$ 2.00
1488	$ 1.25
1489	$ 1.25
D3205	$ 3.00
D3242	$14.00
P3404	$ 6.75
TMS5501	$19.00
DM8131	$ 3.00

UARTS

TR1602B	$ 4.50
AY5-1013A	$ 4.50

CHARACTER GENERATORS

2513 UP CASE (5&12V)	$10.95
2513 LWR CASE (5&12V)	$10.95
2513 UP CASE (5V)	$ 9.75
2513 LWR CASE (5V)	$10.95

6800 PRODUCTS

6802P	$18.00
6821P	$ 5.25
6840P	$18.25
6845P	$22.00
6850P	$ 4.80
6860P	$11.55
6875P	$ 7.40

QT PRODUCTS

SBC+2/4
SINGLE BOARD COMPUTER

Features: 1K RAM (which can be located at any 1K boundary) plus one each Parallel and Serial I/O parts on board • Power on jump to on-board EPROM (2708 or 2716) • EPROM addressable on any 1K or 2K boundary • Full 64K use of RAM allowed in shadow mode • Programmable Baud rate selection, 110-9600 • 2 or 4MHz switch selectable • DMA capability allows MWRT signal generation on CPU board or elsewhere in system under DMA logic or front panel control • Two programmable timers available for use by programs run with the SBC+2/4 (timer output and controls available at parallel I/O connector; parallel input and output ports available for use on CPU board).

Bare Board	$ 60.00
Kit	$190.00
A&T	$295.00

Z+80 CPU

Features: Power on jump to on-board EPROM (2708, 2716 or 2732) • EPROM addressed on any 1K or 2K boundary; also shadow mode allows full 64K use of RAM • On-board USART for Synchronous or Asynchronous RS-232 Operation (Serial I/O port) • Programmable Baud rate selection, 110-9600 • Switch selectable 2 or 4 MHz • MWRITE signal generated if used without front panel • Front panel compatible.

Bare Board	$ 50.00
Kit	$150.00
A&T	$210.00

CLOCK/CALENDAR+
FOR APPLE II, S-100 OR TRS-80

Features: Date/Month/Year • Day of week • 24 hour time or 12 hour (a.m./p.m.) selectable • Leap year (perpetual calendar) • 4 interval interrupt timer; 1024Hz (approx. 1 millisec), 1 sec., 1 min., 1 hr. • On-board battery backup • Simple time and date setting • Simple software interface • Time advance protection while reading.

S-100 or Apple		TRS-80	
A&T	$150.00	A&T Only	$150.00
Kit	$100.00		
Bare Bd.	$ 60.00		

SMART PROTO BOARD+

Features: Wire-wrap or solder sockets • Accepts all std. sockets — .30" & 60" center • Allows grid distributed power • Three voltage regulators • Kluge area for discretes, ext. drives • Two bus bars for ± voltages — int. & ext. • Accepts std. edge connector on .1" center • Kit includes 3 regulators/3 heat sinks/filter capacitors/2 bus bars/Manual.

Bare Board	$ 35.00
Kit	$ 60.00

EXPANDABLE+ REV II
DYNAMIC MEMORY BOARD

NEW

Features: Runs at 4MHz • 3242 refresh controller with delay line • Four layer PC board insures quiet operation • Supports 16K, 32K, 48K or 64K of memory • 24 IEEE-specified address lines • Optional M1 wait state allows error free operation with faster processors • Optional Phantom disable • Uses Z-80 or on-board refresh signal • Bank on/off signal selected by industry standard I/O port 40 (Hex) • Convenient DIP switch selection of data bus bits determines bank in use • 3 watts low power consumption • Convenient LED indication of bank in use.

Definitely works with Cromemco and North Star.

Bare Board .... $ 75.00

KIT		A&T	
No RAM	$230.00	16K	$350.00
16K	$280.00	32K	$450.00
32K	$360.00	48K	$575.00
48K	$480.00	64K	$675.00
64K	$525.00		

RAM+16

Features: S-100, 16K x 8 bit static RAM • 2 or 4 MHz • Uses 2114 1K x 4 static RAM chip • 4K step addressable • 1K increment memory protection, from bottom board address up or top down • Deactivates up to six 1K board segments to create "holes" for other devices • DIP switch selectable wait states • Phantom line DIP switch • Eight bank select lines expandable to ½ million byte system • Data, address and control lines all input buffered • Ignores I/O commands at board address.

Bare Board	$ 35.00
4Mhz Kit	$180.00
4Mhz A&T	$210.00

WATCH FOR THE FOLLOWING NEW BDS:

- **4 Port Serial Bd (FEB)**
- **E-PROM Programmer (MAR)**
- **Floppy Disk Controller (APR)**
- **Hard Disk Controller (MAY)**
- **Color Video Bd (JUN)**

I/O+
INDUSTRIAL GRADE I/O BD

Has two serial Sync/Async ports (RS-232, current loop or TTL) with individual Xtal controlled programmable baudrate generators • Four 8-bit Parallel ports; one latched input port and other three can be programmed in combinations of input, output or bidirectional • Also, has three 16-bit Programmable Timers and an 8-level Programmable Interrupt Controller w/Auto restart (8080/Z80) • Other features include; on-board clock divisor for timers, completely socketed, wire wrap posts for easy port configuration plus more.

Bare Board	$ 70.00
Kit	$200.00
A&T	$375.00

SILENCE+
MOTHERBOARDS

These motherboards are among the quietest on the market. A unique grounding matrix — with each line completely surrounded by ground shielding — eliminates need for termination and gives high crosstalk rejection • They're customer-proven, without crosstalk sometimes operating at 14MHz • A LED power indicator helps eliminate zapped circuits • IEEE S-100 std. compatible, available with 6, 8, 12, 18 or 22 slots • (The 22 slot board fits Imsai chassis and has slot for front panel.)

6 Slot	
Bare Board	$ 25.00
Kit	$ 40.00
A&T	$ 50.00
8 Slot	
Bare Board	$ 27.00
Kit	$ 55.00
A&T	$ 70.00
12 Slot	
Bare Board	$ 30.00
Kit	$ 70.00
A&T	$ 90.00
18 Slot	
Bare Board	$ 50.00
Kit	$100.00
A&T	$140.00

QT MAINFRAMES

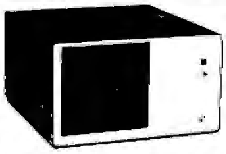
5¼" Disk Mainframe with 18A Pwr Sup

MF+MD12 (12 slot M/B)	$500.00
MF+MD6 (6 slot M/B)	$450.00
MF+MD w/o M/B	$400.00

Q.T. Mainframe

MF+12 (12 slot M/B)	$450.00
MF+18 (18 slot M/B)	$500.00
MF+22 (22 slot M/B)	$600.00

MAINFRAME+ DISK DRIVE



Includes cabinet, 30 amp power supply, IEEE S-100 compatible 6, 8 or 12 slot motherboard and dual 8" disk drive with disk drive power supply.

MF+DD6	$625.00
MF+DD8	$650.00
MF+DD12	$675.00

DDC-8
SINGLE 8" DISK CABINET

Accepts one 8" disk drive (Shugart, Remex, PerSci, Siemens, etc.) • Fan cooled, with data cable and AC line filter to eliminate EMI • Operates from 100-125VAC/200-250VAC at 50-60Hz • Disk drive NOT included.

DDC+8	$175.00

QT COMPUTER SYSTEMS INC.
15620 South Inglewood Avenue
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(213) 970-0952

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Apple is a trademark of Apple Computer, Inc.
CP/M and MP/M are trademarks of Digital Research.
TRS-80 is a trademark of Radio Shack.

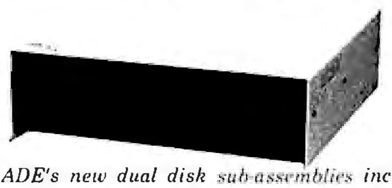
TERMS OF SALE: Cash, checks, money orders, credit cards accepted. Also C.O.D. orders under $100.00. Minimum order $10.00. California residents add 6% sales tax. Minimum shipping and handling charge $3.00. Prices subject to change without notice. International sales in American dollars only.

VISA

Circle 329 on inquiry card.

SALE SALE SALE

Disk Drives



JADE's new dual disk sub-assemblies include: Handsome metal cabinet with proportionally balanced air flow system, rugged dual drive power supply, cooling fan, cable kit, lighted power switch, approved fuse assembly, line cord, Never-Mar rubber feet, and all necessary hardware to mount 2-8" disk drives - it's all American made, guaranteed for six months, and it's in stock!

Dual 8" Sub-Assembly Cabinet

END-000421	*Cabinet kit*	**$225.00**
END-000420	*Bare cabinet*	**$59.95**

Single sided, double density disk drive sub-system

END-000423	*Kit w/2 8" drives*	**$975.00**
END-000424	*A & T w/2 8" drives*	**$1195.00**

Double sided, double density disk drive sub-system

END-000426	*kit w/2 8" drives*	**$1495.00**
END-000427	*A & T w/2 8" drives*	**$1695.00**

JADE DISK PACKAGE

Double density controller, two 8" double density floppy disk drives, CP/M2.2 (configured for controller), hardware and software manuals, boot PROM, cabinet, power supply, fan, & cables

Special package price **$1395.00**

8" Disk Drive Sale

Highly reliable double density floppy disk drives

Shugart 801R single sided, double density

MSF-10801R	*SA-801R*	**$425.00**
Special Sale Price		***2 for $790.00***

Siemens FDD100-8D2 single sided, double density

MSF-201120	*6 mo warranty*	**$385.00**
Special sale price		***2 for $750.00***

Real Double-Sided Drives

8" Double-Sided Double-Density Sale

★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★

★ ***Shugart SA-851R double-sided, double-density*** ★

★ *only* **$625.00 ea** .... ***2 for $1190.00*** ★

★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★

MFE M701 8" double-sided, double-density drives

only **$525 ea** .... ***2 for $1040.00***

Qume Data Track 8 double-sided, double-density drives

only **$575.00** .... ***2 for $1100.00***

Printers

CENTRONICS 737-1

9 x N dot matrix, letter quality, proportional spacing

PRM-15737	*Parallel*	**$795.00**
With interface for Apple		**$895.00**

MX-80 - Epson

132 column, 9 x 9 dot matrix, multiple fonts

PRM-27080	*Save $100.00*	**$545.00**
Interface for Apple		**$110.00**

SPINWRITER - NEC

65 cps, bi-directional, letter quality printer with deluxe tractor mechanism, both parallel and serial interfaces on-board, 16K buffer, ribbon, print thimble, graphics, micro space justification, data cable, and self test/diagnostic ROM.

PRD-55511	*without 16K buffer*	**$2795.00**
PRD-55512	*with 16K buffer*	**$2895.00**

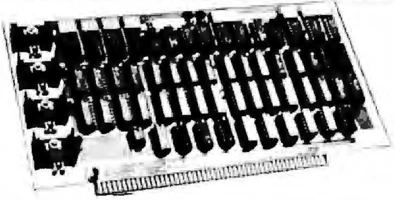
S-100 Systems

S-100 SYSTEM - Calif Computer Sys

Complete S-100 system including 12 slot mainframe, 4 MHz Z-80 CPU, 64K RAM memory, double density disk controller, RS-232 cable, 8" & 5¼" disk drive cables, CP/M 2.2, manuals, auto boot ROM, completely assembled & tested.

2210A	*Integrated & tested*	**$1995.00**
2210B	*Not integrated*	**$1795.00**

S-100 Memory



64K RAM - Calif Computer Sys

4 MHz bank port / bank byte selectable, extended addressing, 16K bank selectable, PHANTOM line allows memory overlay, 8080 / Z-80 front panel compatible.

MEM-64565A	*A & T*	**$449.95**

MEMORY BANK - Jade

4 MHz, IEEE S-100, bank selectable, 8 or 16 bit

MEM-99730B	*Bare board*	**$55.00**
MEM-99730K	*Kit, no RAM*	**$219.95**
MEM-16730K	*16K kit*	**$249.95**
MEM-32731K	*32K kit*	**$289.95**
MEM-48732K	*48K kit*	**$324.95**
MEM-64733K	*64K kit*	**$359.95**
Assembled & tested		add **$50.00**

EXPANDORAM II - S D Systems

1 MHz RAM board expandable from 16K to 256K

MEM-16630K	*16K kit*	**$275.95**
MEM-32631K	*32K kit*	**$295.95**
MEM-48632K	*48K kit*	**$315.95**
MEM-64633K	*64K kit*	**$335.95**
Assembled & tested		add **$50.00**

32K STATIC RAM - Jade

2 or 4 MHz expandable static RAM board uses 2114L's

MEM-16151K	*16K 4 MHz kit*	**$169.95**
MEM-32151K	*32K 4 MHz kit*	**$299.95**
Assembled & tested		add **$50.00**

16K STATIC RAM - Cal Comp Sys

2 or 4 MHz 16K static RAM board, IEEE S-100, bank selectable, Phantom capability, addressable in 4K blocks

MEM-16160A	*16K 2 MHz A & T*	**$286.95**
MEM-16162A	*16K 4 MHz A & T*	**$289.95**
MEM-16160B	*Bare board*	**$50.00**

PB-1 - S.S.M.

2708, 2716 EPROM board with built-in programmer

MEM-99510K	*Kit*	**$154.95**
MEM-99510A	*A & T*	**$229.95**

PROM-100 - SD Systems

2708, 2716, 2732, 2758, & 2516 EPROM programmer

MEM-99520K	*Kit*	**$219.95**
MEM-99520A	*Jade A & T*	**$269.95**

S-100 Video

VB-3 - S.S.M.

80 characters x 24 lines expandable to 80 x 48 for a full page of text, upper & lower case, 256 user defined symbols, 160 x 192 graphics matrix, memory mapped, has key board input.

IOV-1095K	*4 MHz kit*	**$375.00**
IOV-1095A	*4 MHz A & T*	**$450.00**
IOV-1096K	*80 x 48 upgrade*	**$39.95**

VIDEO BOARD - Jade

64 characters x 16 lines, 7 x 9 dot matrix, full upper lower case ASCII character set, numbers, symbols, and greek letters, normal/reverse/blinking video, S-100.

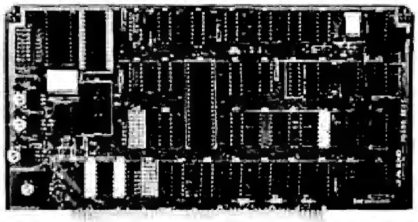
IOV-1050K	*Kit*	**$99.95**
IOV-1050A	*A & T*	**$125.00**
IOV-1050B	*Bare board*	**$19.95**

S-100 CPU

2810 Z-80* CPU - Cal Comp Sys

2 4 MHz Z-80A CPU with RS-232C serial I O port and on-board MOSS 2.2 monitor PROM, front panel compatible.*

CPU-30400A	*A & T*	**$269.95**



THE BIG Z* - Jade

2 or 4 MHz switchable Z-80 CPU with serial I O, accomodates 2708, 2716, or 2732 EPROM, baud rates from 75 to 9600*

CPU-30201K	*Kit*	**$145.00**
CPU-30201A	*A & T*	**$199.00**
CPU-30200B	*Bare board*	**$35.00**

CB-2 Z-80 CPU - S.S.M.

2 or 4 MHz Z-80 CPU board with provision for up to 8K of ROM or 4K of RAM on board, extended addressing, IEEE S-100, front panel compatible.

CPU-30300A	*A & T*	**$229.95**

SBC-200 - SD Systems

4 MHz Z-80 CPU with serial & parallel I O ports, up to 8K of on-board PROM, software programmable baud rate generator, 1K of on-board RAM, Z-80 CTC.*

CPC-30200K	*Kit*	**$339.95**
CPC-30200A	*Jade A & T*	**$399.95**

S-100 Disk Controller

DOUBLE DENSITY - Cal Comp Sys

5¼" and 8" disk controller, single or double density, with on-board boot loader ROM, and free CP/M 2.2 and manual set.*

IOD-1300A	*A & T*	**$369.95**

DOUBLE-D - Jade

Double density controller with the inside track, on-board Z-80A, printer port, IEEE S-100, can function on an interrupt driven buss*

IOD-1200K	*Kit*	**$299.95**
IOD-1200A	*8" A & T*	**$389.95**
IOD-1205A	*5¼" A & T*	**$389.95**
IOD-1200B	*Bare board*	**$65.00**

VERSAFLOPPY II - SD Systems

New double density controller for both 8" & 5¼"

IOD-1160K	*Kit*	**$379.95**
IOD-1160A	*Jade A & T*	**$439.95**

Motherboards

ISO-BUS - Jade

Silent, simple, and on sale - a better motherboard

6 Slot (5¼" x 8⅝")

MBS-061B	*Bare board*	**$19.95**
MBS-061K	*Kit*	**$39.95**
MBS-061A	*A & T*	**$49.95**

12 Slot (9¾" x 8⅝")

MBS-121B	*Bare board*	**$29.95**
MBS-121K	*Kit*	**$69.95**
MBS-121A	*A & T*	**$89.95**

18 Slot (14½" x 8⅝")

MBS-181B	*Bare board*	**$49.95**
MBS-181K	*Kit*	**$99.95**
MBS-181A	*A & T*	**$139.95**

Card Cages

S-100 CARD CAGE - Jade

Metal cage with card guides & fan mounting

ENX-106001	*Six slot*	**$29.95**

S-100 CARD CAGE - Vector

19" rack mountable, adjustable, holds 21 cards

VCT-CCK100	*Anodized Al*	**$49.95**

SALE SALE SALE

S-100 I/O

S.P.I.C. - Jade

Our new I/O card with 2 SIO's, 4 CTC's, and 1 PIO

IOI-1045K	*2 CTC's, 1 SIO, 1 PIO*	$199.00
IOI-1045A	*A & T*	$259.00
IOI-1046K	*4 CTC's, 2 SIO's, 1 PIO*	$259.00
IOI-1046A	*A & T*	$319.00
IOI-1045B	*Bare board w/ manual*	$59.95
IOI-1045D	*Manual only*	$20.00

I/O-4 - S.S.M.

2 serial I/O ports plus 2 parallel I/O ports

IOI-1010K	*Kit*	$179.95
IOI-1010A	*A & T*	$249.95
IOI-1010B	*Bare board*	$35.00

TERMINATOR - S.S.M.

Active terminator for S-100 bus

TSX-195K	*Kit*	$29.95
TSX-195A	*A & T*	$54.95
TSX-195B	*Bare board*	$22.95

S-100 EXTENDER - Cal Comp Sys

Put those problem boards (the ones you probably bought from one of our competitors) within easy reach.

TSX-160A	*A & T*	$37.95

S-100 PROTO BOARD - Jade

Universal design, plated thru holes, gold fingers

TSX-140B	*Bare board*	$24.95

TERMINATOR & EXTENDER - C.C.S.

Can be used as both an S-100 extender and terminator

TSX-150K	*Kit*	$43.95

Diskettes

DISKETTES - Jade

Bargain prices on magnificent magnetic media

5¼" single sided, single density, box of 10

MMD-5110103	*Soft sector*	$27.95
MMD-5111003	*10 sector*	$27.95
MMD-5111603	*16 sector*	$27.95

5¼" double sided, double density, box of 10

MMD-5220103	*Soft sector*	$39.95

8" single sided, single density, box of 10

MMD-8110103	*Soft sector*	$33.95

8" single sided, double density, box of 10

MMD-8120103	*Soft sector*	$39.95

8" double sided, double density, box of 10

MMD-8220103	*Soft sector*	$49.95

Video Monitors

9" B & W MONITOR - A.P.F.

High quality, high resolution video monitor

VDM-750900	*9" monitor*	$159.95

13" COLOR MONITOR - Zenith

The hi res color you've been promising yourself

VDC-201301		$449.00

12" GREEN SCREEN - NEC

20 MHz, P31 phosphor video monitor with audio, exceptionally high resolution - A fantastic monitor at a very reasonable price

VDM-651200	*12" monitor*	$259.95

Mainframes

MAINFRAME - Cal Comp Sys

12 slot S-100 mainframe with 20 amp power supply

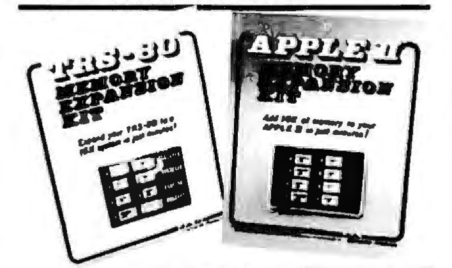
ENC-112105	*Kit*	$359.95
ENC-112106	*A & T*	$419.95

DISK MAINFRAME - NNC

Holds 2 8" drives and an 8 slot S-100 system. Attractive metal cabinet with 8 slot motherboard, power supply, fan, key switch, and other professional features

ENS-112320	*with 30 amp p.s.*	$699.95

Accessories-Apple/TRS-80



16K MEMORY UPGRADE

Add 16K of RAM to your TRS-80, Apple, or Exidy in just minutes. We've sold thousands of these 16K RAM upgrades which include the appropriate memory chips (as specified by the manufacturer), all necessary jumper blocks, fool-proof instructions, and our 1 year guarantee.

MEX-16100K	*TRS-80 kit*	$29.00
MEX-16101K	*Apple kit*	$29.00
MEX-16102K	*Exidy kit*	$29.00

DISK DRIVE for APPLE

5¼" disk drive with controller for your Apple

MSM-12310C	*with controller*	$499.95
MSM-123101	*w/out controller*	$375.00

DISK DRIVES for TRS-80

23% more storage, 8 times faster, 40 track with free patch. 120 day warranty, includes case, power supply, and cable

MSM-12410C	*Save $125.00 !!!*	$299.95

DOS 3.3 UPGRADE - Apple

Upgrade your old DOS to the improved 3.3

IOD-2233A	*Complete kit*	$64.95

APPLE STICK - Micromate

Joy stick with pots for Apple II

SYA-1510A	*A & T*	$35.95

Z-80* CARD for APPLE

Z-80 CPU card with CP/M 2.2 for your Apple*

CPX-30800A	*A & T*	$279.95

AIO - S.S.M.

Parallel & serial interface for your Apple

IOI-2050K	*Kit*	$155.95
IOI-2050A	*A & T*	$194.95

PRINTER INTERFACE - C.C.S.

Centronics type I/O card w/ firmware

IOI-2041A	*A & T*	$99.95

APPLE CLOCK - Cal Comp Sys

Real time clock w battery back-up

IOK-2100A	*A & T*	$109.95

Modems

★★★★★★★★★★★★★★★★★★★★★★★★★★★

LEX-11 MODEM - Lexicon

A real star! 300 baud, answer/originate, RS 232C

IOM-5511A	*Best buy !!!*	$128.00

★★★★★★★★★★★★★★★★★★★★★★★★★★★

NOVATION CAT

300 baud, answer/originate acoustic modem

IOM-5200A	*1 year warranty*	$179.00

D-CAT 300 baud, direct connect modem

IOM-5201A	*Special sale price*	$189.00

AUTO-CAT Auto answer originate, direct connect

IOM-5230A	*Special sale price*	$239.95

MICROMODEM - D.C. Hayes

Auto answer/dial modem card for Apple or S-100

IOM-2010A	*Apple modem*	$349.95
IOM-1100A	*S-100 modem*	$375.00

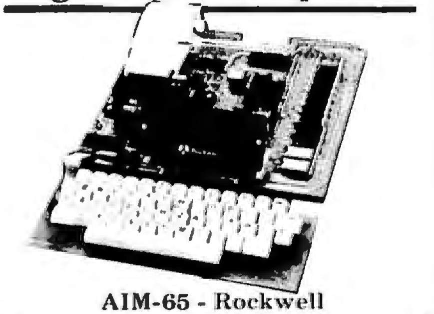
MICRONET MODEM - Micromate

Direct connect with extra features - a best buy

IOM-2020A	*Best Apple modem*	$275.00

* Z-80, Z-80A, and the letter Z are recognized trademarks of Zilog, Inc. *CP/M is a registered trademark of Digital Research Corp. *CBASIC is a trademark of Compiler Systems, Inc.

Single Board Computers



AIM-65 - Rockwell

6502 computer with alphanumeric display, printer, & keyboard, and complete instructional manuals

CPK-50165	*1K AIM*	$374.95
CPK-50465	*4K AIM*	$449.95
SFK-74600008E	*8K BASIC ROM*	$99.95
SFK-64600004E	*4K assembler ROM*	$84.95
PSX-030A	*Power supply*	$64.95
ENX-000002	*Enclosure*	$49.95

4K AIM, 8K BASIC, power supply, & enclosure

Special package price **$625.00**

Z-80* STARTER KIT - SD Systems

Complete Z-80 computer with RAM, ROM, I/O, display, keyboard, manual, and kluge area.*

CPS-30010K	*Kit*	$369.95
CPS-30010A	*Jade A & T*	$459.95

MICROPROCESSORS

Z-80	10.95
Z-80A	12.95
6502	11.50
6800	11.95
6802	17.95
6809	39.95
8035	24.00
8080A	6.59
8085	15.95
8748	59.95

Z-80 SUPPORT

3881 *PIO*	9.50
3881-4 *PIO-4 MHz*	14.50
3882 *CTC*	9.50
3882-4 *CTC-4 MHz*	14.95
3883 *SIO*	29.50
3884 *SIO*	49.50

BAUD RATE GENERATORS

MC14411	10.00
1.843 MHz xtal	4.95

UARTS

AY5-1013A	5.25
AY3-1014A	8.25
TR1602B	5.25
TMS6011	5.95
IM6402	9.00

6800 SUPPORT

6821P	5.95
6828P	11.95
6834P	22.50
6840P	18.75
6850P	4.80
6852P	5.79
6875L	7.40
68488P	25.00

PROMS

2708 *450ns*	6.25
10 for $4.90 ea	
2716 *12.5v*	11.95
2716 *5v*	11.95
10 for $8.90 ea	
2532 *5v*	39.95
2732 *5v*	39.95
2758 *5v*	9.95

RAMS

21L02 *2 MHz*	1.25
21L02A *4 MHz*	1.50
2114L *2 MHz*	3.75
2114LA *4 MHz*	3.95
4116	4.25
4164 *64K x1*	59.95
5257 *2 MHz*	6.75
5257A *4 MHz*	7.25
MK4118	18.95

SUPPORT DEVICES

8212	3.25
8214	4.65
8216	2.95
8224	3.25
8224-4	5.75
8226	3.85
8228	4.95
8238	4.95
8243	8.00
8250	14.95
8251	6.50
8253	17.95
8255	6.50
8257	19.95
8259	17.95
8275	49.95
8279	15.95

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Continental U.S.	*Inside California*
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For Technical Inquiries or Customer Service call

213-973-7707

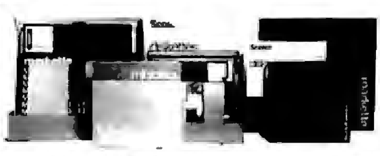
JADE
Computer Products
4901 W. Rosecrans, Hawthorne, Ca 90250

TERMS OF SALE: Cash, checks, credit cards, or Purchase Orders from qualified firms and institutions. Minimum order $15.00. California residents add 6% tax. Minimum shipping and handling charge $3.00 **Pricing and availability subject to change without notice.**

Circle 330 on Inquiry card.

California Digital

Post Office Box 3097 B • Torrance, California 90503



DISKETTES

FREE PLASTIC LIBRARY CASE INCLUDED WITH THE PURCHASE OF EVERY BOX OF DISKETTES

Private labeled for California Digital by one of the most respected producers of magnetic media. Each diskette is certified double density at 40 tracks. To insure extended media life each diskette is manufactured with a reinforced hub-hole. And of course, a plastic library case is included with every box of diskettes. MMD-CDS(01)(10) Please specify computer or required sectors.

$24.95 BOX

Ten boxes $22.75 One hundred boxes $21.50

MINIDISKETTES	Box	10 boxes		Box	10 boxes
Memorex 3401	$27.00	$25.00	Scotch 744(0)(10)(16)	$31.00	$20.00
Verbatim 525(01)(10)	29.00	27.00	Dysa	45.00	43.00

EIGHT INCH	Scotch	box	10 bx.	Dysan	box	10 bx.	MRX	box	10 bx.
Single side/single den.	740-0	$33.	$33.	3740/1	$49.	$47.	3060	$45.	$43.
Single side/double den.	741-0	45.	43.	3740/1d	75.	73.	3090	37.	35.
Single side/32 sector	740-32	35.	33.	na.			na.		
Double side/ double D.	743-0	65.	59.	na.			3115	49.	48.

SCOTCH brand head cleaning kit. $24.95 MMA-CK(5)(8) please specify 5 1/4 8"

Prices available on request for: tape, cartridges, diskpacks, volume diskettes.

MEMORY

TRS-80 APPLE II $29

16k memory (8) 4116's

Installation is simple. Anyone who has ever changed a spark plug should be able to up-grade his microcomputer. How can California Digital offer these memory up-grade sets at 25% below our competition? Simple, we buy in volume, wholesale to dealers and sell the balance directly to owners of personal micro-systems. These 16K dynamic memory circuits are factory prime and unconditionally guaranteed for one full year. NOW, before you change your mind, pick up the telephone and order your up-grade memory from California Digital. Add $3 for TRS80 jumpers.

STATIC	1-31	32-99	100-5C	-999	1K+
21L02 450nS.	1.19	.99			
21L02 250nS.	1.49	1.39		*	*
2114 1Kx4 450	5.95	5.50	5.25	4.75	4.50
2114 1Kx4 300	8.95	8.50	8.00	*	*
4044 4Kx1 450	5.95	5.50	5.25	*	*
4044 4Kx1 250	9.95	9.50	9.00	*	*
4045 1Kx4 450	8.95	8.50	8.00	*	*
4045 1Kx4 250	9.95	9.50	9.00	*	*
5257 low pow.	5.95	5.50	5.00	4.80	4.60

2716 EPROM SALE $9.95

We have slashed price in an effort to reduce our over stocked inventory. These are single five volt EPROMs manufactured by one of the Worlds largest producers of semiconductors. All are first quality prime devices. Ceramic 450 nS.

FREE

Ultra-Violet Products UVS 11-E

UV EPROM ERASER

With purchase of FORTY 2716 EPROM's

$79 value

NEW from Shugart Technology 5 Megabyte Hard Disk Drive

Packaged in the same physical size as the industry standard 5 1/4" minifloppy disk drive. The micro-Winchester stores thirty times as much data (6.38 megabytes unformatted). accesses data twice as fast (170 milliseconds) and transfers data twenty times faster (5.0 megabits per second.).

The ST506 is factory sealed to protect the media from environmental contaminates. Requires only DC voltage.

Dual California Digital 5 1/4" enclosure. ST506 drive and power supply. **$1500**

Shugart Associates SA400 removable media disk drive for above package. add: **$300**

S-100 & Apple controller scheduled for spring release.

Shugart Associates

$395

801/ R Disk Drive 15 lbs.

Shugart 801/R with CP206 power supply, muffin exhaust fan, complete in dual enclosure with all the necessary harnessing cables. Documentation included. 30 pounds. MSD-1801 **$795**

Same as above but with two Shugart 801R disk drives. 50 pounds. MSD-2801 **$1195**

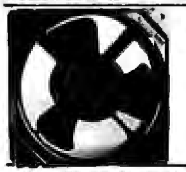
Disk drive cable. 6 feet 50 conductor with edge card connector at both ends. WCA-8505 $25.00

Export Disk drives. 220V. 50MHz add $50.00 per disk drive.

BSR SYSTEM X-10

The new BSR timer runs your home just like clockwork. Turns on lamps and appliances while your away from home. Completely compatible with your existing System X-10 devices.

BSR Timer eight channel	$65.00	Appliance Module 500 W.	$13.95
Master control console	34.95	Lamp Module 300 Watts	13.95
Ultrasonic Controller	19.95	NEW full control wall switch	14.50



Rotron Wisper Fan

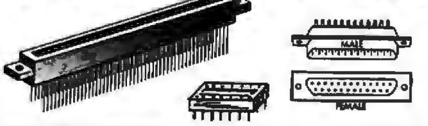
$14.77

115 VAC. 7 Watts WR2A1

Factory fresh Muffin fans

NOT pull-outs. EMF-4M

CONNECTORS



GOLD EDGE CONNECTORS

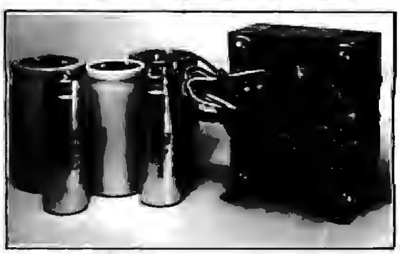
S-100 .125" centers	each	10+
Imsai solder .250" row	$2.95	$2.50
Imsai wire wrap (TI)	3.95	3.50
Sullins Hi-Rel. .250"	4.50	4.00
Sullins Hi-Rel. W/W	5.35	4.90
Sullins /Altair .140"	4.95	4.50
.156" Centers (standard)		
22/44 Kim Eyelet	2.50	2.15
36/72 Digital Group S/T	5.95	5.50
36/72 Digital Group W/W	6.60	6.15
43/86 Motorola 6800S/T	6.60	6.15
43/86 Moto. 6800 W/W	7.00	6.85

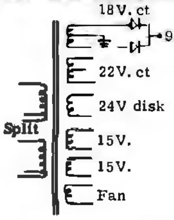
INTEGRATED CIRCUIT SOCKETS

	Low Profile		Wire Wrap	
	each	100+	each	100+
8 pin	$.10	$.09	$.46	$.41
14 pin	.10	.09	.45	.41
16 pin	.12	.11	.50	.45
18 pin	.15	.13	.68	.61
24 pin	.25	.24	.94	.87
40 pin	.42	.40	1.60	1.47

"D" Type	each	10-24	25+
DE9P male	$1.60	$1.40	$1.30
DE9S female	2.25	2.00	1.00
DE hood	1.50	1.35	1.20
DA15P male	2.35	2.15	2.00
DA15S female	3.25	3.10	2.90
DA hood 2/P	1.60	1.35	1.30
DB25P male	2.50	2.35	2.25
DB25S female	3.35	3.15	3.05
DB hood 2/P	1.35	1.15	1.05
DC37P male	4.20	4.00	3.70
DC37S female	6.00	5.75	5.50
DC hood 2/P	2.25	2.00	1.75
DD50P male	5.50	5.10	4.75
DD50S female	9.40	8.60	8.00
DD50 hood 2/P	2.60	2.40	2.10
CENTRONICS			
57-30360	7.95	6.75	5.75
RIBBON CABLE CONNECTORS			
17/34 5" disk	4.85	4.55	3.95
20/40 TRS-80	6.65	5.05	4.70
25/50 8" disk	5.90	5.15	4.00

SURPLUS





S-100 POWER SUPPLY KIT

$59

Kit contains five high current bridge rectifiers. five computer grade electrolytic capacitors and a 700+ watt split primary transformer (110/220V.)

The supply is capable of supporting a full 30 Amp S-100 system along with (2) eight inch disk drives.

Electrolytic capacitors consist of: one each 83,000 uF/15V: 34,000uF/40V: 26,000uF/30V: and Two 12,000/30V.

All components are new surplus acquired from excess inventory of the National Cash Register Company.

Please place your order early, at this low price we expect this kit to be a quick sell out. SPC-PW100. ...Shipping: East of Mississippi add $15.00 California add $8.00 all other states please add $11.00 Foreign $21.00

DATA INPUT TERMINAL

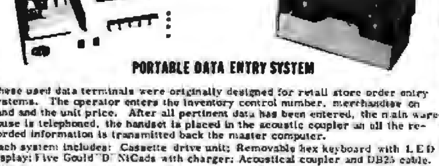
This Keystation terminal was recently acquired from the CMC division of the Pertec Corporation. The unit was originally designed for inputing data directly onto magnetic tape.

The system is comprised of a premium cast aluminium and fiberglass enclosure. along with a Honeywell / Microswitch hall effect keyboard. Thirty display lamps advise the operator of the systems status. Four inch loud speaker acknowledges acceptance of data and alerts the operator of pending problems.

But most of all this "USED" terminal, with a little imagination, can be engineered to make the perfect home for an S-100 computer and video display; or with slight modification will accept the Rockwell AIM-65 micro/computer.

Five volt regulated power supply is available for an additional $20. (see June Byte) All units are in excellent condition. Original acquisition over $700. 22 lbs.

$139.50



PORTABLE DATA ENTRY SYSTEM

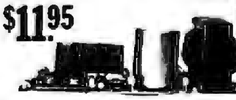
These used data terminals were originally designed for retail store order entry systems. The operator enters the inventory control number, merchandise on hand and the unit price. After all pertinent data has been entered, the main warehouse is telephoned, the handset is placed in the acoustic coupler an all the recorded information is transmitted back the master computer.

Each system includes: Cassette drive unit; Removable hex keyboard with L E D display; Five Gould "D" NiCads with charger; Acoustical coupler and DB25 cable.

All units removed from service in working condition. Original cost over $2,500.

Regulated Power Supply 5 VOLT 5 AMP

$11.95



This USED surplus power supply was removed from working equipment. Pass transistor regulation outputs five volts at a conservative five amps. Suitable for T T L hobby applications. SPC-PS1 8 pounds.

$59 Sankyo Magnetic Card Transport

This Sankyo card transport is capable of storing and retrieving over 400 characters of data from a single 2 x 4 HP style magnetic data card. Motorized mechanism pulls the magnetic card across the four channel read/write head in under two seconds. Ideal for any data processing application where small amounts of information must be randomly retrieved. Original cost over $200.00 Documentation and sample card included. New surplus. SPC-SCR

WESTERN UNION ENCLOSURE

These enclosures were manufactured for Western Union by Universal Technology. The exact purpose of the product is still a mystery but the enclosure is ideally suited for an S-100 motherboard with shielded power supply. Removable hood and plexiglas front make this enclosure an attractive home for any hobby product. New surplus in factory boxes supplied with three 22/44 edge connectors; DB 25S communications connector; six foot grounded power cord and more. Inside dimensions: 19" x 10 1/2" x 6 7/8". Shipping weight 8 lbs.

$24.95

VISA

master charge

All merchandise sold by California Digital is premium grade.
Shipping: First five pounds $2.00; each additional add $.40
Foreign orders 10% shipping. Excess will be refunded.
California residents add 6% sales tax. COD's discouraged.
Open accounts extended to state supported educational institutions and companies with a "Strong Dun & Bradstreet."
Warehouse: 15608 Inglewood Blvd. Visitors by appointment.

TOLL FREE ORDER LINE

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TECHNICAL & CALIFORNIA

(213) 679-9001

California Digital

Post Office Box 3097 B • Torrance, California 90503

MEMOREX 8"DISKETTES

$25 WITH FREE LIBR RY CASE

Recently the Memorex Corporation had a cancellation on a contract for a truck load of eight inch diskettes. California Digital was fortunate to be offered this load of prime magnetic media.

These diskettes are "UNBRANDED" but are guaranteed first quality Memorex Brand. (+3060 single den.)

Like all diskettes sold by California Digital, a library case is supplied free with the purchase of every box.

This offer is subject to remaining inventory on hand.

SUPER BUY

IBM 3101 DISPLAY TERMINAL

The new 3101 display terminal is the IBM entry into the plug compatable micro computer industry.

This modularly constructed CRT terminal has been engineered with the user in mind. The video display module's swivels and tilts to provide the operator with a comfortable viewing posture.

Twelve inch P-39 green phosphor screen boasts a crisp 7 by 14 character matrix.

Standard 80 by 24 line screen format with a 25th line to display machine status and aid in the diagnostics in the event of a system malfunction.

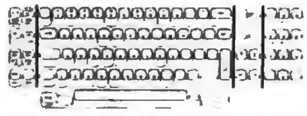
87 key Selectric style keyboard arrangement along with numeric entry pad. Eight user definable function keys.

The 3101 video terminal is RS232 compatable and displays all 128 ASCII characters including control codes.

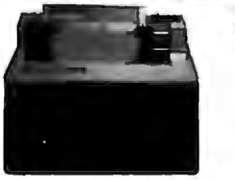
Accessible customer setup switches aid in choosing such options as line speed, parity scroll, and reverse video.

But most of all, built into every 3101 terminal is the quality that you have learned to expect from the IBM Corporation. VDT-3101

IBM direct price $1295
CALIFORNIA DIGITAL discount price
$1195 Immediate delivery



NEW from INTEGRAL DATA 460 Paper Tiger with GRAPHICS $1150



The 460 Paper Tiger uses a dot matrix character formation technique in which the placement of the dots overlap both horizontally and vertically to achieve a correspondence quality printing.
The printer's nine-wire print head uses staggered needle rows to create the vertically overlapping dots. The head is driven bi-directionally under microprocessor control by a stepper motor driven mechanism.
"Two K" buffer allows the printer to accept the entire content of a 1,920 character CRT screen. With graphics suggested retail price $1.395 27 lbs. PRC-460G

NEC Spinwriter 5510P/S $2795

The word processing quality Spinwriter prints at speeds upto 55 characters per second. The Model 5510 P/S is supplied with both parallel and RS-232 serial interfacing. Also included is the tractor feed mechanism, along with print thimble and ribbon. PRN-5510PS 70 lbs. Keyboard (KSR) Model 5520 P/S available $2995. PRK-5520 PS 75 lbs.

TEC V-300 Word Processing DaisyWheel Printer $1595

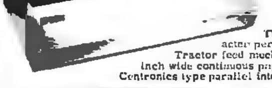
Finally a reasonably priced letter quality printer... Bi-directional printing at 25 characters per second. Full 136 print positions wide. Proportional spacing 1/120" horizontal, 1/48" vertical.
Uses standard Diablo brand interchangable daisy print wheels.
Intel 8085 CPU microprocessor controlled. Interfaces via Centronics parallel connector. Shipping 58 lbs. PRV-300.

TELETYPE® MODEL 43

4320 KEYBOARD MODELS

TTL serial output	AAA	$ 995
RS232 serial	AAK	1050
Friction 80 column	AAE	1100
Friction 80 RS232	AAL	1195
Bell 103 Modem	AAB	1495

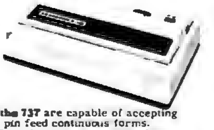
EPSON MX-80 $495



The MX-80 is a 9 x 9 80 character per second dot matrix printer. Tractor feed mechanism adjusts to accept ten inch wide contiuous paper. Requires "Eight bit" Centronics type parallel interfacing. PRE-MX80 17 Lb.

CENTRONICS

730 $595
737 $750

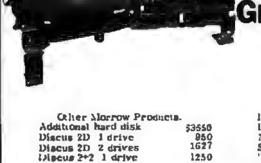


Both the Centronics 730 and the 737 are capable of accepting standard office letterhead or pin feed continuous forms. For higher resolution the 737 implements a nine wire dot matrix print head. Parallel interfacing. Add $65 for RS232. PRC-730P (S). PRC-737P (S) 17 lbs.

HEWLETT PACKARD $2650

The Hewlett Packard HP-85 is a complete, low cost portable computer system. This self contained package includes CPU, keyboard, printer, CRT display and cassette tape drive. SYS-HP85 30 lbs.

26 Megabyte Hard Disk Drive from GEORGE MORROW'S Thinker Toys $3950



Other Morrow Products.			
Additional hard disk	$3550	Disc Jockey 2D controller	$345
Discus 2D 1 drive	950	Disk Jockey 1 Controller	195
Discus 2D 2 drives	1627	M26 hard disk Controller	625
Discus 2+2 1 drive	1250	Switchboard interface	219
Discus 2+2 2 drives	2237	"New" Multiboard	275
		M-10 Ten Megabyte hard	2550

AMPEX DIALOGUE 80 CRT TERMINAL $995

New from the Ampex Corporation. The Dialogue 80 features removable keyboard, displayable two pages (four optional) dual program keys, half intensity protected fields and status line. Transmits data either block, line or character mode. Excellent value. VDT-D80 shipping 47 lbs.

BMC VIDEO MONITOR $259

Green phosphor with 18 MHz bandwidth, composit video input make the BMC KG-12C an ideal monitor for anyone requiring a high resolution 12" display.
High impact plastic enclosure assures that the BMC monitor is a rugged take anywhere instrument. For added protection the unit is equipped with a removable smoked non-glare plexiglas screen. VDM-BMC 18 lbs.

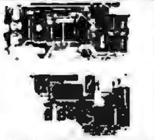
direct connect MODEM Your Choice $169

Direct connect modems eliminate loss of information due to the carbon compression associated with acoustic modems. Choose either of these two great units.

The Universal Data Systems 103LP is switch selectable between answer and originate modes. Fully Bell 103 compatable. Directly connects to the new modular telephone jack. 100% powered from the telephone line. No need to locate modem in proximity to A.C. power recepticle. MOD-103LP 2 pounds.

Novation D Cat connects to most of the new Bell modular handsets. Ideal for multiple line office telephones. Requires external A.C. power. MOD-DCAT 2 Lb.

ACCESSORIES FOR THE APPLE COMPUTER

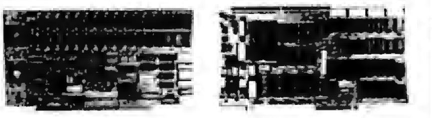


CALIFORNIA COMPUTER SYSTEMS	
Arithmetic Processor 7811 B/C	$319
Asynchronous serial interface 7710	129
Centronics Interface card 7728	95
12K PROM Module 7114	69
Calender/Clock, Bat. back-up 7424	99
Parallel Interface 7720A	99
Programable Timer 7740A	99
Analog/Digital converter 7470A	99
MICROSOFT PRODUCTS	
Apple to Z-80 CPU card	379
D.C. HAYES PRODUCTS	
Micromodem for Apple	319
COMPUTER STOP PRODUCTS	
Double Vision / 80 Column Video	250
INTERACTIVE STRUCTURES	
16 Channel A/D card AIO/2	275

MOUNTAIN COMPUTER PRODUCTS	
Intro X-10 system for BSR	$239
Intro X-10 card only	165
16 channel AD/DA 8 bit	319
Apple Clock battery back-up	225
Supertalker SD200	245
ROM Plus with filter	165
ROM Writer/Programmer	119
APPLE BRAND PRODUCTS	
Apple Language card	450
Floppy disk with controller	560
Floppy disk without controller	495
Apple parallel interface	175
SSM MICROCOMPUTER	
Dual serial parallel interface AIO	
SORRENTO VALLEY ASSOCIATES	
8" floppy controller (Pascal)	360

S-100 BOARDS

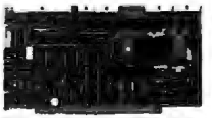
Assembled • Tested • Burned-in



MEASUREMENT SYSTEMS	
Dynamic memory DMB-6400	$770
Dynamic memory DMB-3200	700
GODBOUT/COMPUPRO	
Dual 8088/8085 16 bit CPU	375
Z-80 CPU 24 bit address 4 MHz	239
Static RAM 32K (Alpha Micro)	575
Spectrum color graphics board	329
Interfacer II I/O board	199
SEATTLE COMPUTER PRODUCTS	
8086 16 bit CPU 2 card set/86 dos	595
CALIFORNIA COMPUTER SYSTEMS	
S-100 Mainframe 2200A	329
Disk controller/2.2 CPM 2422	329
Z-80 CPU 4MHz DMA 2810A	250
DIGITAL RESEARCH	
32K 2716 EPROM board	99
EPROMS for above 2716 16 req.	13
CALIFORNIA DATA CORPORATION	
A/D board 16 channel 12 bits	
QT COMPUTER SYSTEMS	
Real time clock/calendar	135

MORROW / THINKER TOYS	
Multiboard "NEW" Daisy wheel port, real time clock, power on jump, program interrupt cont'l 3P/3S	$275
Switchboard interface 4P/2S	219
Disk Jockey 1 disk controller	195
Disk Jockey II double density	375
SD SALES	
PROM-100 programmer	
Video display board 8024	
Versafloppy 3740 controller	
MULLEN PRODUCTS	
Extender board/Logic probe (kit)	49
Relay Opto/control board	149
D. C. HAYES PRODUCTS	
Micromodem S-100 FCC register	375
ARTEC ELECTRONICS	
Wire Wrap proto board WW/100	22
General Purpose proto GP/100	22
CALIFORNIA DIGITAL	
8086 CPU 4K on board static RAM	450

TELETEK SINGLE BOARD COMPUTER FLOPPY DISK CONTROLLER



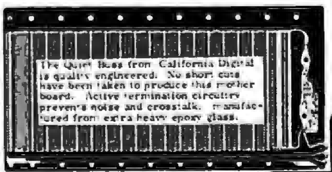
The FDC-1 features the Z-80 CPU along with the NEC 765 floppy disk controller. The board supports both single or double density 5 1/4 or 8" disk drives. Two serial (45-9600bd) and two parallel ports add to the flexibility of this single board computer. Other standard features are realtime clock, reset jump to monitor, vectored interrupts and potential for controlling a Winchester hard disk drive. With the addition of an external 25 volt power supply the Teletek board becomes capable of programing 2716 EPROMS. SBC-FDC1

$695

S-100 Mother Board $35

Quiet Buss™

8803-18
18 slot
IMSAI



The Quiet Buss from California Digital is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy epoxy glass.

All merchandise sold by California Digital is premium grade.
Shipping: First five pounds $2.00; each additional add $.40
Foreign orders 10% shipping. Excess will be refunded.
California residents add 6% sales tax. COD's discouraged.
Open accounts extended to state supported educational institutions and companies with a "Strong Dun & Bradstreet."
Warehouse: 15608 Inglewood Blvd. Visitors by appointment.

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TECHNICAL & CALIFORNIA
(213)679-9001

Circle 321 on inquiry card.

IMAGINE THE 8 INCH FLOPPY

315K BYTES PER SIDE ON 5 1/4" OF COURSE! Micropolis, the worlds largest manufacturer of high density 5 1/4" disk drives, has been doing it for years. And reliably at that.

An ordinary 5 1/4" floppy provides just 35 tracks per side, and stores only 70K bytes. This is not nearly enough for anything useful, so instead, Micropolis uses 77 tracks per side. Each track is then formatted with 16 sectors (hard) at 256 bytes per sector yielding an impressive 315K bytes per side.

Micropolis drives have a larger capacity than many 8" disk drives, though it only occupies the space of a 5 1/4" floppy. The 315K byte capacity is roughly 4 times the capacity of a standard 5 1/4" drive. This is what we call QUAD DENSITY.

To achieve the high density capability, you may think Micropolis had to sacrifice speed or reliability. NOT SO! The track to track access time is only 30us with a high speed data transfer rate of 250,000 bits per second.

By creating this high density format, Micropolis is able to keep your initial subsystem costs to a minimum. Your cost is less than $.002 per byte. Thats a BIG VALUE in a small package.

MICROPOLIS disk subsystems are expandable to keep up with your ever increasing needs. Up to four drives/heads may be daisy-chained on one S-100 controller board. With all four drives/heads in operation, you have access to over 1.2 MEGABYTES of on-line storage.

WITH MICROPOLIS, complete means COMPLETE. Each subsystem comes complete with controller interface, cable, and software. The software includes the MDOS operating system, extended basic, assembler and editor. Everything you need to get "On Line" in one complete package.

MICROPOLIS provides total integration which means they control everything from beginning to end. The result is a better drive for you, backed by a full 120 day factory guarantee.

Anyone can cut price by cutting out capacity or valuable features. But there's no long term advantage in it. Not for the user. Or the builder.

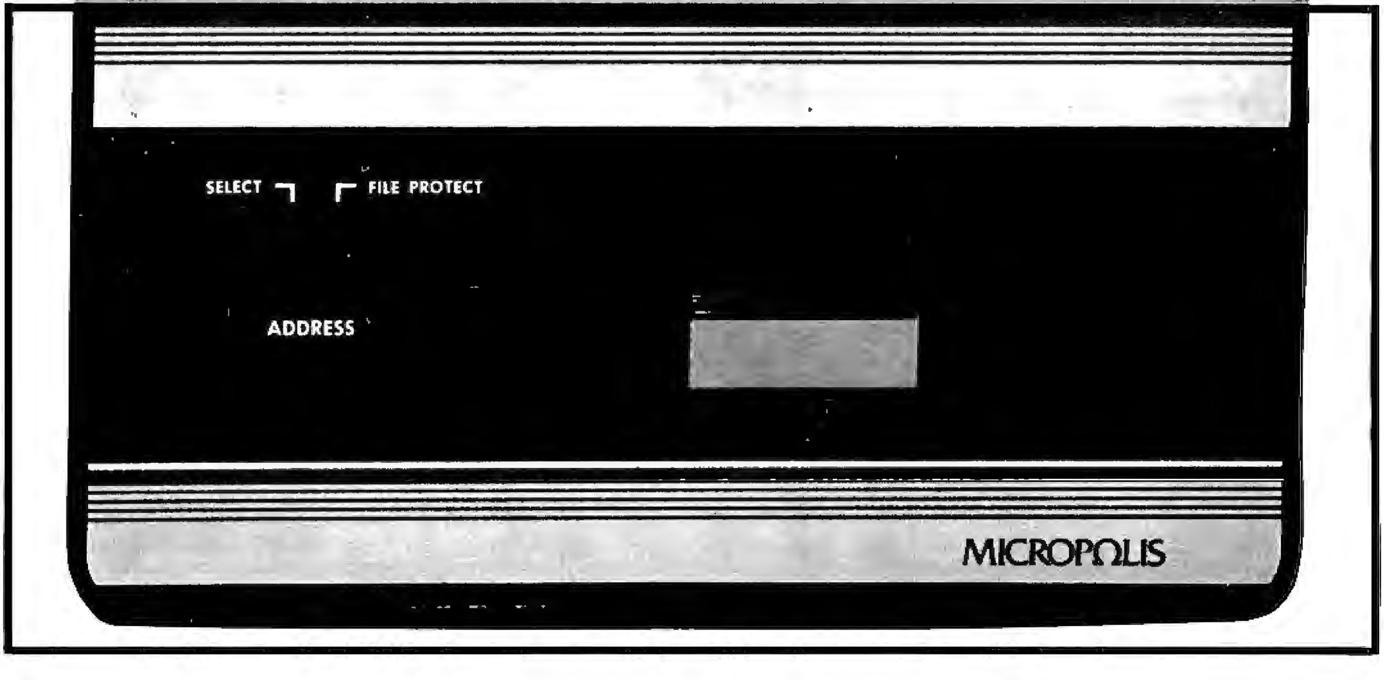
MICROPOLIS takes a better approach, even though it's harder, using advanced design to provide more capability while also lowering cost.

For example, most 5 1/4-inch floppy disks cut costs by using a cheap, less accurate plastic cam or cam follower to position the read/write head. Most 8-inch floppy disks use a better approach, with a rolled steel lead screw for this function.

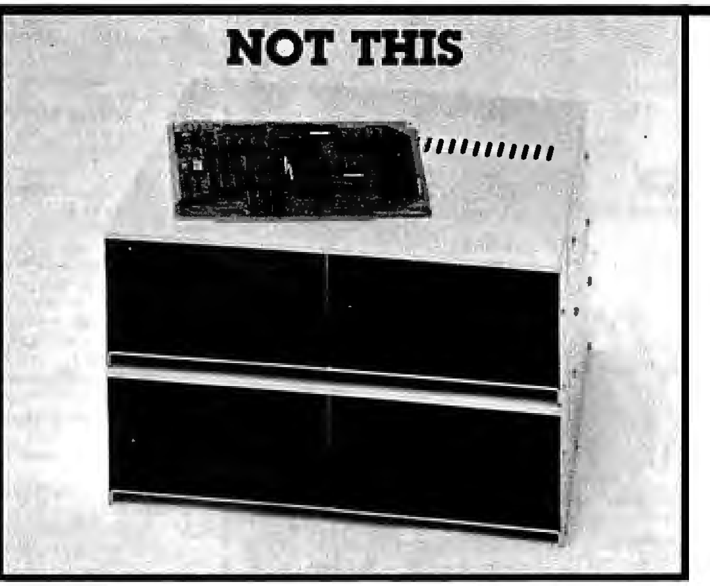
We go them one better and use an all-steel system, with a precision-ground steel lead screw and steel follower. It costs more but gives us greater storage capacity with lower cost per thousand bytes. Not so incidentally, our steel construction (compared to plastic) significantly increases reliability, too. There's even a built-in File Protect feature that prevents accidental loss of valuable data. (A file protected diskette cannot be written on.)

Heat can cause numerous read and write errors that can become hazardous to your data. The major heat producing power supply components are mounted to a large heat sink, external to the cabinet, by the power switch and fuse (located at the rear of the cabinet). This design is to assure that the drive components are kept as cool as possible to assure reliable data recovery.

MICROPOLIS has a reputation for getting along with most everybody. Compatability is not a problem with MICROPOLIS. Their disk drives and/or subsystems can be easily integrated into systems such as Polymorphic, Cromemco, CCS, Ithica Intersystems, Godbout, Northstar, Jade Big Z, QT SBC 2/4, and many others. Many OEM manufacturers rely on MICROPOLIS to get the job done efficiently. Companies like Commodore, Exidy, Harris, and Vector Graphics to name just a few. Years from now, you can look back with a secure feeling knowing you made the best choice, MICROPOLIS.



CAPACITY OF AN IN 5 1/4" FORMAT



Because of our incredible purchasing power, PRIORITY ONE ELECTRONICS is able to buy MICROPOLIS disk drives by the thousands and receive special pricing. That special pricing we receive is passed on to you in the form of tremendously discounted prices. Now all that remains is for you to take advantage of this truly incredible buy.

MODEL	DESCRIPTION	LIST	SALE PRICE
S-100 SUB-SYSTEMS			
MCP-1053-4	1.2 MB 2 HEAD DUAL	$2605.00	**$1395.00**
MCP-1053-2	630 KB DUAL	$1895.00	**$995.00**
MCP-1043-2	315 KB SINGLE	$1145.00	**$695.00**
MCP-1041-2	315 KB SINGLE, NO PS	$1045.00	**$639.00**
MCP-1042-1	143 KB SINGLE	$795.00	**$625.00**
MCP-1041-1	143 KB SINGLE, NO PS	$695.00	**$595.00**
COMPLETE W/S-100 CONTROLLER, CABLES, MANUALS AND MICROPOLIS MDOS AND BASIC			
ADD-ON DRIVES			
MCP-1033-2	630 KB DUAL	$1395.00	**$895.00**
MCP-1023-2	315 KB SINGLE	$645.00	**$495.00**
MCP-1021-2	315 KB SINGLE, NO PS	$545.00	**$475.00**
MCP-1022-1	143 KB SINGLE	$545.00	**$375.00**
MCP-1021-1	143 KB SINGLE, NO PS	$445.00	**$360.00**
REQUIRES ACCESSORY ADD-ON CABLES			

GOOD NEWS FOR TRS-80* OWNERS

We now have a complete line of TRS-80* Model 1 compatible MICROPOLIS add on drives in matching colors. These drives simply plug into the expansion interface via a disc data cable.

197K BYTES PER SIDE FOR YOUR TRS-80*, that's easy! Just order a 77 track add on drive and the New DOS-80 operating system. Among the many features of New DOS-80, is its ability to control any mix of 35, 40, or 77 track drives on the same cable.

TRS-80® DISK DRIVES

MCP-1027-1	35 TRACK SINGLE	$545.00	**$279.95**
MCP-1037-1	35 TRACK DUAL	$1195.00	**$695.00**
MCP-1027-2	77 TRACK SINGLE	$645.00	**$439.00**
MCP-1037-2	77 TRACK DUAL	$1395.00	**$795.00**

ACCESSORIES

APP 395M	NEW DOS/80 TRS-80* 35 thru 77 TRACK OPERATING SYSTEM	SUPPLIED 35 TRACK $149.00	**ON 77 TRACK $159.00**
PR1-34CEEE-2	Two Drive Data Cable		**$29.95**
PR1-34CEEE-4	Four Drive Data Cable		**$39.95**

GOOD THRU MARCH 1981

THIS COULD BE THE START OF SOMETHING SMALL.

1-800-423-5633 *PRIORITY ONE ELECTRONICS* **(213) 894-8171**

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Terms: Visa, MC, BAC, Check, Money Order, U.S. Funds Only. CA residents add 6% sales tax, Minimum order $15.00 Prepaid U.S. orders less than $75.00 include 5% shipping and handling. MINIMUM $2.50. Excess refunded. Just in case ... please include your phone no. Prices subject to change without notice. We will do our best to maintain prices thru March 1981.

*SOCKET and CONNECTOR prices based on GOLD, not exceeding $700 per oz.

*Sale Prices are for prepaid orders only. Credit card orders will be charged appropriate freight

*TRS-80 is a registered trademark of Tandy Corp.

Circle 322 on inquiry card

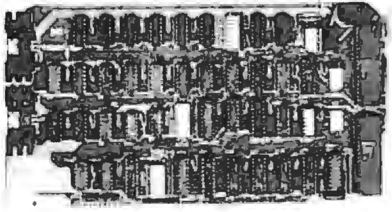
DETACH OUR CATALOG FROM THE NOV. BYTE

DETACH OUR CATALOG FROM THE NOV. BYTE

S-100 HEADQUARTERS

GODBOUT

THE DUAL PROCESSOR BOARD IS HERE!



GBT161 8085 CPU BOARD
GBT1612 8085/8088 CPU BOARD

- 8088 & 8085A CPU
- S-100 IEEE COMPATIBLE
- SWITCHABLE CPU'S
- 5 MHZ OR 2 MHZ SWITCHABLE
- POWER ON JUMP TO ANY 256 BYTE BOUNDARY
- POWER ON JUMP CAN BE DISABLED
- CPU CAN JUMP ON POWER ON ONLY OR POWER ON AND RESET.
- 24 BIT EXTENDED ADDRESSING
- IMSAI FRONT PANEL COMPATIBLE
- AVAILABLE WITH 8085A ONLY

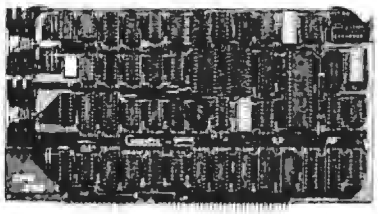
BOARD WITH 8085 ONLY

		List Price	Our Price
GBT161A	Assembled & Tested	$325.00	$305.00

BOARD WITH 8085 & 8088

GBT1612A	Assembled & Tested	$425.00	$399.00

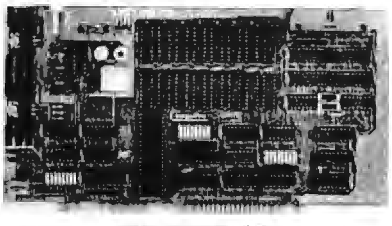
ENHANCED Z80 S-100 CPU BOARD



GBT160
Z80 CPU

- 4-6 MHz Z80 CPU
- IEEE S-100 Bus Compatible
- On Board Prom Sockets For Up To 8K Prom
- Power On Jump Start To Any 256Byte Boundary
- On Board Memory Manager For Direct Addressing For Up To 16 M-Bytes
- Fully Maskable Vectored Interrupts
- Wait State Generation For All Machine Cycles
- Bypassing Of All Supply Line To Suppress Transients
- All IC's Are Socketed

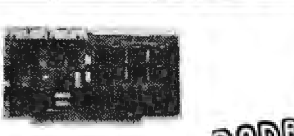
		List Price	Our Price
GBT160U	Unkit		$225.00
GBT160A	Assembled & Tested	$295.00	$280.00



SPECTRUM
S-100 COLOR GRAPHICS BOARD

- Uses the MC6847 LSI IC
- Uses 1372 color encoded/generator
- Alphanumeric/graphics in 8 colors
- Ultra dense 256 x 192 full graphics
- 8K bytes.on-board low power RAM
- One full duplex parallel I/O port with attention, enable & strobe bits with power for running joysticks, keyboards, etc.
- A parallel port for graphics mode control
- Board may be used as a 4MHz RAM for program storage

		LIST PRICE	OUR PRICE
GBT144U	UNKIT		$299.00
GBT144A	A&T	$399.00	$349.00
GBT20	SUBLOGIC UNIVERSAL GRAPHICS INTERPRETER SOFTWARE		$35.00



INTERFACER I

GODBOUT

Our I/O board gives you inparalleled flexibility and operating convenience. We include such features as:

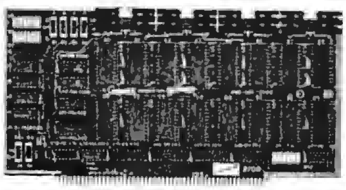
- 2 independently addressable serial ports (dip switch selectable addresses)
- Real LSI Hardware UARTs for minimum CPU housekeeping
- RS232C, current loop (20mA), & TTL signals on both ports
- Precision, crystal-controlled Baud rates up to 19.1 KBaud (Individually dip switch selectable)
- Transmit & receive interrupts on both channels, jumperable to any vectored interrupt line
- Industry standard RS232 level converters with five RS232 handshaking lines per port
- Optically isolated current loop with provisions for both on-board & off-board current sources
- UART parameters, interrupt enables, & RS232 handshaking lines are software programmable with power-on hardware default to customer specified hard-wired settings for maximum flexibility
- Port connectors mate directly to ribbon cable & DB25 connectors in standard pinouts
- RS232 lines will conform to either master or slave configurations
- Board gives full feature operation with both 2 & 4 MHz systems
- Low power consumption: +8V @ 450mA; +16V @ 150mA; -16V @ 70mA max.
- No software initialization required for board operation, although board parameters may be altered by software

		LIST PRICE	OUR PRICE
GBT133U	UNKIT		$199.00
GBT133A	A&T	$249.00	$219.00

INTERFACER II 3PTS

- 1 independently addressable serial port
- RS232C; 20mA current loop, & TTL signals
- Precision crystal controlled Baud rate generator
- Up to 19.2K Baud
- Transmit and receive interrupts, jumperable to and vectored interrupt line
- Five RS232 handshaking lines
- Optically isolated current loop
- 3 parallel I/O
- Utilizes LSTTL octal latches for latched I/O data with 24mA drive current
- Enable & strobe bits on each port (each with selectable polarity)
- Interrupts for each input port
- Separate 25 pin connector with power for each channel and a status port for interrupt mask & port status

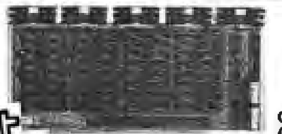
		LIST PRICE	OUR PRICE
GBT150U	UNKIT		$199.00
GBT150A	A&T	$249.00	$219.00



ECONOROM 2708

Has provisions for wait states for 4MHz operations. Configured as four 4K blocks—each independently addressable and disabable. Power-on jump. Does **NOT** include 2708s. Includes all support chips, sockets, regulators, heat sinks, etc. Sold in UNKIT form only. Shipping Weight 2 lbs.

GBT125U Unkit **$85.00**



GODBOUT

Order No.
GBT129A32

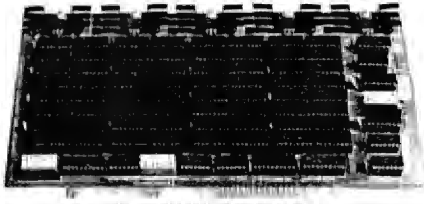
ECONORAM XA 32K RAM

- 4MHz with Z80
- 5MHz with 8085
- Assembled and Tested
- S-100 Compatible
- Fully Static
- 24 Bit Extended Addressing

Reg. $689.00

Sale Priced $429.00

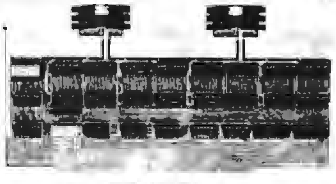
Static S-100 Memory



32K ECONORAM XX

32K Bank Select. IEEE S-100 compatible. Features one 32K block that can be addressed on 4K boundaries. Compatible with the IEEE proposed standard of 24 address lines as well as all currently used bank select configurations. Any or all of the eight 4K byte blocks may be disabled to create as many windows in memory to avoid any system memory conflicts.

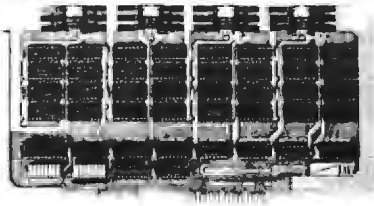
	List Price	Our Price
GBT164A16 16K RAM A & T	$399.00	$329.00
GBT164A24 24K RAM A & T	$539.00	$455.00
GBT164A32 32K RAM A & T	$699.00	$569.00



8K ECONORAM IIA

We realize that this may not look like the 8K. Econoram II board you've known and loved for so many years; however, at Godbout, good things don't come to an end—they just get better! Our NEW 8K Econoram IIA board retains all the best selling features of the old Econoram II PLUS is now 4 MHz STANDARD—still static—with ultra low power consumption. S-100 compatible. Single supply required—guaranteed maximum current under 900mA. Typical boards draw 700 to 800mA. Phantom feature is included on the new Econoram IIA & is switch selectable. Organized as two 4K independently addressable blocks. Includes switched WRITE protect—block & board disable. Also, has provision for memory management. Shipping Weight 2 lbs.

	List Price	Our Price
GBT139U Unkit		$159.00
GBT139A A&T	$189.00	$179.00



ECONORAM XIV

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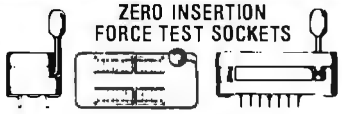

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RNS-16WWG	16	.65	.52	.50	.47	.44
RNS-18WWG	18	.85	.75	.70	.65	.60
RNS-20WWG	2C	1.00	.90	.80	.75	.70
RNS-22WWG	22	1.25	1.15	1.10	1.05	1.00
RNS-24WWG	24	1.25	1.15	1.10	1.05	1.00
RNS-28WWG	28	1.60	1.50	1.40	1.30	1.20
RNS-40WWG	40	1.85	1.65	1.55	1.45	1.35

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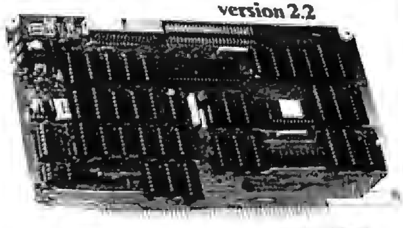
Per Track	41.7 kilobits	83.4 kilobits
IBM Format		
Per Disk	2.0 megabits	n/a
Per Track	26.6 kilobits	n/a
Transfer Rate	250 kilobits/sec.	500 kilobits/sec.
Latency (average)	83 ms	83 ms
Access Time		
Track to Track	8 ms	8 ms
Average	260 ms	260 ms
Setting Time	8 ms	8 ms
Head Load Time	35 ms	35 ms

CP/M
version 2.2



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VRB-MO 577-01	Soft Sector	77 Track Cert	S48.00
VRB-MO 577-16	Hard 16 Sector	77 Track Cert	S48.00
VR8-F032-1000	Hard Sector	Shugart 801R	S37.00
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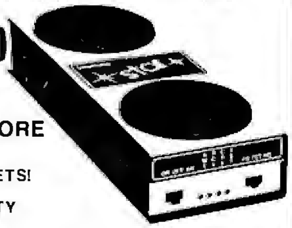

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The exclusive triple seal of Livermore's new flat mounted cups locks the handset into the acoustic chamber yielding superior acoustic isolation and mechanical cushioning. Designed to adapt to most common handsets used throughout the world, the STAR offers the utmost in flexibility and transmission reliability.

Specifications:

- **Data Rate:** 0 to 300 baud
- **Compatibility:** Bell 103 and 113; CCITT
- **Frequency Stability:** ±0.3 percent. Crystal controlled
- **Receiver Sensitivity:** −50 dBm ON, −53 dBm OFF
- **Modulation:** Frequency shift keyed (FSK)
- **Carrier Detect Delay:** 1.2 seconds ON; 120 msec OFF
- **EIA Terminal Interface:** Compatible with RS 232 specifications
- **Teletype Interface:** 20 milliampere current loop
- **Optional Interfaces:** IEEE 488; TTL; TTY 43
- **International (CCITT) frequencies available**
- **Switches:** Originate/Off/Answer; Full Duplex/Test/Half Duplex
- **Indicators:** Transmit Data, Receive Data, Carrier Ready, Test
- **Power:** Supplied by 24 VAC/150 MA UL/CSA listed wall-mount transformer. Input 115 VAC, 2.5 watts. (A 220 VAC, 50 Hz adaptor is available upon request.)
- **Dimensions:** 10" x 4" x 2"
- **Weight:** 1.74 lbs. (3 lbs. shipping weight including AC adaptor.)
- **Warranty:** Two years on parts and labor, excluding the AC adaptor which carries the manufacturer's warranty

Part No.	Description	List Price	SALE PRICE
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LIV-STAR20M	RS232, 20MA Current Loop	S199.00	$129.00
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LIV-IEEE	IEEE 488 Standard	$395.00	$249.00
LIV-IEEE-V21	IEEE 488, CCITT Standard	$465.00	$388.00

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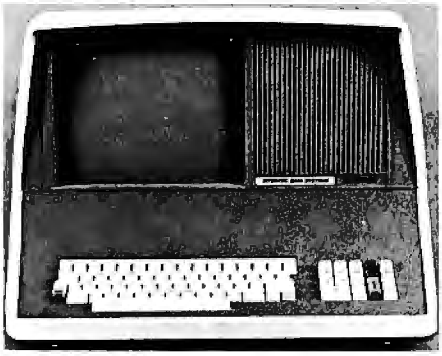

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WANTED: Need SwTPC MP-A or MP-A2 processor card or similar for S-50 bus. Prefer to have operating card, but will consider one that needs repair if necessary. (US Post Office domestic rates, $0.15 letters) George Keim, POB 160, Yap Island GU 96910.

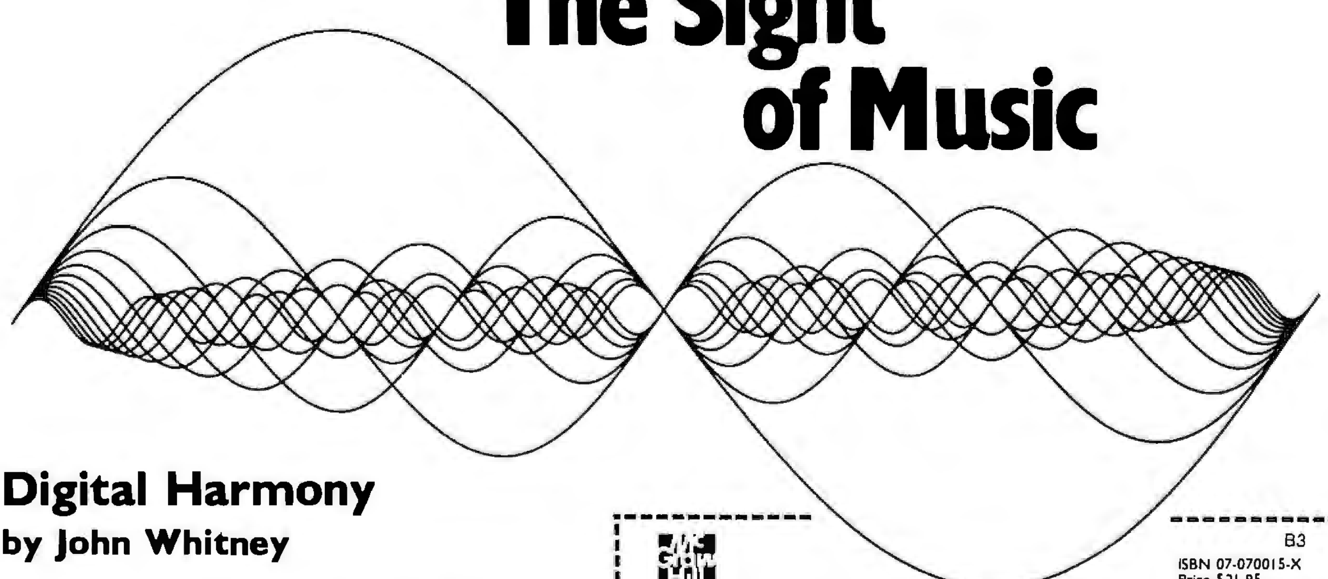
FOR SALE: Used and unused hardware and software for TRS-80 Model I and CP/M systems. Send SASE for complete list. R Lee, 25 Amaryllis Ave, Waterbury CT 06710.

FOR SALE: Two EXECuport portable terminals: 10 thru 30 cps, 80-column printer modems. Both parallel and serial I/O ports for use as printer. See ad on page 217 of the March 1980 BYTE for details. Both units in good working condition. Will ship UPS COD, no risk, pay on delivery. Model #300-$375, #320-$475. Warren V Bell, 1604 N Smith St, Spokane WA 99207, (509) 534-8088 evenings.

WANTED: Apple, Pascal, and dual disks are the base of our research project to develop automated tools for high-level software and systems design architecture. Based on the Design by Objectives methods. We seek contact with hard-working colleagues prepared to contribute to development. MARK I system exists. Tom Gilb and Lech Krzanik, Box 102, N-1411 Kolbotn, Norway.

FOR SALE: CAT-100 video digitizer with frame capture, full instructions, CP/M software, and source listing. It is a two-board system for S-100 bus and includes 32 K of programmable memory with full video and software I/O capability. It has sixteen levels of gray scale or sixteen colors arranged as 240 lines of 256 pixels. $1600 invested. $950/offer. John Underwood, 1171 NE 72nd, Portland OR 97213, (503) 252-7394.

FOR SALE: Ithaca Audio Z80 processor. 2.5 MHz with power on jump and selectable wait states, 2708 not included; $99. Vector 8803 motherboard with active termination and three S-100 connectors; $35. Roy Ortiz, 265 Beech St #21, Hackensack NJ 07601, (201) 488-5405.



FOR SALE OR TRADE: Current model Miniterm portable computer. BASIC, 6800 programming, resident debugger and editor, 32 K programmable memory, built-in microcassette (60 K storage), acoustic coupler, and serial interface. Also has all the features of a portable printing terminal. Disk system available. Other features too numerous to list. Will supply information. Sells new for $5000; will sell for $2500 or trade for 48 K Apple II with two disks and Pascal or similar system. Bob Edison, 215 Newton St, Waltham MA 02154, (617) 891-5618.

SWAP: KIM-1 microcomputer with manuals, barely used, for a pair of Acoustic Research AR-3 speakers (not AR-3a). Will pay shipping both ways. C Lee, 1021 Merritt Dr, Tallahassee FL 32301, (904) 878-1983.

FOR SALE: S-100 compatible, 16-bit 8088 single-board computer; all documents included. Never been used. Original cost of $400, will sell for $300. Trung Dac Lieu, Box 292, 303 Stadium Pl, Syracuse NY 13210.

FOR SALE: Two Pertec disk drives and controller. The drives worth $5000 when new; I will take $1500 or best offer. Both of the drives need some work. Comes complete with power supply, multiplexer boards, 8-inch DOS disk, and complete documentation. (MCI—if wanted.) Will work on various microprocessors. Heinan Landa, 12109 Greenleaf Ave, Potomac MD 20854, (301) 279-9356.

FOR SALE: Computer Mart PME1 32 K memory board, which lifts an 8 K PET to a full 40 K. 8 K of this is addressable through machine language only. The PME1 board installs entirely inside the PET. I used it lightly for three months. Cost $750; asking $350. Philip Restagno, 2910 DeWitt Pl, Bronx NY 10469, (212) 231-2753.

FOR SALE: Back issues of BYTE, postpaid. Also, want 1975 and 1976 issues of BYTE. P Gray, 1505 NW 124th Ave, Portland OR 97229, (503) 641-2747.

FOR SALE: Centronics P-1 printer, parallel, with cable; $250. SwTPC CT-64 terminal; $250. Hitachi 9-inch monitor; $75. SwTPC AC-30 tape controller; $75. All include manuals. Send 10% for COD, ppd orders sent ppd. Charles Shilling, 2003 Fair Meadow, Arlington TX 76012, (817)461-2239.

FOR TRADE: Want to swap cassette programs for TRS-80 Level II. Games, educational, and mathematics. No business programs. Send cassette with your address. Bob Trent, POB 298, Hardinsburg KY 40143.

FOR SALE: TRS-80 disk drive. Less than six hours use. Includes cable. $225. K J Morrison, 10513 Silverdale Way NW, Silverdale WA 98383.

FOR SALE OR TRADE: Assembler for 8080/85. Runs under North Star DOS V5.0. Written in BASIC, creates object file in North Star format. Included are source creator/editor and file dump programs (also in BASIC). Requires one minifloppy drive plus 32 K. Cost: $25; manual only: $5. W T Shaw, 13521 Blenheim Rd N, Phoenix MD 21131, (301) 667-4800.

USED COMPUTERS: Send information on microcomputers you or a friend have sold—make, model, configuration, month sold, price. I'll send a summary of other people's prices in return. Bruce Lynch, 2905 Blue Robin, Herndon VA 22071.

FOR SALE: ESCON Universal Interphase RS-232 for IBM Selectric II typewriter. B K Parekh, (406) 365-3393.

FOR SALE: Novation Model 4202B modem, 1200 bps, originate/auto-answer, direct connect, 2-wire dial-up or 4-wire; $496. Philip Nunn, 201 Netherfield, Comstock Park MI 49321, (616) 361-8681.

FOR SALE: Heath H-9 video terminal expertly assembled, in very good condition; $200. Also, YAESU FR-101, FL-101 with converter boards, filters, clock, and all documentation in English; $900. Mint condition. Mark Miller, 9573 Walley Ave, Philadelphia PA 19115, (215) 698-1905.

FOR SALE: Apple graphics tablet, cost $795, sell $600. Mountain Hardware 388 day clock, cost $199, sell $140. Mountain Hardware Romplus with keyboard filter, cost $169, sell $125. Above items in like new condition and were used less than three hours each. Will be shipped in original cartons with all documentation. Earl A Loobey, FSI/POB 487, Fairbanks AK 99701.

FOR SALE: Digital Group microcomputer. Z80 and 6800 processors, 50 K memory, sixteen parallel ports, front panel, 16 by 64 video display, Marantz tape deck, keyboard, Sanyo monitor, Maxi-BASIC, Super Games, Fig-FORTH documentation, plus much more software and full hardware documentation. Complete system $2000 or best offer. Dennis Ruffer, 423 Garfield St, Kalamazoo MI 49001, (616) 381-8747.

FREE PROGRAMS: As a high school science teacher using a 16 K Apple II Plus, I have had difficulty in locating programs for class use. Since commercial programs are expensive and often not suited for use with high school students, I have written several programs in Applesoft BASIC for use in my physical science, biology, and chemistry classes. If anyone is interested in obtaining a copy of one of these programs, please send me a SASE and I will send you a complimentary copy. William R Ground, J L Mann High School, 61 Isbell Ln, Greenville SC 29607.

FOR SALE: Heath H-11 system. LSI-11 with 40 K bytes memory, CRDS double-density floppies, H-10 paper-tape reader/punch, serial and parallel interfaces. $6400 value, asking $4800. Add $650 for factory-assembled H-19 terminal. Jeff Goldberg c/o CRDS, 4 Tech Cir, Natick MA 01760, (617) 655-1800.

FOR SALE: Apple II DOS 3.3 upgrade kit, including read-only memories, disks, and manual; $35. Joel Buckley, 1212 Broadway, Hanover PA 17331.

FOR SALE: Heathkit ET-3400 and program for same. Good condition. Will sell to the best offer. Ralph Swearingen, 7213 Loras Ln, Wonder Lake IL 60097, (815) 653-7821.

FOR SALE: North Star disk controller board. Single-density, excellent condition. Selling due to an upgrade on my present system. Lots of software, including North Star DOS and BASIC, CP/M, assemblers, games, and lots more. Will run Pascal, FORTRAN, ALGOL, C, and many others. Asking $250. Mark Sauerwald, 7872 Caminito Huerta, San Diego CA 92122, (714) 453-1206.

FOR SALE: North Star controller and software (fifty diskettes); $350. Eprom board, holds sixteen 2708s; $60. Rack-mountable Integrand cabinet; $120. Vector eleven-slots motherboard with connectors; $50. TDL processor; $100. TDL monitor board; $150. TDL cassette software (Assembler, 12 K BASIC, Text Editor, text output processor); $200. Mohammad Mandurah, POB 4272, Stanford CA 94305, (415) 328-3959.

WANTED: Apple II with at least 32 K memory and disk drive. Prefer dual-disk drive. All replies will be answered. Send complete name, address, and phone. Scott Emmons, 1225 Nord Ave #166, Chico CA 95926, (916) 893-5311.

WANTED: Data for Processor Technology GPM-1 board (9 K read-only memory, 1 K programmable memory). Also require for S-100 bus, a cassette I/O prom programmer and disk controller, any make. Consider anything from bare board with data, to working. Please state price required. Larry Dass, 4, Nancevallon, Brea, Camborne, Cornwall, England, phone 0209 714475.

FOR SALE: Heathkit H-14 printer ready to connect to Heathkit, Zenith, or North Star Horizon computer. Features include RS-232 interface, uppercase/lowercase, up to 132 columns wide, adjustable tractor feed to 9.5 inches wide, maximum 165 cps print speed. Unit is in perfect condition. Full documentation and original carton included; $575. Brian Stotesbery, 2544 Second Ave S, Minneapolis MN 55404, (612) 872-0804.

SWAP: TRS-80 machine language and BASIC programs, Level II and Disk BASIC. Send your list of programs to trade, and I'll send mine. Steven Kliewe, 9005 Vickery Rd, Tacoma WA 98446.

FOR SALE: Hewlett-Packard 608D VHF signal generator. Like new, $350. Also, eight computer power supplies, four chart recorders, pulse generator, square-wave generator. W L Pierce, 703 23rd St S, Arlington VA 22202, (703) 525-3223.

WANTED: Processor board for SwTPC 6800 computer. Garth Fisher, Department of Industrial Technology, Walla Walla College, College Place WA 99324.

BOMB

BYTE's Ongoing Monitor Box

Article #	Page	Article	Author(s)
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8	262	A Simple Approach to Data Smoothing	Ruckdeschel and Krinsky
9	300	The New Literacy: Programming Languages as Languages	Handel
10	317	Computer Music: A Design Tutorial	Orlofsky

Opinions and Games Win December BOMB

Computer games of all kinds caught our readers' fancy. Jerry Pournelle's popular User's Column won first place in the December 1980 BOMB; this time, Jerry wrote about "BASIC, Computer Languages, and Computer Adventures." P David Lebling's article "Zork and the Future of Computerized Fantasy Simulations" captured second. The next three places went to "Multimachine Games" (Ken Wasserman and Tim Stryker), "On the Road to Adventure" (Bob Liddil), and "Pirate's Adventure" (Scott Adams).

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BYTE'S BOMB is your direct line to the editor's desk. Each month, the two top-rated authors receive bonuses based on your votes. To cast your vote, first look at the list of this month's articles and corresponding article numbers (located in the unclassified ads section on the page preceding the Reader Service list), then rate each article as **Excellent, Good, Fair,** or **Poor** by circling the appropriate number in each column below. Your feedback helps to produce the best possible magazine each month.

Article No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Excellent	801	805	809	813	817	821	825	829	833	837	841	845	849	853	857	861	865	869	873	877
Good	802	806	810	814	818	822	826	830	834	838	842	846	850	854	858	862	866	870	874	878
Fair	803	807	811	815	819	823	827	831	835	839	843	847	851	855	859	863	867	871	875	879
Poor	804	808	812	816	820	824	828	832	836	840	844	848	852	856	860	864	868	872	876	880

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Ohio Scientific: The leader in Winchester based microcomputers.

Ohio Scientific produced the first large capacity fixed media hard disk (Winchester) based microcomputers in 1977. Since then we have shipped more of these systems than the rest of the microcomputer industry combined.

Family Features
All standard C3 features including:

- 3-processor CPU with 6502, Z80 and 6800
- .7 MIPS 6502A
- 48K static RAM
- Dual 8" floppies
- Free standing rack for direct expansion capabilities
- 17-slot OSI 48 line BUS architecture for large system expansion
- Directly accepts up to 8 users with currently available memory boards, more with higher density boards in the future
- Directly expandable for use as Network data bases
- Slide-mounted subassemblies, removable side panels and locking rear door for easy expansions and service.

C3-A
The floppy only rack based C3 for users who anticipate expansion to hard disk, multi-user and/or networking in the future. **Under $7000.**

C3-B
The world's most powerful microcomputer (when GT equipped). Features the highly advanced and extensively field proven OKIDATA 3306 Winchester disk.

Features

- System boots from floppies or hard disk on power up
- 74 megabytes end user workspace under OS-65U, 80 megabytes unformatted
- Ultra-high performance disk
  74 millisec worst case access
  38 millisec average
  10 millisec access on cylinder (215K user workspace)
  8 megabits per second transfer rate
- Simple on/off disk operation with elaborate internal protection from improper temperature, line voltage and controller failures
- Features spindle brake and designated head landing areas for much longer operational life than the newer low-cost Winchesters
- Highly advanced OS-65U operating system:
  Multiple level pass word security
  Multiple operating systems on disk
  Ultra-high speed "FIND" command for high speed string searches (Associative Access)
  Upward compatible with multi-user and network systems with full file, peripheral and communications arbitration between users
- Available factory configured for up to 8 users and network data base operation
- Expandable to CP/M operation by adding 4K (CM-2 memory) **Under $14,000**

C3-C
A medium performance Winchester disk based system which provides the ideal cost/performance ratio in typical small business applications. The C3-C uses the Shugart SA4008 29 megabyte Winchester disk.
Performance specifications, hardware configuration and software is identical to the C3-B with the following exceptions:

- 23 megabytes of end user workspace under OS-65U
- 29 megabytes unformatted capacity
- Medium performance Winchester
  240 millisec worst case access
  87 millisec average access
  10 millisec access on cylinder (110K user workspace)
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