BYTE®

the small systems journal

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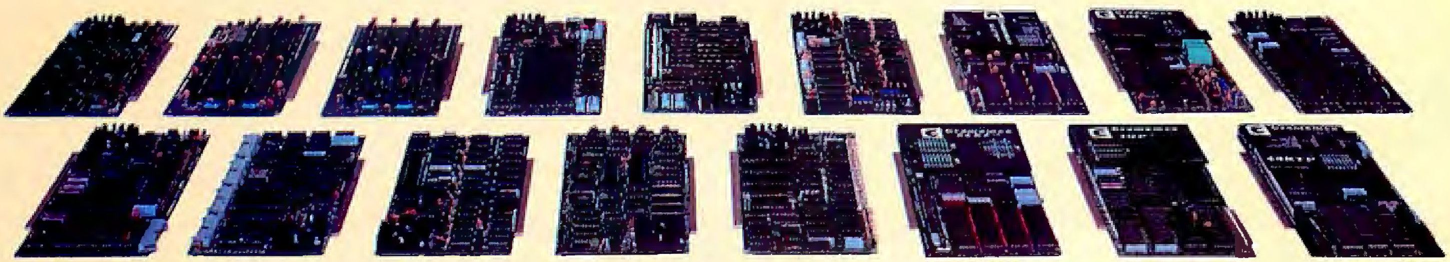
THE IBM PERSONAL COMPUTER

A new small computer that won't limit you tomorrow

New Cromemco System One shown with our high-capability terminal and printer.



Expandability

Here's a low-priced computer that won't run out of memory capacity or expandability halfway through your project.

Typically, computer usage tends to grow, requiring more capability, more memory, more storage. Without a lot of capability and expandability, your computer can be obsolete from the start.

The new System One is a real building-block machine. It has capability and expandability by the carload.

Look at these features:

- **Z80-A processor**
- **64K of RAM**
- **780K of disk storage**
- **CRT and printer interfaces**
- **Eight S-100 card slots, allowing expansion with**
  - **— color graphics**
  - **— additional memory**
  - **— additional interfaces for telecommunications, data acquisition, etc.**
- **Small size**

GENEROUS DISK STORAGE

The 780K of disk storage in the System One Model CS-1 is much greater than what is typically available in small computers. But here, too, you have a choice since a second version, Model CS-1H, has a 5" Winchester drive that gives you **5 megabytes** of disk storage.

MULTI-USER, MULTI-TASKING CAPABILITY

Believe it or not, this new computer even offers multi-user capability when used with our advanced CROMIX* operating system option. Not only does this outstanding O/S support multiple users on this computer but does so with powerful features like multiple directories, file protection and record level lock. CROMIX lets you run multiple jobs as well.

In addition to our highly-acclaimed CROMIX, there is our CDOS*. This is an enhanced CP/M† type system designed for single-user applications. CP/M and a wealth of CP/M-compatible software are also available for the new System One through third-party vendors.

COLOR GRAPHICS/WORD PROCESSING

This small computer even gives you the option of outstanding high-resolution color graphics with our Model SDI interface and two-port RAM cards.

Then there's our tremendously wide range of Cromemco software including packages for word processing, business, and much more, all usable with the new System One.

ANTI-OBSOLESCENCE/LOW-PRICED

As you can see, the new One offers you a lot of performance. It's obviously designed with anti-obsolescence in mind.

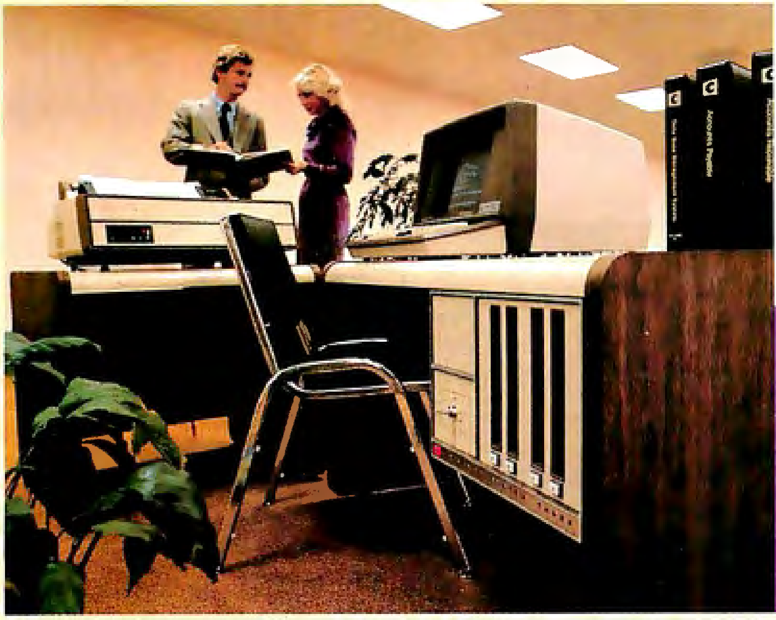
What's more, it's priced at only $3,995. That's considerably less than many machines with much less capability. And it's not that much more than many machines that have little or nothing in the way of expandability.

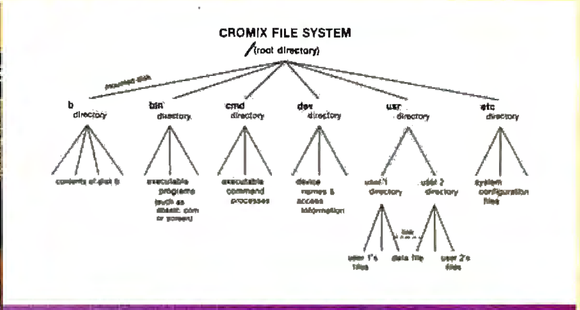
Physically, the One is small — 7" high. And it's all-metal in construction. It's only 14⅛" wide, ideal for desk top use. A rack mount option is also available.

CONTACT YOUR REP NOW

Get all the details on this important building-block computer. Get in touch with your Cromemco rep now. He'll show you how the new System One can grow with your task.

*CROMIX and CDOS are trademarks of Cromemco Inc.
†CP/M is a trademark of Digital Research





CROMIX*— Cromemco's outstanding UNIX†–like operating system

CROMIX is just the kind of major development you've come to expect from Cromemco. After all, we're already well-known for the most respected software in the microcomputer field.

And now we've come up with the industry's first UNIX-lookalike for microcomputers. It's a tried and proven operating system. It's available on both 5" and 8" diskettes for Cromemco systems with 128K or more of memory.

Here are just some of the features you get in this powerful Cromemco system:

- Multi-user and multi-tasking capability
- Hierarchical directories
- Completely compatible file, device, and interprocess I/O
- Extensive subsystem support

FILE SYSTEM

One of the important features of our CROMIX is its file system comprised of hierarchical directories. It's a tree structure of three types of files: data files, directories, and device files. File, device, and interprocess I/O are compatible among these file types (input and output may be redirected interchangeably from and to any source or destination).

The tree structure allows different directories to be maintained for different users or functions with no chance of conflict.

PROTECTED FILES

Because of the hierarchical structure of the file system, CROMIX maintains separate ownership of every file and directory. All files can thus be protected from access by other users of the system. In fact, each file is protected by **four separate access privileges** in each of the three user categories.

TREMENDOUS ADDRESS SPACE, FAST ACCESS

The flexible file system and generalized disk structure of CROMIX give a disk address space in excess of one gigabyte per volume — file size is limited only by available disk capacity.

Speed of access to disk files has also been optimized. Average access speeds far surpass any yet implemented on microcomputers.

'C' COMPILER AVAILABLE, TOO

Cromemco offers a wide range of languages that operate under CROMIX. These include a high-level command process language and extensive subsystem support such as COBOL, FORTRAN IV, RATFOR, LISP, and 32K and 16K BASICs.

There is even our highly-acclaimed 'C' compiler which allows a programmer fingertip access to CROMIX system calls.

THE STANDARD O-S FOR THE FUTURE

The power and breadth of its features make CROMIX the standard for the next generation of microcomputer operating systems.

And yet it is available for a surprisingly low $595.

The thing to do is to get all this capability working for you now. Get in touch with your Cromemco rep today.

*CROMIX is a trademark of Cromemco, Inc.
†UNIX is a trademark of Bell Telephone Laboratories

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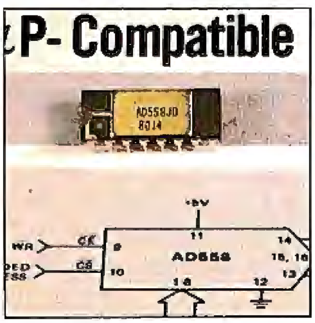

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In This Issue

IBM's entry into the small-computer market with its Personal Computer was a big event in the industry. And that's why we've taken a second look. Showcased in our cover photo by Paul Avis, the IBM Personal Computer is a versatile machine. For an in-depth report on its many features and capabilities read Gregg Williams' article, "A Closer Look at the IBM Personal Computer."

Hardware is our theme this month and among the many articles on that topic are Bill Barden's second in a series, "Build a Joystick A-to-D Converter for the TRS-80 Model I or III," and Kenneth Piggott's "Troubleshooting with Electronic Signatures." As well, learn how to expand your ZX-80's memory, control motors and appliances, and interrupt your Elf. All this plus our regular features and reviews.

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MicroAngelo™
and
beyond.

Editorial

Of IBM, Operating Systems, and Rosetta Stones

by Chris Morgan, Editor in Chief

The story behind the creation of the IBM Personal Computer is as interesting as the machine itself. In this issue Gregg Williams discusses in great detail IBM's most recent offering to the microcomputer field (see "A Closer Look at the IBM Personal Computer," page 36). In this editorial I'll tell you the story of its development, talk about the machine's operating system, and discuss the possibility of establishing a standard for operating systems.

Breaking the Speed Barrier

As IBM watchers know, it usually takes about five years from the time a project at IBM is conceived to the first shipments of the completed product. This is typical for complex computer projects at large companies. Amazingly, the total time for the IBM Personal Computer project was about 13 months. How did this happen?

One answer is that IBM limited the number of in-house innovations. Instead it used existing hardware and software components from outside vendors—a departure for the normally vertically integrated giant. Imagine how bizarre an Intel-manufactured processor would have seemed in an IBM product of, say, five years ago.

Another factor in IBM's speed is that the company gave its design team a wide latitude and a great deal of autonomy. The rest of the company left the designers, based in Boca Raton, Florida, alone to do their job, although IBM's quality-assurance group did keep a close eye on the software chosen for the machine.

One of the most interesting aspects of the Personal Computer is that its design team included many computer hobbyists and "hackers"—people who owned and were familiar with existing microcomputers. And the IBM machine reflects their experience. I'm glad they avoided many design mistakes of the past. The keyboard alone is one of the best I've seen, though I wish the shift keys were more conventionally positioned. (Oh well.)

Operating Systems

IBM has decided to let the marketplace determine which of its three operating systems will become dominant (if any). Thus, you can get UCSD Pascal, CP/M-86, or the IBM Personal Computer operating system from Microsoft. You can have all three if you want; it's a nice choice.

I'm particularly excited about Microsoft's approach to the IBM Personal Computer. As you may know, Microsoft recently introduced Xenix, its superset of Unix, Western Electric's popular multiuser operating system for small- and medium-sized computers. It turns out that Xenix is at the top of a pyramid of upward-compatible operating systems to be made available by

TRS-80* COMPUTING EDITION

©1981 Percom Data Co., Inc. The Percom Peripheral 35 cents

Percom's DOUBLER II™ tolerates wide variations in media, drives

GARLAND, TEXAS — May 22, 1981 — Harold Mauch, president of Percom Data Company, announced here today that an improved version of the Company's innovative DOUBLER™ adapter, a double-density plug-in module for TRS-80* Model I computers, is now available.

Reflecting design refinements based on both theoretical analyses and field testing, the DOUBLER II™, so named, permits even greater tolerance in variations among media and drives than the previous design.

Like the original DOUBLER, the DOUBLER II plugs into the drive controller IC socket of a TRS-80 Model I Expansion Interface and permits a user to run either single- or double-density diskettes on a Model I.

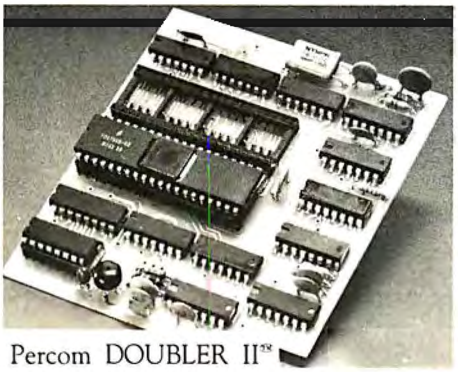
With a DOUBLER II installed, over four times more formatted data — as much as 364 Kbytes — can be stored on one side of a five-inch diskette than can be stored using a standard Tandy Model I drive system.

Moreover, a DOUBLER II equips a Model I with the hardware required to run Model III diskettes.

(*Ed. Note*: See "OS-80™: Bridging the TRS-80* software compatibility gap" elsewhere on this page.)

The critical clock-data separation circuitry of the DOUBLER II is a proprietary design *called a ROM-programmed digital phase-lock loop data separator.*

According to Mauch, this design is more tolerant of differences from diskette to diskette and drive to drive, and also provides *immunity to performance degradation caused by circuit component aging.*



Percom DOUBLER II™

Mauch said "A DOUBLER II will operate just as reliably two years after it is installed as it will two days after installation."

The digital phase-lock loop also *eliminates the need for trimmer adjustments typical of analog phase-lock loop circuits.*

"You plug in a Percom DOUBLER II and then forget it," he said.

The DOUBLER II also features a refined Write Precompensation circuit that more effectively minimizes the phenomena of bit- and peak-shifting, a reliability-impairing characteristic of magnetic data recording.

The DOUBLER II, which is fully software compatible with the previous DOUBLER, is supplied with DBLDOS™, a TRSDOS*-compatible disk operating system.

The DOUBLER II sells for $2[illegible]95, including the DBLDOS diskette. Now $169.95!

Owners of original DOUBLERs may purchase a DOUBLER II upgrade kit, without the disk controller IC, for $30.00. Proof of purchase of an original DOUBLER is required, and each DOUBLER owner may purchase only one DOUBLER II at the $30.00 price.

The Percom DOUBLER II is available from authorized Percom retailers, or may be ordered direct from the factory. The factory toll-free order number is 1-800-527-1222.

Ed. note: Opening the TRS-80 Expansion Interface may void the Tandy limited 90-day warranty. Circle 300 on inquiry card.

Circuit misapplication causes diskette read, format problems.

High resolution key to reliable data separation

GARLAND, TEXAS — The Percom SEPARATOR™ does very well for the Radio Shack TRS-80* Model I computer what the Tandy disk controller does poorly at best: *reliably* separates clock and data signals during disk-read operations.

Unreliable data-clock separation causes format verification failures and repeated read retries.

CRC ERROR-TRACK LOCKED OUT

The problem is most severe on high-number (high-density) inner file tracks.

As reported earlier, the clock-data separation problem was traced by Percom to misapplication of the internal separator of the 1771 drive controller IC used in the Model I.

The Percom Separator substitutes a *high-resolution* digital data separator circuit, one which operates at 16 megahertz, for the low-resolution one-megahertz circuit of the Tandy design.

Separator circuits that operate at lower frequencies — for example, two- or four-megahertz — were found by Percom to provide only marginally improved performance over the original Tandy circuit.

The Percom solution is a simple adapter that plugs into the drive controller of the Expansion Interface (EI).

Not a kit — some vendors supply an untested separator kit of resistors, ICs and other paraphernalia that may be installed by modifying the computer — the Percom SEPARATOR is a fully assembled, fully tested plug-in module.

Installation involves merely plugging the SEPARATOR into the Model I EI disk controller chip socket, and plugging the controller chip into a socket on the SEPARATOR.

The SEPARATOR, which sells for only $29.95, may be purchased from authorized Percom retailers or ordered directly from the factory. The factory toll-free order number is 1-800-527-1222.

Ed. note: Opening the TRS-80 Expansion Interface may void the Tandy limited 90-day warranty. Circle 299 on inquiry card.

All that glitters is not gold

OS-80™ Bridging the TRS-80* software compatibility gap

Compatibility between TRS-80* Model I diskettes and the new Model III is about as genuine as a gold-plated lead Krugerrand.

True, Model I TRSDOS* diskettes can be *read* on a Model III. But first they must be converted and re-recorded for Model III operation.

And you *cannot write* to a Model I TRSDOS* diskette. Not with a Model III. You cannot add a file. Delete a file. Or in any way modify a Model I TRSDOS diskette with a Model III computer.

Furthermore, your converted TRSDOS diskettes cannot be converted *back* for Model I operation.

TRSDOS is a one-way street. And there's no retreating. A point to consider before switching the company's payroll to your new Model III.

Real software compatibility should allow the *direct, immediate* interchangeability of Model I and Model III diskettes. No read-only limitations, no conversion/re-recording steps and no chance to be left high and dry with Model III diskettes that can't be run on a Model I.

What's the answer? The answer is Percom's OS-80™ family of TRS-80 disk operating systems.

OS-80 programs allow *direct, immediate* interchangeability of Model I and Model III diskettes.

You can run Model I single-density diskettes on a Model III; install Percom's plug-in DOUBLER™ adapter in your Model I, and you can run double-density Model III diskettes on a Model I.

There's no conversion, no re-recording.

Slip an OS-80 diskette out of your Model I and insert it directly in a Model III.

And vice-versa.

Just have the correct OS-80 disk operating system — OS-80, OS-80D or OS-80/III — in each computer.

Moreover, with OS-80 systems, you can add, delete, and update files. You can read *and write* diskettes regardless of the system of origin.

OS-80 is the original Percom TRS-80 DOS for BASIC programmers.

Even OS-80 utilities are written in BASIC.

OS-80 is the Percom system about which a user wrote, in Creative Computing magazine, ". . . the best $30.00 you will ever spend."†

Requiring only seven Kbytes of memory, OS-80 disk operating systems reside completely in RAM. There's no need to dedicate a drive exclusively for a system diskette.

And, unlike TRSDOS, you *can* work at the track sector level, defining and controlling data formats — in BASIC — to create simple or complex data structures that execute more quickly than TRSDOS files.

The Percom OS-80 DOS supports single-density operation of the Model I computer — price is $29.95; the OS-80D supports double-density operation of Model I computers equipped with a DOUBLER or DOUBLER II; and, OS-80/III — for the Model III of course — supports both single- and double-density operation. OS-80D and OS-80/III each sell for $49.95. Circle 301 on inquiry card.

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Microsoft. At the bottom is the IBM DOS (called MSDOS by Microsoft). In the middle will be XEDOS, a new operating system written in the C language for the 68000, Z-8000, 8086, and LSI-11 processors. XEDOS will contain Xenix-like features and will be essentially a single-user version of Xenix.

XEDOS and Xenix are processor-independent. Because the different versions of XEDOS are written in C with a minimal amount of native assembly-language code, programs written for one 16-bit processor can be readily transferred to another. Microsoft demonstrated this capability, at the recent COMDEX show in Las Vegas, by exchanging unmodified code between four machines: a 68000, a Z-8000, an 8086, and a PDP-11.

Standards, Anyone?

Unix has become well entrenched in the nation's colleges and universities due to Western Electric's extensive, inexpensive licensing of the system. As a result, many of today's graduating computer scientists are familiar with it. (See "The Unix Operating System and the Xenix Standard Operating Environment" by Robert Greenberg, June 1981 BYTE, page 248.)

Microsoft's proposed family of operating systems will also incorporate a significant feature—a graphics device driver that uses AT&T's proposed videotex graphics standard called PLP (Presentation Level Protocol). It's a minimal standard, admittedly (it's hardly high-resolution graphics), but think what it would mean if *all* 16-bit operating systems could support PLP. At last we'd have a *least common denominator* for graphics. And keep in mind that the creative use of graphics will be a vital part of the future of our field.

Digital Research, for its part, is promoting its latest efforts, CP/M-86 and its multiuser, multitasking version, MP/M-86, as candidates for the standard 16-bit operating systems of the future. (See "CP/M: A Family of 8- and 16-Bit Operating Systems," by Gary Kildall in June 1981 BYTE, page 216.) More than twenty OEMs (original equipment manufacturers) have made commitments to use the two operating systems. Both the IBM Personal Computer and the IBM Displaywriter use CP/M-86. MP/M-86 will soon be available for the IBM Personal Computer. One good feature of MP/M-86 is its foreground/background structure, which, for example, lets the user access the editor while compiling a program.

Of more importance than CP/M-86 is MP/M-2, Digital Research's new multiuser operating system. It will be a real contender against Microsoft's operating system. It includes file locking and record locking, 32-megabyte file capacity, and other sophisticated features. Significantly, the company also currently supports Unix through C BASIC and Pascal. Digital's official stand is that it is not "philosophically opposed" to the Unix concept, thus holding open the possibility for a future operating system standard.

The ultimate single user machine

The PDS-80™ with Cache BIOS™ is a professional system designed for the most rigorous single user CP/M* environments ... in business, software development, scientific, educational and industrial research ... where speed and program space are critical factors.

SymBIOSis quadruples speed

No matter what high-level language you use ... Cobol, Basic, Fortran, PL/1, or Pascal ... PDS-80 offers more speed, power and reliability than any other floppy based CP/M system currently on the market. The InterSystems Cache BIOS fully exploits the advanced DMA and interrupt features of our reliable Series II hardware to buffer whole tracks in extended memory so most operations run two to four times faster than on other floppy based systems ... actually equals the speed of many small hard disk systems. And Cache BIOS also provides many sophisticated system test and protection features to assure reliable operation.

An advanced CP/M application system

PDS-80 has all you need for commercial systems integration and applications software development ... including a choice of the industry's only integral 8 bit front panel. Best of all, PDS-80 allows the systems integrator or applications developer addressing a vertical market to develop on the same components he configures for resale. The highly expandable modular design with 20 slot S-100 mainframe allows almost unlimited options to suit any end use environment ... including a choice of tabletop or rackmount design.

InterSystems will work with you at whatever level is appropriate to configure the target system you need ... right up to fully assembled and tested systems with floppy and Winchester disk drives.

Full software support

In addition to InterSystems' Cache BIOS and the CP/M operating system, models of PDS-80 can include Pascal/Z,

our highly acclaimed Z-80® native code Pascal compiler, and InterPak 80™, a special set of utilities including a powerful screen editor and versatile spelling editor to assist in the rapid editing, proofing and documentation of your code. These powerful programming aids are also available as standalone products.

It's upgradeable!

Both hardware and software are designed to provide for upgrade to 16 bit operation. Programs written for Pascal/Z are fully compatible with I•Pas 8000™, our Z-8000® native code compiler, and all PDS-80 systems are upgradeable to our 16 bit multi-user DPS-8000.

We build micros for bigger ideas.

Your big ideas. We're dedicated to providing the computer professional ... Systems Integrators, commercial program developers, scientific and industrial programmers ... with professional hardware and software tools. And we support our customers to the fullest, with complete, professional documentation, application engineering consultation, and prompt, responsive service both from the factory and through factory-authorized service centers.

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for complete information on any of our 8 or 16 bit systems and software products.

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Editorial

The Battle

Who's going to win the 16-bit operating system sweepstakes? My guess is that there'll be no clear winner for several years; maybe never. Competing software and languages tend to coexist in our field, and this situation is no exception. IBM has set the tone by making *both* CP/M-86 and MSDOS available for its machine. Yet when I look at the mistakes made in the 8-bit world, I hope a standard will emerge.

A New "Rosetta Stone"

In 1799 the Rosetta stone was discovered in Egypt. It contained the same message inscribed in three different languages: Greek, Demotic, and Egyptian hieroglyphics. Using the familiar texts of the Greek and Demotic, scientists were able to painstakingly translate Egyptian hieroglyphics for the first time—a triumph of scholarship that would have been virtually impossible without the decoding stone.

But translating is a slow, arduous job. Creative software designers waste a lot of time customizing their programs for different machines. Today, we need an entire set of "Rosetta stones," translating tools to disseminate software for all of the popular machines. But these tools have become more like a set of millstones around our necks.

We need a new approach to operating systems to cure the ills that still beset us from the footloose days of 8-bit machines. A standard 16-bit operating system is still the best way out of the linguistic woods. ■

Articles Policy

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Articles which are accepted are purchased with a rate of up to $50 per magazine page, based on technical quality and suitability for BYTE's readership. Each month, the authors of the two leading articles in the reader poll (BYTE's Ongoing Monitor Box or "BOMB") are presented with bonus checks of $100 and $50. Unsolicited materials should be accompanied by full name and address, as well as return postage.

S-100 Fast-Aid.

Including 3 new boards for system design relief.

The MB64.

An economical, high-performance 64K static RAM memory.

Just what the doctor ordered. A new 64K static RAM configured as two 32K blocks that's fast (in excess of 6MHz), reliable and economical. The MB64 supports IEEE 696/S-100 24-bit extended addressing for up to 16MB of RAM. Bank switching permits compatibility with popular multi-user computer systems (such as CROMIX*). Up to 8K can be replaced with 2716 EPROMs. The MB64 offers low power consumption (typically less than 600 milliamps). And a provision for optional battery backup.

(The MB64 is priced at less than $850.)

*CROMIX is a trademark of Cromemco, Inc.

The IO8.

An I/O board featuring eight serial interfaces, individually programmable baud rates, and an interrupt clock.

Give your system fast-aid—including easier testing and speedier diagnosis—with SSM's new IO8. This board features eight asynchronous serial RS-232 I/O ports with LED data transfer indicators. Individually programmable I/O port baud rates (110-19,200) meet all your specific configuration requirements. A timer (50/60 Hz) supports real-time or multi-user applications.

And all our Fast-Aid boards offer:

- Card ejectors for painless card removal.
- LEDs for easy troubleshooting and monitoring.
- IEEE 696/S-100 compatibility.

The IO5.

A two-serial/three-parallel I/O board with programmable timer.

The perfect remedy for fast system integration, more precise diagnosis, and far healthier system operation. The IO5 features two RS-232 asynchronous serial interfaces for maximum peripheral compatibility. The board supports a variety of devices with high-speed serial data transmission (110-19,200 baud). Three parallel ports, providing a total of 32 bits, support various I/O configurations: a 16-bit software programmable bi-directional interface, and two 8-bit interfaces. One 8-bit interface supports direct connection to Centronics-compatible printers. The other provides 8 bits of parallel input for such devices as keyboards. The IO5 also offers a software-programmable timer for real-time or multi-user applications.

For more details about these new boards, or any of SSM's S-100 compatible boards (including various CPU, EPROM, video and development boards), just call your local dealer or SSM today.

SSM

SSM Microcomputer Products, Inc.
2190 Paragon Drive
San Jose, CA 95131
(408) 946-7400 Telex: 171171
TWX: 910-338-2077

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When You Have To Face A Deadline...

Since its introduction, Pascal/MT+® has been used to produce thousands of professional solutions to industrial, business and systems level application problems. In addition to implementing the complete ISO STANDARD, Pascal/MT+® contains a host of powerful features and facilities which make program construction a snap!

Pascal/MT+® is a total programming system including our native machine code compiler, linker, Pascal-level debugger, disassembler, run-time subroutine library and the exclusive SpeedProgramming™ Package.

With the advent of 16-bit machines and increasing customers demands, you can no longer afford to write programs in anything but a professionally constructed and professionally supported package like Pascal/MT+®. MT MicroSYSTEMS has demonstrated its commitment to keeping your programs and programmers productive with our recent introduction of Pascal/MT+86 and Pascal/MT+68K for the 8086 and 68000. While Pascal/MT+® provides the capability to write non-portable programs when the need arises, true portability between radically different machines is a reality while still translating into efficient, optimized native machine code.

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Letters

Park Your Benchmark Here

Jim Gilbreath's article "A High-Level Language Benchmark" was very useful. (See the September 1981 BYTE, page 180.) The comparisons between different languages and microprocessors are particularly relevant, since we are considering getting several microcomputers for word-processing and control tasks here at the Arecibo Observatory.

Peter M. B. Shames, Head
Computer Department
Arecibo Observatory
POB 995
Arecibo, Puerto Rico 00612

My thanks to Jim Gilbreath for "A High-Level Language Benchmark." It was far and away the most immediately valuable article I have seen in BYTE.

I was, however, disappointed by the numerous "omissions" in Mr. Gilbreath's tables. For example, how long was the program in 68000 assembly language? In 8086 assembly language? I would dearly like to know how those machines compare to each other (and to the 8-bit machines) in code-storage efficiency.

I do most of my programming in FORTH, so I wanted to compare that language to others in the article. I was disappointed to find that Mr. Gilbreath left blanks in the "compiled bytes," "total size," and "compile and load [time]" columns for FORTH. (See table 2, page 192.) When I tried to collect the missing figures, I found that the FORTH benchmark in the article would not compile. (See listing 9, page 190.) The word PRIME, used in the seventh line of the definition of DO-PRIME, should have been FLAGS. PRIME is not defined in the program.

I hope that readers who can augment the information in Mr. Gilbreath's article will share their knowledge. We badly need more information of this sort.

Jonathan Sachs
6713 Richmond Ave.
Richmond, CA 94805

I read Jim Gilbreath's article with interest. I realize that the purpose of a benchmark program is not efficiency in any one particular language or machine, but to compare the execution times of many languages or machines. But some languages are more efficient than others at particular aspects of data processing, such as data access, I/O (input/output), etc. One of these aspects is looping. APL, for instance, is designed to handle arrays of any dimension with ease, but program loops are, in fact, not its forte. If I understand Mr. Gilbreath's benchmark program correctly, by the time it has looped 63 times (I=62, producing 127, the largest odd integer less than the square root of the highest number to be searched), all nonprime numbers in the list have been flagged and the remaining loops will find no new nonprime numbers. Eliminating the extra looping causes the BASIC program to require about half the execution time. I don't know about the other languages.

The extra loops seem to penalize those languages that do not loop well but may have some efficient alternate method of addressing vector or array elements (rather than addressing each element by the use of a loop). It may well be that this objection does not apply to any of the 10 languages tried in this article, in which case my point is moot. But as Mr. Gilbreath points out, an efficient algorithm is the best way to speed up a program.

Thank you, Jim Gilbreath, for the useful compilation of execution times as a function of language and machine.

Dwight Divine III
2735 Gelid Court
Anaheim, CA 92806

I found a few errors in Jim Gilbreath's article and programs. Zero and 1 are not prime numbers. Prime numbers are defined on the set of natural numbers, otherwise known as counting numbers, which consists of positive integers. Thus, 0 cannot be a prime number any more than can −7, 1.3, or pi. The idea that 1 is a prime number arises from the common (inaccurate) definition of a prime number as "a number divisible only by itself and 1." The actual definition is "a natural number which has two and only two distinct divisors." Thus, 1 cannot be a prime number, as it has only one distinct divisor, 1.

In reading the program listings, I noticed the statement PRIME=I+I+3 in various forms. It seemed somehow wrong to me, and I felt that PRIME=I+I+1 would be right. On analyzing the algorithm, I discovered that the former arises from the use of 0 as the first subscript and that PRIME=2*(I+1)+1 is the primitive form, which converts to the one Gilbreath used.

James C. Fairfield
4414 East Addington Dr.
Anaheim, CA 92807

Congratulations are due Jim Gilbreath for his fine article. His comparisons were very informative due to the wide range of hardware and software covered. He noticed the same thing that I have discovered: PL/I generates very efficient code! I disassembled CP/M version 2.2 (written in PL/I) so that I could interface a digital-tape system as the primary storage device. I needed to know how the disk allocation was accomplished. More or less as a "labor of love," I went through the disassembled code with an editor, adding meaningful labels and comments. The resulting code is very readable and understandable thanks to the excellent code generated by the PL/I compiler. The subroutines look as if an assembly-language programmer wrote them: no wasted instructions anywhere.

Clark A. Calkins
2564 Walnut Blvd. #106
Walnut Creek, CA 94598

The comparing of apples and oranges is a job sorely in need of doing. And Jim Gilbreath has done a fine piece of work, part of its merit being the arguments it will generate. I'm sure the COBOL folks are not happy. Nor are we BASIC people, although we could salve our wounds with the excuse that interpreters have to be slow.

The dogma of true BASIC people is that structure is in the mind. Let those who want structured languages have them. But treat us fairly. Since our language isn't supposed to be structured, don't force us to use little-bitty short lines like Jim's listing 7 because we know it takes our interpreter time to hop down lines. And we have different kinds of variables just like the big boys, so let us use integers too. And we suspect that most compilers don't include similar checking, so let us use NEXT without the index. Note that these aren't tricks or innovations. What some might call tricky, but certainly not innovative at this date, is the use of FOR . . . NEXT loops in preference to GOTOs.

The moral: we agree strongly with Jim

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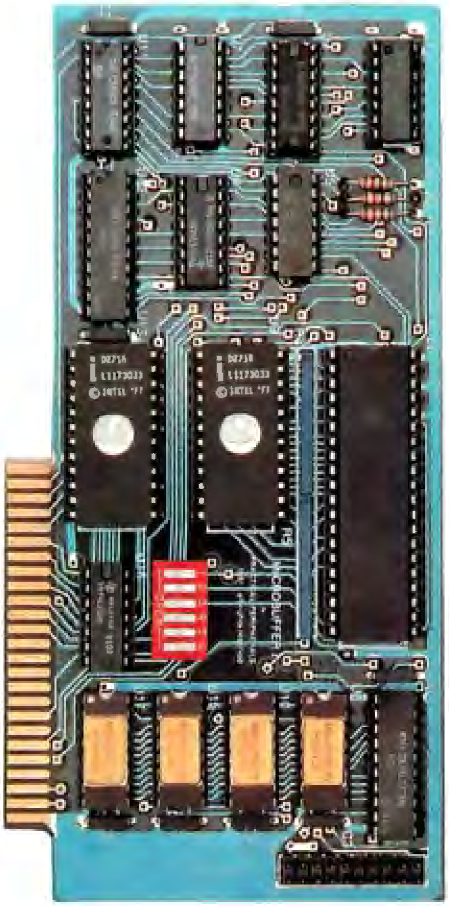

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Gilbreath on the necessity of choosing the best algorithm for the job. To that we add, know your language and use its power. There is no language that will turn bad writing into good writing.

James D. Childress
5108 Springlake Way
Baltimore, MD 21212

Jim Gilreath Replies

The response to my article has been very gratifying, and I have received so many letters that it is beyond my ability to respond to them individually. All are appreciated, especially those that pointed out errors and supplied data for machines and languages I did not have the opportunity to time. All contributed data will be reported in a subsequent article.

I regret the error in the FORTH program. It was caused by me, not BYTE, and occurred in transcribing the program from paper to a file. The word PRIME should be changed to FLAGS. Thanks to Dick Miller and Jonathan Sachs for finding this.

This was not a commissioned assignment, it was simply a computer hobbyist's report of his experiences and data collected in a project for presentation at the local computer club. The intent was to report, not to review. The data were collected over a nine-month period whenever an opportunity presented itself.

Much of the data was obtained in computer stores and computer-conference environments with limited time, so there are gaps in the tabular data for program sizes when that data were not readily obtained without detailed knowledge of the operating system. There was little time to dig deeply into nuances. It was never intended to be a Consumer's Union quality project. Think what that would cost! Hundreds of hours were spent just doing what I did.

It is not surprising that the programs listed required a bit of customization before running on some systems. There were several slightly differing versions of the program in all of the languages, but only one was printed for each case to save space.

The FORTRAN program used 0 as the first-element array subscript for consistency and because this is allowed in some (but not all) compilers. In retrospect, this was a poor choice because it violates fundamental FORTRAN-language definitions.

The BASIC program only does one iteration, which helps you avoid staying up all night (this axiom was removed from my article by the BYTE editor). Thus, these times have been multiplied by 10 for comparison with the others.

On the PET, the array would not fit, so the program was run on a smaller array, and the results were extrapolated linearly (this works—try it). The same was done for Microsoft COBOL and FORTH.

Mr. Divine's insightful observation that the algorithm has flagged all nonprime numbers after looping only 63 times nicely reinforces my contention that a better method is often more fruitful than changing languages.

It seems that my lack of COBOL expertise was quite obvious, and thanks are due to James Fairfield and others who supplied improved programs that run much faster.

It is worth reiterating that a simple benchmark such as mine is but one point on a long curve and many more specifics should be considered carefully in selecting a language or computer.

Open Letter to Potential SuperBrain Buyers

Our company recently purchased four Intertec SuperBrain QD computers from a local mail-order firm, whose advertisement stated that "all equipment is in factory cartons with the manufacturer's warranty." After one of the units failed, we discovered that the warranty had lapsed while the computers were still in the dealer's stock and we would have to pay Intertec nearly $400 to repair the unit.

Intertec's policy is that the warranty period begins when it ships the unit to the dealer. This policy is contrary to industry standards and discourages dealer stocking. A letter to Intertec regarding the above evoked this response from Andrea K. Welch, Intertec's Marketing Support Manager: "I do sincerely regret the misunderstanding that appears to exist between your organization and the company from which you purchased this equipment. I can assure you that all of our dealers are intimately familiar with our warranty policy." The dealer's response was that he was totally unaware of Intertec's policy and that it was our problem to work out with Intertec.

Any SuperBrain buyer should be sure that he or she is going to receive an adequate warranty from the dealer after receipt of the computer. After our computer failed, we were informed by the dealer that he has had problems with SuperBrains being "dead on arrival." We could have received units that were inoperable when the cartons were first opened and we would have had to pay repair charges.

James E. Ford
Paoluccio Willis Nau Associates
Civil Mechanical Electrical Engineers
7175 Construction Court
San Diego, CA 92121

Interetec Data Systems Replies

Since the initial production of the SuperBrain in 1979, Intertec has enjoyed an enviable position as the microcomputer industry's price/performance leader. Because of our commitment to total vertical integration, Intertec manufactures a product of exceptional quality at an extremely competitive price.

In keeping with this commitment to quality and leadership, Intertec offers an impressive 120-day warranty on its products. This warranty covers all parts and components deemed to be originally defective by Intertec Data Systems Corporation. We at Intertec feel that this four-month warranty offers our customers excellent coverage and that it is in keeping with our marketing endeavors. In addition, our Customer Services Department is fully staffed to insure our customers of fast, efficient service.

Like Ms. Welch, Intertec's Marketing Support Manager, I, too, regret that Mr. Ford and the company from which he purchased his SuperBrain appear to have had a misunderstanding with regard to our warranty and assure BYTE readers that all of our dealers are well informed as to its specifics. Our warranty is clearly and carefully explained in Section Six of our Master Agreement and is reiterated in virtually every manual and document issued by Intertec. It is unlikely that our dealer was "totally unaware of [our] policy."

We at Intertec are very proud of our Customer Services Department and our warranty. Intertec has carved its place in the microcomputer industry by offering our dealers products and services that we feel are better than the industry standards.

Karen K. Hubbard, Manager
Public Relations
Intertec Data Systems Corporation
2300 Broad River Rd.
Columbia, SC 29210

Fallout from BYTE's BOMB

Editor's Note: *Since the beginning of 1981, BYTE has gone through some substantial changes, both in format and size. Here are some comments about BYTE that we have received from our readers on the monthly BOMB cards (for an explanation of the cards, see the back of this issue):*

- This issue almost gave me a hernia. I love reading all the ads.
- At first I was only interested in the ads, but then I accidentally read an article!
- I enjoyed reading all the articles (fast reader), but why so many ads?
- I can't read all those ads.
- I don't read any of the articles.
- It's too big to read!
- More, more, more!
- Thank you for always making BYTE interesting, stimulating, and pregnant.

Many of our readers had comments on some of BYTE's particular features:

• I like the Programming Quickies. I seem to find your Nucleus section more useful than the feature articles (the long ones take too much time to read).
• Wow! Computing e to 116,000 places! [That's] a really worthwhile endeavor.
• I find the comparative software reviews to be of great help.
• Forget about the numbers and the philosophical articles; get back to the guts of personal computing: homebrew hardware!
• I very much liked the Color Computer article. What about software for it?
• The article on Extended Color BASIC for the Color Computer was fantastic.
• The Color Computer is sadly deficient in software. Manufacturers should apologize for saddling users with BASIC as the only available language; a giant step backwards.
• Most articles too technical.
• I enjoyed Ciarcia's articles on constructing speech synthesizers.
• Great, now they talk back!
• It did my heart good to see Steve [Ciarcia] do something I can use on my Apple II directly, without translating it from TRS-80.
• I'm going to love building my super-simple floppy-disk interface.
• As usual, BYTE has too many do-it-yourself tinkerer's projects. Can't you get more out of Pournelle?
• Gregg Williams has really hit the bull's-eye with BYTE's Arcade; please make it a monthly feature.
• My kids rush to read BYTE's Arcade each month and are very disappointed if it's not there.
• I hate to see all those pages wasted. Please review nothing but games from now on.
• I do not wish to judge your writers.

While others only made suggestions:

• Articles #6 and #7 seemed to disagree. There should never be any question as to the true static [sic] of things.
• I do wish you could pick articles that are more appealing to us, but it's probably not your fault.
• With the new 16-bit processors now available, perhaps BYTE should change its name to CHOMP.
• Why don't you make the Reader Service Card computer readable?

The requests for future articles would fill volumes. Let's have more . . .

• construction articles
• software reviews
• hardware reviews
• Programming Quickies
• on the TRS-80 Model (I, II, III, Color Computer)
• on the Apple (II, III, IV, V)
• on Heath/Zenith systems
• on the Sinclair systems
• on the Compucolor II
• on the Osborne I
• on the new (CP/M, Unix, Xenix, Zeus, Unica) operating systems
• C programs
• Pascal programs
• machine-language programs
• FORTH programs
• robotics articles
• music articles
• printer tests

There were even an amazing few who predicted articles that we had planned before they were published:

• An in-depth series on the Atari is about due. ("The Atari Tutorial, Part 1" appears

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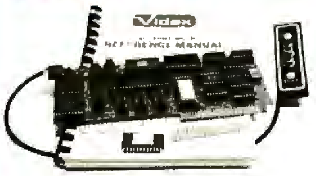

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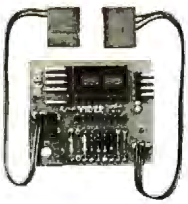
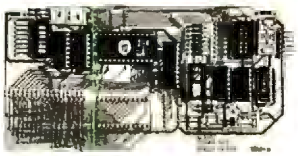


The Soft Video Switch is an automatic version of the popular Switchplate. It knows whether it should display 40 or 80 columns or Apple graphics. It does the tedious work of switching video-out signals so you don't have to. The Soft Video Switch can be controlled by software. Any Videoterm with Firmware 2.0 or greater may be used with the Soft Video Switch. The single wire shift mod is also supported. Package price is $35.00.

■ KEYBOARD AND DISPLAY ENHANCER



The original Keyboard and Display Enhancer is still available for Revision 0-6 Apples (on which the new Enhancer][will not fit). These Apples have memory select sockets at chip locations D1, E1 & F1. The Keyboard and Display Enhancer allows entry and display of upper & lower case letters with fully functional shift keys. It does NOT have user definable keys nor a type ahead buffer. The price is $129.00.

■ ACCESSORIES:

Videoterm Utilities Disc (includes) $37.00

- Font Editor
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- Applesoft Read Screen Utility
- Top & Bottom Scrolling
- Pascal Vidpatch
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Character Set EPROMs $29.00ea

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- Inverse
- German
- Katakana (Japanese)
- Line Drawing Graphics (Expanded)
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- French
- Math & Greek Symbols
- Super & Subscript

Dvorak EPROM (Enhancer) $29.00

Lower Case Chip $29.00

Circle 375 on inquiry card.

in the September 1981 BYTE, page 284.)
• What we really need is a comparison of the languages available on microcomputers. ("A High-Level Language Benchmark" appears in the September 1981 BYTE, page 180.)
• Doesn't anyone realize the problems small business has with software? ("Bridging the 10-Percent Gap" appears in the October 1981 BYTE, page 264.)
• When are you going to tackle database systems? ("Database Management Systems" is the theme of the November 1981 BYTE.)

Thank you all for writing; we scrutinize every word.

A New Small-Computer Company: IBM

As an owner of a two-year old Apple II computer system, I read with great interest Phil Lemmons' first impressions of IBM's new Personal Computer. (See "The IBM Personal Computer: First Impressions," October 1981 BYTE, page 26.) What surprised me is that Mr. Lemmons said little about documentation for the system. Is this because it doesn't yet exist? If it does not, it certainly would not be the first time a personal computer was put up for sale with meager documentation. The documentation for the Apple II was also meager at the beginning, but then that was a very different stage in the history of microcomputers, and Apple Computer Inc. did not quite have the resources of IBM.

One of the excellent features of the Apple II is the documentation that comes with it. I know of no other personal computer that comes with documentation of the quality of Apple's. Documentation is an important point, and I think BYTE a bit remiss for not insisting that Mr. Lemmons pay more explicit attention to this.

I hope that in future, fuller reviews of IBM's new system, BYTE will treat the documentation issue more extensively.

Stephen E. Bach
Rte. 2, Box 89
Scottsville, VA 24590

For a more in-depth description of IBM's documentation and its machine, see Gregg Williams' article on page 36 of this issue. . . . MH

Pushing Relatives

My thanks to George S. Losey for his article "Use a Relative Subroutine Call for Relocatable Z80 Programs" (see the October 1981 BYTE, page 366); it's a feature I could have used in the past.

The only problem, as stated by Mr. Losey, is that returns are limited to the unconditional types because of the use of the JP(HL) instruction to cause the return instead of the RET instruction. Also, programming is restricted because the HL register pair is tied up storing the return address.

Both these problems can be eliminated by making the first instruction of each subroutine PUSH HL (E5 hexadecimal). This places the return address on the stack as would a CALL instruction. This allows returns to be made in the usual manner. It also frees the HL register pair for programming.

Grant S. Killey
736 Michigan Ave. Apt. 13
Ontonagon, MI 49953

Some of the weaknesses of the Z80 relative-call technique proposed by George Losey in his October 1981 BYTE Technical Forum can be avoided at a cost of 10 more bytes in page 0 and an execution time longer by 23.25 microseconds. Instead of E1 E5 23 23 C9 hexadecimal at the reset location, try:

```
E5 E5 E1 E1 E1 23 23 E5 2B 2B
  E5 3B 3B E1 C9
```

The advantages are that no changes need to be made in the subroutine being called; it still ends with a RET, it can use conditional returns, and no registers are altered. Nested subroutines will work this way; they won't with George's method.

Lee Bonnifield
1025 Chalk Level Rd.
Durham, NC 27704

Beamin' Report

I want to tell BYTE readers about the service and the product that I received when I responded to an ad carried in the September 1981 BYTE. The ad was for the PowerText system by Beaman Porter, Inc. (see page 269). Both the product and the service provided by this company are outstanding, which is why I have taken the time to write about them. The growth of an industry often depends upon the commitment of the vendors to customer service. Beaman Porter is certainly an outstanding example of a commitment to customer service.

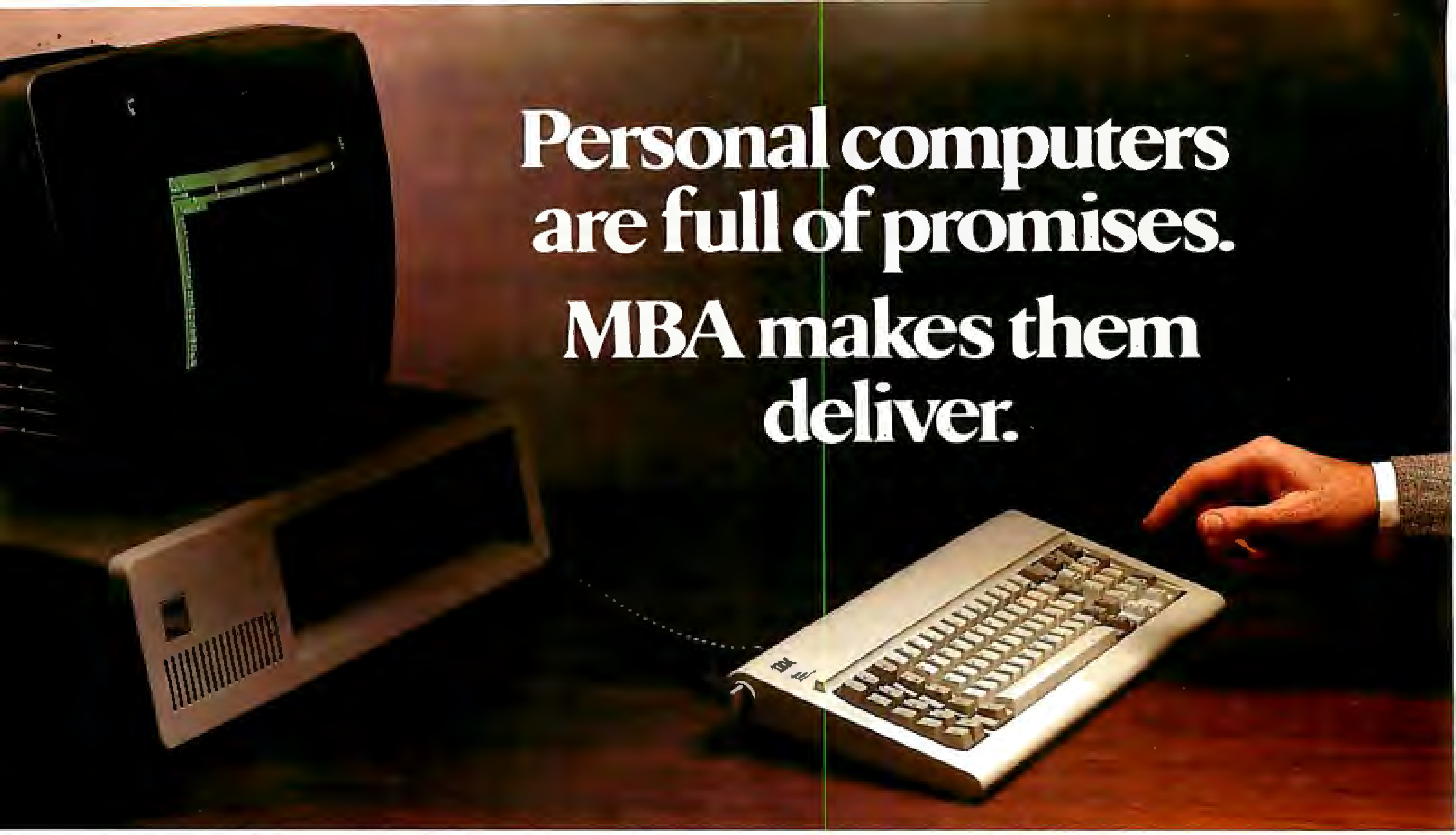
Several weeks ago, I was in the middle of preparing a lengthy report for a client when hardware problems caused me to lose not only all the text that I had created but also the use of the hardware to continue with the report. In a minor panic, I called Beaman Porter to order a copy of its Pascal-based text formatter. I sent payment special delivery, the company also used special delivery, and I had the package in four days. Included was a note indicating times when the author would be available to help me as I attempted to reproduce my report.

The PowerText package has performed without any problems. For the sort of consulting work that I do, it allows even greater productivity than the package I previously used. I called the company once for assistance and received it quickly and accurately.

Microcomputing is a mass market. It is encouraging to see that firms like Beaman Porter maintain a commitment to customer service.

My thanks to them.

Alan D. Tompkins
R.D. #1, Box 122C
Waitsfield, VT 05673■



You've heard how the personal computer is going to revolutionize the way you work.

So far, the reality hasn't measured up to the promises.

But now there's a remarkable new software package that transforms the IBM Personal Computer into an incredibly powerful management tool (Apple and Xerox owners: read on).

The first totally integrated management software.

There are a lot of useful programs available for personal computers.

Unfortunately, they all seem to use different commands and different ways of storing data. This creates two major problems:

1. Every time you want to add a new function, you have to learn a whole new command language.

2. You may not be able to exchange data between different programs.

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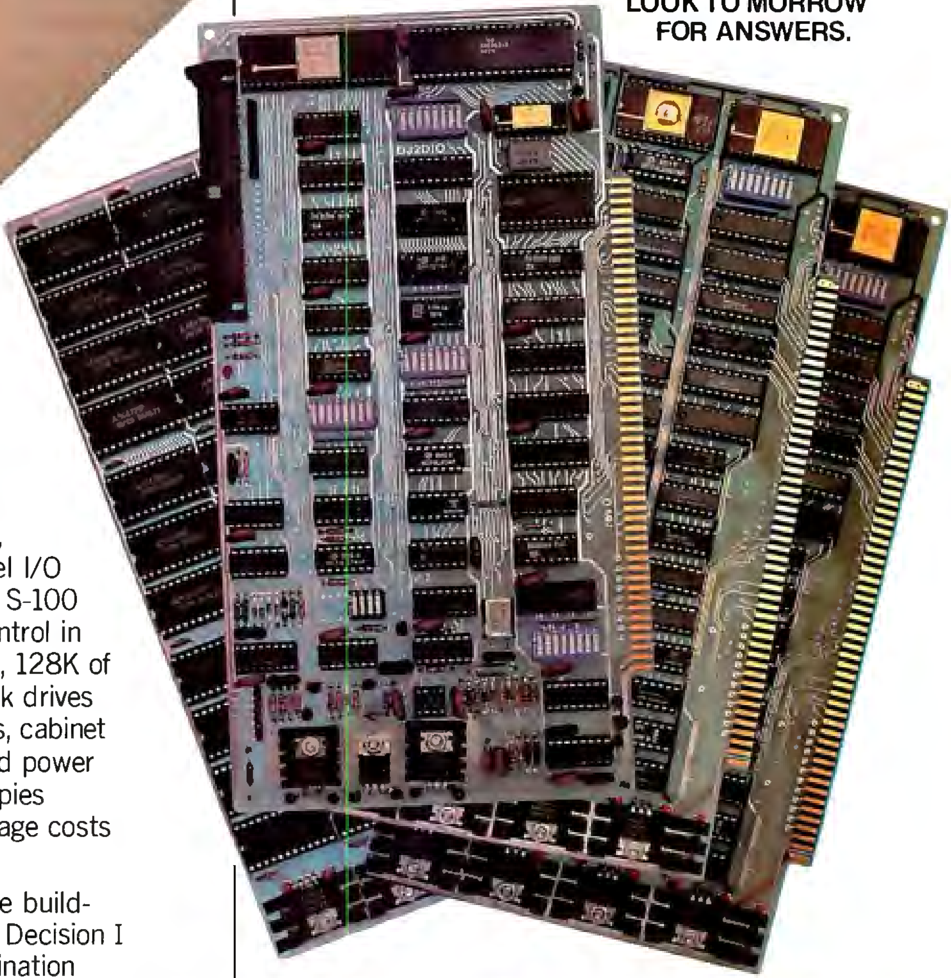

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The Atari Tutorial

Part 5: Scrolling

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Quite frequently, the amount of information that a programmer wants to display exceeds the amount of information that can fit on the screen. One way of solving this problem is to scroll the information across the display. For example, listings of BASIC programs scroll vertically from the bottom of the screen to the top. All personal computers implement this type of scrolling. The Atari personal computer system, however, has two additional scrolling facilities that offer exciting possibilities. The first is Load Memory Scan (LMS) coarse scrolling; the second is fine scrolling.

Conventional computers use coarse scrolling. With this type of scrolling, the pixels that hold the characters are fixed in position on the screen and the text is scrolled by moving bytes through the screen random-access read/write memory (RAM). The resolution of the scrolling is a single character pixel, which is very coarse. (Throughout this article, the term pixel refers to an entire character, not to the smaller dots that make up a character.) This produces a jerky and quite unpleasant scrolling. Furthermore, it is achieved by moving up to a thousand bytes around in memory, a slow and clumsy task. In essence, the program must move data through the playfield to scroll.

Some personal computers produce a somewhat finer scroll by drawing images in a higher-resolution graphics mode and then scrolling these images. Although higher scrolling resolution is achieved, more data must be moved to attain the scrolling and the program is consequently slowed.

The fundamental problem in both methods is that the scrolling is implemented by moving data through the screen area.

By manipulating just two address bytes, you can produce an effect identical to moving the entire screen RAM.

Coarse Scrolling

A better way to achieve coarse scrolling with the Atari 400/800 is to move the screen area over the data. The display-list op codes support a feature called Load Memory Scan (LMS). The LMS instruction was described in part 1 of this series. Briefly, it tells ANTIC where the screen memory is. A normal display list has one LMS instruction at the beginning of the display list. The RAM area it points to provides the screen data for the entire screen in a linear sequence. By manipulating the operand bytes of the LMS instruction, a primitive scroll can be implemented. In effect, this moves the playfield window over the screen data. Thus, by manipulating just two address bytes, you can produce an effect identical to moving the entire screen RAM. The program in listing 1 does just that. This program sweeps the display over the entire address space of the computer. The contents of the memory are dumped onto the screen. The scroll is a clumsy serial scroll combining horizontal scrolling with vertical scrolling. A pure vertical scroll can be achieved by adding or subtracting a fixed amount (the line length in bytes) to the LMS operand. The program in listing 2 does that.

A pure horizontal scroll is not as simple to do as a pure vertical scroll because the screen RAM for a simple display list is organized serially. The screen-data bytes for the lines are strung in sequence, with the bytes for one line immediately following the bytes for the previous line. We can horizontally scroll the lines by shifting all the bytes to the left: this is done by decrementing the LMS operand. The leftmost byte on each line, however, will then be scrolled into the rightmost position in the next higher line. The sample program in listing 1 illustrated this.

The solution is to expand the screen-data area and break it into a series of independent, horizontal-line

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Listing 1: *A simple program in Atari BASIC demonstrating coarse scrolling. Both horizontal and vertical scrolling are combined, but the end result is rather clumsy. The entire address space of the computer will be displayed.*

```
10  DLIST=PEEK(560)+256*PEEK(561):REM        find display list
20  LMSLOW=DLIST+4:REM                       get low address of LMS operand
30  LMSHIGH=DLIST+5:REM                      get high address of LMS operand
40  FOR I=0 TO 255:REM                       outer loop
50  POKE LMSHIGH,I
60  FOR J=0 TO 255:REM                       inner loop
70  POKE LMSLOW,J
80  FOR Y=1 TO 50:NEXT Y:REM                 delay loop
90  NEXT J
100 NEXT I
```

Listing 2: *An Atari BASIC program demonstrating a pure vertical scroll. The line length (in bytes) is either added to or subtracted from the LMS operand to achieve upward and downward scrolling, respectively. Lines 70, 120, and 130 accomplish this for upward scrolling only.*

```
10  GRAPHICS 0
20  DLIST=PEEK(560)+256*PEEK(561)
30  LMSLOW=DLIST+4
40  LMSHIGH=DLIST+5
50  SCREENLOW=0
60  SCREENHIGH=0
70  SCREENLOW=SCREENLOW+40:REM              next line
80  IF SCREENLOW<256 THEN GOTO 120:REM      overflow?
90  SCREENLOW=SCREENLOW-256:REM             yes, adjust pointer
100 SCREENHIGH=SCREENHIGH+1
110 IF SCREENHIGH=256 THEN END
120 POKE LMSLOW,SCREENLOW
130 POKE LMSHIGH,SCREENHIGH
140 GOTO 70
```

Listing 3: *An Atari BASIC program demonstrating pure horizontal scrolling. Each display line is actually 256 characters (bytes) long, though only 20 can be observed at any time. The 256-byte line is used in this example to simplify the program by avoiding the use of 2-byte address manipulations. The display produced scrolls from right to left. Upon reaching the end of the line, it starts over from the beginning.*

```
10  REM first set up the display list
20  POKE 1536,112:REM            8 blank lines
30  POKE 1537,112:REM            8 blank lines
40  POKE 1538,112:REM            8 blank lines
50  FOR I=1 TO 12:REM            loop to put in display list
60  POKE 1536+3*I,71:REM         BASIC mode 2 with LMS set
70  POKE 1536+3*I+1,0:REM        low byte of LMS operand
80  POKE 1536+3*I+2,I:REM        high byte of LMS operand
90  NEXT I
110 POKE 1575,65:REM             ANTIC JVB instruction
110 POKE 1576,0:REM              display list starts at $0600
120 POKE 1577,6
130 REM tell ANTIC where display list is
140 POKE 560,0
150 POKE 561,6
160 REM now scroll horizontally
170 FOR I=0 TO 235:REM           loop through LMS low bytes
175 REM we use 235—not 255—because screen width is 20 characters
180 FOR J=1 TO 12:REM            for each mode line
190 POKE 1536+3*J+1,I:REM        put in new LMS low byte
200 NEXT J
210 NEXT I
220 GOTO 170:REM                 endless loop
```

data areas. Figure 1 illustrates this idea. On the left is the normal arrangement. One-dimensional serial RAM is stacked in linear sequence to create the screen-data area. On the right is the arrangement needed for proper horizontal scrolling. The RAM is still one-dimensional and serial, but it is now used differently. The RAM for each horizontal line extends much further than the screen can show. This is no accident. The whole point of scrolling is to let a program display more information than the screen can hold. We can't show all that extra information if we don't allocate the RAM to hold it. With this arrangement we can implement true horizontal scrolling. We can move the screen window over the screen data without the undesirable vertical roll of the earlier approach.

The first step in implementing pure horizontal scrolling is to determine the total horizontal line length and allocate RAM accordingly. Next, a completely new display list with an LMS instruction on each mode line is written. The display list will, of course, be longer than usual, but there is no reason why we cannot write such a list. What values are used for the LMS operands? It is most convenient to use the address of the first byte of each horizontal screen-data line, the points marked with Xs in figure 1. Each mode line on the screen will have one such address. Once the new display list is in place, ANTIC must be informed of it and screen data must be written to populate the screen. To execute a scroll, each and every LMS operand in the display list must be incremented for a rightward scroll or decremented for a leftward scroll. Program logic must insure that the image does not scroll beyond the limits of the allocated RAM areas; otherwise, garbage displays will result. In setting up such logic, the programmer must remember that the LMS operand points to the first screen-data byte in the displayed line. The maximum value of the LMS operand is equal to the address of the last byte in the long horizontal line minus the number of bytes in one displayed line. As this process is

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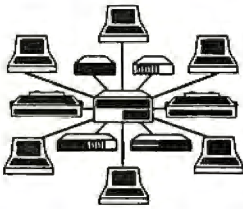

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rather intricate, let us work out an example.

First, the total horizontal line length is selected. For this example, we shall use a horizontal line length of 256 bytes. This will simplify address calculations. Each horizontal line will then require one page of RAM. Since we will use BASIC mode 2, 12 mode lines will be on screen; thus, 12 pages, or 3 K bytes, of RAM will be required. For simplicity (and to guarantee that our screen RAM will be populated with nonzero data) we will use the bottom 3 K bytes of RAM. Since this area is used by the operating system and disk operating system, it should be full of interesting data. To make matters more interesting, we'll put the display list on page 6 so that we can display it on the screen as we are scrolling. The initial values of the LMS operands will thus be particularly easy to calculate: the low-order bytes will all be zeros and the high-order bytes will be (in order) 0, 1, 2, etc.

The program in listing 3 performs these operations and scrolls the screen horizontally. This program scrolls the data from right to left. When the end of a page is reached, it simply starts over at the beginning. When executing this program, the display list is found on the sixth line down (it's on page 6). It appears as a sequence of double quotation marks.

The next step is to mix vertical and horizontal scrolling to get diagonal scrolling. Horizontal scrolling is achieved by adding 1 to or subtracting 1 from the LMS operand. Vertical scrolling is achieved by adding the line length to or subtracting the line length from the LMS operand. Diagonal scrolling is achieved by executing both operations. Four diagonal-scroll directions are possible. If, for example, the line length is 256 bytes and we wish to scroll down and to the right, we must add $256+(-1)=255$ to each LMS operand in the display list. This is a 2-byte add; the BASIC program example given in listing 3 avoids the difficulties of 2-byte address manipulations. However, most programs will not be so contrived. For truly fast two-dimensional scrolling, assembly language is necessary.

All sorts of weird arrangements are possible if we differentially manipulate the LMS bytes. Lines could scroll relative to each other, or hop over each other. Some of this could be done with a conventional display, but more data would have to be moved to do it. The real advantage of LMS scrolling is its speed. Instead of manipulating an entire screen full of data many thousands of bytes in size, a program need only manipulate perhaps a few dozen bytes.

Fine Scrolling

The second important scrolling facility of the Atari 400/800 is the fine-scrolling capability, scrolling a pixel in steps smaller than the pixel size. Coarse scrolls proceed in steps equal to one pixel dimension; fine scrolls proceed in steps of one scan line vertically and one color clock horizontally. Fine scrolling can only be carried so far. To get full fine scrolling over the entire screen, we must use fine scrolling with coarse scrolling.

Only two steps are required to implement fine scrolling. First, we set the fine-scroll enable bits in the display-list instruction bytes for the mode lines in which we want fine scrolling. (Since we generally want the entire screen to scroll, we set all the scroll enable bits in all the display-list instruction bytes.) Bit D5 of the display-list instruction is the vertical-scroll enable bit; bit D4 of the display-list instruction is the horizontal-scroll enable bit. We then store the scrolling value desired into the appropriate scrolling register.

Two scrolling registers are available, one for horizontal scrolling and one for vertical scrolling. The horizontal-scroll register (HSCROL) is at hexadecimal address D404; the vertical-scroll register (VSCROL) is at hexadecimal address D405. For horizontal scrolling, we store in HSCROL the number of color clocks by which we want the mode line scrolled. For vertical scrolling, we store in VSCROL the number of scan lines that we want the mode line scrolled. These scroll values will be applied to

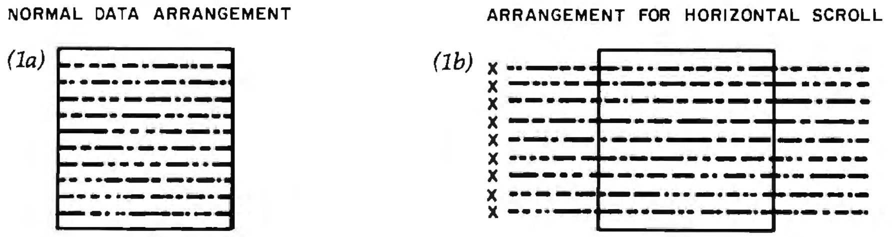

Figure 1: *Figure 1a shows how screen data are normally organized. Horizontal scrolling can be accomplished by arranging the screen-data area as shown in figure 1b.*

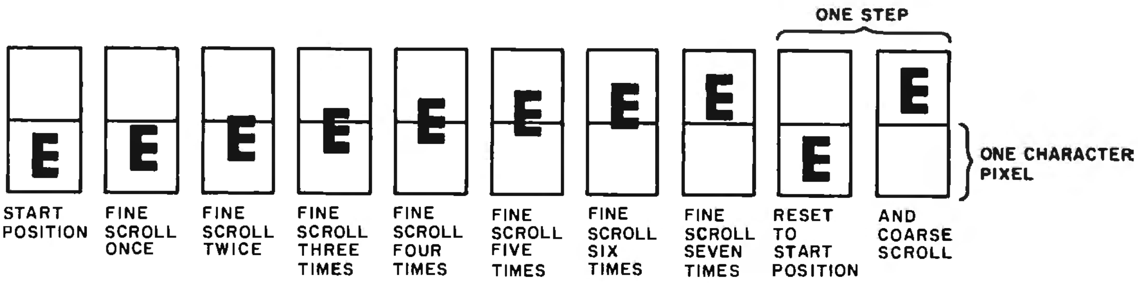

Figure 2: *In order to achieve fine scrolling over the entire display screen, a combination of fine and coarse scrolling is used. After the seventh fine scroll is performed, the fine-scroll register is reset and a coarse scroll is performed.*

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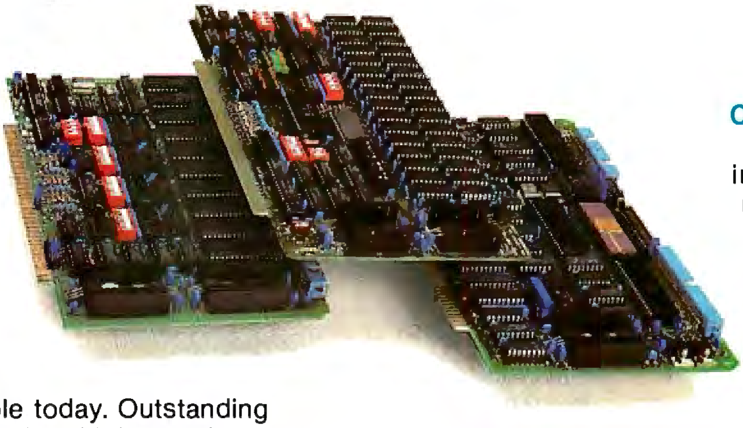

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Listing 4: *An Atari BASIC program demonstrating fine scrolling. Scroll registers should be changed only during vertical blanking, necessitating assembly-language programming for most applications. Otherwise, ANTIC gets confused and causes the screen to jerk.*

```
1   HSCROL=54276
2   VSCROL=54277
10  GRAPHICS 0:LIST
20  DLIST=PEEK(560)+256*PEEK(561)
30  POKE DLIST+10,50:REM         enable both scrolls
40  POKE DLIST+11,50:REM         do it for two mode lines
50  FOR Y=0 TO 7
60  POKE VSCROL,Y:REM            vertical scroll
70  GOSUB 200:REM                delay
80  NEXT Y
90  FOR X=0 TO 3
100  POKE HSCROL,X:REM           horizontal scroll
110  GOSUB 200:REM               delay
120  NEXT X
130  GOTO 40
200  FOR J=1 TO 200
210  NEXT J:RETURN
```

every line for which the respective fine scroll is enabled.

Two complicating factors are encountered when we use fine scrolling. Both arise from the fact that a partially scrolled display shows more information than a normal display. Consider, for example, what happens when we horizontally scroll a line by half a character to the left. The 40th character scrolls to the left, but what takes its place? Half of a new 41st character should scroll over to take the place of the now scrolled 40th character. But there are only 40 characters in a normal line.

The solution to this problem has already been built into the hardware with three display options for line widths: the narrow playfield (128 color clocks wide), the normal playfield (160 color clocks wide), and the wide playfield (192 color clocks wide). These options are chosen by setting appropriate bits in the DMACTL register. (DMACTL is at address D400 hexadecimal; most users will access shadow register SDMCTL at address 22F hexadecimal.) When using horizontal fine scrolling, ANTIC automatically retrieves more data from RAM than it displays. For example, if DMACTL is set for normal playfield, which in BASIC mode 0 has 40 bytes per line, ANTIC will actually retrieve data at a rate appropriate to wide playfield—48 bytes per line. This will throw lines off horizontally if it is not taken into account. The problem does not appear if the programmer has already organized screen RAM into long horizontal lines as in figure 1.

The corresponding problem for vertical scrolling can be handled in two ways. The sloppy way is to ignore it. We will not get half images at both ends of the display. Instead, the images at the bottom of the display will not scroll properly; they will suddenly pop into view. The proper way takes very little work.

To get proper fine scrolling into and out of the display region, we must dedicate one mode line to act as a buffer. This is done by refraining from setting the vertical-scroll bit in the display-list instruction of the last mode line of the vertically scrolled zone. The window will now scroll without the unpleasant jerk and the screen image will be shortened by one mode line. An advantage of scrolling displays now becomes apparent. It is quite possible to create screen images that have more than 192 scan lines in the display. This could be disastrous with a static display. However, with a scrolling display, images above or below the displayed region can always be scrolled into view.

Fine scrolling will only scroll so far. The vertical limit is 16 scan lines; the horizontal limit is 16 color clocks. If we attempt to scroll beyond these limits, ANTIC simply ignores the

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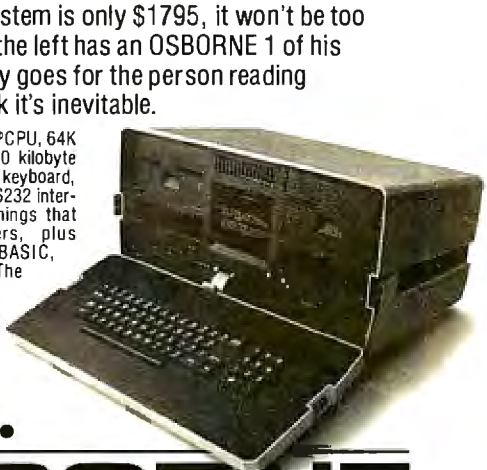

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higher bits of the scroll registers. To get full fine scrolling (in which the entire screen scrolls smoothly as far as we wish), we must couple fine scrolling with coarse scrolling. To do this we first fine scroll the image, keeping track of how far it has been scrolled. When the amount of fine scrolling equals the size of the pixel, we reset the fine-scroll register to zero and execute a coarse scroll. Figure 2 illustrates the process.

The program in listing 4 illustrates simple fine scrolling. It shows fine scrolling taking place at very slow speed and demonstrates several problems that arise when using fine scrolling. First, the display lines below the scrolled window are shifted to the right. This is due to ANTIC's automatically retrieving 48 bytes per line instead of 40. The problem arises only in unrealistic demonstration programs such as this one. In real scrolling applications, the arrangement of the screen data (as shown in figure 1) precludes this problem. A more serious problem arises when the scroll registers are modified while ANTIC is in the middle of its display process. This confuses ANTIC and causes the screen to jerk. The solution is to change the scroll registers only during vertical-blank periods. This can be done only with assembly-language routines. Thus, fine scrolling normally requires the use of assembly language.

Applications

The applications of full fine scrolling for graphics are numerous. An obvious application is for large maps created with character graphics. Using BASIC graphics mode 2, I have created a large map of Russia that contains about 10 screens full of image. The screen becomes a window to the map. The user can scroll over the entire map with a joystick. The system is very memory efficient: the entire map program, data, display list, and character-set definitions require a total of about 4 K bytes of RAM.

Any very large image that can be drawn with character graphics is amenable to this system. (Scrolling does not require character graphics, but map graphics are less desirable for scrolling applications because of their large memory requirements.) Large electronics schematics could be presented in this way. The joystick could be used both to scroll around the schematic and to indicate particular components that the user wishes to address. Large blueprints or architectural diagrams could also be displayed with this technique. Any big image that need not be seen in its entirety can be presented with this system.

Large blocks of text are also usable here, although it might not be practical to read continuous blocks of text by scrolling the image. This system is better suited to presenting blocks of independent text. One particularly exciting idea is to apply this system to menus. The program starts by presenting a welcome sign on the screen with signs pointing to submenus in other regions of the larger image. "This way to addition" might point up; "this way to subtraction" might point down. Users scroll around the menu with the joystick perusing their options. When making a choice, a cursor is placed on the option and the red button is pressed. Although this system could not be applied to all programs, it could be of great value to certain types of programs.

. . . And More

Two blue-sky applications of fine scrolling have not yet been fully explored. The first is selective fine scrolling, in which different mode lines of the display have different scroll bits enabled. Normally, we would want the entire screen to scroll, but it is not necessary to do so. We could select one line for horizontal scrolling only, another line for vertical scrolling only, and so forth. The second blue-sky feature is the prospect of using display-list interrupts to change the HSCROL or VSCROL registers "on the fly." Changing VSCROL on the fly is a tricky operation; it would probably confuse ANTIC and produce undesirable results. Changing HSCROL is also tricky, but might be easier.■

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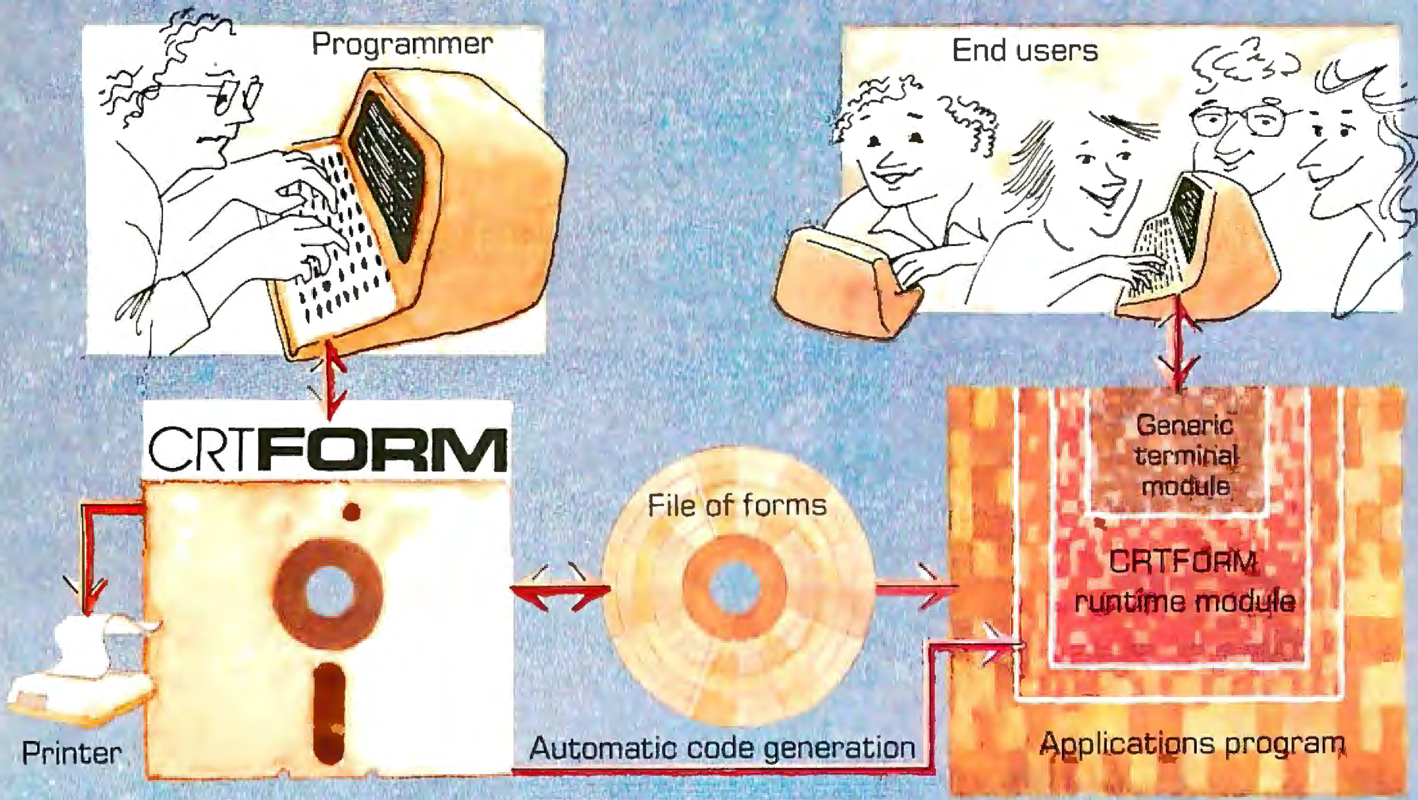

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A Closer Look at the IBM Personal Computer

Gregg Williams
Senior Editor

What microcomputer has color graphics like the Apple II, an 80-column display like the TRS-80 Model II, a redefinable character set like the Atari 800, a 16-bit microprocessor like the Texas Instruments TI 99/4, an expanded memory space like the Apple III, a full-function uppercase and lowercase keyboard like the TRS-80 Model III, and BASIC color graphics like the TRS-80 Color Computer? Answer: the IBM Personal Computer, which is a synthesis of the best the microcomputer industry has offered to date. It has a number of interesting features and a few flaws, but it is easily the best-designed microcomputer to date. In this article, I will take a closer look at the IBM Personal Computer, inside and outside.

An Overview

The IBM Personal Computer (photos 1 and 2) is housed in two units, the keyboard and the System Unit. The keyboard (photo 3) has a standard typewriter layout with the addition of a numeric keypad to the right, a set of function keys to the left, and miscellaneous other keys to bring the total number to 83. It is connected by a coiled cable to the System Unit, which houses the Intel 8088 microprocessor, the 40 K-byte extended Microsoft BASIC in ROM (read-only memory), up to 64 K bytes of dynamic memory, up to two disk drives, a cassette interface, a built-in speaker, and five expansion slots. (Extra dynamic memory cards placed in expansion slots can bring the total up to 256 K bytes.)

Other peripherals include the IBM Monochrome Display (shown in photo 2) and the IBM 80 CPS (characters per second) Matrix

Photo 1: *The IBM Personal Computer System with a non-IBM color monitor.*

Printer (shown with the optional printer stand in photo 1).

What's It Going to Cost?

The IBM Personal Computer is an impressive unit. But how much is it going to cost? Although the component prices in the "At a Glance" textbox look reasonable (the System Unit and keyboard are only $1265), the price of a usable configuration is somewhat higher. The higher cost is due to a marketing technique called *unbundling,* which is common in the computer industry and a trademark of IBM in particular. When a system is unbundled, components that usually are priced as one are priced separately. In the case of the IBM Personal Computer, the main unit needs one of two video-display adapter cards, a monitor or television set, a cable, and perhaps an external radio-frequency (RF) modulator.

Table 1a shows several sample configurations of the IBM Personal Computer, and tables 1b and 1c show the list prices of comparable Apple II and Radio Shack TRS-80 Model III units with 48 K bytes of memory and one disk drive. The IBM unit is somewhat more expensive than the standard configurations (note that the Apple II Plus is less expensive if you want only 40-column uppercase output). Still, you get a *lot* more for your money.

Video-Display Options

One thing not commonly understood about the IBM Personal Computer is that you must choose between two separate ways of getting video output. The Monochrome Display and Printer Adapter gives high-quality black-and-white output only, while the Color/Graphics Monitor Adapter can produce color graphics or text. Each takes one of the five expansion slots available on the IBM motherboard (called the System Board by IBM). While you could have both kinds of output by using both adapter cards, most people will not want to tie up the extra slot (more on that later).

The monochrome adapter card is most suited to IBM machines that will be used in an office environment only. The adapter card gives you a

Photo 2: *The IBM Personal Computer System with the IBM Monochrome Display.*

Photo 3: *The IBM Personal Computer keyboard unit.*

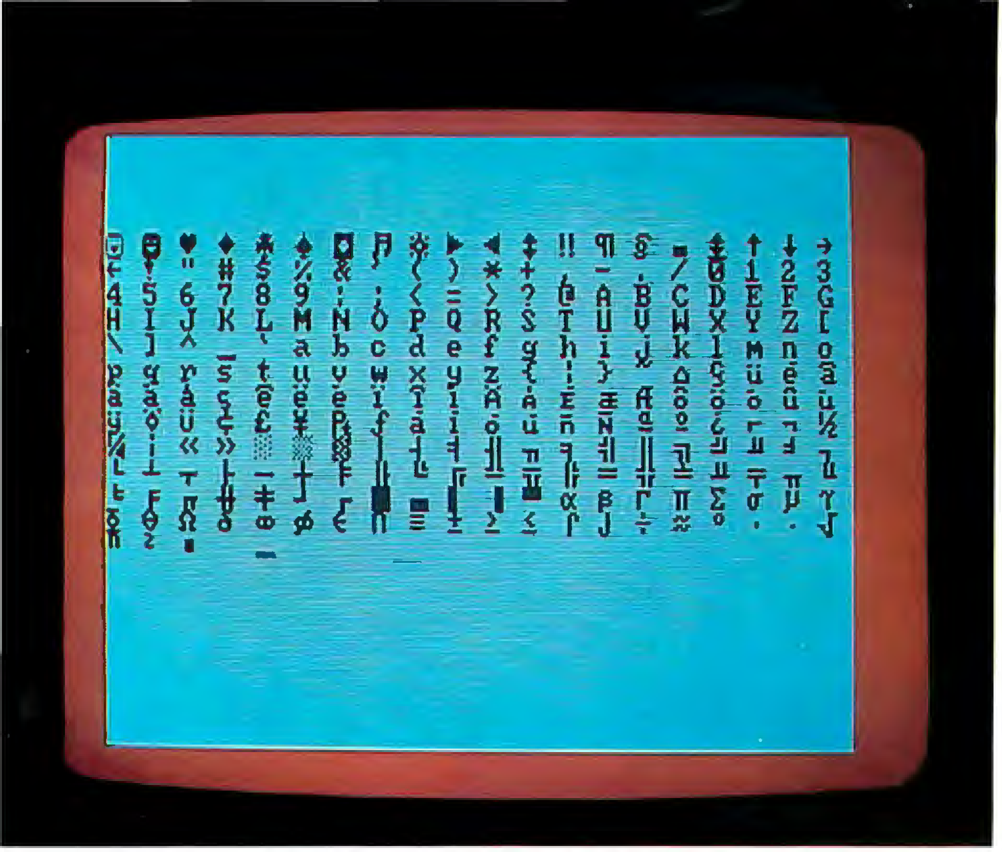


Photo 4: *The 256 characters available on the IBM Personal Computer video display.*

sharp 25-line by 80-column display with well-formed characters. A 9 by 14 dot matrix is used, and characters are displayed within a 7 by 9 dot matrix; this makes for an extremely readable screen, an important factor if you are using the computer for long periods of time.

Among the 256 characters available are miscellaneous graphics characters (musical note, male and female symbols), all standard uppercase and lowercase letters, numbers, punctuation, some familiar foreign-language, Greek, and mathematics symbols, and a set of rectangular shapes that can be combined to create rectangles and lined tables. A display of the full 256-character set is shown in photo 4.

Although you can use a suitable monitor if you want, the IBM Monochrome Display is also available. The IBM monitor has a green-phosphor tube and matches the appearance of the rest of the system.

The monochrome adapter card contains 4 K bytes of on-board memory. (In this article, 8 bits will be referred to as a "byte," as opposed to a 16-bit "word.") The on-board display memory prevents the available system memory from being steadily decreased by peripheral cards. In addition, due to the architecture of the 8088 microprocessor, the on-board memory itself does not reduce the main memory address space available to the IBM microcomputer; in contrast, the memory taken by the video display of an 8-bit microcomputer always reduces its 64 K-byte workspace.

The manuals will set the standard for all microcomputer documentation in the future.

Twenty-five lines of 80 characters each amounts to only 2000 characters, yet the on-board display memory has 4096 bytes. The reason for this is that the IBM Personal Computer *always* uses two bytes per stored character, regardless of the adapter card used. When the monochrome adapter card is used, individual characters can have any of the following characteristics: invisible (white-on-white, black-on-black), blinking, high-intensity, or underline. The permissible combinations of these are shown in figure 1.

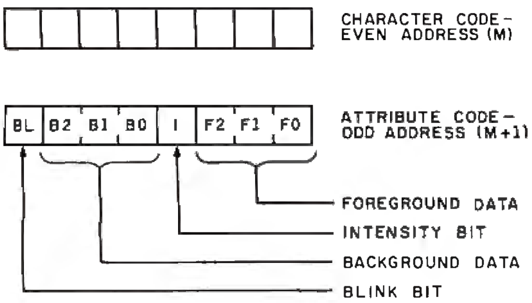
One final advantage of the monochrome adapter card is that it includes an interface to the IBM 80 CPS Matrix Printer, which saves you the expense of an IBM Printer Adapter card (around $150) and one expansion slot.

Of course, the main disadvantage of the monochrome adapter card is that it does not produce color graphics. As you can see from photos 5a through 5d, this is some disadvantage. The graphics available through the color/graphics adapter card are very good—slightly better than color graphics on existing microcomputers, and they are more versatile and easier to use.

Color/Graphics Monitor Adapter

Residing in one of the five expansion slots in the System Unit, the Color/Graphics Monitor Adapter has 16 K bytes of on-board memory, can display two kinds of text and two (actually, three) kinds of graphics, and allows you to connect to a black-and-white monitor or to a color monitor with composite or RGB (red-green-blue) input, or to a color television. The color pictures accompanying this article were made with a $1000 RGB color monitor, so don't expect such stunning graphics to come from your composite monitor or an ordinary color television. (RGB monitors are more expensive and produce better images because they have separate red, green, and blue inputs to get a more detailed image. For an RGB monitor to work properly with the color/graphics adapter card, it must accept the following signals: red, green, blue, intensity, horizontal drive, vertical drive, and ground. RGB monitors that do not have an intensity signal can display only 8 of the possible 16 colors.)

Let's consider graphics first. The IBM color/graphics adapter card has three color-graphics resolutions, only two of which are supported by the system software in ROM. The first mode, the IBM low-resolution mode, is unsupported by IBM. It gives you a display of 100 rows and 160 pixels (picture elements), each of which can be any of the standard 16 colors (for the color list, see table 2). IBM



BACKGROUND			FOREGROUND			RESULTING CHARACTER
B2	B1	B0	F2	F1	F0	
0	0	0	0	0	0	NON DISPLAY (BLACK ON BLACK)
0	0	0	0	0	1	NORMAL UNDERLINED CHARACTER
0	0	0	1	1	1	NORMAL CHARACTER
1	1	1	0	0	0	REVERSE CHARACTER (BLACK ON WHITE)
1	1	1	1	1	1	NON DISPLAY (WHITE ON WHITE)

Figure 1: *Character storage within the monochrome adapter board.*

representatives told me that the only way to use this mode is to directly address the Motorola 6845 CRT Controller, which is at the heart of both the monochrome and color/graphics adapter cards. (For both units, the 6845 device is addressed through two ports: hexadecimal 3D4 and 3D5; more information on this is given in *Technical Reference,* the IBM Personal Computer manual.)

The IBM medium-resolution mode is comparable to what Apple calls its high-resolution mode. It allows 200 rows of 320 pixels each, with four possible colors. (The Apple II allows four colors plus black and white.) The colors are referred to in memory as colors 0 through 3. Color 0 can be any of the 16 colors available, while colors 1 through 3 are set by choosing one of two three-color sets. Set 1 produces cyan, magenta, and white, while set 2 produces green, red, and brown; only the colors from one set are available at any one time. Each byte represents 4 pixels; the mapping scheme is shown in figure 2.

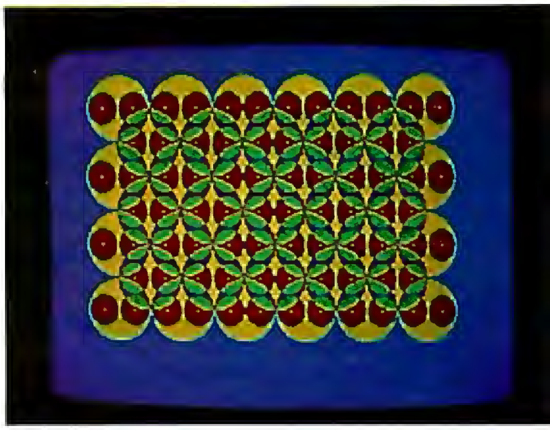
The IBM high-resolution mode uses a white-on-black image and gives you control of 200 rows of 640 pixels each. (Although it is not a well-known fact, the Apple II can display a resolution of 192 by 560 on a black-and-white monitor, although there are some limitations to pixel locations and the mode must be supported by user-supplied software.) In the IBM high-resolution mode, the mapping of graphics bytes to video scan lines is the same as for medium-resolution graphics, but each byte represents 8 pixels.

Photos 6a and 6b show one edge of the screen to highlight the differences between IBM medium-resolution and high-resolution graphics. As you would expect, corresponding lines in the IBM high-resolution mode are finer drawn, but I can't see that much difference between the two modes.

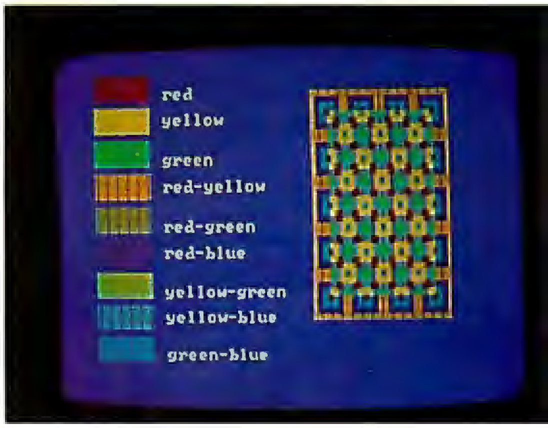
The color/graphics adapter card supports two text formats: the first, suitable for color televisions and composite monitors, is 25 rows of 40 characters each, while the second, usable by RGB monitors only, is 25 rows of 80 characters each. The card displays characters in an 8 by 8 dot matrix, with characters being drawn in a 5 by 7 dot matrix.

Although the IBM microcomputer has separate text and graphics modes, text can be displayed while in the graphics mode. If you are in graphics mode and want to print text, you simply give the appropriate command (for example, PRINT when in BASIC) and the computer draws the

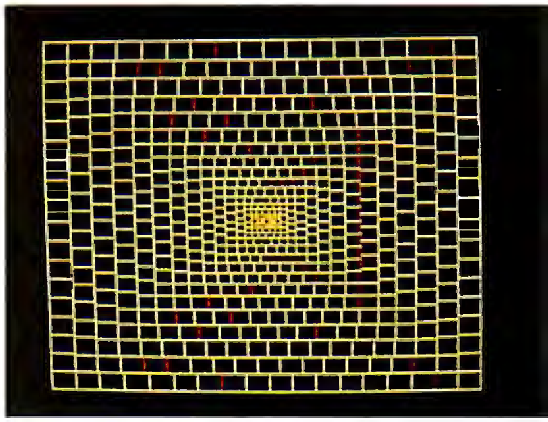
5a



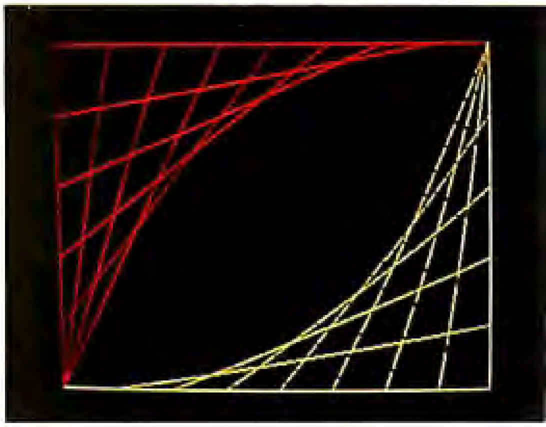
5b



5c



5d



Photos 5a-5d: *Four examples of IBM medium-resolution color graphics.*

characters on the graphics screen automatically. An example of this is shown in photo 7. While using a text screen, you have access to the same 256-character set used by the monochrome adapter card. If you are using a graphics screen, you have access to only the bottom 128 characters (some symbols, all punctuation, digits, uppercase and lowercase letters). The top 128 characters can be user defined by pointing interrupt vector hexadecimal 1F (contained in hexadecimal memory locations 7C through 7F) to the beginning of a 1 K-byte area that defines the dot pattern of the top 128 characters, 8 bytes per character.

In the text modes, each character can be one of sixteen colors, with the background of that character being one of eight colors, or the text can be displayed without a color signal (for black-and-white monitors). This is done automatically in BASIC with the COLOR statement. The data that cause a given combination are stored in the attribute byte for each character. Figure 3 shows the layout of the data in the attribute byte, and photo 8 shows an example of multiple background and foreground colors used with text.

Since the color/graphics adapter card has 16 K bytes of memory and the two kinds of text pages take only 2000 and 4000 bytes, respectively, you can store up to four 80-column pages of text or eight 40-column pages at once. In addition, you can specify the display of a page independent of the page actually being written to at the moment. In BASIC, all this is available from the SCREEN statement.

1a
IBM Personal Computer (suggested retail prices)

48 K-byte cassette-based unit with color/graphics adapter card	$1745
all the above, plus one floppy-disk drive, adapter card, and DOS software	$2575
all the above, plus 16 K bytes more (total, 64 K bytes) and game adapter card	$2720
all the above, plus a second disk drive	$3290
all the above, plus one 64 K-byte card (total, 128 K bytes)	$3830

1b
Apple II Plus

48 K-byte Apple II Plus with one floppy-disk drive and DOS software	$2175
all of the above, plus Videx Videoterm and Enhancer II (to modify Apple for 80-column display and upper- and lowercase keyboard)	$2788

1c
Radio Shack TRS-80 Model III

48 K-byte unit with one floppy-disk drive and DOS software	$1995

Table 1: *Prices for several versions of the IBM Personal Computer and roughly comparable Apple II Plus and Radio Shack TRS-80 Model III microcomputers. The versions to be compared are shaded.*

Intensity	Red Bit	Green Bit	Blue Bit	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

Table 2: *The 16 available colors on the IBM Personal Computer, and their representation in memory. When only the first eight colors are available (*intensity = 0*), they can be represented with only the bottom three bits.*

Inside the Main Unit

The IBM Personal Computer is as well designed on the inside as it is on the outside. As shown in photo 9a, the five expansion slots are in the upper left corner, the memory and an internal speaker are in the lower left corner, and the floppy-disk drives (if any) are in the lower right corner. Figure 4 shows the signals on the IBM expansion slot, and table 3 gives the full names of the signals. The bus allows four DMA (direct-memory access) channels, one of which is used to refresh the dynamic memory, the others for high-speed DMA data transfer between memory and peripheral cards. In addition, the bus supports eight levels of interrupts, six of which are available to the user.

The system memory is shown in detail in photo 9b. The set of eight large integrated circuits with gold faces is the 40 K-byte extended Microsoft BASIC in ROM. Notice the empty socket at the bottom of the same row; this can house an 8 K-byte ROM or EPROM (erasable programmable read-only memory). Just to the right of the ROMs are four rows of 4116 dynamic memory rated with an access time of 250 ns. Only the first row is filled in a 16 K-byte IBM microcomputer; successive rows are filled to bring the microcomputer to 64 K bytes before additional memory is added through the expansion slots.

Notice that there are nine integrated circuits per row. The device on the extreme left is used as a parity bit. To increase the reliability of the system, IBM has made all user memory (i.e., all the memory used for programs and data) 9 bits wide. When a parity error is detected, the IBM microcomputer issues the appropriate error message and stops whatever program is running; this prevents an application program from continuing if it has read the memory incorrectly.

In the middle of the right half of the board are two DIP (dual inline package) switches that set certain parameters of the system. The positions of these switches tell the IBM microcomputer how many disk drives are installed, what kind of video device is attached, and how much memory is in the system. These switches are usually hidden by the floppy-disk-drive cables, as shown in photo 9a.

Photo 9c shows the Intel 8088 microprocessor (the large device in the center) and, above it, an integrated circuit socket identified by IBM only as an "auxiliary processor socket." An IBM representative would only say that the slot could house "any architecturally compatible processor," but it is probable that the device to go in that slot is an Intel 8087, a mathematics coprocessor device. With the appropriate software, the Intel 8087 or something similar could improve the performance of the IBM microcomputer.

Photo 9d shows one of the IBM peripheral cards, the 64KB Memory Expansion Option. This card is interesting in that it uses two modified 4116 16 K-bit dynamic memory devices "piggybacked" into each 18-pin socket. IBM was buying a lot of these two years ago—now we know where they went.

The Intel 8088 itself is functionally equivalent to the 16-bit Intel 8086 microprocessor, except that all 16-bit input/output (I/O) is done 8 bits at a time, with the help of a few extra support devices. Even though the 8088 has the same instruction set as the 16-bit 8086 microprocessor, the necessity of funneling all data through an 8-bit path degrades the 8088's performance to the point

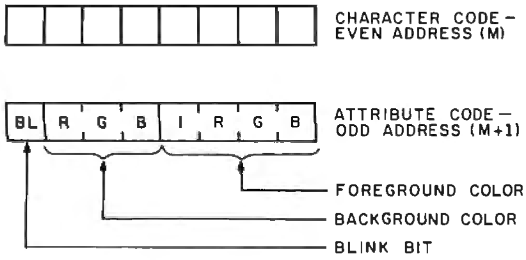
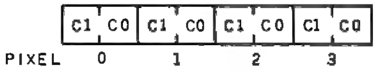


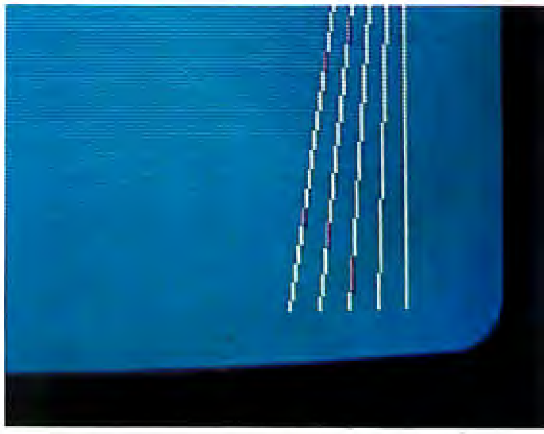
Figure 2: *IBM medium-resolution-graphics storage within the color/graphics adapter board.*



C1	C0	COLOR NUMBER	WHERE FROM?
0	0	0	ANY OF 16 COLORS
0	1	1	FROM SELECTED COLOR SET
1	0	2	
1	1	3	

Figure 3: *Character storage within the color/graphics adapter board.*

6a



6b

Photo 6: *Close-up views of equivalent screen images using IBM medium-resolution (photo 6a) and high-resolution (photo 6b) graphics.*

Photo 7: *An example of combining text and graphics on the same video screen. The program shown, when run, generates the circular image just above it.*

Signal Name	Description
OSC	14.31818 MHz oscillator signal
CLK	4.77 MHz system clock
RESET DRV	reset driver; resets system logic
A0 through A19	address bits 0 (low) through 19 (high)
D0 through D7	data bits 0 through 7
ALE	address latch enable
I/O CH CK	I/O channel check
I/O CH RDY	I/O channel ready
IRQ2 through IRQ7	interrupt request 2 (highest priority) through 7 (lowest)
IOR	I/O read command line
IOW	I/O write command line
MEMR	memory read command line
MEMW	memory write command line
DRQ1 through DRQ3	DMA request 1 through 3
DACK0 through DACK3	DMA acknowledge 0 through 3
AEN	address enable
T/C	terminal count

Table 3: *Signal names and descriptions for the IBM Personal Computer System Board I/O Channel (expansion slot). See also figure 4.*

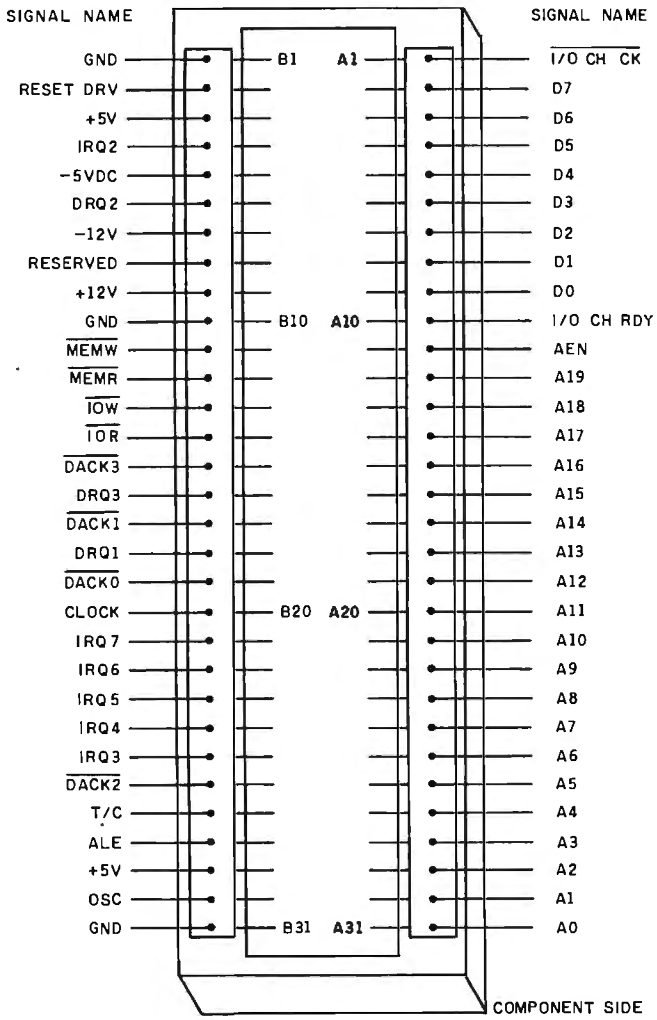


Figure 4: *Electrical signals on the IBM System Board I/O Channel (expansion slot). See table 3 for signal descriptions.*

where it is more like a fast 8-bit microprocessor with an extended instruction set than it is a 16-bit microprocessor. After all, how much processing can you do on a number without accessing memory again?

Still, the IBM microcomputer combines the architecture of a 16-bit machine with the cost advantages of using familiar 8-bit memory and system design. The 8088 microprocessor in the IBM microcomputer runs at 4.77 MHz.

The disk drives are soft-sectored, double-density, single-sided drives that use MFM (modified frequency modulation) encoding. The floppy-disk drive uses 40 tracks per disk, with eight 512-byte sectors per track. This results in 163,840 bytes of storage per drive. The drive has a motor-start time of 500 ms, a track-to-track seek time of 8 ms, and a data transfer rate of 250 K bits (not bytes) per second.

The IBM Personal Computer includes a cassette-recorder interface that connects to any good-quality cassette recorder through a user-supplied cable. The IBM microcomputer can be configured to use either the microphone or the auxiliary input of the recorder by changing a jumper on the bottom of the main printed-circuit board in the System Unit. The data-transfer rate is between 1000 and 2000 bits per second (bps), depending on the content of the data. The signals used to control a cassette recorder are motor control, ground, data in, and data out.

The right side of the back panel of the main unit (photo 10) contains whatever sockets are made available by the peripheral cards plugged into the expansion slots. Unused slots are masked by metal plates to prevent the escape of any RF radiation. The bottom left corner of the panel contains the power plug to the IBM Monochrome Display and the plug for the main power supply. In the bottom center of the panel are 5-pin DIN plugs that go to the keyboard (left) and the cassette tape recorder (right).

The Keyboard

The keyboard (see photo 3) is one

of the most important components of any computer because it is the primary device through which you give instructions to the computer. Most existing microcomputers have something wrong with their keyboard design; the most common errors are functions unavailable from the keyboard and poor keyboard layout. With one exception, the IBM keyboard seems to be faultless. It is, bar none, the best keyboard on any microcomputer.

The IBM keyboard abounds with good features. The keys have a nice "feel" to them and give tactile and audible feedback when pressed. The keyboard is a separate unit that can be placed up to several feet away from the main unit. It is light enough to rest and use in your lap. The keys themselves are "sculpted"—that is, an imaginary plane touching all the key tops has a slight concave curve to it. The keyboard has two plastic feet that can be used to tilt it up when it is used on a flat surface. A plastic ledge just above the top row of keys can be used to prop an open book between the video display and the keyboard.

Several keyboard features deserve more description. The right side of the keyboard contains a numeric keypad that doubles, in certain situations, as a set of text and cursor-movement keys. The left side contains ten function keys, whose functions can change with the application. (The twenty-fifth line of the video display can be used to illustrate their current use, and you can redefine these keys at any time from BASIC.)

Three keys must be pressed simultaneously to restart the system: Ctrl, Alt, and Del; it takes two hands to do this. Depressing the Ctrl and Scroll Lock/Break keys interrupts a running BASIC program. The up-arrow (shift) and PrtSc keys cause the text contents of the video display to be printed. Ctrl plus Num Lock causes the executing BASIC program to pause; the next key pressed causes it to resume.

The Alt key lets you generate any extended ASCII value from 1 to 255, even if that code is not otherwise generated by the keyboard. By holding down the Alt key and typing a number between 1 and 255 on the numeric keypad, that code is generated when the Alt key is released. (For some reason, the IBM unit I tried would not generate 0 with the Alt key. However, 0 could be generated by Ctrl plus the 2 key on the top row of the keyboard.)

Photo 8: *An example showing the independence of foreground and background colors when using the text mode of the color/graphics adapter board.*

By not having a full product line, the IBM Personal Computer may fall prey to hardware and software incompatibility.

Another nice feature of the IBM keyboard is its 10-character type-ahead buffer, which keeps you from losing keystrokes if you type information into the IBM microcomputer before it is ready to receive it. In addition, the system software is written such that every key has an auto-repeat feature; i.e., every key repeats its function if it is held down for more than half a second.

My one complaint against the keyboard is minor. The right and left shift keys are one key farther away from the center of the board than most people are used to. This means that, until you get used to reaching for the shift keys, you will accidentally type the slash and reverse-slash keys instead. This problem is minor, however, compared to some of the gigantic mistakes made on almost every other microcomputer keyboard. The IBM Personal Computer is a delight to use largely because of its keyboard.

System Startup

When the IBM Personal Computer is first turned on, a series of fourteen tests are performed on the system, and any errors are reported immediately. These include tests of the 8088 microprocessor, the internal ROM, the main memory, the video-display adapter card, the keyboard, the cassette recorder (if attached), and the floppy-disk system. The memory test includes five different read/write tests of the entire user-memory area, each using a different bit pattern for testing. Because of this, the initial startup of the IBM microcomputer may take between 5 seconds and about 1.5 minutes, depending on how much memory is in the machine. For example, in my test a 64 K-byte, disk-based machine took about 18 seconds to complete its initial tests and about 25 seconds more to complete the bootup of the machine. When the system is restarted from the keyboard with the Ctrl-Alt-Del triad of keys, the system tests are omitted, thus greatly reducing the delay associated with rebooting.

Three Levels of BASIC

Because BASIC is the most commonly used programming language, I plan to describe some of the features of the 40 K-byte extended Microsoft BASIC in great detail. But before I start talking about the more prominent features of BASIC, I'll look at the three kinds of BASIC that are available with the IBM Personal Computer.

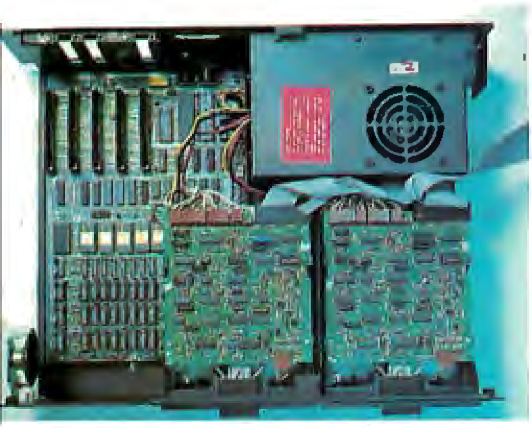
Cassette BASIC is the simplest BASIC you can get. It is available on *every* IBM microcomputer, and it is contained in the 40 K bytes of ROM mentioned before. In addition to the standard features that are associated with Microsoft BASIC, Cassette BASIC gives you the ability to plot points and draw lines in both the IBM medium- and high-resolution modes, to make sounds through the internal speaker, and to use light pens and joysticks.

Disk BASIC, which requires at least 32 K bytes of memory and one floppy-disk drive, occupies extra user memory which can be added to the ROM version of BASIC. The IBM

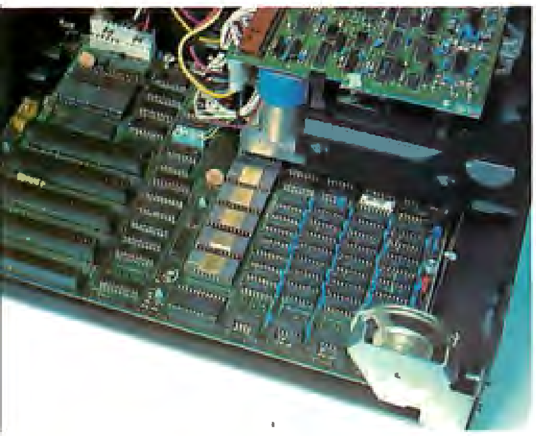
Command	Description
AUTO	generates line numbers automatically
BLOAD	load machine-language (binary) program
BSAVE	save machine-language program
CLEAR	clear program variables
CONT	continue interrupted program
DELETE	deletes a range of BASIC lines
EDIT	edit a line of BASIC
FILES	list all or selected files on disk
KILL	delete a disk file
LIST	list BASIC lines
LLIST	list BASIC lines to printer
LOAD	load a BASIC program file
MERGE	merge a BASIC program file into an existing program
NAME	rename a disk file
NEW	erase current program
RENUM	renumber BASIC program
RESET	close all disk files
RUN	load and run program
SAVE	save current program
SYSTEM	exit BASIC and return to DOS
TRON, TROFF	turn tracing option on and off

Table 4a: *A summary of IBM BASIC commands.*

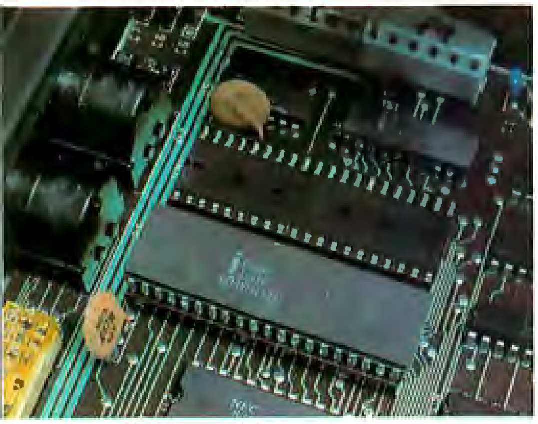
9a



9b



9c



9d

Photo 9: *Inside the IBM Personal Computer System Unit. Photo 9a shows the overall interior of the unit; the floppy-disk drives are in the lower right corner, and the expansion slots are in the upper left. Photo 9b is a detailed shot of the expansion slots (left), the BASIC in ROM (large devices with gold faces, center), and the workspace memory (right). Photo 9c shows the Intel 8088 microprocessor (bottom) and the empty "auxiliary processor socket" (just above the 8088). Photo 9d shows the IBM 64KB Memory Expansion Option card, which holds 64 K bytes of memory. Notice that two 4116-like devices are "piggybacked" into one socket.*

DOS (disk operating system) takes 12 K bytes of user memory, and disk BASIC adds about another 12 K bytes (depending on certain options). Disk BASIC adds a large number of disk input and output options, access to a date and time-of-day clock, the ability to store and redraw rectangular areas of graphic images, communications support using a standard RS-232C port, and software support for two extra printers. Disk BASIC is called by typing "BASIC" from the DOS prompt.

Advanced BASIC, which requires at least 48 K bytes of memory and one floppy-disk drive, occupies an additional 5 K bytes of user memory (for a total overhead of about 29 K bytes). Advanced BASIC adds event trapping, some advanced graphics commands, and an advanced music-playing command (all of these are covered in greater detail later). Advanced BASIC is called by typing "BASICA" from the DOS prompt.

Tables 4a, 4b, and 4c list the commands, statements, and functions of IBM BASIC.

The BASIC Program Editor

The BASIC Program Editor, common to all the versions of IBM BASIC, allows you to make changes far more quickly and easily than is possible on other microcomputers. It is a full-screen editor in that changes can be made to a program line by use of the four arrow keys and the Ctrl (control), Ins (insert), Del (delete), and End keys. If the new line (enter) key is pressed while the cursor is *anywhere* on the program line where changes have just been made, the changed line takes the place of the old line. With the BASIC Program Editor, changing a program is as easy as it would be if the text of the program were being manipulated by a word processor.

In addition, the Alt key has a special function within BASIC. Simultaneously pressing Alt and a letter of the alphabet causes a predefined BASIC keyword to be printed on the screen. For example, Alt plus C causes the word "COLOR" to be printed. This "shorthand" method is often helpful when you are typing in a long BASIC program.

Along the same lines, all levels of IBM BASIC have the AUTO (automatic line numbering), RENUM (renumber a BASIC program), and MERGE (merge two programs) commands—all very useful commands that are often absent or awkward to use in other microcomputers.

Graphics in BASIC

The following summarizes most of the graphics commands available from BASIC:

- COLOR (all BASICs) is used to choose the four colors available in the IBM medium-resolution mode. As stated before, color 0 can be any of

At a Glance

Product Name
The IBM Personal Computer

Manufacturer
International Business Machines Corporation
Information Systems Division
Entry Systems Business
POB 1328
Boca Raton, FL 33432

Components
System Unit
Size: width 20 inches, depth 16 inches, height 5.5 inches; weight (without disk drives) 21 pounds, (with two disk drives) 28 pounds
Electrical needs: 120 VAC
Processor: Intel 8088
Cycle Time: main storage, 410 nanoseconds; access, 250 nanoseconds
Memory: 40 K bytes of built-in ROM (read-only memory), 16 K bytes of user RAM (random-access read/write memory); expandable to 256 K bytes
Standard: keyboard for data and text entry; audio-cassette recorder connector; five expansion slots for memory, display, printer, communications, and game adapters; built-in speaker for music programming; power-on automatic self-test of system components; BASIC-language interpreter; 16 K bytes of user RAM (all user RAM includes parity bit)
Keyboard: total of 83 keys for data and text entry; includes 10 keys for numeric entry and cursor control, 10 special function keys, and ASCII characters and special graphics characters (total 256 characters); automatic repeat on all keys; adjustable typing angle; detachable six-foot coil cable
Disk drives: up to two 5-inch floppy-disk drives, 160 K bytes each (will accommodate 4 drives in future)

Operating Systems
IBM Personal Computer DOS (Microsoft)

Software Available for IBM Personal Computer DOS
BASIC interpreter (Microsoft) standard; extended BASIC interpreter (Microsoft) $40; Pascal compiler (Microsoft) $300; VisiCalc (Personal Software) $200; EasyWriter (Information Unlimited Software) $175; General Ledger, Accounts Receivable, Accounts Payable (Peachtree Software) $595 each; asynchronous communications support $40; Adventure (Microsoft) $30; Advanced diagnostics package $155

Hardware Prices

System Unit, 16 K-byte RAM, keyboard	$1265
System Unit, 48 K-byte RAM, keyboard, single floppy-disk drive, disk-drive adapter	2235
Monochrome video display	345
Combination monochrome-display adapter and printer adapter	335
Color-graphics-monitor adapter	300
16 K-byte memory-expansion kit	90
32 K-byte memory-expansion kit	325
64 K-byte memory-expansion kit	540
Disk-drive adapter	220
Disk drive (5-inch floppy disks)	570
Asynchronous communications adapter	150
Game-control adapter	55
Keyboard	270
Printer	755
Printer adapter	150
Printer cable	55
Printer stand	55

the 16 available colors, while colors 1 through 3 are chosen from two available color sets. (In the text mode, COLOR sets the foreground, background, and border colors.)

- LINE (all BASICs) allows you to draw a line, outline a box, or fill in a box in whatever colors are available.
- SCREEN (all BASICs): "SCREEN *n*" is used to choose text mode ($n=0$), IBM medium-resolution graphics ($n=1$), or IBM high-resolution graphics ($n=2$). In text mode, SCREEN can also generate a black-and-white text image and choose which of several pages are to be independently viewed and written to.
- GET and PUT (disk BASIC): GET allows you to save the graphic image within a specified rectangular area into a BASIC array. PUT allows the stored image to be redrawn at any point on the screen, in one of five ways: PSET (replace the existing image with the stored image), PRESET (replace with the inverse of the stored image), XOR (exclusive-or the existing and stored images), OR (add the stored image to the existing image), AND (selectively restore the stored image, using the existing image as a logical mask).
- CIRCLE (advanced BASIC) allows you to draw a circle or ellipse with a given center, color, radius, and eccentricity. In addition, an arc (partial circle) may be drawn (the begin and end points of the arc can be specified); optionally, either or both endpoints can be connected to the center point. (This last feature exists but is not documented in the description of the CIRCLE command in the IBM BASIC manual. The end points must have an absolute value less than or equal to 2π. The same arc is drawn regardless of the sign of the end point; if the end point is negative, however, it is connected to the center point.)
- PAINT (advanced BASIC) lets you specify a starting point, a color, and a boundary color. PAINT then starts painting the screen the given color from the starting point outward until it reaches the boundary color.

Statement	Description
BEEP	beep the internal speaker
CALL	call machine-language subroutine from BASIC
CHAIN	execute a new program, retaining values of program variables
CIRCLE	draw circle, ellipse, arc, or pie-shaped wedge
CLOSE	close data file
CLS	clear video screen
COLOR	set foreground and background colors
COM...ON/OFF/STOP	enable/disable activation of ON COM...GOSUB
COMMON	mechanism to pass variables to CHAINed program
DATA	standard DATA statement
DATE$	set date
DEF FN...	user-defined function
DEF SEG	define current segment of memory
DEF USR	define starting address for USR call
DIM	dimension arrays
DRAW	draw a graphics command string
END	end program
ERASE	reclaim memory from arrays no longer being used
ERROR	simulate a given error condition
FIELD	defines fields within a file buffer
FOR...TO...STEP	standard FOR loop
GET (disk I/O)	get a record from a random-access file
GET (graphics)	put graphics information from screen to array
GOSUB	execute subroutine
GOTO	continue execution at specified line
IF...THEN...ELSE	standard IF statement
INPUT	read data from keyboard or data file
KEY ON/OFF	turn display of function keys on 25th line on or off
KEY	redefine one of ten function keys
KEY...ON/OFF	enable/disable activation of ON KEY GOSUB
LET	standard assignment statement (e.g., LET A= 3)
LINE	draw line, box, or solid box on graphics screen
LINE INPUT	read an entire line from keyboard or data file
LOCATE	position cursor
LPRINT	print to printer
LPRINT USING	print to printer according to a given format

Table 4b: *A summary of IBM BASIC statements.*

Subroutine Interrupts in BASIC

A very unusual and useful feature of the IBM BASIC is its ability to stop execution of a BASIC program to service an external interrupt before continuing the BASIC program. What makes this interrupt capability different from that of any other microcomputer is that the interrupt routine is *not* a machine-language program but a BASIC subroutine within the BASIC program being used. The interrupting events are: a keypress from any of the four cursor-movement keys or the ten function keys, incoming information from the IBM Asynchronous Communications Adapter card, activation of the light pen, or a keypress from a joystick trigger button.

The form of these statements is

ON *event* GOSUB *line*

where *event* is COM*n*, KEY(*n*), PEN, or STRIG(*n*) (joystick trigger), and *line* is the beginning line number of a BASIC subroutine. Another condition for the execution of the subroutine is for the event to be *activated*, which is done by an

Statement	Description
LSET	left-justify a string within a field
MID$	substring substitution statement
MOTOR	control cassette recorder motor
NEXT	ends FOR loop
ON COM/KEY/PEN/ STRIG...GOSUB	interrupt by given event to BASIC subroutine (see text for details)
ON ERROR GOTO	enable error-trapping routine
ON...GOSUB	standard computed GOSUB statement
ON...GOTO	standard computed GOTO statement
OPEN	open a disk or communications file
OPTION BASE	allows array subscripts to start at 0 or 1
OUT	output a byte to a port
PAINT	fill an area of the graphics screen with color
PEN ON/OFF/STOP	enable/disable activation of ON PEN GOSUB
POKE	put a specified value into a byte
PRINT	print to video display or file
PRINT USING	print to video display or file according to a given format
PRESET	plot a graphics point in the background color
PSET	plot a graphics point in a given color
PUT (disk I/O)	write a record to a random-access file
PUT (graphics)	draw a stored image onto the graphics screen
RANDOMIZE	start a new pseudo-random number sequence
READ	read information from DATA statements
REM	standard remark statement
RESTORE	reset pointer to DATA statements
RESUME	return from an error routine
RETURN	return from a subroutine
RSET	right-justify a string within a field
SCREEN	choose text or graphics screen for video display
SOUND	generate sound from the speaker
STOP	stop program execution
STRIG ON/OFF	enable/disable joystick button
STRIG...ON/OFF	enable/disable activation of ON STRIG...GOSUB
SWAP	exchange the values of two variables
TIME$	set time
WAIT	standard Microsoft WAIT statement
WEND	end WHILE loop
WHILE	program loop that executes as long as a given condition is true
WRITE	output data to video screen or file

associated set of BASIC commands. For example, if the statement

PEN ON

is executed and the ON PEN statement exists in the program, the subroutine will be executed the next time the light pen is used. If

PEN OFF

is executed, the use of the light pen will *not* cause the subroutine to be executed. If the statement

PEN STOP

is executed, using the light pen causes the subroutine to be executed as soon as a PEN ON statement is executed. Similar statements are available for COM*n* and KEY(*n*), but not for STRIG(*n*).

With these statements, a program can immediately respond to certain events that may or may not happen.

DRAW and PLAY

One of the most innovative features of the IBM BASIC is the use of predefined BASIC strings to specify a series of draw commands (for DRAW) or note-playing commands (for PLAY). These strings have their origins in the Apple II shape tables; but, by extending the syntax and allowing the "table" to take the form of standard strings that can be manipulated by the BASIC program itself, the concept has been greatly improved.

Table 5 lists the commands available within a DRAW string. To draw a long, narrow rectangle, we simply define

A$="R40;U10;L40;D10"

This draws 40 units to the right, 10 up, 40 to the left, and 10 down. If we execute the statement

DRAW A$

the rectangle will be drawn from wherever the graphics cursor happens to be at that time.

One of the most powerful features of this graphics-command language is the ability to call one string from another. For example, to rotate this box 90 degrees counterclockwise, we could simply command

DRAW "A1;XA$;"

(A1 calls for a 90-degree rotation, and XA$; executes string A$.) In addition, any command can take its argument from an existing variable, so that if we say

DRAW "A=I;XA$;"

the image will be rotated an I-multiple of 90 degrees before being drawn. Note the presence of the semicolon at the end of the X command; this is necessary for the command to work.

Photo 11 shows the listing and the run of a program that first draws the string A$, then draws it in all its rotations. The PSET statement simply moves the graphics cursor to a new location before drawing.

The PLAY statement works similarly to the DRAW statement, but with a different set of commands. For example, the statement

PLAY "C1;D#2;G-4"

Function	Description
ABS	absolute value
ASC	convert ASCII character to its numeric value
ATN	arctangent
CDBL	convert to double-precision number
CHR$	converts number to equivalent ASCII character
CINT	round to nearest integer
COS	cosine
CSNG	convert to single-precision number
CSRLIN	returns row number of current cursor position
CVD	convert string to double-precision number
CVI	convert string to integer
CVS	convert string to single-precision number
EOF	logical test for end-of-file condition
ERL	line number of an error that has just occurred
ERR	error code of an error that has just occurred
EXP	exponential function, base e
FIX	truncate to an integer value
FRE	amount of workspace left unused
HEX$	converts number to a string containing a hexadecimal number equivalent to the original number
INKEY$	read a character from the keyboard
INP	read 8-bit value from port
INPUT$	read characters from a file
INSTR	find substring within a given string
INT	largest integer less than or equal to argument
LEFT$	take substring starting with first character
LEN	length of a string
LOF	amount of space in a file
LOG	natural logarithm
LPOS	carriage position of printer
MID$	extract a substring from a given string
MKD$	convert a double-precision number to a string
MKI$	convert an integer to a string
MKS$	convert a single-precision number to a string
OCT$	converts number to a string containing an octal number equivalent to the original number
PEEK	read value of byte in memory
PEN	read light pen
POINT	get color number point on graphics screen
POS	cursor column position
RIGHT$	take substring ending with last character
RND	random number
SCREEN	character or color at given position (text mode only)
SGN	sign of argument
SIN	sine
SPACE$	creates a string full of spaces
SPC	prints spaces
SQR	square root
STICK	get coordinates of joystick
STR$	converts a number to a string
STRING$	creates a string filled with one ASCII constant
TAB	spaces over to an absolute print position
TAN	tangent
USR	call machine-language subroutine
VAL	converts string to numeric value
VARPTR	get address of variable; or get file control block of a file

Table 4c: *A summary of IBM BASIC functions.*

plays a whole C note, a half D-sharp note, and a quarter G-flat note. Many variations are possible, including octave and tempo change, note length, pauses, substring execution, and variable command parameters. In addition, a sequence of up to 32 notes can be stored in a buffer and played in background—that is, the BASIC program continues to execute, and the music is played independently by the buffer.

Communications Files

If the IBM Asynchronous Communications Adapter is installed in the IBM Personal Computer, a BASIC program can interact with a remote device as if it were a simple disk file. GET and PUT can be used, as well as the I/O statements INPUT #*f*, LINE INPUT #*f*, INPUT$, PRINT #*f*, PRINT #*f* USING, and WRITE#*f*. In all these cases, *f* is a file specification that has a device name of COM1: or COM2:. Thus more people can write programs that use remote devices, because BASIC automatically takes care of most of the communication details.

The IBM DOS

The IBM disk operating system (DOS) (written by Microsoft with help from Seattle Computer Products) bears a superficial resemblance to Digital Research's CP/M operating system. (For example, the IBM DOS gives the prompt "A>".) However, the IBM DOS is a scaled-down version of Microsoft's 16-bit Unix lookalike, the Xenix operating system. In addition, the commands are better worded than in CP/M. For example, the cryptic

```
PIP B:NEWFILE1=A:MYFILE1
```

of CP/M is replaced by

```
COPY A:MYFILE1 B:NEWFILE1
```

which copies MYFILE1 from drive A to drive B, where it will be named NEWFILE1. Other commands include ERASE (to delete a file), FORMAT (to format a floppy disk), RENAME (to rename a file), DIR (to list the directory of a disk), DATE (to set the

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Micropro Int'l Corp.	**WORDMASTER, WORDSTAR**
Microsoft	**BASIC, FORTRAN, COBOL, PASCAL**
Midwest Micro-Tek, Inc.	**BASIC-compiler**
Ryan-McFarland Corp.	**RM/COBOL**
The Soft Warehouse	**LISP compiler, MuMATH**
Sorcim Corp.	**PASCAL/M, TRANS-86**
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date), and TIME (to set the system clock).

The IBM DOS floppy disk contains BASIC and BASICA (the disk and advanced BASICs), as well as some disk utility programs. LINK combines object files (created by an assembler or compiler) into a form that can be executed. DEBUG allows you to examine both memory and disk files and debug a machine-language program. Photo 12 shows the DEBUG program tracing the execution of a program and displaying all the 8088 registers.

Another feature of the IBM DOS is the file AUTOEXEC.BAT. If a disk file with this name is present on the disk used to start the system, it is automatically executed as soon as the IBM microcomputer is working. The ".BAT" suffix marks it as a *batch file,* which is a text file of statements that are executed sequentially as if they had been typed in from the keyboard in a manner similar to a CP/M submit (.SUB) file or an Apple II EXEC file. Because the AUTOEXEC.BAT file is a batch file, it can perform many operations before giving control to the user.

The IBM BIOS

All software interacts with the hardware of the IBM microcomputer through part of the DOS called the BIOS (basic input/output system). In the IBM microcomputer, all calls to the BIOS are done as 8088 software interrupts. There are 256 such interrupts available on the 8088, of which 193 are used by DOS and BASIC.

BASIC uses many of the reserved interrupts to interact with the rest of the machine. By using the interrupts as "hooks" to the actual routines, which are stored in high memory (see table 6), the system can add new devices and change the behavior of existing ones by writing new routines in user memory and changing the appropriate interrupt vectors to point to the new code. In fact, this is how the disk and advanced BASICs add features to the cassette BASIC in ROM. In the same way, a programmer with sufficient skill can extend the behavior of the IBM Personal Computer by modifying the BIOS and placing the commands needed to patch them into the system into an AUTOEXEC.BAT file; the batch file should end with a program that executes an INT 27 interrupt, which allows the code to remain in the system until it is turned off. Much technical information (including an 80-page fully documented listing of the IBM BIOS) is included in the manual *Technical Reference.*

One interesting use of the IBM BIOS relates to the IBM keyboard. The keyboard, which contains an Intel 8048 microprocessor, does not deliver ASCII codes to the System Unit. Instead, it delivers two *scan codes* per keypress: one when the key is pressed, and a different one when the key is released. The IBM BIOS decodes the scan codes into an extended ASCII code that can return 256 one-byte codes and several two-byte codes for each keypress.

Command	Description
U*n*	move up *n* steps
D*n*	move down *n* steps
L*n*	move left *n* steps
R*n*	move right *n* steps
E*n*	move diagonally up and to the right *n* steps
F*n*	move diagonally down and to the right *n* steps
G*n*	move diagonally down and to the left *n* steps
H*n*	move diagonally up and to the left *n* steps
M*x,y*	move to point (*x,y*) or (if in relative mode) move (*x,y*) units from current position; plot a point
B*x,y*	same as M, but no point is plotted
N*x,y*	same as M, but return to original location when finished
A*n*	set angle as a multiple of 90 degrees (*n* = 0 through 3)
C*n*	set current color to *n*
S*n*	set scale factor (step size)
X*string$*;	execute substring *string$*

Table 5: *Commands for the DRAW statement.*

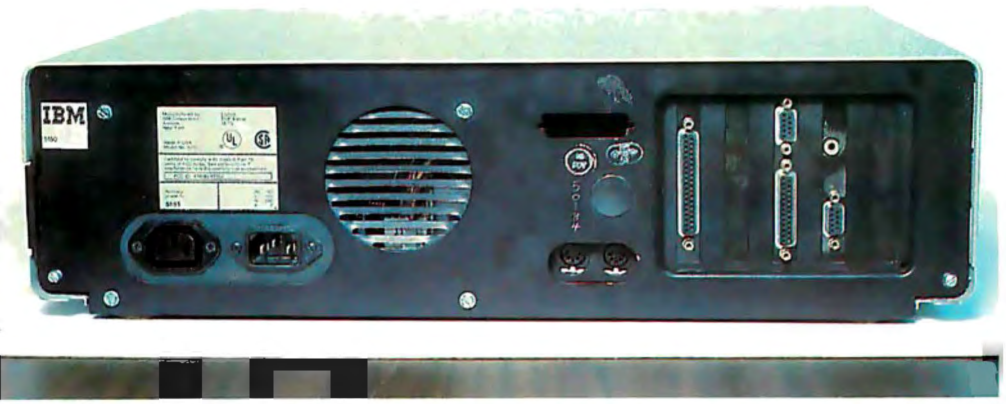

Photo 10: *The back panel of the IBM Personal Computer. See the text for a description of the plugs and sockets.*

How Fast Is IBM BASIC?

Surprisingly, IBM BASIC is not much faster than its 8-bit counterparts. Table 7 compares the execution times of five BASIC programs on several popular microcomputers; the programs themselves are in listing 1. The first four benchmarks test an empty do-loop, division, subroutine jumps, and the MID$ string function. The fifth test is a slightly modified version of Jim Gilbreath's Sieve of Eratosthenes benchmark program (see "A High-Level Language Benchmark," September 1981 BYTE, page


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180); note that the algorithm accesses lots of memory but uses only addition and subtraction.

The results of these comparisons are not encouraging. For example, IBM BASIC is somewhat faster than Applesoft, but the difference is modest, and Applesoft is one of the slower microcomputer BASICs. (All the BASICs tested are versions of Microsoft BASIC.) A comparison of IBM BASIC to Microsoft MBASIC 4.51 running on a 4-MHz Z80-based machine shows MBASIC to be faster in everything but division; this last makes sense in that the 8088 microprocessor has a hardware divide instruction, which accounts for its better performance in the division benchmark. Still, it seems that IBM BASIC does not have a definite superiority over its 8-bit counterparts.

Although I hesitate to draw conclusions about the IBM microcomputer's performance in disk-based or machine-language programs, it is obvious that the IBM microcomputer does not gain a speed advantage from its memory access—the 8088 micro-

Address (in Hexadecimal)	Location	Type	Function
00000	on System Board	RAM	BIOS interrupt vectors
00080	"	"	BIOS available interrupt vectors
00400	"	"	BIOS data area
00500	"	"	workspace memory
10000 (decimal 64 K)	on memory card	"	workspace memory
40000 (256 K)	not available now; reserved for future expansion	"	proposed workspace memory
A0000 (640 K)	?	?	reserved
A4000 (656 K)	on video boards	RAM	reserved for all forms of video display (note 1)
C0000 (786 K)	?	?	memory expansion area
F0000 (960 K)	?	?	reserved
F4000 (976 K)	on System Board	ROM/PROM	8 K-byte slot available for user programs
F6000 (984 K)	"	ROM	40 K-byte BASIC in ROM
FE000 (1016 K)	"	"	BIOS code in ROM

Note 1: Not all this space is currently in use. The memory for the monochrome adapter card starts at hexadecimal B0000 (704 K bytes), and the memory for the color/graphics card starts at hexadecimal B8000 (736 K bytes).

Table 6: *Memory map of the IBM Personal Computer.*

	IBM	Applesoft		4 MHz Z80 MBASIC 4.51		Radio Shack TRS-80 Model II	
Benchmark	time	time	ratio to IBM	time	ratio to IBM	time	ratio to IBM
empty do-loop	6.43	6.66	1.04	5.81	0.904	7.98	1.24
division	23.8	29.0	1.22	24.9	1.05	19.4	0.815
subroutine jump	12.4	13.9	1.12	9.4	0.758	17.1	1.38
MID$ (substring)	23.0	32.3	1.40	18.6	0.809	24.8	1.08
prime number program	190	241	1.27	151	0.795	189	0.995

Table 7: *Benchmark results for the IBM Personal Computer against several 8-bit microcomputers: an Apple II Plus running Applesoft BASIC, a 4 MHz Z80 microcomputer running MBASIC 4.51, and a Radio Shack TRS-80 Model II running Model II BASIC. All times (given in seconds) and ratios are valid to three significant digits. See listing 1 for the actual benchmark programs.*

Listing 1: *BASIC benchmark programs used in table 7. Listing 1a tests an empty do-loop; the two constants are included to allow the isolation of the features being tested in listings 1b and 1c. Listing 1b tests the division operation. Listing 1c tests a subroutine call-and-return sequence. Listing 1d tests the MID$ (substring extraction) operation. Listing 1e is the Sieve of Eratosthenes algorithm to generate prime numbers; it is used as a composite benchmark of several BASIC features working together in a short, but nontrivial, program.*

1a

```
60 A=2.71828
80 B=3.14159
100 FOR I=1 TO 5000
320 NEXT I
```

1b

```
60 A=2.71828
80 B=3.14159
100 FOR I=1 TO 5000
120 C=A/B
320 NEXT I
```

1c

```
60 A=2.71828
80 B=3.14159
100 FOR I=1 TO 5000
120 GOSUB 1000
320 NEXT I
340 END
1000 RETURN
```

1d

```
80 A$="abcdefghijklm"
100 FOR I=1 TO 5000
120 B$=MID$(A$,6,6)
320 NEXT I
```

1e

```
1 SIZE=7000
2 DIM FLAGS(7001)
3 PRINT "only 1 iteration"
5 COUNT=0
6 FOR I=1 TO SIZE
7 FLAGS(I)=1
8 NEXT I
9 FOR I=0 TO SIZE
10 IF FLAGS(I)=0 THEN 18
11 PRIME=I+I+3
12 K=I+PRIME
13 IF K>SIZE THEN 17
14 FLAGS(K)=0
15 K=K+PRIME
16 GOTO 13
17 COUNT=COUNT+1
18 NEXT I
19 PRINT COUNT," primes"
```

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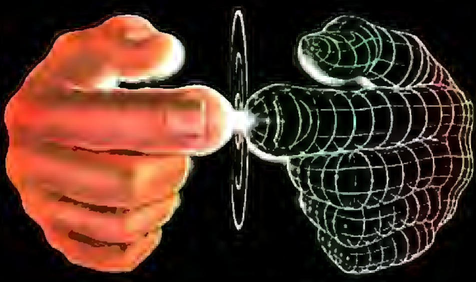

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*SOME MICROCOMPUTERS MAY REQUIRE A DIFFERENT INTERFACE. CONSULT YOUR DEALER processor has to get memory one byte at a time, like the 8-bit 6502 and Z80. Still, this does not fully account for the IBM microcomputer's modest performance. Perhaps IBM's BASIC has only been translated from its 8-bit predecessors and not optimized for the 8088's instruction set.

Documentation

IBM uses the slogan "The IBM of Personal Computers" in one of its advertisements. The manuals that accompany the IBM microcomputer and various pieces of software could likewise be called "The IBM of Documentation." They will set the standard for all microcomputer documentation in the future. Not only are they well packaged, well organized, and easy to understand, but they are also *complete*. With the inclusion of the manual *Technical Reference*, the IBM Personal Computer is as well documented as any existing microcomputer, and the documentation is available much earlier in the life of this machine than it has been for other machines.

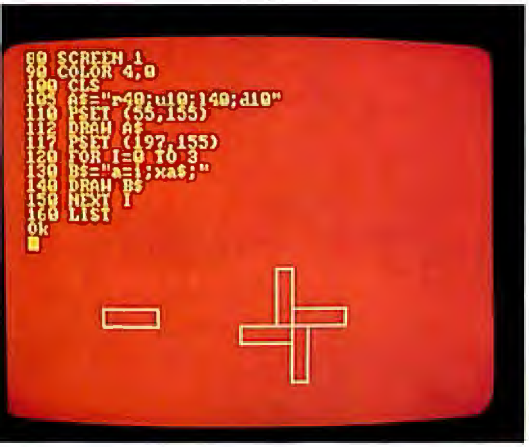

Photo 11: *A demonstration of the DRAW command. See the text for details.*

Photo 12: *An example of the DEBUG program at work.*

Each manual is in a hardcover D-ring binder with its own slip cover. The pages are 14 by 21.6 cm (5.5 by 8.5 inches), and the binder is built so that the opened book lies flat. Included with the minimal configuration IBM microcomputer are manuals titled *Guide to Operations* and *BASIC*. A separate boxed manual is given with each software package; some IBM Personal Computer products have softcover documentation booklets.

Guide to Operations explains the capabilities of the IBM Personal Computer system and provides information to be used in the setup and initial operation of the microcomputer. A 145-page section called "Operations" describes the IBM keyboard layout and usage, the IBM 80 CPS Matrix Printer, the IBM DOS, and selected information on IBM BASIC. Other sections tell you what to do if the IBM microcomputer doesn't work, what additional peripherals are available for the system, and how to prepare the system to physically move it to another location. The manual is written in a friendly, tutorial manner and includes the basic information that most manuals take for granted (i.e., how to turn the machine on, how to start BASIC).

BASIC is 406 pages long and contains a 258-page section that fully describes each BASIC command, function, statement, and variable. Each BASIC keyword is documented under several headings: format (the syntax of the keyword), versions (the version or versions of IBM BASIC under which the keyword is available), remarks (a commentary that further explains the use of the keyword), and an example. Other sections describe the use of the BASIC Program Editor, floppy-disk I/O, communications files, and other topics.

The Reference Manual

The manual *Technical Reference* deserves special recognition simply for its existence. It is 372 pages long and is in three sections, plus appendixes; its price is a modest $36. Section 1 gives a short overview of the IBM Personal Computer System and some of its internal workings. Section 2, which is 147 pages long, gives a functional specification for every piece of hardware in the IBM Personal Computer product line. This includes highly detailed specifications of the operation of the hardware, pinouts for peripheral connectors, and connection diagrams showing how to interface IBM peripheral cards with non-IBM devices. Section 3 describes the IBM BIOS. Five appendixes give additional information, including a complete, commented listing of the IBM BIOS and schematics for all hardware in the system.

I'm sure that adventurous microcomputer enthusiasts will discover many more things about the IBM microcomputer as they buy and use the machine. But *Technical Reference* gives us a tremendous amount of information from the start. Most computer enthusiasts will want to have a copy of this book.

Sales and Service

Many companies are trying to become authorized IBM dealers; at the time of this writing, all Computerland stores are authorized dealers, and Sears Roebuck and Company has announced plans to sell the IBM Personal Computer through its Sears Business Systems Centers. IBM itself will sell its microcomputer through the IBM Product Centers in Baltimore, Philadelphia, and San Francisco. Since a potential dealer has to qualify as an authorized repair center before a dealership will be awarded, service will always be available from the dealer that sold you the unit.

IBM is also offering warranty extensions to increase the 90-day warranty that comes with the machine to one year, as well as annual maintenance contracts. The prices are reasonable; for example, the prices for a 48 K-byte system with one floppy disk and the monochrome display are $154 for the warranty extension

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[2] TRS-80 is a registered trademark of Radio Shack, a Tandy Company

and $196 for the annual maintenance contract. On the other hand, the prices for the IBM 80 CPS Matrix Printer (which has a lot of moving parts) are $141 and $179, respectively.

Prices may become a source of potential bad feelings between you and the dealer. The prices quoted in the "At a Glance" textbox are suggested retail prices that are guaranteed to be in effect *only* at the three IBM Product Centers, listed above. Dealer prices may vary from this somewhat—expect a variation between $10 and $100 on most products, depending on their suggested price. However, at the time of this writing, one authorized IBM dealer is selling the Peachtree Software business packages (General Ledger, Accounts Receivable, and Accounts Payable) at $995 each, a full $400 above the IBM suggested price of $595. Since the IBM suggested price includes a sufficient profit margin for most products, I think this price (which I confirmed with the dealer) is exorbitant.

Advanced BASIC adds event trapping, some advanced graphics commands, and an advanced music-playing command.

The moral is to shop around for the best prices, if you can. However, this may be difficult for two reasons. First, IBM is probably going to authorize only one dealer per geographic area, at least initially. Second, the IBM microcomputer product line is probably not going to be available by mail for quite some time. Another problem with buying software from a dealer in a distant city is that the dealer is going to be responsible for software support. Still, for $400, I would be tempted to buy my software in another city and make some long-distance calls when I needed software support.

Other Vendors

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sole supplier of both hardware and software. But potential hardware and software vendors have wasted no time in providing products for what they feel will be a very popular microcomputer. In particular, Lifeboat Associates announced last October that it is "making available most of its existing applications programs to serve users of IBM's new 16-bit Personal Computer." When this is accomplished, it will do a lot to ease the shortage of business and applications software that currently exists for the IBM Personal Computer.

(In a related development, Lifeboat also announced that it will be selling all its 16-bit software for the SB-86 operating system, which is its name for the IBM disk operating system. The fact that IBM, Microsoft, and Lifeboat have put their names behind this 16-bit operating system poses a serious threat to Digital Research's prospects of dominating the 16-bit market with its new CP/M-86 8086 operating system, as it has the 8-bit arena with its popular CP/M 8080 operating system.)

As for hardware, several gaps will, for the moment, be filled by outside vendors. IBM does not currently supply a high-quality RGB color monitor, a letter-quality printer, or any of the special input devices provided for in the system (joystick, light pen, paddles). IBM's position is that the potential demand for these products will cause third-party vendors to independently market them. (In the next section, I will discuss some problems with this philosophy.) In addition, the expansion slots provide the opportunity to interface the IBM microcomputer with many outside devices. Given a reasonable period of time, plenty of hardware and software will probably be developed for the IBM Personal Computer.

One other item of interest is the announcement of a new magazine called *PC: The Independent Guide to the IBM Personal Computer*. It is published by David Bunell, of Software Communications, Inc., 44 Montgomery St., San Francisco, CA 94104; subscriptions are $12 for 12 issues. It should be of great interest to owners of the IBM Personal Computer.

Current Weaknesses

The IBM Personal Computer is a very good machine, but it does have some shortcomings. This is no reflection on IBM's ability to design a microcomputer; rather, it is a reflection of the trade-offs between capability and cost that had to be made to make the machine competitive in the existing market.

The most serious weakness of the IBM Personal Computer is the small number of expansion slots available for future use. Note that I say "for future use"; one slot is taken up by a video adapter card (or two if you want both kinds of display), and another is taken up for each of the following devices: the 5¼-inch Diskette Adapter card (if you want a floppy disk), the Asynchronous Communications Adapter card (if you want an RS-232C port), the Printer Adapter card (if you have the color/graphics video card and want a parallel printer), and the Game Control Adapter card (if you want joysticks or game paddles). Since you need an empty expansion slot for each 64 K bytes of memory above the *first* 64 K bytes, it is obvious that you cannot put everything into the IBM microcomputer that you might want to. The most frequently encountered limitation is the amount of memory you can have in the microcomputer; if you want a floppy disk and the RS-232C card, you can have only (!) 192 K bytes of memory—all five slots are filled. With a moment's reflection, you will see that the expansion slots in the IBM Personal Computer will fill rather quickly.

At the moment, the IBM Personal Computer system is weak with respect to word processing. First, IBM does not market a letter-quality printer. This means that, if you want to do word processing on the IBM microcomputer, you have to trust that your IBM dealer will also sell

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Parity checking*

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9 x 9 character matrix*

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you a letter-quality printer and cable that will work properly with your software. This problem of compatibility has been very common in the microcomputer industry to date. It is surprising that IBM, which has worked so hard in some other areas to avoid this problem, has literally left it to chance here.

Of course, the explanation of "limited resources" can be given here, too. That is, if IBM had waited until it had *everything* lined up, the product would not have been introduced as early as it has been. Still, the criticism stands that, by not providing a full product line, *the IBM Personal Computer system, through no fault of its own, may fall prey to hardware and software incompatibility,* thus creating still more disappointed microcomputer users.

Another weakness of the IBM Personal Computer as a word processor is the lack of versatile word-processing software to drive the machine. The only word processor available at the time of this writing is Information Unlimited's EasyWriter. I was given a chance to work with the EasyWriter word processor on the IBM microcomputer, and I found a few things I didn't like about it. In general, the software didn't seem to be of the same caliber as, say, VisiCalc or the Peachtree business packages. Specifically, at times the software left me not knowing exactly what to do next, and I found the scrolling—both up *and* down—to be slow. (Scrolling down is understandably slow because the entire screen has to be rewritten, but scrolling up is usually fast, whether it be on a memory-mapped video display or a terminal. On the IBM EasyWriter, the scrolling is as slow going up as it is going down.) I have used the Apple II version of EasyWriter extensively, and my opinion of it is the same as for the IBM version: it is a good piece of software for the money, but it isn't as versatile as some applications require.

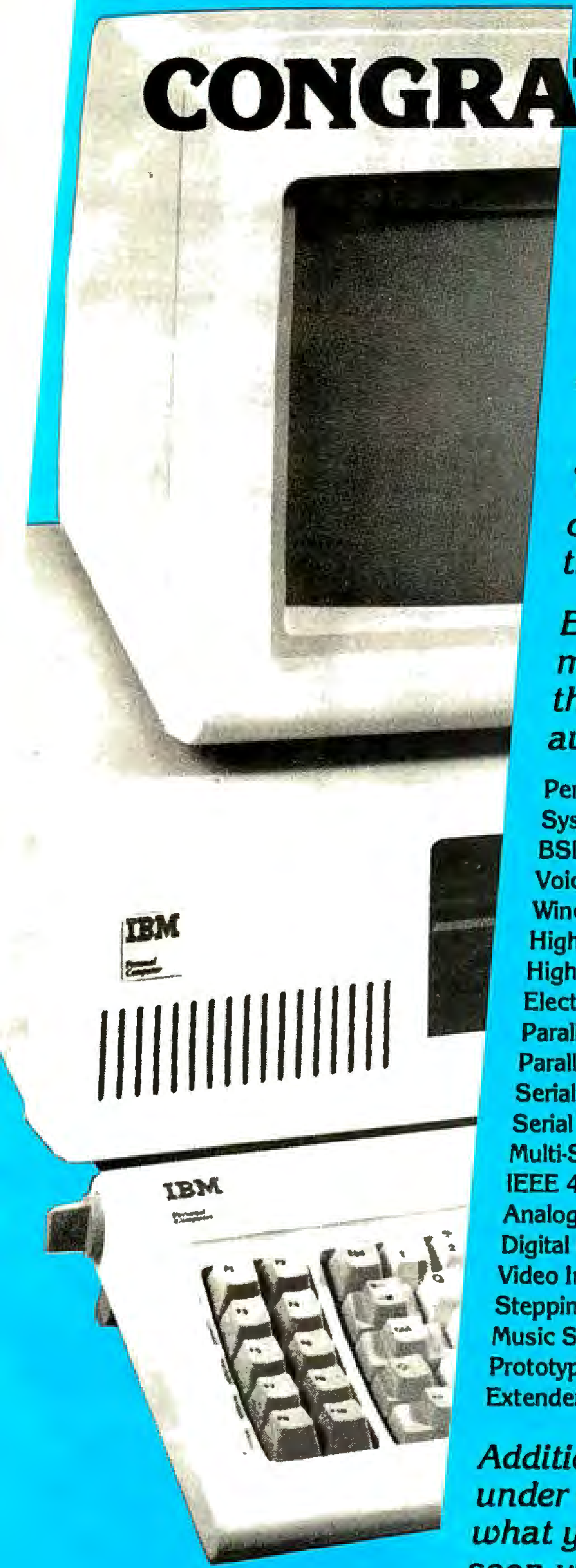
I'm sure that Magic Wand, WordStar, or something similar will be available very soon for the IBM microcomputer, but EasyWriter is the only choice for the moment. My advice is: if you have an IBM Personal Computer, use the EasyWriter package a lot before you buy it. If you are looking for a system to be used primarily for word processing and you can't afford to wait for better software, I suggest that you look at other existing systems, such as the Radio Shack TRS-80 Model II or the Xerox 820. The IBM system, as it currently stands, does not compare favorably with these other systems.

Another limitation of the IBM Personal Computer is that, even though up to 256 K bytes of memory are available, the extended Microsoft BASIC cannot access more than a 64 K-byte workspace (I assume this includes both program and data), even though the IBM Pascal Compiler (also by Microsoft) and other proposed system software are said to be able to access all the workspace memory in the machine. Sixty-four K bytes seems to be so much memory, especially since we are used to program, data, *and* the BASIC interpreter fitting into 64 K bytes. Still, it's unfortunate that all that extra memory (which is one of the main reasons for buying the machine) can't be used by BASIC, the computer language that will probably most often be used on the machine.

Another weakness that must be mentioned is an extension of one previously discussed: the IBM dealer will have to supply certain useful or even vital components of a complete IBM microcomputer system. IBM says it has no interest in manufacturing color monitors, letter-quality printers, joysticks, or light pens, nor can IBM supply you with the cables that will have to be made to connect these devices to the IBM microcomputer. In addition, if you want to connect your IBM microcomputer to a standard color TV (which is what most people will do), you will have to rely again on the judgment of your IBM dealer for the correct cable and RF modulator. I'm sure that in most cases no serious problems will arise, but by not making the entire product line itself, IBM has lost its guarantee of total system compatibility.

As someone not unacquainted with the programming of games, I found a

CONGRATULATIONS IBM!



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Serial High Speed Input/Output Interface
Multi-System Printer Sharing Facility
IEEE 488 Interface
Analog to Digital Converter-8, 12, 14, 16 Bit
Digital to Analog Converter-8 and 12 Bit
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few inadequacies with the graphics commands of the extended Microsoft BASIC. Although the graphics-definition language is excellent, shapes are allowed to rotate only in 90-degree increments. In addition, the only way I found to detect the collision of a drawn shape with the contents of the screen is through a POINT function that gives the color number of a given point on the screen. Although this *can*, with some effort, be used for that purpose, it falls far short of the methods of detecting collisions available on the Apple II and the Atari 400/800 computers. Perhaps some enthusiastic programmer will find a memory location that indicates whether or not a drawn shape has collided with another image on the screen. In any case, these are small criticisms of a machine that does so many things so well.

Speculations

One interesting thing about IBM is that it refuses to acknowledge the existence of any product that is not ready to be put on dealers' shelves tomorrow. Although this is frustrating at times, it is a refreshing change from some companies' practice of announcing a product even before its design is finished. Here are some speculations about future IBM Personal Computer products. The first two are almost assured, while the rest follow in increasing degree of uncertainty.

- *Two more disk drives.* Although, at the time of this writing, IBM maintains that only two disk drives are available for the IBM microcomputer, *Technical Reference* indicates in several places that provision is made for two external disk drives to be connected to the 5¼-inch Diskette Drive Adapter via the DB-37 connector on the back of the adapter card. (See the leftmost plug in the expansion slot area in photo 10.)
- *An 8086/8088 macro assembler.* The *Technical Reference* bibliography lists a manual for the *IBM Personal Computer Macro Assembler.* It may be available by the time you read this article.

Now we start with the speculations:

- *SofTech Microsystems' UCSD p-System.* IBM announced that this operating system would be available for the IBM Personal Computer; this would make UCSD Pascal, FORTRAN, and BASIC available, and it would allow the IBM microcomputer to run the same programs as other UCSD systems. However, IBM would not give me any availability dates.
- *A typing tutorial program.* This was mentioned once in the front of the IBM *Guide to Operations*—but then, so were joysticks and RF modulators. Microsoft may adapt its Typing Tutor for the IBM Personal Computer.
- *An official letter-quality printer and a major-league word processor.* IBM may have plans to do this, or it may be relying on manufacturers' eagerness to expand their potential market. Someone will probably do it, but it may not be IBM.
- *An "expansion box" to increase the number of peripheral cards that can be placed in the computer at one time.* This would resolve a design limitation of the IBM Personal Computer as it now exists.
- *A 128 K-byte (or more) memory board.* As the 64 K-bit memory ICs decrease in price and become more available, IBM may market expansion boards that hold more than their current 64 K-byte limit. This would free up one or two expansion slots, but it might also allow the IBM Personal Computer to hold more than 256 K bytes.
- *A database management system.* This, like many other business packages, is needed to strengthen the position of the IBM microcomputer in the business area.
- *An official RGB color monitor.* I don't think IBM is going to go for this one, but it should. I have seen three separate IBM Personal Computers with RGB monitors. In all three cases, the monitor used did not have an input for the intensity signal and so could display only eight of the sixteen

Text continued on page 68

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Text continued from page 64:

possible colors. This is, again, a situation where IBM has surrendered the guarantee of complete compatibility by not manufacturing the product itself.

- *A Winchester hard disk* (the bigger, the better). Admittedly, this is a real guess, but it would make the IBM Personal Computer more attractive for certain business applications. The Apple III, a direct competitor to the IBM microcomputer, is now being offered with a Winchester disk. Is IBM going to ignore this?
- *Memory expansion past 256 K bytes.* It may be possible to replace the 16 K-bit 4116 dynamic memory integrated circuits with the new 64 K-bit devices, both on the main printed-circuit board and on the memory-expansion cards. If this can be done, the theoretical memory limit is the 20-bit, one-megabyte addressing limit of the 8088 microprocessor. The actual limit is somewhat less than that—a memory map in the *Technical Reference* manual (see table 6) allows room for "future expansion" of 576 K bytes, for a total of 832 K bytes.

Summary

When I look at the several inches of IBM Personal Computer manuals that fill my bookshelf, I am reminded that there is so much about this system that I have left out. Still, I have tried to talk about the most exciting and most important aspects of the system. The genius of the people who designed the IBM microcomputer is that they managed to do everything conventionally but well—the IBM Personal Computer doesn't have any startling innovations, but it also lacks the moderate-to-fatal design problems that have plagued other microcomputers.

The IBM Personal Comptuer isn't as well supported as the Radio Shack TRS-80 family or the Apple II, but then it hasn't been around very long. In two years or so, I think the IBM microcomputer will be one of the most popular and best-supported microcomputers around. This microcomputer is as close as I've ever seen to being all things to everybody. IBM should be proud of the people who designed it. ■

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Analog Interfacing in the Real World

Steve Ciarcia
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Most Circuit Cellar articles present basic concepts of digital electronics in the form of novel construction projects. Sometimes, however, I have to cover a significant subject without a disguise.

One such subject area is analog-to-digital (A/D) and digital-to-analog (D/A) conversion. It has been about three years since I last wrote an article discussing these essential processes. Judging from my mail, many new readers of BYTE are just now discovering that their computers can be connected to more than a printer and modem. With these readers in mind, I am presenting basic information on A/D and D/A conversion in addition to the usual construction project.

Meet the Real World

Many applications for computer controls exist around the home, such as energy management, security, and environmental monitoring. All these applications require measurement inputs and control outputs in quantities not easily expressed in the 0- and +5-volt (V) transistor-transistor logic (TTL) levels present in your computer.

An energy-management system, for example, may need to monitor a temperature range of 0 to 100°C with a resolution of 0.1°. The thermocouple sensing this temperature range might generate only 1 or 2 millivolts

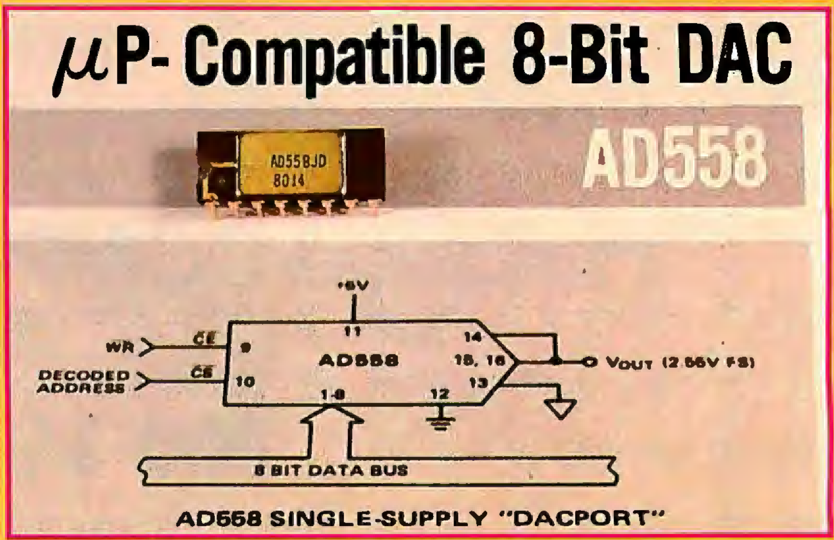
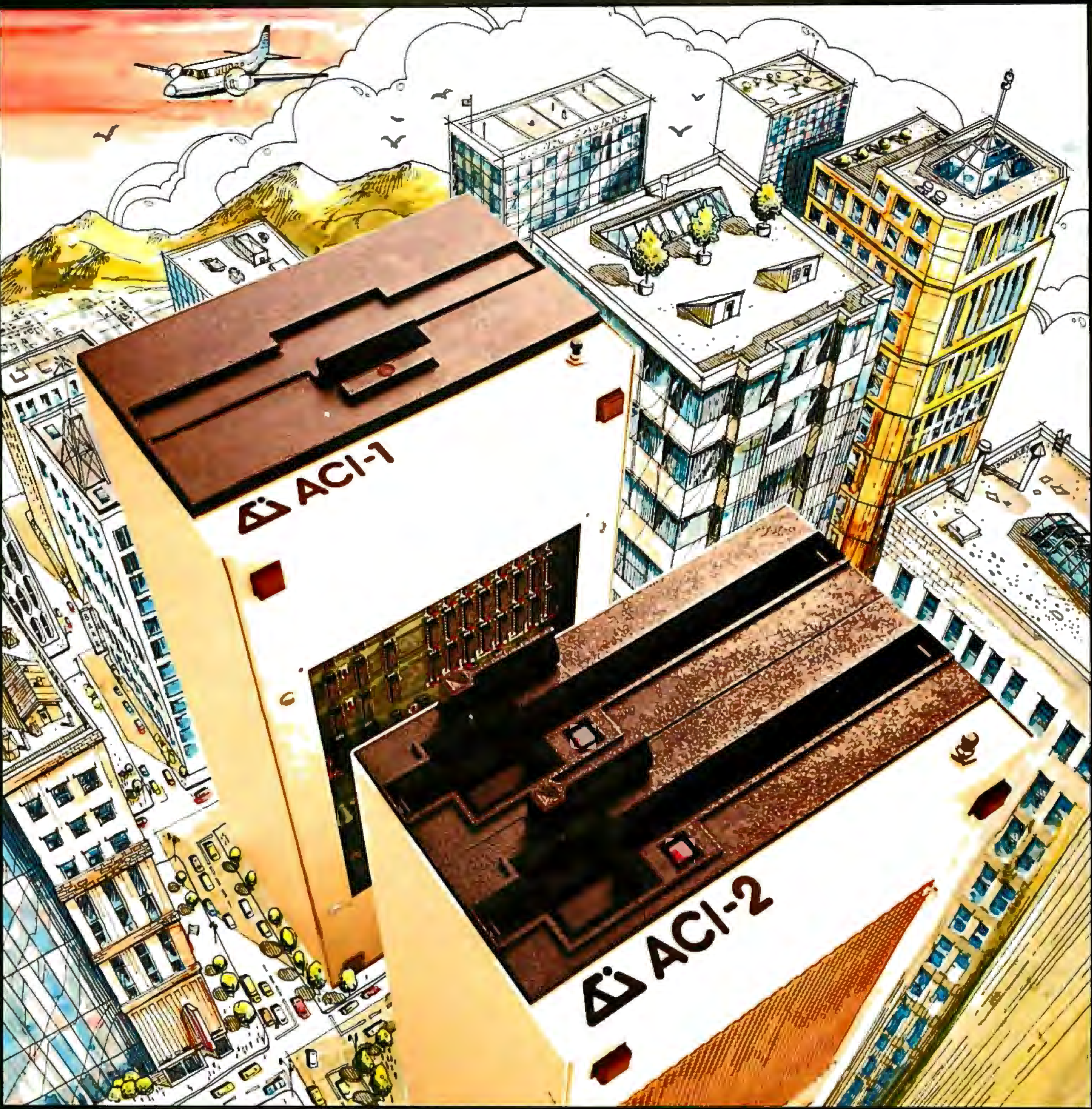


Photo 1: *Interfacing digital computer systems to their external analog environment has been made easy by the development of integrated digital-to-analog converters, such as this AD558 component from Analog Devices, Inc., POB 280, Norwood, MA 02062, (617) 935-5565.*



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(mV) per degree. A proportional-drive pump motor in the same system might require a 2.40-V set-point control input to produce the proper flow rate through the system.

Systems such as these are in the "real world," the continuous, analog environment outside the binary logic-0 and logic-1 domain of digital computers. A computer system's interaction with the real world requires some scheme for translating analog measurements to and from quantized binary equivalents.

In this article, therefore, we'll look at the design and construction of economical analog interfaces. I shall first outline the basics of digital-to-analog conversion and then go on to analog-to-digital conversion, describing the design of a low-cost circuit for each. Finally, I'll describe the characteristics and use of some of the newer D/A- and A/D-converter components on the market.

Digital-to-Analog Conversion

The digital-to-analog converter can be thought of as a digitally controlled programmable potentiometer that produces an analog output voltage. This output voltage V_O is the product of a digital signal D, a multiplier constant K (usually 1), and an analog reference voltage V_{REF}, related by the following equation:

$$V_O = KDV_{REF}$$

The binary value transmitted to the D/A converter by the computer is a binary fraction representing what portion of the full possible output voltage is to be emitted. The fraction is multiplied by a reference voltage, which can be either fixed or variable. D/A converters with variable reference voltages are often referred to as "multiplying" D/A converters, although all D/A converters can be said to multiply.

In finite binary fractions, the most significant bit (MSB) has a value of ½ (that is, 2^{-1}), the next most significant bit is ¼ (2^{-2}), and the least significant bit (LSB) is $(½)^n$ or 2^{-n}, where n is the number of bits in the binary fraction. If all the bits in the fraction are added, the sum approaches 1; the more bits in the fraction, the closer the sum is to 1. The difference between 1 and the approach to 1 is the *quantization error* of the digital system. I'll discuss this later.

Different implementations of D/A converters (and A/D converters, too) use different formats for representing the binary digital quantities. One basic difference is the systems' capacities for representing negative binary numbers and negative voltages; some can and some can't. Analog-interface systems that can represent both are called *bipolar* converters; systems that can handle only positive voltages and quantities are called *unipolar*.

Unipolar converters chiefly use straight binary and binary-coded-decimal (BCD) representations of digital quantities. Bipolar converters use a variety of representations, including offset binary, one's- and two's-complement formats, and Gray code. For brevity, I will limit this discussion to converters using straight binary and offset binary representations.

Offset binary differs from straight binary only slightly. In offset binary, a number consisting of all zeros is said to represent the most negative possible quantity. The most obvious consequence of this convention is that the most significant bit acts as a sign bit, 0 for negative values and 1 for positive. For instance, in offset notation the bit string 01000000 represents −64, while the bit string 11000000 stands for +64.

The translation of digital values to proportional analog values is performed by either of two basic D/A-conversion circuits: the weighted-resistor circuit or the R-2R circuit. The *weighted-resistor* converter is by far the simpler and more straightforward. This parallel decoder requires only one resistor per input bit.

In the weighted-resistor D/A converter, solid-state switches are driven directly from the signals that represent the digital number D. Individual currents with voltage magnitudes related by powers of 2 (magnitudes of ½, ¼, ⅛, ..., 2^{-n}) are generated and summed by connecting a network of resistors with values of R, $2R$, $4R$, ..., 2^nR between the reference voltage $-V_{REF}$ and the summing point of an operational amplifier (op amp) by means of the set of electronic switches. After being summed, the various currents are converted to a voltage by the op amp, as shown in figure 1.

While this may appear to be a simple answer to an otherwise complex problem, this method has some significant drawbacks. The accuracy of this type of converter is a function of the combined accuracies of the resistors, switches (all switches have some resistance), and the output amplifier. In D/A-conversion systems of greater than 10 bits resolution, the values of the resistors become extremely large, and the resultant current flow is reduced to such a low value as to be lost in circuit noise.

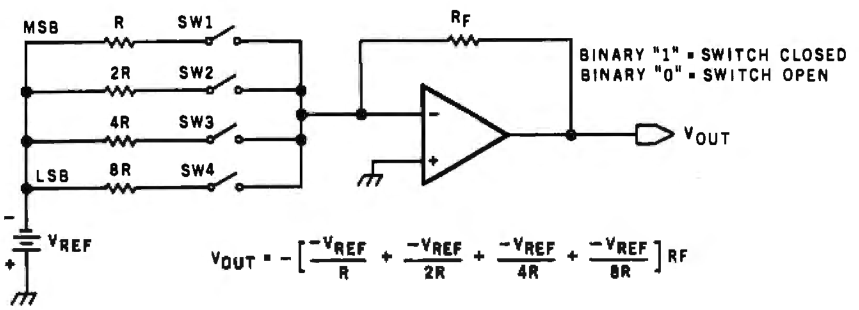

Figure 1: *A 4-bit weighted-resistor digital-to-analog converter. A 4-bit word is used to control four single-pole, single-throw solid-state switches. Each switch is in series with a resistor. The resistor values are related as powers of 2. The other sides of the switches are connected together at the summing point of an operational amplifier. Currents with magnitudes inversely proportional to the resistors are generated when the switches are closed. They are summed by the operational amplifier and converted to a corresponding voltage.*


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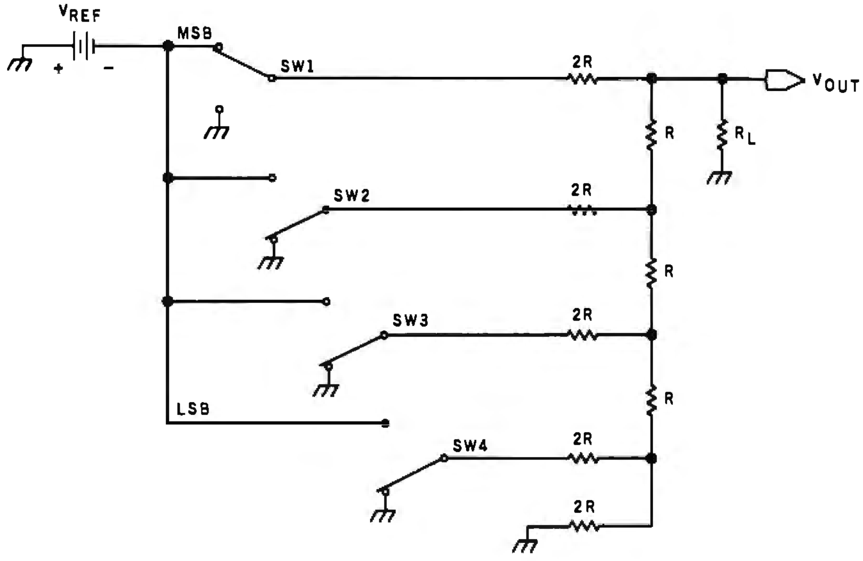
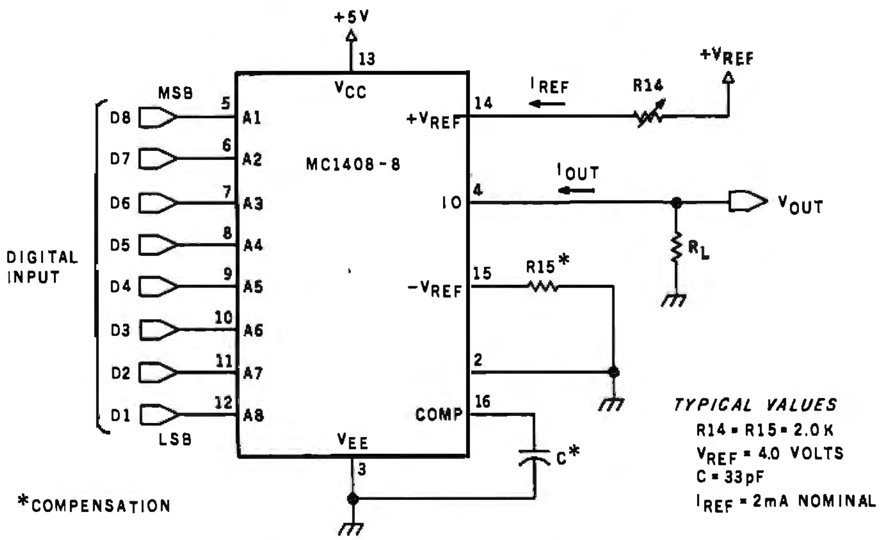


Figure 2: *A 4-bit R-2R-type resistor-ladder digital-to-analog converter. This type of D/A converter makes use of a resistor-ladder network constructed with resistors of value R and 2R. The topology of this network is such that the current flowing into any branch of a three-branch node will divide itself equally through the two remaining branches. Because of this, the current will divide itself in half as it passes through each node on its way to the end of the ladder. The four switches are again related as powers of 2. The position of each switch with respect to its distance from the end of the ladder determines its binary significance.*



$$I_{OUT} = A\left[D1/2 + D2/4 + D3/8 + D4/16 + D5/32 + D6/64 + D7/128 + D8/256\right]$$

WHERE $A \cong V_{REF}/R14$
AND DN = 1 FOR HIGH LOGIC LEVEL
DN = 0 FOR LOW LOGIC LEVEL

Figure 3: *A circuit employing the Motorola MC1408-8, a typical 8-bit current-output monolithic multiplying D/A converter. This integrated circuit contains an R-2R network like the one in figure 2, plus additional current-switching logic.*

For example, in an 8-bit D/A converter with R (the value of the resistor for the most significant bit) set to 10 k ohms, the value of the resistor for the least significant bit turns out to be 1.28 megohms. With a reference voltage of 10.00 V, only 7.8 microamperes would flow into the operational amplifier. This current is significantly below the response threshold of most low-cost op amps and would not be detected. Lowering the value of R to 100 ohms creates the opposite problem. At a reference voltage of 10.00 V, the input current to the amplifier would be 100 milliamperes (mA), more than most op amps can handle.

A reasonable alternative to the weighted-resistor D/A converter is the *R-2R* D/A converter, often referred to as a *resistor-ladder* converter. The R-2R D/A converter is the more widely used type even though it uses more components than the weighted-resistor type. A simple R-2R design is shown in the schematic diagram of figure 2 on page 76, including the reference voltage, a set of binary switches, and an output amplifier. The basis of this converter is a ladder network constructed with resistors of two values, R and $2R$.

In each bit position of the network, one resistor ($2R$) is in series with the bit switch, and the other (R) is in the summing line, so that the combination forms a pi network. This suggests that the impedances of the three branches of any node are equal, and that a current I, flowing into a node through one branch, flows out as $I/2$ through the other two branches. In other words, the current produced in the network by closing a bit switch is cut by half as it passes through each node on the way to the end of the ladder. Simply stated, the position of a switch with respect to the point where the current is measured determines the binary significance of the particular switch closure.

The R-2R D/A converter is easy to manufacture because only two resistor values are needed. The component stock could be reduced to one resistor value if two are used in series for each bit. Keeping matched resistor

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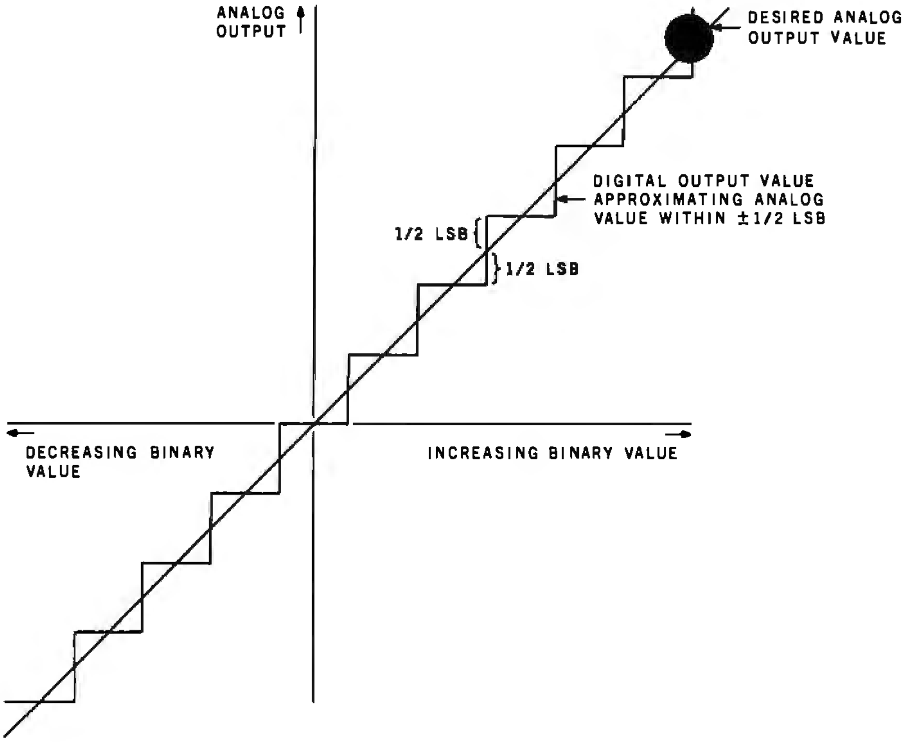

Figure 4: *Output characteristics of a digital-to-analog converter showing least-significant-bit quantization.*

values that have the same temperature coefficients contributes to a very stable design. Certain trade-offs are required between ladder resistance values and current flow to balance accuracy and noise.

One form of the R-2R ladder circuit is found in the multiplying digital-to-analog converter. Multiplying D/A converters, which utilize external variable analog reference voltages, produce outputs that are directly proportional to the product of the digital input multiplied by this reference. Functionally, these converters are available as current- or voltage-output types. The current-output devices are faster and less complex because they do not include additional output-amplifier stages. Therefore, they cost less than voltage types.

Probably the most economical current-output 8-bit multiplying D/A converter is the Motorola MC1408-8, shown in figure 3. It is duplicated by

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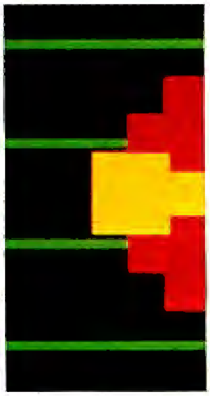
Features

• compact single board display controller • high efficiency 6809 microprocessor • Telidon alpha-numeric/geometric Videotex software in ROM • RS232C full duplex communication • independent transmit/receive baud rates, strap selectable from 75 to 9600 baud (odd, even or no parity). • 200 x 256 x 4 bit high speed raster video RAM • 8 grey levels (black to white), 6 colors and blinking white • RS170 RGB video and composite sync outputs. • input device interface for optional keypad or keyboard. • 8 character sizes including a maximum of 20 lines of 40 characters each.


Block Mosaic


Geometric

Ease of Operation

By virtue of the Picture Description Instruction (PDI) protocol used in Telidon Systems, images may be created from familiar graphic primitives such as points, lines, arcs and polygons. This same presentation level protocol is recognized as an international videotex standard and forms the kernel of the protocol selected by AT & T for their image communication networks. The use of an 8 bit data format, ASCII standard characters and RS232C serial communication, enhances the general purpose nature of the NORPAK display generator.

Applications

The compact size and low power consumption of the basic module facilitates integration into a complete display unit which may include a monitor and other specialized communications interfaces. It may be used as a simple output device connected to a computer or may form part of a stand-alone workstation. Many users who have been introduced to the potential of color graphics, through low resolution mosaic displays, will enjoy the increased spatial resolution of the pixel oriented raster bit plane technology. Some of the many potential applications include:

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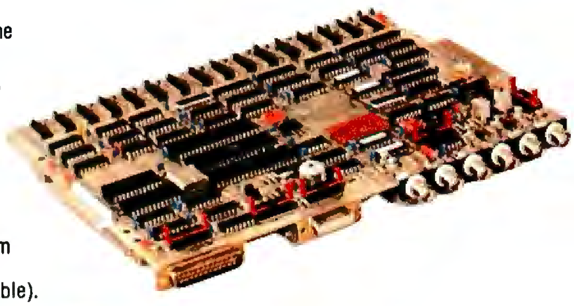

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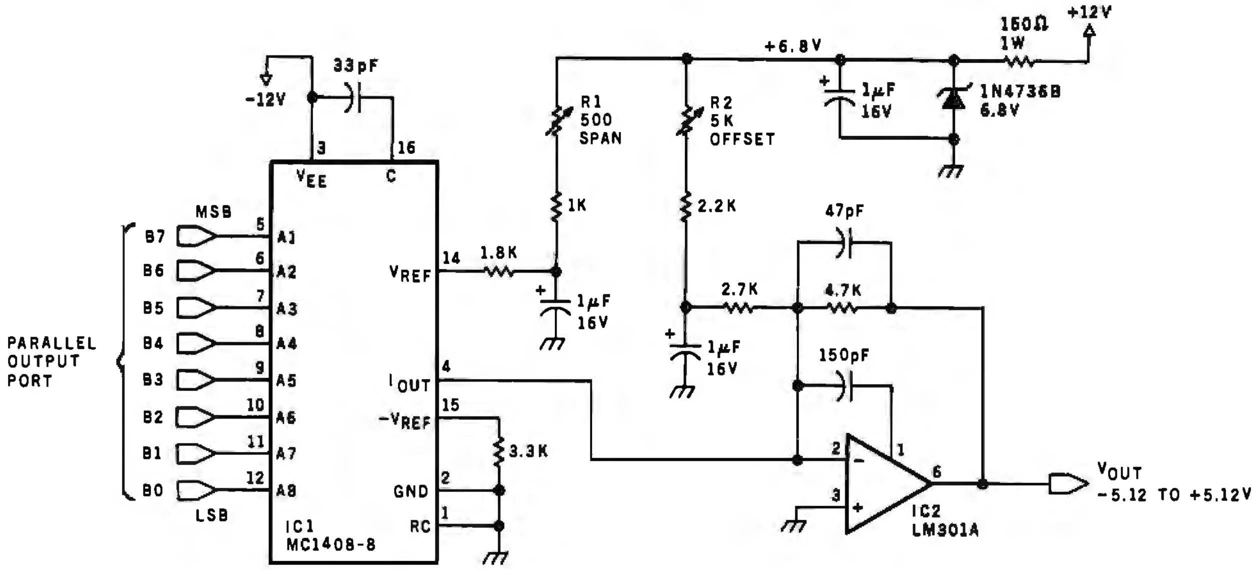

Number	Type	+5 V	GND	−12 V	+12 V
IC1	MC1408	13	7	3	
IC2	LM301A			4	7

Figure 5: *Schematic diagram of the final 8-bit MC1408-8-based multiplying digital-to-analog converter with span and offset adjustments.*

a number of companies under similar names. (For instance, Analog Devices, Inc., calls its version the AD1408.) This monolithic integrated circuit contains an R-2R ladder network and current-switching logic. Each binary bit controls a switch that regulates the current flowing through the ladder. If an 8-bit digital input of binary 11000000 (decimal 192) and a 2-mA reference current (derived from V_{REF}) are applied to the control lines of the converter, the output current would be equal to 192/256 × 2 mA or 1.50 mA.

Note that when binary 11111111 (decimal 255) is applied, there is always a remainder current equal to the least significant bit. This current is shunted to ground, and the maximum output current differs from the reference-amplifier current by a factor of 255/256. It comes out to be 1.992 mA for a 2.0-mA reference current. The relative accuracy of the MC1408-8 version is ±½ of the least significant bit, or 0.19 percent of full scale (see figure 4). This is more than adequate for most personal computer analog-control applications.

The final such circuit (see figure 5 on page 80) is an 8-bit multiplying D/A converter that uses the MC1408-8. As previously outlined, "multiplying" means that it uses an external variable reference voltage. In this case, a 6.8-V zener-diode-regulated voltage is passed through a resistor that sets the current flowing

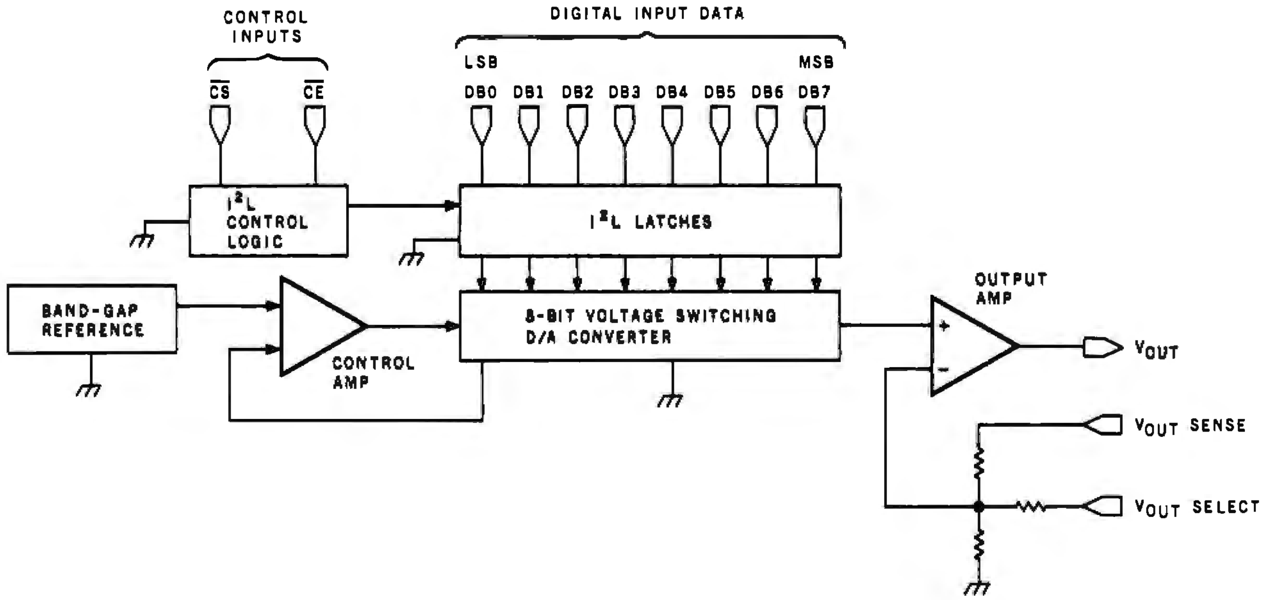

Figure 6: *Functional block diagram of the Analog Devices AD558 digital-to-analog converter.*


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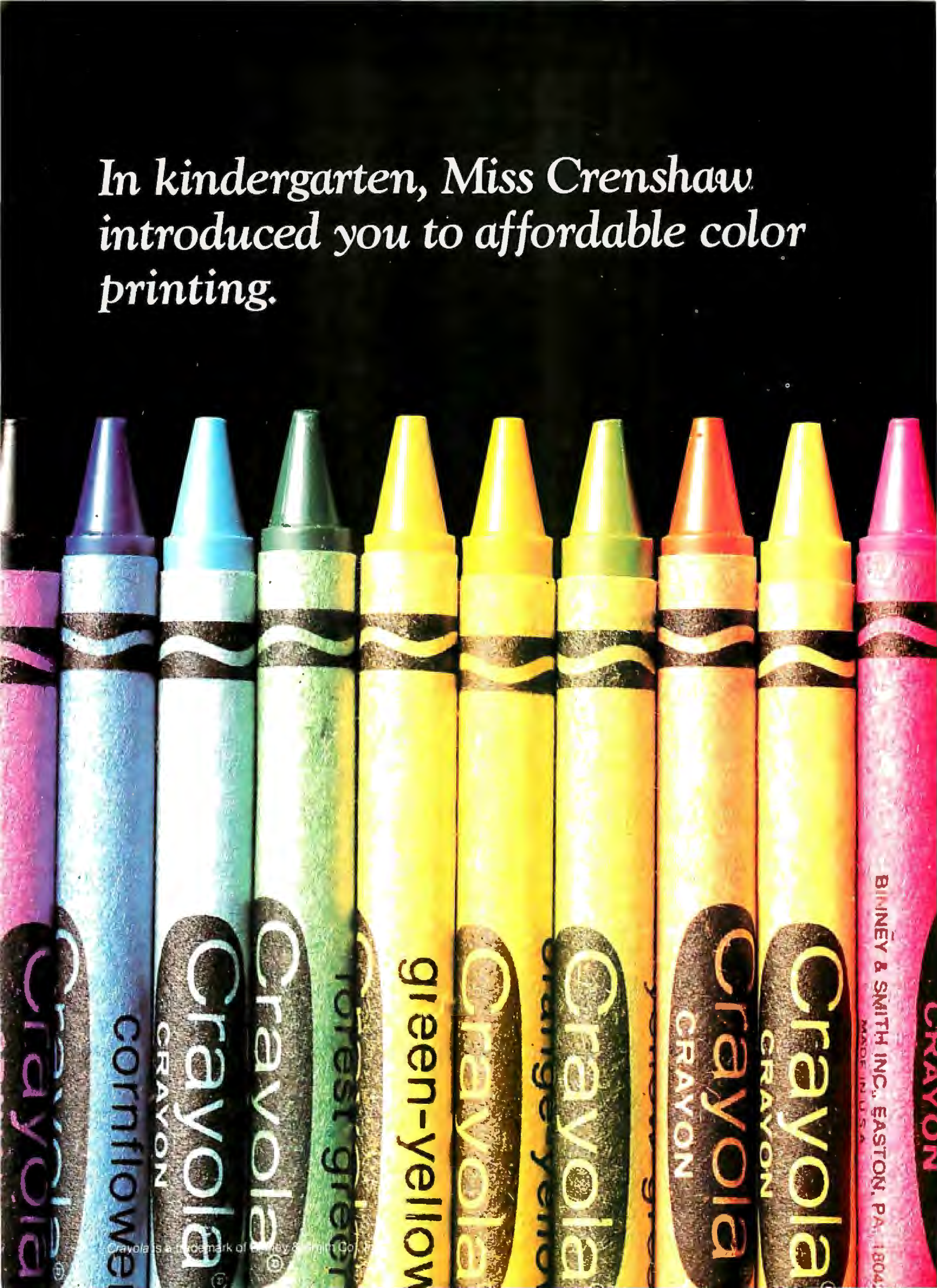
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BINNEY & SMITH INC., EASTON, PA.

into pin 14 to approximately 2 mA.

An additional resistor of value R1 (also in this current leg) allows the current to be varied by a small percentage and provides the ability to adjust the full-scale range of the converter. The output of the converter is a current equivalent to the product of the reference current and the binary data on the control lines. The current is converted to a voltage through IC2. When used in the offset-binary mode, the converter output is zero-offset through the use of the offset-adjustment potentiometer R2.

In offset binary, a value of hexadecimal 00 produces an output of −5 V from the converter. Hexadecimal FF produces an output of +5 V. In offset binary, if the most significant bit is 0, the output is negative; if the most significant bit is 1, the output is positive. Since the converter has a range of 10 V and is an 8-bit device, the resolution of the converter is 1/256 of 10 V, or approximately 40 mV. This means that the smallest output increments will be in 40-mV steps. Changing this to finer increments requires that the range be shorter, such as +2.56 V to −2.56 V. By adjusting the span and zeroing potentiometers, any reasonable range may be chosen. The resolution, however, will always be equal to the least significant bit or 1/256 of the range. With the 1408, the accuracy will be ±½ of the least significant bit.

Using this circuit is simply a matter of connecting the input lines of IC1 to a convenient latched parallel-output port. Any 8-bit value sent to that port will be converted to a voltage proportioned to that output.

While we don't have to contend with wiring up the actual ladder network to construct the D/A converter in figure 5, a parallel port and many discrete components are still required. Fortunately, analog I/O (input/output) technology has developed quickly in recent years, and sophisticated integrated circuits have become available, such as the Analog Devices AD558.

This 8-bit D/A converter can replace all the components previously discussed, including the parallel port, with a single chip. The AD558, shown in the block diagram of figure 6, contains an 8-bit latch, R-2R ladder network, reference voltage source, and output amplifier. The AD558 can run on a +5- to +15-V power supply and can be jumper-selected for 0- to 2.56-V or 0- to −10-V ranges. Using a separate operational amplifier, an offset converter can be configured or the ranges modified.

The AD558 can be used as a transparent D/A converter similar to the 1408 by holding the chip-enable and chip-select lines constantly low. However, it was primarily designed to be bus operated and appear as a "write-only" location in memory or I/O address space. Typical connections consist of a decoded address strobe, a write-enable signal, and the 8-bit data bus (illustrated in figure 7).

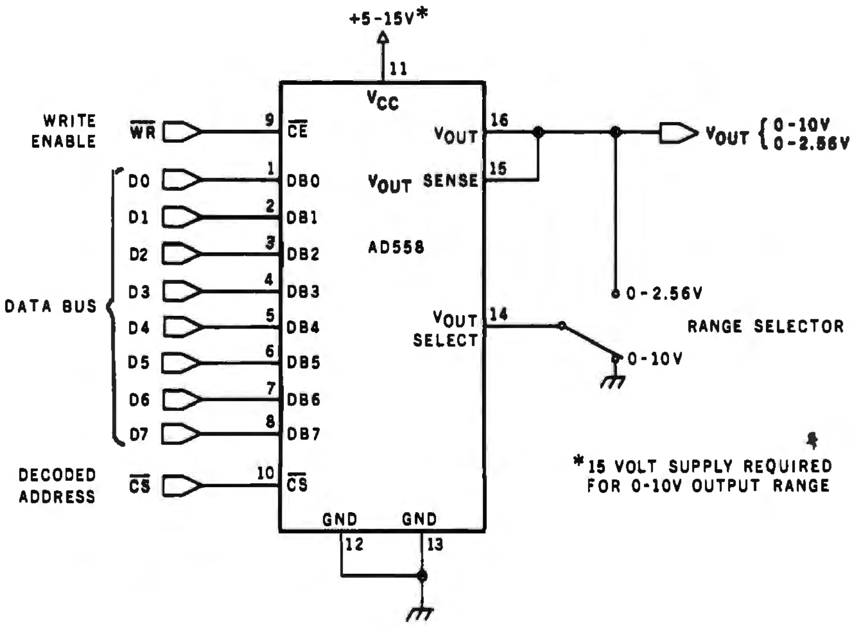

Figure 7: *Schematic diagram outlining typical connection of the AD558.*

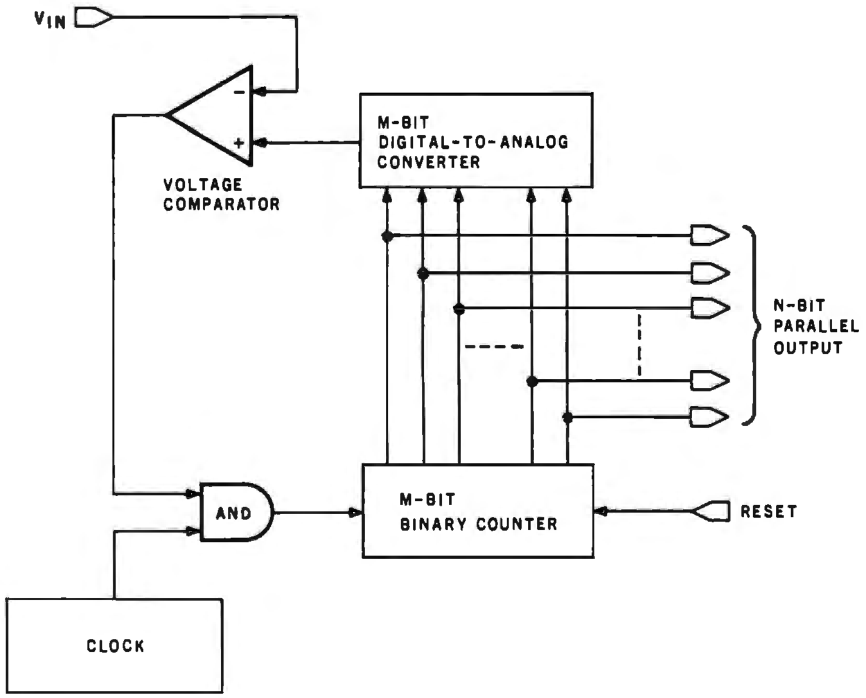

Figure 8: *Block diagram of a basic binary-ramp-counter A/D converter.*

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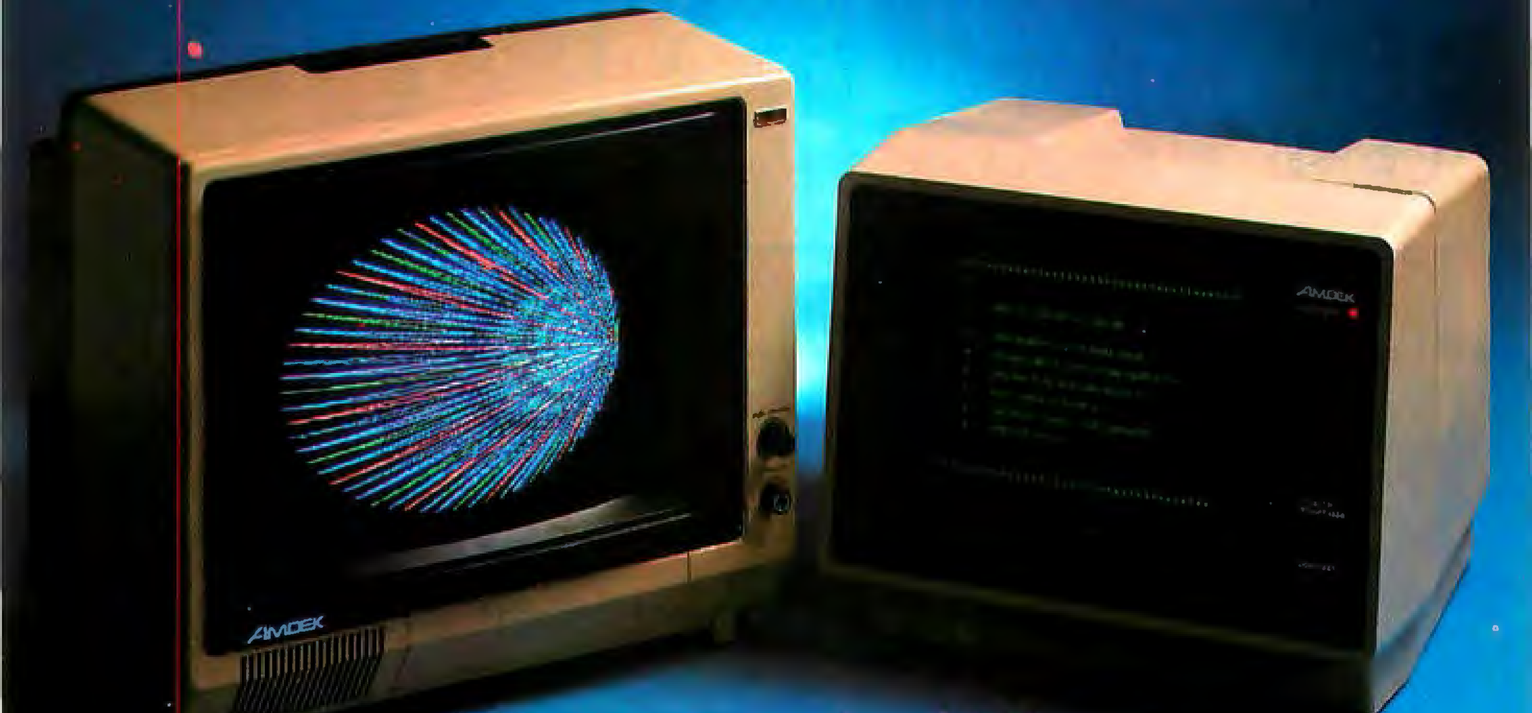

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Number	Type	+5 V	GND	−12 V	+12 V
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IC2	LM301A			4	7
IC3	MC1408	13	7	3	
IC4	7493	5	10		
IC5	7493	5	10		
IC6	7486	14	7		
IC7	7400	14	7		
IC8	NE555	8	1		
IC9	7495	14	7		
IC10	7495	14	7		

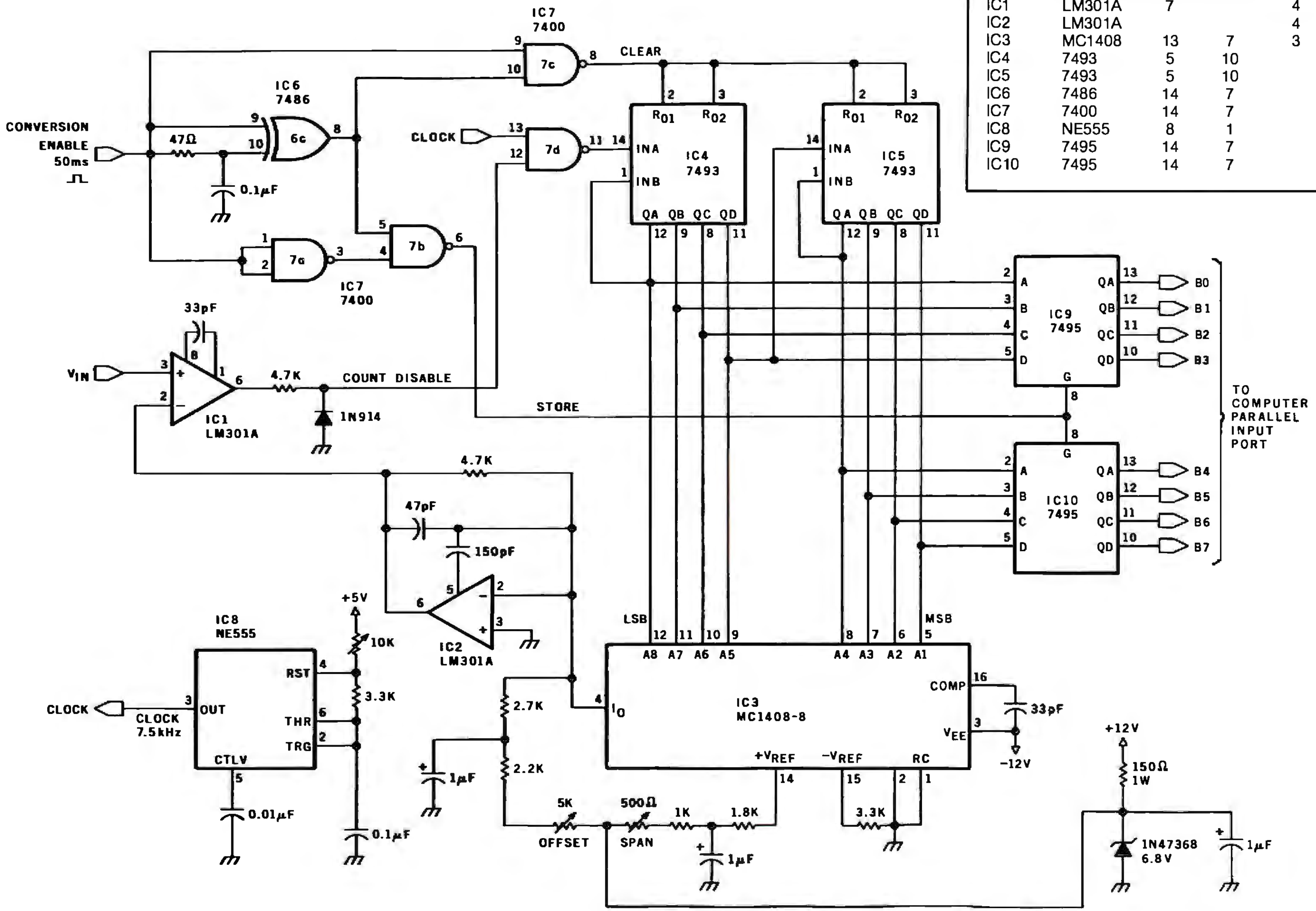
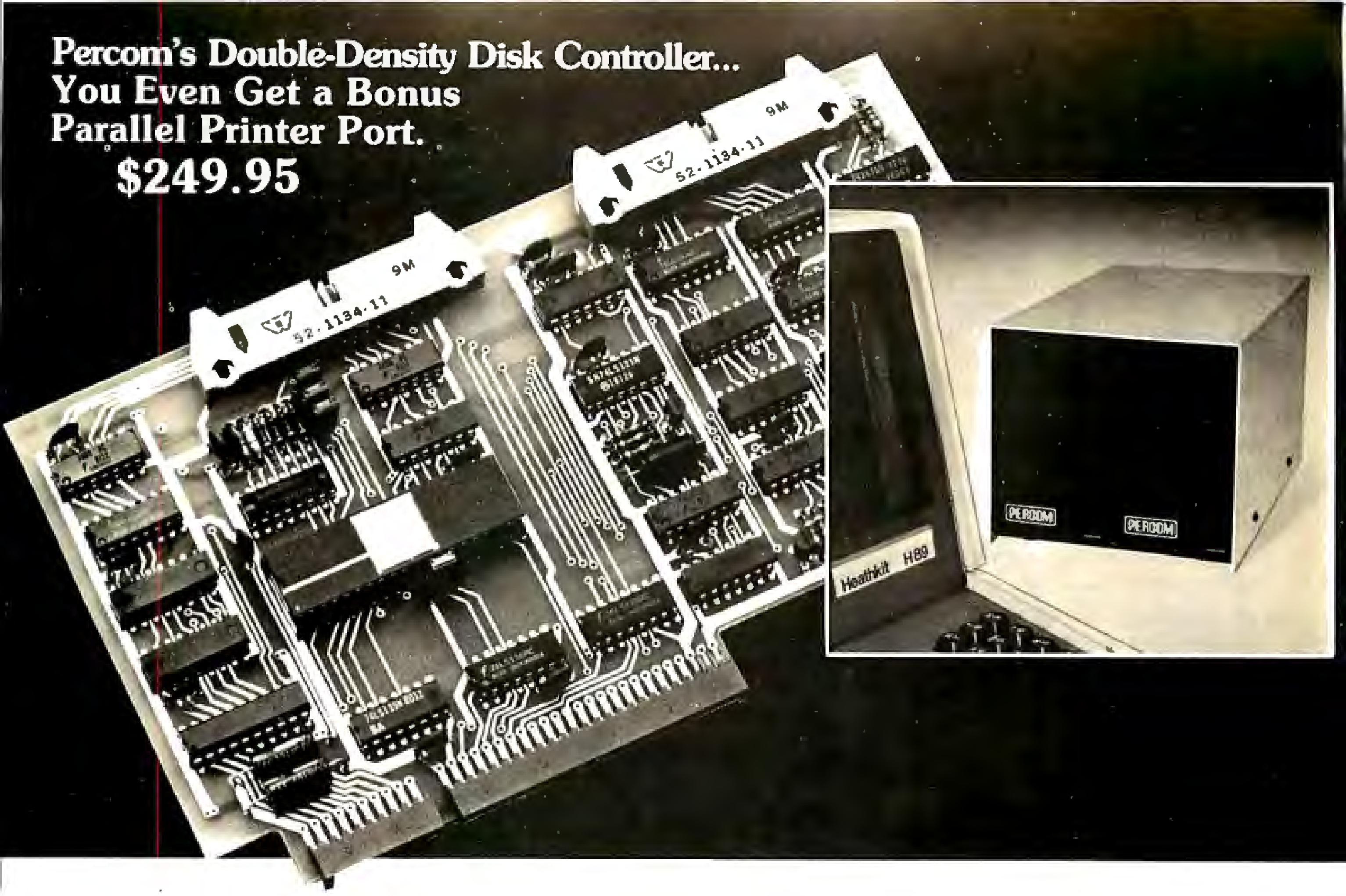


Figure 9: *Schematic diagram of an 8-bit binary-ramp-counter A/D-converter circuit.*



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(Many readers have written to me requesting circuits that facilitate connecting an analog x,y-coordinate chart recorder to a computer. Two AD558s addressed separately are all that is required.)

Analog-to-Digital Converters

In this sort of presentation, it is always a good idea to discuss digital-to-analog converters first. They are not complex and have only two basic methods of conversion worth discussing. Also, by introducing them first, I hope that you will become aware of the process of binary conversion and appreciate the concepts of resolution and accuracy. Practically speaking, however, if you're going to use your computer in a data-acquisition mode, say reading and recording temperatures, you need an analog-to-digital (A/D) converter.

An A/D converter converts analog voltages into a digital representation compatible with the computer's input needs. Akin to the 8-bit D/A converter, an A/D converter is subject to the same conversion rules. If you are trying to read a 10-V signal with an 8-bit converter, the resolution will be 1/256 of 10 V (approximately 40 mV), and the accuracy will be ±½ the least significant bit.

For greater resolution, more output bits are necessary. The number of bits does not set the input voltage range of a converter; it only determines with what precision the output value is represented. An 8-bit converter (either A/D or D/A) can be set up just as easily to cover a range of 0 to −1 V as it can be to cover 0 to +1000 V. Often the same circuitry is used with only a final amplification stage or resistor-divider network changed. Note that an 8-bit converter with a range of 1000 V has a resolution of only 4 V, and it would be useless to measure 0- to 10-V signals. The problem can be reconciled in a number of ways. The easiest solution is to use a converter with more bits. A 16-bit converter, which has 65,536 steps instead of 256, would cover the same 1000-V range in 15-mV increments.

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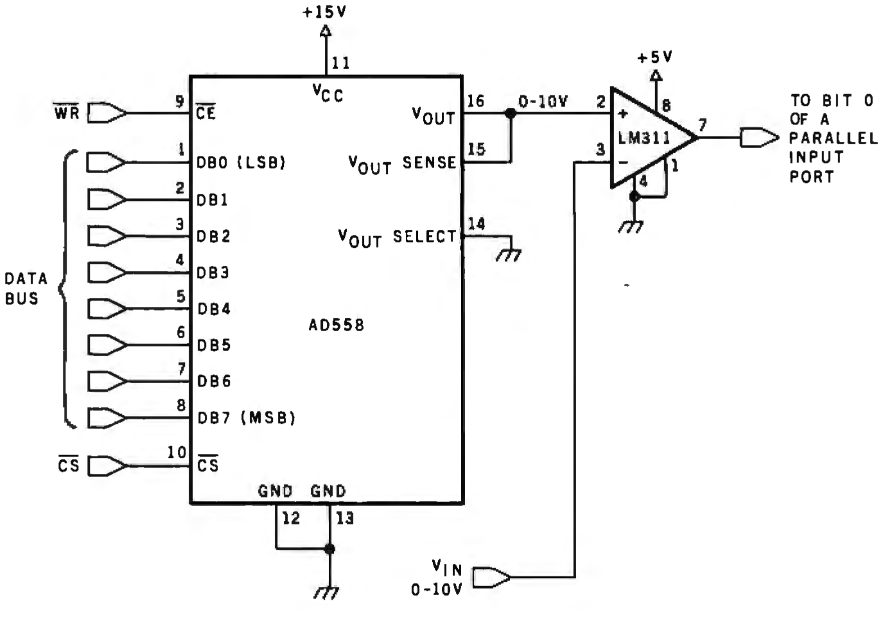

Figure 10: *A software-driven 8-bit A/D converter.*

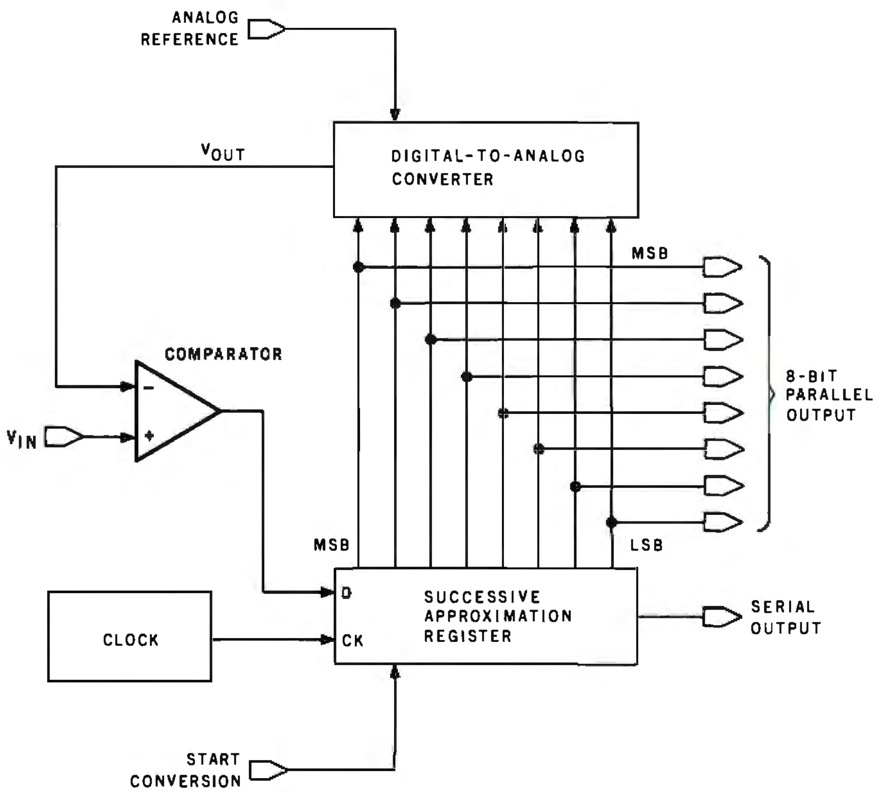

Figure 11: *Block diagram of a typical 8-bit successive-approximation A/D-conversion system.*

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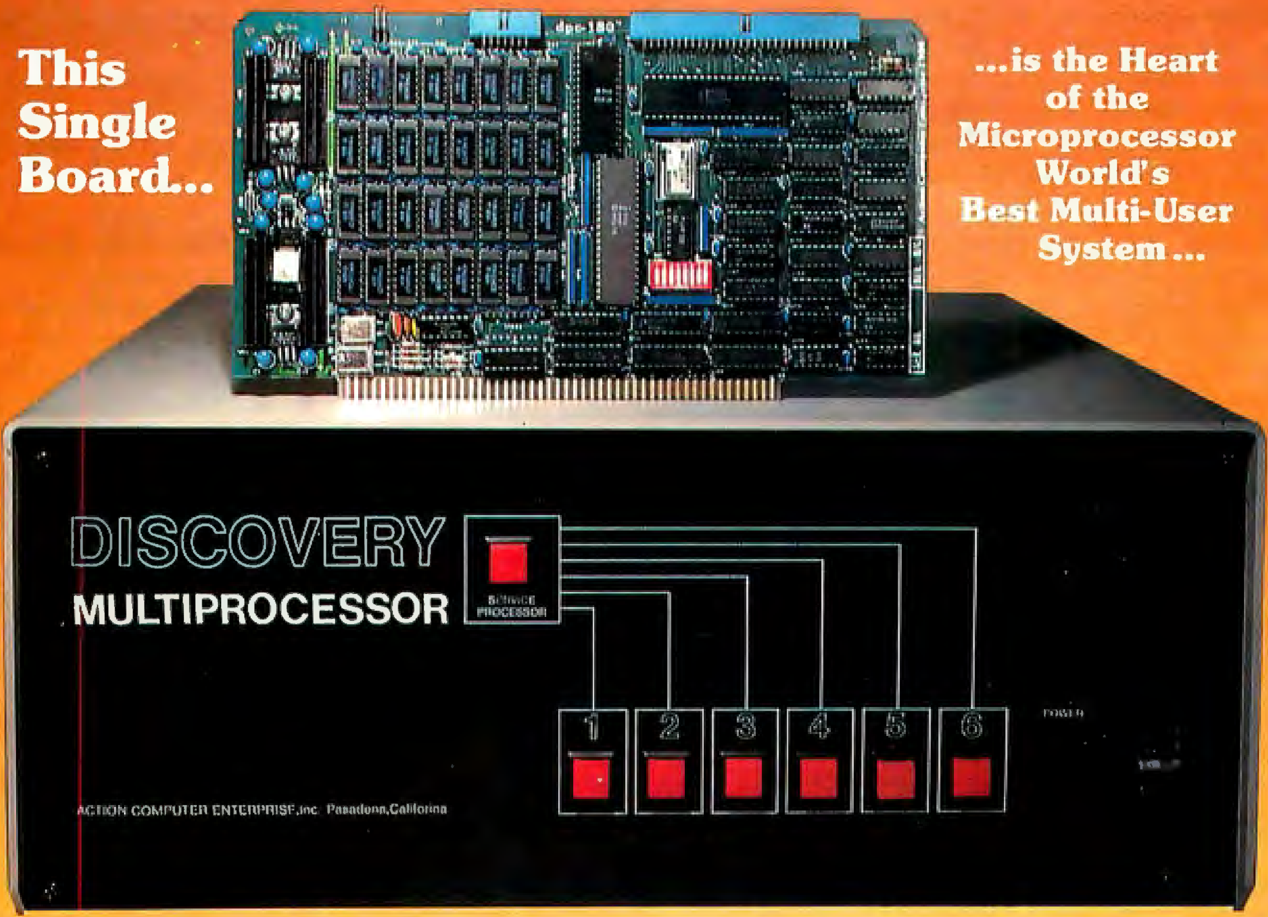

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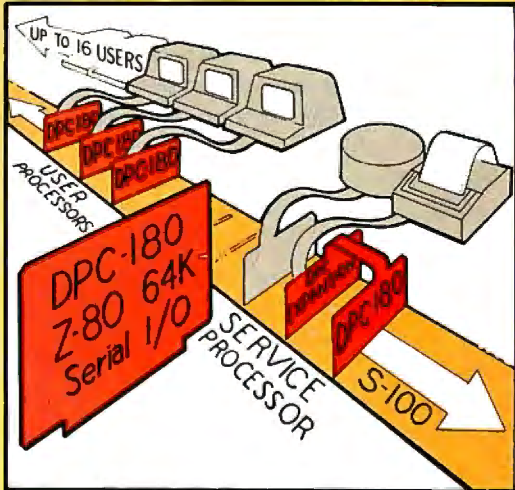

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able price/performance ratio is often more important than wide-range capability. Analog-to-digital conversion is considerably more expensive than digital-to-analog conversion, and price is directly related to resolution and accuracy.

The A/D converter that scans thermistor probes and controls the ambient temperature in a large supermarket cannot encode video information from an optical scanner. A/D converters, much more than D/A converters, are specifically tailored to an application. Speed, accuracy, and resolution are variables in any converter design, but the blending of these choices can greatly affect the cost in A/D conversion.

Most confusing is the variety of A/D-converter designs. They range from very slow, inexpensive techniques to ultrafast, expensive ones. Ultimately, you get what you pay for. In the limited space available, I shall present the more practical approaches. For further information on other techniques, I recommend the sources listed at the end of the article.

Binary-Counter A/D Converter

If you plan to build an analog-to-digital converter, the binary-counter design is the type to consider because it uses relatively few components and is easy to build.

Figure 8 on page 84 shows the basic block diagram for the binary-ramp-counter converter. A D/A converter is used to reconvert the digital output of a binary counter back to analog form for comparison against the analog input. If at any instant during the count the two signals are found to be equal, whatever binary value is currently set on the D/A input is deemed to be our A/D output.

The simplest way to operate the system is to start the counter initially at a zero count and allow it to count until the D/A reading equals or exceeds the analog input. The only consideration to keep in mind when designing this type of circuit is that the clock frequency sent to the D/A converter cannot be faster than the combined response of the comparator and D/A converter. If it takes 100

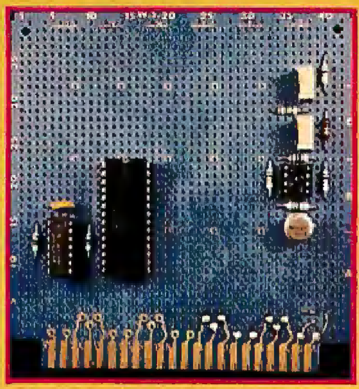

Photo 2: *Prototype of the analog-to-digital converter system of figure 13, which uses the Analog Devices AD7581 integrated analog-to-digital converter.*

microseconds (μs) for these components to settle out, the maximum counter-incrementing rate should be 10 kilohertz. For an 8-bit converter (counting from 0 to 256 each sample period), the maximum sample rate is 10,000/256, or about 39 samples a second. In practice, however, 5 μs is a more reasonable settling time, with about 750 samples per second.

Figure 9 on page 86 shows the schematic diagram of a binary-ramp converter. The counter output is connected to the MC1408-8 to provide a direct-feedback analog comparison of the value set on the counter.

Initially, IC4 and IC5 are cleared, and the D/A-converter output should be at whatever the minimum input voltage will be. For a 0- to 5.12-V converter, this would be 0 V; for a −2.56- to +2.56-V unit, it would be −2.56. If the output of IC1 is less than V_{IN}, the clock pulses are allowed to reach the counter. As each pulse increments the counter, the output of the D/A converter keeps rising until it eventually equals or just exceeds V_{IN} on the comparator. When this happens, additional clock pulses are inhibited. At the end of the sample period, the count values on IC4 and IC5 are stored in a separate register.

For the computer to read this data, it is merely necessary to connect this register to an input port and read it directly.

The circuit of figure 9 can stand alone. It does not require a computer for operation. The A/D converter updates itself at a preselected sample rate and loads this value into an 8-bit latch. All functions of the conversion are performed in hardware.

If you are willing to substitute the computer for a few of the hardware blocks in figure 9, much of the hardware can be reduced. For example, parameters for an AD558 D/A converter can be loaded directly from a program and its output compared to the unknown input voltage.

If the comparison is negative when read through an input port, the AD558 is incremented and the comparison repeated. At some point the comparison has a true result, and that value is the desired digital result. Shown in figure 10 on page 88, the entire circuit requires only two chips.

Successive Approximation

A simple binary-ramp counter should suffice for noncritical data acquisition. However, such devices are slow. Each sample can take as many as 256 iterations of the program. This is especially critical in a software-driven converter where each iteration may take 20 or 30 μs for execution of all the instructions. For faster sampling rates, a technique called *successive approximation* is used.

Figure 11 is a block diagram of a typical successive-approximation A/D converter. Like the binary-ramp converter just discussed, this converter also uses a D/A converter in the feedback loop, but the binary counters are replaced with a special successive-approximation register (SAR).

Initially, the outputs of the successive-approximation register and the mutually connected D/A converter are at a zero level. After a start-conversion pulse is received, the SAR enables its bits one at a time starting with the most significant bit. As each bit is enabled, the comparator gives an output signifying that the input signal is greater or less in amplitude than the output of the

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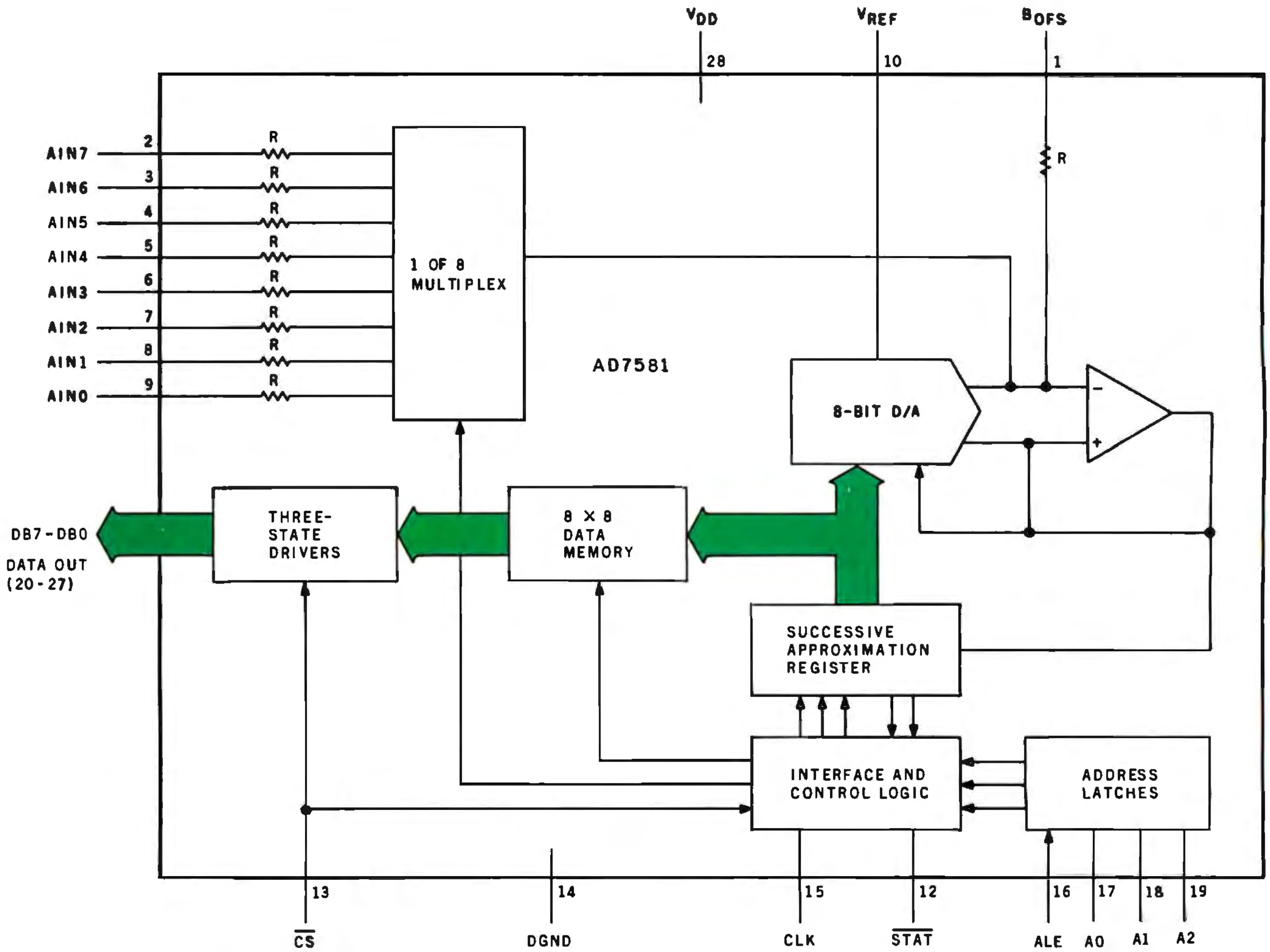


Figure 12: *Functional block diagram of the Analog Devices AD7581 A/D converter.*

D/A converter. If the D/A output is greater than the input signal, a 0 is set as the value of the corresponding output bit. If the D/A output is less than the input signal, the circuit sets the corresponding bit to a 1. The register successively moves to the next bit (retaining the settings on the previously tested bits) and performs the same test. After all the bits have been tested, the conversion cycle is complete. In contrast to the 256 clock pulses of the binary-counter method, the entire conversion period of the successive-approximation A/D converter takes only eight cycles. (It is possible to use the circuit of figure 10 as an SAR converter simply by having the program perform a successive-approximation comparison rather than a strict binary addition.)

8-Channel 8-Bit Converter

The majority of commercial monolithic A/D converters presently available use SAR-conversion techniques. Advances in integration processes have arrived at the point where almost an entire data-acquisition system can be built on a single chip. This is the case with the Analog Devices AD7581 8-bit 8-channel data-acquisition system. A block diagram is shown in figure 12.

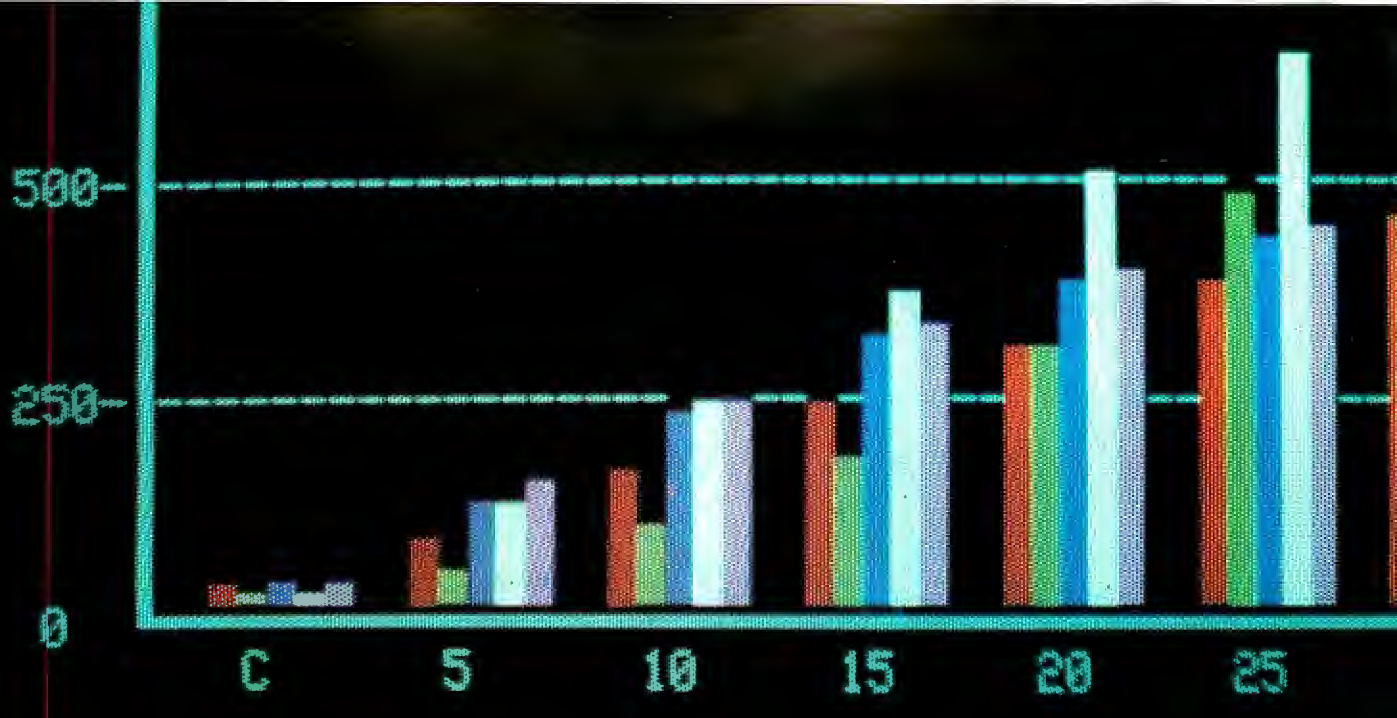
The AD7581 connects directly to the microcomputer bus through three-state bus drivers and appears to the computer as eight sequential memory or input-port locations. This single 5-V CMOS (complementary metal-oxide semiconductor) chip contains an 8-channel successive-approximation A/D converter and an on-chip 8- by 8-bit dual-port memory.

In functioning, the AD7581 scans the eight inputs and loads the values in an 8-byte register. When the computer reads data from these address locations, it reads the value stored during the converter's most recent scan. Each conversion requires 80 μs (at a 1-megahertz clock rate) and 640 μs for a complete channel scan. The normal conversion range is 0 to +10 V on each input.

Figure 13 is the schematic diagram of a typical AD7581 interface. IC1 and IC2 are an AD581 voltage-reference chip and MC1458 op amp. IC2 inverts the output of IC1 to produce a −10.00-V reference input for the AD7581. The other half of IC2 is used as an offset-adjustment input for the AD7581.

Two control lines, ALE (address latch enable) and $\overline{CS}$ (chip select), facilitate computer synchronization. Normally, the ALE line can be tied high on computers that send the address out on the address-bus lines A0 through A7 during memory and I/O transfers. Reading the proper input channel requires only logical-

Text continued on page 98



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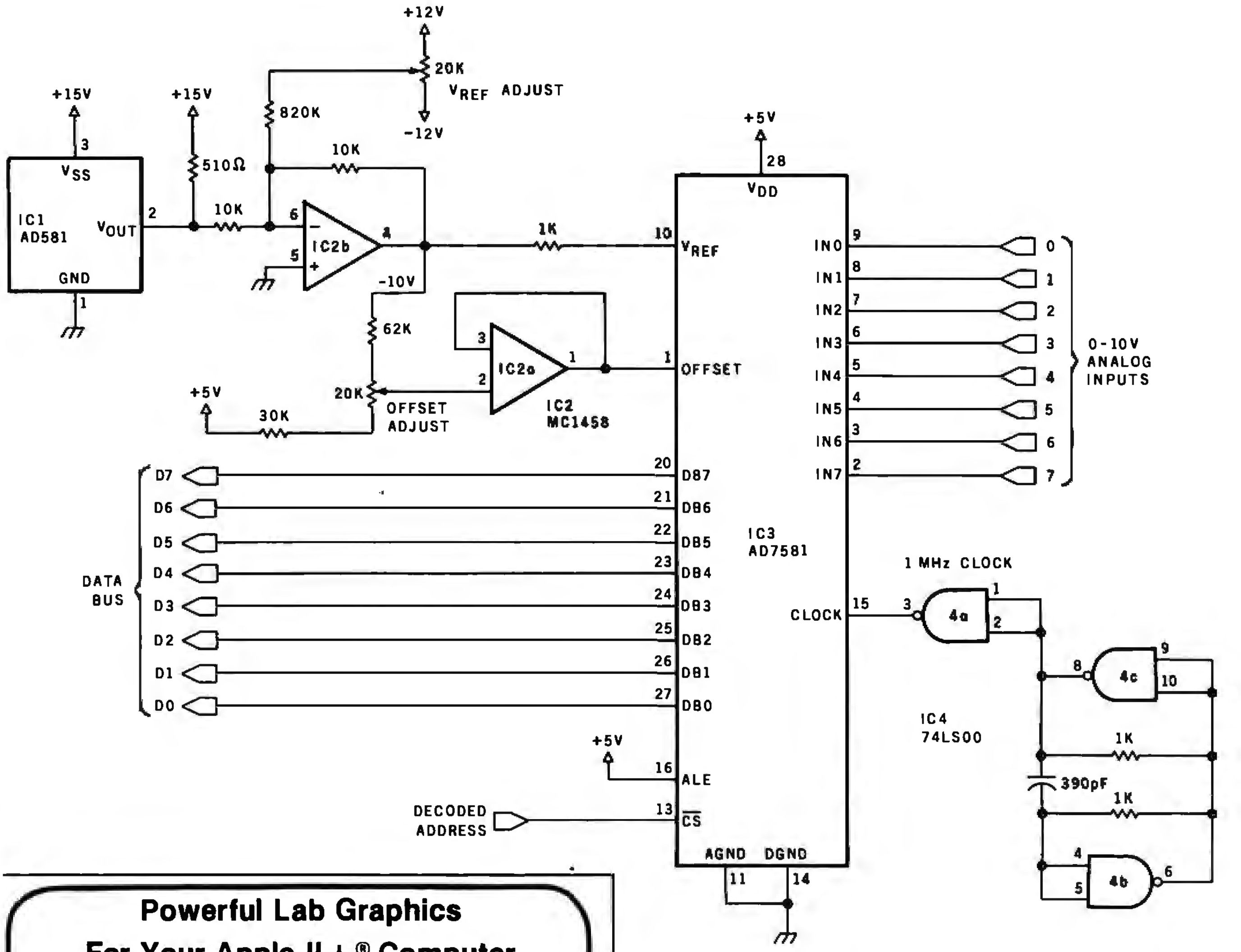

Number	Type	+5 V	GND	−15 V	+15 V
IC1	AD581		1		3
IC2	MC1458			4	8
IC3	AD7581	28	14		
IC4	74LS00	14	7		

Figure 13: *Schematic of an 8-channel 8-bit data-acquisition system using the AD7581. Because of the dual-port memory design of the AD7581, the eight analog-input channels appear to the host processor as eight addressable memory locations.*

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Text continued from page 92:

ANDing the read-enable line and a chip-select signal.

In Conclusion

Anyone who has ever built an analog I/O interface for a computer will immediately recognize the significance of these two products from Analog Devices. For the first time, analog-interfacing components are being correctly referred to as data-acquisition systems, rightly so because virtually everything is provided.

Another important consequence of such cost-effective components is their eventual integration into many more computer-based systems. Some day, even games and pocket calculators will be able to make an instant inventory of their "real-world" environment and react accordingly.

Next Month:

Build a computerized weather monitor. ■

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Editor's Note: *Steve often refers to previous Circuit Cellar articles as reference material for the articles he presents each month. These articles are available in reprint books from BYTE Books, 70 Main St., Peterborough, NH 03458.* Ciarcia's Circuit Cellar *covers articles appearing in BYTE from September 1977 through November 1978.* Ciarcia's Circuit Cellar, Volume II *presents articles from December 1978 through June 1980.*

To receive a complete list of Ciarcia's Circuit Cellar kits available from the Micromint, circle 100 on the inquiry card.

MIKBUG and the TRS-80

Part 2: A File Transfer and Debugging Package

Robert Labenski
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West Hartford, CT 06119

Last month in part 1, I presented a 6800 editor/cross-assembler that allows a TRS-80 Model I to produce object code for a MIKBUG system. In this concluding part, I'll present a file-transfer and debugging package called the MOM6800. It can make your TRS-80 act like an enhanced MIKBUG terminal with disk storage of your 6800 object-code files. (Your TRS-80 must be equipped with a disk drive and an RS-232C interface. Your 6800 system should be equivalent to the Motorola MEK 6800 D1 with the MIKBUG monitor.)

Features of the MOM6800

The 6800 MIKBUG and TRS-80 are linked via their RS-232C interfaces. MIKBUG thinks the TRS-80 is an I/O (input/output) terminal, which means that the TRS-80 can communicate only via standard MIKBUG commands. However, the MOM6800 program interprets your input, allowing you to use MIKBUG commands plus some extras, including file transfer, display of 16 bytes of memory (D*xxxx*), and execution at a specified address (G*xxxx*).

When you're running the MOM6800 program, you'll see the "*" prompt (à la MIKBUG). Whenever this is displayed, you can enter a normal MIKBUG command. To use one of my added commands, press the "@" key. This produces a new prompt, CMD=>, that indicates that you may enter any of the commands given in table 1.

Some of these enhanced commands may take a while for completion, since they require a fair amount of communication between computers.

Command	Description
L	Load an assembled program into the 6800 system. Unless you've already used this command in this session, you will be prompted for the name of the TRS-80 disk file containing the object code. You can only load programs created by the cross-assembler presented last month. The program will be loaded and transferred automatically to the 6800 system. Each byte will be echoed in hexadecimal on the TRS-80 screen.
D*xxxx*	Display 16 bytes of 6800 memory starting at hexadecimal *xxxx*.
G*xxxx*	Start execution at hexadecimal *xxxx*. (Using ordinary MIKBUG commands, this would be equivalent to loading *xxxx* into hexadecimal addresses A048-A049 and executing a G (go).)
S	List the source code currently in TRS-80 memory. The format will be that of my cross-assembler. To pause the scrolling display, press SHIFT @. To continue, press ENTER.
B	Set or reset a breakpoint. Up to ten are available, numbered 0-9. When you set a breakpoint, the monitor will enter an SWI into the address you specify and save the previous contents of that address. When the breakpoint is taken during execution, MIKBUG will stop and display the register contents. The PC (program counter) will point to the breakpoint address. To continue after a breakpoint, reset the breakpoint and use the G command.
H	Display a "help" menu.

Table 1: *A summary of commands available in the MOM6800 monitor program. Notice the additions to the ordinary MIKBUG commands. In addition to these, you can use any of the standard MIKBUG commands:* M*xxxx*, *G, R, P, and L.*

How to Use the MOM6800

There are two parts to the MOM6800 package: an initialization program, written in Z80 assembler code, and an enhanced monitor program, written in BASIC. The initialization program is given in listing 1; the monitor program in listing 2.

Using a Z80 editor/assembler,

Text continued on page 107

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Listing 1: *The Z80 program to initialize the RS-232C interface and set up input/output linkages from the TRS-80 to the MIKBUG system. Some of the code is from my Dasher printer driver; hence, the Dasher references.*

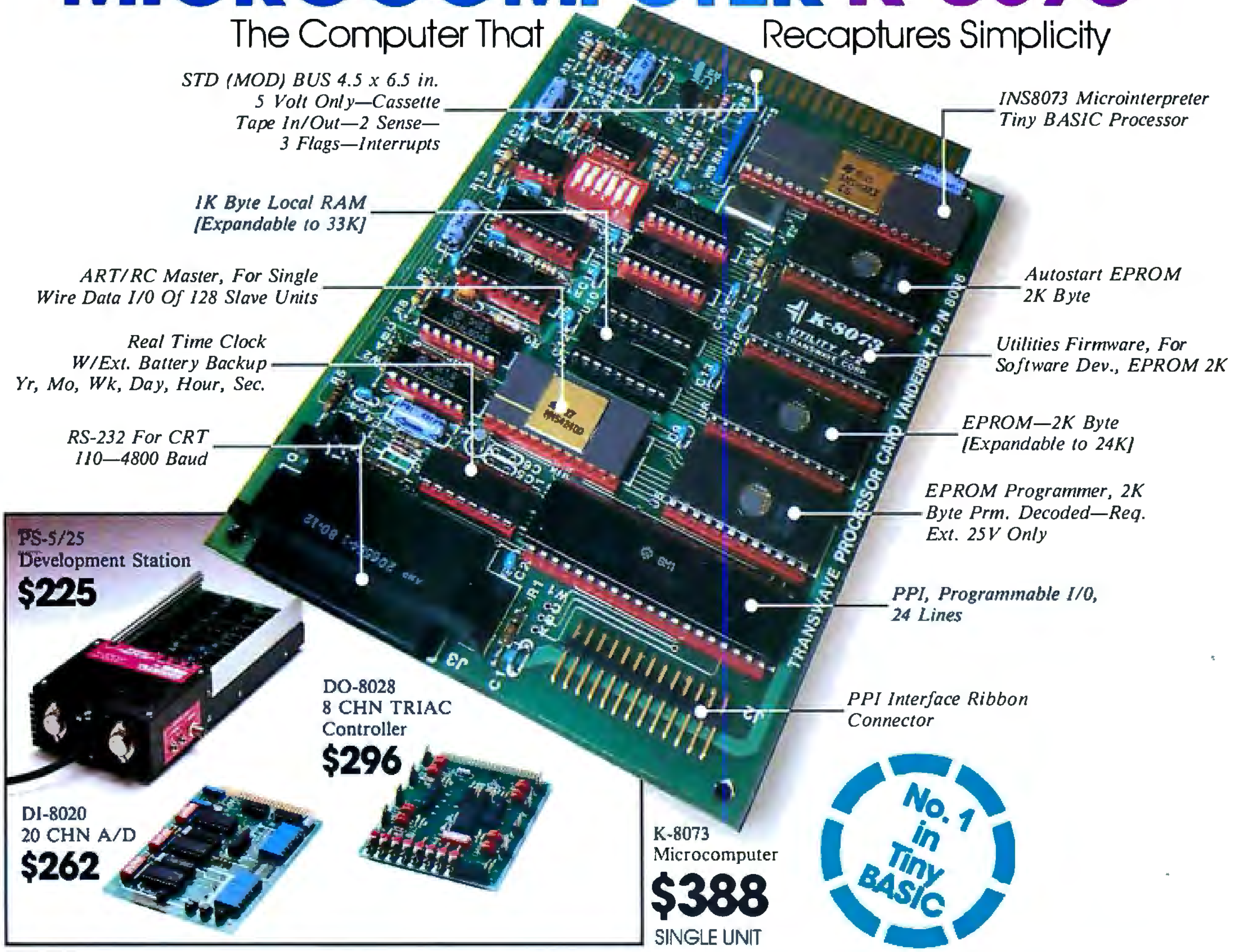
Memory Location | Object Code | Source Code

```
                 ; 6800 MIKBUG:TRS80 DRIVER PROGRAM
                 ;WRITTEN BY ROBERT LABENSKI
                 ;
                 ; 6800  DRIVER PROGRAM
                 ; LPRINT FOR OUTPUT
                 ;INPUT DEFUSR0(&HFEFA)
                 ; B$="":B=USR0(VARPTR(B$))
                 ; B$= DATA FROM 6800: B=LENGTH OF DATA
4026                      ORG 4026H
4026 AFFE                 DEFW DOUT ; SET PRINTER DCB ADDRESS
4049                      ORG 4049H ; SET BASIC UPPER LIMIT
4049 ADFE                 DEFW DOUT-2
40B1                      ORG 40B1H ; SET BASIC MEM
40B1 ADFE                 DEFW DOUT-2
FE80                      ORG 0FE80H
FE80 D3E8        START    OUT (0E8H),A ;RESET UART
FE82 DBE9                 IN A,(0E9H) ; READ SWITCHES
FE84 E6F8                 AND 0F8H
FE86 F604                 OR 04H
FE88 D3EA                 OUT (0EAH),A ; SET CHR+SS+PARITY
FE8A DBE9                 IN A,(0E9H)
FE8C E607                 AND 07H
FE8E 21A7FE               LD HL,TABLE
FE91 0600                 LD B,00H
FE93 4F                   LD C,A
FE94 09                   ADD HL,BC
FE95 7E                   LD A,(HL)
FE96 D3E9                 OUT (0E9H),A ;SET BAUD RATE
                 ;INIT KEYBOARD
FE98 2A1640               LD HL,(4016H)
FE9B 22F8FE               LD (KEND+1),HL
FE9E 21CAFE               LD HL,KBFIX
FEA1 221640               LD (4016H),HL
FEA4 C32D40               JP 402DH ; GO BACK TO DOS
FEA7 22          TABLE    DEFB 22H
FEA8 44                   DEFB 44H
FEA9 55                   DEFB 55H
FEAA 66                   DEFB 66H
FEAB 77                   DEFB 77H
FEAC AA                   DEFB 0AAH
FEAD CC                   DEFB 0CCH
FEAE EE                   DEFB 0EEH
                 ; SEND DATA FOR THE PRINTER THERE
FEAF E5          DOUT     PUSH HL
FEB0 C5                   PUSH BC
FEB1 79                   LD A,C ; TEST FOR
FEB2 FE0D                 CP 0DH ; CR
FEB4 2808                 JR Z,STATIN ; OK PASS
FEB6 FE0A                 CP 0AH ; LF
FEB8 2804                 JR Z,STATIN ; OK PASS
FEBA FE20                 CP 20H ;CONTROL CHARACTER
FEBC 3809                 JR C,RETX ; DON'T PRINT
FEBE DBEA        STATIN   IN A,(0EAH) ; LOAD STATUS
FEC0 CB77                 BIT 6,A ; TEST READY
FEC2 28FA                 JR Z,STATIN ; PTR BUSY LOOP
                 ; OUTPUT CHR
FEC4 79                   LD A,C
FEC5 D3EB                 OUT (0EBH),A ;SEND IT OUT
FEC7 C1          RETX     POP BC
FEC8 E1                   POP HL
FEC9 C9                   RET
                 ;GET DATA FROM DASHER
FECA 32F6FE      KBFIX    LD (ASAVE+1),A ; SAVE ACC
FECD DBEA                 IN A,(0EAH) ; ANY DATA
FECF CB7F                 BIT 7,A ; FROM THE DASHER
FED1 2822                 JR Z,ASAVE ; NO EXIT TO CK THE TRS KB
FED3 DBEB                 IN A,(00EBH) ; GET DASHER DATA
FED5 E67F                 AND 7FH ; GET RID OF PARITY BIT
FED7 FE0D                 CP 0DH
FED9 2804                 JR Z,KEY1
FEDB FE20                 CP 20H ; CTL CHAR
FEDD 3816                 JR C,ASAVE ; FORGET IT
                 ; DATA FROM 6800 CAPTURED HERE
FEDF E5          KEY1     PUSH HL
FEE0 2A38FF               LD HL,(CURR) ; GET CURRENT ADDRESS
FEE3 77                   LD (HL),A
FEE4 3A3AFF               LD A,(LEN)
FEE7 FE40                 CP 64 ; ONLY 64 CHARCTERS
FEE9 CAF4FE               JP Z,NOSAVE
FEEC 23                   INC HL
FEED 2238FF               LD (CURR),HL
FEF0 3C                   INC A
FEF1 323AFF               LD (LEN),A
FEF4 E1          NOSAVE   POP HL
```

Listing 1 continued on page 107

TRANSWAVE'S Tiny BASIC MICROCOMPUTER K-8073

The Computer That Recaptures Simplicity



INPUT ▶▶▶▶▶ DECISION ▶▶▶▶ OUTPUT

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In addition to an extensive input range, this A/D module eliminates the usual installation hassles because of the unique ART/RC communications route. A single twisted pair or coaxial wire serves as the bi-directional DPW (Data Pathway) between the DI-8020 and the K-8073 Tiny BASIC Microcomputer.

DECISION

After receiving data, the K-8073 executes from your EPROM based Tiny BASIC program.

OUTPUT

Completing the cycle of I→D→O is the DO-8028: an 8 channel TRIAC Control Module. This board features 8 optically isolated TRIACS with a maximum rating of up to 300 Watts AC control per channel. Receiving commands from the K-8073 via the full duplex DPW, you can daisy chain as many as 128 of these "slave" stations.

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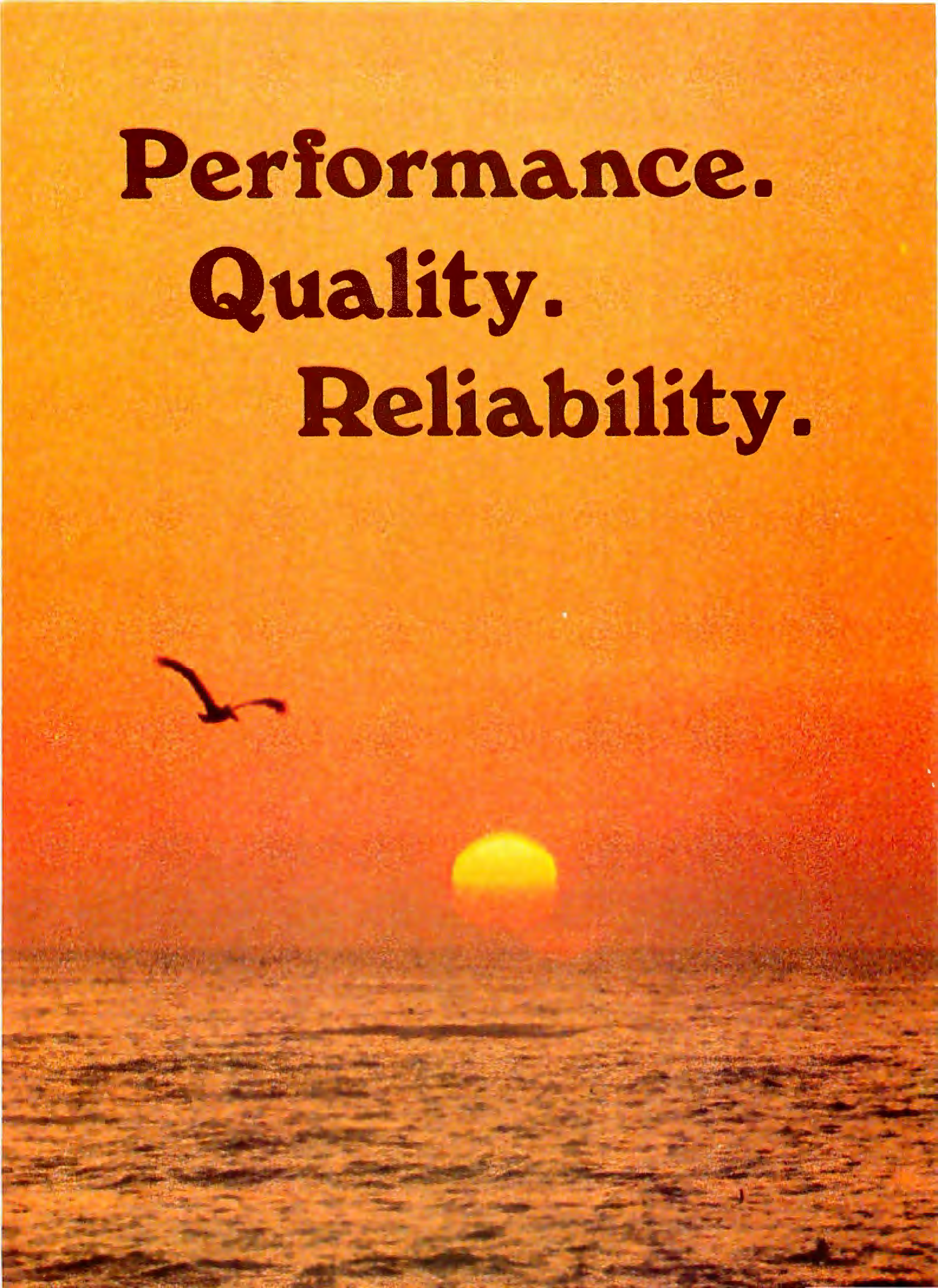
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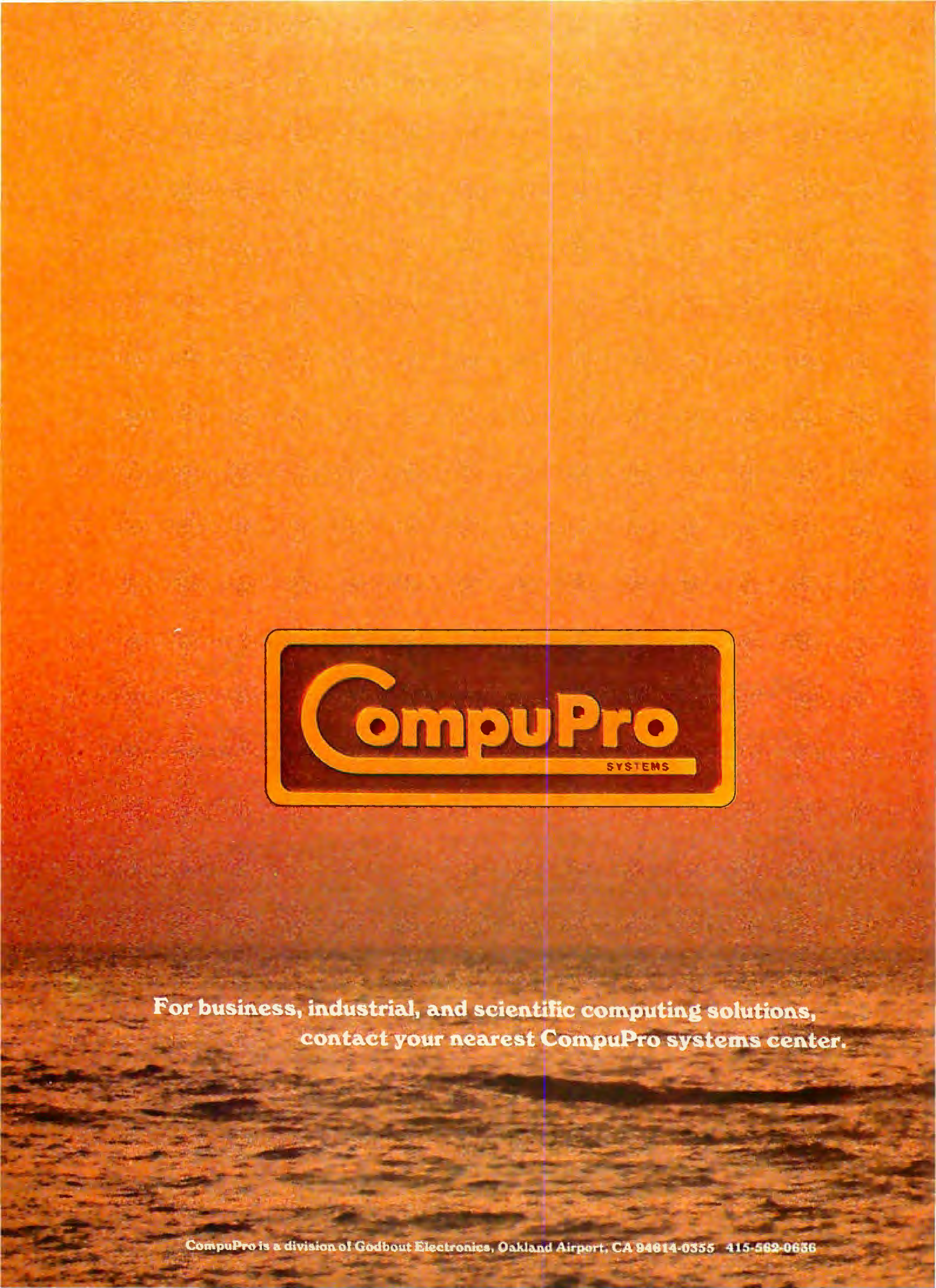
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Listing 1 continued:

```
Memory    Object    Statement         Source
Location  Code      Number            Code

FEF5 3E00     00860 ASAVE   LD A,00H ; RESTORE ACCM
FEF7 C3F7FE   00870 KEND    JP KEND
FEFA F5       00880 BASIN   PUSH AF
FEFB 2600     00890         LD H,00H
FEFD 2E00     00900         LD L,00H
FEFF 3A3AFF   00910         LD A,(LEN)
FF02 FE00     00920         CP 00H ; NO DATA HAS COME IN
FF04 282E     00930         JR Z,BEXIT
FF06 C5       00940         PUSH BC
FF07 D5       00950         PUSH DE
FF08 CD7F0A   00960         CALL 0A7FH ; GET BUFF ADDRESS
FF0B E5       00970         PUSH HL
FF0C D1       00980         POP  DE
FF0D 213AFF   00990         LD HL,LEN
FF10 0600     01000         LD B,00H
FF12 0E03     01010         LD    C,03H
FF14 EDB0     01020 PMOV    LDIR ; MOVE PARMS
FF16 213DFF   01030         LD HL,BUFF
FF19 1182FF   01040         LD DE,BBUFF
FF1C 3A3AFF   01050         LD A,(LEN)
FF1F 4F       01060         LD C,A
FF20 EDB0     01070 DMOV    LDIR ; MOVE BUFF
FF22 213DFF   01080         LD HL,BUFF
FF25 2238FF   01090         LD (CURR),HL
FF28 3A3AFF   01100         LD A,(LEN)
FF2B 2600     01110         LD H,00H
FF2D 6F       01120         LD L,A
FF2E AF       01130         XOR A
FF2F 323AFF   01140         LD (LEN),A
FF32 D1       01150         POP DE
FF33 C1       01160         POP BC
FF34 F1       01170 BEXIT   POP AF
FF35 C39A0A   01180 BACK    JP 0A9AH
FF38 3DFF     01190 CURR    DEFW    BUFF
FF3A 00       01200 LEN     DEFB    00
FF3B 82FF     01210         DEFW    BBUFF
0045          01220 BUFF    DEFS  69
0040          01230 BBUFF   DEFS 64
FE80          01240         END START
00000 TOTAL ERRORS

ASAVE   FEF5 00860   00640 00670 00730
BACK    FF35 01180
BASIN   FEFA 00880
BBUFF   FF82 01230   01040 01210
BEXIT   FF34 01170   00930
BUFF    FF3D 01220   01030 01080 01190
CURR    FF38 01190   00760 00820 01090
DMOV    FF20 01070
DOUT    FEAF 00450   00110 00130 00150
KBFIX   FECA 00640   00330
KEND    FEF7 00870   00320 00870
KEY1    FEDF 00750   00710
LEN     FF3A 01200   00780 00840 00910 00990 01050 01100 01140
NOSAVE  FEF4 00850   00900
PMOV    FF14 01020
RETX    FEC7 00600   00530
START   FE80 00170   01240
STATIN  FEBE 00540   00490 00510 00560
TABLE   FEA7 00360   00240
```

Text continued from page 100:

create a program file for the initialization routine. You will have to execute this program under TRSDOS READY before starting BASIC and loading the monitor program. The initialization program does the following:

- It sets the RS-232C protocol (word length, parity, bit rate, etc.) according to the setting of the sense switches on the Radio Shack RS-232C circuit board. (Be sure these switches are set to match your 6800 system's requirements.)
- It routes all BASIC printer output (LPRINT) to the RS-232C port.
- It uses the 25-millisecond (ms) interrupt of the TRS-80 expansion interface to check for any data transmitted from the MIKBUG system.

Here's a breakdown of the program's functional segments (numbers refer to source statement numbers):

20-430 Set bit rate as determined by switches, put a hook into the printer and keyboard DCBs (device control blocks), and return to TRSDOS.

440-620 Route all LPRINTs to the

Text continued on page 110

Listing 2: *The BASIC monitor program that makes the TRS-80 act like an enhanced MIKBUG terminal.*

```
100 ' MIKBUG MONITOR
110 ' WRITTEN BY ROBERT LABENSKI
120 ' WEST HARTFORD CONNECTICUT
130 '
140 CLS DEFINT A-Z CLEAR 5000
150 DIMS$(100) ' SOURCE
160 DIMOB$(100) ' OBJECT
170 DIMAD(100) 'ADDRESS
180 DEFUSR0=&HFEFA
190 COSUB 210  :GOSUB 240  :GOTO190
200 ' TRS KEYBOARD INPUT
210 A$="":A$=INKEY$:IF A$="@" THEN 260  ELSEIF A$<>"" LPRINTA$;
220 RETURN
230 ' 6800 INPUT
240 B$="":B=USR0(VARPTR(B$)) IF B<>0 S=INSTR(B$,"!"):PRINT; RIGHT$(B$,LEN(B$)-S
);
250 RETURN
260 'CMD PROCESSOR
270 INPUT"CMD=>";A$
280 IF A$="@" RETURN
290 IF LEFT$(A$,1)="D" GOSUB 360
300 IF LEFT$(A$,1)="G" GOSUB 400
310 IF LEFT$(A$,1)="L" GOSUB 510
320 IF A$="S" GOSUB 660
330 IF A$="H" GOSUB 690
340 IF A$="B" GOSUB 820
350 RETURN
360 'DUMP 32 BYTES
370 LPRINT "M";:W=90:GOSUB 440   LPRINT RIGHT$(A$,4)
380 W=200:FOR L=1TO16 GOSUB440  :B$="".B=USR0(VARPTR(B$)):PRINT RIGHT$(B$,3);:L
PRINT  NEXT L:PRINT GOSUB440   LPRINT "   ";
390 B$="":B=USR0(VARPTR(B$)):RETURN
400 ' G XXXX
410 LPRINT "M";:W=90:GOSUB440  :LPRINT "A048"
420 W=200:GOSUB 440  : LPRINT" "; MID$(A$,2,2):GOSUB 440  :LPRINT " ";RIGHT$(A$
,2):GOSUB 440  :LPRINT "    ";:GOSUB 440
430 LPRINT "G":W=20:GOSUB 440  :GOTO 390
440 FOR Z=1 TO W:NEXT Z :RETURN'WAIT LOOP
450 ' DEC TO HEX
460 C$="":X=INT(AD(Z)/256):GOSUB 490
470 X=INT((AD(Z)-(X*256))/16):GOSUB 490
480 X=INT(AD(Z)-(INT(AD(Z)/16)*16))
490 IF X>9 THEN C$=C$+CHR$(X+55) ELSE C$=C$+RIGHT$(STR$(X),1)
500 RETURN
510 'LOAD
520 IF OK THEN 560
530 INPUT "FILE SPEC'S >";A$:IF A$="" RETURN ELSE OPEN "I",1,A$:INPUT#1,OK,N
540 FOR Z=0TON-1:INPUT#1,S$(Z),OB$(Z),AD(Z):NEXT
550 CLOSE
560 LPRINT"M":W=90:GOSUB 440  :Z=0:GOSUB 450  :LPRINT "0";C$
570 PRINT "ADDRESS =>";C$:S=AD(0)
580 W=200:FOR X=0TON-1:IF OB$(X)="" THEN 640
590 IF S=AD(X) THEN 600  ELSE GOSUB440  :LPRINT "     ":GOSUB 440  :LPRINT "M":Q
=X:Z=X:GOSUB 450  :GOSUB 440  :LPRINT "0";C$:GOSUB 440  :X=Q:PRINT:PRINT"ADDRES
S=>";C$
600 FOR Y=1 TO LEN(OB$(X)) STEP 2
610 PRINT MID$(OB$(X),Y,2);
620 GOSUB440  : LPRINT " ";MID$(OB$(X),Y,2):NEXT Y
630 S=S+(LEN(OB$(X))/2)
640 NEXT X: GOSUB 440  :LPRINT "     "
650 PRINT" DONE ":GOTO 390
660 'SHOW SOURCE
670 IF OK THENFOR Z=0TON-1:GOSUB 450  :PRINT Z;TAB(6)C$;"   ";OB$(Z);TAB(22) S$(
Z):NEXT:RETURN
680 PRINT "NO SOURCE":RETURN
690 ' HELP SCREEN
700 PRINT">>> MIKBUG COMMAND'S  ( * PROMPT) <<<"
710 PRINT "  M XXXX    DISPLAY/MODIFY MEMORY"
720 PRINT"  G      EXECUTE PROGRAM POINTED TO BY PC (A048-49)
730 PRINT"  R   DISPLAY REGS ( CC BB AA XXXX PPPP SSSS )"
740 PRINT"  P/L PUNCH/LOAD ADDRESS A002-3 TO A004-5
750 PRINT:PRINT">>> MON6800 COMMANDS  (@ FOR CMD=>  PROMPT) <<<"
760 PRINT"  L  LOAD ASSEMBLED PROGRAM FROM DISK FILE"
770 PRINT"  DXXXX   DISPLAY 16 BYTES AT XXXX
780 PRINT"  GXXXX   EXECUTE PROGRAM AT XXXX"
790 PRINT"  S  SHOW SOURCE OF PROGRAM FROM DISK"
800 PRINT"  B SET (SX) RESET (RX) BREAKPOINT 0-9"
810 RETURN
820 'BREAK POINT PROCESSOR E$(10)=ADDRESS + INSTR
830 INPUT "(S)ET  OR (R)ESET NUMBER";A$:B$=LEFT$(A$,1)
840 IF B$<>"S" AND B$<>"R" RETURN
850 IF LEN(A$)>2 OR  VAL(RIGHT$(A$,1))>9 PRINT " BREAK POINT NUMBER INCORRECT":
RETURN
860 X=VAL(RIGHT$(A$,1))
870 IF B$="S" THEN 900
880 IF E$(X)="" PRINT " NO BREAKPOINT SET":RETURN
890 W=200:LPRINT "M":GOSUB 440  :LPRINT LEFT$(E$(X),4):GOSUB 440  :LPRINT " ",R
IGHT$(E$(X),3):GOSUB440  :LPRINT "    ":PRINT "ADDRESS WAS ";LEFT$(E$(X),4):E$(X
)="":GOTO 390
900 INPUT " ADDRESS ";E$(X)
910 W=200:LPRINT "M":GOSUB440  :LPRINT LEFT$(E$(X),4):GOSUB440
920 B$="":B=USR0(VARPTR(B$)):E$(X)=E$(X)+RIGHT$(B$,3)
930 GOSUB 440  : LPRINT " 3F":GOSUB 440  LPRINT "    ":GOTO 390
```

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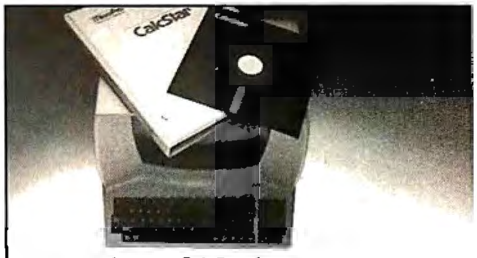

A glance at CalcStar features

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Text continued from page 107:

RS-232C interface.

630-870 On the 25-ms interrupt used by the keyboard routine, capture any data transmitted by MIKBUG. Nulls and other control characters are stripped off. The data are collected in BUFF for a maximum of 64 characters.

880-1180 The entry point BASIC uses to get the MIKBUG data. See statements 60-90 for the protocol.

1190-1240 Buffers and other required storage areas.

Once you've set up the system, you are ready to run the BASIC monitor program (listing 2). Start BASIC, ask for at least one file, and answer the memory-size question with an address at or below 65151 (if you change the origination address of the Z80 program, you'll have to change the memory-size answer, too).

We've already described the commands available in the monitor, so let's look at the function segments of the program (numbers refer to program line numbers):

100-180 Define variables and set up the machine-language subroutine calls.

190 Start the main program loop. Because the main loop and subroutines are in BASIC, the keyboard may feel "mushy."

210-220 Scan the TRS-80 keyboard and check for the "@" key. Input will be passed to MIKBUG or, in case of the "@" key, to the special command processor.

230-250 Process a special command. If you want to add any special commands, put them here.

360-390 Dump 16 bytes in hexadecimal by repeating the MIKBUG M command 16 times.

400-440 Load program counter and go (G*xxxx*).

450-500 Convert decimal to hexadecimal.

510-650 Load object code into the 6800 system. The code is transferred one byte at a time, and each byte is echoed in hexadecimal form on the TRS-80 screen.

660-680 Display the code currently in memory (source and object will be displayed).

690-810 Display a "help" screen.

820-930 Process (set or reset) a breakpoint.

A few words about the bit rate: the variable W determines how long BASIC will wait for a byte from the 6800 system. The value I have given is appropriate when you use 300 bits per second (bps). If you change bit rates, you'll have to change the value of W (for a higher bps, use a smaller value; for a lower bps, use a larger value). ■

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Technical Forum

Floppy-Disk Performance

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Athens 104, Greece

Dennis Nendza's article "Comparing Floppy-Disk Drives by Software Simulation" (see the May 1980 BYTE, page 130) contained the principles of drive operation and timing plus a comparison of a number of disk drives from various manufacturers.

Nendza's conclusions were:

- The performance of sequential read operations are practically the same for like-sized drives.
- There is a sizable difference between the predicted and actual performance of many drives.
- Despite the theoretical figures given by many manufacturers, actual floppy-disk performance is low.

In random operations, the situation is even worse. Since transfer efficiency is dependent on the file structuring and file searching involved, I will restrict my observations to sequential performance.

In attempting to explain the discrepancy between the theoretical prediction for reading 500 records (about 43 seconds) and the actual time (109 seconds), I noticed that Nendza's program assumes that the read head is in a random position before reading the next record in sequence. It is my belief that the random-position assumption is incorrect since the timing of the appearance under the head of each sequential record or sector is exactly known. In fact, if we assume that the software requires a period of time to transfer the record to memory and process it, when the head goes to read the next sequential sector it will have passed the beginning and will have to wait until the next revolution to continue the read.

If we make this assumption, we can estimate the time to read one sector to be equal to the time of disk revolution (about ⅙ second) for an 8-inch disk. Therefore, the

time required to read 500 records is 83.3 seconds. An extra one to two seconds is required for the initial seek, head load, and the subsequent track-to-track accessing (if not absorbed within the sector-waiting time). This gives a total read time of approximately 85 seconds for 500 records, which is much closer to the actual figure.

The question remains: Is this the best performance we can expect from a floppy-disk drive? Reading a 128-byte sector every 166 milliseconds (768 bytes per second) is very far from the theoretical floppy-disk transfer rate of 30,000 bytes per second. Looking at it another way, it's only an eightfold improvement over a cassette that operates at 1200 bits per second.

I ran across this problem when developing an 8-inch floppy-disk system for a minicomputer. I was told there was no way to improve the performance but decided to give it a try.

The most obvious way to improve the transfer rate is to increase the sector size (at the expense of departing from the IBM standard) and the memory requirements. This encouraged the choice of hard sectoring, allowing easy selection of multiples of the standard sector size plus an increased capacity per track of 32 standard-sized sectors rather than 26.

The selection of 256-byte sectors automatically doubles the transfer rate. Further improvement can be obtained if you are prepared to go as far as half-track sectors. This sacrifices about 2 K bytes of memory per opened file but results in an *eightfold* increase in transfer efficiency. However, it should be noted that this is not the best way to obtain fast transfer rates, because large record sizes not only waste memory but are also unsuitable for many applications.

Another alternative was therefore considered: make sure that the next sequential sector to be read is optimally positioned after the previous sector is read. Using this technique, sequential sectors are not dictated by the time needed for a complete disk revolution.

Since the processing time of the information retrieved from the disk varies, the time between the reading of sectors also is variable. In many cases, only record transfers are performed with little need for processing. Therefore, the time of sector processing should be no greater than the time required to read the sector (32 microseconds per byte). In the ideal situation, if the next sector to be read is positioned two sectors away from the previously read sector, one full track could be read in two disk revolutions.

If this method is used, you must depart from the "one every other" rule. In my application, I used the following format: each track was divided into 16 sectors of 256 bytes each. Access of sequential sectors was adjusted to one every three (i.e., the record/read sequence was 0,3,6,9,12,15,2,5,8,11,14,1,4,7,10,13, etc.; the numbers represent the physical location of each sector relative to the index hole). With this format, I obtained a transfer rate of one sector (256 bytes) every 30 microseconds, or about 8000 bytes per second.

The time available to transfer each sector from the operating-system buffer to the memory is 20 microseconds, which leaves ample time for processing the data. Also, since the sector number is continually monitored by the hardware, there is in most cases sufficient time to access the next track without waiting for another revolution of the disk.

This method works particularly well in applications where you have to frequently load large programs. For example, the 500 records mentioned in Nendza's article could be loaded in 8 seconds if the timing is not lost during access of the track, or in 11 seconds if one revolution is lost on each of the 20 tracks to be accessed.

I have to stress that there is still room for further improvement in the transfer ratio. For example, a variable spacing of sequential sectors can be adopted to suit various needs for record processing. Odd numbers of sectors per track can give the maximum transfer rate. Also, synchronizing dual drives can yield optimum disk-to-disk transfer performance.

The fact remains that the capabilities of the floppy disk have not been fully exploited. As it stands now, the most impressive figures remain in the specification sheets of the disk-drive manufacturers. ■

AC Motor Control

Simple Algorithms and Hardware

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Oslo 9 Norway

Connecting a microcomputer to an external device is an efficient way to acquire a realistic understanding of the possibilities offered by the microprocessor. As a teacher of computer science, I illustate techniques for interfacing such devices to a computer through a series of experiments performed by the engineering students in the laboratory. In most of these experiments some quantity (like speed or temperature) is measured, or some external device is controlled.

Ideally, the experiments should be interesting and instructive, yet not too complex or time consuming. Also, they should involve components and devices that are easily obtainable and not too expensive. I believe the following two applications will satisfy these demands.

Measuring Rotational Speed

The hardware used to measure rotational speed is shown in figure 1. An electric fan is placed between a phototransistor and a light source (an ordinary incandescent lamp). Each time the light beam is interrupted by the rotating blades of the fan, the output of IC1, the 74LS14 Schmitt trigger, goes low. As a result, the input line to the computer, called PHOTO in the figure, goes low. The pulses thus generated are counted for a set duration. I use a fan with five blades, and the number of rotations per second will then be directly given by the number of pulses counted during 1/5 second.

Selecting a suitable phototransistor should not be difficult; I have tried several common types, and they all worked satisfactorily. If necessary, you can modify the resistor value in figure 1.

You may find it convenient to mount all components on a breadboard with spring-type connections. The breadboard may be connected to the computer with a ribbon cable. To perform the experiment, the breadboard is held in such a position that the phototransistor "sees" the light source between the fan blades. Spurious light sources should be kept away from the phototransistor.

Of course, to measure the speed of a motor in an actual application, a somewhat different arrangement would have to be used. For example, a small disk, either perforated or with alternately transparent and opaque segments, could be attached to the motor shaft. Or a special optical switch, containing an LED (light-emitting diode) and a phototransistor in the same unit, could be used. However, these more sophisticated approaches tend to require mechanical arrangements that are harder to set up and get working. For experimental purposes, I prefer the simple use of a fan. (After all, the aim of the experiment is to illustrate principles, not to produce commercial equipment).

Obviously, the program for measuring time and counting pulses will depend on the computer you use: its language, input/output ports, clock frequency, etc. Whether the computer is based on the 6502, the Z80, the 8085, or some other microprocessor, writing the assembly-language program for this experiment is an instructive exer-

Number	Type	+5 V	GND
IC1	74LS14	14	7

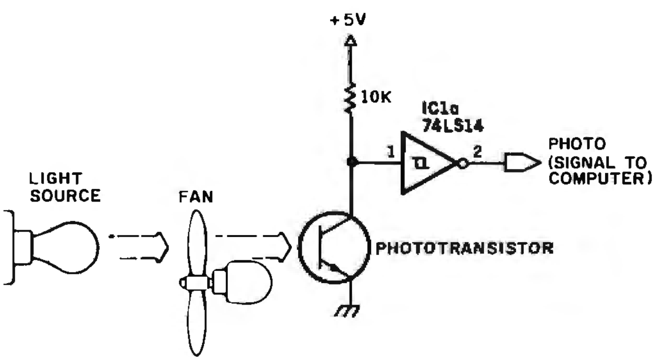

Figure 1: *A sensing circuit for measuring rotational speed. The blades of the fan cast a shadow on the phototransistor as they pass between it and the light; the signal thus created is conditioned by a 74LS14 Schmitt trigger prior to being presented to the computer.*

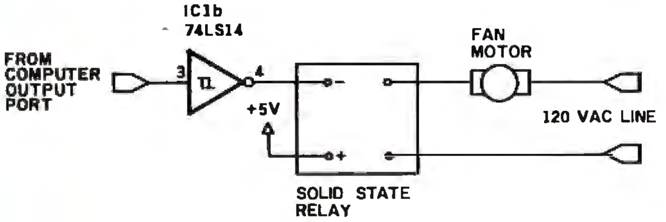

Figure 2: *The interface used to turn the fan motor on and off. A solid-state relay is simply driven from the computer's output port via a 74LS14 Schmitt trigger. This circuit is used in conjunction with the one shown in figure 1 to form a closed-loop control system. If the fan speed is too fast, the motor is turned off; if it is too slow, it is turned on.*

cise. I will present a fairly detailed algorithm here, leaving the actual programming up to you.

1. Initialize the time counter to 200 decimal. (Use a register for this purpose. When the measurement starts, the time counter will be decremented every millisecond (ms), so that when zero is reached, 1/5 second has elapsed.)
2. Initialize the pulse counter to zero. (Use a register as a pulse counter.)
3. Read PHOTO. Is it low? If yes, go to 3. (In steps 3 and 4 the input line is sensed continuously to detect a high-to-low transition. When this occurs, the measurement starts.)
4. Read PHOTO. Is it high? If yes, go to 4. (See the preceding comment.)
5. Increment the pulse counter. (A fan blade is now cutting the light beam.)
6. Call a delay subroutine to obtain a 1-ms delay. (The subroutine should execute a delay loop of 1 ms duration.)
7. Decrement the time counter. Is the result zero? If yes, go to 13.
8. Read PHOTO. Is it low? If yes, go to 6. (Low means that the fan blade is still interrupting the beam.)
9. Call the same delay subroutine as above.
10. Decrement the time counter. Is the result zero? If yes, go to 13.
11. Read PHOTO. Is it high? If yes, go to 9. (Repeat from 9 while waiting for the next fan blade.)
12. Go to 5.
13. The measurement is now complete. The pulse counter contains the number of times the light beam has been cut by the fan blades during 1/5 second. Display the result, and repeat from step 1. The execution of the program may terminate here if only a single measurement is required.

Note that if your computer is equipped with a programmable interrupt timer, this device can be used as a real-time clock. Thus, an interrupt timer may provide an alternative to using a delay subroutine for time measurement.

Controlling a Motor

Several methods are available to control the rotational speed of a motor. One of these is sometimes called "on-off control." Admittedly, this technique does not regulate the speed with great precision under all conditions. It is, however, the simplest method, and for this reason it will be used here.

The "on-off control" method measures the motor speed periodically and compares it to a desired value. If the motor runs too fast, it is turned off. If it runs too slowly, power is applied. Thus, this experiment will demonstrate the principle of a closed-loop control system, where the input sensed by the computer is used to determine the control output. This experiment also provides an example of how to interface AC appliances to a computer.

A phototransistor and a fan are used, as in the first experiment. However, in this case the fan is connected to the AC outlet through a solid-state relay, as shown in figure 2. The fan motor is turned on and off by sending 1 and 0, respectively, to the output port. A Schmitt trigger is used to drive the relay. Many other gates could drive the relay equally well, but the 74LS14 contains six Schmitt triggers. Many models of solid-state relays are available, with various current ratings, and most of them can be used for this experiment.

As in the previous experiment, the actual writing of the program is left up to you. The program should operate as follows:

1. Initialize the time counter to 100 decimal. (Note that a relatively short measuring period is chosen, in order to obtain a well-regulated speed. In this example 1/10 second is used.)
2. Initialize the pulse counter to zero.
3. Read PHOTO. Is it low? If yes, go to 7.
4. Call a 1-ms delay subroutine.
5. Decrement the time counter. Is the result zero? If yes, go to 12.
6. Go to 3.
7. Increment the pulse counter.
8. Call the delay subroutine.
9. Decrement the time counter. Is the result zero? If yes, go to 12.
10. Read PHOTO. Is it high? If yes, go to 4.
11. Go to 8.
12. Turn on the motor if the rotation is too slow; turn it off if the rotation is too fast. (The value of the pulse counter is compared to a value you have stored in a memory location before running the program. If the rotation is too slow, 1 is sent to the output port. Otherwise 0 is sent.)
13. Repeat from step 1.

When the experiment is performed, various speeds should be tried, high as well as low. You may also try to vary the load by applying moderate pressure to the motor shaft, if the design of the fan permits this. ■

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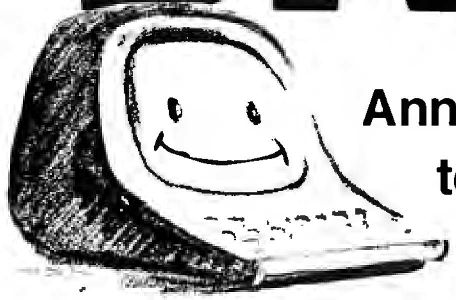

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Customized Versions • TRS80 Mod II, TRS80 Mod III, APPLE, OSBORNE, INTERTEC, VECTOR , ZENITH

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The RCA VP-3301 Data Terminal

Tim Daneliuk
4927 N Rockwell
Chicago, IL 60625

With the cost of most computer hardware decreasing, RCA's introduction of an inexpensive data-entry terminal hardly comes as a surprise. For a modest investment, the VP-3301 delivers many features formerly available only on more expensive terminals.

The terminal comes complete with an RS-232C interface and a 20-milliamp (mA) current-loop interface. It is capable of directly driving a standard television monitor, or it can be connected to a television receiver if an RF (radio-frequency) modulator is used.

Physical Features

The VP-3301 is small and lightweight enough to fit into a briefcase for use as a portable/remote data-entry terminal. The keyboard is a flat membrane type in the standard 58-key typewriter format, and two-key rollover is also provided. The unit has two extra keys that can activate switch closures for controlling user-supplied hardware. The switches are rated at 30 volts, 0.2 ampere, and 1 watt maximum.

The terminal also includes a small audio amplifier and speaker that can provide audio feedback when a key is pressed. A slide switch on the rear of the unit can turn this function off. With the control and escape keys, you can program the speaker and amplifier to produce a wide range of tones and sounds.

The terminal can interface to a standard RS-232 device or to a 20-mA current loop through a 25-pin subminiature "D" connector located on the back of the unit. Included as part of the RS-232 interface is a group of switches that control the serial port operating parameters and certain video-display characteristics. Using these switches, you can choose from:

- uppercase only/uppercase and lowercase
- even/odd parity (RS-232)
- mark/space (current loop)
- two stop bits/one stop bit
- full duplex/half duplex
- enable/disable control features
- display/no display of control characters
- 40/20 characters per line (24/12 lines on screen)
- current loop/RS-232
- local/line
- data rate (110 to 19,200 bps)

A small AC adapter comes with the terminal. To incorporate the terminal as a more permanent part of a larger system, you need only provide 8.3 volts DC at 900 mA.

Operating Features

One of the strengths of the VP-3301 is its flexibility; many options can be exercised from the keyboard under

At a Glance

Name
RCA VP-3301 Data Terminal

Use
Data entry and communication

Manufacturer
RCA
New Holland Ave.
Lancaster, PA 17604

Price
$369

Dimensions
13.1 inches long by 7 inches deep by 2 inches high

Features
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Hardware needed
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Hardware options
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software control. For example, you can redefine any character on the keyboard to display custom characters on a 6 by 8 matrix. Up to 128 characters can be redefined at any one time, allowing you to use almost any key on the keyboard to make the alphanumeric or graphics character of your choice appear on the screen. Similarly, foreground/background color, sound-generator pitch and dynamics, cursor operation, and reverse video can all be controlled from the keyboard.

A beeping sound that signifies a data input overrun makes the terminal particularly useful for remote data-entry or timesharing applications.

The VP-3301 offers an impressive array of graphics- and video-related features. The character set is suitable for word processing, with lowercase and true descenders. You can select either 40 characters per line and 24 lines per page, or 20 characters per line and 12 lines per page. The cursor can be on, off, or blinking. The terminal also offers a choice of eight colors or seven levels of gray for both foreground and background video, and the color parameters can be redefined in the middle of a line.

The terminal does not, however, allow character size to be changed in the middle of a line. For example, if you change from 20 to 40 characters per line in the middle of the screen, the change will affect the entire screen, not just the subsequent characters.

You can also use the keyboard to program the terminal's sophisticated sound generator. The choices include pitch over about four octaves on the musical scale and loudness of tone. A white-noise generator is available for various sound effects.

Conclusions

I used the RCA VP-3301 in conjunction with an RF modulator, color television receiver, and 300-bps acoustic modem to access the computer facilities at a university in Chicago. Although it is difficult to second-guess a manufacturer's reasons for doing things a certain way, I did have a few problems with the terminal. For example, the VP-3301 is very limited in timesharing applications because it lacks a second serial or parallel port for printer support.

In addition, I would gladly give up all the video-display options in favor of an 80-character-per-line display format. I also question the usefulness of color graphics, as you can buy a complete color computer system for about the same cost. Because the graphics on the VP-3301 are not suitable for serious industrial-quality displays, perhaps RCA should have made the terminal more compatible with remote computing applications.

Despite the thin overlay that helps you feel the position of the keys, I found the flat membrane keyboard really cumbersome to use. I would gladly trade it for a standard keyboard. The membrane keyboard does, however, have

Circle 182 on inquiry card.

Circle 233 on inquiry card. →

the advantage of being impervious to moisture, dust, and other contaminants because it is completely sealed.

Most disturbing, I found the documentation for the VP-3301 poor to awful. To be fair, the manual I used was only a preliminary edition, which may explain its incoherence. Although the manual did cover all facets of the terminal, it lacked complete examples, did not clearly explain many of the control and escape sequences, and contained almost no technical information. It did include interfacing schematics.

Despite these drawbacks, the terminal provides good performance for the price. RCA wins high marks for the construction of the VP-3301, a well-built piece of hardware that promises to remain trouble-free. None of its problems is insurmountable, and the terminal offers enough versatility to find its way into many diversified applications. ■

Photo 1: *The RCA VP-3301 Data Terminal.*

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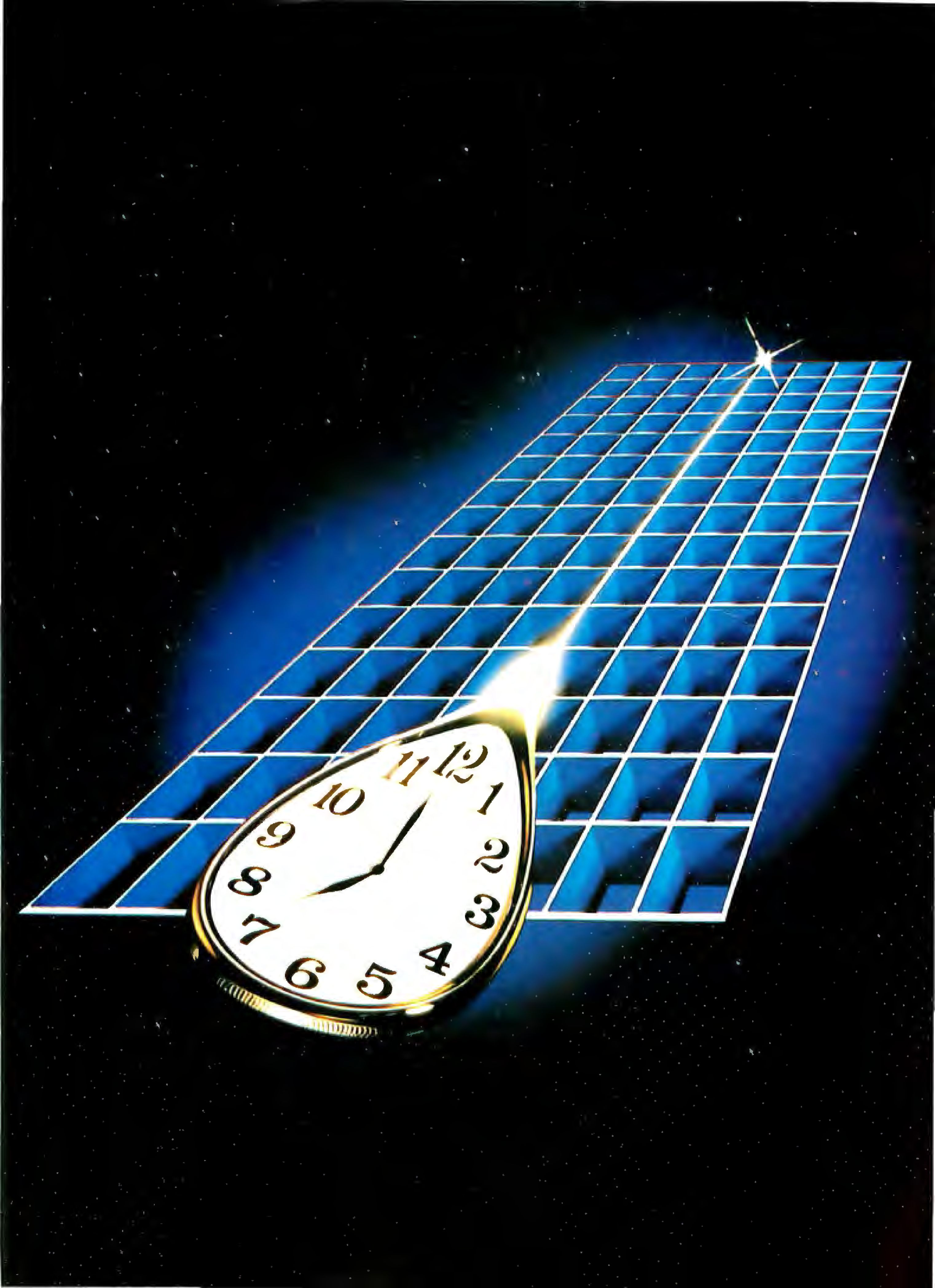

Operating Systems, Languages, Statistics, Pirates, and the Lone Wolf

Jerry Pournelle
c/o BYTE Publications
POB 372
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"People do strange things," said my mad friend Mac Lean. "They invent things like this new operating system, OS-1."

"You mean it doesn't work?"

"No, it works fine," he said. "And it's about as useful as a chocolate-covered wristwatch. Or maybe a triple hernia. If you like to play with operating systems, and God knows I do, OS-1 will give you hours of delight. But if you want to *use* it, you get hours of tedium."

"Why? Isn't it like Unix?"

"Well, yes, it is, sort of."

"But then why isn't OS-1 useful? Everyone likes Unix . . . ."

"Do they? Well, maybe a lot of programmers do, as they ought to. I'm not so sure other users are going to like Unix all that much, but maybe they will. Besides, OS-1 isn't *quite* Unix. OS-1 has a tree-structured directory system, but there's no mechanism for finding a file in there unless you've kept lists. And you can't make lists. Although the 'SET TTY' command will set the screen width, it won't set the printer width, so you can't even list for hard copy unless you've got a 132-wide printout device. If you don't remember what's in those directories, you'll never find the files!"

"What, never?" I asked.

"Well, hardly ever. The idea is that you can have multiple directories, so a lot of different users can each have their own, right? But floppy disks are too small for that kind of structure. Look, your utilities occupy most of one disk, and your operating system and its directories take up another disk. On top of that, the OS is so big that you've only got about 32 K bytes of RAM left over. That's not enough to work in. The PL/I compiler can't do much in that. Whitesmiths' C compiler won't even start to work. Leor Zolman's [excellent!] BDS C compiler hasn't got room to breathe. What use is a Unix-like system that won't let you compile C programs?"

I still wasn't convinced. "Look," I said. "OS-1 is supposed to have all kinds of nifty features taken from Unix . . . ."

"It almost does," my mad friend said. "The notion behind the Unix system, with pipelines and all that groovy stuff, is great. Unix treats *everything* like a file, and you can build 'pipelines' from your directory to the device you want the file to go to, or between programs. But OS-1 doesn't do that. Instead, it has pseudopipelines, with intermediate file structures. Why do that? Better to use CP/M and a submit program than that. With OS-1 you just don't have enough RAM, and you have trouble keeping track of where you are, and the command strings are long and tedious if you want to look at other directories. They really tried hard, and you ought to give them an A for effort, but only about a C for usefulness."

"And if we go to 16-bit machines?" I asked. "Such as the 8086? Where we've got plenty of RAM to play with, and hard disks and fast access and . . . ."

He shrugged. "Who knows? But I suspect that if you want a Unix-like system, you might as well have Unix and be done with it. Why compromise with something else?"

And on reflection I have to agree. OS-1 is a heroic effort, but it somehow just doesn't make it.

Future Operating Systems

So what *will* be the operating system for future micros? Will we, as Chris Morgan wrote in his recent editorial "The New 16-Bit Operating Systems, or, The Search for Benützerfreundlichkeit" (June 1981 BYTE, page 6), "get it right the second time"? Or are we stuck with CP/M forever and aye?

Well—first, what does "stuck" mean? For all its problems—and Lord knows it has plenty—CP/M isn't all that bad, for *users*. Programming hackers really hate it, but true hackers hate almost anything they didn't grow up with. Users don't know some of the inconveniences of CP/M. Worse, most users don't know all its nifty features because of the wretched documentation for which Digital Research is notorious, but CP/M *is* fairly easy to learn and use, even for beginners. It gets the job done.

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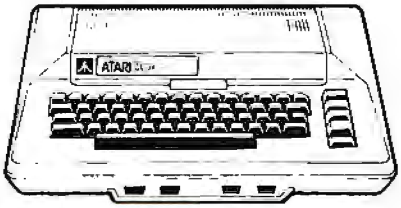

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advertised systems, one conclusion is plain: any popular system of the future will have to be upward compatible with CP/M, because there's just so much good software running under CP/M. Digital Research did us all a good turn by coming up with something approaching a *standard* in this field. I remember when we had to use F-DOS.

And then there are the CP/M utilities. You don't have to understand CP/M, as long as someone else does. I've mentioned the CP/M User's Group (CPMUG) before; it's an outfit that distributes all kinds of nifty utilities, like COPY routines, and FAST (which speeds up CP/M 1.4), and the like. The problems with CPMUG are selectivity and updating: there are more than 50 disks in the

Items Reviewed

Workman & Associates
112 Marion Ave.
Pasadena, CA 91106

CP/M Disk Utilities	8-inch single-density disk	Disk I $27.50 Disk II $27.50

Ecosoft
POB 68602
Indianapolis, IN 46268

Microstat	8-inch CP/M or 5-inch North Star disk	$250

Software Labs, Inc.
735 Loma Verde
Palo Alto, CA 94303

OS-1		price information unavailable

Ashton-Tate
Suite 1510
3600 Wilshire Blvd.
Los Angeles, CA 90010

dBASE II	8-inch CP/M	$700

Lobo Drives International
354 South Fairview Ave.
Goleta, CA 93117

LX-80 (expansion interface for TRS-80)		price under $1000 as tested
LDOS (operating system for TRS-80)		$169

Digital Research
POB 579
Pacific Grove, CA 93950

PL/I-80 with LINK-80 linker		$600

Book Reviewed

Winston, P. H. and B. K. P. Horn.
LISP
Reading, MA: Addison-Wesley
Publishing Company, 1976 — $11.95

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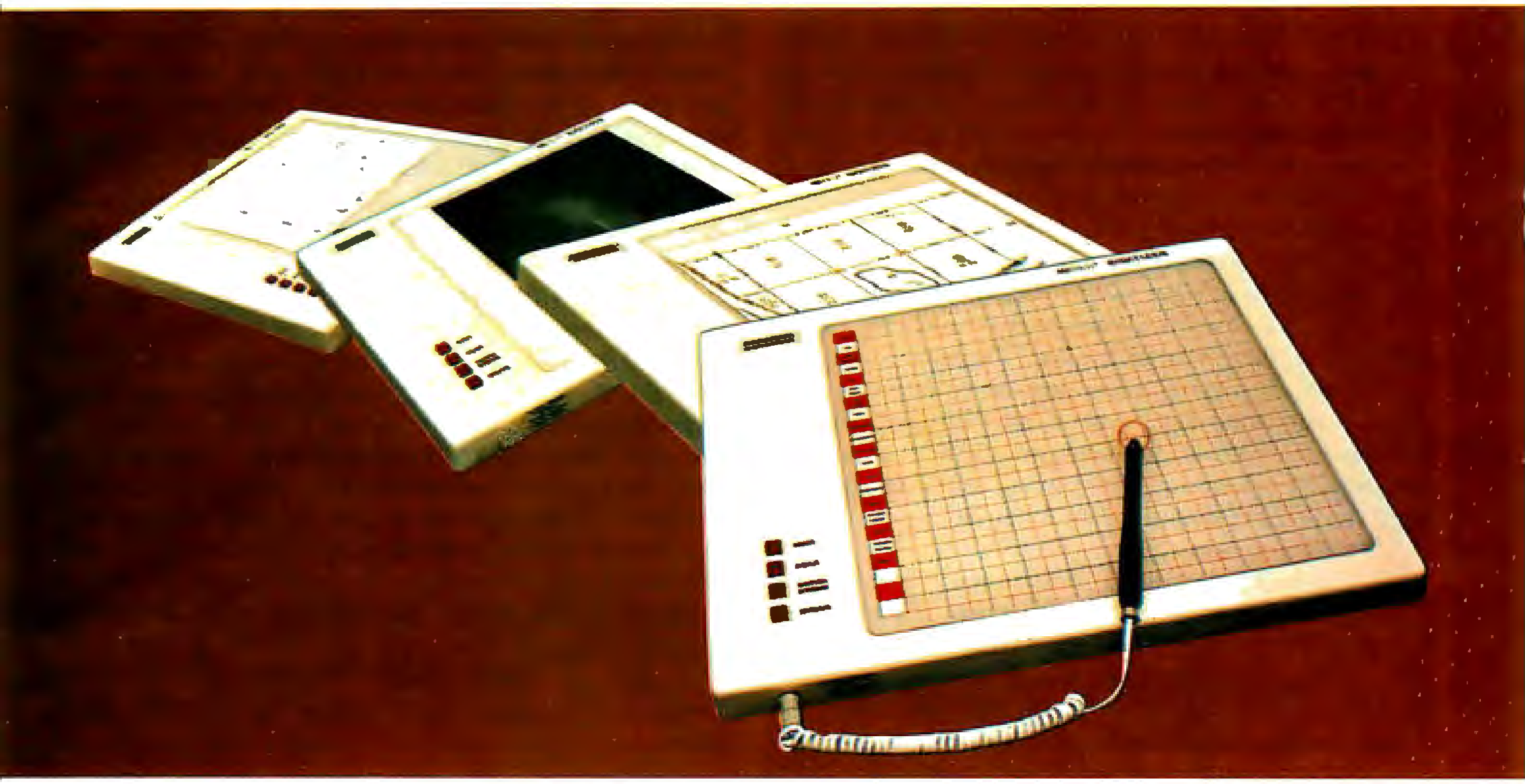

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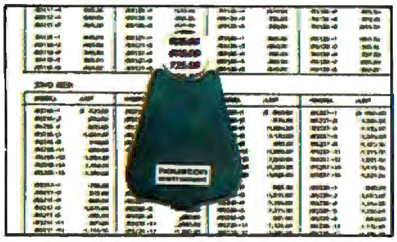

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CPMUG library, most filled with junk, useless games, or obsolete versions of programs since updated.

There are other sources of utilities. Various user networks distribute all kinds of nifty programs—modem emulators, catalog programs, library routines, you name it. And these get revised all the time. So how could you tell which ones to use?

The answer is, you couldn't—until Barry Workman, of Workman & Associates, came along. Barry sifts through the CPMUG and other public-domain sources and puts together disks of utilities, which he'll sell for $27.50 a disk. Right now he's got two such disks.

"Utility Disk One will always be the most useful CP/M utilities I can find," Workman says. "The latest and fastest copy routines, command-line processors, directory programs, a good modem program to use with The Source or Micronet or whatever. Comparators and filters, stuff like that. Ward Christenson's disk catalog utility, which is by itself worth more than the disk if you don't have it."

"How do you select the programs?"

"Mostly I ask people like you what you'd like to have."

The documentation on the Workman disks is adequate, generally better than what was on the CPMUG disks. At least it had better be: Barry, by supplying quantities of a wonderful liquor called slivovitz, which he finds in some unknown place, gets me to go over the stuff for him. I do *not* rewrite it, but I do smooth out some of the ambiguities.

Workman's Utility Disk Two has Ward Christenson's disassembler, some comments on how disassemblers work, and instructions. It also has some other utilities probably more useful to programmers than users, although again Workman has tried to keep things simple and provide what he thinks will be most useful.

I can't list exactly what's on each of the disks, because that changes according to what Barry thinks is the most useful selection he can put together each month. He does try to send out the latest versions of the various utilities as he gets them.

The Workman utilities are public-domain programs, and almost all of them could be obtained by swapping with other people—for that matter, the only copyrighted materials on the Workman disks are some documentation files. The price may be just a bit steep, but Barry says he can't afford to produce the disks for less. He's selling them as a service; he won't get rich at $27.50 per disk. If your time is valuable, the utilities are worth the price.

The Workman utility programs are for 8-inch soft-sectored, single-density CP/M systems only, the kind of stuff that my friend Ezekial, who happens to be a Cromemco Z-2, likes. But of course I have another computer. . . .

Lobo to the Rescue

It was at the West Coast Computer Faire. I was talking to Roger Billings, president of Lobo Drives International, about their hard disks.

"I'm in big trouble," I said.

"Why?"

"Here I am at the Faire. I'll be bringing home a lot of new software. Automated Simulations has some great new games. And when I get home my kids are going to kill me, because Ezekial is running fine, but *their* computer isn't. And my name is mud if I can't get that TRS-80 going again . . . ."

"What happens?" Roger asked.

"Won't boot. Drives spin, but the system won't come up."

"Hmm. Can we come see you next week?"

"Sure," I said, and promptly forgot the conversation, there being so much to see and do at the Faire. Precisely a week later I was talking on the telephone when the doorbell rang. Here at Chaos Manor that's a big deal. Dogs bark and madly skid on rugs to the door, followed by shouting boys trying to restrain the dogs. Anyone who waits for the door to open is *determined.*

Eventually I got off the phone to find Eliot Lane, Lobo's product engineering manager. He had a van outside. "I've come to fix up your TRS-80," he said.

And fix it up he did. The first step was to replace my Percom disk drives with two new Lobo drives. That turns out to be easy: Lobo drives have the cable connector on the back where you can get at it without taking out

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screws (and I wish the Percoms were built that way; it's bloody easy to have one of the power cables come loose inside the drive when you put it together after connecting the data cable). But when we tried booting the system, nothing happened. At least we knew it wasn't the fault of the Percoms, which had always worked well and still do, except for the inconvenient placement of those cable connectors.

Next we installed Lobo's LX-80 expansion interface to replace my TRS-80 interface. My TRS-80 Model I is one of the intermediate versions; in addition to the ribbon cable (with flat booster box) connecting the keyboard to the expansion interface, there's also a round cable—which makes it pretty crowded and hard to get at the RESET button. There's no connection for anything like that on Lobo's LX-80.

"Just ignore it," Eliot said. He proceeded to connect the LX-80. It didn't work, so we took apart the TRS-80 keyboard, and lo, there was a broken wire in the ribbon cable connecting the two halves of the system. Eliot soldered jumpers around the broken parts and tried again, and all worked fine.

It still does. We're now running the Lobo LX-80 with LDOS operating system, and both work splendidly. The disk drives are a pair of Lobo 5¼-inch and another pair of Lobo 8-inch; all four are running at double density and doing fine, and with this system you can move everything from small disks to big ones and back again, giving you a *lot* of storage.

Now, about the LX-80: this is an excellent product. It's well made, in a metal case, with precisely located components. The insides *look* professional, as opposed to the TRS-80 expansion interface with its jumpers and cut traces and soft plastics and such. The one I've got is the full-blown model, with two serial ports and a parallel port, and cable outlets for both 5¼- and 8-inch drives, and 32 K bytes of memory. There's an on-board PROM (programmable read-only memory) that brings the system up into LDOS. It supplies power for all the ports from a single wall plug that works through a positive action switch. There's a good pilot light. The LX-80 comes with documents that explain what's going on. It connects to your TRS-80 with a single cable and with no booster-box. You don't need the various kludges that Radio Shack threw in to keep its Model I working.

The LX-80 will reformat and run both 5¼- and 8-inch disks, at either single or double density. It will let you transfer files from single density to double density. It has an external data separator (which separates data signals from timing signals), so that you don't get the disk errors for which TRS-80s are notorious. (The TRS-80 system uses the data separator internal to the disk-controller chip; even Western Digital, which makes the chip, recommends that you don't do that.)

In other words, I like the Lobo LX-80.

The problem is that it's expensive; the model I tested would probably retail for just under $1000. It's really bet-

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ter than the computer it supports. Lobo was a bit late getting the LX-80 on the market. Most of the people who need one may already have a Radio Shack expansion interface, and now Percom will sell you a doubler to allow double-density operations and an external data separator to add to your Radio Shack interface. If you're using the TRS-80 Model I, and you're thinking about an expansion interface and disk drives, the LX-80 won't cost much more than the Radio Shack plus Percom's separator and doubler. And if you want quiet, trouble-free operation, if you want to be *sure* your expansion interface isn't giving you trouble, and you're willing to pay for that assurance, then the LX-80 is a very good way to go. Lobo builds quality products, and it stands behind them.

There's one more problem with the LX-80: it won't work with George Gardener's Omikron Mapper. The Mapper is a device for letting you run CP/M with a TRS-80 Model I; I reviewed the Mapper more than a year ago (see "Omikron TRS-80 Boards, NEWDOS+, and Sundry Other Matters," July 1980 BYTE, page 198), and I'm pleased to say ours has never given us any trouble. (True, the broken wires in my TRS-80 probably came from the flexing during installation and removal of the Mapper, but after all, I did that about 20 times in order to put in other stuff for test, so that hardly counts against Omikron.) There's no reason why the LX-80 and the Omikron Mapper *can't* work together; it's just that the LX-80's PROM is geared to disable certain parts of the TRS-80, and to readdress some of the system's ports. A good software expert could make the two work together, and I think Lobo ought to consider doing that. The ability to convert the TRS-80 Model I for CP/M and still run regular TRS-80 stuff as well adds greatly to the computer's value.

Lobo's Disk Operating System

The TRS-80 used to drive me mad because of the operating system. I always used NEWDOS instead of Tandy's standard TRSDOS. Now there's LDOS, Lobo's disk operating system for the TRS-80 Model I. Although I still think it's needlessly complex, LDOS is now the best TRS-80 operating system going. It's a *lot* better than TRSDOS.

Although it was designed to work with the LX-80, LDOS will work fine with a TRS-80 Model I and a Radio Shack expansion interface. With LDOS you can run 40 tracks per drive if your disks can do that. (TRSDOS is limited to 35 tracks no matter what your disks are.) LDOS will also work with the Percom doubler and data separator. LDOS knows whether your disks are formatted for single or double density and stores the files accordingly. You don't need to keep track of that, or to use special commands.

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User's Column

A major feature is that files created with LDOS can be transferred from a TRS-80 Model I to a Model III, and they say you can get from a Model I to a Model II also, although I'm not sure how.

LDOS is superficially similar to TRSDOS. It has all the inanities about passwords and protection levels and such that TRSDOS sticks us with. Fortunately, though, with LDOS you can get rid of all that stuff—as you should. Anyone who trusts those "password" and "protection" systems should get his head examined. Any of those systems can be defeated by any half-competent programmer.

You get all kinds of utilities with LDOS: a debugger, a job-control language, and a patch to Microsoft (Tandy) BASIC that allows you to renumber selectively, use random-access files, step through a BASIC program one statement at a time, and cross-reference programs. There's also a spooler to allow printouts while you work on other programs.

The system is easier to use than TRSDOS, but you do have to learn it. The LDOS documentation is fairly clear, but dense in places; you really have to read through most of the document, then go back and start over. The usual hacker's way of plunging in and doing this and that while thumbing through the manual probably won't work—at least it didn't for me.

On the other hand, LDOS comes with a toll-free number that you can call to get help. I called it several times and found myself speaking to systems programmers who really know LDOS. They tended to think I was nuts—the answers to almost all the questions I had were right there in the manual (and if I'd read through the manual instead of jumping right in like any hacker, I'd have known that). They also tended to expect me to know more than *I'd* expect a typical user to know; but then I had an early copy of LDOS, and they hadn't had a lot of experience with naive questioners yet. By now I bet they know better.

The documentation is nothing to brag about, but it's adequate, provided that the reader is patient and will go through it twice. There are plenty of examples, most of them informative. It needs a good index and an analytical table of contents and a better introduction to the "philosophy" behind LDOS, but you can, with patience, learn the LDOS system from the manual. That beats the daylights out of some system manuals I know of.

One reason LDOS is complex is that it really is an operating system not just for the disks, but for the whole TRS-80. It has the ability to set logical devices, and trace programs, and do lots of neat things you don't associate with the TRS-80. LDOS with the LX-80 gives you a fairly powerful system, with a real monitor just like regular computers, and even with the Tandy interface you still get a lot more control over your machine than you get with either NEWDOS or TRSDOS.

As far as I can tell, you can run any programs under LDOS that you can run under TRSDOS, except for those

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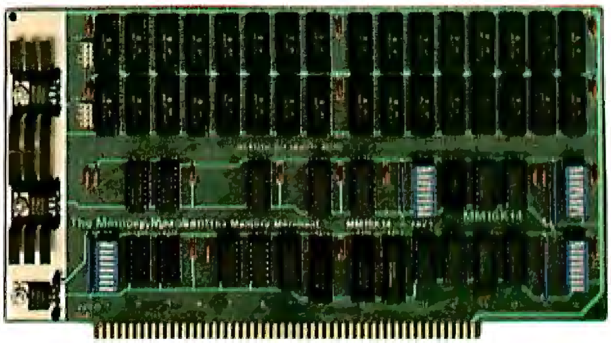

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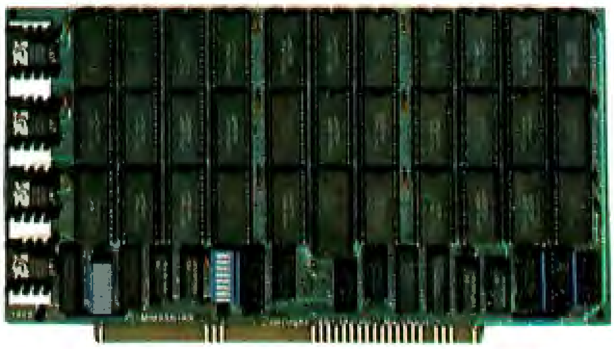

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User's Column

programs that are artificially protected with goofy sectoring and other strange tricks to keep you from copying them. And anyone who uses such programs is, in my judgment, not doing the profession much of a favor to begin with. On that, more later.

The bottom line on LDOS is that I like it. It's kind to the user, and it's a fairly complete operating system. I still prefer to convert my TRS-80 Model I to CP/M, but I'll keep LDOS around to use when I'm running it as a TRS-80, since it will work on Omikron's Mapper if you get an LDOS patch from Omikron.

Code and Swash

"Do you read BYTE?" my mad friend asked.

"Stupid question. I *write* for BYTE."

"What's that got to do with reading it? Anyway, did you read the editorial on software piracy?" (See "How Can We Stop Software Piracy," by Chris Morgan, May 1981 BYTE, page 6.) I admitted that I had.

"What did you think of it?"

"Didn't think about it a lot . . . ."

"You should. It's dead wrong," Mac Lean said. "Look. Your editor, Chris Morgan, says that software piracy is a major problem . . . ."

"And it really isn't, for users," I mused.

"Well, it's sure going to be," Mac Lean said. "Because look what they're doing. Making programs complicated and uncopyable to 'protect' the publishers. What that really does is make the user's life impossible. Disks are fragile things. I've *got* to have copies of them. Suppose I have a brownout. Ever have that happen to you?"

I nodded. Once we had a power failure while I was copying a disk. It took Mac Lean and a program called SPAT and a *lot* of work to recover most of what was on either disk.

"And it's worse than that," Mac Lean said. "They worry about pirates, and the result is that the programs are fragile. They can't recover from mistakes, because instead of error traps they've put in some kind of 'security'."

And he's right. The more I think about "uncopyable" programs, the more I hate the idea. I wouldn't bet any part of my income on an "uncopyable" program—and I'm unlikely ever to recommend one in this column.

But, then, how do we protect the rights of programmers?

Rights to what? If you mean the right to several hundred bucks for a program, why should we protect that? I mean, if people can get that for a program, more power to them, but why is it my concern to help publishers get that much? I *want* the price of software to come down.

"But," I mused, "if the price comes down, will we still get good software?"

My mad friend chortled. "Ever meet a true hacker who didn't write software? True, they won't do adequate *documentation*, they never do no matter what you're paying, but try to stop them from writing programs."

And of course he has a point. There's another argument: that software takes a long time to write, maybe

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User's Column

months and months or even a year, so doesn't the programmer deserve high prices?

Well, it takes me a year or so to write a book, and I don't notice anyone getting $400 per copy. And as for piracy, I even pay taxes to support public institutions whose purpose is to lend my books *free*. Yet I'm not starving, and neither are my publishers. The average paperback book sells about 40,000 copies, at perhaps $2.25, and makes a little money for the publisher, the distributor, and the author. Nobody gets rich on that; the money is in best-sellers, which sell a million and more copies.

Or there's the textbook situation. Take Kernigan and Plauger's excellent *Software Tools* (Addison-Wesley, 1976), or Grogono's *Programming in Pascal* (Addison-Wesley, 1978), as examples. They sell for around $15, and I suppose they sell 30,000 to 40,000 copies. Maybe more. Does anyone seriously contend that it's harder to write a good program than to write a good book? I've done both, and programs are easier, if a bit more tedious; there's more of the equivalent of reading galley proofs (we call it galley slavery) in programming than in writing. But both are hard work.

As to thefts: look, it's really in everyone's interest to bring the price of software down. The more good software—and by good, I mean stuff that ordinary people can use to do worthwhile things, programs that are self-instructing and have really good documentation—the more good software available at a reasonable price, the more machines will be sold, and the larger the software market will become—and I believe it's *already* approaching the book-buying market.

But, pleads the software developer, book publishers don't have to maintain their books; they don't have people telephoning with questions . . . .

Two answers to that. First, if you make sure the software and its documents are right the first time, you shouldn't be getting those complaints. Book publishers don't depend on their customers to be an unpaid quality-control department. Second—why, the pirates *can't* call in with questions.

So my heart doesn't bleed for the publishers. After all, who steals software? Business people? Nonsense. Try selling a computer system to your local architect and then tell him you're furnishing him with stolen programs. Oh boy! No, there are two categories of thieves: hobbyists and shady systems houses. Let's look at them.

First the hobbyist. This poor joker is typically broke. The computer industry gets every nickel he has. Since he *couldn't* pay for what he steals, he wouldn't have bought the stolen program anyway. Furthermore, he'll spend the saved money on something else that's computer-related. Nobody is losing that much money, even in the case of the clubs where members line up and make copy after copy, because darn few of those present would ever buy $500 programs. These people want programs to play with, not to sell, and probably not even to use.

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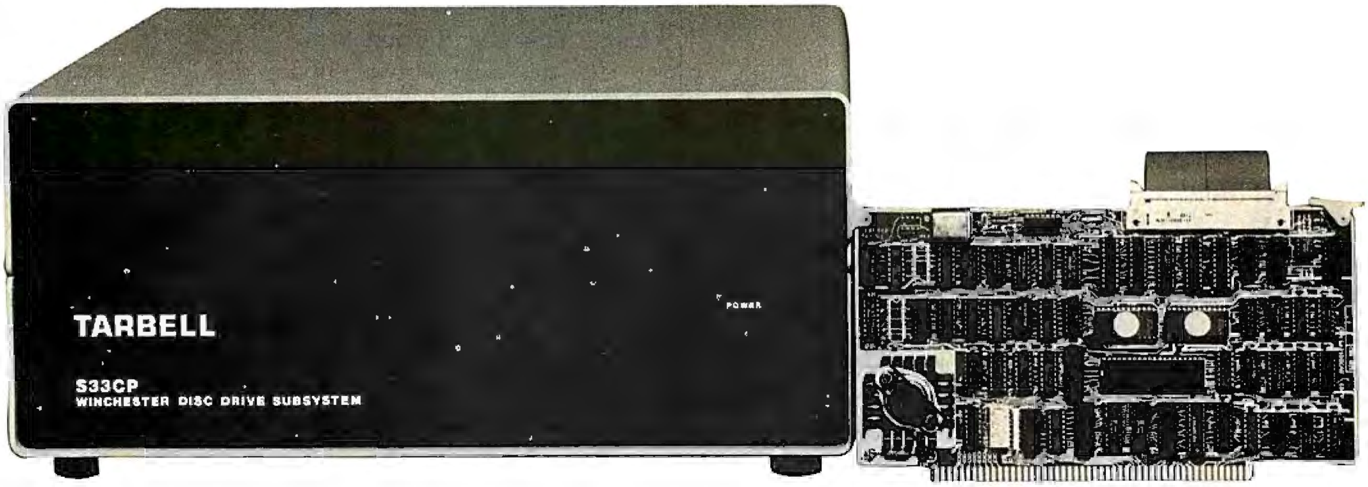

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What are the alternatives? To preserve those $500 price tags by making the programs unstable? Doggone it, that's precisely what some outfits have done. In an attempt to thwart pirates, they've made their software fragile. One database outfit has sent me *four separate copies* of its widely advertised program, each supposedly configured just for me. We have *yet* to make one work. I've given up on them.

Then there's what Mac Lean calls "Levitical Programming"; the first half of the manual is filled with "Thou Shalt Not" statements, and the licensing agreement is such that you have to be insane to give them your right name. This is professionalism?

Then too, if the software houses did decent documents, they'd make their pile selling those. Adam Osborne got rich giving away programs and selling books. So can anyone else. You just won't convince me that I ought to feel sorry for an outfit that can palm off some wretched document at $30 and sell hundreds of copies of it at discounts that would set a major publisher's eyes gleaming with greed.

And that's the answer to the systems-house pirate, who, if the truth be known, isn't all that great a threat either. True, he does soak up legitimate profits. I know a writer who bought a system from a fly-by-night company and found that his WordStar and CP/M were pirated. But when he went back to demand satisfaction, the systems house was gone—as, indeed, such houses usually will be. If they're successful, they *have* to go legitimate eventually; there's just no way to keep their pirate acts secret forever. And if they're not successful, they just can't have stolen that much. (Oh, true, at the hideously inflated prices software publishers charge, the total dollar value is high; but in fact we're talking about fewer than a hundred copies at most, and many of those wouldn't have been sold, but could only be given away. Not everyone who takes low-priced software will pay a high price for it.)

But if the documentation were useful, well written, had lots of examples, and was professionally printed—which, coming with something that sells for hundreds of bucks, darn well *ought* to be the case, even though very few programming documents meet any of those criteria—then even the pirate software houses would have to buy the books.

The answer to software piracy, it seems to me, is about the same as the answer to book piracy: sell decent products at reasonable prices and write decent documentation for sale at prices competitive with the price of photocopying the book. And stop worrying so much about protecting $500 and $600 price tags, because it isn't in the interest of the user community for software prices to stay that high. Very few programs are worth that much.

PL/I-80

What *is* a program worth? Well, there's a legal maxim: "the value of a thing is what that thing will bring," which is to say that something's worth what people are willing

to pay for it.

And you can bet that a program worth $600 had better *work*, and do so with minimum effort, and have decent instructions that can be read by a human being.

And just how many of those are around?

There are a few. My mad friend is ecstatic about Digital Research's PL/I compiler, PL/I-80.

"No bugs. It runs. It does what it says it will do."

"How did you learn the language?" I asked.

"Well, you need Digital's documents, of course," he said. "And two or three standard references on PL/I, one of them certainly being the Joan Hughes book [*PL/I Programming: A Structured Approach*, John Wiley and Sons, 1979] that you mentioned last time."

"You do need other reference works, then?"

"Oh, yeah. As usual, Digital has encrypted its documents. But they're up to Digital's usual standards of clarity, meaning that you'll need a Swahili interpreter . . . ."

Well, Mac Lean tends to exaggerate. They're not *that* bad. Not quite. It is true that Digital is a company that seems determined never to hire any writers, but its documents *are* complete, if confusing.

And Mac Lean remains as enamored of PL/I now as he was six weeks ago, which for him is quite a long time. I think we can safely add Digital's PL/I to the armory of good stuff—programs that work properly and are useful.

PL/I does have difficulties. There's no CASE (SWITCH) statement, which means you'll have far too many *if . . . then . . . else* statements; but everything necessary for rigidly structured code is in the language. The error reports are excellent. PL/I is not as fussy about declarations as Pascal. The language doesn't come out as compact as Pascal, and the programs don't run as fast, but they're easier to write. PL/I forgives quite a few errors.

There are other problems. The input/output is confusing, and worse, that's the part that you have to rely on Digital to tell you about. But you can learn it, and having done that, you're safe in programming with PL/I, because Digital is committed to support PL/I compilers for all its operating systems. You'll be able to transport your programs from your present micro to whatever machine—8086, Z8000, whatever—you eventually replace it with.

Thus, I'll stick my neck out this far: it's worth the time investment—a couple of weeks—to become mildly proficient in PL/I, always assuming that you're going to do some programming of your own, of course. If you're *strictly* a user, though, you're still safe in investing in PL/I programs, since you're probably guaranteed they'll be useful on the next generation of machines.

Digital PL/I also comes with a really groovy linker and library-management routine, allowing you to build up a raft of software tools that you can stick into other routines. The method for calling in outside procedures and passing them variables is straightforward, and again

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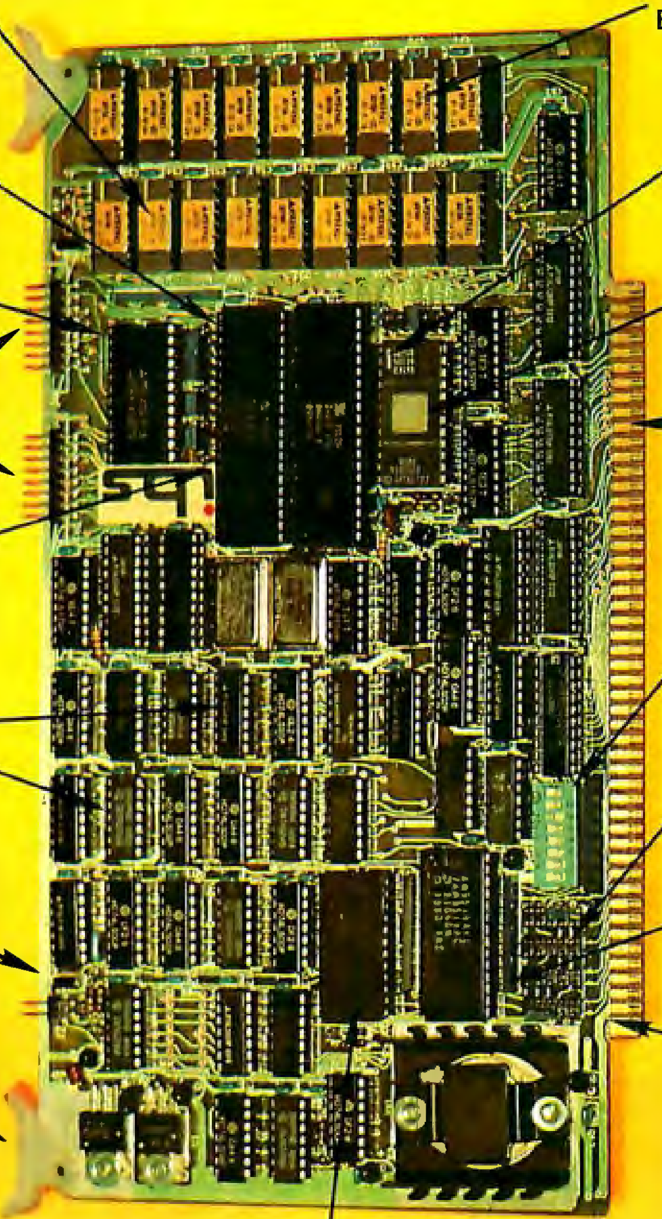

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PL/I is a good language for learning structured program concepts, and the Digital implementation is much better than acceptable. Recommended.

Bilge and Circumstance

Now we come to dBASE II versus the bilge pumps.

First: dBASE II is what used to be called VULCAN. The original VULCAN programmer formed a partnership with Messrs. Ashton and Tate, and now Ashton-Tate markets it. I'm told my evaluation was crucial in the decision to rewrite and expand the documentation, but to keep the program (with some fixes).

My original evaluation of VULCAN was "infuriatingly excellent"; it was potentially a very useful program, but fatally flawed by the worst user instructions I'd ever seen.

I'm pleased to say that now it's not infuriating, just excellent. The flaws are (almost) all gone, the program documents have been rewritten and expanded until almost anyone can learn to use dBASE II, and VULCAN always was a darn good database program. I think it's overpriced at $700, but apparently Ashton-Tate gets away with it. If any program is worth that price, dBASE II is.

dBASE II is a *relational database*. This is in contrast to tree-structured databases. Relational databases make a kind of matrix of data; you can then structure the data any way you want, examine relationships you hadn't realized were there, and in general play about with the data. Tree-structured systems of the CODASYL variety require you to do the structuring in advance, and woe to you if you get it wrong.

It's a bit hard to describe dBASE II, because it's very versatile and powerful. For instance, you can build a full accounting system from dBASE II, tailoring it to your needs, and it really would work. (I think you'd be better off buying an accounting system, but that's for another article.) You can put up libraries in dBASE II, and then take the same data and reorganize it by subject matter to make bibliographies. What dBASE II preserves are the *relationships* among the mass of data entered; the exact structure of the data can be changed at any time. This makes for a very powerful tool, one whose capabilities aren't entirely realized just yet.

And, dBASE II is now well documented. What they did was keep the old documentation, which was a really complete reference manual but sans examples or sane organization, and add, up front where it belongs, a complete new program-user's guide, done by someone just learning to use the VULCAN system. Thus you can go through the first set of documents and learn how to use dBASE II, after which you can use the second chunk as a handbook, which, once you actually understand dBASE II, isn't all that bad. (It remains, however, the most frustratingly miserable excuse for a way to *learn* a system that I've ever seen.)

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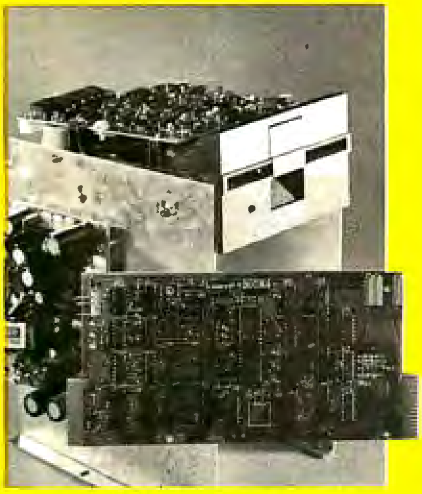

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Second, the bugs have been fixed. Not that there ever were many; VULCAN was always excellent, even if infuriating.

And finally, the program remains very powerful. dBASE II isn't just a means of storing and retrieving data. It contains what amounts to a whole data-handling language with the ability to do sorts and restructures, to copy data from one place to another, and to do conditional arithmetic. For example,

```
REPLACE ALL FOR (BILL:DATE <= 791031)
        COST WITH COST*1.1
```

would be a command to search the database to find records that had BILL:DATE older than October 31, 1979 and for those records to replace the value of the variable COST by the current value plus ten percent.

Other forms of magic are possible. You have to study dBASE II; it can do things you wouldn't think of. But it's well worth the study. I'm using it to organize my files, by subject, type, date, date of last access, and drawer number, and also adding keywords; eventually I'll have this place organized, and this time for sure. (The last time I got this ambitious I was using VULCAN, and the documentation drove me to quit in disgust, but this time things seem to be going much better.) And my time wasn't wasted last year, since dBASE II can read the old VULCAN files and then reshape them into the new system I've designed. What happens is that dBASE II copies the old records into new ones, ignoring any in the old database that aren't in the new structure; while if it finds variables in the new structure that weren't in the old records, it fills them with blanks, leaving room for you to enter the data at your leisure.

dBASE II, I'm pleased to say, makes no attempt to prevent you from making backup copies. Far from it: all through the documentation, you're urged to make a safety copy of both data and program, just in case. That advice is worth taking, given the relative costs of data-entry labor as opposed to floppy disks. I expect people will try to rip off the dBASE II software, given the price, but I guarantee they'll get zero use of it without a complete set of documents . . . .

Statistical Analysis with Microstat

Microstat by Ecosoft. I don't care much for the house name—I'm growing weary of "ecology" names for software companies, since they make me think their products may contain significant portions of natural organic waste—but I can recommend the program, with warnings.

First warning: you, or someone you work with, better know quite a lot about statistics. Microstat will do some *very* sophisticated statistical analyses, but it will *not* tell

you which of its many features you want to use.

On the other hand, you can make up your data files rather easily, then manipulate the daylights out of them with Microstat's various routines; so you don't have to know in advance that you'll want to employ the Kolmogorov-Smirnov Two Group Test (whatever that is) in order to use it later.

I wish I'd had Microstat last fall. About a year ago I quit smoking and took up running (and yes, I'm still at running, and it's a year today since I last smoked). Like many new converts, I began reading the various running magazines, and one of them rates running shoes. It gave a fairly low rating to the shoes I like, and I got interested in why. (It shouldn't have; one of the measures was shoe weight, rank ordered to a *tenth of a gram*! I doubt the magazine has balances that sensitive, and a few drops of sweat would change the ratings.)

The magazine published its data—more or less—as well as its ratings, so I decided to do a fairly complete statistical analysis to see just how much confidence you could put in those ratings. (Not a lot, I concluded. Many of the measures are highly correlated and not sufficiently thought out.) I didn't have a decent stat program, so I had to write my own, based mostly on Paul Horst's matrix algebra routines I learned way back when. My routine will do a couple of things Microstat doesn't do, such as generate a new data file with the data entries transformed to "Z" scores (in which the mean is 0 and the standard deviation is 1), and my system preserves a "name and comment" string field associated with each data case. But I'd still have been far better off using Microstat with its much more complete statistical analyses. The Microstat package has a data-entry routine with some elementary error-correction procedures, including an EDIT routine; I could have used that.

Microstat does what you'd expect: means, variances, correlation matrices, etc. It also does auto-correlation (a variable correlated with itself). It does analysis of variance, "Student's" T test, the F test, and various non-parametric tests such as chi-square. It tries different distributions and checks goodness of fit. About the only thing missing that I'd like to see is Chebyshev's criterion. But *note this well*: if this paragraph is meaningless to you, you will not understand Microstat's documentation. This is not a program intended for the casual "cookbook" stat user. It *has* everything the cookbook experimenter would need, but in a fairly intimidating context. In fact, Ecosoft (which seems to be some professors at a Midwestern university) would do well to write a simple-minded cookbook to accompany its programs.

On the other hand, if you do know a bit about statistics—if you've mastered something beyond the elementary textbooks—then Microstat can help you. It has a surprising number of features, and if you know what statistics you want, or can find someone to advise you on the math theory, the Microstat documentation is more than adequate to tell you how to use the program. Given that caveat, I recommend Microstat; but do be warned that the book is written with graduate-level experimental statistics students in mind.

Soothing the Savage LISPer

And finally we have a good book on LISP. I confess I'm slowly beginning to appreciate just how powerful the LISP programming language is, and I will now concede that anyone intending to make a career in computer science should become aware of the language. I'm still not convinced LISP can be learned without tutorial help, but certainly *LISP*, by Patrick Henry Winston and Berthold Klaus Paul Horn, will help. The book is intelligently written. There are a lot of examples; the most useful are given as exercises, which made me furious until I realized there were answers in the back of the book. It has a good table of contents.

I'm still not at all convinced that LISP programs will ever be comprehensible to anyone who doesn't spend a lot of time working with the language. The claims that they're easy to read and don't require comments are, in my view, just wrong and would only be made by a maniacal LISPer (and a lot of LISP users do tend to be maniacs, as witness the hate mail I get for not sufficiently praising the language).

Anyway, the book is the best I've seen on the subject and tells a lot about LISP. ■

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Build a Joystick A-to-D Converter for the TRS-80 Model I or III

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[**Editor's Note:** *This series of articles describes hardware and software projects for the Radio Shack TRS-80 (Model I, Model III, and Color Computer).*]

Last month I examined the Color Computer's built-in analog-to-digital converter ("Color Computer from A to D," page 134). I described the software that reads the joysticks and showed how other analog input devices can be connected to the Color Computer.

This month I'll give equal time to Model I and III users by presenting a hardware/software project that allows joystick and other analog inputs to these computers. Since the Model I and III don't have built-in analog-to-digital (A/D) conversion circuitry, we'll have to make our own. It's a simple project requiring two common integrated circuits, a few resistors, and some other components—costing less than $20 (not bad for a two-channel, 64-step A/D converter). You won't have to modify your computer at all—the A/D circuit plugs in as a printer does. Since the device connects to the line-printer bus, you'll need a Model I with Level II BASIC and an expansion interface or a Model III with Model III BASIC.

I'll provide step-by-step instructions for fabricating and testing the circuit. Finally, I'll show you how to use the A/D converter with a joystick and other analog input devices.

About the Author
William Barden Jr. has written many books on microcomputer programming and design. He is a member of the Association for Computing Machinery and the Institute of Electrical and Electronics Engineers.

General Description

The block diagram of the circuit we'll build is shown in figure 1. Note that it connects to the TRS-80's printer (a.k.a. *Centronics*) bus. Therefore, you won't be able to use the line printer during joystick operations and vice versa.

The A/D circuit largely duplicates that found in the Color Computer. (For further background, see the discussion in last month's article.) It consists of a digital-to-analog converter (DAC) and two comparators—one each for the joystick's X and Y channels. Using a reference voltage from the DAC, the comparators allow you to perform successive approximations of the voltage levels input from the X and Y joystick channels.

Six outputs go from the line-printer bus to the DAC;

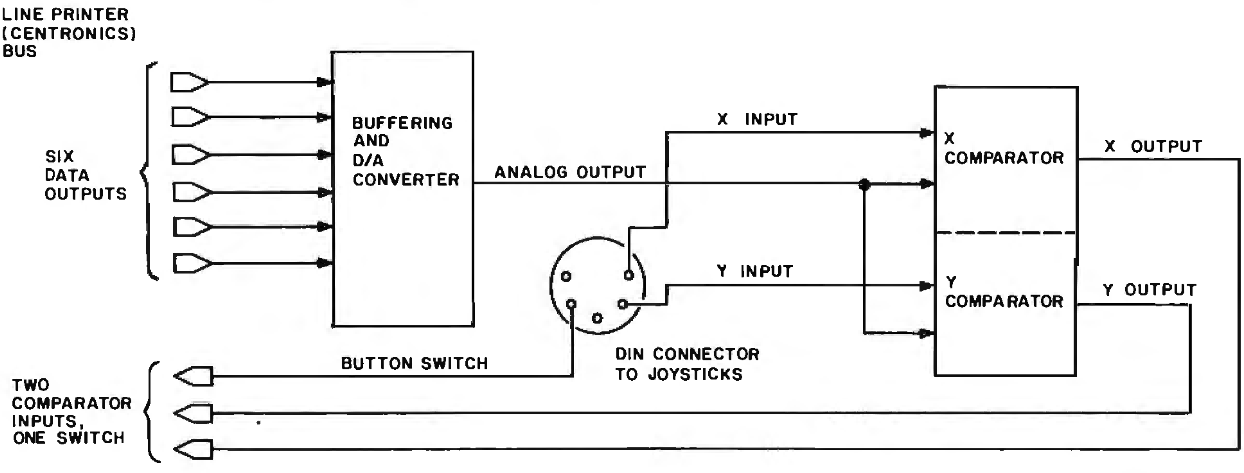

Figure 1: *Block diagram of the A/D circuit. The DAC is driven by outputs from the line-printer port. Its output goes into two comparators, one comparing the DAC voltage with the X channel, and the second comparing the DAC voltage with the Y channel. The comparator outputs are fed back into the line-printer port.*

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these make up a 6-bit digital value that is converted into a 64-step range of reference voltages by the DAC. Three inputs go to the line-printer bus: one for the X channel, one for the Y channel, and an optional one for a joystick push-button switch.

The TRS-80 printer bus. To some extent, our A/D circuitry must emulate a printer, strange as that may sound. Therefore, before getting into the details of the A/D and joystick circuits, I'll briefly explain the TRS-80 printer logic. Figure 2 gives a simplified version of the Model I printer-bus circuit. (The Model III's circuitry is slightly different, but for our purposes the Model I description will suffice.) It consists of two 74LS175 integrated circuits (ICs), each containing four flip-flops; four buffers of a 74LS367 IC; and a one-shot strobe implemented by half of a 74LS123 monostable multivibrator.

Writing a character to hexadecimal address 37E8 in the Model I causes the clock signal (CLK) to strobe the 8 bits of data into the two 74LS175s, and also triggers a one-shot strobe (DATA STROBE) telling the printer that data are available on lines DATA8-DATA1 of the line-printer bus. The data remain in the 74LS175s until a new character is written or a system clear (CLR) is done.

Reading hexadecimal address 37E8 in the Model I causes the four signals BUSY, OUTPAPER, UNIT SELECT, and FAULT to be gated onto data lines D7-D4 of the expansion-interface bus.

A typical Model I printing cycle goes like this:

1. The Model I reads the line-printer status by executing the Z80 instruction LD A,(37E8H).
2. It tests status bits 7 (BUSY) and 6 (OUTPAPER). If both are zero, the line printer is ready to accept more data; otherwise, it is not ready, and the Model I loops back to step 1.
3. If the line printer is ready, the Model I loads the character to be printed into the accumulator and then writes it to the printer logic with the instruction LD (37E8H),A. This activates the one-shot strobe, putting the 8 bits of data into the two 74LS175s. The one-shot resets itself after a short delay, strobing the data into the line-printer electronics, starting the printing cycle, and setting the BUSY status bit.

Memory mapping versus I/O mapping. In the Model I, the line-printer bus is memory-mapped to hexadecimal address 37E8. In the Model III, the printer bus is input/output-mapped to Z80 port 0F8 (hexadecimal). Aside from using different ICs, the Model III has the same logical implementation as the Model I. To test status, do an IN A,(0F8H) instead of an LD A,(37E8H). To output a character, do an OUT (0F8H),A instead of an LD (37E8H),A.

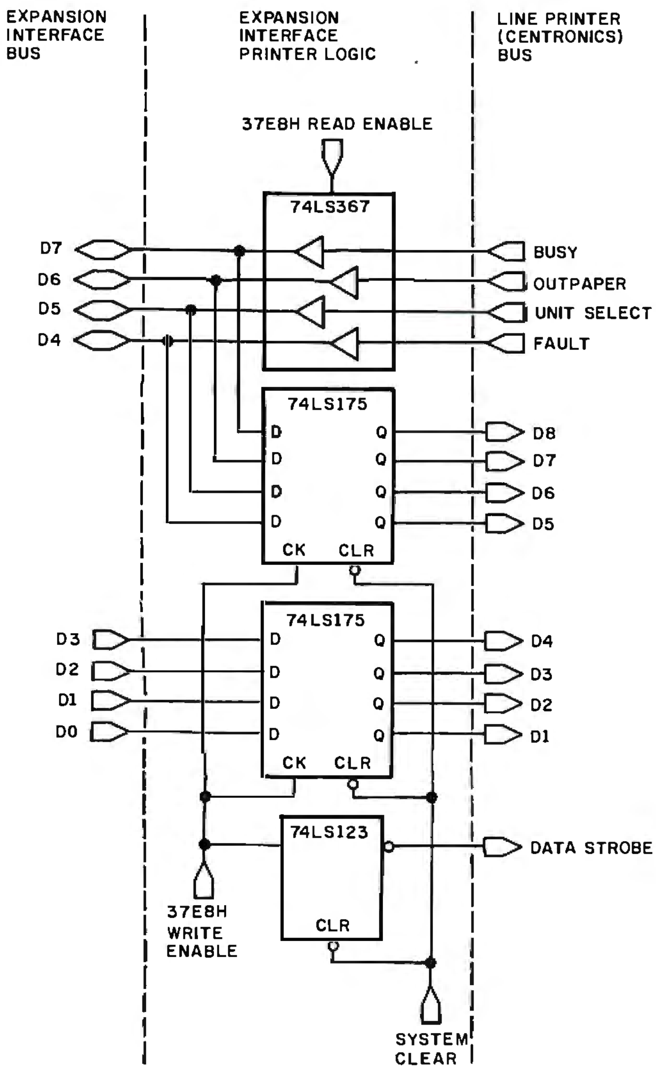

Figure 2: *Model I line-printer controller. Two 4-bit registers strobe in the 8 bits of the character to be printed. At the same time, the one-shot is set to allow the output line-printer electronics to strobe in the data from the register. Four status lines are gated to the computer's data bus on a read.*

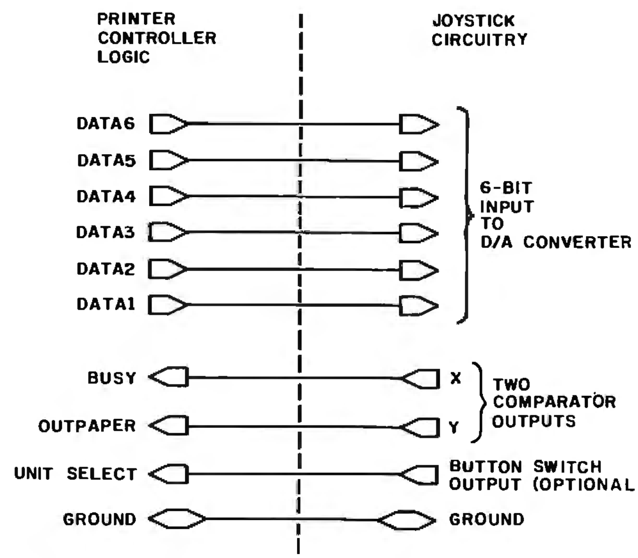

Figure 3: *Line-printer lines used in the A/D circuit. Six output lines transmit a digital value to the DAC. Two input lines read the comparator values. One optional input line allows checking the button switch on a joystick.*

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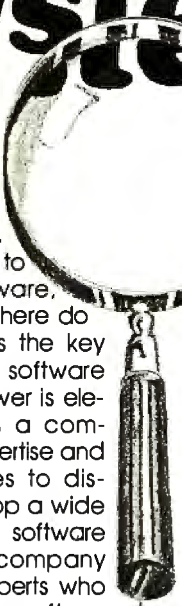

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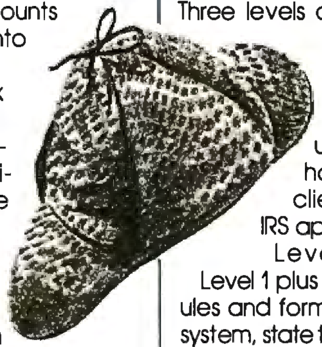

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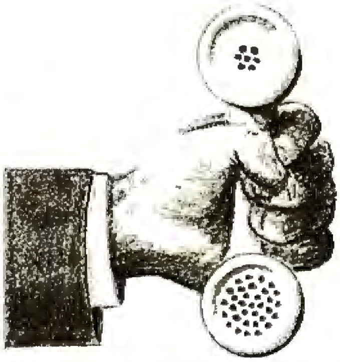

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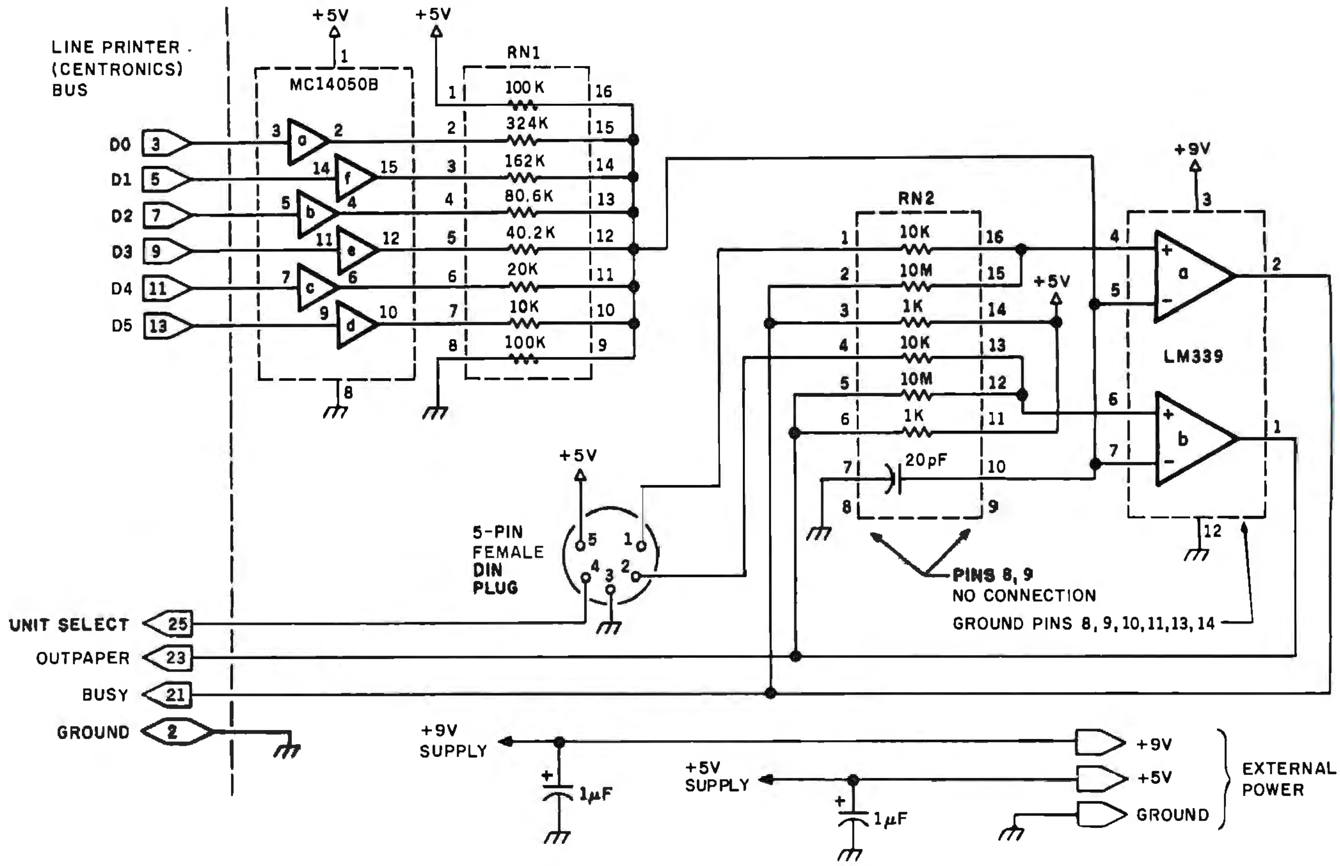

Figure 4: *Detailed logic diagram of the A/D circuit. Power is supplied by a 9-V transistor battery and a 5-V power supply.*

So far, we've done all the printer I/O using Z80 machine instructions. You can also use BASIC:

	Model I	Model III
Get Status	PEEK(14312)	INP(248)
Output Character (*x*)	POKE14312,*x*	OUT 248,*x*

Detailed Circuit Description

We can easily make the joystick circuitry emulate a line printer. First, forget about the DATA STROBE output. It's only there for the line-printer electronics. Since data stay in the 74LS175s (or their Model III equivalents), we can simply write to hexadecimal address 37E8 (or 0F8) to output 8 bits to DATA8-DATA1. Whenever we want to read in data, we just read hexadecimal address 37E8 (or 0F8) to input 4 bits.

I've chosen to dedicate DATA6-DATA1 as outputs from the program to the DAC, the BUSY input as the X-channel comparator input, and the OUTPAPER input as the Y-channel comparator input. These eight lines plus ground are all that are needed to perform the basic joystick operation. They're shown in figure 3. A ninth line is optional as a joystick button input.

The detailed A/D circuit is shown in figure 4. Its physical layout corresponds to that of the block diagram in figure 1.

A typical joystick schematic is shown in figure 5. It is comprised essentially of two potentiometers with the two ends of each connected between +5 volts (V) and ground. The wiper of each potentiometer varies with the position of the joystick. Output from the wiper varies between 0 and +5 V. The X-channel 0-V position is toward the left; the Y-channel 0-V position is toward the top.

You can buy a bare-bones joystick (dual 100-k-ohm potentiometers) from Radio Shack for $4.95 (catalog number 271-1705). You can also use one of the Color Computer's joysticks, sold as a pair for $24.95 (catalog number 26-3008). Figure 6 shows the bare-bones joystick

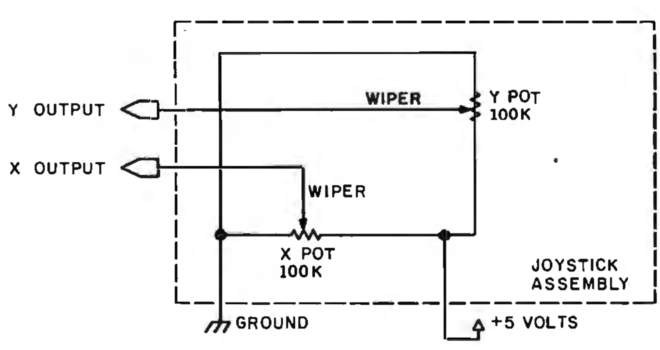

Figure 5: *Joystick schematic. Two 100-k-ohm potentiometers are connected to ground and +5 V. Each wiper outputs a voltage of 0 to 5 V depending upon the joystick position along the X and Y axes.*

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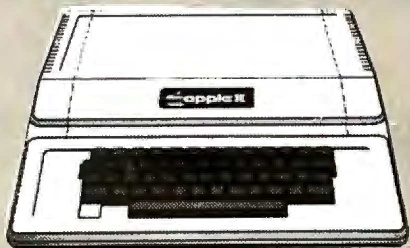

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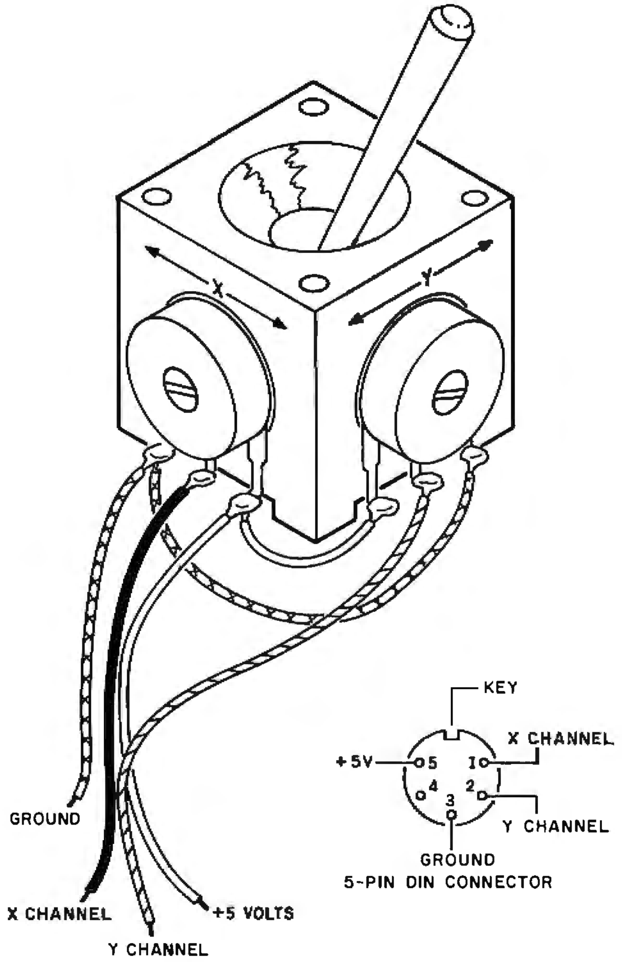

Figure 6: *A prebuilt joystick available from Radio Shack. The device comes with a 5-pin male DIN plug.*

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1 162-k-ohm ⅛ watt or greater 1% resistor
1 80.6-k-ohm ⅛ watt or greater 1% resistor
1 40.2-k-ohm ⅛ watt or greater 1% resistor
1 20-k-ohm ⅛ watt or greater 1% resistor
1 10-k-ohm ⅛ watt or greater 1% resistor
1 20- or 47-pF disk capacitor
2 1-μF electrolytic capacitors
1 MC14050B (4050B) hex buffer/converter (noninverting) IC
1 LM339 quad comparator IC
wire-wrap and hook-up wire
1 joystick potentiometer, 100-k-ohm, with
1 5-pin male DIN plug
1 9-V transistor battery

Table 1: *Parts list for the A/D circuit and joystick controller.*

with the required connections.

Each of the joystick voltage outputs goes into one of the comparator's plus (+) inputs. The minus (−) input for both comparators comes from the output of the DAC. Each comparator compares the current joystick voltage with the DAC output. If the joystick voltage is lower than the DAC output, a logic 0 is output from the comparator. Otherwise, a logic 1 is output. The results of both comparators go to the input lines BUSY (X-coordinate) and OUTPAPER (Y-coordinate).

To determine the voltage level on either joystick channel, we just vary the DAC output from 0 to +5 V until we get a comparator output of 1 for the channel. That's easy to do with the DAC.

The DAC converts a 6-bit digital value into an analog voltage. Each of its resistors has approximately double the resistance of the next lower resistor. Each resistor is connected to the output of one bit of the MC14050B. This is a complementary metal-oxide semiconductor (CMOS) buffer with an output of close to 0 V for a logical 0 input, and about +4.95 V for a logical 1 input. By varying the 6-bit input from 000000 to 111111, we will get a voltage range from about 0.25 V to 4.75 V in 64 steps of about 70 millivolts (mV) each (see figure 7).

As a side issue, for a digital-to-analog conversion, we can simply forget about the comparator output and take the output from pin 12 of the MC14050B. The voltage output will be the analog equivalent of the 6-bit input value.

Circuit Construction

A parts list for the joystick circuit is shown in table 1. All the parts can be obtained from Radio Shack or other electronics suppliers. The resistor tolerances are somewhat critical. If you cannot get 1% resistors with the values indicated, you can use hand-selected 5% resistors. Measure the resistance with a multimeter and choose values within 2 to 3% of the listed values. There is enough variation in most resistors that you should be able to come fairly close. Two resistors can be used in

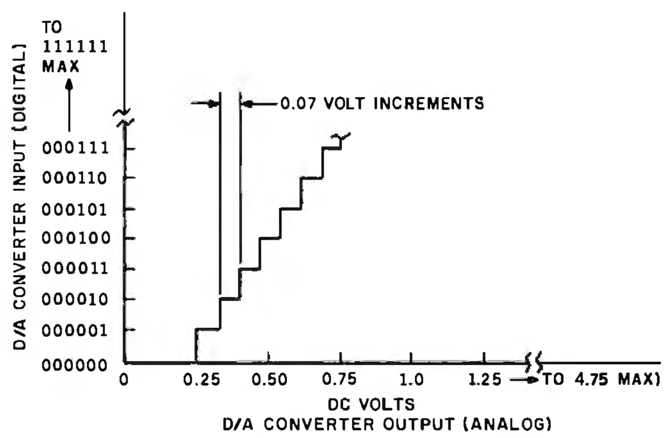

Figure 7: *DAC output as a function of digital input. The output should increase monotonically as shown.*

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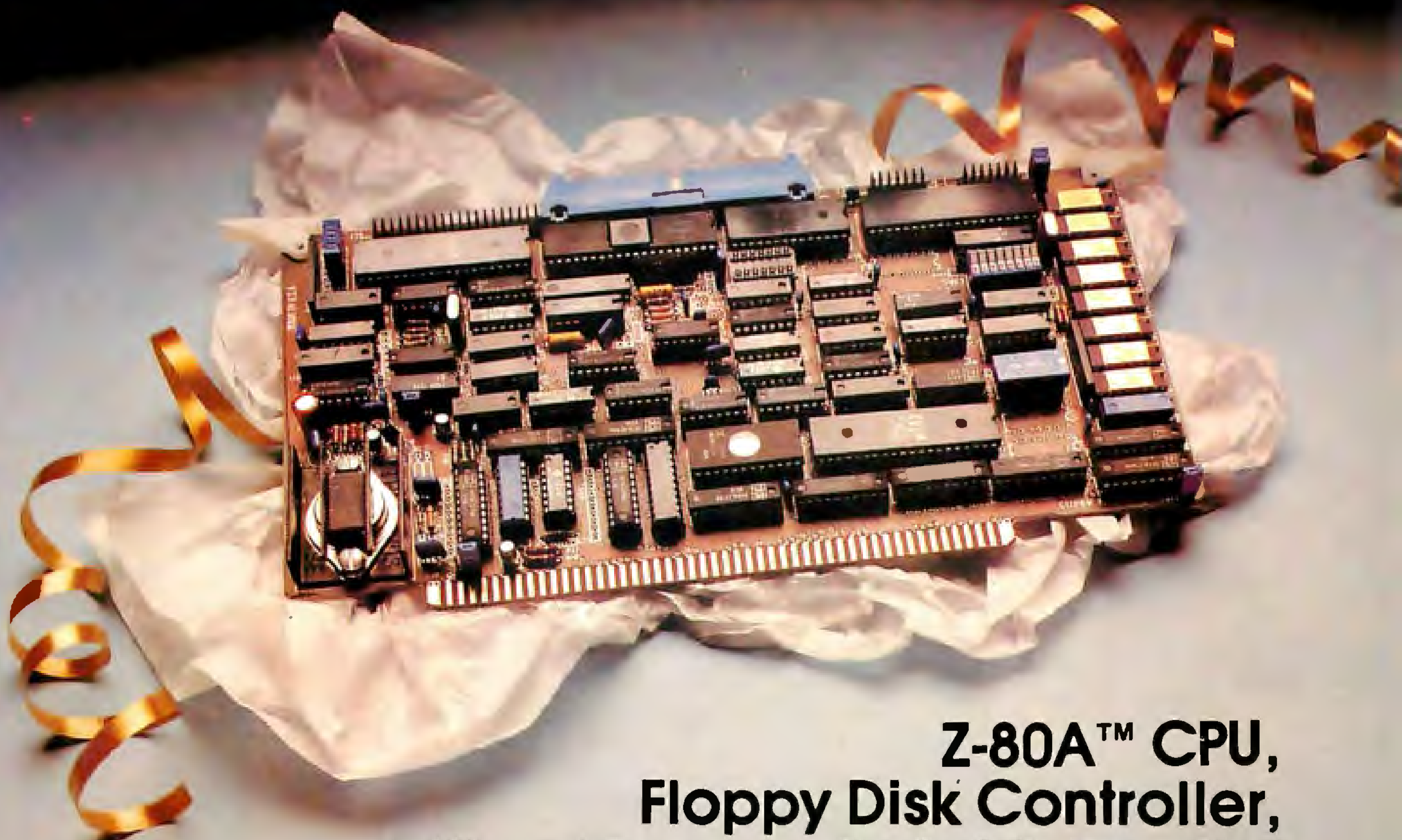

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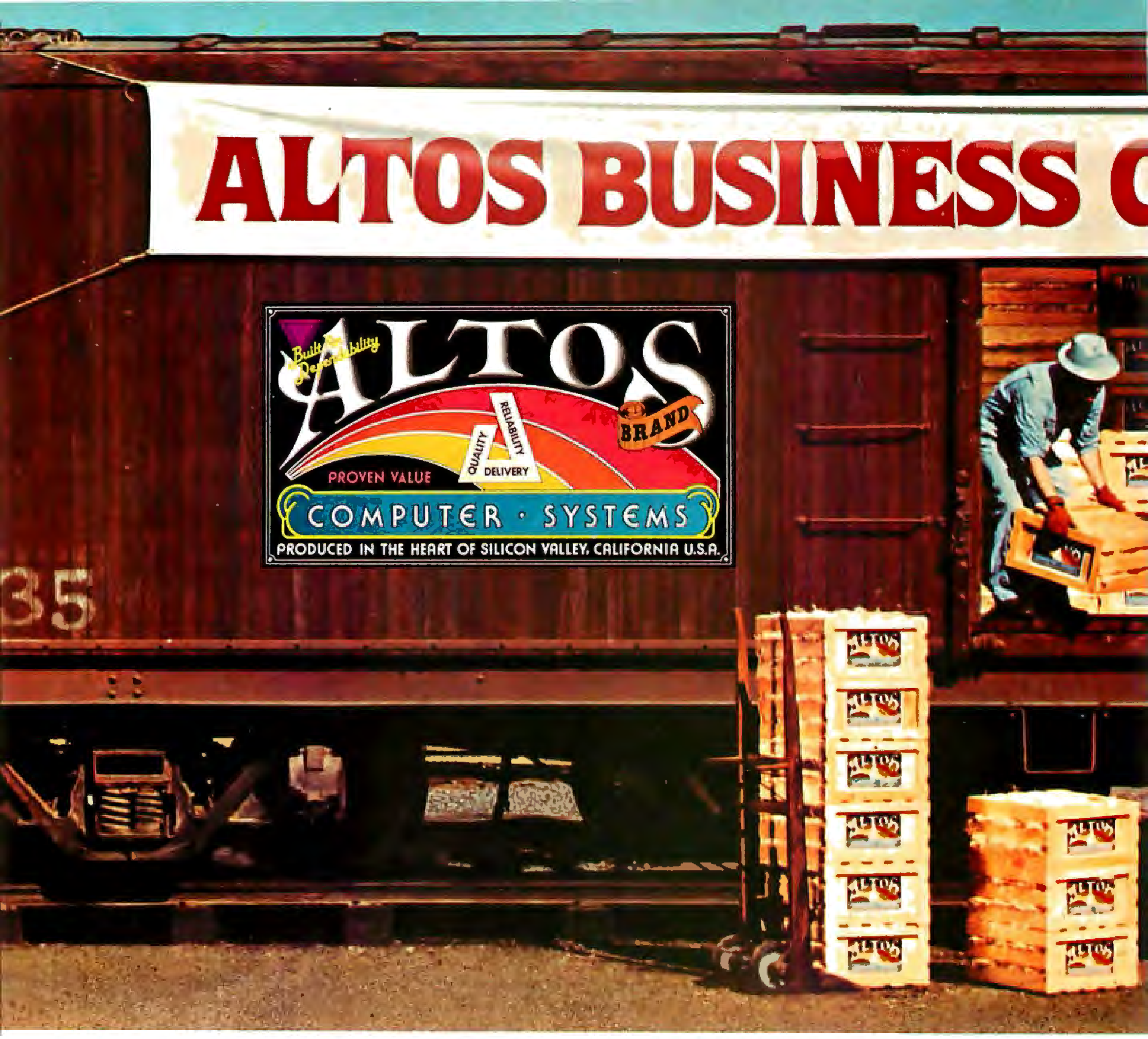

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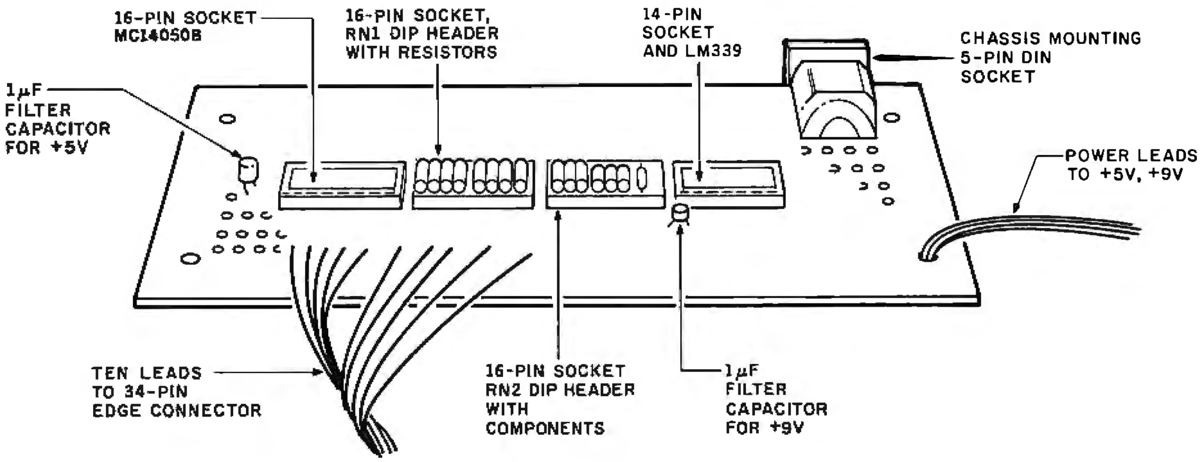

Figure 8: *Physical layout of the A/D circuit as laid out on a prototype board.*

series to get a total resistance that is correct. The prototype circuit, which works well, was made using hand-selected 5% resistors.

Soldering and wire-wrapping. You will need a small (30-watt (W)) soldering iron, rosin-core solder, and a wire-wrap tool or gun. If you've never wire-wrapped, don't worry—it's easy to do and you can make about one connection per minute. Assuming you have all the tools and parts, it will probably take about an hour and a half for the entire job.

Mounting the parts. The circuit is mounted on a small prototype board (Radio Shack catalog number 276-170). The general layout is shown in figure 8. The board is bare on one side and has 55 rows with solder pads on the other. The spacing of the holes is compatible with the spacing on the pins of the four wire-wrap IC sockets.

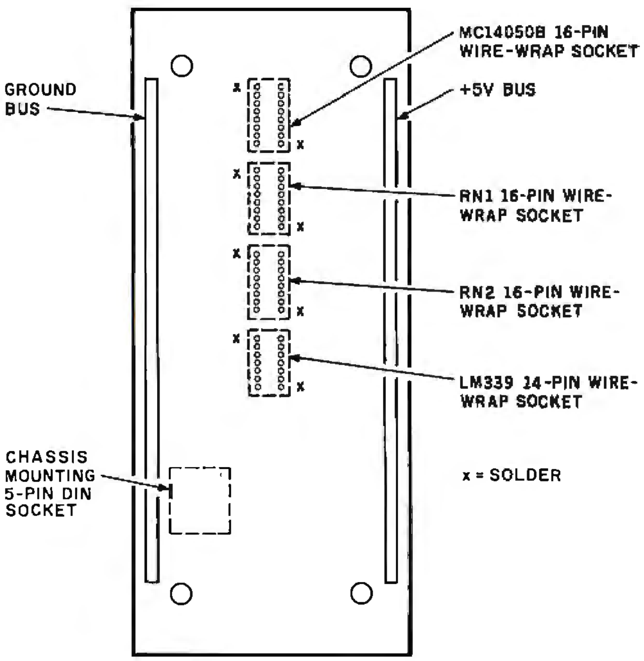

Figure 9: *Underside of the A/D prototype board showing positions of ground and +5-V buses and solder points for the wire-wrap sockets.*

Mount the four IC sockets by soldering opposite corners of each socket, as shown in figure 9.

Use the left-hand strip for the ground bus and the right-hand strip for the +5-V bus.

The 34-pin edge connector may be difficult to find even though Radio Shack is now carrying it. For Model Is, you can get by with their 40-pin edge connector by inserting a cardboard "filler" in one side to properly "key" the edge connector. For Model IIIs, you *have* to use a 34-pin connector because the cutout in the cover will only pass a 34-pin width.

I soldered the wires to the pins of the edge connector even though the edge connector was really meant as an insulation displacement type that pokes metal contacts through a ribbon cable. The pin layout for the edge connectors is shown in figure 10. The edge connector is designated EC.

The 5-pin DIN connector is another problem. If you use the Color Computer joysticks, the matching 5-pin plug will probably have incompatible spacing. Consider

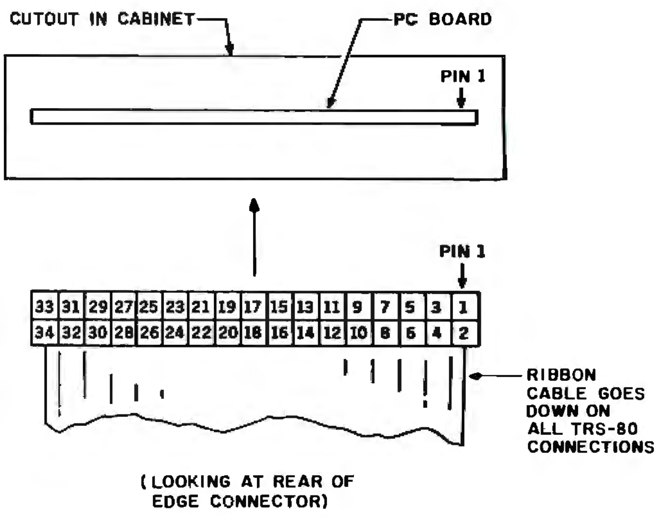

Figure 10: *Pinouts for the card-edge plug that connects the A/D circuit to the TRS-80 line-printer bus. Use a displacement-type ribbon connector and solder the hook-up wires to the connector pins.*

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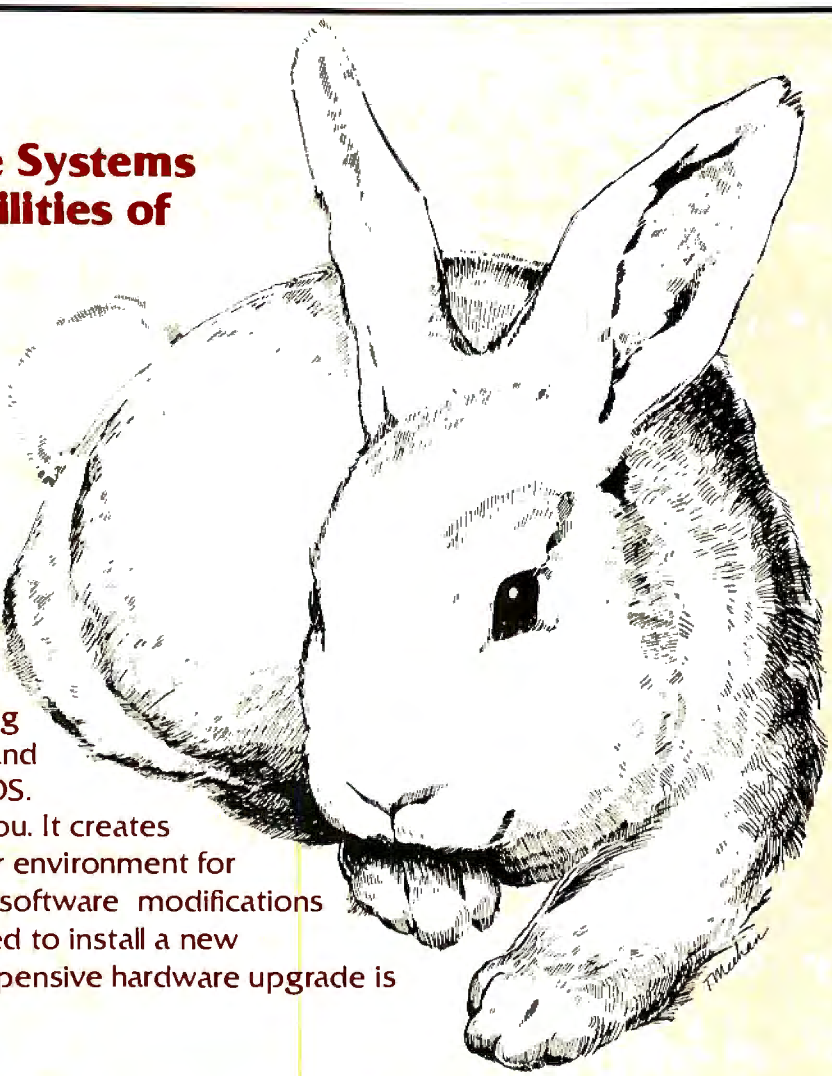

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34-pin edge connector to other components

EC – 3	to	MC14050B – 3
– 5	to	– 14
– 7	to	– 5
– 9	to	– 11
– 11	to	– 7
– 13	to	– 9
– 21	to	LM339 – 2
– 23	to	– 1
– 25	to	DIN – 4

MC14050B to RN1

MC14050B – 2	to	RN1 – 2
– 15	to	– 3
– 4	to	– 4
– 12	to	– 5
– 6	to	– 6
– 10	to	– 7

LM339

LM339 – 7	to	LM339 – 5

RN1

RN1 – 16	to	RN1 – 15
– 15	to	– 14
– 14	to	– 13
– 13	to	– 12
– 12	to	– 11
– 11	to	– 10
– 10	to	– 9
– 12	to	LM339-5

RN – 2

RN2 – 1	to	DIN – 1
– 2	to	LM339 – 2
– 2	to	RN2 – 3
– 4	to	DIN – 2
– 5	to	LM339 – 1
– 5	to	RN2 – 6
– 10	to	LM339 – 7
– 12	to	– 6
– 12	to	RN2 – 13
– 15	to	LM339 – 4
– 15	to	RN2 – 16

Table 2: *Wire-wrap list for the A/D circuit.*

cutting off the plug and attaching the cable to an audio-type DIN plug or attaching the wires directly. If you are using the joystick potentiometer, it comes with a 5-pin male DIN plug attached. For the A/D circuit, get a 5-pin female DIN chassis-mounting jack.

Wire-wrap connections. Make the wire-wrap connections shown in table 2. Most of these are wire-wrap to wire-wrap, although some will be wire-wrap to solder. These connections can be made with 30-gauge wire-wrap wire. However, you might consider 22-gauge stranded wire for cable running to the edge-connector leads. Route the edge-connector leads through board holes for strain relief.

Now connect the ground points shown in table 3a. You can wire-wrap common ground pins onto the same point and then route a single wire to the ground bus. Make the +5-V connections in table 3b in similar fashion.

Power connections. Now run four wires as shown in figure 11. Two "hook-up" wire (22-gauge stranded) leads run from the ground bus. One +5-V lead runs from the

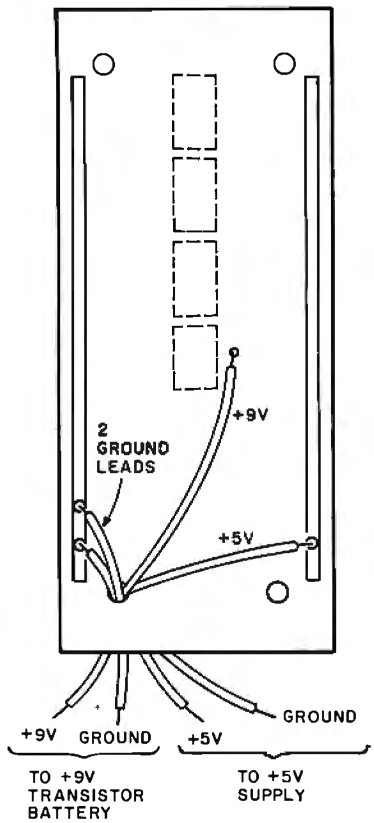

Figure 11: *Power connections for the A/D circuit. For +5 V, use a regulated 5-V power supply, such as Radio Shack's 277-125 (a kit).*

(3a)	(3b)
LM339 – 12, 8, 9, 10, 11, 13, 14	MC14050B – 1
MC14050B – 8	RN1 – 1
RN1 – 8	RN – 2, 11, 14
DIN – 3	DIN – 5
RN2 – 7	
EC – 2	

Table 3: *Ground connections are shown in table 3a. Table 3b gives the +5-V connections.*

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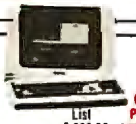

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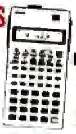

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+5-V bus. One +9-V lead runs from pin 3 of the LM339. These leads can be combined in a four-wire ribbon cable and routed through one hole for convenience. Two of the leads, one ground lead and the +9-V lead, attach to a 9-V transistor battery. The other two leads connect to a regulated +5-V supply. (In case you don't have one already, I suggest you get Radio Shack's $6.99 kit, catalog number 277-125.) Leave the power leads unconnected for the time being.

Without plugging in any chips, test the connections with a multimeter or continuity checker. A common straight pin works fine for getting into the IC socket holes. As each circuit checks out, cross it out on the schematic. This check takes little time and saves a lot of grief later on due to connection errors.

Solder one 1-microfarad (μF) filter capacitor between +9 V and ground and another between +5 V and ground, as shown in figure 8. Make certain that the polarity of the capacitors (note the + or − sign) is oriented properly.

Construct two dual-inline package (DIP) headers as shown in figure 12. One of these contains the DAC resistors; the other has the resistors and other components for the LM339. If you apply much heat during the soldering, you should remeasure the values for the six DAC resistors; they may have changed due to the heat.

Now plug in the DIP headers, the MC14050B, and the LM339. The A/D converter is (hopefully) complete. Connect it to the line-printer card-edge connector (pin 1 is on the top right), turn on the Model I or III, and connect the +5-V and +9-V supplies. Make the following test: watch for smoke and try a fingertip test of the board components. They should be warm but not hot. If everything seems okay, plug in the joystick connector and repeat the test. You're now ready for program debugging.

Program Testing

The following preliminary tests are included as a means to "bring up" the circuit one step at a time. If you feel like going directly to the final program instead of following this procedure, by all means do so. If you have problems, fall back on these preliminary tests.

DAC output. The first program tests the output of the DAC. A voltmeter is required to run it. If you don't have one, go on to the next test.

Hook the voltmeter between ground and the output of the DAC—pin 12 of the MC14050B. Run the program in listing 1. Substitute 120 OUT 248,V for statement 120 if you are using a Model III.

The program steps the DAC through the range of output voltages by sending it the values 000000-111111. Each voltage step should be approximately 70 mV over the

Listing 1: *Using a voltmeter and this BASIC program, you can measure the voltage levels produced by the DAC when the digital input ranges from binary 000000 to 111111. Table 4 shows the values obtained by the author.*

```
100 REM DAC TEST. OUTPUT VOLTAGES FROM 0 TO 63.
110 FOR V=0 TO 63
120 POKE 14312,V
130 CLS: PRINT @ 534,"DAC VALUE=";V
140 IF INKEY$="" GOTO 140
150 NEXT V
```

Listing 2: *For Model I computers, this BASIC program compares the voltages at the X and Y joystick channels with stepped voltages from the DAC.*

```
100 REM COMPARATOR TEST
110 FOR V=0 TO 63
120 POKE 14312,V: CLS
130 PRINT @ 520,"VALUE=";V;
140 PRINT @ 540,"X=";(PEEK(14312) AND 128)/128;
150 PRINT @ 560,"X=";(PEEK(14312) AND 64)/64;
160 FOR I=0 TO 1000: NEXT I
170 NEXT V
```

Listing 3: *The same as listing 2, but for Model III computers.*

```
100 REM COMPARATOR TEST
110 FOR V=0 TO 63
120 OUT 248,V: CLS
130 PRINT @ 520,"VALUE=";V;
140 PRINT @ 540,"X=";(INP(248) AND 128)/128;
150 PRINT @ 560,"Y=";(INP(248) AND 64)/64;
160 FOR I=0 TO 1000:NEXT I
170 NEXT V
```

Digital Input	Analog Output	Digital Input	Analog Output
0	0.240	32	2.48
1	0.312	33	2.55
2	0.387	34	2.63
3	0.460	35	2.70
4	0.530	36	2.77
5	0.602	37	2.84
6	0.677	38	2.92
7	0.749	39	2.99
8	0.785	40	3.03
9	0.857	41	3.10
10	0.932	42	3.18
11	1.005	43	3.25
12	1.075	44	3.32
13	1.147	45	3.39
14	1.222	46	3.47
15	1.294	47	3.54
16	1.419	48	3.67
17	1.492	49	3.74
18	1.568	50	3.82
19	1.640	51	3.89
20	1.710	52	3.96
21	1.782	53	4.04
22	1.858	54	4.12
23	1.930	55	4.19
24	1.966	56	4.22
25	2.03	57	4.30
26	2.11	58	4.37
27	2.18	59	4.44
28	2.25	60	4.52
29	2.32	61	4.59
30	2.40	62	4.67
31	2.47	63	4.74

Table 4: *Values obtained from DAC test of author's prototype.*

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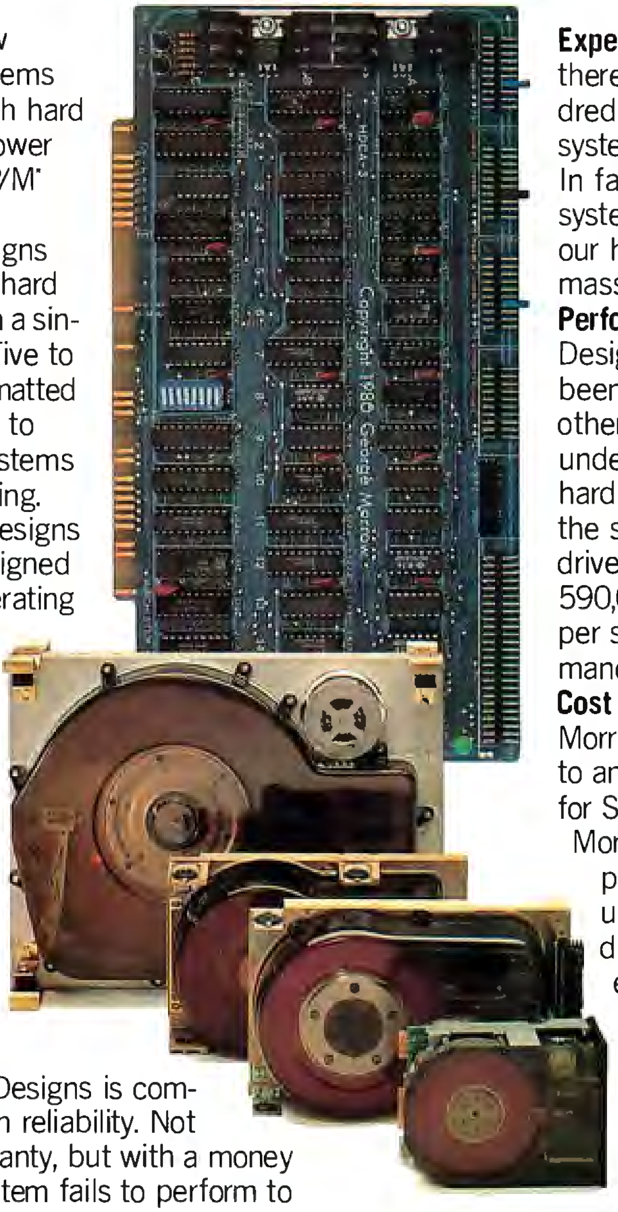

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preceding step. Table 4 shows the values I obtained with the prototype.

If you do not get what my calculus instructor called a "monotonically increasing" set of voltages (see figure 13), you have a problem. In other words, if any successive output is *lower* than the previous one, you must recheck the resistance values. One of your resistors is probably "out of spec." If not corrected, this will lead to problems in determining the voltage level at the analog input.

Comparator outputs. Listings 2 and 3 show the comparator tests for Models I and III, respectively. This test steps the DAC from 0 through 63 (+0.25 V through +4.75 V) and displays the step number, X input, and Y input. The X and Y inputs will be either 0 or 1.

If the input is a 0, the X or Y voltage is less than the current DAC voltage. Move the joystick and observe that the comparator inputs change. Moving the joystick to the upper-left corner should reset both comparator inputs to 0 after several steps, for example. Also observe that when the input changes from 0 to 1, all successive inputs remain at 1. If there is a 1 followed by several zeros, you have the "not monotonically increasing" problem (in case you didn't have a voltmeter to diagnose it previously). If so, recheck the resistance values in the DAC array (RN1).

If all seems well with this test, you're ready for a machine-language driver for the joysticks.

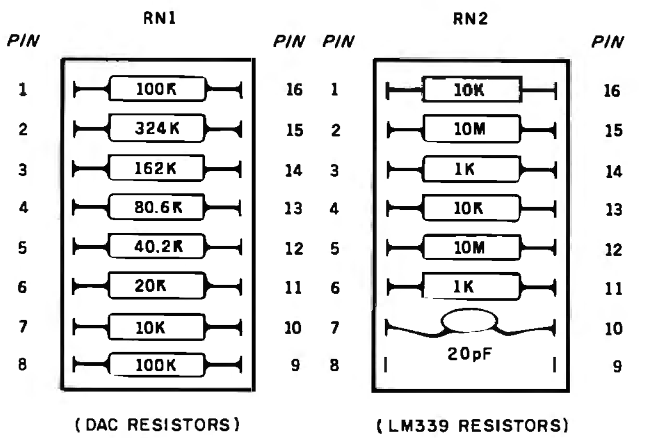

Figure 12: *Layouts for the DIP headers. One position on RN2 is not used.*

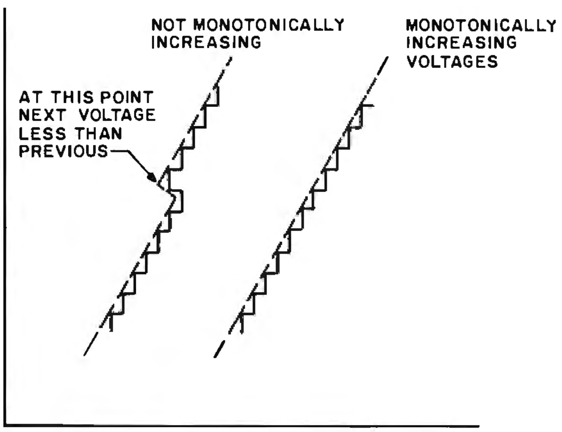

Figure 13: *For digital inputs from 0 to 63, the output from the DAC should increase monotonically (as in the curve on the right). Otherwise, the A/D circuit will give invalid readings for analog values in that voltage region.*

Joystick Software

Listings 4 and 5 show Z80 assembly-language drivers for the Model I and III, respectively. The only difference is that one uses a memory-mapped LD instruction; the other uses I/O-mapped INs and OUTs. Both programs are completely relocatable even though they are assembled at hexadecimal address 8000.

You can reassemble using your own editor/assembler or simply key in the object code using DEBUG. Another alternative is to convert the hexadecimal code to decimal and incorporate the 62 bytes in DATA statements that can then be READ and POKEd into a block of memory.

The calling sequence in Disk BASIC, the same for Model I and III, is shown in listing 6. This program clears the screen and defines the USR0 routine at hexadecimal address 8000. Next, a call is made to the USR0 routine. The X,Y position of the joystick is returned in variable A. The X position is in the most-significant byte; the Y position is in the least-significant byte.

Both X and Y are returned as values of 0-63. For display purposes, the X value (B) is multiplied by 2 and used in a SET command. The Y value is converted from a range of 0-63 to a range of 0-48 and used in the same SET command. As long as the cursor position remains fixed, one pixel of the SET appears on the screen. If the joystick is moved, the last pixel is RESET and the new one is SET. The result is a joystick-controlled cursor.

The pixel may have a tendency to jump from one spot to another. This is normal and occurs when the reference increment is close to the input-voltage value. For most positions, however, pixel motion will be reasonably steady. Although a resolution of 64 X and 48 Y is not very precise, it is more than adequate for positioning the cursor. The mechanical limitations of the joystick make it very difficult to avoid vertical "drift" when moving horizontally; therefore, greater resolution, as with 7 bits instead of 6, would be wasted.

How the Program Works

The programs in listings 4 and 5 consist of two parts. SRCHJY is the actual search program that finds the comparator value for the current joystick channel. This program is called twice by the driver routine READJY. The CALL is made by loading the C register with 128 or 64 and executing a JR instruction to SRCHJY.

The value in C serves two purposes—it acts as a flag for the return point and serves as a mask value for the X/Y comparator bit. The X-channel comparator bit is found by performing a logical AND of the A/D input with 128. The Y-channel comparator bit is found by performing a logical AND of the A/D input with 64.

Text continued on page 184

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Listing 5: *The same as listing 4, but for the Model III.*

```
8000          00100           ORG     8000H
              00110 ;*********************************************************
              00120 ;* SUBROUTINE TO READ JOYSTICK                            *
              00130 ;*       ENTRY: NO PARAMETERS                             *
              00140 ;*       EXIT:  (H,L)=X VALUE 0-63, Y VALUE 0-63          *
              00150 ;* SUBROUTINE IS RELOCATABLE ANYWHERE IN RAM. SUBROU-    *
              00160 ;* TINE IS SETUP FOR STANDARD MODEL I/III BASIC USR     *
              00170 ;* CALL.                                                 *
              00180 ;*********************************************************
              00190 ;
8000 0E80     00200 READJY  LD      C,128           ;MASK FOR X
8002 180A     00210         JR      SRCHJY          ;READ X VALUE
8004 F5       00220 REA010  PUSH    AF              ;SAVE X VALUE
8005 0E40     00230         LD      C,64            ;MASK FOR Y VALUE
8007 1805     00240         JR      SRCHJY          ;READ Y VALUE
8009 E1       00250 REA020  POP     HL              ;X TO H
800A 6F       00260         LD      L,A             ;Y TO L
800B C39A0A   00270         JP      0A9AH           ;***BASIC RTN***
              00280 ;
              00290 ;*********************************************************
              00300 ;* SUBROUTINE TO SEARCH FOR X OR Y VALUE                 *
              00310 ;*       ENTRY: (C)=128 FOR X, 64 FOR Y                   *
              00320 ;*       EXIT:  (A)=ANALOG VALUE 0-63                     *
              00330 ;* SUBROUTINE FINDS ANALOG VALUE WITH 8 RETRIES.         *
              00340 ;*********************************************************
              00350 ;
800E 21FFFF   00360 SRCHJY  LD      HL,-1           ;DUMMY VALUE FOR COMPARE
8011 E5       00370         PUSH    HL              ;INITIALIZE LAST VALUE
8012 0608     00380         LD      B,8             ;8 TRIES
8014 1640     00390 SRC005  LD      D,40H             ;START VALUE=64
8016 1E20     00400         LD      E,20H             ;START DELTA=32
8018 CB1A     00410 SRC010  RR      D                   ;ALIGN TO H'WARE FORM
801A 7A       00420         LD      A,D                 ;PUT IN A FOR OUTPUT
801B D3F8     00430         OUT     (0F8H),A            ;OUTPUT VALUE TO DAC
801D CB12     00440         RL      D                   ;BACK TO SCALED DELTA
801F DBF8     00450         IN      A,(0F8H)            ;GET COMPARATOR INP
8021 A1       00460         AND     C                   ;TEST CHANNEL
8022 7A       00470         LD      A,D                 ;CURRENT VALUE TO A
8023 2003     00480         JR      NZ,SRC020           ;GO IF COMP=1
8025 83       00490         ADD     A,E                 ;TOO LOW-ADD 1/2
8026 1801     00500         JR      SRC030              ;CONTINUE
8028 93       00510 SRC020  SUB     E                   ;TOO HIGH-SUB 1/2
8029 57       00520 SRC030  LD      D,A                 ;SAVE ADJUSTED VALUE
802A CB3B     00530         SRL     E                   ;DELTA/2
802C 20EA     00540         JR      NZ,SRC010           ;GO IF DELTA NOT 0
802E CB3A     00550         SRL     D                 ;CONVERT TO 0-63 FORM
8030 F1       00560         POP     AF                ;GET LAST VALUE
8031 BA       00570         CP      D                 ;TEST WITH CURRENT
8032 D5       00580         PUSH    DE                ;SAVE CURRENT
8033 2802     00590         JR      Z,SRC040          ;GO IF EQUAL
8035 10DD     00600         DJNZ    SRC005            ;NOT EQUAL-8 RETRIES
8037 F1       00610 SRC040  POP     AF              ;RESTORE LAST
8038 CB79     00620         BIT     7,C             ;TEST FOR RETURN POINT
803A 20C8     00630         JR      NZ,REA010       ;X CASE
803C 18CB     00640         JR      REA020          ;Y CASE
8000          00650         END     READJY
00000 Total errors
```

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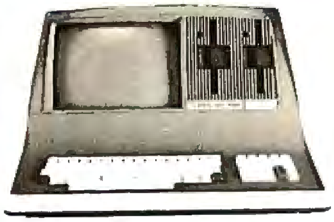

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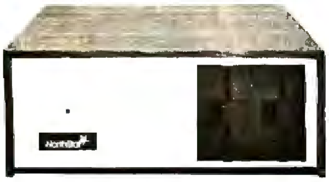

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Listing 4: *Z80 assembly-language subroutine to read both channels of the joystick input (Model I version).*

```
8000          00100         ORG     8000H
              00110 ;*******************************************************
              00120 ;* SUBROUTINE TO READ JOYSTICK                         *
              00130 ;*      ENTRY: NO PARAMETERS                           *
              00140 ;*      EXIT:  (H,L)=X VALUE 0-63, Y VALUE 0-63        *
              00150 ;* SUBROUTINE IS RELOCATABLE ANYWHERE IN RAM. SUBROU-  *
              00160 ;* TINE IS SETUP FOR STANDARD MODEL I/III BASIC USR    *
              00170 ;* CALL.                                               *
              00180 ;*******************************************************
              00190 ;
8000 0E80     00200 READJY  LD      C,128          ;MASK FOR X
8002 180A     00210         JR      SRCHJY         ;READ X VALUE
8004 F5       00220 REA010  PUSH    AF             ;SAVE X VALUE
8005 0E40     00230         LD      C,64           ;MASK FOR Y VALUE
8007 1805     00240         JR      SRCHJY         ;READ Y VALUE
8009 E1       00250 REA020  POP     HL             ;X TO H
800A 6F       00260         LD      L,A            ;Y TO L
800B C39A0A   00270         JP      0A9AH          ;***BASIC RTN***
              00280 ;
              00290 ;*******************************************************
              00300 ;* SUBROUTINE TO SEARCH FOR X OR Y VALUE               *
              00310 ;*      ENTRY: (C)=128 FOR X, 64 FOR Y                 *
              00320 ;*      EXIT:  (A)=ANALOG VALUE 0-63                   *
              00330 ;* SUBROUTINE FINDS ANALOG VALUE WITH 8 RETRIES.       *
              00340 ;*******************************************************
              00350 ;
800E 21FFFF   00360 SRCHJY  LD      HL,-1          ;DUMMY VALUE FOR COMPARE
8011 E5       00370         PUSH    HL             ;INITIALIZE LAST VALUE
8012 21E837   00380         LD      HL,37E8H       ;PRINTER ADDRESS
8015 0608     00390         LD      B,8            ;8 TRIES
8017 1640     00400 SRC005  LD      D,40H            ;START VALUE=64
8019 1E20     00410         LD      E,20H            ;START DELTA=32
801B CB1A     00420 SRC010  RR      D                  ;ALIGN TO H'WARE FORM
801D 72       00430         LD      (HL),D             ;OUTPUT VALUE TO DAC
801E CB12     00440         RL      D                  ;BACK TO SCALED DELTA
8020 7E       00450         LD      A,(HL)             ;GET COMPARATOR INP
8021 A1       00460         AND     C                  ;TEST CHANNEL
8022 7A       00470         LD      A,D                ;CURRENT VALUE TO A
8023 2003     00480         JR      NZ,SRC020          ;GO IF COMP=1
8025 83       00490         ADD     A,E                ;TOO LOW-ADD 1/2
8026 1801     00500         JR      SRC030             ;CONTINUE
8028 93       00510 SRC020  SUB     E                  ;TOO HIGH-SUB 1/2
8029 57       00520 SRC030  LD      D,A                ;SAVE ADJUSTED VALUE
802A CB3B     00530         SRL     E                  ;DELTA/2
802C 20ED     00540         JR      NZ,SRC010          ;GO IF DELTA NOT 0
802E CB3A     00550         SRL     D                ;CONVERT TO 0-63 FORM
8030 F1       00560         POP     AF               ;GET LAST VALUE
8031 BA       00570         CP      D                ;TEST WITH CURRENT
8032 D5       00580         PUSH    DE               ;SAVE CURRENT
8033 2802     00590         JR      Z,SRC040         ;GO IF EQUAL
8035 10E0     00600         DJNZ    SRC005           ;NOT EQUAL-8 RETRIES
8037 F1       00610 SRC040  POP     AF             ;RESTORE LAST
8038 CB79     00620         BIT     7,C            ;TEST FOR RETURN POINT
803A 20C8     00630         JR      NZ,REA010      ;X CASE
803C 18CB     00640         JR      REA020         ;Y CASE
8000          00650         END     READJY
00000 Total errors
```

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Text continued from page 176:

READJY calls SRCHJY twice and merges the result into the HL register for return. H will contain an X value of 0-63, and L a Y value of 0-63. The JP 0A9AH is the standard BASIC method of returning an argument to BASIC from a machine-language subroutine. Convert this to a normal RET if the program will be "stand-alone" (non-BASIC).

The SRCHJY subroutine operates similarly to the Color Computer joystick subroutine discussed in last month's article. A successive-approximation, analog-to-digital conversion is performed. A start value of 32, or half the voltage range, is first output to the DAC and a "delta" value of 16 is initialized. The comparator output is then read in. Depending upon the comparator output, the next value tried is 32 plus or minus the delta. The delta is then halved. This successive approximation continues until the delta has been reduced to ½ unit (the value is "scaled up" by two to permit the last delta of ½).

As the input may change rapidly, eight tries are made to obtain a steady X or Y input value. The minimum number of times through SRCHJY will be two, the maximum eight. If the value does not match the previous value after eight tries, the last value is used.

Listing 6: *A BASIC program to call the joystick input subroutine (listings 4 and 5).*

```
100 REM JOYSTICK-CONTROLLED CURSOR
110 FOR I=15360 TO 16383
120 POKE I,128
130 NEXT I
140 D=0: E=0
150 DEFUSR0=&H8000
160 A=USR0(0)
170 B=INT(A/256)
180 C=(A-B*256)*47/63
190 IF (D<>B) OR (E<>C) THEN RESET (D*2,E)
200 SET (B*2,C)
210 D=B: E=C
220 GOTO 160
```

Other Uses for the A/D Circuit

In the previous article of this series, I described some "real-world" analog inputs that could be used in place of the joystick. Basically, anything that can be converted into a voltage can be used as an input to the DIN connector and converted to an increment of 0-63.

One example used was a cadmium sulfide photocell that had a variable resistance dependent upon the amount of light striking it. When used with a resistor in a divider network, a varying input voltage is generated. The second example used was a thermistor, a resistor whose resistance varied inversely to the temperature. These devices and many others may be connected to the A/D circuit in this fashion.

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Thirty More Days to a Faster Input

Edward M. Roberts
19 Smith St.
Glen Head, NY 11545

The program in Arthur Armstrong's article "Thirty Days to a Faster Input" was intended to help you learn touch-typing on a home computer. (See the December 1979 BYTE, page 250.) However, when I tried to copy his listing into my machine, it was a nightmare. The listing was apparently a facsimile of a printout done on an ancient Teletype. I finally decoded it, however, and modified it so that it would run on my Radio Shack TRS-80 running Level II BASIC.

Listing 1 shows my version of the program written the way I would have liked to have seen it—clear, nicely spaced, with the loops inset and the index variables spelled out in DO LOOPs (like NEXT I instead of just NEXT) for clarity. I hope BYTE readers enjoy using this program.■

Listing 1: *A typing program for the Radio Shack TRS-80. This is a modified version of a program given in the article "Thirty Days to a Faster Input," by Arthur Armstrong in the December 1979 BYTE.*

```
10 REM *** TYPING DRILL***
20 REM ** BY ART ARMSTRONG 9/8/77 **
30 REM * PUBLISHED 'BYTE' MAGAZINE 12/79 *
40 REM # ADAPTED TO R/S LEVEL II BASIC BY ED ROBERTS
   12/20/79 #
50 CLEAR 200
90 CLS: PRINT@ 145, "TYPING DRILL": PRINT
100 INPUT "WHAT CHARACTERS DO YOU WANT";C$
105 L = LEN(C$): DIM A(L)
110 INPUT "HOW MANY LETTERS IN EACH WORD"; WL
120 INPUT "DO YOU WANT ECHO"; A$
125 IF LEFT$(A$,1) = "Y" THEN E = 1
130 INPUT "HOW MANY TRIALS"; NT
195 CLS
200   FOR T = 1 TO NT
210   NP = NP + WL
220   A$ = " "
230     FOR I = 1 TO WL
240     R = INT(L * RND(0) + 1)
250     A$ = A$ + MID$(C$,R,1)
260     NEXT I
270   PRINT:PRINT CHR$(23): PRINT A$
300     FOR I = 1 TO WL
310     E$ = INKEY$: IF E$ = " " THEN 310
320     IF E = 0 THEN 350
330     PRINT E$;
350     IF E$ <> MID$(A$,I,1) THEN 500
360     NR = NR + 1
370     NEXT I
375   IF E = 1 THEN PRINT
380   NEXT T
400 CLS:PRINT:PRINT "YOUR SCORE IS "; INT(100 * NR/NP);"%"
402 IF NR = NP THEN 415
405   PRINT "ERRORS:":FOR I = 1 TO L: IF A(I) = 0 THEN 410
407   PRINT MID$(C$,I,1);A(I)
410   NEXT I
415 PRINT: INPUT "SELECT:
         REPEAT W/ SAME SPECS, CUME SCORING & ERRORS
         (R)
         REPEAT WITH NEW SPECIFICATIONS (N)
         DONE — GOODNIGHT — (D)          ";A$
420 IF A$ = "R" THEN 195
425 IF A$ = "N" THEN 50
430 IF A$ = "D" PRINT:PRINT " SAY GOODNIGHT,
    GRACIE.":END
500   FOR J = 1 TO L
510   IF MID$(C$,J,1)<>MID$(A$,I,1) THEN NEXT J: GOTO 520
515 A(J) = A(J)+1
520 PRINT:PRINT "ERROR ON "; MID$(A$,I,1)
530   FOR I = 1 TO 300: NEXT I
540 GOTO 380
550 END
```

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Troubleshooting with Electronic Signatures

Kenneth M. Piggott
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Until recently, the tools available for finding hardware errors in microprocessor systems have been meager. Logic probes are satisfactory for detecting logic levels and the presence of pulses but are unable to detect errors in data streams. An oscilloscope is of limited use because all data pulses tend to look alike. Logic analyzers let you store long data streams (250 bits and longer) for later evaluation. But in order to check for single-bit errors, each bit stored has to be compared to a known good pattern (a long and tedious job). Additionally, using a logic analyzer generally requires a certain amount of expertise. A technique known as *signature analysis*, however, allows easy detection of hardware-related data-stream errors.

Signature Analysis

Signature analysis is a technique, pioneered by Hewlett-Packard, that detects errors in data streams caused by hardware failure. Much as waveforms in an analog circuit being tested can be compared with ideal waveforms shown on a schematic, signatures derived from a digital system can be compared with known good signature values in order to isolate defective components. Single-bit errors can be detected with greater than 99.99 percent certainty using signature analysis.

Signature analysis reduces a data stream into a four-digit hexadecimal sequence. This four-digit sequence is the signature. By supplying known data streams to a digital system, unique signatures can be obtained at various points in the circuit. These correct signatures can be recorded and later compared with the results obtained from a malfunctioning system. (Any signatures that are different indicate a problem.) With proper documentation and troubleshooting procedures, the faulty components causing the hardware failures can be pinpointed.

With signature analysis, single-bit errors can be detected with almost 100% accuracy.

One of the real advantages of signature analysis is that only one data line is sampled at a time. In the case of bus-oriented microprocessors, it is very easy to check each individual address-bus line and detect such difficult problems as shorts between two bus lines.

Inside an Analyzer

The basic component of the signature analyzer is a 16-bit shift register. Data is shifted through the register by means of a clock signal supplied by the system under test. This signal indicates when the data is valid. Connected to the input of the shift register is the output of a modulo-2 adder. There are two groups of inputs to the adder. One is the incoming data stream and the other is feedback from the shift register.

If an incorrect bit is in the data stream, it will be shifted and fed back, so an incorrect output from the modulo-2 adder will result. This result enters the shift register and is again shifted and fed back; it will again affect future inputs to the shift register. This process will repeat until a stop signal is received. The remaining contents in the shift register result in an incorrect four-digit signature on the unit's hexadecimal display.

In order to generate a signature, certain control signals are required. The first is the start signal, which tells the signature analyzer when the data stream starts and resets all the bits in the shift register to logic 0. Note that this and all other control signals are *edge-triggered* signals that may be selected to trigger on either the positive- or the negative-going edge.

The next signal of interest is the clock signal. Do not confuse this signal with the microprocessor clock. The clock signal is used to indicate when the incoming data to the signature analyzer is valid.

The last control signal of concern is the stop signal, which initiates the transfer of the contents of the shift register to the displays. In the reference literature, the period between the start and stop signals is often referred to as the *measurement window*.

A Simplified Example

Let's look at a simplified example with a 4-bit shift register and one

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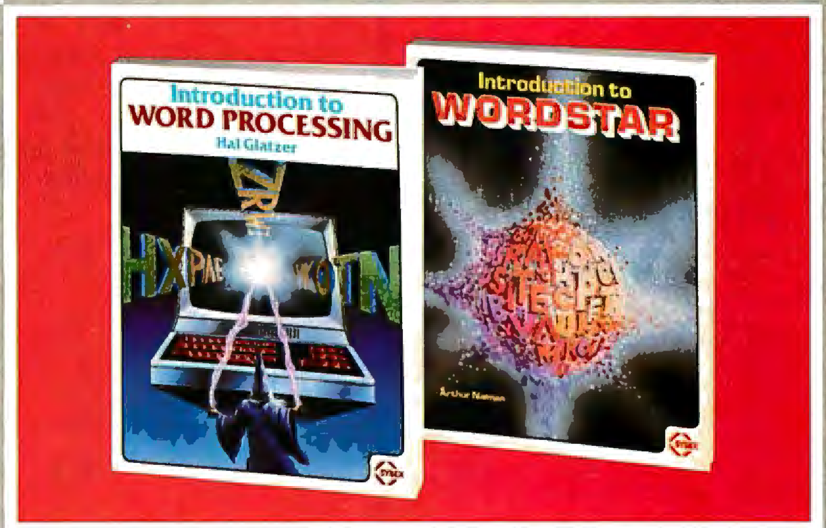
THE WORD FROM SYBEX . . .



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feedback point that will generate a single-hexadecimal-digit signature (see figure 1 and table 1). For convenience, let's substitute an exclusive-OR gate for the adder, as it will perform the same function as a modulo-2 adder when only one feedback path in addition to the input signal is present.

The output of the exclusive-OR gate goes to the input of the shift register. (An exclusive-OR gate is similar to an OR gate except that when two logic 1s are presented to the inputs, the output is a logic 0.) In this example, the feedback path is from the third bit of the shift register to the input of the exclusive-OR gate. (In the 16-bit shift register version, the four feedback paths are from bits 7, 9, 12, and 16.)

In the correct signature example, when the start pulse is applied, the bits in the shift register are all set to logic 0. At the end of the third clock pulse, a logic 1 is fed back to the input of the exclusive-OR gate. Since the fourth data bit is a logic 0, the input to the shift register is a logic 1. When the data stream is completed and the stop signal is received, the bits present in the shift register are transferred to the display register and an "H" is displayed. (For clarity, the output digits are represented by one of the numerals 0 through 9 or the letters A,

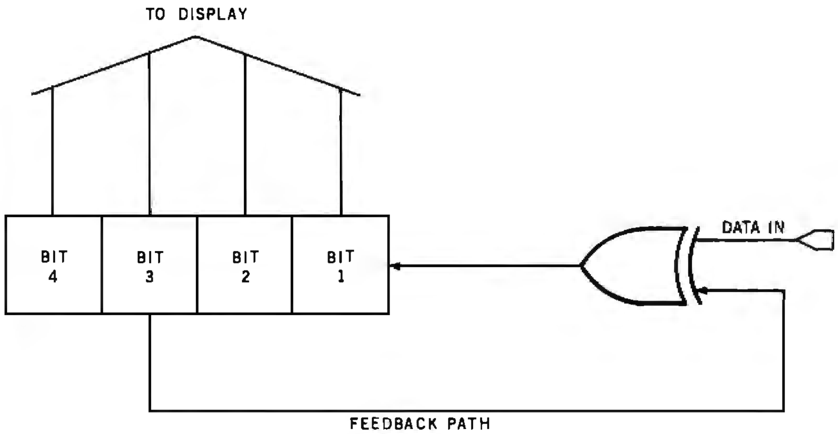


Figure 1: *A simplified version of a signature analyzer. In this scaled-down unit, only four bits are used in a shift register (as opposed to 16), and a simple exclusive-OR gate is used in place of the adder. Each bit of the incoming data stream is fed back to the exclusive-OR gate as it reaches the third position in the shift register.*

	Correct Signature Data Stream = 10101010		Incorrect Signature Data Stream = 10001010	
Control Signal	Shift Register Contents	Data Remaining	Shift Register Contents	Data Remaining
Start	0000	10101010	0000	10001010
Clock (1)	0001	0101010	0001	0001010
(2)	0010	101010	0010	001010
(3)	0101	01010	0100	01010
(4)	1011	1010	1001	1010
(5)	0111	010	0011	010
(6)	1111	10	0110	10
(7)	1110	0	1100	0
(8)	1101		1001	
Stop				
Displayed Digit	H		9	

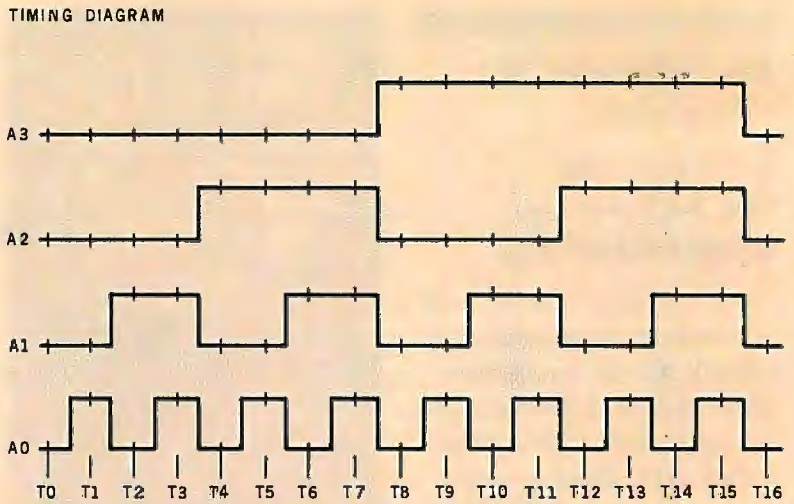
Table 1: *The contents of the shift register as two slightly different data streams are fed in. In the incorrect signature example, the third bit from the left has been changed from a 1 to a 0; the final results (after the eighth clock pulse) are quite different.*

C, F, H, P, or U, instead of the conventional hexadecimal digits.) Keep in mind that in the actual device the shift register is 16 bits long and the actual signature is four digits.

To demonstrate the effectiveness of the technique, let's look at the same example with the third bit in the data stream set to logic 0 instead of logic 1, to simulate an error (see the incorrect signature example in table 1). Notice that after the third clock pulse, an incorrect bit has entered the shift register. After the fifth clock pulse, this incorrect bit is at the feedback point, which results in an incorrect bit entering the shift register on the sixth clock pulse. After the stop pulse is received, a "9" is transferred to the display. The correct display should have been an "H".

Applying Signature Analysis

The premise behind signature analysis is that known data streams can be generated by the system. One approach to doing this for microcomputer systems is to have a diagnostic program stored in memory that generates the required data streams. It is then possible to isolate faults at the component level in various parts of the unit under test. This approach, however, is best incorporated into the initial design of a product and, unfortunately, does not help those who already have computer systems; very few personal



Signatures of a Free-running Microprocessor

It is necessary to recall how a microprocessor operates in order to see how the data stream is generated for use in free-running analysis. When a reset occurs, the program counter in the microprocessor is set to 0000 and the data stored at memory location 0000 is accessed on the next instruction-fetch cycle.

However, when a free-running analysis is occurring, a NOP instruction is placed on the data-in bus to the microprocessor. As a result, after reset occurs, the only action that the microprocessor takes is to read the next memory location (where a NOP instruction is encountered) and increment the program counter.

This process will repeat as long as a NOP instruction is present on the data bus; but note what occurs when the program counter reaches hexadecimal FFFF. A NOP instruction is encountered, and the program counter increments to 0000. As the cycle repeats, the memory space is sequentially accessed, and the resulting data stream generated on the address lines provides the known data stream required for signature generation.

The timing diagram above shows the data streams generated on address lines A0 through A3. Only four address lines are shown for clarity, but the patterns on address lines A4 through A15 are similarly generated. The pattern shown will repeat as long as the microprocessor is in the free-running mode.

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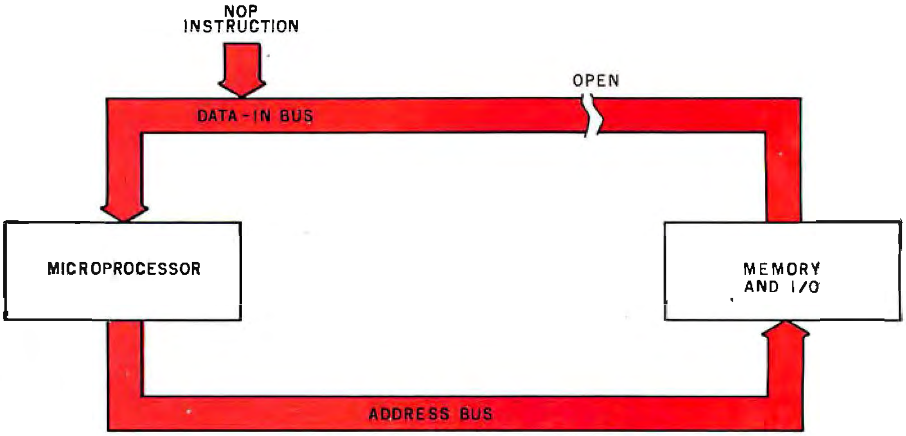

Figure 2: *One method for generating signals for signature analysis. The data-in bus is opened, and a NOP instruction is forced on the bus. This causes the processor to constantly increment the program counter, so that a stream of values appears on each address line. Interrupts should be disabled.*

computers have provision for signature analysis.

Fortunately, there is a signature-analysis technique, called *free-running* signature analysis, that can be applied to existing systems. Free-running analysis derives its name from the manner in which the data streams are generated. Unlike the diagnostic-program method, which uses a program to generate the data-bit stream, the free-running method allows the microprocessor to continually increment its 16 address lines.

While free-running analysis does not supply as much testing capability as a built-in diagnostic program, it will generate a known data stream on each of the 16 address lines, check the microprocessor for basic operation, and check the operation of the data-in bus. (See the text box Signatures of a Free-running Microprocessor on page 194.) Additionally, other parts of the circuitry that use the address bus can use these data streams for the generation of signatures.

In order to use free-running analysis, two important hardware requirements must be met. First, the feedback loop within the processor must be opened (see figure 2). In most cases, this means opening the incoming bus lines. Second, a NOP (no operation) instruction must be inserted on the data-in bus. (In the case of the Z80 microprocessor, the NOP instruction is hexadecimal 00.)

Fulfilling these two requirements can be accomplished in several ways. If the system has input buffering on the processor board, as most S-100 systems do, the data-in lines can be disabled by removing the buffering devices and replacing them with a dual-inline header that has the NOP instruction hardwired on it. If you are lucky, the integrated circuits will be socketed and easy to remove. If not, they should be unsoldered, removed, and replaced with sockets to facilitate this operation. Any instruction internal to the microprocessor, such as an arithmetic or logical instruction, can be used in place of a NOP instruction, as it will perform the same function—incrementing the program counter to the next address without accessing the data-in bus.

For some S-100 users, the procedure of setting up for signature analysis is easier. The Ithaca Audio (now Ithaca Intersystems) Z80 board has a feature that causes the microprocessor to jump to a preset address upon reset. This transfers control to a monitor program whenever a reset occurs. The data-in buffer from the S-100 bus is disabled, and a NOP instruction is placed on the board's internal data-in bus. The program counter, which is reset to 0, increments each time the NOP instruction is encountered. This incrementing of the program counter continues until the program counter reaches the beginning address of the monitor pro-

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*CP/M REGISTERED TRADEMARK DIGITAL RESEARCH gram. An on-board decoder detects that the program counter has reached the proper address, removes the NOP instruction from the data-in bus, and enables the S-100 data-in buffer. The address at which all this happens is user-selectable through a set of switches mounted on the board. If all the switches are open, no decoding address is selected, and the program counter will increment continuously. This, in essence, gives you the capability to do a free-running signature analysis simply by performing the following operations:

1. Open all the jump-address switches (switch at IC28 on the Ithaca Intersystems Z80 board).
2. Enable the auto-jump on reset.
3. Connect the Start and Stop lines to A15 (pin 32 on the S-100 bus). Select falling-edge trigger on the signature-analyzer probe.
4. Connect the Clock line to sMEMR (pin 47 on the S-100 bus). Select rising-edge trigger on the signature-analyzer probe.
5. Turn on power to the system and reset.

When the above steps are performed, the individual address lines can be probed with the signature-analyzer probe, and if they are functioning normally, the results will be as shown in table 2. Any other reading indicates a problem with the hardware, assuming, of course, that the setup of the analyzer is correct.

This illustrates another major advantage of signature analysis. The interpretation of the signature is based on a "go/no-go" technique. If the signature observed differs by even one digit from the signature known to be correct, a problem is indicated. Regardless of the type of processor used in the system, as long as the processor can be set up for free-running analysis and has 16 address lines, the results shown in table 2 are valid.

For applications in systems other than that described above, refer to the references listed at the end of this article.

Troubleshooting Techniques

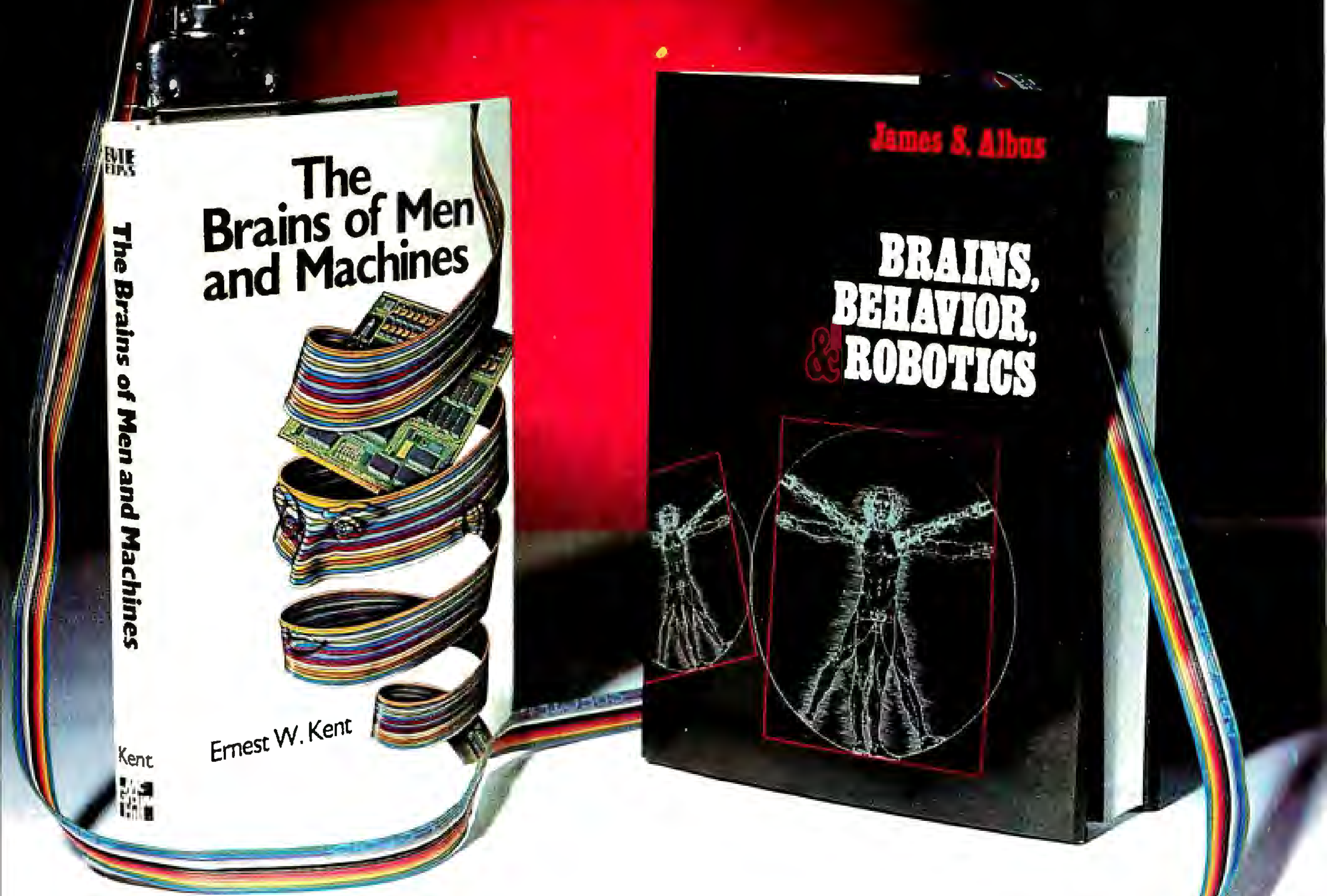
Troubleshooting when using signature analysis can be done in several ways. One is to start with the processor and continue checking with additional buffers, gates, etc., until a bad signature is found. Ideally, the faulty hardware will lie somewhere between the bad reading and the previous good reading.

An equally valid troubleshooting technique is to take a reading midpoint in the circuit. If a bad reading is

Signal Name	S-100 Pin	Signature	Analyzer Control Line	Trigger Edge
Ground	50 and 100	—	Ground	—
sMEMR	47	—	Clock	Rising
A0	79	UUUU	—	—
A1	80	5555	—	—
A2	81	CCCC	—	—
A3	31	7F7F	—	—
A4	30	5H21	—	—
A5	29	OAFA	—	—
A6	82	UPFH	—	—
A7	83	52F8	—	—
A8	84	HC89	—	—
A9	34	2H70	—	—
A10	37	HPPO	—	—
A11	87	1293	—	—
A12	33	HAP7	—	—
A13	85	3C96	—	—
A14	86	3827	—	—
A15	32	755U	Start	Falling
A15	32		Stop	Falling

Table 2: *Signals of interest on the S-100 bus. Using free-running analysis, many portions of an S-100 computer sytstem can be tested. The signatures are the same for all computers that use a 16-bit address.*

Mindful Machines



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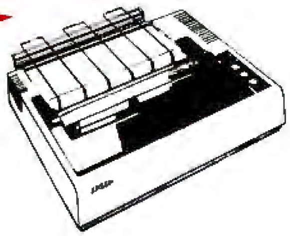

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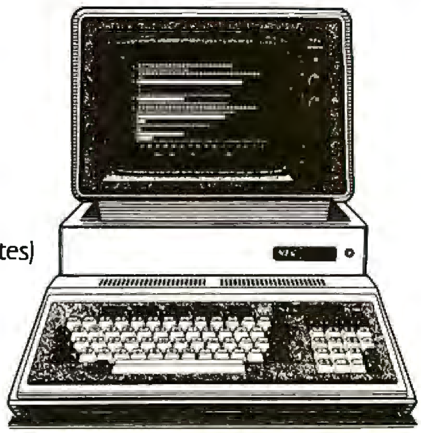

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discovered, a new reading midway between the processor and the bad reading is made. In this way, the bad component will eventually be located through elimination. Conversely, if a good reading is found at the midpoint, the same technique is used, but in the other half of the circuit.

A good compromise is to take the initial readings at the S-100 bus lines, which can be accomplished quite easily with the aid of an extender board. This will very quickly indicate if the problem is on the processor board or elsewhere.

It is possible to test the other boards in the system, but keep in mind that the signatures obtained on the boards will vary as the board addresses are changed. Therefore, it is important that signature readings and the switch settings be recorded on the schematic or on a table when the system is set up initially (see figure 3 and table 2). This will give you something to compare your readings with when a problem does occur.

Memory devices, ROMs (read-only memories), and I/O (input/output) circuits, asynchronous and otherwise, can be checked with the signature-analysis technique. Most often this is done with the aid of

Operating B&K Precision's Model SA-1010 Signature Analyzer

One instrument that will perform signature analysis is the B&K Precision Model SA-1010. It consists of a measurement unit containing the circuitry required to generate the signature, and SP1 control and data probes, which are attached to the basic unit with a connector.

The SP1 probe assembly consists of a control probe and a data probe. The control probe provides the control-signal interface between the system under test and the signature analyzer. The pod also contains switches to select positive- or negative-edge triggering of the control signals. Additionally, a switch is provided to select between CMOS (complementary metal-oxide semiconductor) and TTL (transistor-transistor logic) threshold levels.

The data probe is used to sample the data stream being measured. Built into the probe is a logic probe, which has LEDs (light-emitting diodes) to indicate the presence of high and low logic levels and pulses. The pulse LED will remain lit for a minimum of 100 ms, allowing the user to observe pulses as short as 10 ns. Also on the probe is a reset button that is used in conjunction with the hold button on the signature analyzer.

The SA-1010 unit contains a 4-digit display, used to show the signatures from the system being tested. To the left of the display is a Gate LED that, when lit, indicates that a measurement is being made. To the right of the display is an Unstable Signature LED. The Unstable Signature LED lights whenever the current signature reading is different from the previous reading. This is useful in tracking down intermittent faults.

Under the display are three switches. The left switch is the Power switch. In the middle is the Hold switch. When the Hold switch is depressed and the reset button on the SP1 data probe is pushed, a new signature will be generated and "held" on the display. When the Hold switch is in the extended position, signatures will be generated as long as a data stream is being sampled. The switch on the right is the Unstable Hold switch. When pressed, it will latch the Unstable Signature LED on whenever a change from one reading to the next occurs. To reset the Unstable Signature LED, the Unstable Hold button should be returned to the extended position. When in the extended position, the Unstable Signature LED will be lit only from the time a difference in two readings occurs until two consecutive identical readings are made.

Above the data-probe connector are connectors used to self-test the unit. When the control and data probe signals are connected to the appropriate points on the front panel, a signature of 0055 will be displayed if the instrument is functioning properly.

On the back panel is an output connector for an internally generated 1 MHz TTL-level clock. This clock can be used if the circuit under test has been removed from a system and clock pulses are required to drive the circuit.

The SA-1010 has a maximum operating speed of 20 MHz. Data must be present on the input line for a minimum of 10 ns prior to the clock pulse. No hold time is required after the clock pulse.

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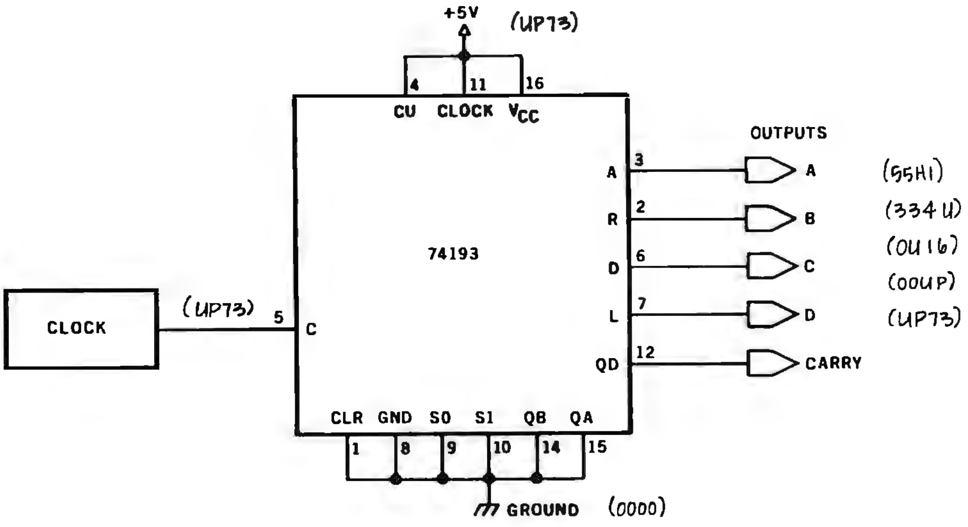

SIGNATURE ANALYZER HOOKUP

CONTROL SIGNAL	TRIGGER EDGE	IC PIN
START	FALLING	7
STOP	FALLING	7
CLOCK	FALLING	5
GROUND		8

Figure 3: *An example of how a schematic diagram might be annotated to include signatures.*

special diagnostic programs developed for the system. For more information, consult the references listed at the end of this article.

Conclusion

Signature analysis is a troubleshooting technique that is invaluable in locating hardware faults in complicated microprocessor circuits. To make maximum use of the technique, special programs should be used. However, since most systems do not presently incorporate this capability, free-running analysis is a viable alternative. The major limitation of signature analysis should be reemphasized: it is imperative that signatures be generated and recorded on the system before it breaks down. ■

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Analyze Audio by Visualizing

Dr. Thomas Phillips
22 Newton Ave.
Norwich, NY 13815

Listing 1 is a program that allows you to digitally record approximately 1 second of sound (a word, a phrase, or a musical note), play it back (forward or reverse), and display all or any portion of it on a video screen. A routine is included that allows reverberation with variable delay; both are in 8080 source code.

My system uses a Cromemco D+7A A/D (analog-to-digital) converter and a Cromemco Dazzler as the graphics display. To record 1 second of sound (at the maximum sampling rate), 28 K bytes of programmable memory (from hexadecimal 7000 to E000) are required. In addition to the 219 bytes of memory required by the program, 2 K are used by the Dazzler display (driven by a short point-plotting routine in low memory).

Listing 2 is a North Star BASIC program. It is the main control program and is used to alter the audio parameters. The reverberation routine allows a time delay (adjusted by setting the joystick on the Cromemco console, analog input port 26). As Tom O'Haver discussed in his article "Audio Processing with a Microprocessor" (June 1978 BYTE, page 166), a long delay gives a reverberation effect and a short delay causes a comb filter effect. With simple modification of the routine, phase phlanging could be performed.

Music enthusiasts can use this program to analyze individual notes of a particular instrument and to determine the amplitude of the major harmonics (via brute force or Fourier transformation). The results can help synthesize that instrument. (See Hal Chamberlin's "Advanced Real-Time Music Synthesis Techniques," April 1980 BYTE, page 70.)

The linguist can *graphically* demonstrate the subtle differences in enunciation, such as the unaspirated "Qui" in Spanish or French versus the aspirated "Key" in English. (See photos 1a and 1b.) Some experimentation may reveal "lie detector" applications involving vocal-stress analysis.

If you're a computer-speech experimenter, detailed analysis of vowel sounds and other phonemes can be made, which could help you develop software for speech simulation without the attendant hardware so common today. ■

Listing 1: *8080 routines for the audio-analysis program.*

```
P
* AAP  &  AAP2
*****************************************************************
*                                                             ***
*     AUDIO ANALYSIS PROGRAM                                  ***
*     BY TOM PHILLIPS 11-30-79                                ***
*     TO BE LOADED AT 0600H                                   ***
*                                                             ***
*   FUNCTIONS:                                                ***
*     1  INPUT VOICE SAMPLE                                   ***
*     2  PLAY VOICE SAMPLE FORWARD                            ***
*     3  PLAY VOICE SAMPLE BACKWARD                           ***
*     4  REVERBERATION (VARIABLE)                             ***
*     5  DISPLAY EACH POINT SAMPLED FROM 7000H TO E000H       ***
*     6  DISPLAY EACH POINT (IN NARROWER RANGE)               ***
*                                                             ***
*****************************************************************
        JMP    2028H          JUMP TO NORTH STAR DOS
START   JMP    CONS           JUMP TO MAIN ROUTINE
PPC     DB     253            POINTS PER COLUMN
TOP     DB     0E0H           TOP ADDRESS IN H OF HL
BOT     DB     070H           BOTTOM ADDRESS IN D OF DE
****************************************************************
*
* THIS ROUTINE COLLECTS THE INPUT SAMPLE IN RAM BUFFER
*
****************************************************************
INPUT   LXI    H,07000H       HL -> BOTTOM (BEGINNING) OF SAMPLE
        LXI    B,0E000H       BC -> TOP (END) OF SAMPLE
INP     IN     27             GET BYTE FROM A-D PORT
        MOV    M,A            PUT IN SAMPLE BUFFER
        INX    H              INCREMENT POINTER
        MOV    A,H
        CMP    B              TOP OF SAMPLE?
        JZ     CONS           YES, GO TO CONSOLE
        JMP    INP            NO, GET NEXT BYTE
*********************************************************************
*
* THIS IS THE MAIN ROUTINE WHICH SCANS THE CROMEMCO CONSOLE
* 254 = 1       245 = 4 & 2
* 253 = 2       246 = 4 & 1       (BYTE AT PORT 24 = BUTTONS DEPRESSED)
* 251 = 3       243 = 4 & 3
*
*********************************************************************
CONS    NOP
        IN     24             SCAN CONSOLE
        CPI    254            IS IT 1 ?
        JZ     INPUT          YES, GET AUDIO INPUT SAMPLE
        CPI    253            IS IT 2 ?
        JZ     PLAY           YES, PLAY SAMPLE
        CPI    251            IS IT 3 ?
        RZ                    YES, RETURN TO BASIC CONTROL
        CPI    245            IS IT 4 & 2 ?
        JZ     BACK           YES, PLAY SAMPLE BACKWARDS
        CPI    246            IS IT 4 & 1 ?
        JZ     REVRB          YES, GO REVERBERATE
        CPI    243            IS IT 4 & 3 ?
        JZ     WAVE           YES, DISPLAY WAVE
        JMP    CONS           NO, GO RESCAN CONSOLE
*******************************************************
*
* THIS ROUTINE PLAYS THE SAMPLE FORWARDS
*
*******************************************************
PLAY    LXI    H,07000H       HL -> BOTTOM OF SAMPLE
        LXI    B,0E000H       BC -> TOP OF SAMPLE
PL      MOV    A,M            GET NEXT BYTE
        OUT    25             SOUND IT
        INX    H              INCREMENT POINTER
        MOV    A,H
        CMP    B              TOP OF SAMPLE?
        JZ     CONS           YES, JUMP TO CONSOLE
        JMP    PL             NO, GET NEXT BYTE OF SAMPLE
*********************************
*
* THIS ROUTINE IS THE SAME AS 'PLAY'
* EXCEPT IT PLAYS THE SAMPLE IN REVERSE
*
*********************************
BACK    LXI    H,0E000H
        LXI    B,07000H
BA      MOV    A,M
```

Listing 1 continued on page 208

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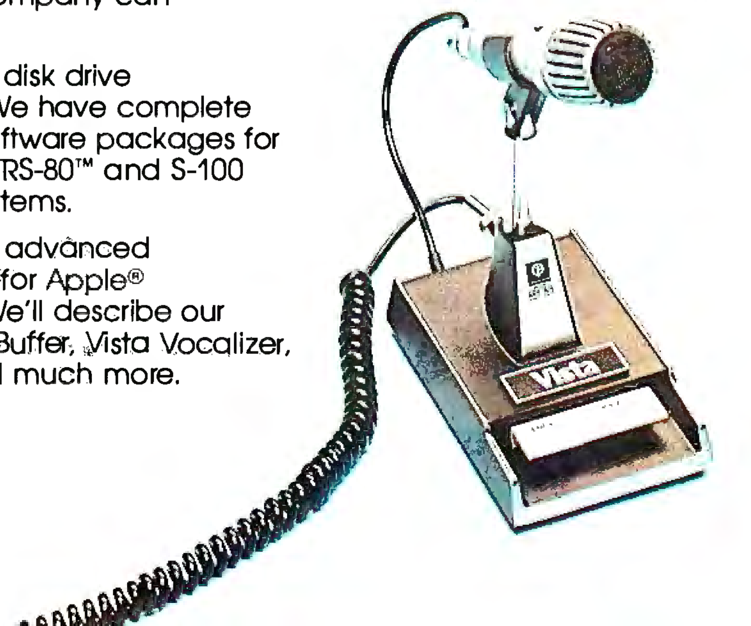

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```
        OUT   25
        DCX   H
        MOV   A,H
        CMP   B
        JZ    CONS
        JMP   BA
*******************************************
*
* THIS REVERBERATION ROUTINE TAKES THE
* INPUT SAMPLE CONTINUOUSLY & PLAYS IT
* BACK CONTINUOUSLY.  THE DELAY IS
* DETERMINED BY THE DIFFERENCE BETWEEN
* REGISTER PAIRS DE & BC.
*
*******************************************
REVRB   LXI   B,07000H       SET INPUT POINTER
        IN    26             GET REVERB DELAY BYTE
        SUI   30             SUBTRACT 30 TO CALIBRATE
        MOV   D,A            SET OUTPUT POINTER
        MVI   E,00H
REV     IN    27             GET VOICE BYTE
        STAX  B              PUT IT WHERE BC POINTS
INX     B     INCREMENT      INPUT POINTER
        LDAX  D              FILL A WITH OUTPUT POINTER BYTE
        OUT   25             SOUND IT
        INX   D              INCREMENT OUTPUT POINTER
        MOV   A,B
        CPI   0E0H           IS INPUT POINTER AT TOP?
        CZ    RSTB           YES, RESET TO BOTTOM
        MOV   A,D
        CPI   0E0H           IS OUTPUT POINTER AT TOP?
        CZ    RSTD           YES, RESET TO BOTTOM
        IN    24             CHECK CONSOLE
        CPI   251            IS 3 DEPRESSED?
        JZ    2A04H          YES, RETURN TO BASIC CONTROL
        CPI   247            IS 4 DEPRESSED ?
        JZ    REVRB          YES, GET NEW REVERB DELAY BYTE
        JMP   REV            NO, CONTINUE WITH SAME DELAY BYTE
RSTB    LXI   B,07000H
        RET
RSTD    LXI   D,07000H
        RET
*******************************************
*
* 'WAVE' DISPLAYS THE SAMPLE
* ON THE GRAPHICS DEVICE
*
* 'PIXEL' IS A USER SUPPLIED ROUTINE TO
* PLOT A POINT.
*
* 'X' IS A MEMORY LOCATION USED FOR STORAGE
* OF THE X-COORDINATE LOCATION.
*
* 'Y' IS A MEMORY LOCATION USED FOR STORAGE
* OF THE Y-COORDINATE LOCATION.
*
*******************************************
WAVE    NOP                  SET UP CONSTANTS
        MVI   A,1
        STA   SWB            TURN PIXEL ON
        MVI   A,0            X LOCATION=0 (BEGINNING OF SCREEN)
        STA   XLOC
        LDA   PPC            POINTS PER COLUMN IN B
        MOV   B,A
        LDA   TOP
        MOV   D,A            TOP IN DE
        MVI   E,0
        LDA   BOT
        MOV   H,A            BOTTOM IN HL
        MVI   L,0
WA      MOV   A,M            GET NEXT BYTE (AMPLITUDE)
        ADI   68             CALIBRATE CENTER OF SCREEN
        STA   Y              STORE AS Y-COORDINATE
        LDA   XLOC           GET X-COORDINATE
        DCR   B              DECREMENT PPC; LAST POINT?
        JNZ   W1             NO, CONTINUE
        INR   A              YES, INCREMENT X LOCATION
        PUSH  PSW            SAVE XLOC
        LDA   PPC
        MOV   B,A            RESET POINTS PER COLUMN
        POP   PSW            RESTORE XLOC
W1      STA   XLOC           STORE X LOCATION
        STA   X
        PUSH  D
        PUSH  B
        CALL  PIXEL          PLOT A POINT
        POP   B
        POP   D
        INX   H              INCREMENT POINTER
        MOV   A,H
        CMP   D              POINTER AT TOP?
        JM    WA             NO, GET NEXT BYTE
        JMP   CONS           YES, GO SCAN CONSOLE
PIXEL   EQU   10             PLOT A POINT
X       EQU   13             X LOCATION OF PIXEL
Y       EQU   14             Y LOCATION OF PIXEL
SWB     EQU   15             1=PIXEL ON  2=PIXEL OFF
XLOC    DB    0
*
```

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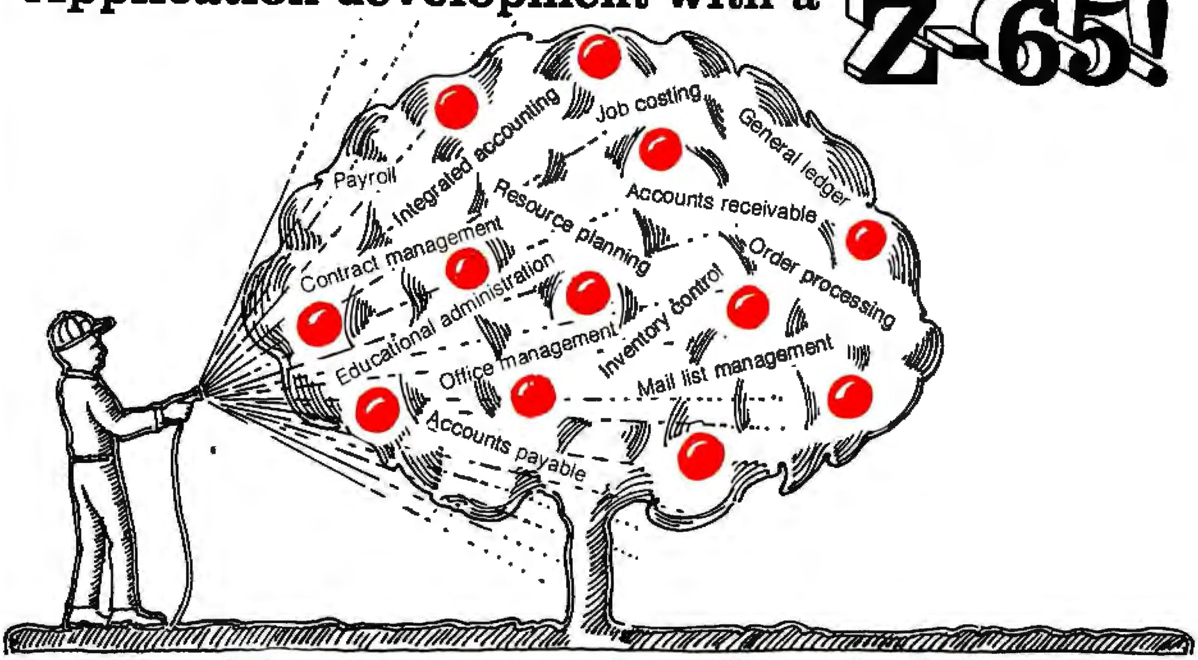

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Listing 2: *North Star BASIC driver program to be used with listing 1.*

```
LIST

100 !"BAAP  &  BAAP2"
110 REM
120 REM    BASIC AUDIO ANALYSIS PROGRAM (BAAP)
130 REM    INTEGRATED WITH MACHINE LANG ROUTINE AT 0600H
140 REM    BY TOM PHILLIPS  11-30-79
150 REM
160    !CHR$(7),\OUT14,0\FOR A=1 TO 700\ NEXT A \  REM TURN OFF DAZZLER
170    !" 1 - INPUT(1)  PLAY(2)  REVERSE(4 & 2)  REVERB(4 & 1)  RETURN(3)"
180    !" 2 - DISPLAY ANY SECTION OF INPUT SAMPLE"
190    !" 3 - AUTOMATIC INCREMENTING SEGMENTAL DISPLAY"
200    INPUT"YOUR CHOICE:",A
210    ON A GOTO 220,320,480
220 REM
230 REM (INPUT - PLAY - REVERSE - REVERB)
240 REM
250    OUT 14,0              \  REM   TURN OFF DAZZLER
260    FILL 1544,112         \  REM   BOTTOM
270    FILL 1543,224         \  REM   TOP
280    FILL 1542,255         \  REM   POINTS PER COLUMN
290    A9=CALL(1539)         \  REM   CALL AUDIO ANALYSIS PROGRAM
300    GOTO 170
310 REM
320 REM     DISPLAY ANY SEGMENT OF SAMPLE
330 REM
340    FILL 3,0 \ A9=CALL(0)  \  REM CLEAR GRAPHICS DISPLAY
350    !"ENTER '0' TO END"
360    INPUT1"BOTTOM:",B \ FILL 1544,B
370    INPUT "    TOP:",T \ FILL 1543,T
380    IF B=0 THEN 170
390    FILL 1542,(T-B)*2      \  REM  POINTS PER COLUMN
400    FILL 14,127
410    FILL 15,1
420    FOR X=0 TO 128 STEP (128/(T-B))  \  REM  OPTIONAL SCREEN DISPLAY OF CALIBRATION
430    FILL 13,X  \  A9=CALL(10)
440    NEXT X
450    A9=CALL(1539)          \  REM   CALL AUDIO ANALYSIS PROGRAM
460    GOTO 320
470 REM
480 REM    AUTOMATIC INCREMENTING SEGMENTAL DISPLAY
490 REM
500    INPUT"INCREMENT:",I
510    FOR A=112 TO 224 STEP I
520     FILL 3,0 \ A9=CALL(0) \  REM  CLEAR GRAPHICS DISPLAY
530     FILL 1544,A           \  REM  BOTTOM
540     FILL 1543,A+I         \  REM  TOP
550     FILL 1542,I*2         \  REM  POINTS PER COLUMN
560     IF A+I>224 THEN 610
570     !"NOW DISPLAYING",A," TO ",A+I,
580     A9=CALL(1692)         \  REM  DISPLAY WAVE
590     !CHR$(13),
600    NEXT A
610    OUT 14,0               \  REM  TURN OFF DAZZLER
620    GOTO 170
READY
```

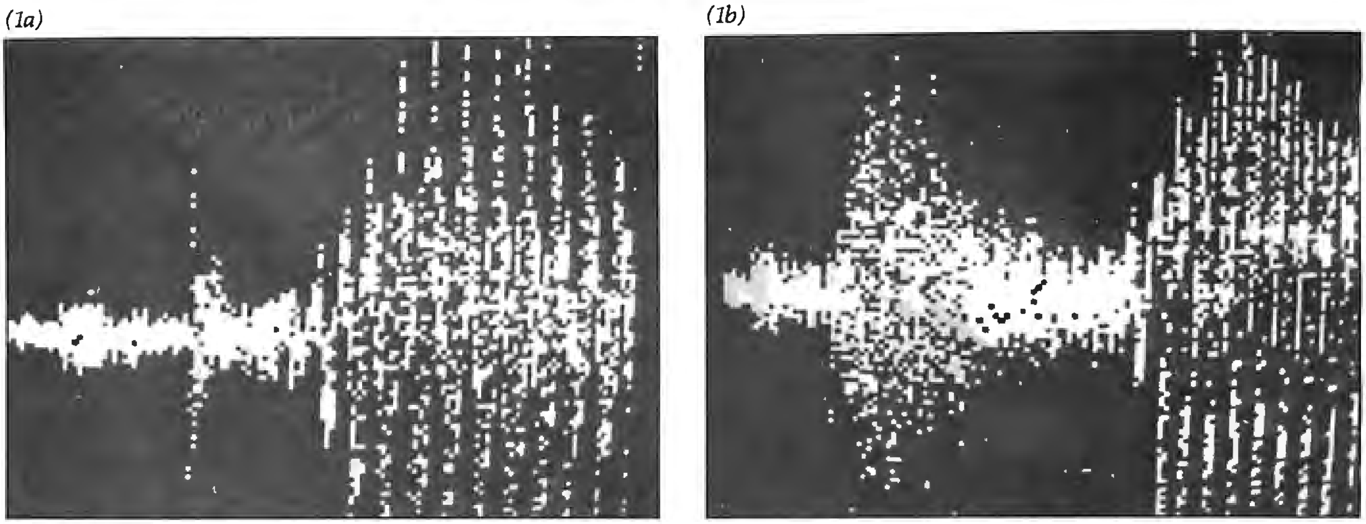

Photo 1: *Video display of sample sounds as captured by the audio-analysis routine. Photos 1a and 1b show the difference between aspirated and unaspirated enunciations of the word "Tom."*

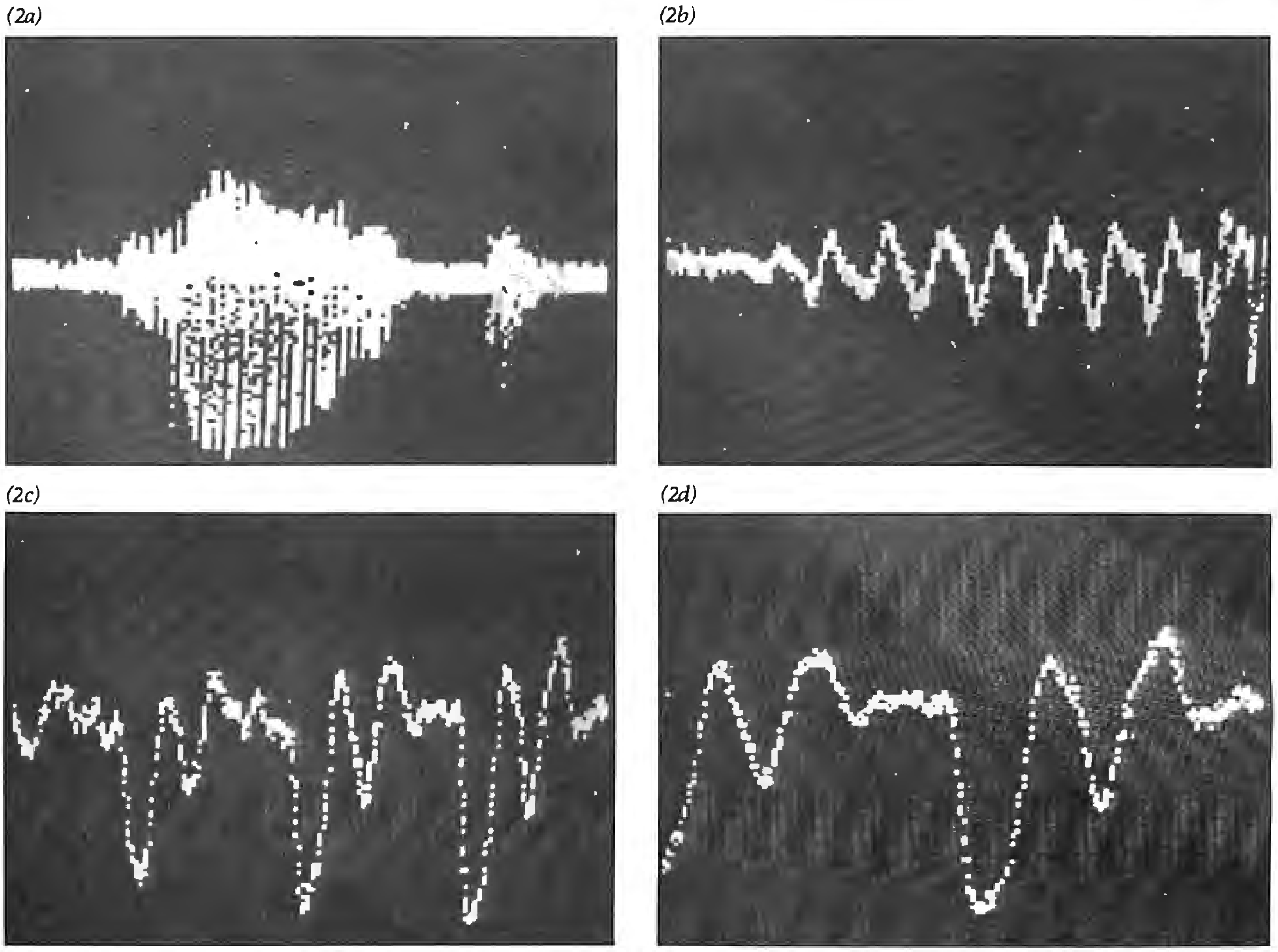

Photo 2: *Progressive expansion of the word "boot." Note that the calibration dots at the top of the display provide a reference for the extent of the expansion.*

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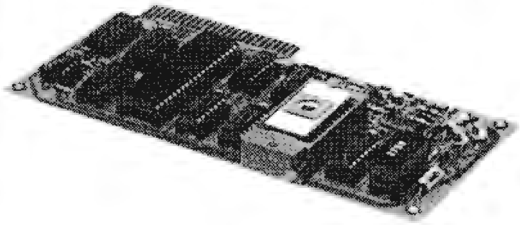

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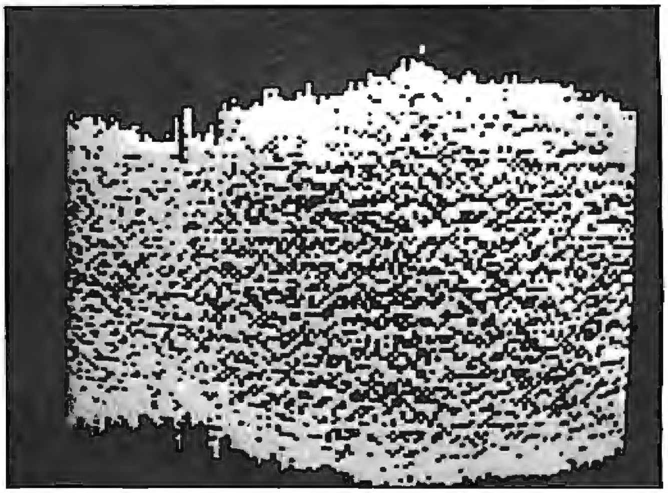

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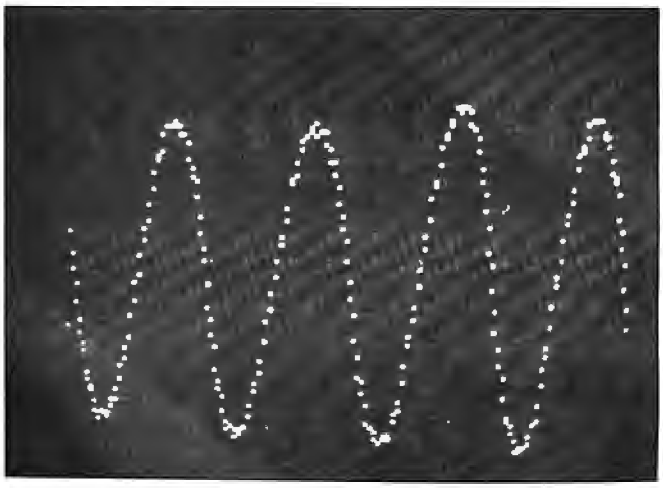

Photo 3: *Progressive expansion of the note middle C as played on a recorder.*

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Memory Expansion for the ZX-80

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On first glance, the Sinclair ZX-80 seems to be an ideal personal computer. It is small (very), cheap ($199), and has video output, cassette storage, plus a high-level language (BASIC). Sinclair is just now offering an expansion of the minuscule 1 K bytes of on-board RAM (programmable memory) to 16 K bytes, for less than $100, and also offers an 8 K-byte floating-point BASIC for $40. The machine appears ideal for running some interesting programs.

Though the availability of the 16 K-byte RAM is a recent development, my desire to expand the ZX-80's capabilities took root many months ago and caused me to take action myself. Being impatient, I decided to design my own 16 K-byte expansion using static, not dynamic, memory devices. (After I completed this expansion project, Sinclair's 8 K Extended BASIC became available. I am now using it with my 16 K-byte ZX-80.)

Selecting Memory

I used a commercially available RAM board for two reasons: first, it is faster, as well as neat and clean, and second, the cost is about the same as a home-fabricated one. Only a few criteria need to be met for adaptability to the ZX-80. Operation at 4 MHz is essential since the Sinclair clocks at 3.25 MHz, and it must be addressable in a contiguous 16 K-byte block starting at location hexadecimal 4000. Incidentally, trying to increase RAM size by more than 16 K is useless because the BASIC software will not access it. The exact reason for this will be shown in the section on checkout of added memory.

Thanks to the Sinclair software, the extra memory is easy to check.

I chose the MEM-16151K board from Jade Computer Products (4901 W. Rosecrans, Hawthorne, CA 90250). It comes in kit form for $169.95 and includes 16 K bytes of programmable memory in 2114-type static RAM ICs (integrated circuits). The board can contain up to 32 K bytes of RAM, which must be installed at either 0-32767 or 32768-65535, using a jumper to select the desired 32 K-byte block. To suit the requirements of the ZX-80, I installed the 16 K of RAM from 16384 to 32767.

Interfacing

Interface circuitry is required to make the board work with the ZX-80. As shown in figure 1, the Sinclair's edge-connector definitions look like plain old garden-variety Z80 CPU (central processing unit) signals, and they are . . . up to a point. The CPU in this small machine performs a lot of functions other than just number crunching; when not actually computing, it is making video, supplying TV sync, and reading the keyboard, to name a few. Consequently, the data bus (D0'-D7') is split internally

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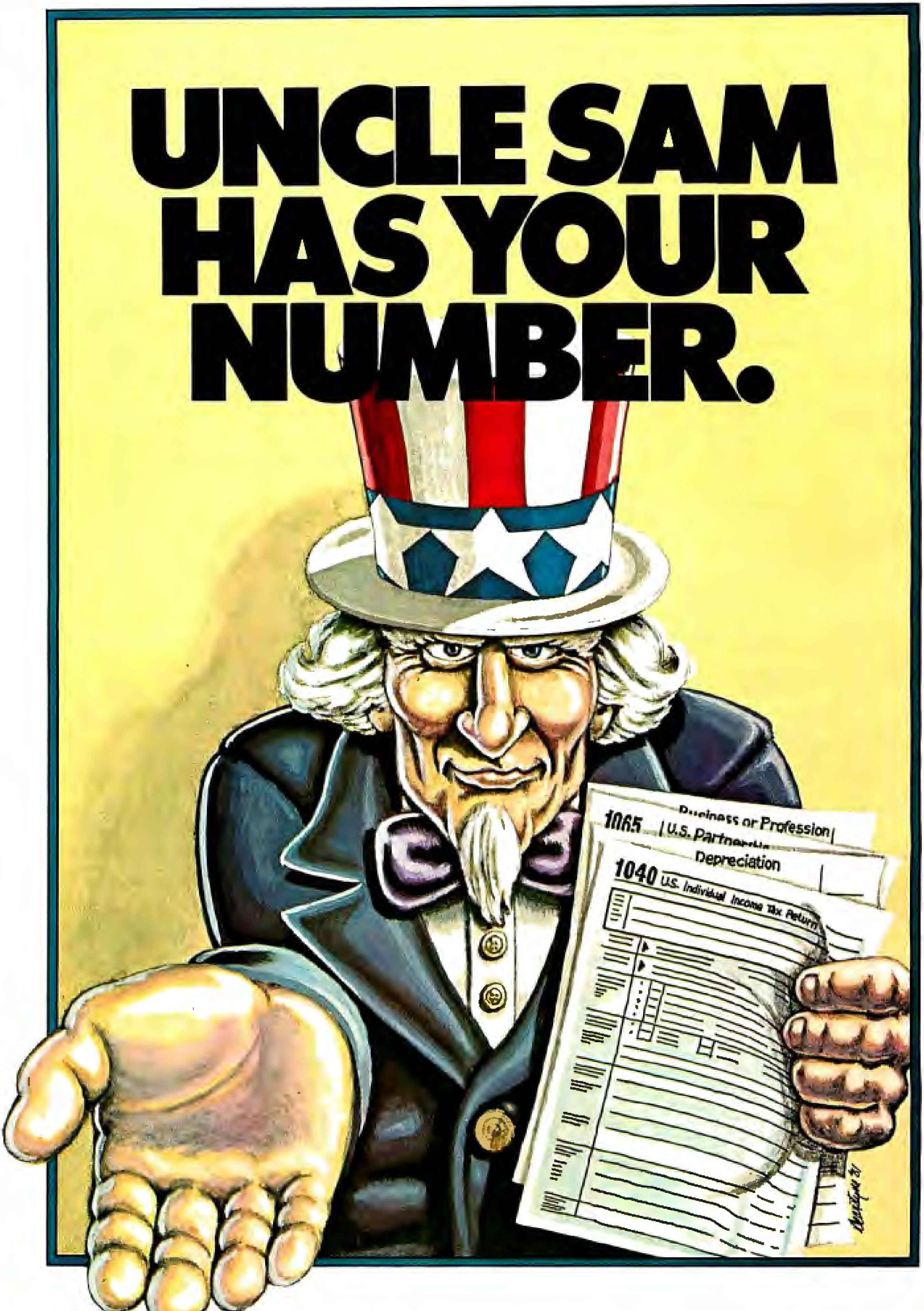
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4 PRINT QUESTIONNAIRE              14 COPY CLIENT FILES
5 ENTER DATA                       15 DELETE CLIENT FILES
6 COMPUTE TAX                      16 EXIT TO STATE TAX TABLE
7 DISPLAY TRIAL RETURN             17 EXIT TO PARTNERSHIP TAX SYSTEM
8 PRINT RETURN                     18 LOAD SALES TAX TABLE
9 DEPRECIATION MODULE              19 UPDATE SYSTEM FILE
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1065			•
A,B,C,D,E,ES,G,R,RP	•	•	
F, SE	•	•	•
K, K-1			•
2106	•	•	
2119	•	•	
2210		•	
2440	•	•	
2441	•	•	
3468		•	•
3903	•	•	
4137	•	•	
4562	•*	•	•
4625	•	•	•
4684	•	•	•
4726	•	•	
4797		•	•
4952			•
4972		•	
5695	•	•	
6251	•	•	
6252	•	•	•
6765		•	
Accelerated Cost Recovery System		•	•
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and isolated from the CPU by 1-kilohm resistors.

Any additions to this data bus must not load it except when actually performing a memory read or write. Loading effects are *very* critical. Since several other signals appear to be reaching their maximum fan-out, I decided to build the interface on a separate card and buffer all of the signals to provide for reliable operation as well as future expansion capability without complications.

The interface circuits are shown in figure 2. Six 74LS367s make up buffers for all address and signal lines as well as a bidirectional data bus. Strictly speaking, the address buffers are probably not necessary since the memory card buffers them again (except, curiously, A10, A11 and A12), but I decided to do it anyway just to be safe. The other gate chips control the direction of the data bus and generate pseudo S-100 signals for the Jade board. PSYNC is generated at memory request time ($\overline{MREQ}$) except

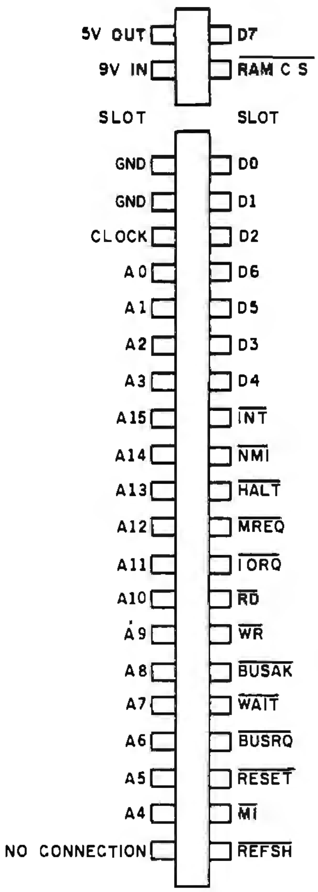

Figure 1: *Signal pinouts on the ZX-80 edge connector as seen from the rear.*

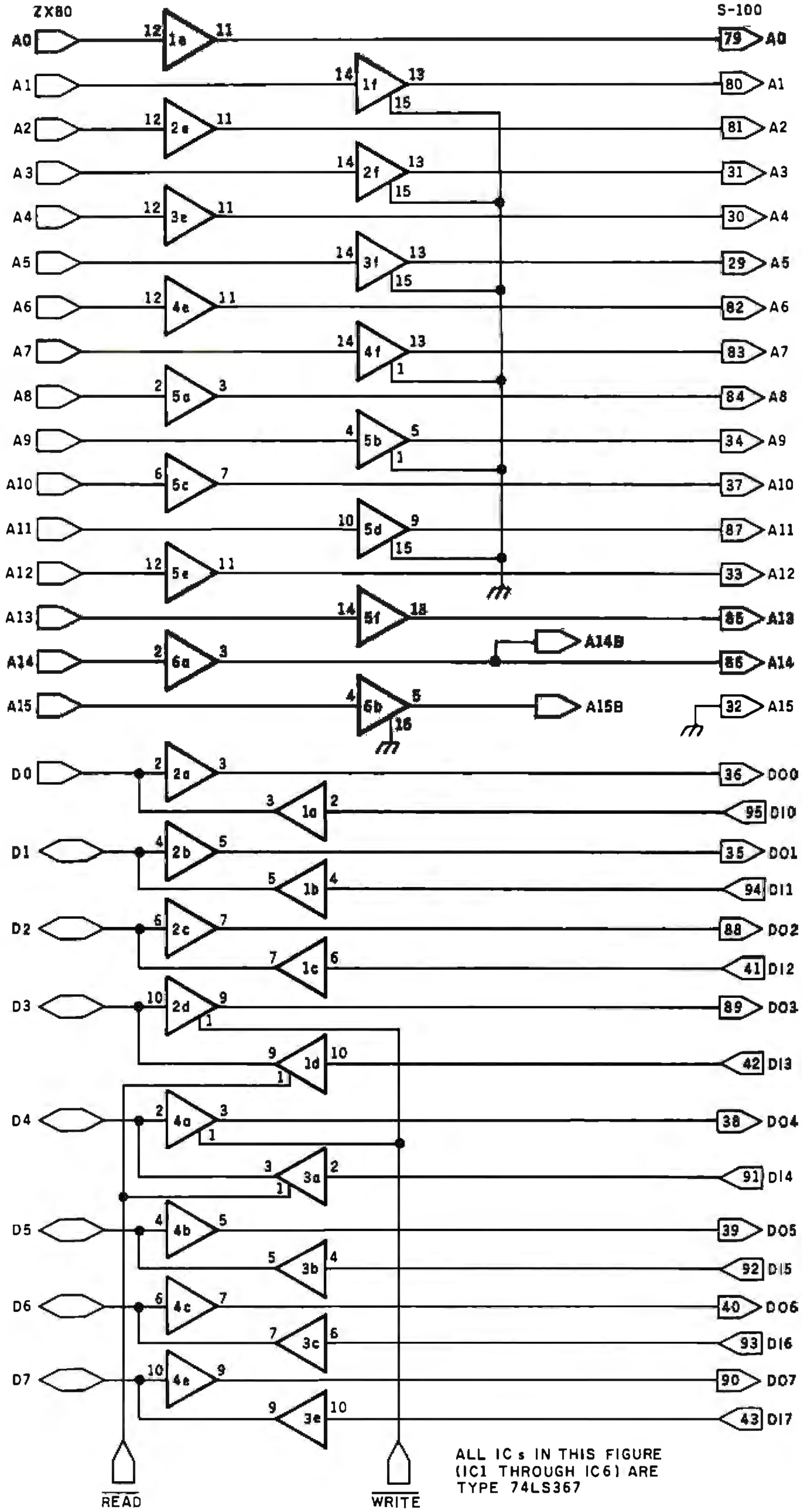

Figure 2: *Schematic diagram of the ZX-80/S-100 interface.* *(Figure 2 continued on page 222.)*

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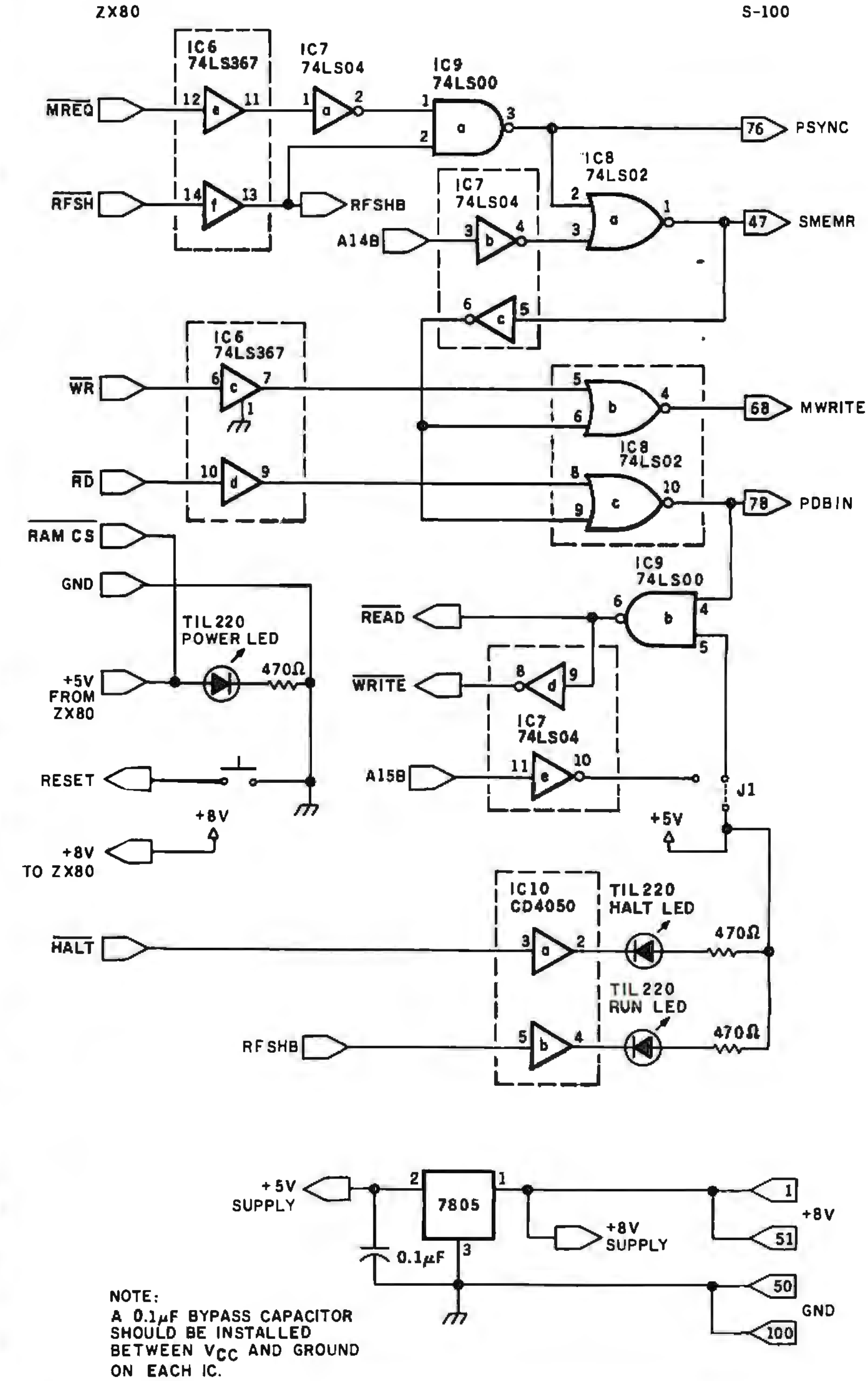
Figure 2 continued:



Number	Type	+5 V	GND
IC1	74LS367	16	8
IC2	74LS367	16	8
IC3	74LS367	16	8
IC4	74LS367	16	8
IC5	74LS367	16	8
IC6	74LS367	16	8
IC7	74LS04	14	7
IC8	74LS02	14	7
IC9	74LS00	14	7
IC10	CD4050	1	8

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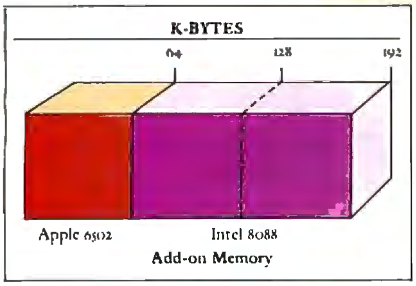

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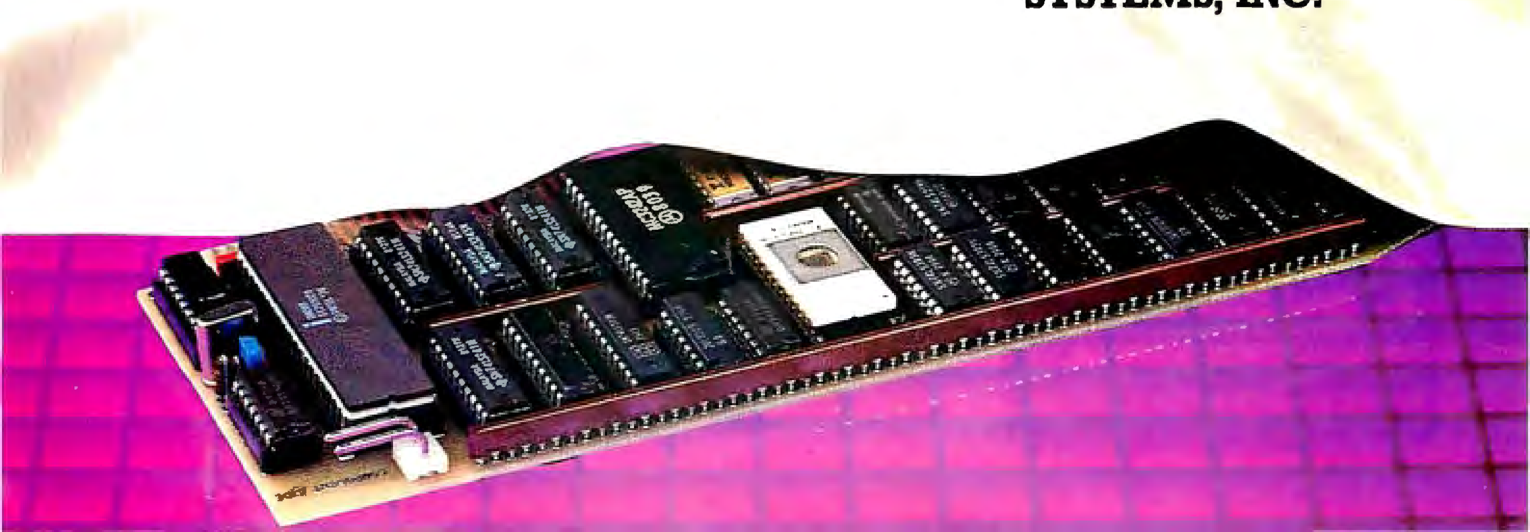

during refresh (RFSH), since the ZX-80 uses the refresh cycle in its video-generating mode. All other S-100 signals are dependent on PSYNC. SMEMR will occur during a memory request when A14 is active, an access in the range hexadecimal 4000 to 7FFF where the ZX-80 expects to find programmable memory. MWRITE and PDBIN are keyed by WR and RD, respectively, plus SMEMR. Refer to the timing diagram in figure 3 for the relationship of these signals.

Data-bus direction is controlled by PDBIN. The bus is normally in the outward direction (away from the CPU) except during a legitimate read operation, when it is switched inward. This is necessary due to the short duration of the ZX-80's WR signal (slightly longer than one clock cycle). Since data on the 2114 RAM chips must be stable before write-enable goes low, and since the write pulse is shortened even more by the memory board's logic, this technique insures proper operation.

Now to A15. As seen in the schematic in figure 2, J1 permanently enables the read/write gate. I had intended to use A15 here to inhibit switching the data bus inward when past the legal limit of hexadecimal 7FFF. However, the ZX-80 uses A15 for certain video-generation tasks, so there are times when A14 and A15 are high at the same time. Consequently, the interface would not work with A15 hooked up. I included this feature as an option in case it is needed for some future modification.

The presence of RFSH is a good sign that the CPU is functioning, and it makes a nice run indicator. HALT shows what is happening in the software; when the program is generating video, the HALT LED (light-emitting diode) will be lit. Tying RAM CS high disables the on-board RAM. There is no decoding of RAM addresses in the ZX-80, and any address

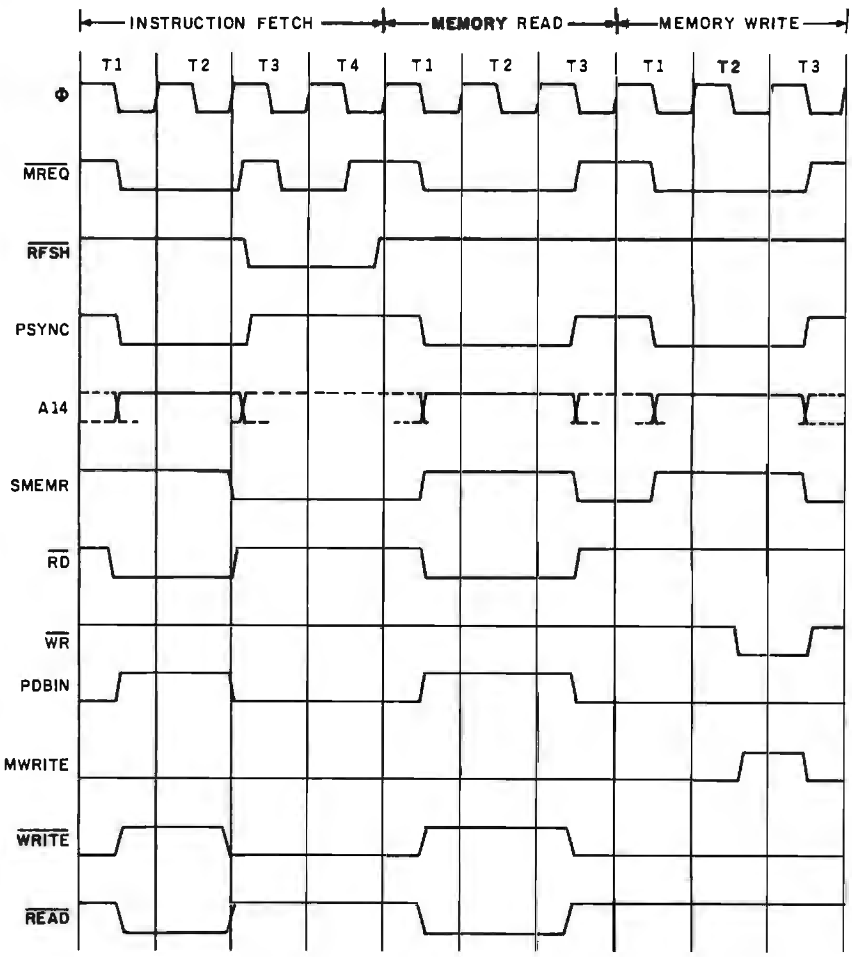

Figure 3: *Timing diagram of ZX-80 signals. At 3.25 MHz, one t-state is 307 ns.*

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within the range of hexadecimal 4000 to 7FFF activates this on-board RAM. If not disabled, some not too interesting things would happen to a program that used more than 1 K. Extending the reset pin to a momentary switch provides a little extra convenience, as none is present on the ZX-80.

Power-Supply Considerations

Providing power to the ZX-80 through the edge connector makes it possible to get rid of the calculator-type wall transformer. The S-100 memory and the ZX-80 both have on-board regulators, so a well-filtered 8- to 9-V supply will do nicely for both. Altogether, the memory card, computer, and interface circuit draw about 2 A. I used a 6.3-V, 4-A transformer with a bridge rectifier and a 12,000-μF filter. This combination works fine. Notice also that the power-on LED is fed from the ZX-80's regulator, providing a good telltale sign to proper operation of the entire system.

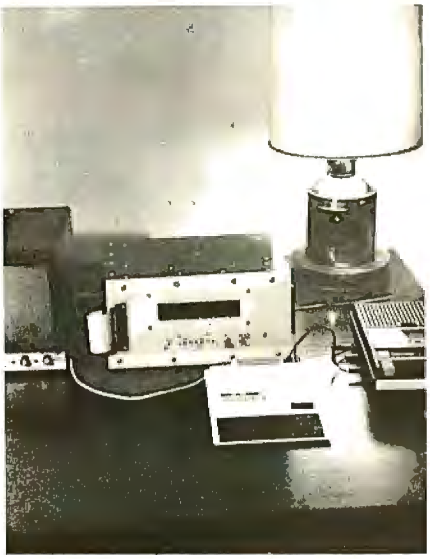

Photo 1: *The complete ZX-80 system. The memory-expansion box dwarfs the ZX-80 unit, making it look rather like a keyboard terminal.*

Memory-Board Modifications

To speed up propagation of signals through the Jade board's CMOS buffer circuitry, the following simple modifications should be made. Gently bend pins 9, 10, 11, 12, 14, and 15 of IC E3 outward to clear the socket with the chip in place. Do likewise for IC E5 pins 11 and 12. Insert a piece of U-shaped, bare #28 wire in the socket of E3 to short pins 9-10, 11-12, and 14-15, and pins 11-12 of E5. Reinsert the chips in their sockets and the job is done. The board remains unaltered and resaleable in case you should decide to move up from the ZX-80.

Construction

Actual construction of the expansion is not too difficult as long as a few simple rules are followed. Most important, keep the leads as short as possible. I used two 25-conductor ribbon cables and was able to keep the distance to the interface less than four inches. The leads between the interface and the S-100 board should also be short. As seen in photo 1, I used an old Augat wire-wrap board for the interface and mounted the memory card directly above it with

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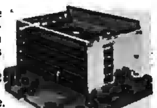

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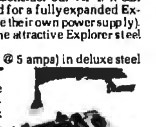

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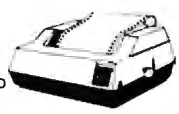

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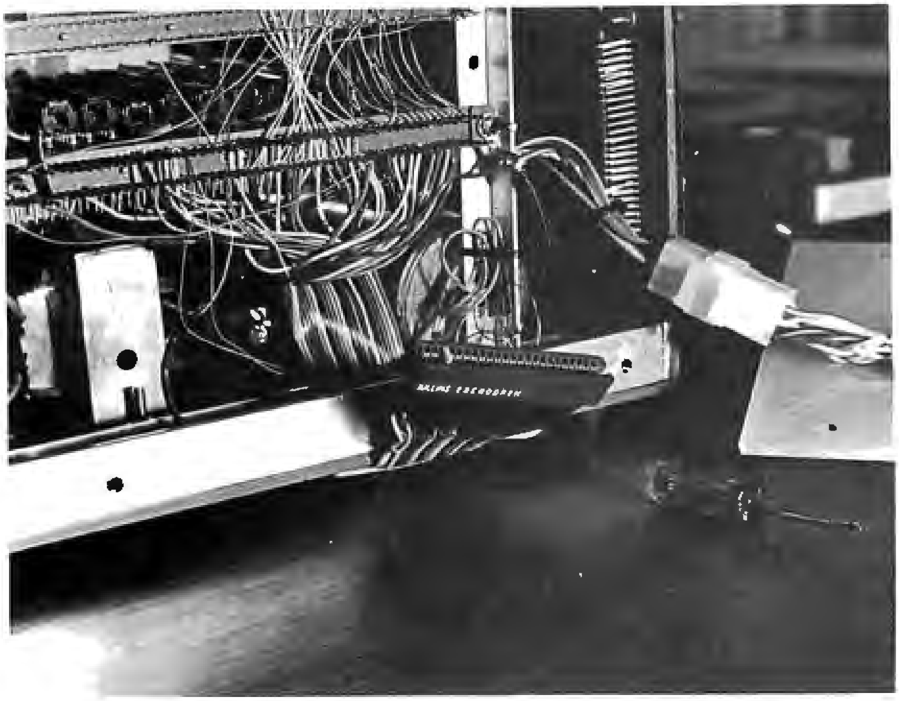

Photo 2: *A custom-made edge connector and ribbon cable tie the ZX-80 to the S-100 memory board. Be sure to keep the cables as short as possible.*

wire-wrap connections of less than an inch between them. The 7-segment LEDs on the front are not yet functional: they will probably evolve into some kind of front panel at a later date.

Acquiring an edge connector for the ZX-80 can be a problem. The Sinclair uses a dual 26-pin arrangement with 0.100-inch spacing. A search through various catalogs turned up no prospects, so I cut down a Jade #CNE-1108011 40-pin unit with a razor saw and made a polarizing blade from a scrap of PC board epoxied in place. Originally, my enclosure was made of sheet PVC plastic held together with aluminum angle and "pop" rivets, but the assembly was electrically unstable. A stray hand brought near the right spot produced erratic operation. I was forced to line the box with well-grounded PC board to get rid of the problem. Starting with a metallic box would be

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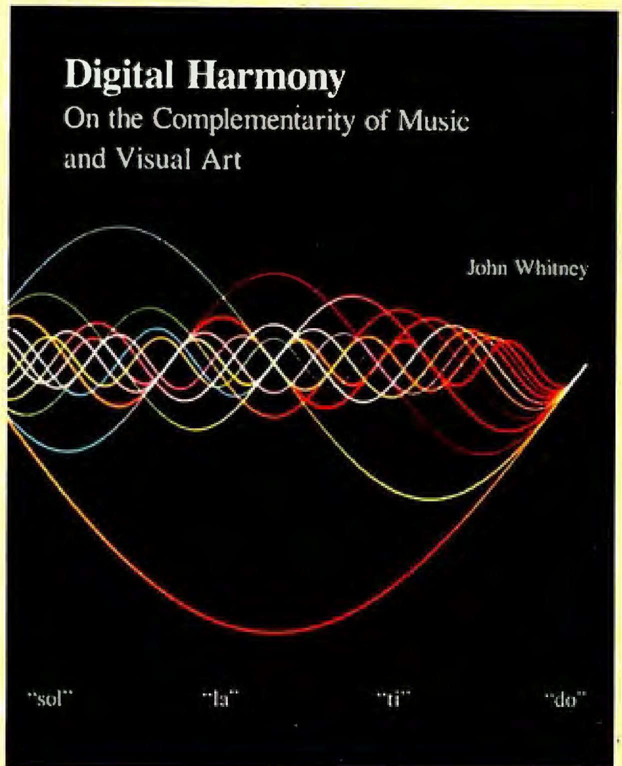

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Listing 1: *A disassembly of the ZX-80's built-in code to locate the highest address in programmable memory. This code is executed whenever the computer is reset.*

Label	Address	Data	Code
RESET	0000	21	LD HL,7FFFH
	0001	FF	
	0002	7F	
	0003	3E	LD A,3FH
	0004	3F	
	0005	C3	JP 0261H(START)
	0006	61	
	0007	02	
START	0261	36	LD (HL),01H
	0262	01	
LOOP1	0263	2B	DEC HL
	0264	BC	CP H
	0265	20	JR NZ,LOOP1
	0266	FA	
LOOP2	0267	23	INC HL
	0268	35	DEC (HL)
	0269	28	JR Z,LOOP2
	026A	FC	
	026B	F9	LD SP,HL

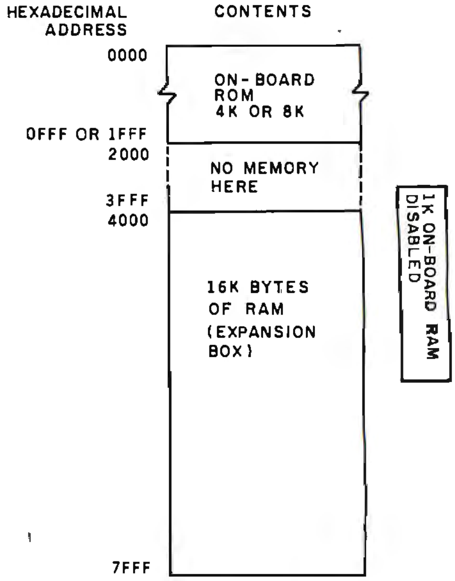

Figure 4: *The ZX-80 memory map with the 16 K-byte memory expansion installed.*

a much better idea. (See photo 2 for a view of the completed system.)

Checkout

Thanks to the Sinclair software, the extra memory is easy to check. Sinclair's ROM (read-only memory) contains the code to do it! The first few locations of the BASIC ROM decoded to assembly language are shown in listing 1. This piece of code is executed every time the ZX-80 is reset (to location zero); it is computing the highest available memory address where it will set the stack pointer. Hexadecimal 01s are written from hexadecimal location 7FFF all the way down to 4000. Then, working forward, each location is decremented by one and the result compared to zero. The first time the comparison is not true, the address is decremented by one and the stack pointer is set to that location. To see what the ZX-80 found after it is up and running, all you have to do is PEEK a few locations in each 1 K block starting at hexadecimal 4000. If the content is zero, the ZX-80 probably found that location. If the content is one, it was written but not read correctly. If neither, it was probably not written. A word of caution: the last few highest locations will contain data actually stored on the stack by the program, and the first 40 will contain variables used by BASIC, as shown in figure 4.

Summary

Building this expansion was rewarding, not only in terms of the increased capabilities of the machine, but also for the learning involved. The Sinclair is remarkable both from the hardware and the software viewpoints. A word of warning, however, to anyone embarking on this or any other project involving the ZX-80: the only technical documentation Sinclair provides is a poorly reproduced schematic diagram with absolutely no functional description. The same holds true for the software. If it's not in the BASIC manual, forget it. The only way I found out anything was by dumping the ROM and disassembling the machine code.■

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I was an owner stuck with the older, single-key RESET. Wanting to modify this, I looked at some of the solutions

Text continued on page 238

Number	Type	+5 V	GND
IC1	7400	14	7

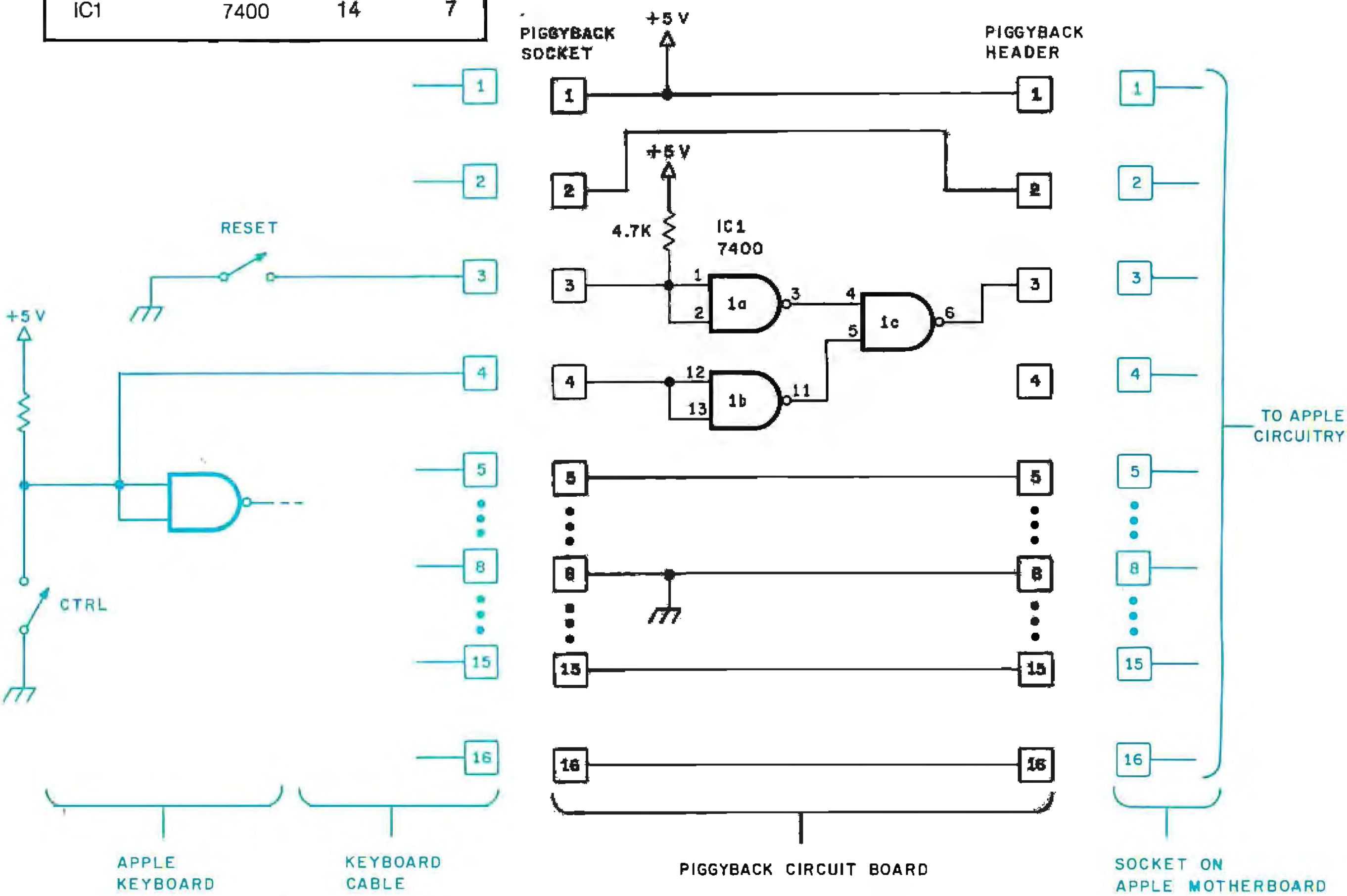

Figure 1: *Schematic diagram of the control-plus-reset modification to the Apple II computer. One connection from the control key to pin 4 of the keyboard circuit board is shown in this diagram and figure 2. The cable from the Apple keyboard plugs into the piggyback board socket, and the piggyback board header (on the other side of the printed-circuit board) plugs into the socket on the main Apple board (the motherboard). Pins not shown have connections similar to pin 5.*

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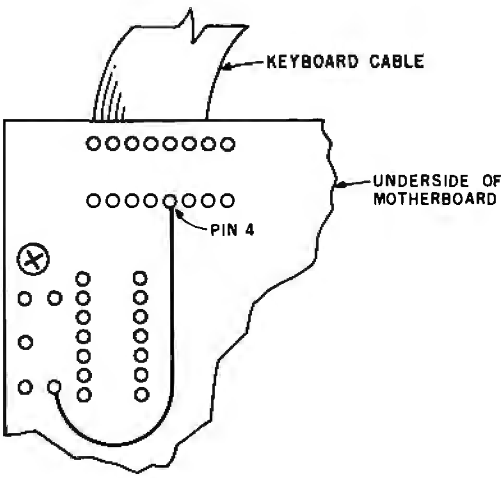

Figure 2: *A jumper must be added to the Apple's motherboard to pass a signal from the CTRL key to the reset-enabling circuitry shown in figure 1.*

(3a)

(3b)

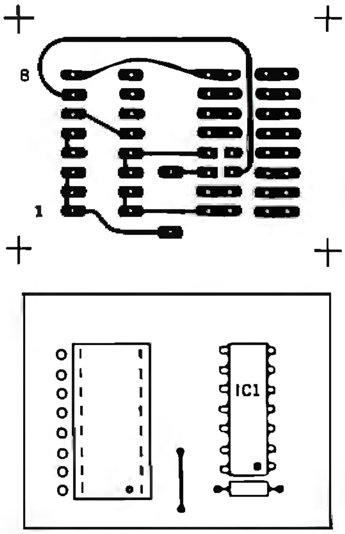

Figure 3: *Printed-circuit artwork and layout for the control-plus-reset conversion. The circuit board has a 16-pin socket on the top side to accept the keyboard cable, and a dual in-line 16-pin header on the bottom (foil) side to plug into the motherboard's keyboard socket. As seen from the top (figure 3b), the holes for the socket are located to the right of the holes for the header pins. From the foil side of the printed-circuit board (figure 3a), the situation is reversed—the left holes (on the elongated pads on the right half of the board) are from the socket, and the holes on the right go to the header pins. Also, note the placement of the dot in figure 3b, which marks pin 1 of both IC1 and the 16-pin socket.*

currently available. I found everything from simple cardboard shields, which slip around the RESET key, to switches mounted on the side or rear of the Apple's case that are wired in series with the key. Prices ranged from $0.15 to $20 or more.

After careful consideration, I decided I wanted a modification that was invisible from the outside of the case and required both hands to operate. The best way to accomplish this is to duplicate Apple's efforts and use the CTRL key.

Figure 1 is the schematic diagram of my modification with the existing Apple hardware shown in color. Although there are several ways to incorporate the new components, I chose to develop a printed-circuit board that is mounted "piggyback" on the motherboard socket for the keyboard cable. This also required adding a jumper wire to the bottom of the keyboard as shown in figure 2. The foil and component layouts of the board are shown in figures 3a and 3b.■

An 8080-Based Remote Appliance Controller

David C. Staehlin
5430 Candleglow NE
Albuquerque, NM 87111

Many of us are familiar with BSR's console command units and receiving modules that control lights and appliances by transmitting signals over ordinary 115-volt AC wiring. In the January 1980 BYTE ("Computerize a Home," page 28), Steve Ciarcia discussed the control signals required to communicate with the BSR console command unit and presented an interface circuit for controlling the ultrasonic unit.

Being a gadget nut, I had already purchased a console command unit that did not have ultrasonic capabilities. My decision to discard a perfectly good console and purchase one with ultrasonic capabilities met with stiff opposition from my wife. So I was faced with converting my present unit if I wanted to experiment ("play," as my wife puts it) with computer control of remote appliances.

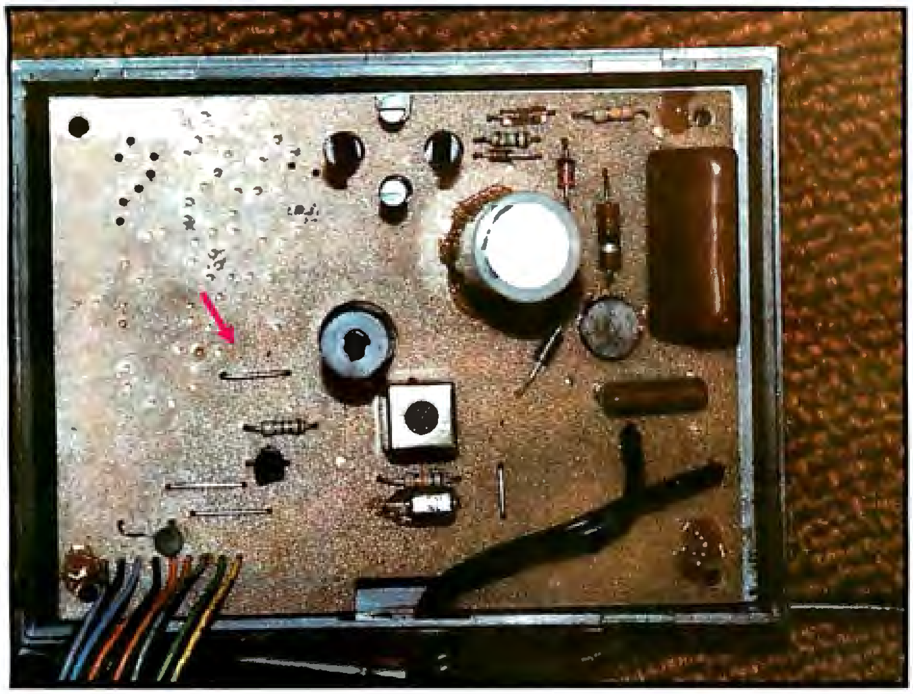

Photo 1: *The standard BSR command console. This unit is exactly the same as the ultrasonic version but does not have the 40-kHz transducer and amplifier. The arrow points to a jumper at the input of the custom LSI controller integrated circuit developed by BSR. This is the input that can accept serial information from a computer. (Photo courtesy Dan Thompson)*

BSR System Operation

Even though the standard BSR command unit cannot be used with the hand-held ultrasonic controller, serial communications with the unit remain possible. As a preface, I'll briefly review operation of the ultrasonic data link between the hand-held transmitter and the console receiver.

When a command button is pushed on the hand-held controller, a coded series of 40-kHz bursts is transmitted to a receiver section within the console unit. These bursts are amplified and applied to pin 7 of the custom LSI (large-scale integration) integrated circuit (IC) within the console unit, where they are decoded and executed as the desired command. To eliminate the added expense of producing a different custom IC, BSR uses the same device in both the standard and ultrasonic controller models. They differ only in that the 40-kHz transducer and amplifier sections are omitted in the standard model. Since it is always good practice and usually necessary to have all pins of an integrated circuit connected to some-

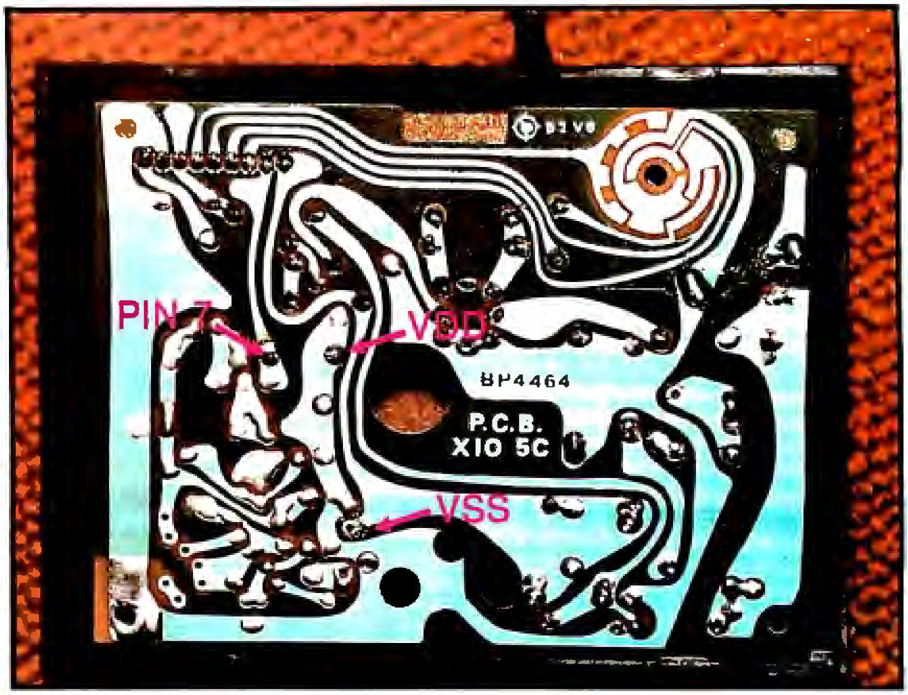

Photo 2: *Foil side of the BSR controller. Arrows indicate mounting holes available for use by the experimenter. Be careful not to bridge adjacent foil traces when making connections to the board.*

thing, BSR connected pin 7 to ground with a wire jumper (see photo 1). If this jumper is removed, you should be able to "fool" the command unit into accepting your commands when the proper information is injected into it.

Inexpensive Interface Circuit

As stated previously, pin 7, the serial-data-input pin, communicates with the outside world through a properly encoded series of 40-kHz tone bursts. Figure 1 details a circuit that can generate these 40-kHz waveforms. If you have only a serial port on your computer and can't afford a parallel port, the circuit shown in figure 1 will work with either RS-232C or standard parallel communication levels. All that is needed for RS-232 communications is a device-control or status port that can be toggled between 0 and 1.

The circuit uses an integrated circuit to form the communications link with the computer. IC1, a CD 4001 CMOS (complementary metal-oxide

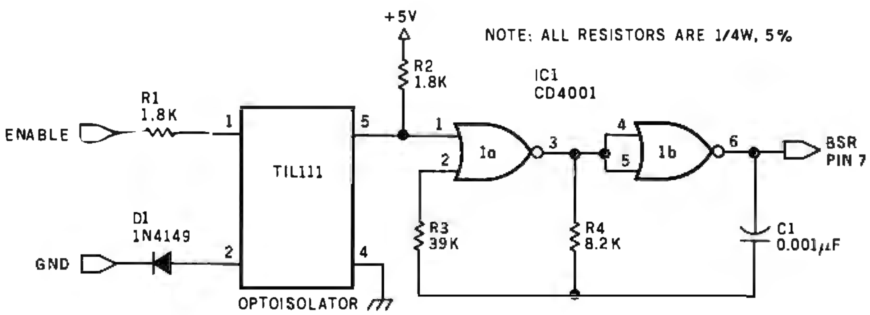

Figure 1: *Schematic diagram of the serial interface circuit. The ENABLE signal may be originated by a computer's RS-232 port or from a parallel port driven by the appropriate software. The optoisolator is used to isolate the controller from the computer (the controller's ground "floats" at power-line voltage). The oscillator made from IC1 is designed to produce a 40-kHz "burst" when the ENABLE signal is received, thus mimicking the signals found in a BSR controller with ultrasonic capability.*

Number	Type	+5V	GND
IC1	CD 4001	14	7

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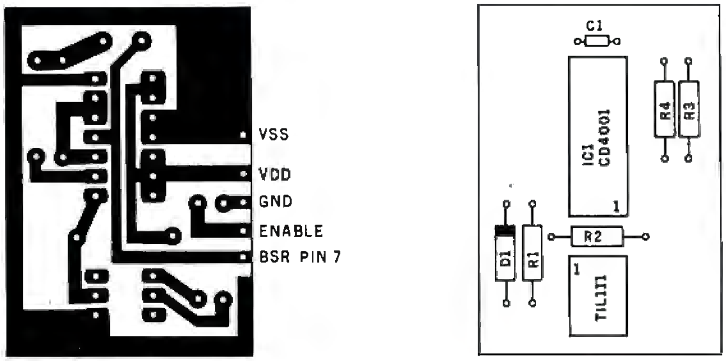

Figure 2: *Interface etching, drilling, and component layout. A printed-circuit card of the proper size (the figure is actual size) will fit easily in the controller's case, although other construction techniques may work as well. Note the orientation of pin 1 on each of the integrated circuits.*

semiconductor) quad, two-input NOR gate is used to create the 40-kHz output injected into pin 7 of the BSR custom IC. The other IC is an optoisolator that provides electrical isolation between the computer and the BSR unit's ground, which is floating at line voltage. Do *not* try this circuit without the optoisolator; that would be a very expensive mistake.

Operating power for the circuit comes directly from the BSR's internal power supply. BSR has conveniently provided holes in the console circuit board for power and pin 7 connections. Photo 2 shows the foil side of the command unit's printed circuit board, where to pick up the V_{SS} and V_{DD} supplies required for the interface circuit, and where to tie into pin 7 of the custom IC.

The construction technique or component layout for the circuit is not critical. However, to keep the finished circuit small enough to fit inside the existing housing, I recommend using a printed-circuit board. Figure 2 illustrates a full-size etching and drilling layout for this purpose. Photo 3 shows the completed board tucked neatly into the corner of the BSR controller housing. Be sure to cover the foil side of the finished circuit board with an insulative material to prevent the foil patterns from shorting to any jumpers installed on the BSR circuit board.

This circuit is not limited to controllers lacking ultrasonic capabilities. Ultrasonic command units may be used by disconnecting the output of the 40-kHz transducer amplifier section from pin 7 of the custom IC and hooking up this interface circuit in the same manner as the standard control console. With a little work, I'm sure a modification can be made to the interface circuit presented to allow operation of both the interface and the 40-kHz transducer and amplifier. Since I was too frugal to buy an ultrasonic model, I can't say for sure.

Talking to the Controller

Now that we have a method of injecting 40-kHz pulses into the control unit's custom IC, it becomes neces-

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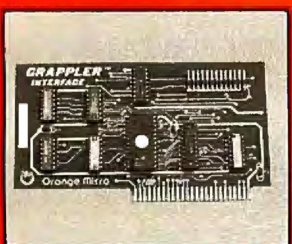

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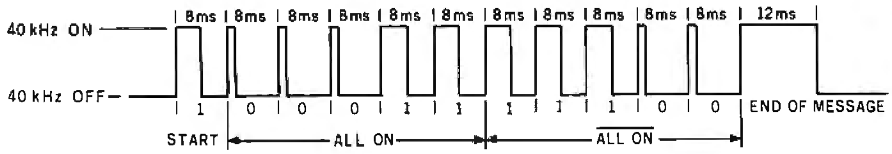

Figure 3: *Data format for the ALL ON command. Note that the 5 command bits are complemented and repeated before the end-of-message pulse. Once a command or unit number has been sent, allow a 24-ms interval before the next transmission.*

D0	D1	D2	D3	D4	FUNCTION
0	0	0	1	1	ALL ON
0	0	0	0	1	ALL OFF
0	0	1	0	1	ON
0	0	1	1	1	OFF
0	1	0	1	1	BRIGHT
0	1	0	0	1	DIM
0	1	1	0	0	CHANNEL 1
1	1	1	0	0	CHANNEL 2
0	0	1	0	0	CHANNEL 3
1	0	1	0	0	CHANNEL 4
0	0	0	1	0	CHANNEL 5
1	0	0	1	0	CHANNEL 6
0	1	0	1	0	CHANNEL 7
1	1	0	1	0	CHANNEL 8
0	1	1	1	0	CHANNEL 9
1	1	1	1	0	CHANNEL 10
0	0	1	1	0	CHANNEL 11
1	0	1	1	0	CHANNEL 12
0	0	0	0	0	CHANNEL 13
1	0	0	0	0	CHANNEL 14
0	1	0	0	0	CHANNEL 15
1	1	0	0	0	CHANNEL 16

Table 1: *BSR command codes. These are the 5-bit codes sent to the BSR controller by the computer.*

sary to switch this in a manner the controller can understand. Controller communication messages are made up of three main components: logic zeros, logic ones, and the end-of-message signal.

A logic zero is sent to the controller by injecting the 40-kHz bust into pin 7 of the control unit's IC for 1.2 milliseconds (ms) followed by the absence of the 40-kHz signal for 6.8 ms, for a total time of 8 ms. Similarly, a logic one is sent by enabling the 40-kHz burst for 4 ms followed by a 4-ms off-time, again yielding a total time of 8 ms. The end-of-message signal is a 16-ms message composed of a 12-ms burst of 40 kHz followed by a 4-ms off-time.

Table 1 lists the codes required for any given controller function and the channel-number codes required to alert any given receiver module in the system. A complete command is sent to the control module as a series of 12 bits. First, a logic one is sent to alert the controller that a message is forthcoming. Next, the 5-bit channel number or function code as given in table 1 is sent, followed by the logical inversion of the same five-channel number or function code bits. Lastly, the end-of-message signal is sent to alert the controller the message has been completed. Figure 3 shows how the ALL ON command would be sent to the controller. Keep in mind one important item when using this circuit: a waiting period of at least 24 ms must elapse between command messages, or the controller will only respond to the first command sent.

Putting It All Together

Home Control Package (HCP), a complete manual control program for this interface system, is given in listing 1 (which begins on page 250), along with a sample run listing to show the various features implemented. This program is written in 8080 assembly language for operation under the Heath Disk Operating System (HDOS) on a Heath H-8 computer. It uses Heath system calls (SCALLS) for disk functions and various routines stored in the H-8's read-only memory. For users of other systems, table 2 gives the names and functions of these routines.

This program is designed to be extremely modular to allow the inclusion of various subroutines in a clock-driven control routine. Therefore, little program-memory optimization

FUNCTION NAME	FUNCTION
1. $TYPEX	Outputs the text in the define byte (DB) statement immediately following the function name. The last bit of the string has the parity bit set to signal the end of the string.
2. .SCIN	Inputs a single byte from the console terminal. If the carry flag is set after the function is called, no data was available so a loop for data input is executed.
3. .OPENR	The HDOS open file for read function. The DE register holds a default file device name and extension, HL contains the file name, and the accumulator holds the channel number of the file. A carry flag that is set upon routine exit indicates an error of some type.
4. .READ	Reads data from an open file. The A register contains the number of the channel to be read and the BC register contains the number of bytes to read. The number in BC must be a full sector multiple (i.e., an integer multiple of 256). Again, a set carry flag at exit indicates a read error.
5. .CLOSE	Closes the file on the channel indicated by the accumulator.
6. .EXIT	Exits the program and returns to the HDOS system command level.
7. .SCOUT	Outputs a single character to the console terminal. Carry set indicates that the console is not ready to accept the character.
8. $HLIHL	Loads the HL register indirectly through the HL register. That is, the data at the address in HL and at HL + are loaded into the HL register pair.
9. $TJMP	The number in the A register is used to select the proper routine to execute from the list of define word (DW) statements following the command. For example, if the A register contains the number 2 then the address indicated by the third DW statement is where execution continues.
10. .CLRCO	Clears the console terminal's internal buffer when executed.

Table 2: *HDOS (Heath Disk Operating System) commands and routines available in read-only memory. These may be used in providing disk I/O and to interface with the operating system. The same functions may be simulated under CP/M.*

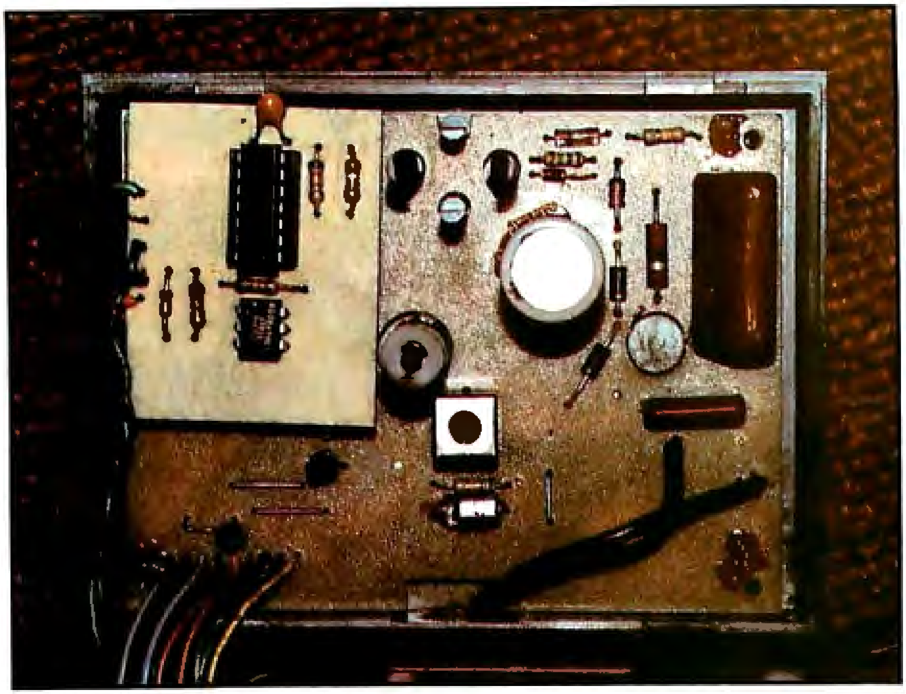

Photo 3: *The BSR controller with the serial computer interface installed. Cover the foil side of the interface board to prevent shorts to jumpers on the controller.*

has been done. Five major sections of routines are used to make up the complete program package. An explanation of each major routine's function follows.

Title: The program signs on by executing the routine TITLE, which clears the computer's terminal screen and prints the name of the program. Users of terminals other than the Heath H-19 will need to examine the control codes used and alter them accordingly. Users of terminals without any sort of graphics capability will probably want to skip this routine entirely, since it will not affect program operation.

Readit: READIT reads a data file named UNITDEF.DAT and initializes the BSR remote-control units according to the data it contains. UNITDEF.DAT also contains all of the remote-control unit name descriptions for use in various menus used later in the program. The READIT routine's internal documentation gives the information necessary to set up this file. A sample file is provided in listing 2 (see page 292). Note that all 166 unit locations must be defined in the file even though only those units which have been enabled will be available for control through HCP's menu routines.

Status: Remote-unit status is displayed by this routine. Information listed includes the channel number, the channel name as defined in UNITDEF.DAT, the brightness level of the channel, and the unit's on-off status.

Menu: Program functions are displayed and selected by this routine. All commands the BSR console command unit can execute (in addition to returning to the status display and exiting from the program) are available from this master menu.

Utility Routines: These routines include the timing loops necessary to send commands to the BSR console command unit. Since the H-8 computer uses about 20 percent of its processing time to update its front-panel display, adjustment of these timing loops will be necessary for other systems. I recommend using an oscilloscope to monitor the duration of the signals sent to the BSR command unit; however, if an oscilloscope is not available, the timing constants in the routines that send the signals to the BSR can be changed through trial and error. If the trial-and-error approach is chosen, I recommend altering all of the timing constants proportionately to preserve the proper timing relationships. Also in this group are routines that update and store the present status of each remote unit and form the command format required by the BSR console command unit.

Summary

So there it is, a complete interface and program package for those of you who want to experiment with home control but don't want to spend the time or money to implement previous BSR interface ideas. Components for the required hardware are inexpensive and readily available from a number of sources. By using a few spare parts lying around the shop, you should be able to build the interface for well under $10.

Even though the program presented is written in 8080 assembly language, a similar routine could be implemented easily in BASIC once the proper timing loops have been set up. The assembly-language program presented here was written as such to allow the inclusion of various routines in a real-time control system designed for background operation in the H-8 computer system.

The ability to regulate remote devices inexpensively is an important part of any home-control system. The next step in my own system will be to tie in this system with the temperature-sensing circuits presented by Tom Hall in the February 1981 BYTE ("A Heating and Cooling Management System," page 326) to allow efficient control of my heating and cooling system. Someday I'll have a computer-controlled sprinkler system tied in with a moisture detector to prevent watering the lawn when it's raining. (How many times have you seen home owners' sprinklers spraying away during a downpour?) Maybe I should link the system to small servo motors in my house's heating and cooling system to regulate room air flow. Then there's always the electric lawn mower.■

Listings 1 and 2 follow on pages 250 through 292.

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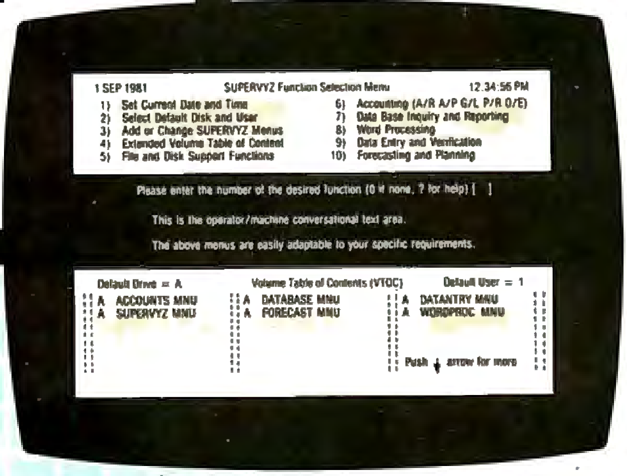

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Listing 1: *HCP (Home Control Package) for the BSR interface. This program is written in 8080 assembly language for Heath's HDOS. A sample run is shown at the end of the listing.*

```
         ORG     USERFWA         *BEGIN PROGRAM HERE IN MEMORY
PORT     EQU     374Q            *OUTPUT PORT ASSIGNMENT

BEGIN    CALL    TITLE           *PRINT THE TITLE
         CALL    READIT          *READ DATA FILE AND INITIALIZE
LOOP     CALL    STATUS          *PRINT UNIT STATUS
         CALL    $TYPTX
         DB      0AH,'Hit Return For The Command Menu',' '+080H
HOLDIT   SCALL   .SCIN              *GET INPUT
         JC      HOLDIT             *LOOP UNTIL READY
         CPI     0AH                *RETURN?
         JNZ     HOLDIT             *WAIT IF NOT
         CALL    MENU               *DISPLAY THE MENU
         JMP     LOOP               *AND DO AGAIN


*READ UNIT DEFINITIONS AND STATUS

 ***********
 * READ IN UNIT DEFINITION FILE
 *      FORMAT           COLUMNS          ITEM
 *                          1          STATUS BIT, 1=ON, 2=OFF
 *                          2          LEVEL BIT, 9=BRIGHT, 0=DIM
 *                         3-4         UNIT NUMBER, 1 THRU 16
 *                         5-          UNIT DESCRIPTION, ASCII STRING
 *                        LAST         CARRIAGE RETURN
 *
 *      SEE UNITDEF.DAT FILE FOR DATA FILE EXAMPLE (LISTING 2.)
 *

READIT   LXI     D,DEFLT         *LOAD DEFAULT BLOCK
         LXI     H,UNITNAM       *LOAD FILE NAME
         MVI     A,2             *CHANNEL NUMBER
         SCALL   .OPENR          *OPEN FOR READ
         JC      READERR         *ERROR ON CARRY
         MVI     A,2             *CHANNEL NUMBER
         LXI     B,1280          *ATTEMPT TO READ 5 SECTORS
         LXI     D,UNITBUF       *PUT IT HERE
         SCALL   .READ           *READ IT
         JNC     CLOSIT          *CLOSE FILE
         CPI     01H             *IS IT END OF FILE
         JNZ     READERR         *FATAL ERROR IF NOT

CLOSIT   MVI     A,2             *CHANNEL NUMBER
         SCALL   .CLOSE          *CLOSE THE FILE
         JC      READERR         *ERROR ON CARRY

 ***********
 * BREAK DOWN INPUT INTO SEPARATE LINES LOCATED BY UNITLOC

         LXI     B,0FH           *NUMBER OF UNITS
         LXI     D,UNITBUF       *BEGINNING LOCATION
         LXI     H,UNITLOC       *ADDRESS LOCATION
         MOV     M,E             *STORE FIRST LOCATION
```

Listing 1 continued on page 252

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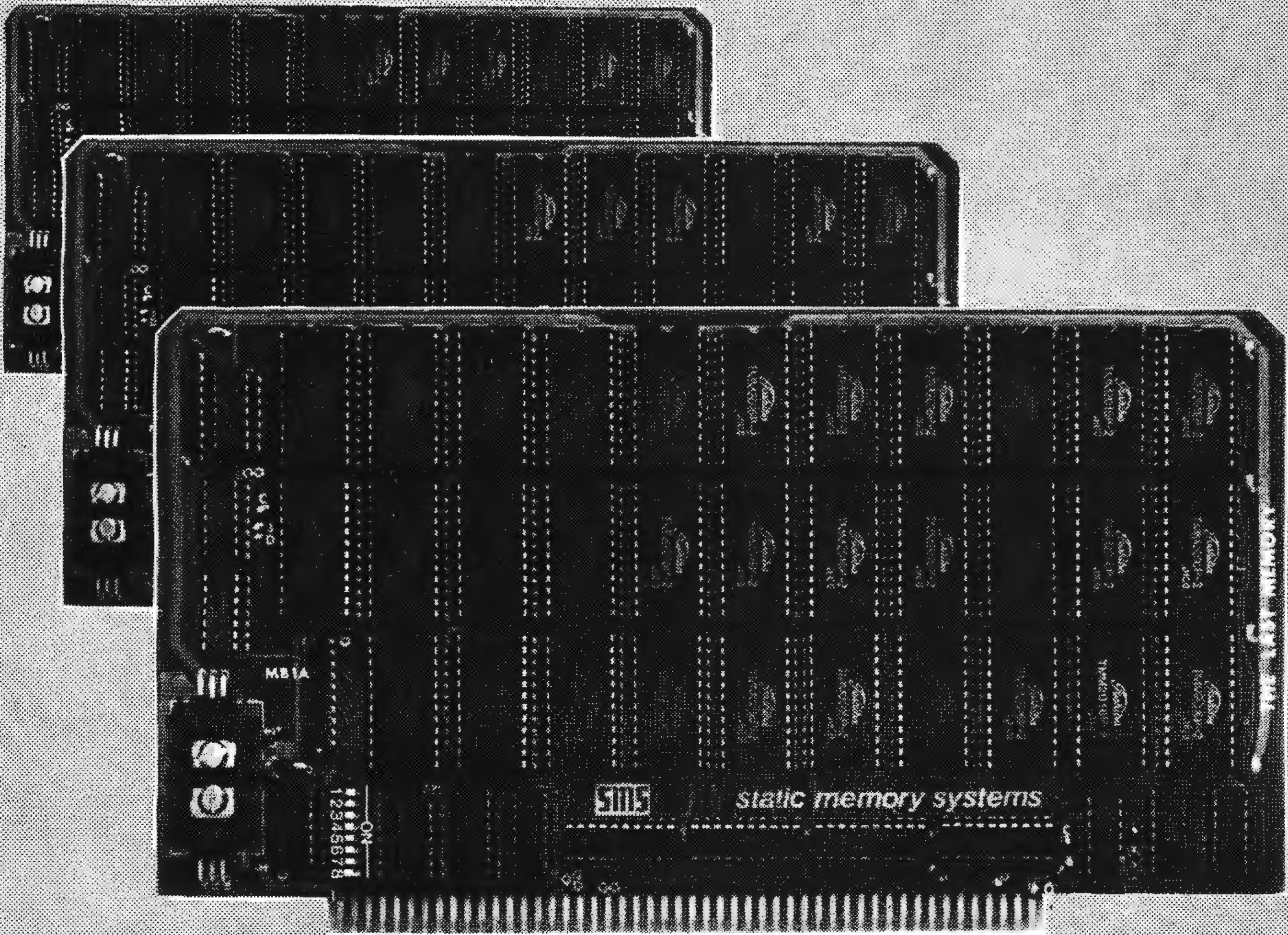

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Listing 1 continued:

```
        INX     H               *INCREMENT MEMORY
        MOV     M,D             *STORE LSB OF ADDRESS
SORTLP  INX     H               *INCREMENT POINTER (STORAGE)
INLOP   INX     D               *INCREMENT BUFFER POINTER
        LDAX    D               *LOAD A FROM ADDRESS IN DE
        CPI     0AH             *CARRIAGE RETURN?
        JNZ     INLOP           *CONTINUE IF NOT
        INX     D               *NEXT CHAR IS THE ONE WE WANT
        MOV     M,E             *STORE MSB
        INX     H               *INCREMENT POINTER
        MOV     M,D             *STORE LSB
        DCR     C               *COUNT ONE UNIT DONE
        JNZ     SORTLP          *DO NEXT ONE
        LXI     D,010H          *NUMBER OF UNITS
INIT    PUSH    D               *SAVE D
        MOV     A,E             *GET NUMBER OF UNIT
        SBI     1               *ADJUST FOR OFFSET
        PUSH    PSW             *SAVE IT
        CALL    GETSTAT         *GET STATUS BYTE
        CPI     '0'             *OFF?
        JNZ     NEXT1           *JUMP IF NOT
        POP     PSW             *ELSE RESTORE CHANNEL #
        PUSH    PSW             *SAVE IT AGAIN
        CALL    OFFONE          *TURN IT OFF
        JMP     SKINIT          *AND LOOP
NEXT1   POP     PSW             *RESTORE CHANNEL
        PUSH    PSW             *SAVE IT
        CALL    ONONE           *TURN IT ON
        POP     PSW             *RESTORE CHANNEL
        PUSH    PSW             *SAVE IT
        CALL    GETLVL          *GET LEVEL BYTE
        CPI     '9'             *IS IT NINE?
        JZ      SKINIT          *LOOP IF SO
        MOV     E,A             *ELSE SAVE THE LEVEL
        MVI     D,0             *CLEAR D
        MVI     M,'9'           *STORE 9 AS PRESENT LEVEL
        POP     PSW             *RESTORE CHANNEL NUMBER
        PUSH    PSW             *SAVE IT AGAIN
        CALL    INTEN           *ADJUST INTENSITY
SKINIT  CALL    LONGWT          *WAIT BETWEEN COMMANDS
        POP     PSW             *CLEAR STACK
        POP     D               *RESTORE COUNT
        DCR     E               *COUNT DOWN
        JNZ     INIT            *DO ANOTHER
        RET                     *AND RETURN WHEN DONE

LONGWT  LXI     D,28H           *LONG WAIT ROUTINE
LONGLP  PUSH    D               *SAVE COUNTER
        CALL    WAIT            *WAIT
        POP     D               *RESTORE COUNTER
        DCR     E               *DECREMENT COUNT
        JNZ     LONGLP          *LOOP UNTIL DONE
        RET

READERR CALL    $TYPTX
        DB      0AH,0AH,'DATA FILE MISSING - PROGRAM ABORTED'
        DB      07H,0AH+080H
        SCALL    EXIT
```

Listing 1 continued on page 254

Circle 353 on inquiry card.

Listing 1 continued:

```
*TYPE STATUS OF HOUSEHOLD UNITS

  ***********
  * DISPLAY THE UNIT STATUS
  *         ENTRY    NONE
  *         USES     ALL

  STATUS    LXI      B,010H              *NUMBER OF UNITS
            LXI      D,0                 *UNIT INDEX OFFSET
            CALL     $TYPTX              *PRINT HEADING
            DB       01BH,045H,0AH,09H,09H,09H,'     '
            DB       01BH,'pREMOTE UNIT STATUS',01BH,'q',0AH,0AH
            DB       'UNIT',09H,09H,09H,'UNIT NAME',09H,09H,09H
            DB       'LEVEL  STATUS',0AH
            DB       '_________________________________________'
            DB       ':_________________________________________'
            DB       0AH+080H

  STATLP    PUSH     B                   *SAVE BC
            PUSH     D                   *SAVE DE
            MOV      A,E                 *FETCH CHANNEL NUMBER
            PUSH     PSW                 *SAVE CHANNEL NUMBER
            CALL     GETCHAN             *ADDRESS OF ASCII STRING
            MOV      A,M                 *GET BYTE
            CPI      '9'                 *DISABLED?
            JZ       STANEXT             *DO NEXT ONE IF SO
            CALL     $TYPTX              *INDENT
            DB       ' '+080H
            CALL     STROUT              *OUTPUT THE NUMBER
            CALL     $TYPTX              *DO TWO TABS
            DB       09H,09H+080H
            POP      PSW                 *RESTORE CHANNEL
            PUSH     PSW                 *SAVE IT AGAIN
            CALL     GETDESC             *GET ADDRESS DESCRIPTION
            PUSH     B                   *SAVE NUMBER OF CHARS
            CALL     STROUT              *OUTPUT THE STRING
```

Listing 1 continued on page 258

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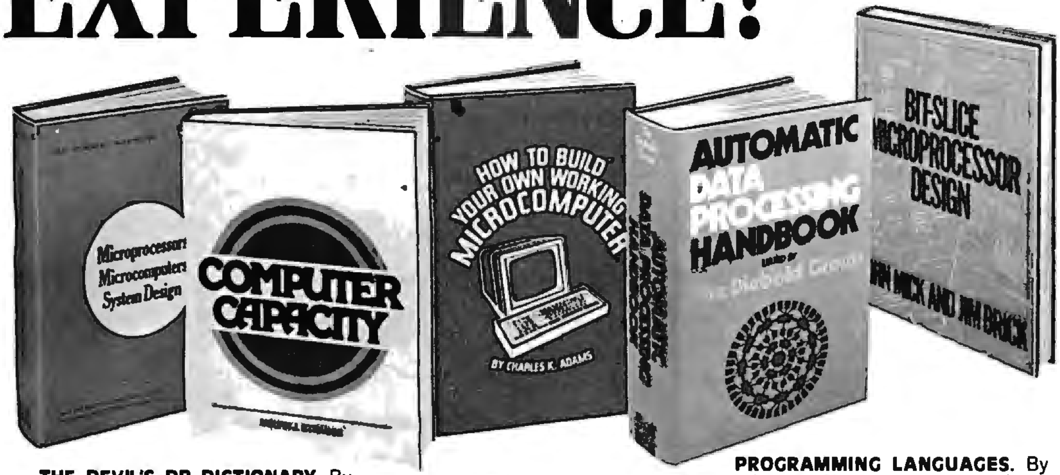

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P39543

Listing 1 continued:

```
          POP     B                   *RESTORE B
          MOV     A,C                 *NUMBER OF CHARS INTO A
          CMA     A                   *COMPLEMENT IT
          ADI     02BH                *NUMBER OF SPACES TO PAD
          JNC     STSKIP              *SKIP IF 47 ALREADY OUTPUT
          MOV     C,A                 *STORE THE NUMBER
STSPC     MVI     A,' '               *LOAD A SPACE
          SCALL   .SCOUT              *OUTPUT IT
          JC      STSPC               *LOOP UNTIL READY
          DCR     C                   *DECREMENT COUNT
          JNZ     STSPC               *LOOP UNTIL DONE
STSKIP    POP     PSW                 *RESTORE A
          PUSH    PSW                 *SAVE IT AGAIN
          CALL    GETLVL              *GET LEVEL BYTE
STWAIT    SCALL   .SCOUT              *OUTPUT IT
          JC      STWAIT              *LOOP UNTIL READY
          CALL    $TYPTX              *INDEX OVER TO PROPER COLUMN
          DB      '       ',' '+080H
          POP     PSW                 *GET CHANNEL NUMBER
          PUSH    PSW                 *SAVE IT AGAIN
          CALL    GETSTAT             *GET STATUS BYTE
          CPI     '1'                 *IS IT ONE?
          PUSH    PSW                 *SAVE FLAGS
          CZ      PRON                *PRINT ON IF SO
          POP     PSW                 *RESTORE FLAGS
          CNZ     PROFF               *ELSE PRINT OFF
          CALL    CRLF                *OUTPUT CARRIAGE RETURN
STANEXT   POP     PSW                 *RESTORE A
          POP     D                   *RESTORE D
          POP     B                   *RESTORE B
          INX     D                   *INCREMENT UNIT #
          DCR     C                   *DECREMENT COUNT
          JNZ     STATLP              *DO NEXT ONE
          RET                         *ALL DONE

**********
* PRINT ON OR OFF

PRON      CALL    $TYPTX
          DB      01BH,'p ON',01BH,'q'+080H
          RET

PROFF     CALL    $TYPTX
          DB      'OF','F'+080H
          RET


UTILITY ROUTINES

**********
* GET ADDRESS OF STATUS BYTE
*         ENTRY   A=CHANNEL NUMBER
*         EXIT    A=STATUS BYTE
*                 HL=STATUS BYTE ADDRESS
*         USES    ALL
```

Listing 1 continued on page 260.

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BUSINESS 100 PROGRAM LIST

	NAME	DESCRIPTION
1	RULE78	Interest Apportionment by Rule of the 78's
2	ANNUI	Annuity computation program
3	DATE	Time between dates
4	DAYYEAR	Day of year a particular date falls on
5	LEASEINT	Interest rate on lease
6	BREAKEVN	Breakeven analysis
7	DEPRSL	Straightline depreciation
8	DEPRSY	Sum of the digits depreciation
9	DEPRDB	Declining balance depreciation
10	DEPRDDB	Double declining balance depreciation
11	TAXDEP	Cash flow vs. depreciation tables
12	CHECK2	Prints NEBS checks along with daily register
13	CHECKBK1	Checkbook maintenance program
14	MORTGAGE/A	Mortgage amortization table
15	MULTMON	Computes time needed for money to double, triple, etc.
16	SALVAGE	Determines salvage value of an investment
17	RRVARIN	Rate of return on investment with variable inflows
18	RRCONST	Rate of return on investment with constant inflows
19	EFFECT	Effective interest rate of a loan
20	FVAL	Future value of an investment (compound interest)
21	PVAL	Present value of a future amount
22	LOANPAY	Amount of payment on a loan
23	REGWITH	Equal withdrawals from investment to leave 0 over
24	SIMPDISK	Simple discount analysis
25	DATEVAL	Equivalent & nonequivalent dated values for oblig.
26	ANNUDEF	Present value of deferred annuities
27	MARKUP	% Markup analysis for items
28	SINKFUND	Sinking fund amortization program
29	BONDVAL	Value of a bond
30	DEPLETE	Depletion analysis
31	BLACKSH	Black Scholes options analysis
32	STOCVAL1	Expected return on stock via discounts dividends
33	WARVAL	Value of a warrant
34	BONDVAL2	Value of a bond
35	EPSEST	Estimate of future earnings per share for company
36	BETAALPH	Computes alpha and beta variables for stock
37	SHARPE1	Portfolio selection model-i.e. what stocks to hold
38	OPTWRITE	Option writing computations
39	RTVAL	Value of a right
40	EXPVAL	Expected value analysis
41	BAYES	Bayesian decisions
42	VALPRINF	Value of perfect information
43	VALADINF	Value of additional information
44	UTILITY	Derives utility function
45	SIMPLEX	Linear programming solution by simplex method
46	TRANS	Transportation method for linear programming
47	EOQ	Economic order quantity inventory model
48	QUEUE1	Single server queueing (waiting line) model
49	CVP	Cost-volume-profit analysis
50	CONDPROF	Conditional profit tables
51	OPTLOSS	Opportunity loss tables
52	FQUOQ	Fixed quantity economic order quantity model
53	FQEOWSH	As above but with shortages permitted
54	FQEOQPB	As above but with quantity price breaks
55	QUEUECB	Cost-benefit waiting line analysis
56	NCFANAL	Net cash-flow analysis for simple investment
57	PROFIND	Profitability index of a project
58	CAP1	Cap. Asset Pr. Model analysis of project
59	WACC	Weighted average cost of capital
60	COMPBAL	True rate on loan with compensating bal. required
61	DISCBAL	True rate on discounted loan
62	MERGANAL	Merger analysis computations
63	FINRAT	Financial ratios for a firm
64	NPV	Net present value of project
65	PRINDLAS	Laspeyres price index
66	PRINDPA	Paasche price index
67	SEASIND	Constructs seasonal quantity indices for company
68	TIMETR	Time series analysis linear trend
69	TIMEMOV	Time series analysis moving average trend
70	FUPRINF	Future price estimation with inflation
71	MAILPAC	Mailing list system
72	LETWRT	Letter writing system-links with MAILPAC
73	SORT3	Sorts list of names
74	LABEL1	Shipping label maker
75	LABEL2	Name label maker
76	BUSBUD	DOME business bookkeeping system
77	TIMECLCK	Computes weeks total hours from timeclock info.
78	ACCTPAY	In memory accounts payable system-storage permitted
79	INVOICE	Generate invoice on screen and print on printer
80	INVENT2	In memory inventory control system
81	TELDIR	Computerized telephone directory
82	TIMUSAN	Time use analysis
83	ASSIGN	Use of assignment algorithm for optimal job assign.
84	ACCTREC	In memory accounts receivable system-storage ok
85	TERMSPAY	Compares 3 methods of repayment of loans
86	PAYNET	Computes gross pay required for given net
87	SELLPR	Computes selling price for given after tax amount
88	ARBCOMP	Arbitrage computations
89	DEPRSF	Sinking fund depreciation
90	UPSZONE	Finds UPS zones from zip code
91	ENVELOPE	Types envelope including return address
92	AUTOEXP	Automobile expense analysis
93	INSFILE	Insurance policy file
94	PAYROLL2	In memory payroll system
95	DILANAL	Dilution analysis
96	LOANAFFD	Loan amount a borrower can afford
97	RENTPRCH	Purchase price for rental property
98	SALELEAS	Sale-leaseback analysis
99	RRCONVBD	Investor's rate of return on convertable bond
100	PORTVAL9	Stock market portfolio storage-valuation program

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Listing 1 continued:

```
GETSTAT MOV     C,A                 *CHANNEL NUMBER IN C
        MVI     B,0                 *CLEAR B
        LXI     H,UNITLOC           *ADDRESS OF FIRST UNIT
        DAD     B                   *ADD OFFSET
        DAD     B                   *ADD IT AGAIN
        CALL    $HLIHL              *GET THE ADDRESS
        MOV     A,M                 *FETCH THE STATUS BYTE
        RET                         *RETURN

**********
* GET ADDRESS OF LEVEL BYTE
*       ENTRY   A=CHANNEL NUMBER
*       EXIT    A=LEVEL BYTE
*              HL=LEVEL BYTE ADDRESS
*       USES    ALL

GETLVL  CALL    GETSTAT             *GET THE STATUS BYTE
        INX     H                   *INDEX TO LEVEL BYTE
        MOV     A,M                 *LOAD THE BYTE
        RET

**********
* GET THE DESCRIPTOR STRING ADDRESS
*       ENTRY   A=CHANNEL NUMBER
*       EXIT    C=NUMBER OF CHARACTERS TO PRINT
*              HL=FWA OF STRING
*       USES    ALL

GETDESC CALL    GETLVL              *GET LEVEL BYTE
        INX     H                   *INCREMENT TO PROPER BYTE
        INX     H
        INX     H
        PUSH    H                   *SAVE FWA
        LXI     B,0                 *CLEAR BC
DESLOOP MOV     A,M                 *FETCH A CHARACTER
        CPI     0AH                 *CARRIAGE RETURN?
        JZ      DESDONE             *RETURN IF SO
        INX     B                   *INCREMENT COUNT
        INX     H                   *INCREMENT POINTER
        JMP     DESLOOP             *AND DO AGAIN
DESDONE POP     H                   *RESTORE FWA
        RET                         *AND RETURN

**********
* OUTPUT A GIVEN STRING
*       ENTRY   HL=FWA OF STRING ADDRESS
*               C =NUMBER OF CHARACTERS TO PRINT
*       USES    ALL

STROUT  MOV     A,C                 *GET COUNT
        ANA     A                   *SET FLAGS
        JZ      STRDONE             *NOTHING TO OUTPUT
STRLOOP MOV     A,M                 *FETCH A BYTE
        SCALL   .SCOUT              *OUTPUT IT
        JC      STRLOOP             *WAIT UNTIL READY
        INX     H                   *NEXT BYTE ADDRESS
        DCR     C                   *COUNT ONE DONE
```

Listing 1 continued on page 262

Listing 1 continued:

```
         JNZ      STRLOOP            *LOOP UNTIL DONE
STRDONE  RET                         *AND RETURN

**********
* OUTPUT A CARRIAGE RETURN/LINE FEED

CRLF     CALL     $TYPTX
         DB       0AH+080H
         RET

**********
* GET ADDRESS OF CHANNEL NUMBER ASCII STRING
*        ENTRY    A=CHANNEL NUMBER
*        EXIT     C=NUMBER OF CHARS TO PRINT
*                HL=FWA OF ASCII STRING
*        USES     ALL

GETCHAN  CALL     GETLVL             *GET LEVEL BYTE
         INX      H                  *POINT TO CHANNEL
         MVI      C,2                *LOAD CHARS
         RET                         *RETURN

**********
* CALCULATE WAIT REQUIRED
*        ENTRY    A=CHANGE
*        USES ALL
*        EXIT     BC=COUNT TO WAIT

CALC:    PUSH     PSW                *SAVE A
         ADD      A                  *A=2*A
         ADD      A                  *A=4*A
         MVI      B,1                *SET B=1
         MOV      C,A                *C=4*A
         POP      PSW                *GET 1*A BACK
         ADD      C                  *A=5*A
         MOV      C,A                *C=5*A
         RET

LVLCHG   PUSH     B                  *SAVE BC
         CALL     SENDIT             *SEND THE COMMAND
         POP      B                  *RESTORE B
```

Listing 1 continued on page 264

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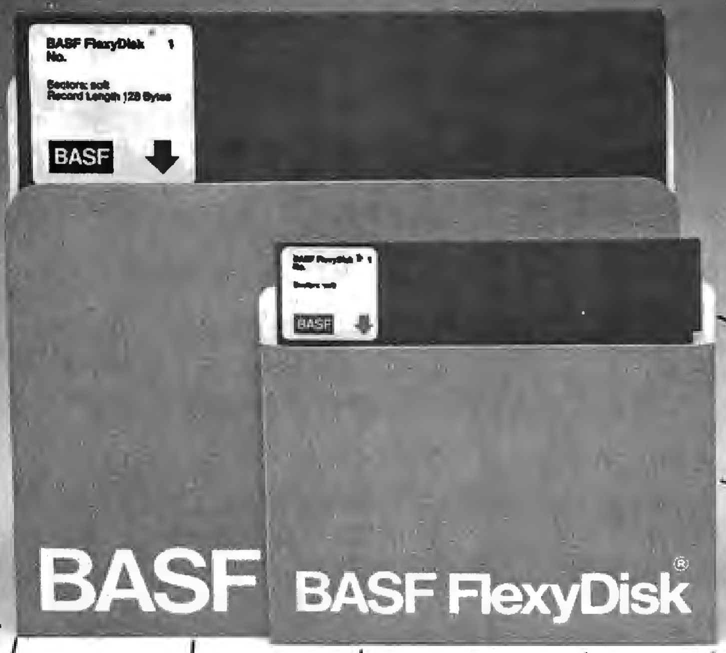
Listing 1 continued:

```
        DCR     C               *DECREMENT INNER LOOP
        JNZ     LVLCHG          *LOOP UNTIL ZERO
        DCR     B               *DECREMENT OUTER LOOP
        JNZ     LVLCHG          *LOOP UNTIL DONE
        RET

*****************************************************************
*                       SEND THE CODE
*
* SET UP THE COMMAND BYTES TO REFLECT THE CODE DESIRED

INDEX   MVI     B,0             *CLEAR B
        MOV     C,A             *OFFSET IN C
        LXI     H,ONE           *FIRST COMMAND LOCATION
        DAD     B               *ADD OFFSET
        MOV     A,M             *GET THE BYTE
        STA     COMMAND         *STORE IT
SENDIT  LDA     COMMAND         *GET THE COMMAND BYTE
        XRI     11111111B       *COMPLEMENT THE ACCUMULATOR
        STA     COMMAND+1       *STORE THE COMPLEMENTED BYTE
        LDA     COMMAND         *GET THE ORIGINAL VALUE BACK

*START SENDING THE CODE

        CALL    SEND1           *ALERT COMMAND MODULE OF MESSAGE
        CALL    ROTOUT          *ROTATE A AND SEND BITS
        LDA     COMMAND+1       *GET THE COMPLEMENTED COMMAND
        CALL    ROTOUT          *SEND THE COMPLEMENTED BYTE
        CALL    EOM             *SEND END OF MESSAGE
        RET                     *RETURN WHEREVER

*****************************************************************
*       ROUTINES TO SEND LOGIC CONTROL PULSES TO THE BSR
*
*
* ROTATE A AND SEND APPROPRIATE LOGICAL BITS

ROTOUT  MVI     E,05H           *COUNT IN E - 5 BITS TO SEND
ROTLOOP RAL                     *PUT A BIT INTO THE CARRY POSITION
        CC      SEND1           *SEND A ONE IF BIT IS 1
        CNC     SEND0           *ELSE SEND A ZERO
        DCR     E               *DECREMENT THE COUNT
        RZ                      *RETURN IF DONE
        JMP     ROTLOOP         *ELSE CONTINUE

*WAIT BETWEEN COMMANDS

WAIT    PUSH    PSW             *SAVE A AND FLAGS
        LXI     H,075H          *36ms TIMING CONSTANT
        CALL    DELAY           *AND WAIT
        POP     PSW             *RESTORE A AND F
        RET                     *RETURN WHEREVER

* SEND LOGIC '1' ROUTINE
*       SEND 4ms ON PULSE AND 4ms OFF PULSE
*       (4ms EQUALS 160 STATES)
```

Listing 1 continued on page 266

Ten reasons why your floppy disk should be a BASF FlexyDisk.®



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Listing 1 continued:

```
SEND1   PUSH    PSW                     *SAVE A AND FLAGS
        CALL    OSCENA                  *ENABLE THE BSR OSCILLATOR
        LXI     H,0EH                   *TIMING CONSTANT
        CALL    DELAY                   *AND WAIT
        CALL    OSCOFF                  *TURN OFF OSCILLATOR
        LXI     H,0EH                   *OFF TIME DELAY
        CALL    DELAY                   *WAIT
        POP     PSW                     *RESTORE A AND F
        RET                             *RETURN WHEREVER

***     WAIT 1.2ms ON PULSE AND 6.8 ms OFF PULSE
*       (LOGIC ZERO)

SEND0   PUSH    PSW                     *SAVE A AND FLAGS
        CALL    OSCENA                  *ENABLE THE BSR OSCILLATOR
        LXI     H,2                     *TIMING CONSTANT
        CALL    DELAY                   *AND WAIT
        CALL    OSCOFF                  *TURN OFF OSCILLATOR
        LXI     H,01AH                  *OFF TIME DELAY
        CALL    DELAY                   *WAIT
        POP     PSW                     *RESTORE A AND F
        RET                             *RETURN WHEREVER

***
*       END OF MESSAGE - 12 ms ON SIGNAL - 4ms OFF

EOM     PUSH    PSW                     *SAVE A AND FLAGS
        CALL    OSCENA                  *ENABLE THE BSR OSCILLATOR
        LXI     H,02AH                  *TIMING CONSTANT
        CALL    DELAY                   *AND WAIT
        CALL    OSCOFF                  *TURN OFF OSCILLATOR
        LXI     H,0EH                   *OFF TIME DELAY
        CALL    DELAY                   *WAIT
        POP     PSW                     *RESTORE A AND F
        RET                             *RETURN WHEREVER

*ENABLE THE 40KHZ OSCILLATOR
OSCENA  MVI     A,0FFH                  *ENABLE BIT
        OUT     PORT                    *OUTPUT IT
        RET

*DISABLE THE OSCILLATOR
OSCOFF  MVI     A,000H                  *DISABLE BIT
        OUT     PORT                    *OUTPUT IT
        RET

*TIMING LOOP - ENTER WITH TIMING CONSTANT IN H-L
DELAY   PUSH    D                       *SAVE D-E
DELAY1  LXI     D,01EH                  *INNER LOOP CONSTANT
DELAY2  DCR     E                       *DECREMENT INNER LOOP
        JNZ     DELAY2                  *KEEP WAITING
        DCR     L                       *ELSE DECREMENT OUTER LOOP
        JNZ     DELAY1                  *AND WAIT SOME MORE
        POP     D                       *RESTORE D-E
        RET                             *AND RETURN
```

Listing 1 continued on page 268

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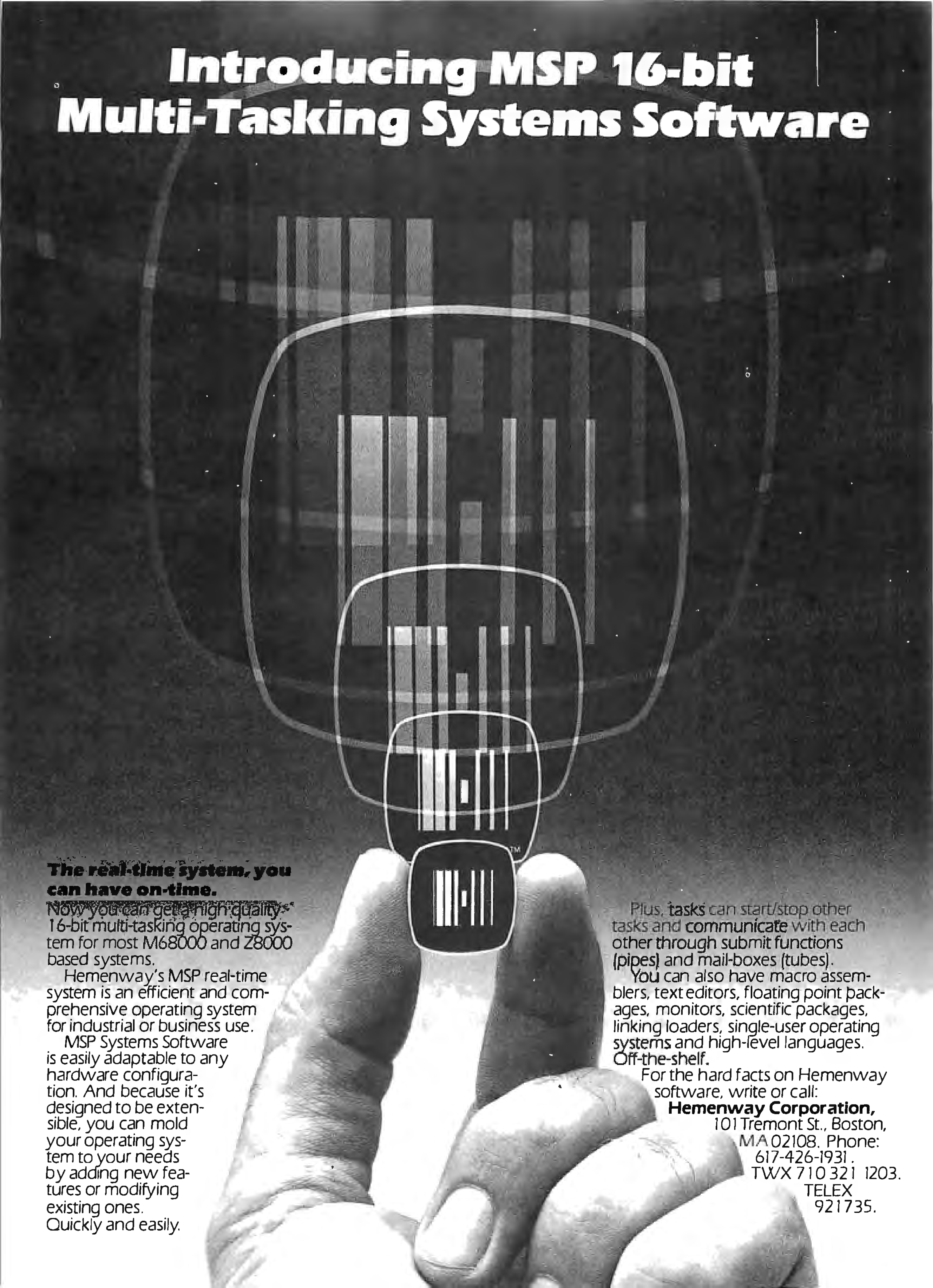
Circle 46 on inquiry card.

Listing 1 continued:

```
***********
* UPDATE STATUS BYTE TO SHOW IF UNIT IS OFF OR ON
*       ENTRY   A=CHANNEL NUMBER(0-15)
*       USES    ALL

ZEROBIT CALL    GETSTAT         *GET THE BYTE
        MVI     M,'0'           *STORE ZERO
        RET                     *AND RETURN

SETBIT  CALL    GETSTAT         *GET THE BYTE
        MVI     M,'1'           *STORE ONE
        RET                     *AND RETURN


*BSR COMMAND ROUTINES

***********
* TURN OFF ALL UNITS
*       ENTRY   NONE
*       USES    ALL

OFFALL  LXI     D,010H          *NUMBER OF UNITS
OFFALL1 MOV     A,E             *LOAD UNIT NUMBER
        SBI     1               *SUBTRACT OFFSET
        CALL    ZEROBIT         *UPDATE STATUS
        DCR     E               *DECREMENT COUNT
        JNZ     OFFALL1         *LOOP UNTIL DONE
```

Listing 1 continued on page 270



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Listing 1 continued:

```
        LDA     ALLOFF          *LOAD THE COMMAND
        STA     COMMAND         *STORE IT
        CALL    SENDIT          *AND SEND THE COMMAND
        RET

***********
* TURN ON ALL UNITS
*       ENTRY   NONE
*       USES    ALL

ONALL   LXI     D,010H          *NUMBER OF UNITS
ONALL1  MOV     A,E             *LOAD UNIT NUMBER
        SBI     1               *SUBTRACT OFFSET
        CALL    SETBIT          *UPDATE STATUS
        DCR     E               *DECREMENT COUNT
        JNZ     ONALL1          *LOOP UNTIL DONE
        LDA     ALLON           *LOAD THE COMMAND
        STA     COMMAND         *STORE IT
        CALL    SENDIT          *AND SEND THE COMMAND
        RET

***********
* TURN A SINGLE UNIT OFF OR ON
*       ENTRY   A=CHANNEL OFFSET
*       USES    ALL

OFFONE  PUSH    PSW             *SAVE CHANNEL
        CALL    INDEX           *SEND CHANNEL CODE
        CALL    WAIT            *PAUSE BETWEEN COMMANDS
        POP     PSW             *GET CHANNEL BACK
        CALL    ZEROBIT         *UPDATE STATUS
        LDA     OFF             *LOAD THE COMMAND
        STA     COMMAND         *STORE IT
        CALL    SENDIT          *SEND THE CODE
        RET                     *ALL DONE

ONONE   PUSH    PSW             *SAVE CHANNEL
        CALL    INDEX           *SEND CHANNEL CODE
        CALL    WAIT            *PAUSE BETWEEN COMMANDS
        POP     PSW             *GET CHANNEL BACK
        CALL    SETBIT          *UPDATE STATUS
        LDA     ON              *LOAD THE COMMAND
        STA     COMMAND         *STORE IT
        CALL    SENDIT          *SEND THE CODE
        RET                     *ALL DONE

***********
* ADJUST LAMP INTENSITY
*       ENTRY   A=CHANNEL NUMBER(0-15)
*               DE=REQUESTED LEVEL(0-9 ASCII)
*       USES    ALL

INTEN   PUSH    D               *SAVE REQUESTED LEVEL
        PUSH    PSW             *SAVE THE CHANNEL NUMBER
        CALL    GETSTAT         *GET THE STATUS BYTE
        CPI     '1'             *IS IT ON?
        JZ      ITSON           *YES - ADJUST LEVEL
        POP     PSW             *GET UNIT NUMBER BACK
```

Listing 1 continued on page 272

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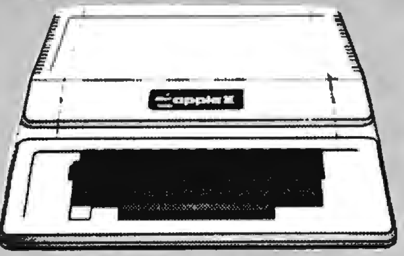

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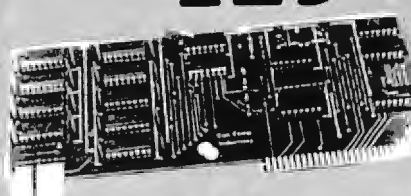

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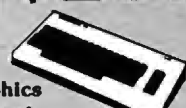

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Circle 103 on inquiry card.

Listing 1 continued:

```
        PUSH    PSW             *SAVE IT
        CALL    ONONE           *TURN ON THE UNIT
ITSON   POP     PSW             *RETURN CHANNEL NUMBER
        PUSH    PSW             *SAVE IT AGAIN
        CALL    INDEX           *SELECT UNIT CODE AND TRANSMIT
        CALL    LONGWT          *WAIT BTEWEEN COMMANDS
        POP     PSW             *RESTORE CHANNEL NUMBER
        CALL    GETLVL          *GET THE LEVEL BYTE
        POP     D               *RESTORE REQUESTED LEVEL
        SUB     E               *SUBTRACT REQUESTED LEVEL
        RZ                      *NO CHANGE REQUESTED - RETURN
        JC      BRIGHTR         *CARRY - BRIGHTER REQUEST
        MOV     M,E             *STORE NEW LEVEL
        CALL    CALC            *GET WAITING PERIOD
        LDA     DIM             *GET THE COMMAND
        STA     COMMAND         *STORE IT
        CALL    LVLCHG          *OUTPUT IT
        RET                     *ALL DONE
BRIGHTR MOV     M,E             *STORE NEW LEVEL
        CMA     A               *COMPLEMENT - NUMBER IN A
        ADI     1               *ADD ONE
        CALL    CALC            *GET WAIT
        LDA     BRIGHT          *GET COMMAND
        STA     COMMAND         *STORE IT
        CALL    LVLCHG          *SENT IT
        RET                     *AND RETURN

**********
* PRINT MANUAL CONTROL MENU
*       ENTRY   NONE
*       USES    ALL
MENU    CALL    $TYPTX          *PRINT AVAILABLE SELECTIONS
        DB      01BH,045H,0AH,09H,09H,09H
        DB      01BH,'pMANUAL CONTROL MENU',01BH,'q',0AH,0AH,0AH
        DB      'Commands Available:',0AH,0AH
        DB      09H,'0.......... Exit Program',0AH
        DB      09H,'1.......... All Units Off',0AH
        DB      09H,'2.......... All Units On',0AH
        DB      09H,'3.......... Single Unit Off',0AH
        DB      09H,'4.......... Single Unit On',0AH
        DB      09H,'5.......... Single Unit Brightness Adjust'
        DB      0AH
        DB      09H,'6.......... Return to Status Display'
        DB      0AH,0AH,0AH
        DB      'Enter Number Of Choice',' '+080H

MENUIN  SCALL   .SCIN           *GET COMMAND
        JC      MENUIN          *LOOP UNTIL READY
        PUSH    PSW             *SAVE IT
        SCALL   .CLRCO          *CLEAR CONSOLE BUFFER
        POP     PSW             *RESTORE COMMAND
        SUI     '0'             *LESS THAN ZERO?
        JC      MENUERR         *ERROR IF SO
        CPI     7               *MORE THAN 6?
        JNC     MENUERR         *ERROR IF SO
        CALL    $TJMP           *JUMP TO PROPER ROUTINE
        DW      EXIT
```

Listing 1 continued on page 274

TASC.™ The Applesoft* Compiler. It turns your Apple into a power tool.

Step up to speed. TASC, the Applesoft Compiler, converts a standard Applesoft BASIC program into super-fast machine code. By increasing program execution speed up to 20 times, Microsoft gives you a power tool for Applesoft BASIC programming.

Highest capacity available. TASC will compile and run larger programs than any other Applesoft Compiler. As a disk-based system, it doesn't require the simultaneous presence of compiler and program in memory. The memory you save allows you to compile significantly bigger programs.

Power without bulk. Code expansion of up to 100% severely restricts other compilers. TASC's special code compression schemes typically limit code expansion to only 25%. You'll really appreciate that with complex programs or programs that utilize Apple's hi-res graphic pages.

More BASIC power. TASC's powerful new commands increase Applesoft BASIC programming capability. Chain with COMMON allows compiled programs to share variables, so a main menu

supports several programs in a single runtime environment.

TASC's True Integer Arithmetic and Integer FOR...NEXT capabilities maximize the execution speed of compiled programs. TASC's near total compatibility with Applesoft speeds compilation of existing programs with little or no modification.

What about mistakes? You perfect your programs interactively with Applesoft. If something does slip by, TASC recovers from errors discovered in compilation and traps all runtime errors. It even permits graceful interruptions during compilation.

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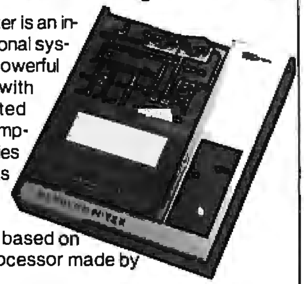
Circle 249 on inquiry card.

Listing 1 continued:

```
         DW       AOFF
         DW.      AON
         DW       OOFF
         DW       OON
         DW       ADJUST
         DW       MENDONE

EXIT     XRA      A                  *CLEAR A
         SCALL    .EXIT              *NORMAL EXIT

AOFF     CALL     OFFALL             *TURN THEM OFF
         JMP      MENDONE            *RETURN

AON      CALL     ONALL              *TURN THEM ON
         JMP      MENDONE            *RETURN

OOFF     CALL     CHAMENU            *PRINT MENU
         CALL     $TYPTX
         DB       0AH,0AH,'Number of Unit to Turn Off?',' '+080H
         CALL     CHANIN             *GET SELECTION
         CALL     OFFONE             *TURN IT OFF
         JMP      MENDONE            *ALL DONE

OON      CALL     CHAMENU            *PRINT MENU
         CALL     $TYPTX
         DB       0AH,0AH,'Number of Unit to Turn ',01BH,'pON'
         DB       01BH,'q?',' '+080H
         CALL     CHANIN             *GET SELECTION
         CALL     ONONE              *TURN IT ON
         JMP      MENDONE            *ALL DONE

ADJUST   CALL     CHAMENU            *PRINT MENU
         CALL     $TYPTX
         DB       0AH,0AH,'Number of Unit on Which to Adjust'
         DB       'Brightness?',' '+080H
         CALL     CHANIN             *GET CHANNEL NUMBER
```

Listing 1 continued on page 278

The Nanocomputer: the professional approach to microcomputers



The Nanocomputer is an integrated educational system based on a powerful microcomputer with education-oriented software and complemented by a series of training books written specially for the system.

POWERFUL — based on the Z80 microprocessor made by SGS-ATES

COMPLETE — hardware, software and peripherals backed by a series of step-by-step training books on programming, digital electronics and interfacing.

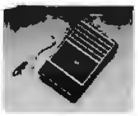
MODULAR — as the student learns, the hardware can be expanded to introduce new concepts and experiments: Z80 code programming, interfacing and high-level languages (BASIC).

NBZ80S Nano Computer Includes the Nano Computer with power supply, the NEZ80 bread board for experiments and interfacing, the card frame, K1Z80 Cable Kit, the technical manual and training books one and three $570.00

K1Z80 Extra K1Z80 Cable Kit 11.00

K2Z80 Active and experimental component kit 33.10

K3Z80 Socket kit with 3 40 pin sockets 5.70



RCZ80/P Cassette recorder for all Nano Computer Systems (requires a W10Z80 see below) 88.60

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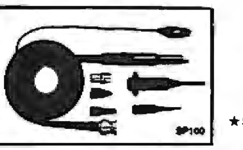

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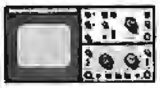

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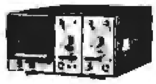
- Triggering up to 30 MHz
- 8cm x 10cm Display

HM203 .... $580.00
HM203N with long persis $600.00

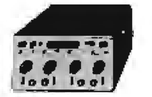
10 MHz SINGLE TRACE



- DC-10 MHz Bandwidth
- LPS-Triggering
- Component Tester Built-in
- Timebase 0.2μs-0.2s/cm

HM307 .... $405.00

4-CHANNEL AMPLIFIER



- DC-50 MHz Bandwidth
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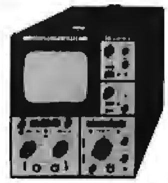
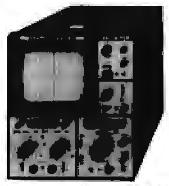


20 MHz DUAL TRACE

• Overscanning • LPS Trig to 40 MHz
• Delayed Sweep • DC-20 MHz

Internal stabilized power supplies. Both vertical channels incorporate a varible gain control which increases the gain to 2 mV/cm. Channels can be Added or Subtracted. A special feature of the HM412 is the vertical Overscanning facility, location of a "lost" trace is indicated on two LED's. Both the trigger and delayed conditions are indicated by LED's. These facilities coupled with graticule illumination, Z Modulation, and a square-wave calibrator make the HM412 a very versatile instrument.

HM412 with sweep delay $880.00
HM412N with delay and long persis ... $985.00



70 MHz DUAL TRACE

• DC-70MHz • Sweep Delay 0.1μs-1s
• Sens. 2mV/cm • Graticule 8x10cm

General-purpose scope designed for both laboratory and field service. The HM705 triggers even complex signals beyond 100MHz. Two non-synchronus signals, or a composite signal with a non-synchronus component, and also aperiodic events can likewise be triggered. Single-shot operation is also possible. The wide sweep range from 5ns/cm (including x10 magnification) to 2.5s/cm gives an excellent resolution. These features and others make the HM705 an instrument of great flexibility in all fields.

HM705 with delay $885.00
HM705N with delay and long persis $1000.00

50 MHz DUAL TRACE

- 50 MHz Dual Trace Storage Scope Plus Varible Persistence
- Delayed Sweep with After-Delay-Trig.
- Storage of Single-Shot Signals "Automatic Store"
- LED Indication for Overscanning, Single-Shot, Trigger Action, Delay Mode and Automatic Store
- Automatic Blanking

HM812-2 .... $4032.00

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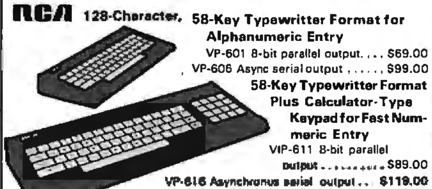

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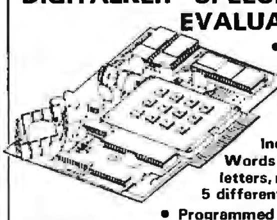

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The DT1000 speech synthesis evaluation board is an extremely easy to use device for understanding the operation and application of the DIGITALKER chip set in an end product.

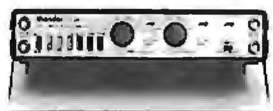
The DT1000 contains all components required to output speech upon demand: a speech processor chip, 2 MAXI-ROMs* containig 138 individual words, linear filter, audio amplifier, keyboard, and a COPS™ microcontroller complete with stored data programmed to provide the various functions on the board. The only external hardware required for complete operation are a single 7V-11V power supply and speaker.

DT1000 Evaluation Board Kit $495.00

The DT1050 is a 2-chip set for speech synthesis. It contains a speech processor chip and a speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech.

DT1050 2-Chip set $85.00

TG105 PULSE GENERATOR



- Period: 200nsec to 200ms (5MHz to 5Hz)
- Pulse Width: 100nsec to 100ms
- 50 ohm output range: 0.1V-10V
- TTL output • Sync. output
- Operating Modes: Run, External trigger, External gate, Manual 1-shot or Gate
- Compliment and square wave

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MC78M06CT	1.47	MC1391P	1.44	MC3302P	1.12	MC6860P	12.92	MC10125L	3.01	MPN3402	.76	MRF476	2.93
MC78M08CT	1.47	MC1403U0	4.08	MC3303P	5.80	MC6875L	13.49	MC10125P	2.52	MPS918	1.28	MRF901	3.15
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MC78M18CT	1.47	MC1408L7	4.75	MC3360P	3.50	MC6885P	2.72	MC10189L	3.27	MPS6514	.68	MV839	2.42
MC78M20CT	1.47	MC1408L8	6.55	MC3370P	3.72	MC6886P	2.72	MC10195L	2.52	MPS6520	.72	MV2115	2.27
MC78M24CT	1.47	MC1408P8	4.40	MC3403P	1.77	MC6887P	2.72	MC10216L	1.83	MPS6521	.83	MV2205	.78
MC79L05CP	1.12	MC1413P	1.68	MC3405P	3.60	MC6888P	2.72	MC14411P	17.26	MPS6522	.76	MV2209	.78
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MC79L24CP	1.12	MC1439L	4.62	MC3417L	14.83	MC7808CT	1.65	MC14457P	6.60	MPS8099	.57	SC1360	1.17
MC664P	3.20	MC1439P1	3.97	MC3420L	10.08	MC7812CK	3.14	MC14458P	13.73	MPS8599	.60	SC141B	1.76
MC680P	2.05	MC1445G	4.20	MC3423P1	1.66	MC7812CT	1.65	MC14490FP	5.60	MPSA06	.73	SC141D	1.98
MC684P	5.10	MC1456P1	.99	MC3438L	4.33	MC7815CK	3.14	MC14490VP	4.24	MPSA12	.85	T2800B	1.91
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MC839L	5.88	MC1458CP1	1.08	MC3476P1	3.18	MC7824CK	3.14	MC68488P	32.26	MPSA42	.82	TIP110	1.36
MC848L	3.17	MC1458P1	1.08	MC3480P	12.85	MC7902CT	2.10	MCA255	1.76	MPSA56	.88		
MC847L	2.46	MC1458P1S	1.33	MC3503L	18.62	MC7905CT	2.10	MCM68A10P	5.59	MPSA64	.75		
MC857P	1.50	MC1488L	1.68	MC4016P	10.10	MC7906CK	4.20	MCM6666L25	46.50	MPSA70	.44		

Circle 27 on inquiry card.

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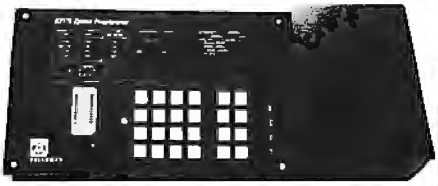

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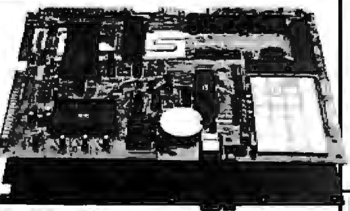

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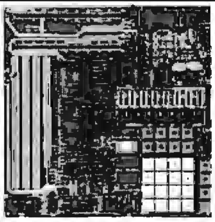

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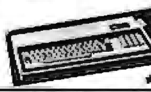

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2.00	HC33	CY2A	8.25	5.068	HC18	[illegible]	6.00	18.432	HC18	CY18B	[illegible]
2.4576	HC33	CY2B	[illegible]	5.7143	HC18	[illegible]	[illegible]	19.6608	HC18	CY20A	[illegible]
3.2768	HC33	CY3B	6.00	6.00	HC18	[illegible]	6.00	[illegible]	HC18	CY22A	[illegible]
3.579	HC33	CY3D	[illegible]	6.144	HC18	[illegible]	6.00	23.584	HC18	CY23B	[illegible]
4.00	HC18	CY3A	6.00	8.00	HC18	[illegible]	[illegible]	27.00	HC18	CY27A	[illegible]
4.434	HC18	CY4C	6.00	10.00	HC18	CY12A	4.75	32.00	HC18	CY32A	[illegible]
[illegible]	HC18	[illegible]	[illegible]	14.31818	HC18	CY14A	4.75	[illegible]	HC18	[illegible]	[illegible]

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74C08N	.38	74C107N	1.89	74C240N	2.28	74C922N	5.65
74C10N	.38	74C150N	5.67	74C244N	2.28	74C923N	5.75
74C14N	.76	74C151N	3.80	74C373N	2.67	74C925N	7.46
74C20N	.38	74C154N	5.67	74C374N	2.67	74C926N	7.46
74C30N	.38	74C157N	3.40	74C901N	.71	74C927N	7.46
74C32N	.38	74C160N	1.71	74C902N	.71	74C928N	7.46
74C42N	1.42	74C161N	1.71	74C903N	.71	74C932N	2.22
74C48N	2.13	74C162N	1.71	74C904N	.71	74C941N	2.28
74C73N	.90	74C163N	1.71	74C905N	11.20	74C989N	7.80
74C74N	.87	74C164N	1.61	74C906N	.71	80C95N	.79
74C76N	.90	74C165N	1.61	74C907N	.71	80C96N	.79
74C83N	2.00	74C173N	1.50	74C908N	1.49	80C97N	.79
74C85N	2.00	74C174N	1.20	74C909N	2.54	80C98N	.79
74C86N	.99	74C192N	1.71	74C910N	12.05	82C19N	5.67
74C89N	7.80	74C193N	1.71	74C911N	11.00	88C29N	2.98
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				74C914N	2.18		

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Listing 1 continued:

```
        PUSH    PSW                     *SAVE IT
ADJREQ  CALL    $TYPTX
        DB      01BH,045H,0AH,'Brightness Level (0=Dim,'
        DB      ' 9=Bright)?',' '+080H
ADJIN   SCALL   .SCIN                   *GET THE LEVEL
        JC      ADJIN                   *LOOP UNTIL READY
        PUSH    PSW                     *SAVE THE INPUT
        SCALL   .CLRCO                  *CLEAR THE INPUT BUFFER
        POP     PSW                     *GET INPUT BACK
        MOV     E,A                     *STORE REQUESTED LEVEL
        MVI     D,0                     *CLEAR D
        SBI     '0'                     *LESS THAN 0?
        JC      ADJREQ                  *ERROR IF SO
        CPI     0AH                     *MORE THAN 9?
        JNC     ADJREQ                  *ERROR IF SO
        POP     PSW                     *RESTORE CHANNEL NUMBER
        CALL    INTEN                   *ADJUST THE LEVEL
        JMP     MENDONE                 *RETURN.

MENDONE RET                             *RETURN TO MAIN PROGRAM

MENUERR CALL    $TYPTX
        DB      07H,0AH,0AH,0AH,01BH
        DB      'pINVALID INPUT - HIT RETURN TO CONTINUE'
        DB      01BH,'q'+080H
ERRWAIT SCALL   .SCIN                   *GET CHARACTER
        JC      ERRWAIT                 *LOOP UNTIL READY
        CPI     0AH                     *RETURN?
        JNZ     ERRWAIT                 *LOOP UNTIL TRUE
        JMP     MENU                    *AND TRY AGAIN

*CHANNEL SELECTION MENU ROUTINES

 ***********
 * PRINT CHANNEL NUMBER SELECTION MENU
 *      ENTRY   NONE
 *      USES    ALL

CHAMENU CALL    $TYPTX
        DB      01BH,045H,09H,09H,09H,01BH,'pCHANNEL SELECTION'
        DB      'MENU',01BH,'q',0AH,0AH+080H
        LXI     D,010H                  *NUMBER OF CHANNELS
        LXI     B,0                     *CLEAR BC
MENULP  PUSH    D                       *SAVE THE NUMBER
        PUSH    B                       *SAVE BC
        MOV     A,C                     *GET CHANNEL NUMBER
        PUSH    PSW                     *SAVE IT
        CALL    GETCHAN                 *GET LOCATION OF CHANNEL STRING
        MOV     A,M                     *GET FIRST BYTE
        CPI     '9'                     *DISABLED?
        JZ      MENEXT                  *DO NEXT ONE IF SO
        CALL    $TYPTX                  *INDENT LINE
        DB      09H+080H
        CALL    STROUT                  *PRINT CHANNEL NUMBER
        CALL    $TYPTX
        DB      '..........',' '+080H
        POP     PSW                     *CHANNEL NUMBER
```

Listing 1 continued on page 280

Listing 1 continued:

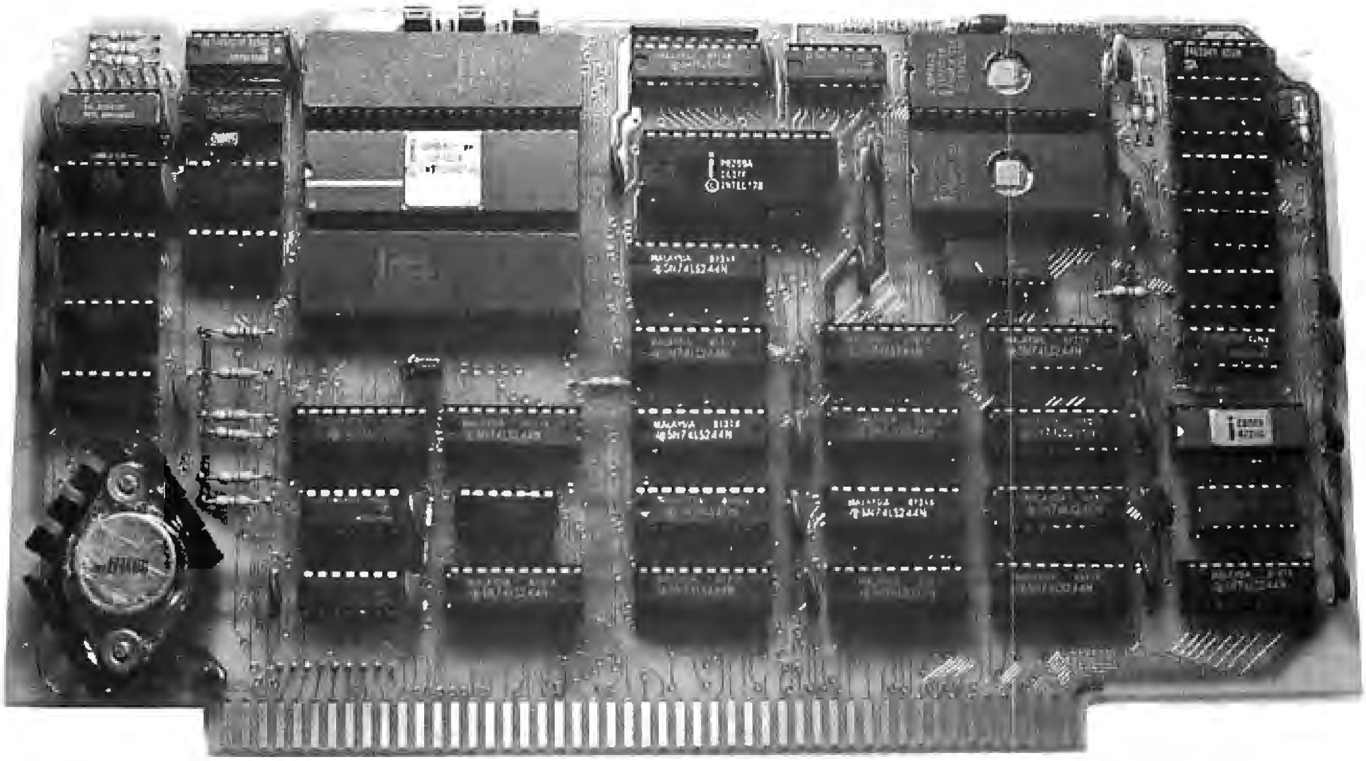
```
PUSH     PSW                   *KEEP STACK STRAIGHT
         CALL     GETDESC          *GET DESCRIPTION ADDRESS
         CALL     STROUT           *PRINT IT
         CALL     CRLF             *NEW LINE
MENEXT   POP      PSW              *RESTORE A
         POP      B                *RESTORE B
         POP      D                *RESTORE D
         INX      B                *INCREMENT CHANNEL NUMBER
         DCR      E                *DECREMENT COUNT
         JNZ      MENULP           *OUTPUT UNTIL DONE
         RET                       *ALL DONE

**********
* GET CHANNEL SELECTION
*        ENTRY    NONE
*        EXIT     A=CHANNEL OFFSET(0-15)
*        USES     ALL

CHANIN   SCALL    .SCIN            *GET CHANNEL BYTE
         JC       CHANIN           *LOOP UNTIL READY
         STA      COMMAND          *STORE IT
CHANIN1  SCALL    .SCIN            *GET SECOND BYTE
         JC       CHANIN1          *LOOP UNTIL READY
         CPI      0AH              *CARRIAGE RETURN?
         JZ       ONLY1            *ONLY ONE INPUT BYTE IF SO
         STA      COMMAND+1        *ELSE STORE IT
         SCALL    .CLRCO           *CLEAR THE BUFFER
         LDA      COMMAND          *GET FIRST BYTE
         CPI      '1'              *ONE?
         JNZ      CHANERR          *ERROR IF NOT
         LDA      COMMAND+1        *FETCH SECOND BYTE
         SBI      '0'              *LESS THAN ZERO?
         JC       CHANERR          *ERROR IF SO
         CPI      7                *MORE THAN 6?
         JNC      CHANERR          *ERROR IF SO
         ADI      09               *ADD TENS DIGIT OFFSET
         JMP      CHADONE          *ALL DONE
ONLY1    LDA      COMMAND          *GET BYTE
         SBI      '1'              *LESS THAN 1?
         JC       CHANERR          *ERROR IF SO
         CPI      0AH              *MORE THAN 9?
         JNC      CHANERR          *ERROR IF SO
CHADONE  PUSH     PSW              *SAVE CHANNEL NUMBER
         CALL     VALID            *CHANNEL ENABLED?
         JZ       DISAB            *ERROR IF Z CLEAR
         POP      PSW              *RESTORE CHANNEL NUMBER
         RET                       *AND RETURN

CHANERR  CALL     $TYPTX
         DB       0AH,0AH,07H,01BH
         DB       'FCHANNEL NUMBER INPUT ERROR - HIT RETURN'
         DB       ' TO CONTINUE',01BH,'q'+080H
ERRIN    SCALL    .SCIN            *GET INPUT
         JC       ERRIN            *LOOP UNTIL READY
         CPI      0AH              *RETURN?
         JNZ      ERRIN            *LOOP IF NOT
         POP      PSW              *CLEAR THE RETURN ADDRESS
```

Listing 1 continued on page 282

Introducing the fastest processor board available on the S100 bus today. . .

The Lightning One™

8086/8087/8089 CPU Board



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The *Lightning One*™ contains not one processor, but three processors all working in parallel. It uses the Intel 8086 as the main processor. The math capability is augmented with the 8087 math processor and the I/O handling capabilities are augmented with the 8089 dual channel I/O processor. The board complies with all IEEE-696 specifications.

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In addition to the *Lightning One,* Lomas Data Products has a full line of S100 bus support cards including: memory, disk controllers, and serial and parallel I/O.

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Circle 215 on inquiry card.

Listing 1 continued:

```
        RET                         *RETURN TO PROG THAT CALLED MENU

**********
* CHECK FOR VALID CHANNEL NUMBER
*       ENTRY   A=CHANNEL NUMBER
*       EXIT    'Z' CLEAR IF DISABLED
*               'Z' SET IF ENABLED
*       USES    ALL

VALID   CALL    GETCHAN             *GET CHANNEL ADDRESS BYTE
        MOV     A,M                 *LOAD THE CHARACTER
        CPI     '9'                 *ENABLED?
        RET                         *AND RETURN

DISAB   POP     PSW                 *CLEAR STACK
        CALL    $TYPTX
        DB      0AH,0AH,07H,01BH
        DB      'pTHAT CHANNEL IS DISABLED - HIT RETURN'
        DB      ' TO CONTINUE',01BH,'q'+080H
        JMP     ERRIN               *RETURN TO MAIN PROGRAM

*TITLE PRINT ROUTINE

TITLE   CALL    $TYPTX
        DB      01BH,045H+080H
        LXI     H,TITBUF            *LOAD BUFFER ADDRESS
TITLOOP MOV     A,M                 *FETCH BYTE
        CPI     080H                *END OF FILE?
        RZ                          *DONE IF SO
        CPI     'X'                 *X?
        JZ      REV                 *REVERSE VIDEO IF SO
        SCALL   .SCOUT              *ELSE OUTPUT THE CHARACTER
        JMP     TITNXT              *AND DO NEXT ONE
REV     CALL    $TYPTX
        DB      01BH,'p ',01BH,'q'+080H
TITNXT  INX     H                   *INCREMENT POINTER
        JMP     TITLOOP             *AND CONTINUE

TITBUF  EQU     *
    DB  0AH
    DB  0AH
```

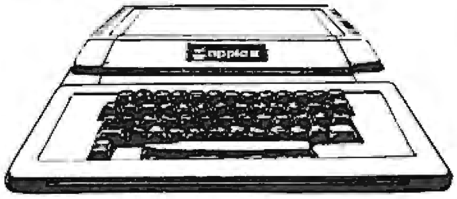
Listing 1 continued on page 284

Computer Exchange

National Sales Dept. of CUSTOM COMPUTER
P.O. Box 1380, Jacksonville, OR 97530

926

FOR YOUR APPLE II



Apple II +

48K	CALL	
Disk II W/3.3 DOS	CALL	

All 48K's are 1981 models with Apple RAM.

APPLE ///	CALL	
Apple Monitor 12" Green	$ 249	25%

HARDWARE

		SAVE
Disk II and 3.3 Controller	CALL	CALL
Disk II only	CALL	CALL

NEW Direct Substitute for Apple Drives
A2 Drives from Micro-Sci---Save $300 on a dual disk system. The A2 does not include DOS software.

		SAVE
Micro-Sci 5" Drives for Apple II		
A2, 143KK, 5" Drives	$ 395	18%
A2 Controller Card for A2 Drive	$ 85	15%
A 70, 286K, 5" Drive	$ 489	20%
A 40, 160K, 5" Drive	$ 369	18%
Controller Card for A70 or A40	$ 79	21%
MONITORS:		
★ ATI: 9" B&W	$ 119	30%
NEC 12" Color	$ 359	24%
12" Green	$ 169	22%
SANYO: 9" B&W	$ 159	32%
NEW 9" green	CALL	CALL
NEW 12" B&W	CALL	CALL
NEW 12" Green	CALL	CALL
13" Color	$ 399	38%
ZENITH 12" Green	$ 119	20%
DISKETTES, 5", box of 10:		
★ Apple	$ 44	21%
Maxell	$ 39	33%
Memorex	$ 25	45%
80 COLUMN VIDEO CARDS:		
Apple, Smarterm	$ 289	20%
Videx Videoterm	$ 249	18%
M&R Sup R Term	$ 319	19%
MISCELLANEOUS:		
Apple: Graphics Tablet	$ 695	13%
1 Yr Extended Warranty	$ 175	20%
IEEE-488 Card	$ 339	25%
CCS: Serial Interface Card	$ 139	22%
Parallel Interface Card	$ 99	20%
★ Hayes: Micromodem II	$ 299	26%
Smartmodem	$ 249	11%
Keyboard Company: Joystick II	$ 45	10%
Numeric Keypad	$ 119	21%
M&R: RF Modulator	$ 25	27%
SUP R FAN	$ 39	25%
★ Microsoft:		
Z80 Softcard	$ 299	33%
16K RAM Card	$ 159	20%
Mountain: CPS Multifunction Card	$ 209	13%
Clock/Calendar	$ 239	15%
Orange Micro Grappler	$ 129	21%
SSM AIO Serial/Para. Interface	$ 159	20%
★ ALS: Smarterm 80 Col Card	$ 289	20%
Z-Card (Z-80)	$ 209	22%
Addram 16K Card	$ 119	20%
Synergizer Package	$ 549	27%
PRINTERS:		
Apple, Silentypew/Interface	$ 329	17%

SOFTWARE

		SAVE
Apple:		
Apple Fortran	$ 149	25%
Apple Pilot	$ 119	27%
Apple Plot	$ 49	30%
Apple Writer	$ 59	21%
DOS 3.3	$ 49	20%
DOS Tool Kit	$ 59	22%
Dow Jones News & Quotes	$ 69	28%
Dow Jones Portfolio Eval.	$ 45	10%
Language/Pascal System	$ 379	25%
Microcourier	$ 189	24%
Broderbund Software	CALL	CALL
★ Central Point Software:		
Copy II Plus	$ 35	10%
Will copy most copy protected software for your backup in 45 seconds! NEW!		
Epson, MX 80 Graphics Dump	$ 7	30%
Hayden, Sargon II (chess)	$ 29	22%
Info. Unlim. Easywriter (PRO)	$ 199	13%
★ Insoft		
ALD System II	$ 110	10%
TransFORTH II	$ 110	10%
Accounting Software	$ 365	66%
A full professional quality integrated GL, A/R, A/P, Payroll package. Hotline support available. Send for free sample printouts. Requires Z80 and 16K RAM card		
Micro Pro		
Word Star	$ 239	36%
Super Sort	$ 129	36%
Mail Merger	$ 79	36%
Data Star	$ 189	36%
Spell Star	$ 159	36%
Microsoft (on disks)		
A L D S	$ 110	10%
BASIC Compiler	$ 299	25%
Cobol 80	$ 559	25%
Fortran 80	$ 149	25%
Olympic Decathlon	$ 24	24%
TASC Compiler	$ 159	22%
Typing Tutor II	$ 19	30%
Muse, Super Text II	$ 109	27%
Peachtree Software	CALL	CALL
Personal Software:		
Desktop Plan II	$ 159	21%
Visicalc 3.3	$ 159	25%
Visiplot	$ 129	28%
Visitrend Visiplot	$ 199	31%
Visidex	$ 159	30%
Visiterm	$ 109	27%
Visifile	$ 199	30%
Software Publishing:		
PFS Filing/Data Base	$ 69	28%
PFS Report	$ 69	28%
Stoneware, DB Master (new version)	$ 179	22%

Epson

		SAVE
MX80	$ 495	36%
MX80 F/T	$ 629	20%
MX100 F/T w/graphics	$ 779	22%
MX 80/100 Apple Interface and Cable	$ 95	15%
MX 80 Friction feed adapter	$ 59	22%
MX 80 Graftrax	$ 79	20%
MX 80/100 Atari Cable	$ 29	22%
MX 80/100 TRS 80 Cable	$ 29	22%

★ Corvus

		SAVE
5 Meg Hard Disk	$ 2995	21%
10 Meg Hard Disk	$ 4345	20%
20 Meg Hard Disk	$ 5245	20%
Omni-Net	CALL	CALL
Constellation	CALL	CALL
Mirror	CALL	CALL
Other Accessories	CALL	CALL

★ STAR INDICATES SPECIAL VALUE

INTERTEC DATA SYSTEMS® SUPERBRAIN

SAVE 60% $ 1995

★ **Superbrain 64K Double Density**

Superbrain 64K Quad Density $ 2895 28%

ATARI® 800 16K $759

ATARI® SAVE 30%

		SAVE
Atari 820 Printer	$ 249	17%
Atari 810 Disk Drive	$ 425	29%
Atari 410 Program Recorder	$ 59	34%
Atari 16K RAM Module	$ 83	27%
Atari 850 Interface	$ 149	32%
Atari/Epson Cable	$ 29	22%
Atari Software	CALL	CALL

HEWLETT PACKARD

		SAVE
HP-85A Microcomputer with built-in printer and monitor	$ 2395	27%
HP-125 New! Microcomputer 64K CPU/Terminal/Keyboard/Monitor	$ 3095	18%
HP-41CV New! 2.2K Memory Calculator	$ 245	25%
HP-41C Calculator	$ 185	26%
Memory module for HP41C	$ 25	25%

Call for other HP equipment, software and accessories!

Above prices for mail orders only. Our store showroom is 126 NE "F" St., Grants Pass, OR. Store prices, which include software service, differ from mail order prices. No mail order sales at store. CALL ORDER DESK.

ORDERING INFORMATION:

Minimum order $100. Money Orders, Cashier Checks or Bank Wire welcomed. Visa and MC orders add 3%. Personal or company checks are accepted (allow 20 days to clear). Add 3% for shipping, handling and insurance; UPS ground is standard. 6% total for UPS Blue or 10% total for foreign orders or US Parcel Post. Include your telephone number. No COD's. Prices are subject to change without notice. Order desk hours are 8 to 5 PST, 10 to 3 Saturdays.

REFERENCES:

Custom Computer has been an Apple dealer since 1978. Our bank reference is First Interstate Bank (503) 776-5620. We belong to the Chamber of Commerce. (503) 772-6293.

Technical Hotline
(503) 772-3803
(CUSTOMERS ONLY-PLEASE HAVE INVOICE # OR PACKING SLIP #)

Oregon Order Desk
(503) 772-3803

VISA master charge

apple computer
Sales and Service

We are an authorized dealer and repair center and will repair all Apple equipment regardless of where you purchased it, in or out of warranty. Normally our turn-around time on repairs is 24 hours. Call before sending equipment.

Repair Department
(503) 772-4401

NO SALES TAX

For specific software not listed, CALL

TOLL FREE
NATIONAL ORDER DESK
(800) 547-1289

Circle 90 on inquiry card.

Listing 1 continued:

```
DB   0AH
DB   '                  '
DB   'XXXX          XXXX             XXXXXXXXXX           XXXXXXXXXXX',0AH
DB   '                  '
DB   'XXXX          XXXX          XXXXXXXXXXXX            XXXXXXXXXXXXX',0AH
DB   '                  '
DB   'XXXX          XXXX        XXXX                      XXXX        XXXX',0AH
DB   '                  '
DB   'XXXX          XXXX        XXXX                      XXXX        XXXX',0AH
DB   '                  '
DB   'XXXXXXXXXXXXXXXX            XXXX                    XXXXXXXXXXXXX',0AH
DB   '                  '
DB   'XXXXXXXXXXXXXXXX            XXXX                    XXXXXXXXXX',0AH
DB   '                  '
DB   'XXXX          XXXX        XXXX                      XXXX',0AH
DB   '                  '
DB   'XXXX          XXXX        XXXX                      XXXX',0AH
DB   '                  '
DB   'XXXX          XXXX          XXXXXXXXXXXX            XXXX',0AH
DB   '                  '
DB   'XXXX          XXXX             XXXXXXXXXX           XXXX',0AH
DB   0AH
DB   0AH
DB   0AH
DB   '                       '
DB   '                  BSR HOME CONTROL PACKAGE',0AH
DB   0AH
```

Listing 1 continued on page 286

DEALERS: By now you know that it takes . . . . .

SOFTWARE
TO SELL
COMPUTERS

and International Micro Systems can provide you with the largest selection of quality business applications ever developed for the microcomputer industry.

If you are just looking for a G.L., A/P, and Payroll, you can find them in a dozen ads in this magazine. But thers's a much bigger market for micros out there than that. Where can you find a fully interfaced Wholesale/Retail Distribution System? How about Manufacturing Inventory Control including Production Scheduling & Control. See that one anywhere else? Maybe your market is Medical/Dental and IMS has the full systems there too. You can't sell computers without software and IMS has the finest selection of software available for you. Each system has been developed by the IMS professional staff and we support what we sell.

But thats not all. International Micro Systems has the strongest dealer marketing plan in the industry. With our . . . . .

$295 Dealer Demo System.

we put all the software shown below in your office or store ready to demo to your prospects and we include the promotional material and our unique video sales presentation to help you move systems. Give us a call or drop us a card and let us show you what selling business systems should be all about.

Financial Systems
- GL, A/P, A/R
- Payroll
- Cash Receipts/Disb.
- Job Costing
- Mailing List Mgmt.

Medical/Dental
- Office Scheduler
- Patient Billing & A/R
- Insurance Forms

Governmental/Educational
- Student Record Keeping and Scheduling
- Fund Accounting

Wholesale Distribution System
- Purchasing & Receiving
- Inventory Control
- Invoicing & Receivables
- Salesman Comm. Reporting
- Backorder Management

Manufacturing Inventory Control
- Finished Goods Inventory Mgmt.
- Parts Inventory Mgmt.
- Parts Purchasing & Receiving
- Bill of Material
- Production Scheduling

INTERNATIONAL MICRO SYSTEMS

For details on our Demo Special, contact us at:
6445 Metcalf, Shawnee Mission, KS 66202
Phone: (913) 677-1137

Circle 178 on inquiry card.

Listing 1 continued:

```
     DB   0AH
     DB   '              '
     DB   '
     DB   '              '
     DB   '
     DB   '       '      '
     DB   '

     DB   'Initializing Remote Control Units.....'
     DB   080H


*****************************************************************
*                      DEFINE COMMAND CODES                     *
*                                                               *
*     CODES ARE SET UP SO THAT THE FIRST FIVE MOST SIGNIFICANT  *
*   BITS REPRESENT THE BINARY CODE FOR THAT CHANNEL.  REMEMBER  *
*   THAT TO SEND A COMMAND FIRST SEND A LOGIC ONE, THEN THE     *
*   FIVE BIT CHANNEL CODE, THE FIVE BIT CHANNEL CODE INVERTED,  *
*   AND LASTLY, THE END OF MESSAGE SIGNAL FOR A TOTAL OF        *
*   TWELVE BITS.                                                *
*****************************************************************
* CHANNEL NUMBER DEFINITIONS
*

ONE      DB       01100000B
TWO      DB       11100000B
THREE    DB       00100000B
FOUR     DB       10100000B
FIVE     DB       00010000B
SIX      DB       10010000B
SEVEN    DB       01010000B
EIGHT    DB       11010000B
NINE     DB       01110000B
TEN      DB       11110000B
ELEVEN   DB       00110000B
TWELVE   DB       10110000B
THIRT    DB       00000000B
FOURT    DB       10000000B
FIFT     DB       01000000B
SIXT     DB       11000000B

****************
* FUNCTION CODES

ALLOFF   DB       00001000B
ALLON    DB       00011000B
ON       DB       00101000B
OFF      DB       00111000B
DIM      DB       01001000B
BRIGHT   DB       01011000B

*****************
* STORAGE REGISTERS

COMMAND DS        2
```

Listing 1 continued on page 288

Listing 1 continued:

```
DEFLT    DB      'SY1ABS''
UNITNAM  DB      'SY1:UNITDEF.DAT',0
UNITBUF  DS      1280
UNITLOC  DS      32


         END     BEGIN

00981 Statements Assembled
8966 Bytes Free
 No Errors Detected
```

SAMPLE PROGRAM RUN

```
>RUN HCP


   Initializing Remote Control Units........


                         REMOTE UNIT STATUS

UNIT                     UNIT NAME                    LEVEL  STATUS
----------------------------------------------------------------------
 1          Living Room Ceiling Lamp                    9      OFF
 2          Kitchen Ceiling Light                       9      OFF
 3          Back Yard Floodlights                       1      OFF
 4          Bedroom Chandelier                          4      ON
 5          Computer Desk Swag Lamp                     9      ON
```

Listing 1 continued on page 290

BETA COMPUTER DEVICES

AVAILABLE NOW ... SYSTEM 2800 FROM SYSTEMS GROUP

FEATURES

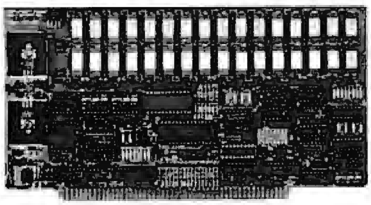
Model 2812/14/24

- IEEE S-100 Bus Compatible Systems, Z80A Based
- Two 8-Inch Drives: Single or Double Sided, Double Density Floppy Disk Drives or 10MB Winchester Hard Disk Drive
- 20MB Winchester and Tape Backup
- 8-Slot Shielded and Terminated Motherboard
- System Software Selection includes CP/M*, MP/M* or OASIS**
- Single-User or Multi-User Systems, Expandable to 6 Users
- Table Top or Rack Mountable
- Two Switched AC Outlets on Rear Panel
- One Year Warranty on Entire System

2812 CP/M, 2 Single Sided Floppies	$3775.00
2814 CP/M, 2 Double Sided Floppies	4425.00
2819 CP/M, 1 10 MB Winchester & 1 Double Sided Floppy	6675.00
2824 MP/M, 2 Double Sided Floppies	5235.00
2829 MP/M, 1 10 MB Winchester & 1 Doubled Sided Floppy	7500.00

Model 2819/29

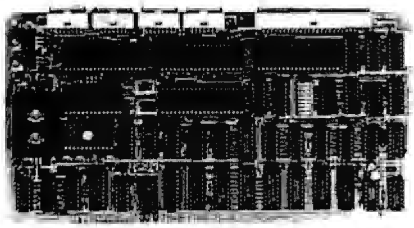
S-100 PRODUCTS



QUALITY RAM FROM SYSTEMS GROUP

- Z-80 4MHZ operation with no wait states
- IEEE compatible timing - 200 NS 4116's
- Factory assembled, tested & burned in

DMB6400 64K (Bank Select, shown)	$740.00
DM6400 64K	540.00
DM4800 48K	510.00
DM3200 32K	475.00



CONFIGURE A COMPLETE S-100 SYSTEM WITH 2nd GENERATION* PRODUCTS FROM SYSTEMS GROUP.

- CPC 2810 (shown) Z-80A processor board (4MHZ) with 4 serial & 2 parallel ports $369.00
- CPC2813 - same as CPC2810 but 2 serial ports only $345.00
- FDC2801/8 - 8" floppy disk controller board, up to 4 single/double sided drives, single or double density $349.00
- INO-2804 - 4 channel serial I/O 329.00
- CRA-100 - Cromix* adaptor board.. $55.00

CALL US FOR OUR MOST CURRENT PRICES!

*2nd Generation is a trademark of Measurement Systems and Controls, Inc. Cromix is a trademark of Cromemco, Inc. CP/M and MP/M are trademarks of Digital Research. OASIS is a trademark of Phase One Systems.

PAPER TIGER PRINTERS

IDS 460G 9x9 Dot Matrix Printer	$890.00
IDS 560G Wide Carriage Printer	1099.00

TERMINALS

ADDS Viewpoint	$569.00
TeleVideo 910	579.00
TeleVideo 912C	679.00
TeleVideo 920C	729.00
TeleVideo 950	929.00

8" DISK DRIVES

Shugart 801R	$399.00
NEC FD1160 (double sided)	525.00

DYNAMIC RAMS

4116 (200ns) .... set of 8	$24.00
4164 (64K x 1)	$18.00

wabash

8" or 5¼" flexible diskettes certified 100% error free with manufacturer's 5-year limited warranty on all 8" media. Soft-sectored in boxes of 10. 5¼" available in 10-sector.

(Add $3.00 for plastic library cases)

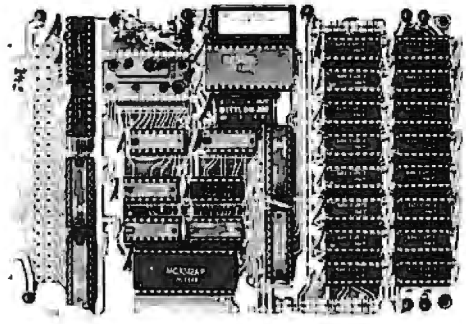
8" single sided, single density	$27.50
8" single sided, double density	35.50
8" double sided, double density	45.50
5¼" single sided, single density	27.50
5¼" single sided, double density	29.50

TERMS: Minimum order $15.00. Minimum shipping and handling $3.00. Calif. residents add 6% sales tax. Cash, checks, Mastercard, Visa and purchase orders from qualified firms are accepted. (Please allow two weeks for personal checks to clear before shipment.) Product availability and pricing subject to change without notice.

INTERNATIONAL ORDERS: *Add 15% to purchase price for all orders. Minimum shipping charge is $20.00. Orders with insufficient funds will be delayed. Excess funds will be returned with your order. All prices are U.S. only.*

6502 PRODUCTS

6502DM



BETA 32K BYTE EXPANDABLE RAM FOR 6502 AND 6800 SYSTEMS

AIM 65 KIM SYM PET S44-BUS

- Plug compatible with the AIM-65/SYM expansion connector by using a right angle connector (supplied).
- Memory board edge connector plugs into the 6800 S44 bus.
- Connects to PET using an adaptor cable.
- Uses +5V only, supplied from the host computer.
- Full documentation. Assembled and tested boards are guaranteed for one full year. Purchase price is fully refundable if board is returned undamaged within 14 days.

Assembled with 32K RAM	$349.00
& Tested with 16K RAM	329.00
Bare board, manual & 6 hard-to-get parts.	99.00
PET interface kit. Connects the 32K RAM board to a 4K or 8K PET	$ 69.00

AIM Professional Enclosure...$175.00

BETA COMPUTER DEVICES
1230 W. COLLINS AVE.
ORANGE, CA 92668
(714) 633-7280

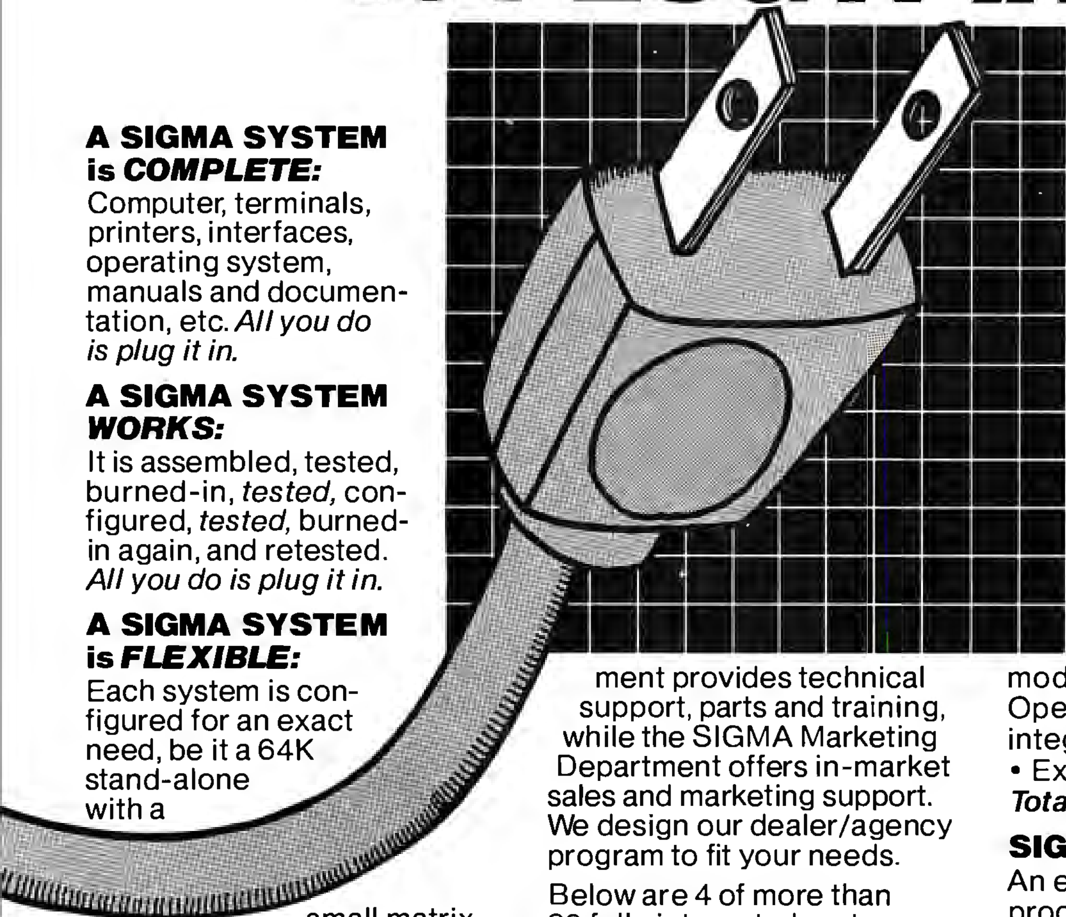
Listing 1 continued:

```
Hit Return For Command Menu @


                              MANUAL CONTROL MENU


Commands Available:

          0.......... Exit Program
          1.......... All Units Off
          2.......... All Units On
          3.......... Single Unit Off
          4.......... Single Unit On
          5.......... Single Unit Brightness Adjust
          6.......... Return To Status Display


Enter Number of Choice 5

                              CHANNEL SELECTION MENU

          1.......... Living Room Ceiling Lamp
          2.......... Kitchen Ceiling Light
          3.......... Back Yard Floodlight
          4.......... Bedroom Chandelier
          5.......... Computer Desk Swag Lamp


Number of unit on which to adjust brightness? 5

Brightness Level (0=Dim, 9=Bright)? 5







                              REMOTE UNIT STATUS

UNIT                         UNIT NAME                        LEVEL   STATUS
--------------------------------------------------------------------------------
 1             Living Room Ceiling Lamp                         9       OFF
 2             Kitchen Ceiling Light                            9       OFF
 3             Back Yard Floodlights                            1       OFF
 4             Bedroom Chandelier                               4       ON
 5             Computer Desk Swag Lamp                          5       ON

Hit Return For Command Menu @
```

Listing 1 continued on page 292

SYSTEMS FROM $3,775

ALL YOU DO IS PLUG IT IN!



A SIGMA SYSTEM is *COMPLETE:*
Computer, terminals, printers, interfaces, operating system, manuals and documentation, etc. *All you do is plug it in.*

A SIGMA SYSTEM *WORKS:*
It is assembled, tested, burned-in, *tested,* configured, *tested,* burned-in again, and retested. *All you do is plug it in.*

A SIGMA SYSTEM is *FLEXIBLE:*
Each system is configured for an exact need, be it a 64K stand-alone with a small matrix printer or a 512K multi-user, multi-processor with several 600LPM line printers—or anything in between. *All you do is plug it in.*

A SIGMA SYSTEM is *EXPANDABLE:*
Each system is designed to grow with your customer's needs. Usually only an additional board is required for expansion. *All you do is plug it in.*

A SIGMA SYSTEM is *SUPPORTED:*
SIGMA's Engineering Department provides technical support, parts and training, while the SIGMA Marketing Department offers in-market sales and marketing support. We design our dealer/agency program to fit your needs.

Below are 4 of more than 80 fully integrated systems:

SIGMA SYSTEM I
A single user stand-alone system: • 64K RAM • 2 x 5¼" QD Floppy Drives (700KB) • 12" CRT with full ASCII Keyboard • Printer-100 cps (data processing) and 50 cps (letter quality) plus graphics capability • CP/M Operating System • Fully integrated and tested • Expandable
Total Price: $3,775

SIGMA SYSTEM II
A multi-user (2) system: • 64K RAM per user • 5¼" Floppy Drive (500KB) • 5MB Hard Disk Drive • 2 CRT Terminals with detachable keyboards • High speed 180 cps printer • MP/M Operating System • Fully integrated and tested • Expandable
Total Price: $8,675

SIGMA SYSTEM III
A four user (4) system: • 64K RAM per user • 2 x 8" Floppy Disk Drives (1.2MB) • 11MB Hard Disk Drive • 4 CRT's with detachable keyboards • Printer—200 cps (data mode), 60 cps (letter quality mode) plus graphics • MP/M Operating System • Fully integrated and tested • Expandable
Total Price: $14,459

SIGMA SYSTEM IV
An eight user (8) multi-processing system: • 512K RAM • 8" Floppy Disk Drive (1.2MB) • 18MB Hard Disk Drive • 8 CRT's with detachable keyboards • Printer—180 cps data printer • Printer—55 cps letter quality • CP/M compatible multi-user system • Data Base Management System • Fully integrated and tested • Expandable up to 16 users
Total Price: $32,997

(The above systems include charge for integration. If integration is not desired, please inquire about additional discounts.)

U.S. Domestic/Canada
Sigma Digital Systems, Inc.
609 N. Scottsdale Road
Scottsdale, Arizona 85257
Telephone: (602) 941-4087

Σ Sigma
SINTEL *COMPANIES*

International
Sigma International Trading Corp.
P.O. Box 1118
Scottsdale, Arizona 85252
Telephone: (602) 994-3435
Telex: 165-745 SIGMA

DEALERSHIPS/AGENCIES AVAILABLE IN SELECTED AREAS
"PLUG INTO SIGMA'S DISTRIBUTION NETWORK"

Circle 335 on inquiry card.

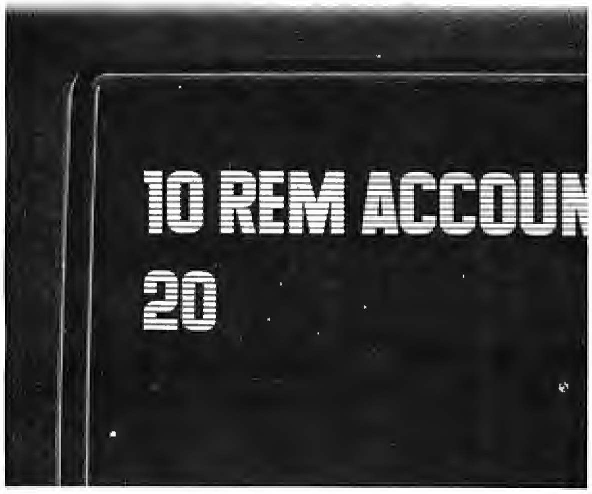
Listing 1 continued:

```
                         MANUAL CONTROL MENU


Commands Available:

        0........... Exit Program
        1........... All Units Off
        2........... All Units On
        3........... Single Unit Off
        4........... Single Unit On
        5........... Single Unit Brightness Adjust
        6........... Return To Status Display


Enter Number of Choice 0
```

Listing 2: *An example of the contents of UNITDEF.DAT. This file controls the status of the remote-control units and defines the remote names for the main program menu-routines. Note that all of the 16 channels must be defined even though 11 are disabled by setting the second and third columns to 99.*

```
09 1Living Room Ceiling Lamp
09 2Kitchen Ceiling Light
01 3Back Yard Floodlights
14 4Bedroom Chandelier
19 5Computer Desk Swag Lamp
0196
0997
0998
0999
0990
0991
0992
0993
0994
0995
0996
```

BOY, IS THIS COSTING YOU.



It's really quite basic: time is money.

And BASIC takes a lot more time and costs a lot more money than it should every time you write a new business software package.

Especially when you could speed things up with dBASE II.

dBASE II is a complete applications development package.

Users tell us they've cut the amount of code they write by up to 80% with dBASE II.

Because dBASE II is the high performance relational database management system for micros.

Database and file handling operations are done automatically, so you don't get involved with sets, lists, pointers, or even opening and closing of files.

Instead, you write your code in concepts.

And solve your customers' problems faster and for a lot less than with BASIC (or FORTRAN, COBOL or PL/I).

dBASE II uses English-like commands.

dBASE II uses a structured language to put you in full control of your data handling operations.

It has screen handling facilities for setting up input and output forms.

It has a built-in query facility, including multi-key and sub-field searches, so you can DISPLAY some or all of the data for any conditions you want to apply.

You can UPDATE, MODIFY and REPLACE entire databases or individual characters.

CREATE new databases in minutes, or JOIN databases that already exist.

APPEND new data almost instantly, whether the file has 10 records or tens of thousands.

SORT the data on as many keys as you want. Or INDEX it instead, then FIND whatever you're looking for in seconds, even using floppies.

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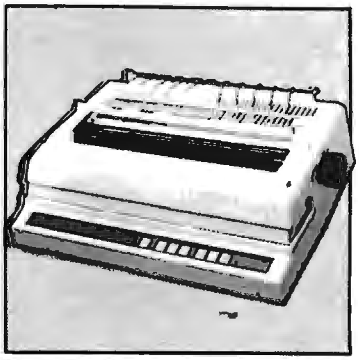

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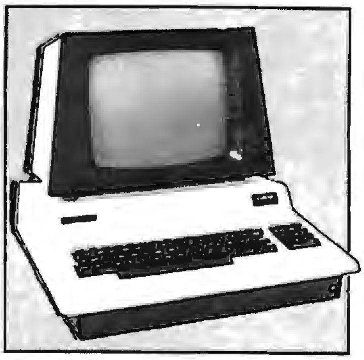

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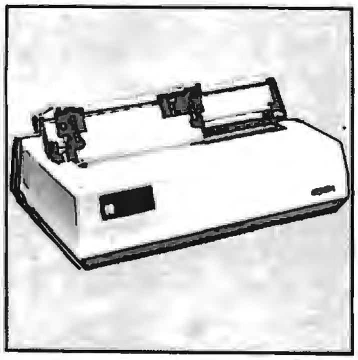

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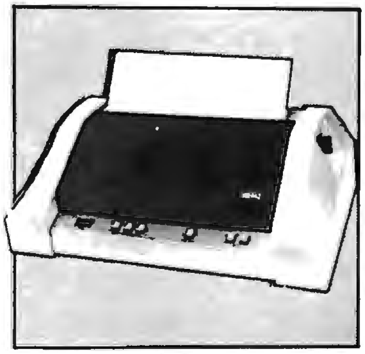

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BYTELINES

News and Speculation About Personal Computing

Conducted by Sol Libes

Random Rumors: It's in the air that Intel is about to announce an IC (integrated circuit) designed specifically for database management (DBM) computers. This IC should make possible the construction of a relational DBM machine that works with a host processor, off-loading DBM functions from the host. Using hardware specifically designed for DBM applications should greatly improve DBM system performance over the current approach of using an existing general-purpose computer system for DBM applications.

Speculation has it that the chip itself will be a processor with an instruction set designed exclusively for database handling. As such, it could handle compression and decompression algorithms, among other tasks. . . . Zilog is rumored to be working with Seeq Technology on a microprocessor having on-board EPROM (erasable programmable read-only memory) for learn-and-remember *self-programming* ability. . . . IBM is expected to introduce an option for its personal computer for bisynchronous communications with 3270-compatible equipment, 3276 SDLC/SNA compatibility (fall of 1982), and X.25 communications support (spring of 1983).

Apple Drops Bomb On Mail Order: In a surprise move, Apple Computer, Inc. has unilaterally decided to prohibit its dealers from selling Apple computer products through mail or phone order sales. It is Apple's feeling that "customers purchasing [Apple products] can be properly served only if they have the benefit of pre- and post-sale education, orientation, and support, specifically including in-person contact with the selling dealer." Dealers are required to sign a "modification" to their dealer sales agreement or their authorized dealership will be terminated. It is not clear just what previously educated customers, especially those not located close to an Apple dealer, are to do.

More rumors are surfacing regarding Apple's new computer offerings. The latest is that we'll see two new Apples: a low-cost system ($500 and up) to use the Motorola 6809 microprocessor and a high-cost, business-oriented system that will use the Motorola 68000. The business-oriented system will be capable of addressing up to 760 K bytes of memory, will probably come with a hard disk, and will be compatible with the Xerox Star local networking system.

Apple has introduced a 5-megabyte, 5¼-inch Winchester Technology disk drive for the Apple III computer. Called the Profile Mass-Storage System, the unit is comprised of an intelligent controller, the drive itself, a power supply, an interface card, and driver software.

Pearcom, a European company, has started to market its Pear II computer (an Apple II work-alike). According to the grapevine, Apple is considering legal action. . . . Sears's computer stores, already carrying the Atari and Vector Graphic computers, are said to be negotiating with Apple.

IBM Coming on Strong: People who've been around the microcomputer industry awhile were surprised when IBM began shipping its new Personal Computer more than a month before the promised October delivery date and less than a month after announcing it. This is unheard of in the personal computer industry. Currently, distribution of the IBM Personal Computer is limited to ComputerLand shops, the few Sears computer stores, and IBM's sales force. ComputerLand and Sears appear to be handling single and limited-quantity sales, while the IBM salespeople seem to be pursuing large-quantity orders.

When IBM announced its Personal Computer, it reportedly received orders for 40,000 systems—that's worth about $160 million. Sales of more than 150,000 systems are projected for 1982.

Early reports indicate that the Personal Computer has affected sales of other systems. Carrying the IBM computer apparently requires a large financial commitment from the stores. This, coupled with the current tight credit situation, is forcing the stores to cut other product lines to make room for IBM.

Several ComputerLand stores have already reported sales of the IBM computer equal to those of Apple. (Incidentally, ComputerLand accounts for 14 percent of Apple's retail sales.)

IBM recently made another unprecedented move when it began offering its 8-inch Winchester disk drive as a separate OEM item to other manufacturers.

Tandy Happenings: If you'd bought 1000 shares of Tandy stock in 1967 at $15 a share, today it would be worth $2,350,000. . . . Tandy owns 91 percent of its outlets. . . . Tandy employees own about 25 percent of the company. . . . Radio Shack has a mailing list of 25 million. . . . Radio Shack manufactures more than half the products it sells. . . . Earnings have doubled since 1978.

Tandy is pressing its copyright infringement suit against Personal Micro Computer Inc., of Mountain View, California, manufacturer of the PMC-80. A federal court has already dismissed PMC's claim that federal copyright laws do not pertain to ROM (read-only memory) based computer programs. Tandy is suing to stop sales of the PMC-80 and to obtain compensation for damages.

Tandy has also introduced Arcnet, a local network system to link up with 255 Model II computers. Arcnet is based on Datapoint's Attached Resource Computer (ARC). Arcnet operates at 21.5 megabytes per second and is reportedly similar to Ethernet.

Radio Shack and Interstate Bank of California have begun a pilot program for a home banking system. TRS-80 Videotex terminals and color computers are

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How Much Faster Are the 16-Bit Micros?: The introduction of several microcomputers based on the Intel 8086/8088 microprocessor has given computer users the chance to compare execution speeds of 16-bit and 8-bit micros.

Several vendors offer identical software—namely the CP/M operating system and Microsoft BASIC—for these machines. It's now possible to run identical BASIC programs and compare execution times. Tests have already shown that there is no significant difference between a microcomputer with an 8086 running at its standard speed (5 MHz) and one with a Z80 running at its standard speed (4 MHz). What must be considered is that CP/M-86 has many new features which may slow it down (compared with CP/M-80). Also, the 8086 version of Microsoft BASIC currently available is a translation of an 8080 version, one with minimal optimization for the 8086. I hope Microsoft will rework its BASIC interpreter to take advantage of the 8086's more powerful architecture. Presently, though, if you expect to get a significant improvement in execution time by moving up to a 16-bit micro, you may be sorely disappointed.

CDC Introduces Personal Computer: Amidst all the publicity given IBM and Xerox personal computers, Control Data Corporation, IBM's leading competitor, has introduced its own personal computer. The CDC-110 uses a Z80, has 64 K bytes of RAM (random-access read/write memory) and a 1.2 megabyte 8-inch floppy-disk system. Prices start at just under $5000. The system can be used as a work station with a timesharing or Plato system.

Pascal Standard Adopted: The IEEE has adopted a standard for the Pascal language, designated IEEE Standard 770-981. This culminates a 2½-year effort by a joint committee that included IBM, DEC, Honeywell, Burroughs, Intel, Motorola, Microsoft, Softech, and others, along with several universities. The base language has been standardized, but much remains undone in standardizing the extensions to Pascal. Standardization should pave the way toward making Pascal a more portable language. Significant differences currently exist among the various versions.

Random News Bits: OKI Electric is the first company to ship samples of a 256 K-bit RAM IC. Production quantities are expected late this year. . . . Intel has announced development of a 4-megabit bubble memory IC. Sampling will start late this year. . . . Shipments of computer equipment in 1981 have totaled about $31.5 billion, a 17.6 percent increase over 1980. . . . The NCC show, to be held in Houston in June, is expected to draw over 600 exhibitors. . . . Shugart Associates recently shipped its one millionth 8-inch floppy-disk drive. . . . Zilog and AMD have signed an agreement whereby AMD will make and sell a 32-bit microprocessor being developed by Zilog. . . . Zilog has introduced the Z80L, a low-power version of the Z80. The Z80L draws only .15 mA instead of 100-150 mA for the standard Z80. . . . Researchers at MIT are building robotic skin—thick sheets of rubber with wire lines imbedded in them to conduct a "sense" of touch.

Predictions, Predictions: Last January I made my customary predictions—eight in all—for 1981. How did I do? Let's check the results:

1. *The S-100 will become the de facto standard for bus interfacing, with the number of manufacturers supporting the bus to increase to more than 40 (and to include IBM).*

Score a *partially correct* on this. Close to 50 firms now make the S-100, and a like number supply peripheral boards. However, IBM chose to go with a new bus of its own design.

2. *Hardware will become more sophisticated and less expensive.*

Score a *correct* on this one. Personal computers have acquired features of their larger, more-expensive predecessors.

3. *The man/machine interface will be improved to accommodate the many users who have little or no knowledge of computers.*

Score a *correct* on this one too. New software packages (e.g., "The Last One") make software development for nonprogrammers possible (although I think we are far from the "last one"). The increasing use of "menu-driven" software (even menu enhancements for CP/M) has also made computers more accommodating.

4. *Cheap mass storage for personal computers will finally arrive via video cassette and optical-disk memories.*

Although two companies have introduced video-cassette interfaces, and others have demonstrated optical-disk interfaces, acceptance has been cool. To make this hardware really useful, we need complementary software operating systems.

Let's score a *correct* on this one.

5. *Higher-quality displays using either liquid-crystal or semiconductor technology will be introduced.*

Epson did show prototypes of its 256-character/graphics liquid-crystal display, and a few semiconductor displays (typically one or two lines) were introduced, but a display suitable for general terminal use has not yet been shown. Therefore, score *partially correct* on this one.

6. *Personal computers will include self-testing capabilities and redundant circuits to improve reliability.*

Score a *correct* on this, as companies include self-test routines in their boot ROM (e.g., the new IBM and Osborne personal computers). Also, several companies have introduced an extra parity bit in RAM and provided circuitry to periodically test memory and correct faults.

7. *Expect BASIC to continue as the dominant language. . . . Natural programming languages and automatic programming still appear to be many years away.*

Score another *correct*.

8. *Operating systems such as Unix, CP/M, MP/M, and more sophisticated systems will increase in popularity, and many manufacturers will design special hardware to support these operating systems.*

Check *correct* here also.

All predictions considered, I was about 90 percent accurate. Not bad!

Predictions for 1982: 1. *Who will dominate the microcomputer market?* I expect 1982 will see continued

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strong growth in the personal computing industry. I also foresee a year of great turmoil as competition heats up among three factions. They are traditional personal computing suppliers (e.g., Tandy, Apple, Heath, Commodore, and Atari), the biggies who have introduced personal computers (IBM, DEC, Xerox, etc.), and Japanese suppliers.

Eight-bit systems will probably retain their dominance in single-user systems, with CP/M reigning supreme among disk operating systems. I predict Apple, Tandy, and IBM will dominate this area.

However, absolute chaos will abound in local networking, as virtually every personal computer maker will have a separate system. Xerox should finally start shipping Ethernet systems, and nearly all personal computer suppliers can be expected to supply Ethernet interfaces for their personal computers. Because of this, Ethernet (if its price is not a deterrent) stands a chance of becoming a local-networking standard. The Corvus Omninet system looks promising too.

Chaos is also expected in the multiuser personal computer area as the new 16-bit microprocessors fight it out. Although the 8086-based systems seem to have an early lead, the 68000-based systems may become dominant. I don't expect Digital Research to achieve the same success with its multiuser MP/M DOS that it has enjoyed with single-user CP/M.

2. *Some hardware predictions.* As memory prices drop, RAM ICs get larger and application software demands more memory. Sixty-four K bytes should become the standard memory configuration for 8-bit, single-user, personal computers. . . . A new recording technology for floppy disks will increase storage for 5¼-inch disks to as much as 5 megabytes. . . . I expect more compact, portable personal computers (similar to the Osborne), with prices possibly dropping as low as $1000 (disk drive, modem, and printer interfaces included). . . . DEC should finally introduce its personal computer, and I imagine it will be based on the LSI-11 architecture. . . . I expect both Xerox and IBM to market new personal computers with costs even lower than their current units. In fact, I anticipate the greatest competition will occur at the lower end of the personal computer market. . . . I foresee at least one S-100 supplier announcing a CPU that employs the Intel 432 32-bit processor. However, it will probably be 1983 before we see production units and software. . . . A low-cost, optically based memory system capable of storing a billion bytes may be introduced by year's end (sometime during 1983 is more likely). . . . Also by year's end or in 1983, we may see typewriters from IBM, Xerox, and Matsushita that feature voice input.

3. *Some software predictions.* BASIC will continue to reign supreme among high-level languages. I expect several software suppliers to furnish new versions of BASIC interpreters. These will eliminate line-number requirements and will use labels to allow better structuring of the BASIC programs. . . . I expect someone to introduce a Pascal interpreter. . . . Disk-operating-systems designers should develop user interfaces that are oriented more toward users than programmers. Thus, DOS systems will all become menu driven, with elaborate prompts for the user. Utilities will increasingly become integral parts of the DOS. . . . Taking advantage of larger memory and storage capabilities, sophisticated business software packages will proliferate.

Commodore Happenings: Commodore is starting to promote Comal, a new structured language, as a substitute for PET BASIC. Developed in Denmark, Comal is supposedly easier to learn than PET BASIC; it uses Pascal-like structures. Also rumored is a version of the PET with Comal resident in ROM that will soon join the Commodore line. Commodore plans a sales promotion campaign for the new version and has signed William Shatner (*Star Trek's* Captain Kirk) to appear in its commercials.

MAIL: I receive a large number of letters each month as a result of this column. If you write to me and wish a response, please include a self-addressed, stamped envelope.

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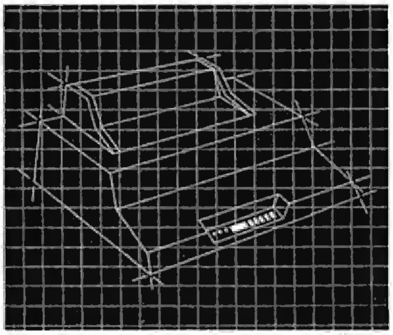

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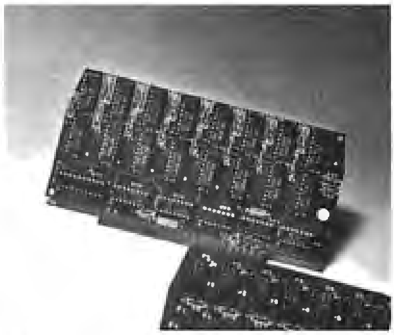

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FLS and MAIL LIST 2.2 are available as a combined package for $59.95.

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SORTIT is a general purpose sorting program written in 8080 assembly language. This program will sort sequential data files generated by NORTH STAR BASIC. Primary and optional secondary keys may be numeric or one to nine character strings. SORTIT is easily used with files generated by DYNACOMP's MAIL LIST program and is very versatile in its capabilities for all other BASIC data file sorting.

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This software package contains a menu-driven collection of programs for facilitating efficient two-way communications through a full duplex modem (required for use). In one mode of operation you may connect to a data service (e.g., The SOURCE or MicroNet) and quickly load data such as stock quotations onto your diskette for later viewing. This greatly reduces "connect time" and thus the service charge. You may also record the complete contents of a communications session. Additionally, programs written in BASIC, FORTRAN, etc. may be built off-line using the support text editor and later "uploaded" to another computer, making the Atari a *very* smart terminal. Even Atari BASIC programs may be uploaded. Further, a command file may be built off-line and used later as controlling input for a time-share system. That is, you can set up your sequence of time-share commands and programs, and the Atari will transmit them as needed; batch processing. All this adds up to saving both connect time and your time.

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DFILE (Atari and North Star diskettes only) — Price: $19.95
This handy program allows North Star and Atari disk users to maintain a specialized data base of all files and programs in the stack of disks which invariably accumulates. DFILE is easy to set up and use. It will organize your disks to provide efficient locating of the desired file or program.

FINDIT (North Star only) — Price: $19.95
This is a three-in-one program which maintains information accessible by keywords of three types: Personal (eg: last name), Commercial (eg: plumbers) and Reference (eg: magazine articles, record albums, etc). In addition to keyword searches, there are birthday, anniversary and appointment searches for the personal records and appointment searches for the commercial records. Reference records are accessed by a single keyword or by cross-referencing two or three keywords.

SHOPPING LIST (Atari only) — Price: $12.95 Cassette/$16.95 Diskette
SHOPPING LIST stores information on items you purchase at the supermarket. Before going shopping, it will remind you of all the things you might need, and then display (or optionally print) your shopping list and the total cost. Adding, deleting, changing and storing data is very easy. Runs with 16K.

TAX OPTIMIZER (North Star only) — Price: $59.95 Diskette
The TAX OPTIMIZER is an easy-to-use, menu oriented software package which provides a convenient means for analyzing various income tax strategies. The program is designed to provide a quick and easy data entry. Income tax is computed by all tax methods (regular, income averaging, maximum and alternate minimum tax). The user may immediately observe the tax effect of critical financial decisions. TAX OPTIMIZER has been thoroughly field tested in CPA offices and comes complete with the current tax tables in its data files. TAX OPTIMIZER is tax deductible!

EDUCATION

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Let HODGE PODGE be your child's babysitter. Pressing any key on your Apple will result in a different and intriguing "happening" related to the letter or number of the chosen key. The program's graphics, color and sound are a delight for children from ages 1½ to 9. HODGE PODGE is a non-intimidating teaching device which brings a new dimension to the use of computers in education.

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MISCELLANEOUS

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STATISTICS and ENGINEERING

DIGITAL FILTER (Available for all computers) — Price: $39.95 Cassette/$43.95 Diskette
DIGITAL FILTER is a comprehensive data processing program which permits the user to design his own filter function or choose from a menu of filter forms. The filter forms are subsequently converted into non-recursive convolution coefficients which permit rapid data processing. In the explicit design mode the shape of the frequency transfer function is specified by directly entering points along the desired filter curve. In the menu mode, ideal low pass, high pass and bandpass filters may be approximated to varying degrees according to the number of points used in the calculation. These filters may optionally also be smoothed with a Hanning function. In addition, multi-stage Butterworth filters may be selected. Features of DIGITAL FILTER include plotting of the data before and after filtering, as well as display of the chosen filter functions. Also included are convenient datastorage, retrieval and editing procedures.

DATA SMOOTHER (Not available for Atari) — Price: $19.95 Cassette/$23.95 Diskette
This special data smoothing program may be used to rapidly derive useful information from noisy business and engineering data which are equally spaced. The software features choice in degree and range of fit, as well as smoothed first and second derivative calculation. Also included is automatic plotting of the input data and smoothed results.

FOURIER ANALYZER (Available for all computers) — Price: $19.95 Cassette/$23.95 Diskette
Use this program to examine the frequency spectra of limited duration signals. The program features automatic scaling and plotting of the input data and results. Practical applications include the analysis of complicated patterns in such fields as electronics, communications and business.

TFA (Transfer Function Analyzer) — Price: $19.95 Cassette/$23.95 Diskette
This is a special software package which may be used to evaluate the transfer functions of systems such as hi-fi amplifiers and filters by examining their response to pulsed inputs. TFA is a major modification of FOURIER ANALYZER and contains an engineering-oriented decibel versus log-frequency plot as well as data editing features. Whereas FOURIER ANALYZER is designed for educational and scientific use, TFA is an engineering tool. Available for all computers.

HARMONIC ANALYZER (Available for all computers) — Price: $24.95 Cassette/$28.95 Diskette
HARMONIC ANALYZER was designed for the spectrum analysis of repetitive waveforms. Features include data file generation, editing and storage/retrieval as well as data and spectrum plotting. One particularly unique facility is that the input data need not be equally spaced or in order. The original data is sorted and a cubic spline interpolation is used to create the data file required by the FFT algorithm.

FOURIER ANALYZER, TFA and HARMONIC ANALYZER may be purchased together for a combined price of $49.95 (three cassettes) and $59.95 (three diskettes).

REGRESSION I (Available for all computers) — Price: $19.95 Cassette/$23.95 Diskette
REGRESSION I is a unique and exceptionally versatile one-dimensional least squares "polynomial" curve fitting program. Features include very high accuracy; an automatic degree determination option; an extensive internal library of fitting functions; data editing; automatic data and curve plotting; a statistical analysis (eg: standard deviation, correlation coefficient, etc.) and much more. In addition, new fits may be tried without reentering the data. REGRESSION I is certainly the cornerstone program in any data analysis software library.

REGRESSION II (PARAFIT) (Available for all computers) — Price: $19.95 Cassette/$23.95 Diskette
PARAFIT is designed to handle those cases in which the parameters are imbedded (possibly nonlinearly) in the fitting function. The user simply inserts the functional form, including the parameters (A(1), A(2), etc.) as one or more BASIC statement lines. Data and results may be manipulated and plotted as with REGRESSION I. Use REGRESSION I for polynomial fitting, and PARAFIT for those complicated functions.

MULTILINEAR REGRESSION (MLR) (Available for all computers) — Price: $24.95 Cassette/$28.95 Diskette
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BASIC SCIENTIFIC SUBROUTINES, Volumes 1 and 2 (Not available for Atari)
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Price per collection: $14.95 Cassette/$18.95 Diskette
All three collections are available for $39.95 (three cassettes) and $49.95 (three diskettes).

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Clocked Interrupts for the COSMAC Elf

Gary H. Price
733 Blue Sage Drive
Sunnyvale, CA 94086

Clocked (periodic) interrupts are useful in many microprocessor applications. My wish was to operate a data-logging system in the background while my COSMAC Elf was also executing other tasks. Clocked interrupts provide a relatively simple software-control method for the background task without burdening the system with software timing loops or flag checks.

Hardware

The 1802 microprocessor, around which the Elf is built, has a simple interrupt capability, which consists of a single hardware interrupt-request line that, when set, causes the pointers to the registers being used as stack pointer and program counter to be saved in register T, the assignment of register 2 as stack pointer, the assignment of register 1 as program counter, and further interrupt requests to be ignored by the 1802 until the interrupt-request line is reenabled by the execution of the RET (Return) instruction.

The 1802 provides instruction for transferring T register contents to the stack; return from the interrupt-service routine is accomplished by restoring the saved pointer values from the stack on execution of the RET instruction. The interrupt-request line can also be enabled and disabled under software control independently of the interrupt-service routine.

Interlacing interrupt tasks can minimize interference.

If the interrupt clock were to be the only source of interrupts in the system, the clock design would present few challenges. But, as do many 1802-based systems, my Elf includes an 1861 video-output processor. This device uses 1802 interrupt, direct memory access (DMA), and flag lines to produce low-resolution graphics with partial software control of the output format. To use this capability concurrently with the clocked interrupts, some means for recognizing the source of an interrupt request must be provided.

An interrupt-priority structure is common to management of multiple-interrupt sources. Such a structure is, however, not necessarily the best choice when two interrupt sources are involved. If synchronizing the interrupt requests does not otherwise handicap performance, interlacing interrupt tasks will minimize their interference with each other; such is the case here, and the interrupt clock was therefore designed to synchronize with the 1861.

Additional hardware may not be needed in some instances. The interrupt clock could be fashioned in software by maintenance of a counter within the 1861 interrupt-service routine—a feasible alternative if the 1861 were never disabled and if its DMA-out requests could be accommodated even when no graphics output is intended. These constraints are sometimes awkward.

The clock circuit is diagrammed in figure 1 for the bus used in the

About the Author

Gary Price is a senior physicist in the Radio Physics Laboratory at SRI International, Menlo Park, California. His professional activities include scientific programming but little involvement with microprocessor hardware or software. He assembled the small Elf II system from kits to gain some understanding of the basic workings of microprocessor systems. His other hobbies include amateur radio (W6IRA) operation and letterpress printing.

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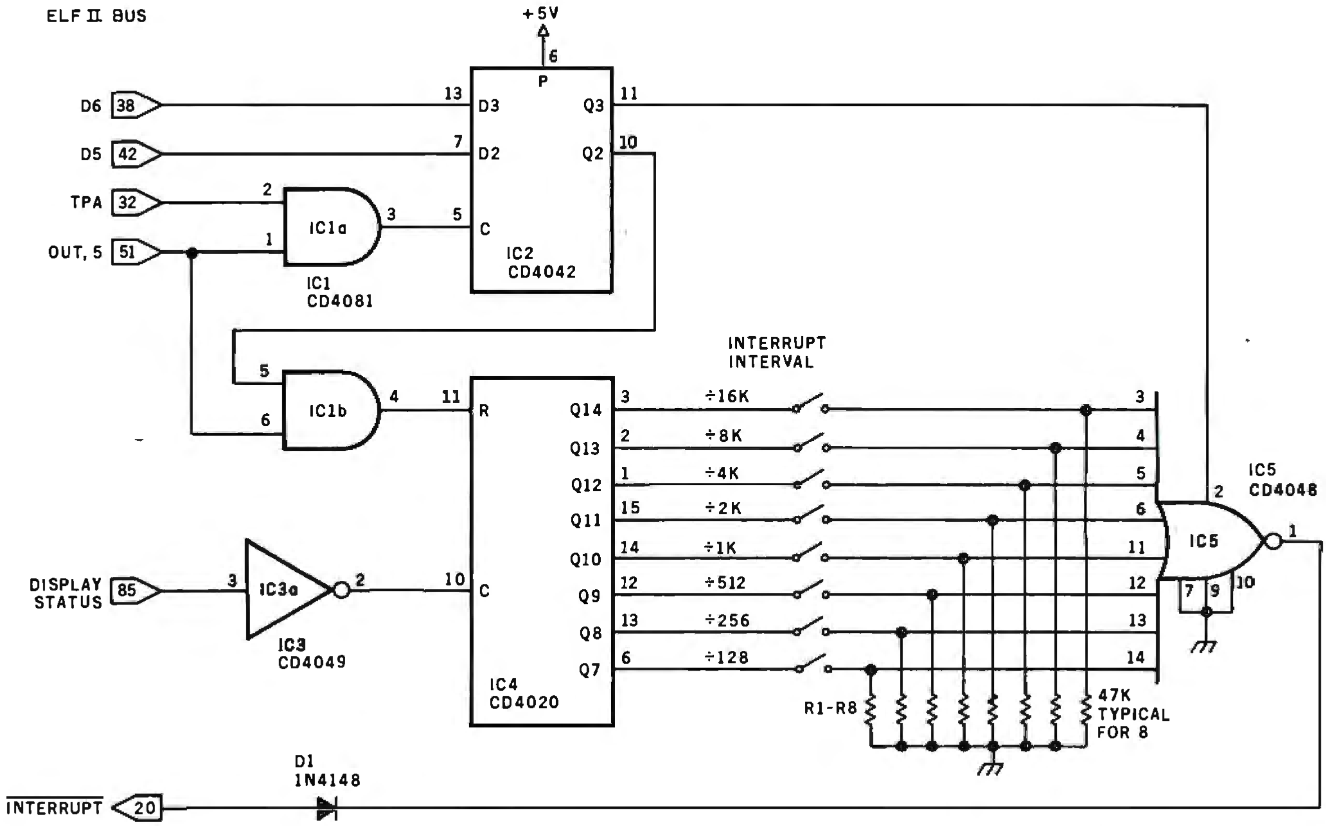

Figure 1: *Schematic diagram of the clock hardware and its connection to the Elf II bus. The clocked interrupts are developed from system-timing signals to alternate with interrupts from the video display; neither will interrupt the other while it is being serviced by the processor. A set of DIP switches allows the user to select a division factor so that interrupts can occur at regular intervals from about two per second to one per minute.*

Netronics Elf II; other Elf versions differ. in their bus structures. Clock-interrupt requests are synchronized with those from the 1861 by driving the clock counter from the 1861 Display Status line, which remains active even when the 1861 is disabled. The line goes low twice during each 1861 video frame, or at about 122 Hz when the Elf is operated with a conventional 3.58-MHz crystal. The rate is divided by IC4, a 4020 CMOS 14-stage binary counter; the last eight stages provide interrupt-output rates ranging from about two requests per second to about one per minute.

The counter-output lines are fed through a set of switches to IC5, an eight-input programmable gate. The interrupt rate is determined by which switch is closed. You may use a control bit (D6) to disable the clock when desired; a second control bit (D5) resets the clock counter. With this arrangement, the clock-interrupt request remains present for up to one full clock interval when not immediately answered.

The interrupt source may be recognized by a Display Status signal test within the interrupt-service routine. In the Elf II, this 1861 output is fed to 1802 flag line 1, so it is readily accessible in software. Display Status is set low twice during each 1861 display frame: once during the last four horizontal video scans of the vertical-retrace time and again in the final four scans of the display frame. The 1861 interrupt-request signal is present only during the last half of the first of the two periods (when Display Status is low). Advancing the clock counter on the trailing (low-to-high) edge of the Display Status signal initiates the clock-interrupt requests while Display Status is high; those from the 1861 occur while Display Status is low. Thus a prompt test of flag line 1 within the interrupt-service routine can be used to distinguish between the two interrupt sources.

The clock-interrupt requests might occur at the end of the Display Status-low period just *preceding* the 1861 video-display time, rather than when Display Status goes high at the end of this time. If this happens, the clock-interrupt service activity and the 1861 display generation are overlaid rather than interlaced. This problem does not arise, however, if the 1802 interrupt line remains disabled from the beginning of the display generation until after termination of the second low period.

In this case response to the first mistimed clock-interrupt request is delayed until after passage of the proper Display Status-low signal. The consequent delay of the clock reset (initiated within the interrupt-service routine) insures correct timing for subsequent clock-interrupt requests. The interrupt-reenable delay needed for this adjustment is usually inher-

Number	Type	+5 V	GND
IC1	CD4081	14	7
IC2	CD4042	16	8
IC3	CD4049	16	8
IC4	CD4020	16	8
IC5	CD4048	16	8

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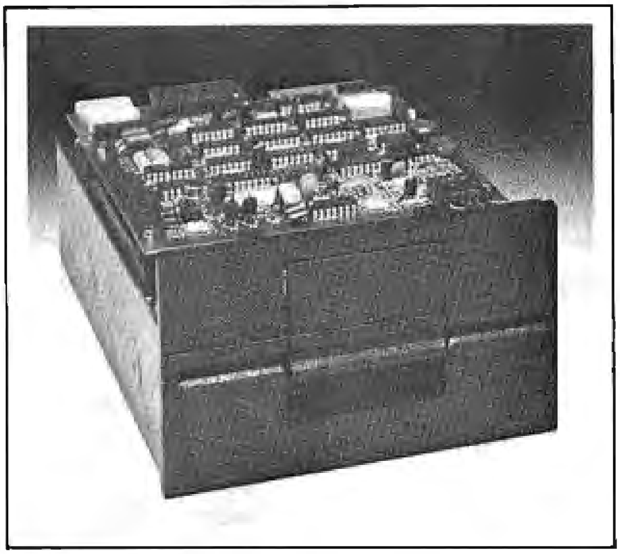

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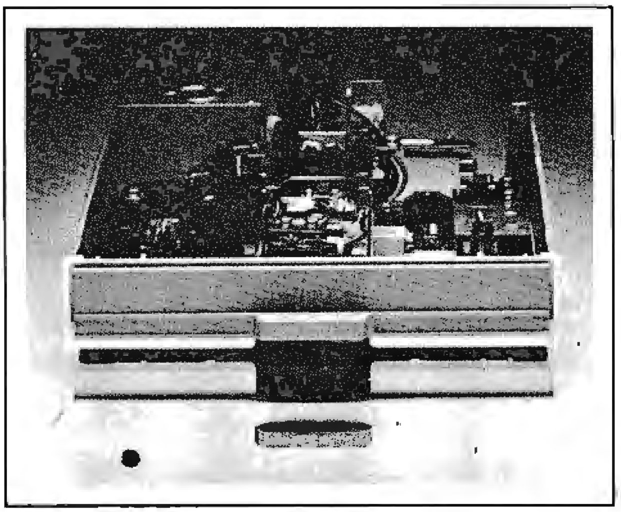

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Listing 1: *A clock-test program illustrates interrupt-service techniques.*

```
        Instr-
Label   uction  Argument  Comments
        DIS     X=0,P=0   Disable 1802
                            interrupt response
        LDI     PAGE
        PHI,1
        PHI,2
        PHI,3
        PHI,4
        LDI     INT.0
        PLO,1
        LDI     STACK.0
        PLO,2
        LDI     MAIN.0
        PLO,3
        LDI     COUNT.0
        PLO,4
        LDI     ZERO      Initialize clock
                            counter
        STR,4
        OUT,4   ZERO      Display initial
                            count
        OUT,5   CLKSET    Start clock, with
                            reset
        RET     X=3,P=3   Jump to main, with
                            interrupt enable
COUNT   --
RETINT  LDXA              Interrupt-service
                            return, restore
                            registers
        PHI,4
        LDXA
        PLO,4
        LDXA
        SHL
        LDXA
        RET
INT     DEC,2             Entry, save register
                            contents on stack
        SAV               T (old X,P)
        DEC,2
        STXD              D
        RSHR
        STXD              DF
        GLO,4
        STXD              R4.0
        GHI,4
        STXD              R4.1
        LDI     PAGE      Set up pointer
                            to COUNT
        PHI,4
        LDI     COUNT.0
        PLO,4
        LDN,4             Increment count
        ADI     ONE
        STR,4
        STR,2             Display count
        OUT,4
        DEC,2
        LDI     CLKSET    Reset clock timer
        STR,2
        OUT,5
        BR      RETINT    Loop to return
MAIN    BN4     MAIN      Wait for interrupt
                            or clock disable
        OUT,5   CLKDIS    Disable clock
HOLD    B4      HOLD        hold disable
        OUT,5   CLKENB    Reenable clock
        BR      MAIN
        --
        --
        --
STACK   --

Register usage:
  R1    Interrupt program counter
  R2    Interrupt stack pointer
  R3    Main program counter
  R4    Storage pointer

Constants:
  CLKENB  40*
  CLKDIS  00
  CLKSET  60*
  ONE     01
  PAGE    00
  ZERO    00

Hex dump:
 Location  Contents
   0000    71 00 F8 00 B1 B2 B3 B4 F8 26 A1 F8 FF A2 F8 43
     10    A3 F8 1D A4 F8 00 54 64 00 65 60*70 33 00 72 B4
     20    72 A4 72 FE 72 70 22 78 22 73 76 73 84 73 94 73
     30    F8 00 B4 F8 1D A4 04 FC 01 54 52 64 22 F8 60*52
     40    65 30 1E 3F 43 65 00 37 47 65 40*30 43

Notes:
 *Hardware dependent, see text.
```

ently present in 1861 interrupt-service routines, so an additional software burden is seldom imposed by this requirement.

A stand-alone clock could be usefully improved if interrupt-rate selection was placed under software control. Replacement of the manual switches with logic gates achieves this. With two control bits performing the interrupt-disable and counter-reset functions, the remaining six can directly access six of the 4020 counter-output lines, or four can help a 4514 4-to-16 line decoder access all 14 counter-output lines. In the last instance, selecting one of the two unused decoder-output lines effectively disables the clock and no separate disable bit is necessary. The decoder contains internal latches, so the 4042 latch (IC2) shown in figure 1 can also be eliminated.

Software

The interrupt clock's operation with your assembly-language programs presents few difficulties. Register 1 must be reserved as the program counter in the interrupt-service routine, and register 2's use as the stack pointer in this routine must also be anticipated. To assure that these registers are initialized before they are called upon by the interrupt-service routine, interrupts must be inhibited upon the 1802's initial entry into the run mode, following reset.

Because no provision is made for clock-hardware-interrupt requests to be disabled by 1802 reset, interrupt inhibition must be performed in software. The 1802 interrupt response is automatically disabled for one instruction following reset, providing sufficient time for this action to be accomplished by execution of a DIS (disable) instruction as the program's first instruction at location 0000.

Execution of the DIS instruction also reassigns the stack-pointer and program-counter registers, through replacement from the stack of the contents of registers X and P. Whenever the same register is being used as both program counter and stack

Text continued on page 312

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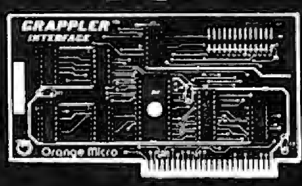

Listing 2: *Coordination of clock and video display is tested by displaying clocked count on screen.*

```
         Instr-
Label    uction   Argument   Comments
         DIS      X=0,P=0    Disable 1802
                               interrupt response
         GHI,0               Initialize registers
         PHI,1
         PHI,2
         LSKP                Reserve display
         IDL                   space
         IDL
         PHI,3
         PHI,B
         PHI,C
         PHI,D
         PLO,7               Initialize clock
                               counter
         LSKP
         IDL
         IDL
         LDI      INT.0
         PLO,1
         LDI      STACK.0
         LSKP
         IDL
         IDL
         PLO,2
         LDI      MAIN.0
         PLO,3
         RET      X=2,P=3    Jump to main, with
                               interrupt enable &
                               R2 assigned as
                               stack pointer
         IDL
         IDL
MAIN     LDI      RESET      Activate clock
         STR,2
         OUT,5
         DEC,2
         LSKP
         IDL
         IDL
LMAIN    BN4      TVON       Top of MAIN loop
         OUT,1               Disable 1861 video
         DEC,2
         BR       HOLD
         IDL
         IDL
RTNC     LDI      RESET      Interrupt-service
                               routine
         STR,2               Reset clock
         OUT,5
         BR       SKIP
         IDL
         IDL
SKIP     DEC,2
         INC,7               Increment clock
                               count
         GLO,7
         STR,2
         OUT,4
RTN      LDXA                Restore registers
         RET
INT      NOP                 Entry to interrupt
                               service routine
         DEC,2               Save register
         SAV                   contents on stack
         DEC,2
         STXD
         SEX,2               Timing
         BN1      RTNC       Test for clock
                               interrupt
         INC,2
         GHI,1               Set up DMA pointer
         PHI,0                 for video output
         LDI      DISP.0
         PLO,0
REFR     GLO,0               Display refresh loop
         SEX,2               Timing
         (DMA)
         SEX,2
         DEC,0
         PLO,0
         (DMA)
         SEX,2
         DEC,0
         PLO,0
         (DMA)
         SEX,2
         DEC,0
         PLO,0
         (DMA)
         BN1      REFR
         BR       RTN
HOLD     B4       HOLD       Hold 1861 disable
TVON     IN,1                Enable 1861
         LDI      ZERO       Start, translation
         PLO,8                 of clock count to
         PLO,9                 decimal, reset
                               digit counters
         LDI      DGTSU.0    Initialize digit
         PLO,D                 pointer
         GLO,7               Get count
LH       SMI      HUND       Extract hundreds
         BM       TENS         digit
         INC,8
         BR       LH
TENS     ADI      HUND
LT       SMI      TEN        Extract tens digit
         BM       UNITS
         INC,9
         BR       LT
UNITS    ADI      TEN
         STR,D               Store digits
         DEC,D
         GLO,9
         STR,D
         DEC,D
         GLO,8
         STR,D
         BNZ      DISPLY     Test for nil
         ADI      TEN          hundreds digit
         STR,D                 Blank if nil
         INC,D               Test for nil tens
         LDN,D                 digit
         BNZ      DISPLY
         ADI      TEN          Blank if nil
         STR,D
DISPLY   LDI      DGTSH.0    Format decimal count
         PLO,D                 for video display
         LDI      DSTRT      Initialize display
         PLO,B                 pointer
         LDI      MSKC1      Column mask to stack
         STR,2
LDSP     LDN,2               Digit loop
         SHR
         STR,2
         GLO,D
         SHR
         BNF      ADV        Test for display
                               byte hi/lo nibble
         LDI      MSKC2      Reset column mask
         STR,2
         INC,B               Increment display
                               pointer
ADV      LDA,D               Load character-table
         SHL                   pointer
         ADI      CHARO.0    Add base address
         PLO,C
         LDA,C               Load character bits
         PHI,A                 to working storage
         LDI      BITCNT     Initialize bit
         PLO,A                 counter
         LDI      COLCNT     Initialize column
         PLO,8                 counter
LCOL     DEC,8               Column loop
                               decrement count
         GLO,B               Reset display
```

Listing 2 continued on page 312

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Listing 2 continued:

```
        SMI     DIGDEC     pointer
        PLO,B
        LDI     ROWCNT    Initialize row
                           counter
        PLO,9
LROW    DEC,9             Row loop, decrement
                           count
        DEC,A             Decrement bit count
        GLO,B             Advance display
        ADI     ROWADV     pointer
        PLO,B
        GHI,A             Extract character
        SHL                bits, to DF
        PHI,A
        LDN,B             Load display byte
        OR                Process bit, set
        BDF     PLOP       Test &
        XOR                reset if reset
PLOP    STR,B              Replace byte
        GLO,A             Check bit count
        BNZ     ENDROW
        LDN,C             Update character
        PHI,A              byte
        LDI     BITCNT
        PLO,A
ENDROW  GLO,9             Check row count
        BNZ     LROW       Loop if not done
        LDN,2             Shift column mask
        SHR
        STR,2
        GLO,8             Check column count
        BNZ     LCOL       Loop if not done
        GLO,D             Check digits count
        SMI     CHARO.0
        BNZ     LDSP       Loop if not done
        BR      LMAIN     End main loop
        --                Stack space
        --
        --
STACK   --
DGTSH   --                Digits storage
        --
DGTSU   --
CHARO   --      74        Character table
        --      5C
        --      4F
        --      C2
        --      9D
        --      52
        --      8D
        --      54
        --      70
        --      BE
        --      ED
        --      64
        --      75
        --      64
        --      9D
        --      30
        --      55
        --      54
        --      45
        --      5C
        --      00
        --      00

Register usage:
  R0    DMA pointer
  R1    Interrupt program counter
  R2    Stack pointer
  R3    Main program counter
  R7.0  Clock count
  R8.0  Hundreds digit, column counter
  R9.0  Tens digit, row counter
  RA.0  Bit counter
  RA.1  Character byte, working storage
  RB    Display pointer
  RC    Character-table pointer
  RD    Digit pointer/counter

Constants:
  BITCNT  08
  COLCNT  03
  DIGDEC  28
  DSTRT   26
  HUND    64
  MSKC1   10
  MSKC2   80
  RESET   60
  ROWADV  08
  ROWCNT  05
  TEN     0A
  ZERO    00
```

Hex dump:

Location	Contents															
0000	**71**	**00**	**90**	**B1**	**B2**	**C8**	**00**	**00**	**B3**	**BB**	**BC**	**BD**	**A7**	**C8**	**00**	**00**
10	F8	3F	A1	F8	DF	C8	00	00	A2	F8	20	A3	70	23	00	00
20	F8	60	52	65	22	C8	00	00	3F	5E	61	22	30	5C	00	00
30	F8	60	52	65	30	38	00	00	22	17	87	52	64	72	70	C4
40	22	78	22	73	E2	3C	30	12	91	B0	F8	00	A0	80	E2	E2
50	20	A0	E2	20	A0	E2	20	A0	3C	4D	30	3D	37	5C	69	F8
60	00	A8	A9	F8	E2	AD	87	FF	64	3B	6E	18	30	67	FC	64
70	FF	0A	3B	77	19	30	70	FC	0A	5D	2D	89	5D	2D	88	5D
80	3A	8C	FC	0A	5D	1D	0D	3A	8C	FC	0A	5D	F8	E0	AD	F8
90	26	AB	F8	10	52	02	F6	52	8D	F6	3B	A0	F8	80	52	1B
A0	4D	FE	FC	E3	AC	4C	BA	F8	08	AA	F8	03	A8	28	8B	FF
B0	28	AB	F8	05	A9	29	2A	8B	FC	08	AB	9A	FE	BA	0B	F1
C0	33	C3	F3	5B	8A	3A	CC	0C	BA	F8	08	AA	89	3A	B5	02
D0	F6	52	88	3A	AD	8D	FF	E3	3A	95	30	28	00	00	00	00
E0	00	00	00	74	5C	4F	C2	9D	52	8D	54	70	BE	ED	64	75
F0	64	9D	30	55	54	45	5C	00	00							

Text continued from page 308:

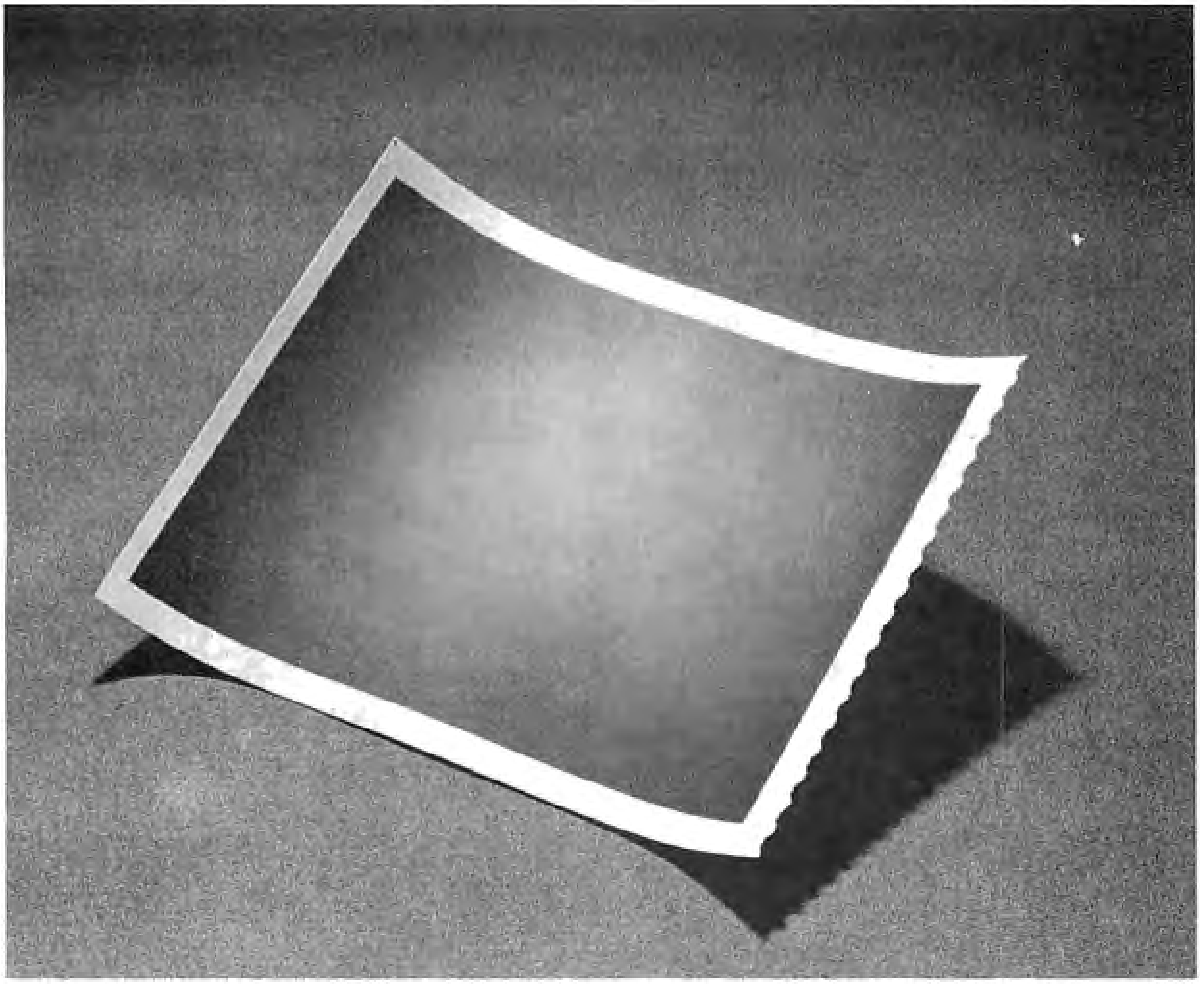
pointer (as on entry into the run mode following reset), any instruction that references the stack actually accesses the byte immediately following the instruction in memory. Thus the initial DIS must precede an immediate data byte of value 00 to preserve register 0 as program counter and stack pointer until other registers are set up to perform these functions.

Several considerations must be kept in mind in the development of the interrupt-service routine. Basically, the contents of all registers outside the routine should be the same on departure from the routine as at the time of the interrupt. Thus the contents of any register used by the interrupt-service routine and the external program should be saved—normally by storage on the stack—before the register is used within the routine. After the interrupt task is completed, contents are restored to their registers before returning to the interrupted program.

To illustrate the preceding points, listing 1 provides a program to verify the clock's basic operation. The interrupt-service routine is somewhat more complex than necessary to demonstrate the treatment of registers. The contents of registers used by the routine—D, DF (in case of overflow on execution of the ADI at 0037), and 4—are all saved and restored, in addition to X and P. Also note the routine's loop structure, which causes register 1 to point to the routine entry upon exit from it.

The interrupt-service routine operation in listing 1 counts the interrupts serviced and shows this count on the Elf II's display, accessed in the Elf II via output port 4. Clock operation is inhibited by pressing the Elf I (input) key, which is connected to 1802 flag line 4 in the Elf II. The

Text continued on page 316



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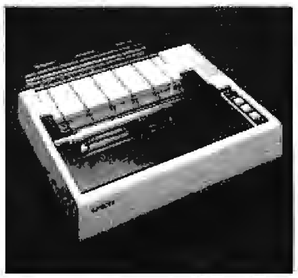

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Listing 3: *Tiny BASIC machine-language modifications to add clocked interrupts when using serial video terminal for I/O.*

Location	Label	Instruction	Argument	Comments
0000		DIS	X=0,P=0	Disable 1802 interrupt response
02		LBR	BASIC	Branch to BASIC start
05		SEX,8		Monitor entry, with
06		DIS	X=0,P=0	1802 interrupt disable
--				
000F		SEP,8		Complete monitor link
--				
0020		--	PRGSTRT	Address of BASIC program start
--				
00B6		--	RESET	Clock reset code
B7	COUNTH	--		Clock count storage
B8	COUNTL	--		
B9	CONTINIT	B3	SKIP	Initialization
BB		BN4*	CONTINIT	Wait for serial input
BD		DIS	X=2,P=3	Disable clock
--				
0106	LCHARIN	LBR	CHARIN	Entry address
09		LBR	CHAROUT	Entry address
--				
0113		--	STKRES	ML stack reserve
--				
011C		--	PRGSTRT	Address of BASIC program start
--				
0182		--	CLKENB	IL jump table entry for clock enable
--				
01A2		--	CLKDIS	IL jump table entry for clock disable
--				
0202		--	INTINIT	Branch to finish interrupt setup
--				
0A7F		--	ENDCHIN	Branch to enable clock on exit from input routine
--				
0AA4		--	ENDCHOU	Branch to enable clock on exit from output routine
--				
0B13		--	LCHARIN	To funnel serial input through clock disable
--				
0B87	CLKENB	SEX,3		Clock enable routine
88		RET	X=D,P=5	by 1802 enable
8A	CLKDIS	SEX,3		Clock disable routine
8B		DIS	X=D,P=5	by 1802 disable
8D	CHARIN	GHI,E		Terminal input routine
8E		BNZ	CONT.A	
90		SEP,5		Return if cannot handle
91	CONT.A	SEX,3		Prepare to disable clock
92	WAIT	BN4*	WAIT	Wait for input
94		DIS	X=2,P=3	Disable clock
96		SHR		Adjust timing delay
97		SMI	ONE	for extra instructions
99		SEP,4	HALFTIME	
9C		B4*	CONT.B	
9E		SEX,3		False alarm,
9F		RET	X=2,P=3	enable clock
A1		BR	CHARIN	
A3	CONT.B	SEX,2		Timing
A4		SEX,2		
A5		LBR	STARTRD	Begin input processing
A8	ENDCHIN	SEX,3		Enable clock at end
A9		RET	X=2,P=3	of input
AB		LBR	FULLTIME	Finish up
AE	CHAROUT	SEX,3		Disable clock for
AF		DIS	X=2,P=3	character output
B1		LBR	STARTWR	Begin output processing
B4	ENDCHOU	SEX,3		Enable clock at end
B5		RET	X=2,P=3	of output
B7		GLO,C		
B8		LBR*	FINWR	Finish up
BB	INTINIT	PLO,7		Interrupt initialization
BC		LDI	INT.1	Set up R1 as inter-
BE		PHI,1		rupt program
BF		LDI	INT.0	counter
C1		PLO,1		
C2		SEX,3		For OUT byte
C3		BNF	CONT.C	Test cold/warm start
C5		OUT,5	ENABLE	Warm, enable clock
C7		LBR	CONTWARM	& continue
CA	CONT.C	RET	X=D,P=7	Cold, enable 1802
CC		--	COUNTH.0	& reset clock
CD		GHI,D		Zero count
CE		STXD		
CF		STXD		
D0		OUT,5		Reset
D1		SEX,3		
D2		LBR	CONTINIT	Back to mainstream
D5	RTN	SEX,2		Interrupt routine
D6		LDXA		Restore registers
D7		SHL		
D8		LDXA		
D9		RET		& return
DA	INT	DEC,2		Entry
DB		SAV		Save registers
DC		DEC,2		
DD		STXD		
DE		SHRC		
DF		STR,2		
E0		LDI	COUNTL.1	Set up R0 as
E2		PHI,0		pointer to clock
E3		LDI	COUNTL.0	count
E5		PLO,0		
E6		SEX,0		
E7		LDI	ONE	Increment count
E9		ADD		
EA		STXD		
EB		LDI	ZERO	
ED		ADC		
EE		STXD		
EF		OUT,5		Reset clock counter
F0		BR	RTN	

Addresses and constants:

BASIC	0100
CONTWARM	021A
ENABLE	40
FINWR	0ADE
FULLTIME	00F6
HALFTIME	00F9
ONE	01
PRGSTRT	0BF2
RESET	60
SKIP	E1
STARTRD	0A65
STARTWR	0A83
STKRES	1C
ZERO	00

Listing 3 continued on page 316

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Listing 3 continued:

```
Hex list:
 Location  Contents
   0000    7 00 C0 01 00 E8 71 00 . . .     . . . D8
    --
   0020    0B F2 . . .
    --
   00B6              . . . 60 00 00 36 E1 3F*B9 71 23 .
    --
   0106              . . . C0 0B 8D C0 0B AE . . .
    --
   0113     . . . 1C . . .            . . . 0B F2 . .
    --
   0182     . . 0B 87 . . .
    --
   01A2     . . 0B 8A . . .
    --
   0202     . . 0B BB . . .
    --
   0A7F                                     . . . 0B
     80    A8 . . .
    --
   0AA3     . . . C0 0B B4 . . .
    --
   0B13     . . . 01 06 . . .
    --
   0B87                . . . E3 70 D5 E3 71 D5 9E 3A 91
     90    D5 E3 3F*92 71 23 F6 FF 01 D4 00 F9 37*A3 E3 70
     A0    23 30 8D E2 E2 C0 0A 65 E3 70 23 C0 00 F6 E3 71
     B0    23 C0 0A 83 E3 70 23 8C C0*0A DE A7 F8 0B B1 F8
     C0    DA A1 E3 3B CA 65 40 C0 02 1A 70 D7 B7 9D 73 73
     D0    65 E3 C0 00 B9 E2 72 FE 72 70 22 78 22 73 76 52
     E0    F8 00 B0 F8 B8 A0 E0 F8 01 F4 73 F8 00 74 73 65
     F0    30 D5
    --
Notes:
  *For unmodified Netronics Tiny BASIC, change B4 (37)
   to BN4 (3F), BN4 (3F) to B4 (37), and the LBR (C0)
   at 0BB8 to SEP,5 (D5).
```

Text continued from page 312:

clock-control byte is sent in this and other program listings to parallel port 5, with bits 6 and 7 (i.e., D5 and D6) used for clock reset and enable, respectively (see figure 1). These assignments should match the hardware implementation of the clock with which the program is run.

Listing 2 illustrates modification of a standard 1861 display routine to sort 1861 and clock interrupts. The clock portion of the interrupt-service routine again counts clock interrupts, and the count is sent to the Elf II's display and the 1861 video-display device. The video-displayed count is translated from hexadecimal to decimal before being formatted for storage in the display memory area. The I key disables the 1861 in this program, permitting independent clock operation to be checked.

The interrupt-service routine's particular placement within the overall program (see listing 2) is not critical; the arrangement shown is simply the first that gave a reasonably efficient procedure for allocating memory space to the display area. Allocation is normally straightforward, but the decision to confine the program (including display) entirely to a single page of memory makes it less so.

The possible disruption of 1861 timing, however, requires serious attention. A strict relationship must be preserved between the onset of 1861 interrupt and DMA requests and the 1802 instruction fetch/execute cycle, in order to maintain a jitter-free video display. To preserve this timing relationship, no three-cycle (fetch/execute/execute) instructions are included within the interrupted program; the one-cycle 1802 interrupt response is compensated by including an odd number of such instructions within the interrupt-service routine, preceding the first low $\overline{\text{SYNC}}$ pulse output by the 1861 subsequent to the 1802 interrupt response. For 1861 interrupts, the pulse normally occurs on the thirteenth 1802 machine cycle following the 1802 interrupt-request response.

The $\overline{\text{SYNC}}$ pulse location within the clock-interrupt-service sequence

Text continued on page 320

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Listing 4: *Tiny BASIC machine-language modifications to add clocked interrupts when using parallel keyboard input and 1861 video device for output.*

```
Loca-            Instr-
tion   Label     uction   Argument   Comments
0000             DIS      X=0,P=0    Disable 1802
                                       interrupt response
  02             LBR      BASIC      Branch to BASIC
                                       start
  05             SEX,3               Monitor entry, with
  06             DIS      X=0,P=0      1802 interrupt
                                       disable
 —
00B6             --       RESET      Reset data byte
  B7   COUNTH    --       ZERO       Clock count storage
  B8   COUNTL    —        ZERO
  B9   CONTINIT  PLO,7               Continue initial-
                                       ization
  BA             SEX,3                 Enable clock
  BB             OUT,5    ENABLE
  BD             LBDF     CONTWARM     Branch if warm
                                         start
  C0             OUT,5    RESET        Reset clock
  C2             SEP,7    COUNTH.0       & zero count
  C4             GHI,D
  C5             STXD
  C6             STXD
  C7             PHI,E                 Set I/O-type flag
  C8             LDI      .FF.           & continue
  CA             SEP,4    LCHAROUT
  CD             LBR      CONTCOLD
  D0   CLKENB    SEX,3               IL Clock enable
  D1             OUT,5    ENABLE       routine
  D3             SEP,5                 Return
  D4   CLKDIS    SEX,3               IL Clock disable
  D5             OUT,5    DISABLE      routine
  D7             SEP,5                 Return
 —
0106             LBR      CHARIN     Entry to character
                                       input routine
  09   LCHAROUT  LBR      CHAROUT    Entry to character
                                       output routine
 —
0113             —        STKRES     ML stack reserve
 —
0182             —        CLKENB     IL table entry,
                                       clock enable
 —
01A2             —        CLKDIS     IL table entry,
                                       clock disable
 —
0202             —        CONTINIT   Branch address to
                                       pick up clock
                                       initialization
09D9             —        INT.0      Lo byte, interrupt
                                       service entry
 —
09DC             —        INT.1        Hi byte
 —
0A5A   RTNINT    LDI      MON.1      Interrupt service
                                       routine
  5C             PHI,0                 Set R0 up for
  5D             LDI      MON.0          monitor jump
  5F             PLO,0
  60             SEX,2                 Restore saved
  61             LDXA                    register
  62             SHL                     contents
  63             LDXA
  64             RET
  65   INT       NOP                   Entry, establish
                                         timing
  66             DEC,2                 Save registers
  67             SAV
  68             DEC,2
  69             STXD
  6A             SHRC
```

```
  6B             STR,2
  6C             SEX,0                      For clock
  6D             BN1        CLOCK           Test interrupt
                                              type
  6F             LDI        DISP.1          Video branch
  71             PHI,0
  72             LDI        DISP.0
  74             PLO,0
  75   VIDLOOP   GLO,0
                 (DMA)
  76             DEC,0
  77             PLO,0
  78             SEX,C
                 (DMA)
  79             DEC,0
  7A             PLO,0
  7B             GHI,0
                 (DMA)
  7C             XRI        ENDPAGE
  7E             BNZ        VIDLOOP
  80             PHI,C
  81             LDI        VIDCNT.0
  83             PLO,C
  84             LDX
  85             ADI        ONE
  87             STR,C
  88             SMI        MAXCNT
  8A             SEX,C                      Timing for fol-
                                              lowing clock
                                              interrupt
  8B             BNF        RTNINT
  8D             STXD
  8E             LDX
  8F             ADI        ONE
  91             STR,C
  92             BR         RTNINT
  94   CLOCK     LDI        COUNTL.1        Clock service
  96             PHI,0                        Set up R0 as
  97             LDI        COUNTL.0            pointer to
  99             PLO,0                          clock count
  9A             LDI        ONE               Increment cour
  9C             ADD
  9D             STXD
  9E             LDI        ZERO
  A0             ADC
  A1             STXD
  A2             OUT,5                        Reset clock
  A3             BR         RTNINT
 --
0AD6             SEX,2                      To delete 1802
                                              interrupt disabl
                                              on 1861 disable
```

```
Addresses and constants:
   BASIC       0100
   CHARIN      0AB0
   CHAROUT     0ABA
   CONTCOLD    0204
   CONTWARM    021A
   DISABLE     00
   DISP.0      B0
   DISP.1      0D
   ENABLE      40
   ENDPAGE     0F
   MAXCNT      3D
   MON.0       00
   MON.1       F0
   ONE         01
   RESET       60
   STKRES      1C
   VIDCNT.0    0F
   ZERO        00
   .FF.        0C
```

Listing 4 continued on page 320

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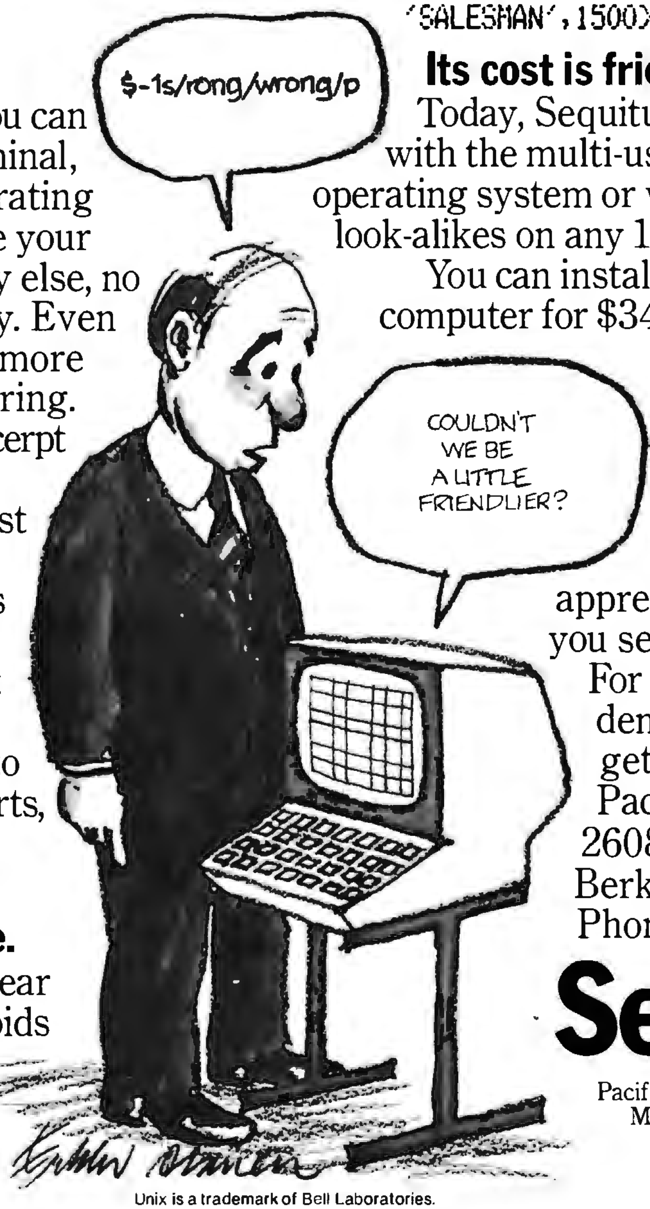

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Listing 4 continued:

```
Hex list:
 Location  Contents
    0000   71 00 C0 01 00 E3 71 00  .  .  .
    --
    00B6               .  .  . 60 00 00 A7 E3 65 40 C3 02 1A
      C0   65 60 D7 B7 9D 73 73 BE F8 0C D4 01 09 C0 02 04
      D0   E3 65 40 D5 E3 65 00 D5  .  .  .
    --
    0106               .  .  . C0 0A B0 C0 0A BA  .  .  .
    --
    0113    .  .  . 1C  .  .  .
    --
    0182    .  . 00 D0  .  .  .
    --
    01A2    .  . 00 D4  .  .  .
    --
    0202    .  . 00 B9  .  .  .
    --
    09D9                        .  .  . 65  .  . 0A  .  .  .
    --
    0A5A                              .  .  . F8 F0 B0 F8 00 A0
      60   E2 72 FE 72 70 C4 22 78 22 73 76 52 E0 3C 94 F8
      70   0D B0 F8 B0 A0 80 20 A0 EC 20 A0 90 FB 0F 3A 75
      80   BC F8 0F AC F0 FC 01 5C FF 3D EC 3B 5A 73 F0 FC
      90   01 5C 30 5A F8 00 B0 F8 B8 A0 F8 01 F4 73 F8 00
      A0   74 73 65 30 5A  .  .  .
    --
    0AD6               .  .  . E2  .  .  .
```

Text continued from page 316:

depends, however, on the timing of the exit from the preceding 1861 interrupt service, near the end of which the clock-interrupt request is normally set. If unrecognized, the dependence can lead to difficulties. In particular, if the SYNC pulse immediately follows the 1802 response to a clock-interrupt request, the interrupt cycle cannot be compensated before timing is tested by the 1861; in this case some minor display jitter occurs with each clock interrupt regardless of where timing is adjusted within the clock-service routine. Timing adjustment of the return from the 1861 interrupt-service routine is necessary here to eliminate the problem (see listing 4).

Careless placement within the interrupt-service routine of the test to separate clock and 1861 interrupt requests may also produce surprises in the Elf II if the Netronics Giant board has been installed. One function performed by this board is to logically OR 1861 Display Status and SYNC to produce the input to the 1802's flag line 1. The flag is consequently *reset* during the SYNC-low intervals, even when Display Status is low. The flag test fails to distinguish between the two interrupt sources if it is executed at this time.

The interrupt clock can also be used while running Tiny BASIC on the Elf, although not without some modification of the BASIC interpreter. The major difficulty to be overcome is interruption by the clock of serial I/O (input/output) transfers. In the Elf, the transfers are handled directly by the 1802 with software formatting and decoding of serial signals. Clock interrupts must therefore be inhibited during the transfers to avoid losing serial data. Interference with the clock unavoidably introduces minor variation to its rate; the variation, though undesirable, is probably less troublesome in many clock applications than are serial-data errors to BASIC use.

Two types of serial transfers are found in Tiny BASIC operation on the Elf: those to and from the terminal, and program SAVEs and LOADs to and from cassette tape. Whether terminal I/O involves serial data transfer depends on the terminal hardware used. Both serial terminal and parallel keyboard input are supported by the Tiny BASIC used here, along with serial terminal and direct (1861) video output. The specific interpreter modifications required to implement the clock depend somewhat upon which hardware options are used and on the Tiny BASIC version being run.

Serial I/O is best dealt with by execution of a clock disable on entry to the input or the output subroutine, followed by a reenable on exit. Clock operation does not affect parallel keyboard input, but the direct video output normally associated with such input in the Elf II involves 1861 interrupts. In this case the interrupt-service routine requires attention. An interrupt-service routine must be provided to perform the clock-initiated task, as well as code within the BASIC-initialization sequence to reset the clock. The interrupt pointer must also be defined preceding interrupt enable.

Protection of the SAVE and LOAD operations from clock interruption, though basically accomplished in the same manner as for terminal I/O, is most simply addressed in the context of the IL (intermediate language) through which BASIC instruction decoding is achieved. This is the approach adopted here, though it does not protect direct use of the tape read and write routines, through USR calls, from interruption by the clock. If such operation is contemplated, the routines should be protected at the machine-language level.

Stack use by the clock's interrupt-service routine must also be taken into account. This problem has been conservatively handled by addition to the stack reserve of the number of bytes used by the clock-service routine. Fewer bytes are probably necessary than are allocated, because the original stack reserve includes an allowance for its use by the 1861 interrupt-service routine. This last routine is denied free rein in Tiny BASIC, however; a prudent course is best in the absence of sure knowledge about the relevance of this restriction to the size of the original stack allocation.

Listings 3 through 5 detail patches developed to implement the clock—with storage in memory of its count—on my Elf II while running Netronics Tiny BASIC. Listing 3 describes changes and additions required by the clock when using serial terminal I/O. The modifications to Tiny BASIC recommended by Netronics for use with its video-terminal board are also assumed. If not, instructions marked with an asterisk should be changed as

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indicated by the note at the listing's end.

Additional space for BASIC programs can be obtained, should the Netronics modifications not have been made, by moving the block of code located between hexadecimal addresses 0B87 and 0BD9 forward to start at 0AA6. This last change requires adjustment of many instructions to indicate new jump and entry-point addresses in the relocated code. Remember to change the start address of the BASIC program area, stored at hexadecimal locations 0020 and 011C, if this modification is made; otherwise, the additional space is not actually allocated. Finally, note that monitor access is not provided in this case. The monitor call is also changed slightly, to USR(12,5,-4096), for the Netronics-modified BASIC version.

Listing 4 describes patches needed to implement the clock when running with parallel keyboard input and 1861 video output. The interrupt-service routine is a modified version of that originally present to service the 1861 video interrupts, to which are added operations necessary to identify and service clock interrupts. The entire routine has been shifted to a location where it need not be split into two pieces to accommodate the additions. A more complex clock-interrupt task, requiring additional code, must be moved to the end of the interpreter (see listing 3) or split. Monitor entry is via a USR(5) function call.

The modified interpreter-language (intermediate-language) sequence for execution of BASIC SAVE and LOAD commands is the same for both hardware options (see code in listing 5). Interpreter-language instruction mnemonics used in listing 5 are those adopted by Pittman (see references), the author of this and other Tiny BASIC interpreters for various microprocessors. Two new instructions, Enable Clock (EC, 1E hexadecimal) and Disable Clock (DC, 0E hexadecimal), are added to the interpreter-language instruction set. The interpreter-language modification requires only minor changes to the original code, providing space for clock enable and disable instructions. The new instructions are implemented in machine language and their entry points added to the interpreter-language jump table.

The clock count, stored at locations 00B7 through 00B8, can be accessed from BASIC with the PEEK command. The clock can also be controlled directly from BASIC with OUT 5,x commands or through USR function calls to the clock enable and disable routines. ■

Listing 5: *Tiny BASIC interpreter-language modifications to add clocked interrupts.*

Location	IL Address	Instruction	Argument
0885	011F	BC	7,'SAVE'
8A	24	BE	0
8B	25	J	0153
8D	27	BC	6,'LOAD'
92	2C	BE	0
93	2D	BR	+2
94	2E	J	0185
96	30	LB	24
98	32	LN	09FA
9B	35	LN	0001
9E	38	LB	20
A0	3A	FV	
A1	3B	DC	
A2	3C	US	
A3	3D	BR	+7
A4	3E	EC	
A5	3F	LN	001B
A8	42	AD	
A9	43	SV	
AA	44	WS	
AB	45	EC	
AC	46	NL	
AD	47	PC	'TAPE ERROR'
B8	52	MT	
B9	53	PC	'START TAPE'
C4	5E	NL	
C5	5F	PC	'HIT KEY'
CD	67	LN	0106
D0	6A	DS	
D1	6B	DS	
D2	6C	US	
D3	6D	SP	
D4	6E	NL	
D5	6F	LN	09FD
D8	72	LB	24
DA	74	FV	
DB	75	LB	20
DD	77	FV	
DE	78	SU	
DF	79	LN	0100
E2	7C	AD	
E3	7D	LB	20
E5	7F	FV	
E6	80	DC	
E7	81	US	
E8	82	EC	
E9	83	SP	
EA	84	NX	

Hex dump:

Location	Contents															
0885			.	.	.	87	53	41	56	C5	E0	39	53	86	4C	4F
90	41	C4	E0	62	39	85	09	24	0A	09	FA	0A	00	01	09	20
A0	12	0E	2E	67	1E	0A	00	1B	18	13	2D	1E	23	24	54	41
B0	50	45	20	45	52	52	4F	D2	2B	24	53	54	41	52	54	20
C0	54	41	50	C5	23	24	48	49	54	20	4B	45	D9	0A	01	06
D0	0B	0B	2E	0C	23	0A	09	FD	09	24	12	09	20	12	19	0A
E0	01	00	18	09	20	12	0E	2E	1E	0C	1D	.	.	.		

References

1. Pittman, T. *Tiny BASIC Experimenter's Kit.* Itty Bitty Computers (POB 23189, San Jose, CA 95153), 1977.
2. Price, G. "Clean Starts for Cosmac 1861 Video Output," *Dr. Dobb's Journal of Computer Calisthenics & Orthodontia,* Volume 5, Issue 7 (47), pp. 14-15 (August 1980).

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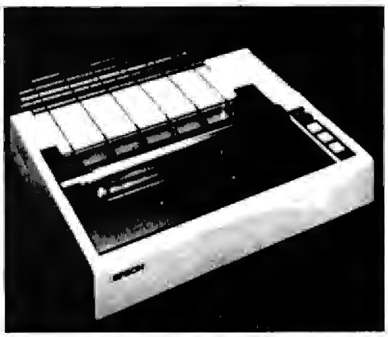

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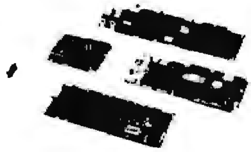

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A couple of years ago the comment was made in BYTE that some experimenters had trouble interfacing a Motorola 6820 PIA (peripheral interface adapter) to the Apple II computer ("Cross-Pollinating the Apple II," April 1979 BYTE, page 20). I found this incomprehensible, since the 6820 is virtually identical to the 6520 PIA, which was designed to work with the 6502 microprocessor (used in the Apple II).

At the request of an associate who sought a parallel port for his Apple, I attempted to interface a 6520 PIA to his computer. The result is shown in figure 1.

In this interface, the active-low select line $\overline{CS2}$ of the PIA is always connected to ground and the active-high select lines CS0 and CS1 are connected to the active-low $\overline{\text{Device Select}}$ (generated by logic in the Apple II) via a logic inverter. The signal selects its particular expansion slot when the microprocessor is addressing a specified area of memory. The $\overline{\text{Device Select}}$ signal considerably simplifies interfacing.

The interface is easy to build. The original prototype was done on a solderless prototyping board with the peripheral slot-connector signals brought out on 16-pin DIP (dual inline package) connectors with ribbon cables. These were in turn plugged into an Apple II expansion-slot prototyping card (Vector 4609DP or equivalent) that had been wire-wrapped to connect the expansion-slot signals to 16-pin DIP sockets. A 25-pair cable (24 AWG twisted pair) was used to bring the PA0 through PA7 and PB0 through PB7 connections on the PIA to the "outside world." Interface layout does not appear critical.

To test the interface, a DIP switch assembly and pull-up resistors were connected to PA0 through PA7 of the PIA, while PB0 through PB7 were connected to LEDs with dropping resistors via 7404 inverting buffers (see figure 2). The program in listing 1 was entered using the Apple II's miniassembler (not found in the newer auto-start ROMs) and was then run starting at hexadecimal address 0300. The program sets up port A as inputs and port B as outputs, with PB0 through PB7 initially set to a logic 0 state.

The program then continuously reads port A and writes the contents to port B. This causes the logic state of each switch to be transferred to its respective LED (a lighted LED corresponds to a logic 1 state). Changing the setting of the DIP switches allows you to test each line as well as the interface to the Apple II. (My associate said the test procedure's overall effect was to replace straight wire between the switches and LEDs with a computer!)

One disadvantage of the interface (see figure 1) is that the PIA is not fully and uniquely decoded—that is, the PIA can also be addressed by other groups of addresses assigned to an expansion slot. Figure 3 shows one method of overcoming this problem. The 74LS42 decodes address lines A2 and A3, so the PIA occupies only four of the 16 addresses allocated to an Apple II expansion slot. This also allows the addition of a second PIA on the same prototyping card. ■

Listing 1: *Program for testing the 6520 interface. Used in conjunction with the circuits in figure 2, it reads the value encoded on the switches through one port and then displays the same value on the LEDs through the other port.*

```
(Reset the Apple II prior to running this program.)
(Reset the Apple II to exit this program)
(PIA register addresses for expansion slot #4 used in this program:
  $C0C0 = Data Direction Register A (DDRA)/Output Register A
          (ORA)
  $C0C1 = Control Register A (CRA)
  $C0C2 = Data Direction Register B (DDRB)/Output Register B
          (ORB)
  $C0C3 = Control Register B (CRB).)

$0300  LDA  #$FF
$0302  STA  $C0C2   Write to DDRB to set PB0-PB7 as outputs
$0305  LDA  #$04
$0307  STA  $C0C1   Write to CRA to enable ORA, disable DDRA
$030A  STA  $C0C3   Write to CRB to enable ORB, disable DDRB
$030D  LDA  $C0C0   Read PA0-PA7 into accumulator
$0310  STA  $C0C2   Write accumulator into PB0-PB7
$0313  JMP  $030D   Repeat until reset
```

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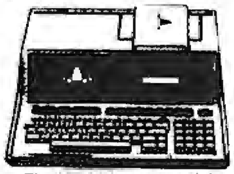

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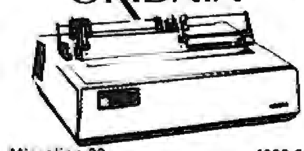

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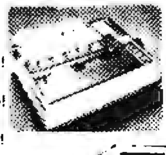

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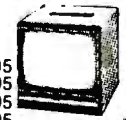

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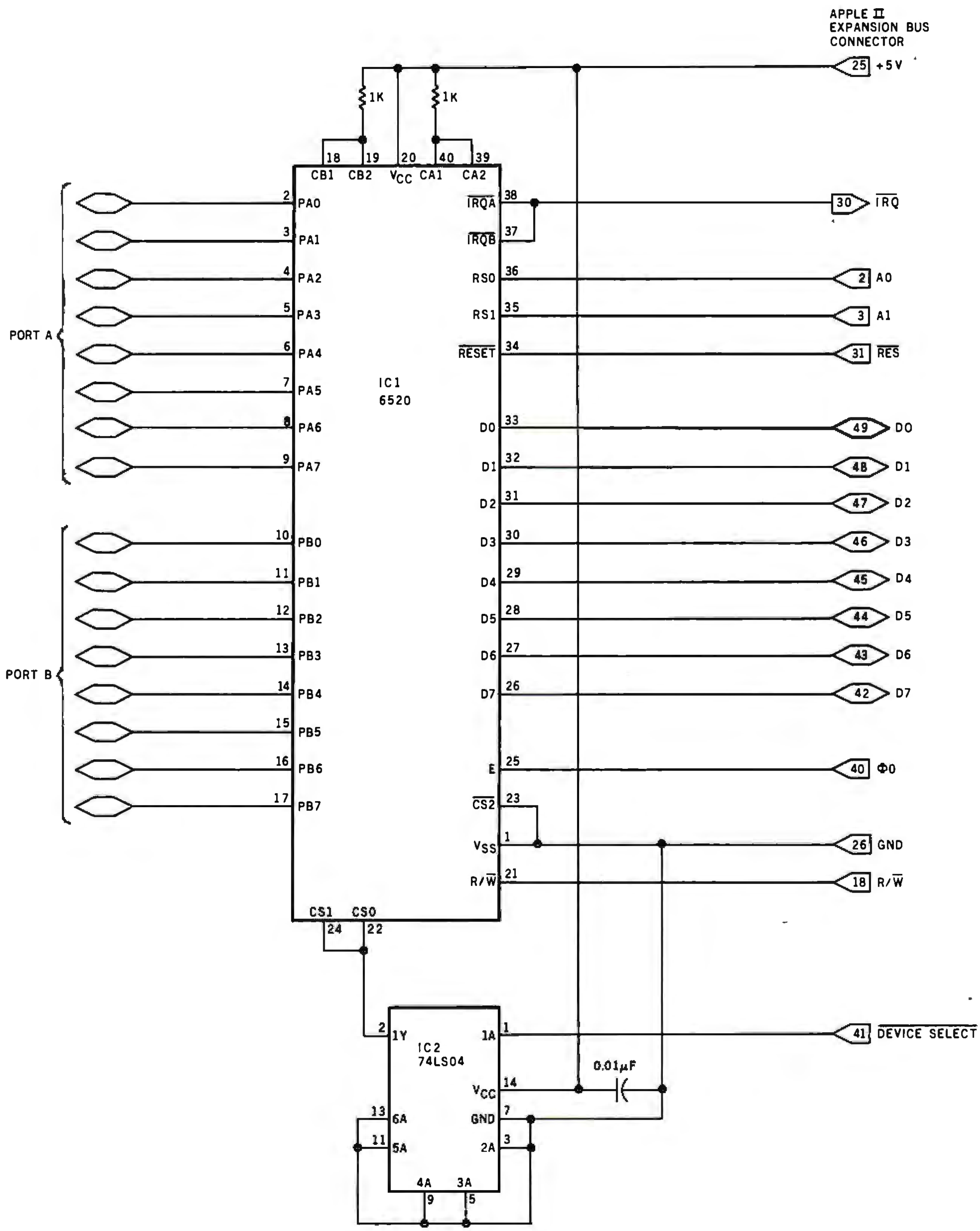

Figure 1: *Interfacing an Apple II to a 6520 peripheral interface adapter. The active-low select line of the 6520 is tied to ground while both active-high select lines are connected via an inverter to* $\overline{\text{Device Select}}$ *(an active-low signal generated by the Apple II that enables one of its eight peripheral positions).*

2a

2b

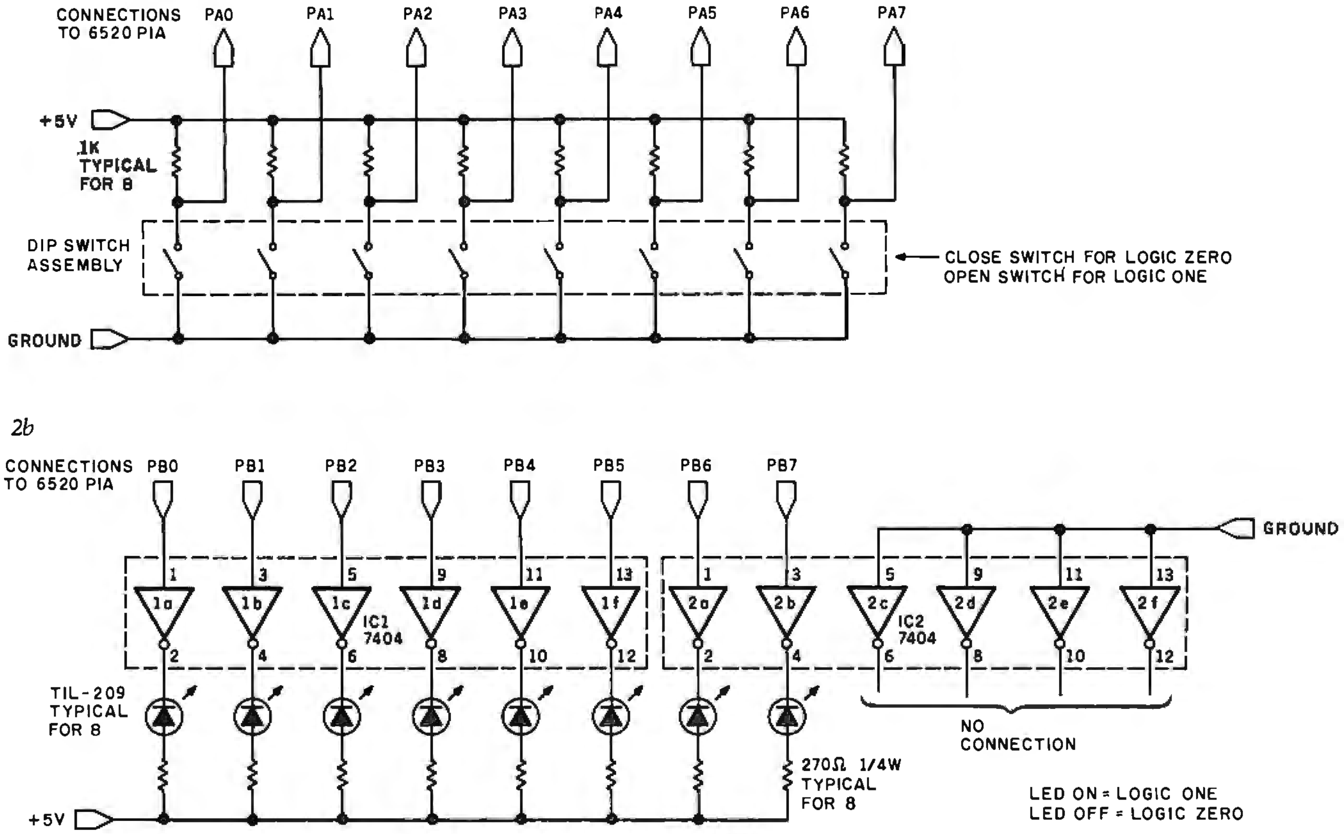

Figure 2: *Controls and indicators for testing the circuit of figure 1. Figure 2a diagrams a method for manually setting the logic conditions on one port of the 6520. Figure 2b shows a circuit that indicates the logic state of each bit in one port of the 6520.*

Number	Type	+5 V	GND
IC1	7404	14	7
IC2	7404	14	7

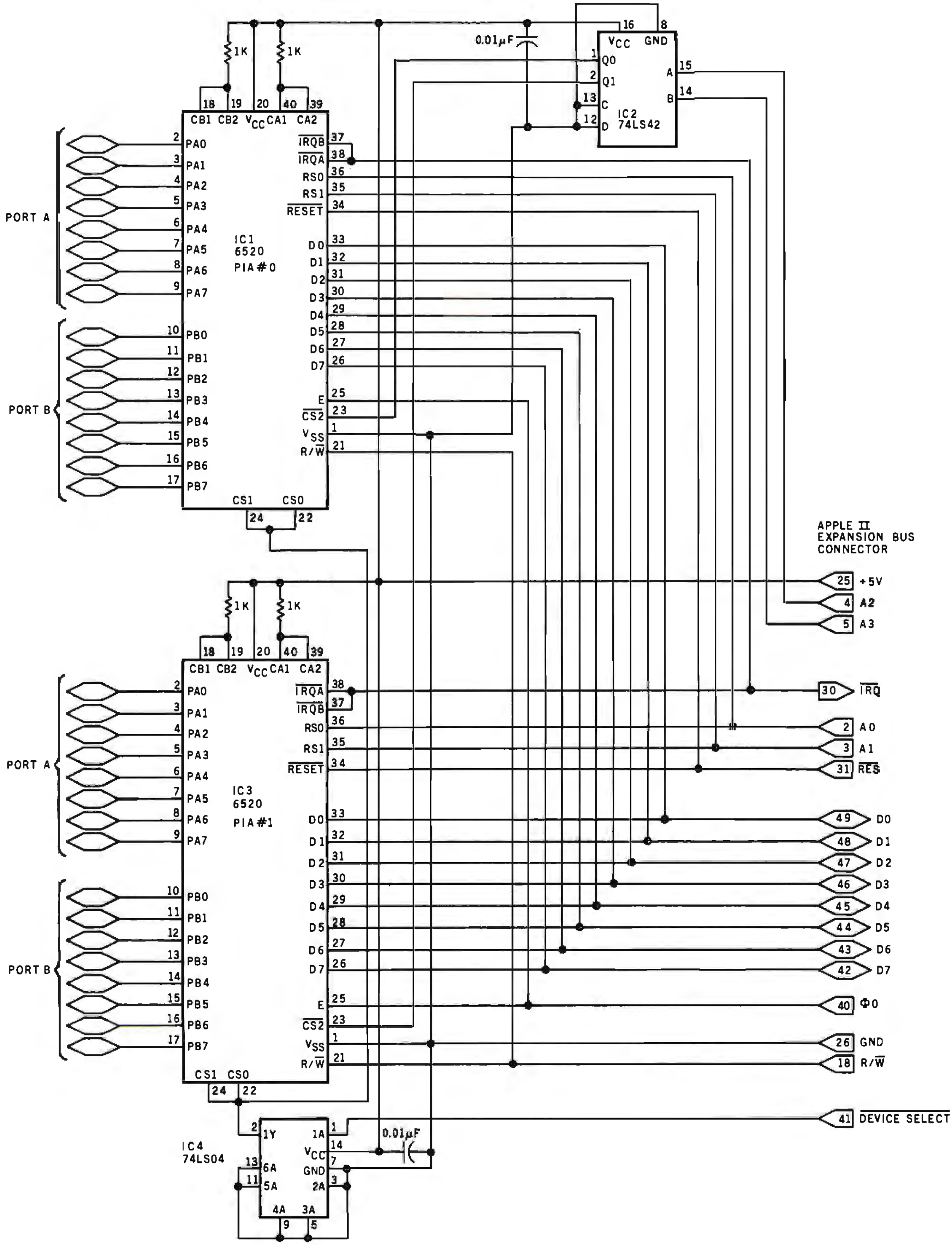

Figure 3: *The addition of a 74LS42 decoder allows more than one 6520 to be addressed by a single Apple II expansion port.*

SD Systems' Z80 Starter Kit

Wayne Angevine
1124 West 29 St. Apt. 4
Los Angeles, CA 90007

SD Systems' Z80 Starter Kit came out in 1979. It is a single-board computer comparable to the KIM-1 (formerly manufactured by MOS Technology) and to the evaluation kits offered by microprocessor manufacturers, particularly Intel's SDK series and Motorola's MEK systems. Such systems are a good beginning for computer enthusiasts who have a limited budget but desire to get involved with microcomputer hardware and machine-level software.

I chose the Z80 Starter Kit because of its Zilog Z80 microprocessor and its expandability. The Z80 is more powerful and potentially faster than Intel's 8080 processor and yet is compatible with 8080 software. Therefore, it can run Digital Research's CP/M, the de facto standard microcomputer disk operating system. It can also be easily interfaced to the S-100 bus. The kit has space for mounting two S-100 circuit boards (connectors are not included). Since I eventually hope to put together a business-type computer system with disk mass storage, the kit seemed like a good place to start.

The Z80 Starter Kit has two other important features that influenced my decision. It can program EPROMS (erasable programmable read-only memories) such as the 2716 and 2758 that require only a single +5 V power supply. No other single-board computer that I know of includes this feature; and the Starter Kit includes enough blank area for prototyping circuitry.

At a Glance

Name
Z80 Starter Kit

Manufacturer
SD Systems
POB 28810
Dallas TX 75228
(214) 340-0303

Price
$401, kit
$531, assembled

Dimensions
12.9 by 32.2 cm
(8¼ by 12¹¹⁄₁₆ inches)

Processor
Z80, 8-bit

System Clock Frequency
1.9968 MHz

Memory
1 K bytes supplied

Mass Storage
Interface for cassette-tape recorder

Features
S-100-like bus, custom wire-wrap area on circuit board, EPROM-programming circuitry

Software Included
ZBUG monitor

Hardware options
Requires external power supply

Audience
Persons interested in learning about small microcomputer systems, persons who need a dedicated controller for custom circuitry

About the Author

Wayne Angevine graduated recently from the University of Colorado at Boulder and is an electronics engineer for Hughes Aircraft Company, where he works on research and development of infrared detector arrays. He is also pursuing a master's degree in electrical engineering at the University of Southern California. He became enthusiastic about personal computers while taking a course in microprocessors, but has been using computers since the seventh grade. His other interests include hiking and cross-country skiing.

Assembly

The Z80 Starter Kit is available either as a kit or assembled. I chose the kit version to save money and become more familiar with the design. The assembly was straightforward and took about six hours. The instructions provided were clear and concise; the only problem I had was in mounting the switches for the keyboard.

Each switch assembly consists of four switches in a row, with two pins per switch; two small threaded studs protrude from the bottom of each assembly. The pins are short and somewhat springy, and aligning eight of them with the appropriate holes in the printed-circuit board is a challenge indeed. To add to the difficulty, the studs for mounting the switch assemblies are barely long enough to be gripped by the nuts provided. Only after considerable effort did the assemblies finally end up in place.

A good section on how to solder is included in the back of the instruction manual, but this kit is not recommended for a person who has never constructed a kit before. Most of the soldering involves sockets for integrated circuits, but there are lots of sockets and plenty of chances to make solder bridges from one pin to another.

All the parts of the starter kit are high quality: the printed-circuit board is a very heavy, double-sided card with a green solder mask and clearly printed component locations and numbers. As previously noted, the keyboard is made up of blocks of real switches (as opposed to the membrane or calculator-type keyboards of other units). The keys are big enough to be easy to use.

The only modification that I made was the addition of

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2	+16 V	+16 V	27	RFU		52	−16 V	−16 V	77	pWR*	
3	XRDY		28	RFU		53	GND		78	pDBIN	
4	VI0*		29	A5	A5	54	SLAVE CLR*		79	A0	A0
5	VI1*		30	A4	A4	55	DMA0*		80	A1	A1
6	VI2*		31	A3	A3	56	DMA1*		81	A2	A2
7	VI3*		32	A15	A15	57	DMA2*		82	A6	A6
8	VI4*		33	A12	A12	58	sXTRQ*		83	A7	A7
9	VI5*		34	A9	A9	59	A19		84	A8	A8
10	VI6*		35	DO1/DATA1	D1	60	SIXTN*		85	A13	A13
11	VI7*		36	DO0/DATA0	D0	61	A20		86	A14	A14
12	NMI*		37	A10	A10	62	A21		87	A11	A11
13	PWRFAIL*		38	DO4/DATA4	D4	63	A22		88	DO2/DATA2	D2
14	DMA3*	+5 V	39	DO5/DATA5	D5	64	A23		89	DO3/DATA3	D3
15	A18		40	DO6/DATA6	D6	65	NDEF		90	DO7/DATA7	D7
16	A16		41	DI2/DATA10	D2	66	NDEF		91	DI4/DATA12	D4
17	A17		42	DI3/DATA11	D3	67	PHANTOM*		92	DI5/DATA13	D5
18	SDSB*		43	DI7/DATA15	D7	68	MWRT	sMEMW	93	DI6/DATA14	D6
19	CDSB*		44	sM1		69	RFU		94	DI1/DATA9	D1
20	GND		45	sOUT	sOUT	70	GND		95	DI0/DATA8	D0
21	RFU		46	sINP	sINP	71	NDEF		96	sINTA	
22	ADSB*		47	sMEMR	sMEMR	72	RDY		97	sWO*	
23	DODSB*		48	sHLTA		73	INT*		98	ERROR*	
24	Φ		49	CLOCK	CLOCK	74	HOLD*		99	POC*	
25	pSTVAL*	ϕ	50	GND	GND	75	RESET*		100	GND	GND

Table 1: *Signals of the IEEE S-100 standard (Task 696.1/D2) compared to the S-100 interface implemented in the SD Systems' Z80 Starter Kit. In the IEEE's nomenclature, an asterisk indicates a signal that is active in the low state.*

binding posts at the power-supply terminals. The stock kit has holes only in the circuit board, to connect the power supply. I added binding posts from Radio Shack to be able to connect and disconnect the cord from my power supply easily. I recommend the type of binding posts in which the metal connector and mounting stud are one piece. The holes on the board must be enlarged slightly by careful use of a drill. After the posts are inserted, they must be soldered to the board on the top and bottom to insure a good connection.

Use and Features

The kit has the same basic configuration as most single-board systems. User input and output are accomplished by a hexadecimal keyboard plus 12 command keys and a 6-digit 7-segment LED (light-emitting diode) display. The display has large (0.6 inch), bright digits and is easy to read under normal lighting.

An audio-cassette interface is supplied. I have used it with an inexpensive Superscope recorder and have found the combination to be highly reliable—I have had only one misload in three months' use. The volume-level indicator, which allows the recorder volume level to be set properly, helps ensure the reliability. The interface uses Kansas-City-Standard coding and the Intel hexadecimal format.

The kit comes with 1024 (1 K) bytes of programmable memory in the form of eight 2102 static memory devices. There is space on the board, and all decoding circuitry is in place, for adding another 1 K bytes of 2102s, but no sockets are provided. However, sockets and integrated circuits can be added for $10 to $15.

The system monitor uses the top 110 bytes of installed memory as a scratch pad, but the remaining memory is

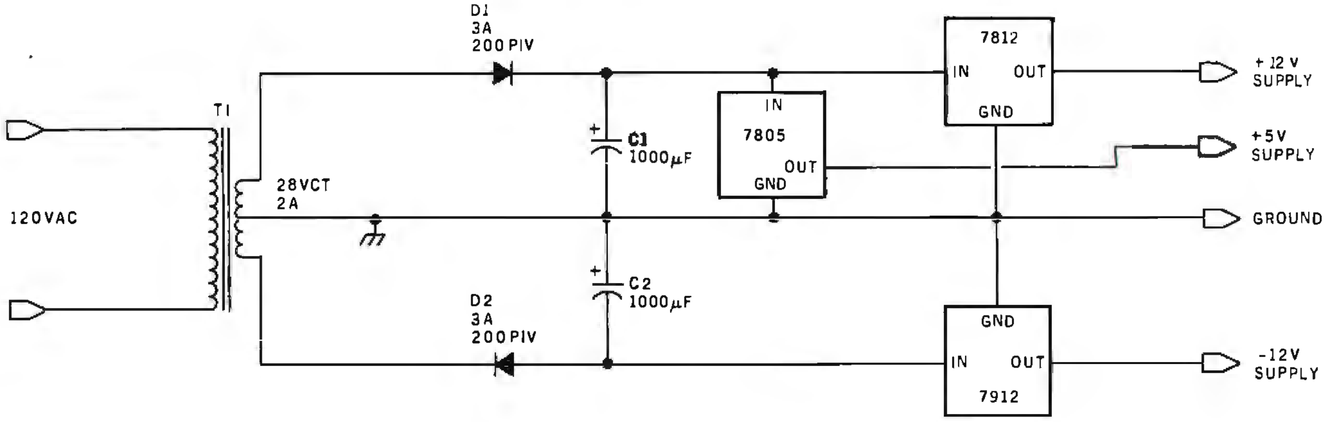

Figure 1: *Simple and inexpensive power supply for the Z80 Starter Kit. It will provide +5 V at 1 A and ±12 V at 200 to 300 mA for the Z80 Starter Kit and user circuitry. Parts used include: T1: 120 VAC primary, 28 VAC center-tapped secondary, 2 A; D1, D2: 3 A, 200 V PIV silicon diodes; C1, C2: 1000 µF, 50 V electrolytic capacitors (note polarity carefully); 7805: +5 V, 1.5 A voltage regulator; 7812: +12 V, 1.0 A voltage regulator; 7912: −12 V, 1.0 A voltage regulator.*

big enough for most uses. There are also three 22-pin sockets on the board for read-only or erasable read-only memory. One of these sockets is occupied by the system monitor. Of the remaining two, one is the programming socket, but it can also be used in a read-only mode. Each socket is selected by decoding circuitry to occupy 2 K bytes in memory-address space and wired for the pin arrangement of 2716-type devices.

One of the biggest selling points of the kit is the on-board S-100 interface. Space for two connectors is provided, although the connectors themselves are not. Technically, however, the interface is not S-100 compatible. The manual says that it is "compatible with general static memory or I/O expansion cards" but "specifically...not with the Expandoram modules." Expandoram is SD Systems' series of dynamic-memory cards. A comparison with the IEEE (Institute of Electrical and Electronics Engineers) S-100 standard shows that only 45 of the Starter Kit's 100 pins carry the signals specified. Many of the unconnected pins are not vital, such as extended addressing and the 16-bit request and acknowledge lines. Others are of more interest, such as DMA (direct memory access) and interrupts. No DMA or interrupt lines are present in the interface as wired. The most significant of the missing signals, however, are the pSYNC, pDBIN, and sM1 timing signals, which are used to implement "invisible" refresh in dynamic-memory boards. It should also be noted that it is not possible to issue a RESET signal to any boards in the S-100 slots. Table 1 gives a comparison of the IEEE S-100 standard and the on-board signal lines.

Also, some confusion exists about clock signals, as pins 24 and 25 in table 1 show. The master bus-timing signal, which the board designers call Φ, is routed to pin 25 of the S-100 interface. The standard specifies pin 24 for Φ and pin 25 for pSTVAL* (the status-valid strobe). However, SD Systems' dynamic-memory boards require clock signal $\phi 1$ on pin 25 and $\phi 2$ on pin 24. I suggest that anyone who plans to use any boards requiring clocks be careful of this.

These difficulties may be overcome, however, if the user has the patience and skill to construct the needed signals from timing diagrams and design the logic to produce them. The logic can then be constructed in the wire-wrap area and the signals routed to the S-100 connectors.

Another problem with the S-100 interface on the starter kit is that the address and data-bus lines are unbuffered. The Z80 processor can safely drive four LS TTL (low-power Schottky transistor-transistor logic) inputs. Many of the address lines are already connected to a

decoder, so they can drive only three more input loads. A high-quality S-100 board will not present more than one load to the bus. If two such boards are present in the S-100 expansion slots, make sure that no more than one load for each line is present in circuitry in the wire-wrap area. The data bus is already driving two loads, so you must be very careful about loading it at all in the wrap area.

There are no restrictions on the number of MOS (metal-oxide semiconductor) loads, such as memory devices or LSI (large-scale integration) peripheral-interface integrated circuits, since such devices present negligible load to the signal buses.

Care must also be taken in using any old boards that have standard TTL, since the processor can drive only one such load. You may have to add supplementary buffering components.

The wire-wrap area is a fairly sizable section of the printed-circuit board, containing holes that mate with standard-pattern DIP (dual-inline packages). Each hole has a solder pad; power and ground buses are available on both sides of the board. The useful signals, 70 in all, are brought out to this area.

For my purposes, the wire-wrap area has two disadvantages. It is too small, and I dislike the idea of continually turning the board upside down to wire and check circuitry—both wiring mistakes and damage to the components already on the board are likely to result. I plan to use 44-pin connectors and standard circuit boards to alleviate these problems.

The on-board EPROM programmer is a strong feature of this system. It will program type-2716 and 2758 which require other supply voltages). In stock trim, the system is capable of programming only 914 bytes, since that is all the user-programmable memory available. However, a program is provided to allow the data to be programmed to reside in any area of memory. This would allow programming from any user-installed memory, and copying read-only memories from the spare socket to the programming socket. One suggestion for those planning to use the starter kit for large-scale read-only memory programming would be to install a ZIF (zero-insertion-force) socket in place of the provided programming socket. This would prevent bent pins and other such damage incurred in prying the programmed device out of the socket.

Some interface capability is built into the Z80 Starter Kit, in the form of a Z80 PIO (parallel input/output) and Z80 CTC (counter/timer circuit) components. The Z80 PIO is a parallel interface circuit similar to the Intel 8255 and Motorola 6820. It has two 8-bit I/O ports with two handshake lines each, and it can be configured in several ways by the use of programmable registers.

The Z80 CTC is a counter and timer circuit (it also is programmable). It has four channels, three of which are used by the kit for timing functions in the read-only-memory programmer and cassette interface. One channel is available to the user. When properly programmed, the

counter will divide the system clock by a 16-bit value and produce a pulse train or interrupt signal.

I should also note that the processor is a 2 MHz Z80, not a 4 MHz Z80A. The precise clock rate is 1.9968 MHz.

The kit features a switch-selectable automatic restart for those interested in dedicating the unit to a particular application. After a system reset, the monitor examines a switch that chooses whether the normal monitor program or the program in the number-1 read-only-memory socket should be executed. This allows the system to run without operator intervention after reset.

System Monitor

The system monitor supplied with the Z80 Starter Kit is called ZBUG. It is a fairly sophisticated program residing in a 2 K-byte read-only memory. The monitor provides the following command functions:

- Return to Monitor
- Examine Memory
- Examine Port
- Examine Register
- Set Breakpoint
- Single-Step
- Execute
- Dump Memory Contents to Cassette
- Load Memory from Cassette
- Program EPROM
- Next (repeat last operation for next location)

Each function is activated by a single key on the keypad.

With one exception, the ideas behind each of these functions should be obvious. Return to Monitor causes the executing program or other monitor function to cease and allows a new monitor command to be entered. It is supposed to be able to recover the system when an executing program is in an infinite loop.

I found that this does not always work. If a jump is executed to an unused area of memory, the monitor will not recover it. Other mistakes are possible also. In a case like this the only alternative is to reset, which scrambles the contents of memory and is generally unproductive.

The monitor has several other capabilities. One of the most important is a subroutine that calculates the offset for a relative-jump instruction. This is very useful in hand-assembling programs. Other user-callable subroutines are available to provide a 20-ms delay and to convert ASCII (American Standard Code for Information Interchange) characters to and from binary.

One hard-to-find piece of information is the address to return control to the monitor from a program. The address of this reentry point is hexadecimal 00AE.

Documentation

The *Z80 Starter Kit Operations Manual* is the main system documentation. A *Mostek Z80 Micro-Reference Manual* is also provided. It is a small booklet that gives the Z80 instruction-set mnemonics, op codes, and timing

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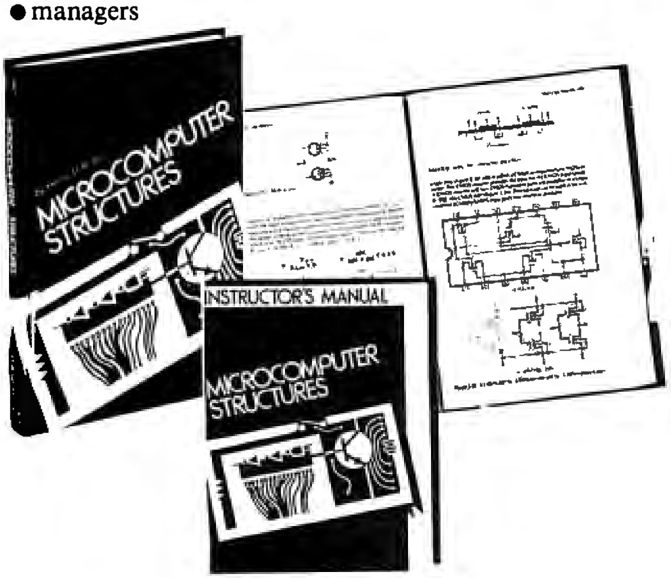

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information. It also gives a summary of Z80 PIO and Z80 CTC programming.

The *Operations Manual* is fairly well written: most of the information is presented clearly, although occasionally a useful item is buried. The best place to look for these is in the "Example Programs" section. Several programs are provided there that give an overview of the kit and help expand its usefulness. A complete schematic diagram and a complete source-code listing of the monitor are also included.

Power Supply

The manual states that the Z80 Starter Kit requires +5 V at 1 A for normal operation and an additional +25 V supply at 30 mA for read-only-memory programming. I designed the power supply shown in figure 1 to provide the +5 V, as well as power for linear semiconductor devices in the wire-wrap area at ±12 V. All parts but the voltage regulators are available from Radio Shack. The regulators can be acquired at most electronics supply houses or by mail from any of several BYTE advertisers. Be sure to mount the regulators on heat sinks, and don't be surprised if they become warm. The supply will put out 1 A at +5 V and 200 to 300 mA at ±12 V. The +25 V supply for EPROM programming can be provided by three 9-V transistor-radio batteries in series, since the current requirement is so small and the duration of use is short.

Summary

If you are looking for a single-board computer that can be expanded and run 8080 or Z80 software, the Z80 Starter Kit is a good choice. You should also consider it for practical applications such as home security and small-scale industrial or laboratory control, and as an inexpensive stand-alone EPROM programmer.■

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COSMAC EPROM Programmer

Dan Rubis
POB 402
St. Clair Shores, MI 48080

Programming an EPROM (erasable programmable read-only memory) has become much easier in recent years. The old-style 2708 EPROMs (1 K by 8 bits) required +26 volts (V) to be turned on and off 100 times for each byte programmed—a total programming time of 100 milliseconds (ms) per byte. A 2708 programmer was a complex device that often relied on adherence to close timing specifications and used switching transistors. It was also necessary to program the whole device at once—unprogrammed addresses contained invalid data and could not be programmed until the entire device was erased.

The newer 2716 (2 K by 8 bits) and 2732 (4 K by 8 bits) EPROMs, on the other hand, use only +5 V on the programming pin (a +25 V supply *is* necessary, though). A single byte at any address can be programmed in 50 ms. Under certain circumstances, you can even program one bit of a byte.

These features make EPROM programming possible with a relatively simple circuit connected to a microprocessor. This article describes an EPROM programmer, based on the RCA COSMAC 1802 microprocessor, which is designed for the not-so-affluent computer enthusiast. (Projected cost for the programmer circuitry is about $30, and single-board 1802 computers are available for about $100. Considering that industrial programmers cost thousands of dollars, this is an outstanding value.) The approach I have taken should allow any 1802 computer to be used.

Design Basics

This is a "bare bones" design, without many protective hardware features, and so a certain amount of care and attention to detail is required: a goof-up could cost you the price of an EPROM. The key here is simplicity; hence the use of the 1802. The 1802 excels in control applications and will provide the address, data, and control signals, as well as perform all the timing functions of the programming process.

Programming a 2716 or a 2732 is quite similar to programming a 2708, the main difference being the storage size. If your computer has only 4 K bytes of programmable memory, any 2732s you program will have to be done in two 2 K-byte segments. The biggest advantage of the new-style EPROMs is the simpler programming process: all that is required to program a byte anywhere in the address space is one 50-ms pulse.

Figure 1 illustrates how the 1802 computer functions as the controller. The computer's programmable memory will hold the data to be programmed into the EPROM. With appropriate software, the computer will supply address and data to their respective latches. Then the control lines of the computer will signal the latches to hold the address and data. The output of each latch is applied to the appropriate pin on the target EPROM.

The computer then applies a control signal (programming pulse) to the EPROM. This pulse signals that the data information is ready and that it should be programmed into the memory location as specified by the address. Three conditions are necessary to successfully program a byte of data into the EPROM:

1. The address location must be applied to the correct pins of the EPROM (A0 through A10).
2. The data byte must be applied to the output pins of the EPROM (O0 through O7).
3. A programming pulse of 50 ms must be applied to the programming pin of the EPROM (PGM).

Notice the two 24-pin integrated circuits (IC3 and IC4) marked CDP-1852 in the circuit diagram (figure 2a). These are RCA CMOS (complementary metal-oxide semiconductor) 8-bit I/O (input/output) ports, which will be used in their output mode as latches.

The memory locations of a 2716 are addressed in the range from 000 through 7FF hexadecimal and therefore require eleven address bits. One

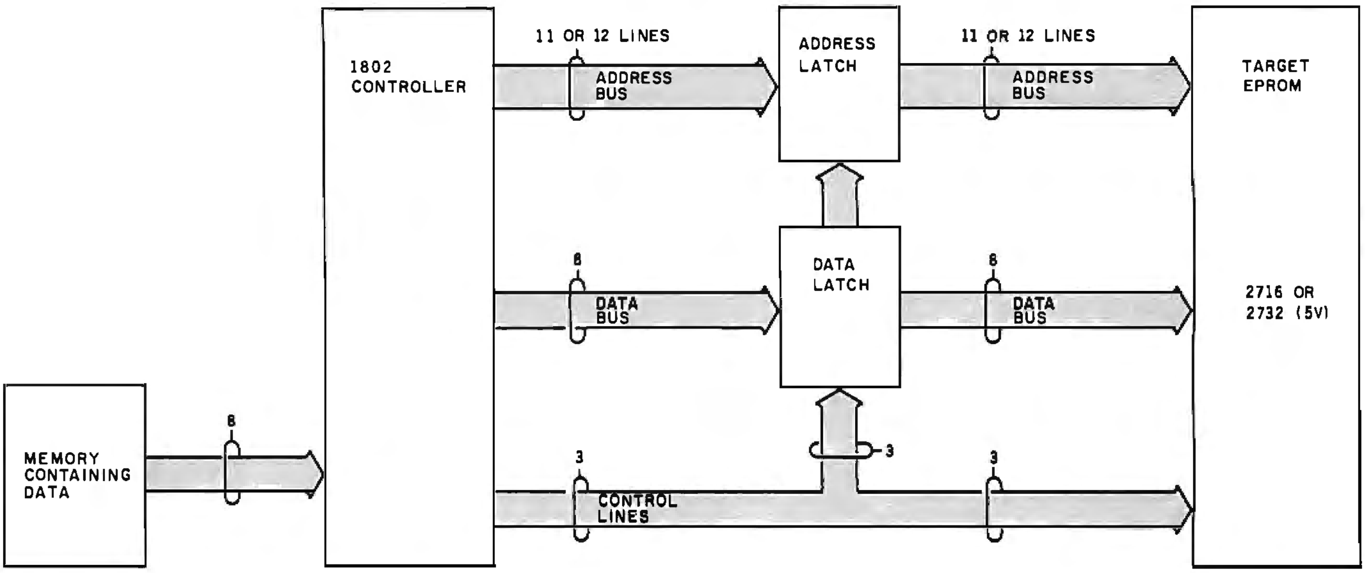

Figure 1: *A block diagram of the EPROM-programmer system. The 1802 microprocessor provides address and data signals to latches, then, through the use of various control signals, releases the information from the latches at the proper time to program the EPROM.*

1852 8-bit latch is not large enough; an additional CD-4042 4-bit latch (IC2) is needed. Also notice that the 1852 has two device-select pins, $\overline{CS1}$ and CS2, and a clock pin. These pins are used to latch the address at the appropriate time. The 4042 is a simple latch and does not have select pins; it is necessary to include a CD-4011 quad NAND gate to help select the latch. See figure 3 for the pin assignments of the CDP-1852, CD-4042, and CD-4011.

The programming data is only 8 bits wide, and, therefore, only one 1852 (IC4) is required for latching. Refer to figure 2a for information on how it is connected to the EPROM.

The 2732 has slightly different pin designations. The A11 address bit is assigned to pin 21, and V_{pp} now shares the output enable (OE) pin 20. A11 has to be accommodated in order for the EPROM to address 4 K bytes of memory. This is the dashed line in figure 2a.

If you plan on programming both 2716s and 2732s, a switch will have to be provided; otherwise jumper wires will do nicely.

Power Supply

The schematic for the 5-V power supply is shown in figure 2b. Its input comes from a well-filtered +8-V source, such as a transformer/bridge-rectifier/capacitor combination. The +25-V programming power supply (figure 2c) is a full-wave rectified 24-V AC transformer, filtered by a 3500 μF capacitor and regulated by an LM 340-24 positive voltage regulator. In order to meet the +25-V requirement using a +24-V regulator, a diode (1N914) is placed in series with the ground reference pin of the regulator. The diode represents about a 0.6-V drop and therefore brings the ground reference of the regulator up from 0 V to 0.6 V. The output of the regulator will therefore be 0.6 V closer to the required voltage. The manufacturer allows a tolerance of ±1 V on the programming voltage, and the added diode puts the voltage within this tolerance.

Timing

The computer has eight clock cycles of period T for every machine cycle (see the timing diagram, figure 4). A machine cycle can be either a fetch or an execute cycle. I will discuss only the programming execute cycle, OUT7 (67). This instruction transfers data from the computer's programmable memory to the data bus.

An OUT7 instruction asserts a logic 1 level on each of the N2, N1, and N0 status lines. In this design, N2 is used to signal the latches when to hold the address and data.

N2 stays at logic 1 during the entire execute cycle. When N2, TPA (line 3), and $\overline{MRD}$ (line 5) are logic true (1, 1, and 0, respectively), the high-order address byte A1 is on the bus and is ready to be latched (see line 2 at clock cycle 1.5).

Only bits A8 through A10 of the high-order address are needed for a 2716 EPROM. These three bits are latched by the 4042. In order to latch them at the correct time, TPA and N2 are ANDed together using the 4011 NAND gates. When both TPA and N2 are at logic 1, the $\overline{STROBE}$ pin of the 4042 latch will be at logic 1. This allows the outputs of the latch to follow the inputs; what appears at the latch's inputs also appears at its outputs. When TPA goes from logic 1 to logic 0, this negative transition essentially freezes the outputs of the latch until a subsequent positive transition (0 to 1) occurs. Another positive transition of the $\overline{STROBE}$ pin will not occur until after the 50-ms programming pulse has been completed (see lines 2, 3, 6, and 7 of the timing diagram, figure 4).

Further down the execute cycle, the low-order bits A0 through A7 are available on the address bus starting at 2.5 on the clock cycle (A0). TPB goes positive at clock cycle 6.5, and

Text continued on page 352

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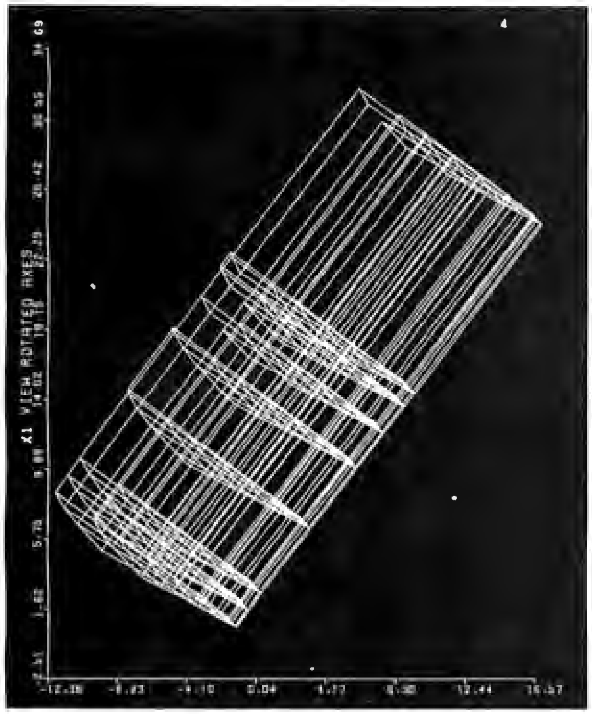

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IC2	CD4042	16	8
IC3	CDP1852	24	12
IC4	CDP1852	24	12

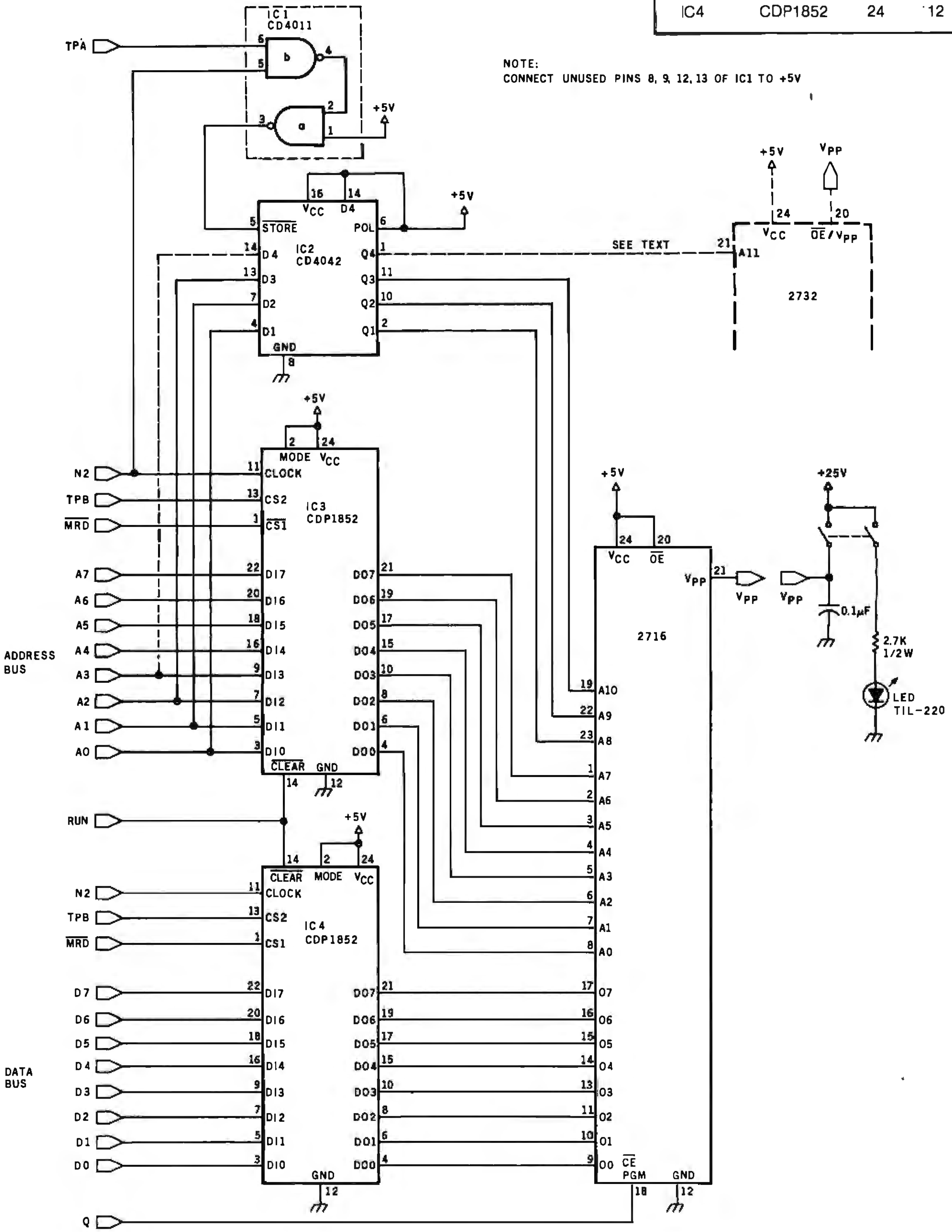

Figure 2a: *A schematic diagram of the EPROM programmer, which illustrates the use of one 1852 8-bit latch (IC4) to hold the data that will be programmed into the EPROM. An 1852 and the combination of a 4042 latch and a 4011 NAND device are used to hold up to 12 address bits.*

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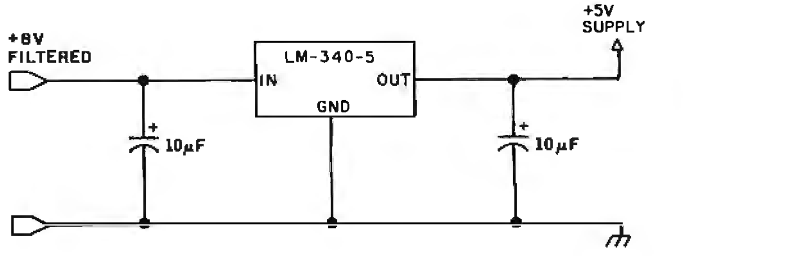

Figure 2b: *A +5-V supply is developed from the computer's +8-V unregulated source.*

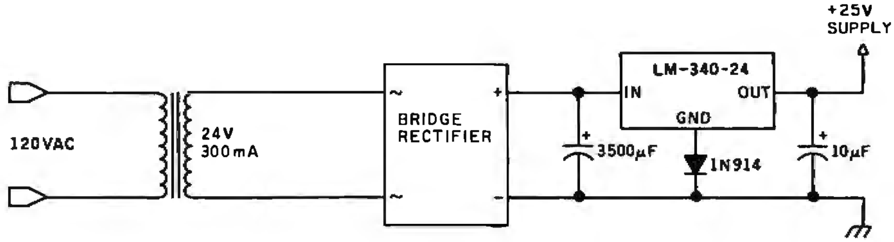

Figure 2c: *A +25-V supply provides programming voltage. A +24-V regulator is used in conjunction with a diode to produce +24.6 V—well within the ±1-V tolerance specified by EPROM manufacturers.*

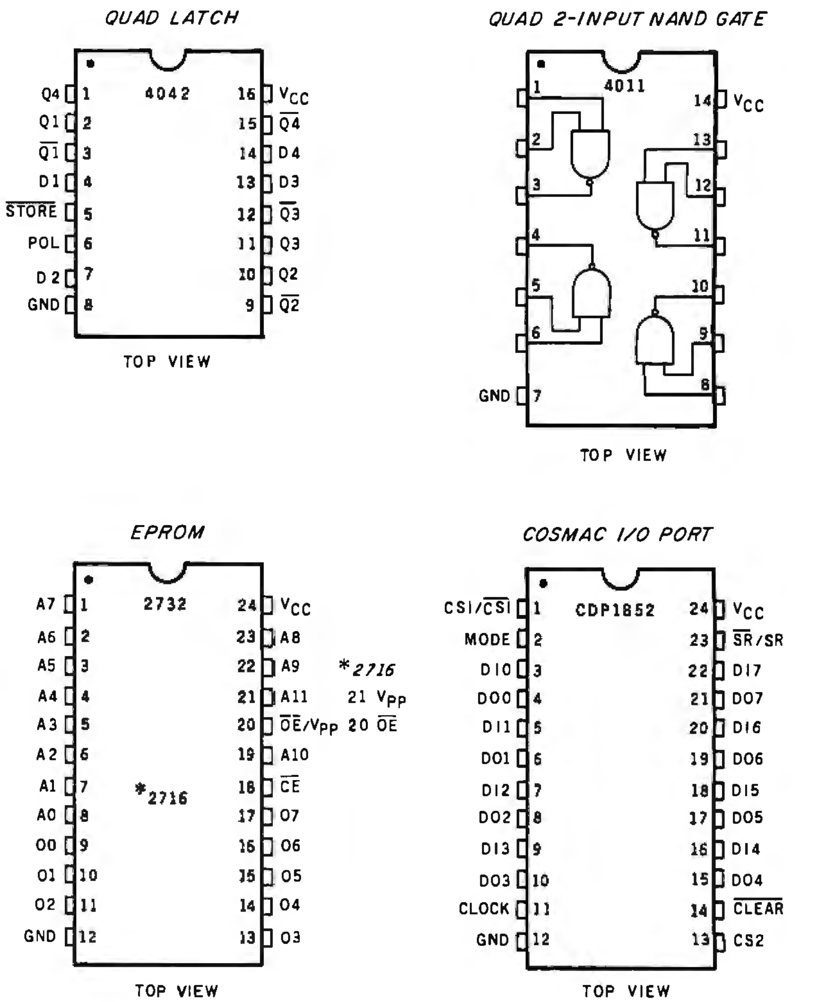

Figure 3: *Pin assignments of the various integrated circuits used in the EPROM programmer.*

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Text continued from page 346:
when TPB, $\overline{MRD}$, and N2 are logic true, the 1852 8-bit latch "knows" that the low-order address byte is on the bus and is ready to be latched. Likewise, the 1852 will stay latched until TPB, $\overline{MRD}$, and N2 are logic true again.

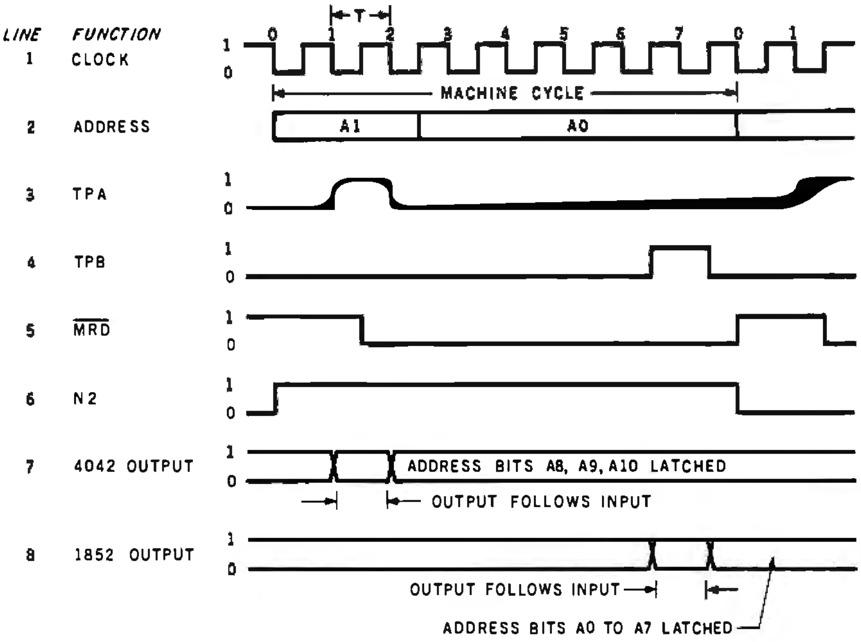

Figure 4: *The 1802 timing diagram is broken into eight T-cycles. A machine cycle can be either a fetch or an execute cycle; the diagram here shows the execute phase and the timing relationship of the control signals.*

Now that the complete address is latched, the same procedure is used for the data byte. The data is available on the data bus when N2 goes positive. By using TPB, $\overline{MRD}$, and N2, we can latch the data at the same time as the low-order address. Again, this data will be held until another logic-true condition appears on the device-select lines.

The outputs of these three latches are applied to the appropriate pins on the target EPROM. With +25 V applied to V_{pp}, it is only necessary to apply a 50-ms logic 1 pulse to the programming pin on the EPROM for a 2716 and a logic 0 pulse for a 2732.

The generation of the programming pulse will be accomplished by programming the 1802's 1-bit Q output port. The Q line can be set or reset with the SEQ and REQ instructions. The Q line will go to logic 1 or logic 0 respectively. By timing the Q line setting and resetting with a 50-ms delay loop, we can use the Q line to control the EPROM programming pulse.

The Program

The program has to accomplish several objectives:

1. Supply the address and data to the bus.
2. Furnish control signals to the latches.
3. Perform address bookkeeping chores of start, current, and finish addresses.
4. Fulfill programming pulse timer requirements.

(See listing 1 for the program and figure 5 for a flowchart of the program. The flowchart is annotated with numbers that correspond to line numbers of the program listing.)

The delay constants in lines 25 and 27 of the program were calculated using the following formula:

$$\text{delay machine cycles} = \frac{DT \times f}{8}$$

where f = clock frequency = ½ crystal frequency, DT = delay time, and 8 clock cycles = 1 machine

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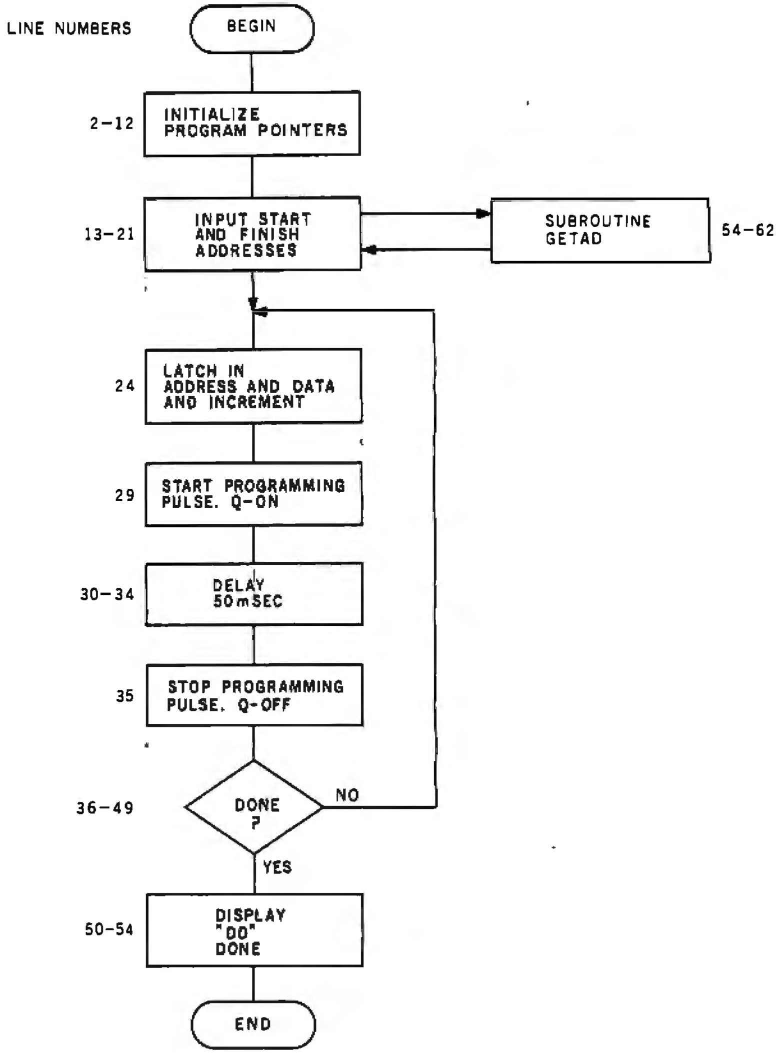

Figure 5: *A flowchart of the program for controlling the 1802. The numbers to the left of the box symbols correspond to program line numbers.*

cycle. In a common system, the system clock is developed from a video color-burst crystal (3.579545 MHz).

The inner delay loop consists of program lines 30, 31, and 32, for a total of six machine cycles for each time through the loop. The outer loop goes from line 30 to 34, for a total of ten machine cycles each time. The correct delay constants can be determined by the following formula:

$$[6n + 6(m - 1)(256)] + [10(256)] = 11{,}186$$

where mn = 16-bit delay constant (m is the high-order byte, n is the low-order byte). The series of terms enclosed in the first set of brackets accounts for the inner loop, those in the second set for the outer loop. Solving for mn gives hexadecimal 69E ($m = 6$, and $n = 157$).

Programming the EPROM

The following is the procedure for programming 2 K bytes of a 2716 EPROM:

1. Using an ultraviolet light source, erase the EPROM to set all bits equal to a logic 1. **Caution:** *The ultraviolet rays seem harmless, but they are not. Do not expose your eyes to the rays, and keep others from inadvertently walking into the area while you are erasing.*
2. Verify that each memory location of the EPROM is filled with FF hexadecimal. Use the program in listing 2.

Text continued on page 362

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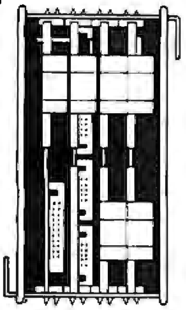

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Listing 1: *Program instructions for controlling the COSMAC microprocessor to program a 2716 EPROM. To program a 2732 EPROM, the mnemonic REQ (7A) in lines 2 and 35 should be changed to SEQ (7B) and SEQ (7B) in line 29 should be changed to REQ (7A).*

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ADD.	CODE	LINE NO.	LABEL	ASM	REGIS. OPERND	COMMENT
0100		1		ORG	0100	: ORIGIN
0100	7A	2		REQ		:INITIALIZE Q = 0
0101	F801	3		LDI	01	:INITIALIZE POINTERS
0103	B2	4		PHI	R2	: STACK HI
0104	B3	5		PHI	R3	: PROGRAM COUNTER HI
0105	B6	6		PHI	R6	: SUBROUTINE GETAD HI
0106	F8FF	7		LDI	FF	:
0108	A2	8		PLO	R2	: STACK LO
0109	F8A1	9		LDI	A1	:
010B	A6	10		PLO	R6	: GETAD LO
010C	F810	11		LDI	10	:
010E	A3	12		PLO	R3	: PRG COUNTER LO
010F	D3	13		SEP	R3	:PROGRAM COUNTER NOW R3
0110	D6	14		SEP	R6	:CALL GETAD
0111	B7	15		PHI	R7	:HI START ADDRESS
0112	D6	16		SEP	R6	:CALL GETAD
0113	A7	17		PLO	R7	:LO START ADDRESS
0114	D6	18		SEP	R6	:CALL GETAD
0115	B8	19		PHI	R8	:HI FINISH ADDRESS
0116	D6	20		SEP	R6	:CALL GETAD
0117	A8	21		PLO	R8	:LO FINISH ADD*PLUS ONE*
0118	D6	22		SEP	R6	:WAIT FOR INPUT PRESS
0119	E7	23	BEGIN	SEX	R7	:SET X TO START ADD
011A	67	24		OUT	#7	:LATCH ADD AND DATA
011B	F806	25		LDI	06	:LOAD DELAY CONSTANTS
011D	BD	26		PHI	RD	: " " "
011E	F89E	27		LDI	9E	: " " "
0120	AD	28		PLO	RD	: " " "
0121	7B	29		SEQ		:START PROGRAMMING PULSE
0122	2D	30	DELAY	DEC	RD	:DECREMENT DELAY COUNTER
0123	9D	31		GHI	RD	:CHECK TO SEE IF FINISHED
0124	3A22	32		BNZ	DELAY	:CONTINUE IF NOT FINISHED
0126	8D	33		GLO	RD	:CHECK TO SEE IF FINISHED
0127	3A22	34		BNZ	DELAY	: "
0129	7A	35		REQ		:STOP PULSE AFTER 50 MSEC
012A	E2	36		SEX	R2	
012B	97	37		GHI	R7	:FINISHED PROGRAMMING BYTE
012C	73	38		STXD		:HI BYTE POINTER ON STACK
012D	60	39		IRX		:REPOSITION STACK POINTER
012E	98	40		GHI	R8	:LOAD HI FINISH ADDRESS
012F	F3	41		XOR		:AND COMPARE
0130	3A19	42		BNZ	BEGIN	:CONTINUE IF NOT FINISHED
0132	87	43		GLO	R7	
0133	73	44		STXD		:LO BYTE POINTER ON STACK
0134	60	45		IRX		:REPOSITION STACK POINTER
0135	88	46		GLO	R8	:LOAD LO FINISH ADDRESS
0136	F3	47		XOR		:AND COMPARE
0137	3A19	48		BNZ	BEGIN	:NOT FINISHED THEN CONTINU
0139	F8DD	49		LDI	DD	:ELSE
013B	73	50		STXD		:LOAD (DD)ONE TO SIGNAL EN
013C	60	51		IRX		:REPRO. STACK POINTER
013D	64	52		OUT	#4	:OUTPUT TO HEX DISPLAY
013E	303E	53	STOP	BR	STOP	: "THE END"
01A0		54		ORG	01A0	:**SUBROUTINE GETAD**

Listing 1 continued on page 358

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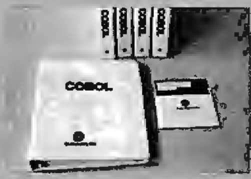

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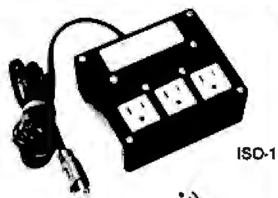
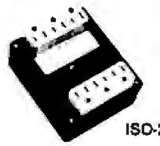

ISO-1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Listing 1 continued:

```
01A0  D3      55   RETURN   SEP   R3       :TO MAIN
01A1  E2      56            SEX   R2       :ENTRY POINT OF SUBROUTINE
01A2  3FA2    57   WAIT1    BN4   WAIT1    :FOR INPUT PRESS
01A4  37A4    58   WAIT2    B4    WAIT2    :FOR RELEASE
01A6  6C      59            INP   #C       :LOAD INPUT INTO MX,D
01A7  64      60            OUT   #4       :DISPLAY BYTE
01A8  22      61            DEC   R2       :REPO. STACK POINTER
01A9  30A0    62            BR    RETURN   :D HOLDS ADDRESS BYTE

TABLE OF LABLES USED
BEGIN    0119:DELAY    0122:STOP    013E:RETURN   01A0:WAIT1    01A2:
WAIT2    01A4:
 :
```

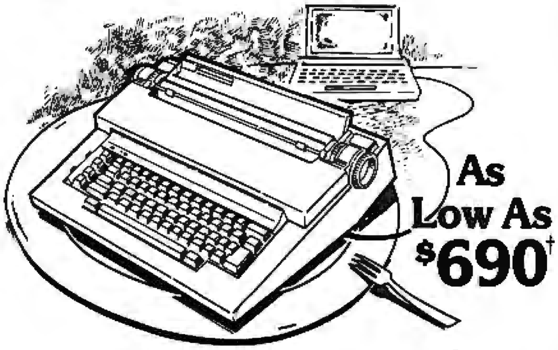
Listing 2: *A program to use the 1802 to check that an EPROM is completely erased.*

```
3/14/81        11.90      CROSS ASSEMBLER  1802 VER 1.1

ADD.   CODE    LINE   LABEL    ASM    REGIS.   COMMENT
               NO.                    OPERND
0100            1              ORG    0100     :  ORIGIN
0100   F801     2              LDI    01       :INITIALIZE POINTERS
0102   B2       3              PHI    R2       :     WORK AREA HI
0103   B3       4              PHI    R3       :     PROGRAM COUNTER HI
0104   B6       5              PHI    R6       :     SUBROUTINE  GETAD HI
0105   F8FF     6              LDI    FF       :
0107   A2       7              PLO    R2       :     STACK LO
0108   F8A1     8              LDI    A1       :
010A   A6       9              PLO    R6       :     GETAD LO
010B   F80E    10              LDI    0E       :
010D   A3      11              PLO    R3       :     PROGRAM COUNTER LO
010E   D3      12              SEP    R3       :PROGRAM COUNTER NOW R3
010F   D6      13              SEP    R6       :CALL GETAD
0110   B7      14              PHI    R7       :HI START ADDRESS
0111   D6      15              SEP    R6       :CALL GETAD
0112   A7      16              PLO    R7       :LO START ADDRESS
0113   D6      17              SEP    R6       :CALL GETAD
0114   B8      18              PHI    R8       :HI FINISH ADDRESS
0115   D6      19              SEP    R6       :CALL GETAD
0116   A8      20              PLO    R8       :LO FIN ADDRESS*PLUS ONE*
0117   D6      21              SEP    R6       :WAIT FOR INPUT PRESS
0118   E7      22     BEGIN    SEX    R7       :  START OF LOOP
0119   72      23              LDXA            :LOAD BYTE FROM EPROM
011A   FBFF    24              XRI    FF       :COMPARE WITH FF
011C   3A35    25              BNZ    BAD      :GOTO BAD BYTE D NOT 0
011E   E2      26              SEX    R2
011F   97      27              GHI    R7       :COMPARE WITH FINISH POINT
0120   73      28              STXD            :    DONE?
0121   60      29              IRX             :REPOSITION STACK POINTER
0122   98      30              GHI    R8       :LOAD HI FINISH ADDRESS
0123   F3      31              XOR             :AND COMPARE
0124   3A18    32              BNZ    BEGIN    :CONTINUE IF NOT FINISHED
0126   87      33              GLO    R7
0127   73      34              STXD            :LO BYTE POINTER ON STACK
0128   60      35              IRX             :REPO. STACK POINTER
0129   88      36              GLO    R8       :LOAD LO FINISH ADDRESS
012A   F3      37              XOR             :AND COMPARE
012B   3A18    38              BNZ    BEGIN    :CONTINUE IF NOT FINISHED
012D   E2      39              SEX    R2
012E   F8DD    40              LDI    DD       :DONE -- NO BAD BYTES
```

Listing 2 continued on page 360

HAVE YOUR CAKE AND EAT IT TOO



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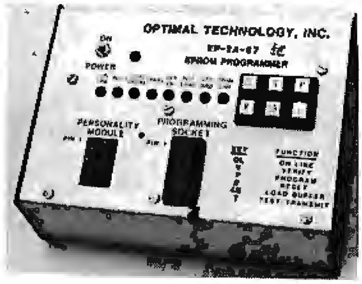

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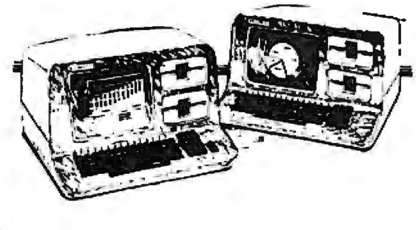

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Listing 2 continued:

```
0130  73          STXD          :LOAD (DD)ONE TO SIG END
0131  60          IRX           :REPO. STACK POINTER
0132  64          OUT    #4
0133  3033  STOP  BR     STOP   :   "THE END"
0135  E2    BAD   SEX    R2     :BAD BYTE
0136  27          DEC    R7     :POINT TO BAD BYTE
0137  87          GLO    R7     :LOAD LO ADDRESS
0138  73          STXD          :STORE ON STACK
0139  97          GHI    R7     :LOAD HI ADDRESS
013A  73          STXD          :STORE ON STACK
013B  F8EE        LDI    EE     : **ERROR**
013D  73          STXD          :LOAD (EE)RROR TO SIG ERR.
013E  60          IRX           :REPO. STACK POINTER
013F  64          OUT    #4     :OUTPUT TO HEX DISPLAY
0140  3033        BR     STOP   :   "THE END"
0A00              ORG    0A00   :**SUBROUTINE GETAD**
0A00  D3    RETURN SEP   R3
0A01  E2          SEX    R2     :ENTER SUBROUTINE HERE
0A02  3F02  WAIT2 BN4    WAIT2  :FOR INPUT PRESS
0A04  3704  WAIT3 B4     WAIT3  :FOR RELEASE
0A06  6C          INP    #C     :LOAD INPUT INTO MX,D
0A07  64          OUT    #4     :DISPLAY BYTE
0A08  22          DEC    R2     :REPO. STACK POINTER
0A09  3000        BR     RETURN : D HOLDS ADDRESS BYTE

TABLE OF LABLES USED
BEGIN    0118:STOP     0133:BAD      0135:RETURN   0A00:WAIT2    0A02:
WAIT3    0A04:
 :
```


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Text continued from page 354:

3. Load the EPROM program at 0100 to 01FF hexadecimal.
4. Load the data at 0800 to 0FFF hexadecimal.
5. Insure that the +25-V power supply is off before installing the EPROM.
6. Install the EPROM to be programmed.
7. Insure that the +5-V power supply is applied to the EPROM. Then turn on the +25-V supply.
8. Run the program loaded at 0100 hexadecimal.
9. Enter the high and low parts of the starting address of the data to be programmed.
10. Enter the high and low parts of the finish address, plus one.
11. Press input again to start programming. The program is finished when "DD" is displayed.
12. Turn off the +25-V power supply; then remove the EPROM.
13. Verify that the data was stored correctly.

The data may be loaded only from hexadecimal 0800 to 0FFF. The EPROM's memory is addressed from X000 to X7FF (or 000 0000 0000 to 111 1111 1111 in binary). Only the least-significant 11 bits are required. The only address space in a 4 K-byte system that meets this requirement is from 0800 to 0FFF (or 1000 0000 0000 to 1111 1111 1111). The 1802's address space from 0000 to 07FF is where its own program is stored in memory.

If you like, you can program just one bit of a byte. When you are programming a byte of data into the EPROM, you are actually programming zeros into the required bit positions of the byte. For example, take the data value 4F hexadecimal (0100 1111 in binary). A zero is programmed into bit positions 7, 5, and 4, while bits 6, 3, 2, 1, and 0 remain at logic 1. Any of the logic 1 bits can be programmed to logic 0. The byte 4F can be changed to 42 (or 0100 0010) because the only bits changed were the logic 1 bits. The only way to change a logic 0 bit to a

Circle 282 on inquiry card.

Circle 345 on Inquiry card.

Circle 320 on inquiry card.

logic 1 is by ultraviolet erasing, and this necessarily means erasing the entire EPROM.

The manufacturer recommends that V_{pp} (+25 V) should always be applied to the EPROM after V_{cc} (+5 V) has been applied. If you adhere to the instructions numbered 5, 6, 7, and 13 closely, there should be no problems.

Construction

Construction of the programmer can be accomplished in several ways but a single-sided printed-circuit board is probably the easiest. The positive photographic system for etching your own boards is recommended because one of the photographic steps is eliminated.

Those who do not have access to an industrial EPROM eraser can make their own. An ultraviolet tube can be purchased at just about any barber-shop supply house. The General Electric number G15T8 is a 15-inch tube that fits nicely into a fluorescent desk-lamp fixture. Place the EPROM about an inch or two away from the tube, and expose it for about one half an hour. Again, be sure to avoid exposing your eyes to ultraviolet rays.

Owners of ELF II computers should be aware that the monitor included with the Giant Board uses the highest two bytes of programmable memory for its own work space. Anyone with only 4 K bytes of memory located at 0000 to 0FFF should take care not to jump to the monitor after loading the EPROM data at 0800 to 0FFF, because bytes 0FFD and 0FFE will be overwritten by the ELF II monitor.

ELF II owners can use the output port that is on the Giant Board, but they will have to cut two traces on the board. It is really very simple and is worth the effort. The objective is to get the clock, CS2, and $\overline{CS1}$ pins of the 1852 connected to the N2, TPB and $\overline{MRD}$ lines, respectively.

That is all there is to it. Now that you have your EPROM programmer running successfully, you have another valuable tool for your hardware and software development system. ■

An Apple Talks with the Deaf

Ned W. Rhodes
2001 North Kenilworth St.
Arlington, VA 22205

When a deaf woman came to work in my office last summer, I realized I had been taking for granted the ability to hear. She read lips and I learned some sign language, so we were able to "talk," and we corresponded by letter when she returned home to St. Louis at the end of the summer. But I was frustrated that I couldn't pick up the phone and wish her a Merry Christmas or happy birthday. This article describes how I overcame that frustration by turning my Apple into a communications device that helps me talk to my friend and other hearing-impaired people.

Devices called TTYs (teletypewriters) allow the deaf and hearing-impaired to communicate with one another over the phone. The two parties type their messages on keyboards and receive a response either as a printout or video display. The process resembles the way microcomputers communicate with a remote computer by using a modem, except that the communications frequencies used by TTYs are not compatible with standard computer-modem frequencies. Phone-TTY Inc. of Fair Lawn, New Jersey (see box on page 377) makes an acoustic coupler with a 60 milliampere (mA) interface that allows communication between TTYs. I bought the M-1 coupler thinking I could easily interface it to my Apple, but I was wrong. The coupler was shipped with very clear instructions on how to connect it to a 60-mA teletypewriter interface, but there were no instructions or schematics to help with my Apple interfacing project. The manufacturer was unwilling to send me a schematic but did give me the name of a local

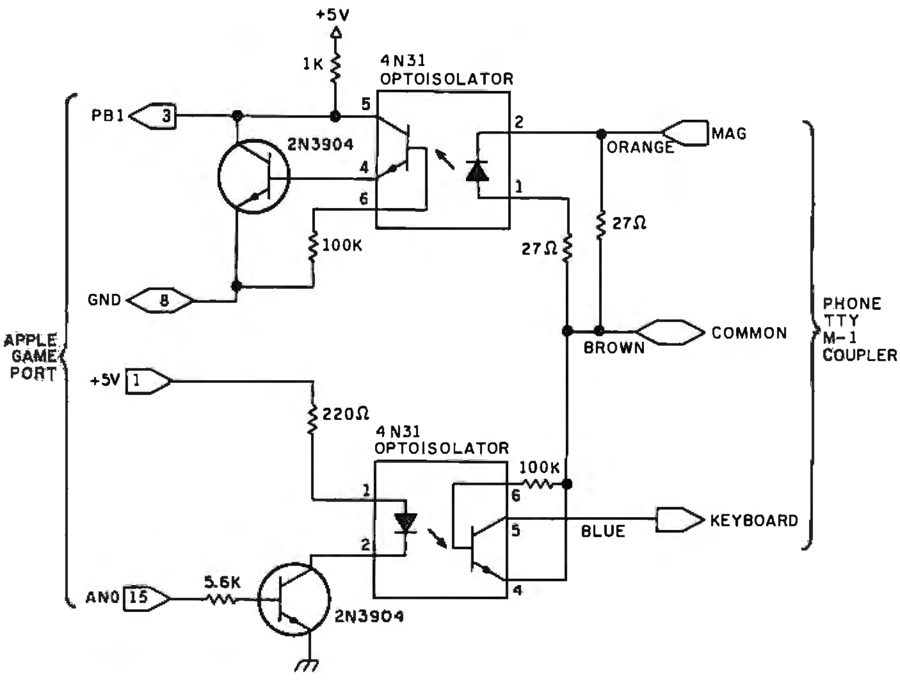

Figure 1: *A schematic diagram of the Apple/M-1 coupler interface. The circuit uses optical isolators to convert the coupler's 60-mA current loop to the TTL levels required by the Apple game-paddle interface.*

About the Author

Ned Rhodes has an electrical engineering degree from the University of Minnesota and a master's degree in computer science from George Washington University. He is employed by the Melpar Division of E-Systems Inc. in Falls Church, Virginia, where he develops minicomputer-based data-acquisition systems.

Circle 268 on inquiry card.

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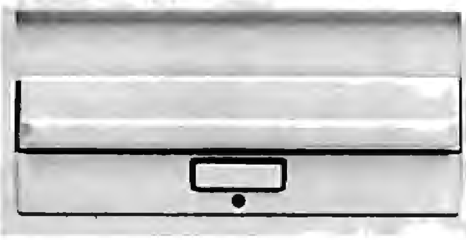

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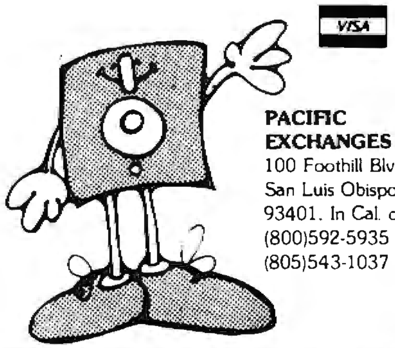

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computer club that had already interfaced the M-1 coupler to the Apple.

Apple/M-1 Interface

A call to Paul Rinaldo of AMRAD (Amateur Radio Research and Development Corporation) in Vienna, Virginia, brought the offer of a schematic and software to drive the hardware. I had expected the schematic, but getting a software package was almost too good to be true. Figure 1 shows the schematic of the Apple/M-1 interface, based on a design by Elton Sanders of AMRAD. As you can see from the circuit diagram, the M-1 coupler is interfaced to the Apple via the game-paddle connector, making the interface inexpensive. The only disadvantage I could see was that the timing of bit transmissions and receptions has to be handled in software. As it turned out, however, this was really an advantage.

The circuit in figure 1 uses optical isolators to convert the 60-mA current loop used by the M-1 coupler to the TTL (transistor-transistor logic) levels used by the Apple game-paddle interface. You can use almost any optical isolator in the circuit as long as the isolator's LED (light-emitting diode) can handle 20 mA or more. The output side of the optical isolator must be able to handle collector-to-emitter voltages of about 15 V. The switching time of the optical isolator doesn't need to be very fast; switching times in the tens of milliseconds can keep up with TTY devices.

Finally, the forward or turn-on voltage of the LED must be 1.5 V or less because the input of the 60-mA interface of the M-1 coupler operates from −1.5 V to 0 V. I had a problem with one brand of optical isolator that had a turn-on voltage greater than 1.5 V. The circuit wouldn't work because the optical isolator was never turning on. I switched to a different brand of isolator (4N31 or Radio Shack 276-133), with a lower turn-on voltage, and then the circuit worked fine.

Communications Software

As I mentioned before, AMRAD gave me a software routine that allowed the Apple to communicate

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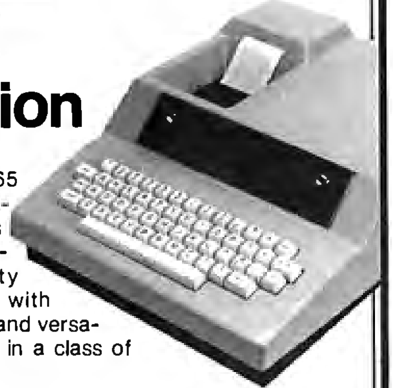

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over the phone with other TTY devices using the M-1 coupler. The routine, written by AMRAD member Nancy Sanders, worked fairly well, but I wanted more. So I sat down and wrote the software in listing 1. When I was finished, my routine was the same size as the original but had some new features. Before explaining those, I'll describe some of the background information I needed to write the routine, as well as some of the software techniques I used.

TTY devices for the deaf use a five-level code called Baudot that differs greatly from ASCII (American Standard Code for Information Interchange). A five-level code like Baudot uses 5 bits to represent each character. At most, 5 bits can represent 32 unique characters (because $2^5 = 32$). In order to represent 26 letters, 10 numbers, and a host of special alphanumeric characters, some sort of encode/decode scheme must be used with Baudot code. Table 1 shows the code for TTY communications. You can see in the table that the Baudot code is defined as having a letters and a figures case. The default case setting is letters; in order to shift to figures case, you must send the figures-case character (11011). Then the figures case is selected until the letters-case character (11111) is sent again. By using these "shift-case" characters, the Baudot code makes 5 bits represent 56 characters (not counting the shift-case characters themselves, and counting only once the four characters that are the same in both cases).

TTY Data Rates

Because the M-1 coupler is interfaced to the Apple via the game I/O (input/output) port, software must handle the timing of all bits both transmitted and received. The transmission rate (bits per second) is obviously an important consideration. For TTY communications, the transmission rate is 60 words per minute or 6 characters per second, allowing 166 ms for transmitting one Baudot character. When each Baudot character is transmitted, 7 bits are sent. First comes a start bit, then the 5 data bits, and finally a stop bit. The time be-

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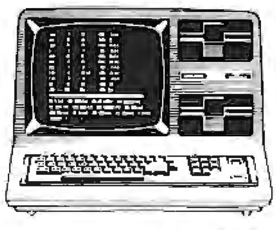

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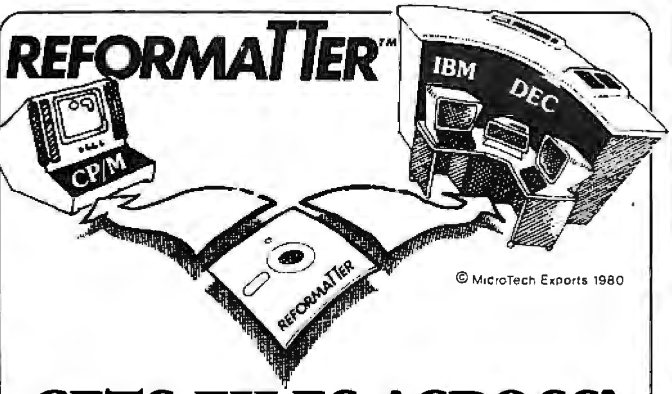
tween bits is constant except for the stop bit. The stop bit time is 1.5 times longer than the times for the other bits. If you choose a bit-delay of 22 ms, the total transmission time for the 7 bits is 165 ms (16 × 22 + 1 × 33). The difference of 1 ms from the ideal time corresponds to an error of about 0.6 percent, which is acceptable. So the pattern of transmission is: first a start bit, then a 22-ms delay; next the 5 data bits, delaying 22 ms between each pair; finally, the stop bit and a delay of 33 ms.

The 22-ms and 33-ms delays are important for proper reception and transmission of Baudot code, but a

Bit Numbers 4	3	2	1	0	Letters Case	Figures Case
0	0	0	0	0	rubout	rubout
0	0	0	0	1	E	3
0	0	0	1	0	line feed	line feed
0	0	0	1	1	A	–
0	0	1	0	0	space	space
0	0	1	0	1	S	'
0	0	1	1	0	I	8
0	0	1	1	1	U	7
0	1	0	0	0	carriage return	carriage return
0	1	0	0	1	D	$
0	1	0	1	0	R	4
0	1	0	1	1	J	'
0	1	1	0	0	N	,
0	1	1	0	1	F	!
0	1	1	1	0	C	:
0	1	1	1	1	K	(
1	0	0	0	0	T	5
1	0	0	0	1	Z	"
1	0	0	1	0	L	)
1	0	0	1	1	W	2
1	0	1	0	0	H	=
1	0	1	0	1	Y	6
1	0	1	1	0	P	0
1	0	1	1	1	Q	1
1	1	0	0	0	O	9
1	1	0	0	1	B	?
1	1	0	1	0	G	+
1	1	0	1	1	figures	figures
1	1	1	0	0	M	.
1	1	1	0	1	X	/
1	1	1	1	0	V	;
1	1	1	1	1	letters	letters

Table 1: *The Baudot code for TTY communications. By using two cases—figures case and letters case—the Baudot code makes 5-bit numbers represent 56 unique characters. The shift-case characters, as well as rubout, line feed, space, and carriage return, are the same in the two cases.*

Circle 251 on inquiry card.



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74LS15	.35	74LS139	.48	74LS257	.55
74LS20	.18	74LS151	.40	74LS258	.55
74LS21	.18	74LS153	.40	74LS273	1.15
74LS22	.25	74LS155	.60	74LS279	.48
74LS26	.36	74LS156	.70	74LS280	1.80
74LS27	.28	74LS157	.48	74LS283	.75
74LS28	.45	74LS158	.48	74LS290	.72
74LS30	.18	74LS161	.58	[illegible]	.38
74LS32	.35	74LS162	.70	74LS365	.52
74LS37	.30	74LS163	.58	74LS366	.52
74LS38	.30	74LS1 4	.58	74LS367	.52
74LS40	.40	74LS168	1.25	74LS368	.52
74LS42	.44	74LS169	1.75	74LS373	1.26
74LS47	.65	74LS170	1.50	74LS374	1.25
74LS51	.20	74LS173	.59	74LS377	1.25
74LS54	.20	74LS174	.45	74LS386	.50
74LS73	.35	74LS175	.40	74LS390	.98
74LS74	.35	74LS181	1.95	74LS393	.98
74LS75	.35	74LS190	.72	74LS670	1.60
74LS76	.45	74LS191	.72	81LS97	1.10
74LS83	.75	74LS192	.65	81LS98	1.10
74LS85	.85	74LS193	.60		
74LS86	.40	74LS194	1.10		
74LS90	.39	74LS195	.90		
74LS92	.45				

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stock Apple lacks a precision interval-timer for timing these delays. You can code a software-delay loop to do the job, but you'll run into a few problems. Because the Apple does not use interrupts for any of its normal processing, it must do everything in a serial fashion. In other words, the Apple can be reading the keyboard or executing a delay loop or sending characters to the M-1 coupler, but it can't do more than one of those things at the same time. In this application, the Apple will usually be executing the delay loop, during which time the processor is doing nothing more than timing 22-ms or 33-ms intervals.

Remember that for every character sent, the Apple is in a delay loop totaling 165 ms. Because of the use of the figure and letter shift characters, however, any key pressed may actually result in the transmission of *two* characters, keeping the Apple busy in delay loops for as long as 330 ms. An average typist, who can easily type faster than the Apple can accept input, ends up having to concentrate more on the process of typing than on the message being typed.

Because most TTY devices are hard-copy terminals with line widths of 64 characters, the software has to send a carriage return/line feed combination after each group of 64 characters in order to prevent characters from being lost at the end of the line. As a result, the Apple stays busy sending the carriage return/line feed and can't read keyboard input in time. The software supplied by AMRAD did in fact lose characters; clearly something was required to remedy the situation.

A "Do Something" Delay Loop

With the processor spending a lot of time in the delay loop, why not make checking the keyboard for input an integral part of that loop? In other words, why not turn the "do nothing" delay loop into a "do something" delay loop? That's exactly what I did. I chose to use an 11-ms delay loop so that I could easily build 22-ms and 33-ms delays. I then constructed an 11-ms delay loop that checks the keyboard for input and does nothing if input is not available. If input is available, it is read and stored (more about that later). This delay loop is the most important part of the communications software. No matter what happens, it must always execute in the same amount of time. The delay loop can follow one of two execution paths depending on whether or not keyboard input is available. As you can see in listing 1, both paths take 47 cycles of the Apple clock. The delay loop is executed 239 times for a total of 11,233 clock cycles. The Apple is running at 1.023 MHz so that each clock cycle is 0.9775 μs. The total time of the delay loop is therefore 11,233 $\times$ 0.9775 μs, or about 10.98 ms, which is within 0.2 percent of the desired 11 ms. But these figures don't take into account the time required to enter the subroutine and then return to the mainline code. The effect of these transitions is to lengthen the delay loop slightly and bring it even closer to the desired 11 ms.

The Input Ring Buffer

Now that you have a routine to read input data from the keyboard, you need a place to put the data. Because you may be reading ahead of the transmission routine, the character currently being read will not necessarily be the next character transmitted. My solution to this problem was to use a ring buffer for the storage of characters awaiting transmission. A ring buffer is conceptually an array in which the last element is followed by the first. That is, when you are reading characters from the buffer and come to the last item in the buffer, the next item to be selected is the item that is now first in the buffer. A ring has no actual start or end but uses position pointers to indicate the next character.

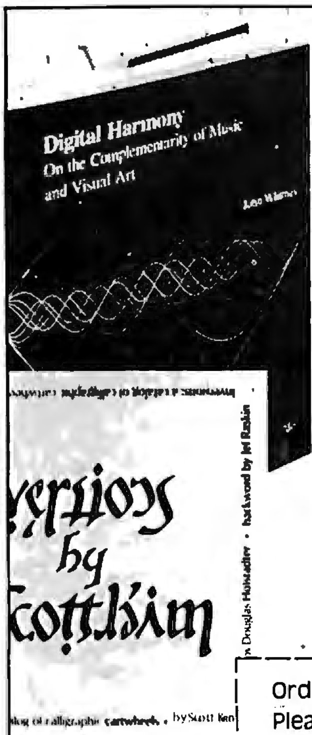
This application requires three position pointers. The first, FILL, indicates the next empty position in the ring buffer. The pointer EMTY indicates the next character to be displayed on the Apple screen. Finally, TOUT points to the next character to be sent to the M-1 coupler. When TOUT or EMTY is equal to FILL, you know all available characters have been sent or displayed. I didn't worry about buffer overflow because I had allocated a 256-character ring buffer and I can't type much faster than the 60-word-a-minute rate used by Baudot. Under normal circumstances, I have only one or two characters in the ring buffer at one time.

The ring buffer is easy to implement in assembly language because of a handy property of integer addition. The largest number that can be represented by 8 bits is 255. When 1 is added to 255, the result is zero, with the carry bit set; that is exactly what is required for a ring buffer. Using an 8-bit pointer as an index into a 256-byte buffer, start the index at 0 and continue to 255. Then, when 1 is added to 255, ignore the carry and use the result of zero as the index into the buffer for the next element—a painless method of implementing a ring buffer. If you needed ring buffers of other sizes, you would need additional software to check the index pointer for values greater than the size of the buffer. If the index exceeded the end of the buffer, you would have to force the index's value to zero and continue.

Program Initialization

The program begins by clearing the Apple screen, displaying a blinking cursor, and then initializing some of the variables used in the program. Then the program enters its main loop, which checks for keyboard input, displays a character from the input ring buffer, sends a character to the coupler, displays a character from the input ring buffer, checks for incoming data, and again displays a character from the input ring buffer.

Here I should mention the repeated calls to the display routine. As stated previously, the delay loop checks for keyboard input and reads in any it finds. The data is stored in the input ring buffer and is not displayed when read. A call to the display routine is necessary in order to "echo" the typed characters to the screen. I had to use this method because I was using the display routine in the Apple monitor and could not be certain of the time required to display one character.



The execution time of the monitor's display routine varies, depending on which character is being displayed and whether a screen scroll is required. Because I needed a delay loop that was constant and precise, I couldn't use the monitor's character-display routine.

Five Program Sections

I will now briefly describe the five major sections of the communications program shown in listing 1: the keyboard-read routine; the character-display routine; the Baudot-send routine; the serial-output routine; and the serial-input routine. I will then describe the program's memory use.

The keyboard-read routine is a straightforward routine that first checks for input and, if any is available, reads it in. Next this routine checks the case of the character and converts any lowercase characters to uppercase. Finally, the keyboard-read routine stores the character in the ring buffer. Just before this final step, you can check for buffer overflow. Note that the character is simply read here, not displayed.

The character-display routine displays characters stored in the ring buffer. For most characters, this means simply reading the character from the ring buffer, displaying it, and then displaying the screen cursor. When a character is displayed, it overwrites the blinking cursor. The blinking cursor must be displayed again and backed over, so that the next character displayed will also overwrite the cursor. When you backspace over the cursor, you change only a pointer, leaving the cursor displayed and blinking.

The characters "carriage return" and "line feed" require special handling. When either of these characters is detected, the character-display routine first clears the screen from the current cursor position to the end of the line. This action erases the cursor and clears off any garbage that may have been displayed on the line. Then the routine displays the character and the cursor.

The "rubout" or "back space" character is also handled in a special fashion. When the "rubout" (or "left arrow" on the Apple) is detected, the routine displays a space to erase the cursor, then backspaces two characters, displays the cursor again, and backspaces over it. This effectively erases the previously typed character by moving the cursor back one character position.

The Baudot-send routine is responsible for sending characters out to the M-1 coupler. As mentioned before, this routine also keeps track of the number of characters on one line. When 64 characters have been sent, a carriage return/line feed combination must follow. The problem with this rule is that, on the receiving end, it may break a word at the end of a line. To solve that problem, the send routine begins looking for a space character after 51 characters have been sent. If a space is found, the carriage return/line feed is inserted, and the next word appears on the following line. If no spaces are encountered before the 65th character, a carriage return/line feed is inserted after the 64th character typed, and a word is broken. This code makes the output easier to read.

Before the characters are sent to the M-1 coupler, they have to be converted from ASCII to Baudot. The conversion is performed by isolating the 7 low-order ASCII bits and subtracting hexadecimal 20. The result is then used as an index into the conversion table, and the equivalent Baudot character is "looked up." Before the character is sent, the routine determines whether the character is of the current shift case, or whether a new character indicating one of three possible shift cases must be sent first. In addition to the letters and figures shifts, certain bit patterns mean the same thing in either shift case. These characters (the "space" character is one example) require no shift change and may be sent in the current shift case. Because Baudot characters use only 5 bits, the 3 remaining bits (out of 8) in the lookup table are used to code the shift case. When the character itself is sent, it consists only of the low-order 5 bits.

The lookup table is constructed so that entries with the seventh bit set require no change in mode or shift case. Entries with the sixth bit set are figures-shift characters, and entries with the sixth bit reset are letters-shift characters. The current shift case is always stored in a temporary location; before a character is sent, its case is compared with the current shift case. If the two cases differ, the appropriate shift case is sent before the character. When the current case is the same as the case of the character to be sent, no case change is required, and the character is dispatched immediately. The Baudot character is sent in a serial fashion to the M-1 coupler, and then to the TTY device on the other end of the line.

The serial-output routine transmits the 5-bit Baudot character to the coupler. First the routine sends the start bit, followed by a a 22-ms delay. The 5 data bits are sent next with a 22-ms delay between each pair. Finally, the serial-output routine sends the stop bit, following it with a 33-ms delay.

The serial-input routine handles character input from the M-1 coupler. First the routine brings in a start bit, followed by 5 data bits and a stop bit. The bits are read in a serial fashion into a memory location that retains only the 5 data bits. Next, the routine checks to see if the character read was either a letters or a figures character. If so, the shift case is stored in a memory location. If the character is not a shift character, the value of the current shift case is added to the character that was read, and this value becomes the index into the Baudot-to-ASCII lookup table. The appropriate character is retrieved from the lookup table and displayed immediately. The character is not placed in the ring buffer, which is reserved for outgoing characters.

Memory Usage

The TTY program uses page zero locations 0 through 9 hexadecimal for internal housekeeping. Memory locations 800 through 8FF hexadecimal are reserved for the input ring buffer. The program itself is located from hexadecimal 900 to B5E and may be relocated to another memory location by reassembly. I relocated my routine to the D800 address space and burned the routine into a PROM so that I could turn on my Apple and begin execution of the TTY program without loading it from disk or cassette.

I chose the Apple as my home computer because it can wear many hats. I am glad to have played a part in adding another hat to the Apple wardrobe. With the addition of the M-1 coupler and a little bit of software, the Apple makes an excellent communication device for the deaf, the hearing-impaired, and their friends. ■

Listing 1 is on pages 377-386

Telephone Communications Products for the Deaf and Hearing-Impaired

Phone-TTY Inc of Fair Lawn, New Jersey, offers five products to help the deaf and hearing-impaired with telephone communication. The M-1 acoustic-coupler modem described in the accompanying article costs $164.50. Another acoustic-coupler modem, the M-1W, is priced at $174.50 and will send signals through home power lines to a Phone-TTY remote-control receiver ($27.50) plugged into any outlet. A light connected to the receiver will flash when the telephone is ringing. The M-2W direct-connect modem costs $182.50; like the M-1W, the M-2W will send signals to an electrical outlet to trigger an indicator light when the telephone rings. The AM modem is an auto-memory device that can answer the telephone and transmit to the caller a previously programmed message up to 2 K bytes in length. The AM can also convert a KSR (Keyboard Send Receive) teletypewriter to an ASR (Automatic Send Receive) teletypewriter. An ASR teletypewriter normally reads paper tape and sends the data read; the Phone-TTY AM coupler enables a KSR teletypewriter to send data stored in the AM's 2 K-byte buffer. The AM is priced at $545. Phone-TTY Inc is located at 14-25 Plaza Rd., Fair Lawn, NJ 07410, telephone (201) 796-5414 (voice or TTY).

Listing 1: *An assembly-language program that enables the Apple to function as a TTY device for telephone communications with the deaf and the hearing-impaired. The program has five major sections: the keyboard-read routine, the character-display routine, the Baudot-send routine, the serial-output routine, and the serial-input routine. The main program loop starts at line 091D.*

```
:ASM

                1000 *
                1010 *
                1020 *    COMMUNICATIONS PACKAGE TO ALLOW THE APPLE TO FUNCTION
                1030 *    AS A TTY DEVICE. FOR USE BY THE DEAF AND HEARING
                1040 *    IMPAIRED.  THE APPLE IS INTERFACED TO AN M1 COUPLER
                1050 *    MANUFACTURED BY PHONE-TTY OF NEW JERSEY.
                1060 *    THE HARDWARE WAS DESIGNED BY ELTON A SANDERS, MEMBER
                1070 *    OF AMRAD IN VIENNA, VIRGINIA, AND USES PUSHBUTTON 1
                1080 *    AND ANNUNCIATOR 1 OF THE APPLE GAME I/O CONNECTOR.
                1090 *    THIS SOFTWARE ROUTINE IS BASED LOOSELY ON ONE
                1100 *    DEVELOPED BY NANCY SANDERS, ALSO A MEMBER OF AMRAD.
                1110 *    I HAVE ADDED SOME SPECIAL FEATURES SUCH AS A HIGH
                1120 *    SPEED RING BUFFER THAT ALLOWS THE OPERATOR TO TYPE
                1130 *    CHARACTERS FASTER THAN THE INTERFACE CAN SEND THEM.
                1140 *
                1150 *    WRITTEN BY NED W. RHODES
                1160 *    DECEMBER 1980
                1170 *
                1180 *
                1190 *    MEMORY USAGE
                1200 *
                1210 *    BASE PAGE : 0 - 9 -- HOUSEKEEPING VARIABLES
                1220 *    $800-$8FF : RING BUFFER FOR INPUT
                1230 *    $900-$B5E : PROGRAM ITSELF (IT IS RELOCATABLE)
                1240 *
                1250 *
                1260 *    VARIABLE DEFINITIONS
                1270 *
                1280 *
FBE2-           1290 BELL .EQ $FBE2      MONITOR BELL ROUTINE.
0044-           1300 BSPC .EQ $44        BAUDOT SPACE +NO MODE CHANGE
0032-           1310 MAXC .EQ 50         START WITH 50 CHARACTERS PER LINE
C058-           1320 SPA  .EQ $C058      SEND SPACE
C059-           1330 MRK  .EQ $C059      SEND MARK
0040-           1340 RUBO .EQ $40        RUBOUT CHARACTER + NO MODE CHANGE
0042-           1350 LINF .EQ $42        LINE FEED IN BAUDOT + NOMO
0048-           1360 CRC  .EQ $48        CARRIAGE RETURN IN BAUDOT
C000-           1370 KEYB .EQ $C000      KEYBOARD
C010-           1380 STRB .EQ $C010      KEYBOARD STROBE
FDF0-           1390 DISP .EQ $FDF0      MONITOR OUTPUT
0000-           1400 NULL .EQ $00        NULL CHARACTER
FC58-           1410 HOME .EQ $FC58      HOME SCREEN
0024-           1420 CHAR .EQ $24        MONITOR CHARACTER COUNT
0025-           1430 CV   .EQ $25        MONITOR VERTICAL COUNTER
FC9C-           1440 CEOL .EQ $FC9C      CLEAR TO EOL
FC10-           1450 BS   .EQ $FC10      MONITOR BACKSPACE
0020-           1460 FIG  .EQ $20        INDICATE FIGURES SHIFT
0080-           1470 ILLG .EQ $80        ILLEGAL BAUDOT CHARACTER
0040-           1480 NOMO .EQ $40        NO MODE CHANGE REQUIRED
0800-           1490 RING .EQ $800       RING BUFFER IS ON PAGE EIGHT
0000-           1500 SHIFT .EQ $00       SHIFT STATUS
0001-           1510 EMTY .EQ $01        DISPLAY POSITION IN RING BUFFER
0002-           1520 TOUT .EQ $02        TTY OUT POSITION IN RING BUFFER
0000-           1530 LET  .EQ $00        LETTERS SHIFT
001B-           1540 FIGS .EQ $1B        FIGURES SHIFT
0003-           1550 CNT  .EQ $03        BIT COUNTER
0004-           1560 FILL .EQ $04        RING BUFFER FILL POSITION
0005-           1570 HOLD .EQ $05        CHARACTER HOLD AREA
0006-           1580 CNUM .EQ $06        CHARACTER PER LINE COUNTER
0007-           1590 RSFT .EQ $07        RECEIVE SHIFT LOCATION
FFF2-           1600 REM  .EQ MAXC-64    - NUMBER OF CHARACTERS BEFORE 64
C062-           1610 TINP .EQ $C062      TTY BIT INPUT
001F-           1620 LSHF .EQ $1F        LETTERS SHIFT
0008-           1630 CHR  .EQ $08        RECEIVED ASSEMBLED CHARACTER
```

Listing 1 continued:

```
0009-              1640 VALUE .EQ.$09        BIT VALUE OF RECEIVED CHARACTER
008A-              1650 LF    .EQ $8A        LINE FEED
008D-              1660 CR    .EQ $8D        CARRIAGE RETURN
0088-              1670 ROUT  .EQ $88        RUBOUT
0060-              1680 CURS  .EQ $60        CURSOR
00A0-              1690 SPAC  .EQ $A0        SPACE
                   1700       .OR $900       ORG IT HERE, ABOVE THE RING BUFFER
                   1710 *
                   1720 *
                   1730 *     INITIALIZATION -- CLEAR SCREEN AND LOAD VARIABLES
                   1740 *
                   1750 *
0900- 20 58 FC     1760 VINT  JSR HOME       CLEAR SCREEN
0903- A9 60        1770       LDA #CURS      GET CURSOR CHARACTER
0905- 85 00        1780       STA SHIFT      SET SHIFT UP TO FORCE A MODE TRANSMIT
0907- 20 F0 FD     1790       JSR DISP       DISPLAY IT
090A- C6 24        1800       DEC CHAR       BACK UP OVER CURSOR
090C- A9 00        1810       LDA #0         GET A ZERO
090E- 85 04        1820       STA FILL       STARTING POSITION
0910- 85 01        1830       STA EMTY       STARTING POSITION
0912- 85 02        1840       STA TOUT       STARTING POSITION
0914- 8D 59 C0     1850       STA MRK        SET COUPLER TO IDLE MODE
0917- 85 07        1860       STA RSFT       DEFAULT RECIEVER SHIFT TO LETTERS
0919- A9 32        1870       LDA #MAXC      GET CHARACTER COUNT
091B- 85 06        1880       STA CNUM       SAVE AWAY
                   1890 *
                   1900 *
                   1910 *     MAIN PROGRAM LOOP
                   1920 *
                   1930 *
091D- 20 32 09     1940 LOOP  JSR KEYS       READ THE KEYBOARD IF CHARACTER IS PRESENT
0920- 20 51 09     1950       JSR SHOW       DISPLAY CHARACTER FROM RING BUFFER
0923- 20 88 09     1960       JSR SEND       SEND A CHARACTER IF PRESENT
0926- 20 51 09     1970       JSR SHOW       DISPLAY CHARACTER FROM RING BUFFER
0929- 20 3C 0A     1980       JSR INPT       RECEIVE A CHARACTER IF PRESENT
092C- 20 51 09     1990       JSR SHOW       DISPLAY CHARACTER FROM RING BUFFER
092F- 4C 1D 09     2000       JMP LOOP       TRY AGAIN
                   2010 *
                   2020 *
                   2030 *     KEYBOARD ENTRY
                   2040 *
                   2050 *
0932- 2C 00 C0     2060 KEYS  BIT KEYB       CHECK THE KEYBOARD
0935- 10 19        2070       BPL KRTS       NO CHARACTER
0937- AD 00 C0     2080       LDA KEYB       GET CHARACTER
093A- 2C 10 C0     2090       BIT STRB       RESET STROBE
093D- AA           2100       TAX            SAVE A COPY
                   2110 *
                   2120 *
                   2130 *     CHECK HERE FOR LOWER CASE LETTERS
                   2140 *     CONVERT TO UPPER CASE IF FOUND
                   2150 *
                   2160 *
093E- 29 60        2170       AND #$60       MASK OUT LOWER CASE
0940- C9 60        2180       CMP #$60       IS IT LOWER CASE
0942- D0 04        2190       BNE CAP        NO--CAPITAL
0944- 8A           2200       TXA            GET CHARACTER
0945- 29 DF        2210       AND #$DF       MAKE UPPER CASE
0947- AA           2220       TAX            SAVE CHARACTER AGAIN
0948- 8A           2230 CAP   TXA            GET CHARACTER
0949- A6 04        2240       LDX FILL       GET POSITION IN BUFFER
094B- 9D 00 08     2250       STA RING,X     SAVE IT
094E- E6 04        2260       INC FILL       BUMP POINTER
0950- 60           2270 KRTS  RTS            RETURN
                   2280 *
                   2290 *
                   2300 *     SHOW ROUTINE -- DISPLAY A CHARACTER IN
                   2310 *     THE RING BUFFER IF THERE IS ONE AVAILABLE
                   2320 *
                   2330 *
```

Listing 1 continued on page 380

Listing 1 continued:

```
0951- A6 01        SHOW LDX EMTY        GET POINTER
0953- E4 04             CPX FILL        HAVE WE CAUGHT UP??
0955- F0 30             BEQ SRTS        YES--EXIT
0957- BD 00 08          LDA RING,X      GET CHARACTER
095A- E6 01             INC EMTY        BUMP POINTER
095C- 48           SHW2 PHA             SAVE CHARACTER
                   *
                   *
                   *    HANDLE LINE FEED AND CARRIAGE RETURN IN A SPECIAL WAY
                   *
                   *
095D- C9 8A             CMP #LF         IS IT A LINE FEED??
095F- D0 05             BNE NOLF        NOPE
0961- 20 9C FC          JSR CEOL        CLEAR TO END OF LINE
0964- B0 15             BCS NBS         CONTINUE ONWARD
0966- C9 8D        NOLF CMP #CR         IS IT A CARRIAGE RETURN??
0968- D0 05             BNE CRN         NOPE
096A- 20 9C FC          JSR CEOL        CLEAR TO END OF LINE
096D- B0 0C             BCS NBS         CONTINUE ON

                   *
                   *
                   *    RUBOUT OR BACKSPACE IS SPECIAL CASE
                   *
                   *
096F- C9 88        CRN  CMP #ROUT       IS IT A BACKSPACE
0971- D0 08             BNE NBS         NOPE
0973- A9 A0             LDA #SPAC       GET A SPACE
0975- 20 F0 FD          JSR DISP        ERASE CURSOR
0978- 20 10 FC          JSR BS          BACK SPACE ONE
097B- 68           NBS  PLA             GET CHARACTER
097C- 20 F0 FD          JSR DISP        DISPLAY CHARACTER
097F- A9 60             LDA #CURS       GET CURSOR
0981- 20 F0 FD          JSR DISP        SHOW IT
0984- 20 10 FC          JSR BS          BACK UP OVER IT
0987- 60           SRTS RTS             RETURN
                   *
                   *
                   *    SEND ROUTINE -- SEND CHARACTER TO MODEM
                   *
                   *
0988- A6 02        SEND LDX TOUT        GET POINTER
098A- E4 04             CPX FILL        HAVE WE CAUGHT UP??
098C- F0 38             BEQ NSND        YES--EXIT
098E- BD 00 08          LDA RING,X      GET CHARACTER
0991- E6 02             INC TOUT        INCREMENT POINTER
                   *
                   *
                   *    CHECK FOR SPECIAL CHARACTERS
                   *
                   *    LINE FEED DOESN'T BUMP CNUM
                   *    CARRIAGE RETURN RESETS CNUM
                   *    RUB OUT BUMPS CNUM DUE TO USE WITH HARDCOPY TERMINALS
                   *
                   *
0993- C9 8A             CMP #LF         IS IT A LINE FEED
0995- D0 06             BNE NLF         NOPE
0997- A9 42             LDA #LINF       GET LINE FEED IN BAUDOT
0999- 20 0A 0A          JSR TTYO        SEND IT
099C- 60                RTS             RETURN
099D- C9 8D        NLF  CMP #CR         IS IT A CARRIAGE RETURN??
099F- D0 0F             BNE NCR         NOPE
09A1- A9 48             LDA #CRC        GET A CARRIAGE RETURN IN BAUDOT
09A3- 20 0A 0A          JSR TTYO        SEND IT
09A6- A9 42             LDA #LINF       GET A LINE FEED ALSO
09A8- 20 0A 0A          JSR TTYO        SEND IT
09AB- A9 32             LDA #MAXC       CHARACTERS PER LINE
09AD- 85 06             STA CNUM        RESET IT
09AF- 60                RTS             RETURN
09B0- C9 88        NCR  CMP #ROUT       HOW ABOUT A RUBOUT??
```

Listing 1 continued:

```
09B2- D0 06     3040      BNE NROU      NOPE
09B4- A9 40     3050      LDA #RUBO     GET A RUBOUT
09B6- 20 C7 09  3060      JSR COUT      DO A RUBOUT
09B9- 60        3070      RTS           RETURN
09BA- 29 7F     3080 NROU AND #$7F      GET ONLY 7 BITS
09BC- 38        3090      SEC           SET CARRY
09BD- E9 20     3100      SBC #$20      BIAS FOR LOOKUP TABLE
09BF- AA        3110      TAX           SEND TO X
09C0- BD E3 0A  3120      LDA BAUD,X    GET BAUDOT CHARACTER
09C3- 20 C7 09  3130      JSR COUT      SHIP IT OUT
09C6- 60        3140 NSND RTS           RETURN
                3150 *
                3160 *
                3170 *    TTY OUTPUT ROUTINE
                3180 *
                3190 *    RING THE BELL IF AN ILLEGAL CHARACTER
                3200 *
                3210 *
09C7- C9 80     3220 COUT CMP #ILLG     IS CHARACTER LEGAL BAUDOT??
09C9- 90 04     3230      BCC CON       YES -- CONTINUE
09CB- 20 E2 FB  3240      JSR BELL      RING - RING
09CE- 60        3250      RTS           RETURN
09CF- C9 40     3260 CON  CMP #NOMO     CHECK MODE
09D1- B0 14     3270      BCS OUT       NO CHANGE
09D3- 48        3280      PHA           SAVE CHARACTER
09D4- 29 20     3290      AND #FIG      LOOK AT MODE BIT
09D6- C5 00     3300      CMP SHIFT     COMPARE WITH CURRENT MODE
09D8- F0 0C     3310      BEQ NCHN      NO CHANGE
09DA- 85 00     3320      STA SHIFT     CHANGE MODE FLAG
09DC- 49 20     3330      EOR #FIG      COMPLEMENT BIT
09DE- 4A        3340      LSR           MOVE BIT TO
09DF- 4A        3350      LSR           CORRECT
09E0- 4A        3360      LSR           POSITION
09E1- 09 1B     3370      ORA #FIGS     CONVERT TO MODE CHARACTER
09E3- 20 0A 0A  3380      JSR TTYO      SEND PROPER MODE
09E6- 68        3390 NCHN PLA           GET CHARACTER
09E7- 48        3400 OUT  PHA           SAVE CHARACTER
09E8- 20 0A 0A  3410      JSR TTYO      REALLY SEND CHARACTER
09EB- 68        3420      PLA           GET CHARACTER
09EC- C6 06     3430      DEC CNUM      HAVE WE PRINTED MAXC+1 CHARACTERS??
09EE- 10 19     3440      BPL CRTS      NO, WE'RE OK
                3450 *
                3460 *
                3470 *    NOW WE TRY SOME INTELLIGENCE.  IF WE HAVE SENT
                3480 *    > MAXC+1 CHARACTERS.  WE BEGIN TO LOOK FOR A BAUDOT
                3490 *    SPACE SO THAT WE CAN BREAK WORDS AT A SPACE INSTEAD
                3500 *    OF RIGHT IN THE MIDDLE.
                3510 *
                3520 *
09F0- C9 44     3530      CMP #BSPC     IS IT A BAUDOT SPACE??
09F2- D0 0F     3540      BNE TEST      NO, CHECK FOR > 64 CHARACTERS ANYWAY
09F4- A9 42     3550 MAXL LDA #LINF     GET LINE FEED
09F6- 20 0A 0A  3560      JSR TTYO      SEND IT
09F9- A9 48     3570      LDA #CRC      GET CARRIAGE RETURN
09FB- 20 0A 0A  3580      JSR TTYO      SEND IT
09FE- A9 32     3590      LDA #MAXC     GET CHARACTER COUNT
0A00- 85 06     3600      STA CNUM      SAVE IT
0A02- 60        3610      RTS           RETURN
0A03- A9 F2     3620 TEST LDA #REM      COUNT OF 64 CHARACTERS WHEN ALL IS SAID A
ND DONE
0A05- C5 06     3630      CMP CNUM      HAVE WE PRINTED 64 PER LINE??
0A07- B0 EB     3640      BCS MAXL      YES, SEND CARRIAGE RETURN
0A09- 60        3650 CRTS RTS           RETURN
                3660 *
                3670 *
                3680 *    SERIAL OUTPUT ROUTINE
                3690 *
                3700 *
0A0A- A0 05     3710 TTYO LDY #5        5 BITS TO SEND
0A0C- 84 03     3720      STY CNT       BIT COUNTER
```

Listing 1 continued on page 382

Listing 1 continued:

```
0A0E- 85 05            STA HOLD       SAVE CHARACTER
0A10- 8D 58 C0         STA SPA        SEND START BIT
0A13- 20 B2 0A    CLOP JSR MS11       11 MSEC DELAY
0A16- 20 B2 0A         JSR MS11       11 MSEC DELAY
0A19- 66 05            ROR HOLD       RIGHT SHIFT
0A1B- 90 05            BCC ZERO       BIT IS 0
0A1D- 8D 59 C0         STA MRK        SEND MARK
0A20- B0 03            BCS OVER       CONTINUE
0A22- 8D 58 C0    ZERO STA SPA        SEND A SPACE
0A25- C6 03       OVER DEC CNT        DEC COUNTER
0A27- D0 EA            BNE CLOP       LOOP FOR ALL CHARACTERS
0A29- 20 B2 0A         JSR MS11       11 MSEC DELAY
0A2C- 20 B2 0A         JSR MS11       11 MSEC DELAY
0A2F- 8D 59 C0         STA MRK        SEND STOP BIT
0A32- 20 B2 0A         JSR MS11       11 MSEC DELAY
0A35- 20 B2 0A         JSR MS11       11 MSEC DELAY
0A38- 20 B2 0A         JSR MS11       11 MSEC DELAY
0A3B- 60               RTS            RETURN
                  *
                  *
                  *    TTY INPUT ROUTINE
                  *
                  *
0A3C- 2C 62 C0    INPT BIT TINP       ANY DATA??
0A3F- 10 44            BPL IRTS       NO--EXIT
0A41- 20 B2 0A         JSR MS11       DELAY 11 MSEC.
0A44- 20 86 0A         JSR TTYI       READ DATA IN
0A47- C9 1F            CMP #LSHF      LETTERS SHIFT??
0A49- D0 05            BNE CFIG       NO--CHECK FOR FIGURES SHIFT
0A4B- A9 00            LDA #LET       GET LETTERS SHIFT
0A4D- 85 07            STA RSFT       STORE IT
0A4F- 60               RTS            RETURN
0A50- C9 1B       CFIG CMP #FIGS      FIGURES SHIFT??
0A52- D0 05            BNE NSH        NO SHIFT
0A54- A9 20            LDA #FIG       GET SHIFTER
0A56- 85 07            STA RSFT       SAVE IT
0A58- 60               RTS            RETURN
0A59- 18          NSH  CLC            CLEAR CARRY
0A5A- 65 07            ADC RSFT       BIAS POINTER
0A5C- AA               TAX            SEND TO INDEX REGISTER
0A5D- BD 1E 0B         LDA ASCI,X     GET ASCII CHARACTER
                  *
                  *
                  *    HERE WE TWIDDLE CNUM SO THAT WE WILL BE
                  *    OK WHEN IT IS OUR TURN TO SEND
                  *
                  *
0A60- C9 8D            CMP #CR        IS IT A CARRIAGE RETURN??
0A62- D0 0A            BNE NRST       NO, NO NEED TO RESET
0A64- A9 32            LDA #MAXC      GET CHARACTERS PER LIN
0A66- 85 06            STA CNUM       SAVE IT
0A68- A9 8D            LDA #CR        GET A CARRIAGE RETURN
0A6A- 20 5C 09         JSR SHW2       DISPLAY IT
0A6D- 60               RTS            RETURN
0A6E- C9 8A       NRST CMP #LF        HOW ABOUT A LINE FEED??
0A70- D0 06            BNE RUB        NO, CHECK FOR A RUBOUT
0A72- A4 24            LDY CHAR       CHECK CHARACTER POSITION
0A74- F0 0F            BEQ IRTS       WE ARE AT BEGINNING OF LINE--NO LINE FEED
0A76- D0 0A            BNE PRN2       PRINT IT
0A78- C9 88       RUB  CMP #ROUT      AND A RUBOUT??
0A7A- D0 04            BNE PRNT       NOPE, PRINT AWAY
0A7C- E6 06            INC CNUM       ADD ONE FOR DELETION
0A7E- 50 02            BVC PRN2       AND PRINT
0A80- C6 06       PRNT DEC CNUM       FIDDLE WITH COUNTER
0A82- 20 5C 09    PRN2 JSR SHW2       DISPLAY IT
0A85- 60          IRTS RTS            AND RETURN
                  *
                  *
                  *    SERIAL INPUT ROUTINE
                  *
```

Listing 1 continued:

```
                4430 *
0A86- A9 01     4440 TTYI LDA #1         A ONE
0A88- 85 09     4450      STA VALUE      BIT VALUE OF INPUT
0A8A- A9 05     4460      LDA #5         5 BITS
0A8C- 85 03     4470      STA CNT        TO INPUT
0A8E- A9 00     4480      LDA #00        ZERO OUT
0A90- 85 08     4490      STA CHR        RECEIVED CHARACTER VALUE
0A92- 20 B2 0A  4500 ILOP JSR MS11       DELAY 11 MSEC.
0A95- 20 B2 0A  4510      JSR MS11       DELAY 11 MSEC.
0A98- 2C 62 C0  4520      BIT TINP       LOOK FOR A BIT
0A9B- 30 06     4530      BMI SPACE      WE READ A SPACE
0A9D- A5 08     4540      LDA CHR        GET CHARACTER BUFFER
0A9F- 05 09     4550      ORA VALUE      GET THE PROPER BIT VALUE
0AA1- 85 08     4560      STA CHR        RE-SAVE CHARACTER
0AA3- 06 09     4570 SPACE ASL VALUE     SHIFT RIGHT ONCE
0AA5- C6 03     4580      DEC CNT        ARE WE DONE??
0AA7- D0 E9     4590      BNE ILOP       NO--GET MORE BITTS
0AA9- 20 B2 0A  4600      JSR MS11       DELAY 11 MSEC
0AAC- 20 B2 0A  4610      JSR MS11       DELAY 11 MSEC
0AAF- A5 08     4620      LDA CHR        GET THE CHARACTER
0AB1- 60        4630      RTS            AND RETURN
                4640 *
                4650 *
                4660 *    11 MILLISECOND DELAY LOOP
                4670 *
                4680 *    THE DELAY LOOP IS LONG BECAUSE WE
                4690 *    ARE CHECKING FOR KEYBOARD INPUT DURING
                4700 *    THE DELAY TIME SO THAT WE CAN ACTUALLY
                4710 *    TYPE FASTER THAN THE 6 CHARACTERS PER
                4720 *    SECOND THAT THE BAUD RATE LIMITS US TO.
                4730 *    THE DELAY LOOP HAS BEEN DESIGNED SO THAT
                4740 *    IT TAKES THE SAME AMOUNT OF TIME WHETHER
                4750 *    OR NOT THE BRANCHES ARE TAKEN.
                4760 *
                4770 *
0AB2- A0 EF     4780 MS11 LDY #239       239 * 47 = 11233 CLOCK CYCLES
0AB4- 2C 00 C0  4790 TOP  BIT KEYB       TEST KEYBOARD [4]  [4]
0AB7- 10 18     4800      BPL NOT        NO DATA       [4]  [3]
0AB9- A6 04     4810      LDX FILL       GET POINTER   [3]
0ABB- AD 00 C0  4820      LDA KEYB       READ THE DATA [4]
0ABE- 2C 10 C0  4830      BIT STRB       RESET STROBE  [4]
0AC1- 9D 00 08  4840      STA RING,X     SAVE IN BUFFER[5]
0AC4- E6 04     4850      INC FILL       BUMP POINTER  [5]
0AC6- EA        4860      NOP                          [2]
0AC7- 48        4870      PHA            PUSH          [3]
0AC8- 68        4880      PLA            POP           [4]
0AC9- EA        4890      NOP                          [2]
0ACA- 88        4900      DEY            DEC COUNTER   [2]
0ACB- F0 15     4910      BEQ EXIT       RETURN        [2]
0ACD- EA        4920      NOP                          [2]
0ACE- 4C B4 0A  4930      JMP TOP        TRY AGAIN     [3]
                4940 *                                 47 CLOCK CYCLES
                4950 *
                4960 *
                4970 *    NO DATA
                4980 *
                4990 *
0AD1- A5 00     5000 NOT  LDA $0         ACESS BASE PG [3]
0AD3- 48        5010      PHA            PUSH          [3]
0AD4- 68        5020      PLA            POP           [4]
0AD5- 48        5030      PHA            PUSH          [3]
0AD6- 68        5040      PLA            POP           [4]
0AD7- 48        5050      PHA            PUSH          [3]
0AD8- 68        5060      PLA            POP           [4]
0AD9- 48        5070      PHA            PUSH          [3]
0ADA- 68        5080      PLA            POP           [4]
0ADB- EA        5090      NOP                          [2]
0ADC- 88        5100      DEY            DEC COUNTER   [2]
0ADD- F0 03     5110      BEQ EXIT                     [2]
0ADF- 4C B4 0A  5120      JMP TOP        TRY AGAIN     [3]
```

Listing 1 continued on page 384

Listing 1 continued:

```
                *                                  47 CLOCK CYCLES
0AE2- 60        EXIT RTS           EXIT
                *
                *
                *    LOOK-UP TABLES
                *
                *    ASCII-TO-BAUDOT
                *
                *
                *    THE TABLE IS CODED AS FOLLOWS:
                *    BIT 6 LIT = NO MODE CHANGE REQUIRED
                *    BIT 5 LIT = FIGURES SHIFT
                *    BIT 5 OFF = LETTERS SHIFT
                *    BIT 7 LIT = ILLEGAL BAUDOT CHARACTER
                *                DO NOT SEND
                *
                *
                *    FIGURES SHIFT
                *
                *
0AE3- 44        BAUD .DA #$04+NOMO SPACE
0AE4- 2D             .DA #$0D+FIG  !
0AE5- 31             .DA #$11+FIG  "
0AE6- 80             .DA #ILLG     # IS ILLEGAL
0AE7- 29             .DA #$09+FIG  $
0AE8- 80             .DA #ILLG     % IS ILLEGAL
0AE9- 80             .DA #ILLG     & IS ILLEGAL
0AEA- 2B             .DA #$0B+FIG  '
0AEB- 2F             .DA #$0F+FIG  (
0AEC- 32             .DA #$12+FIG  )
0AED- 80             .DA #ILLG     * IS ILLEGAL
0AEE- 3A             .DA #$1A+FIG  +
0AEF- 2C             .DA #$0C+FIG  ,
0AF0- 23             .DA #$03+FIG  -
0AF1- 3C             .DA #$1C+FIG  .
0AF2- 3D             .DA #$1D+FIG  /
0AF3- 36             .DA #$16+FIG  0
0AF4- 37             .DA #$17+FIG  1
0AF5- 33             .DA #$13+FIG  2
0AF6- 21             .DA #$01+FIG  3
0AF7- 2A             .DA #$0A+FIG  4
0AF8- 30             .DA #$10+FIG  5
0AF9- 35             .DA #$15+FIG  6
0AFA- 27             .DA #$07+FIG  7
0AFB- 26             .DA #$06+FIG  8
0AFC- 38             .DA #$18+FIG  9
0AFD- 2E             .DA #$0E+FIG  :
0AFE- 3E             .DA #$1E+FIG  ;
0AFF- 80             .DA #ILLG     < IS ILLEGAL
0B00- 34             .DA #$14+FIG  =
0B01- 80             .DA #ILLG     > IS ILLEGAL
0B02- 39             .DA #$19+FIG  ?
                *
                *
                *    LETTERS SHIFT
                *
                *
0B03- 80             .DA #ILLG     @ IS ILLEGAL
0B04- 03             .DA #$03      A
0B05- 19             .DA #$19      B
0B06- 0E             .DA #$0E      C
0B07- 09             .DA #$09      D
0B08- 01             .DA #$01      E
0B09- 0D             .DA #$0D      F
0B0A- 1A             .DA #$1A      G
0B0B- 14             .DA #$14      H
0B0C- 06             .DA #$06      I
0B0D- 0B             .DA #$0B      J
0B0E- 0F             .DA #$0F      K
0B0F- 12             .DA #$12      L
```

Listing 1 continued:

```
0B10- 1C            .DA #$1C       M
0B11- 0C            .DA #$0C       N
0B12- 18            .DA #$18       O
0B13- 16            .DA #$16       P
0B14- 17            .DA #$17       Q
0B15- 0A            .DA #$0A       R
0B16- 05            .DA #$05       S
0B17- 10            .DA #$10       T
0B18- 07            .DA #$07       U
0B19- 1E            .DA #$1E       V
0B1A- 13            .DA #$13       W
0B1B- 1D            .DA #$1D       X
0B1C- 15            .DA #$15       Y
0B1D- 11            .DA #$11       Z
              *
              *
              *     ASCII-TO-BAUDOT TABLE
              *
              *
0B1E- 88      ASCI  .DA #ROUT      RUBOUT
0B1F- C5            .DA #$C5       E
0B20- 8A            .DA #$8A       LINE FEED
0B21- C1            .DA #$C1       A
0B22- A0            .DA #$A0       SPACE
0B23- D3            .DA #$D3       S
0B24- C9            .DA #$C9       I
0B25- D5            .DA #$D5       U
0B26- 8D            .DA #$8D       CARRIAGE RETURN
0B27- C4            .DA #$C4       D
0B28- D2            .DA #$D2       R
0B29- CA            .DA #$CA       J
0B2A- CE            .DA #$CE       N
0B2B- C6            .DA #$C6       F
0B2C- C3            .DA #$C3       C
0B2D- CB            .DA #$CB       K
0B2E- D4            .DA #$D4       T
0B2F- DA            .DA #$DA       Z
0B30- CC            .DA #$CC       L
0B31- D7            .DA #$D7       W
0B32- C8            .DA #$C8       H
0B33- D9            .DA #$D9       Y
0B34- D0            .DA #$D0       P
0B35- D1            .DA #$D1       Q
0B36- CF            .DA #$CF       O
0B37- C2            .DA #$C2       B
0B38- C7            .DA #$C7       G
0B39- 1B            .DA #$1B       FIGURES
0B3A- CD            .DA #$CD       M
0B3B- D8            .DA #$D8       X
0B3C- D6            .DA #$D6       V
0B3D- 1F            .DA #$1F       LETTERS
              *
              *
              *     FIGURES SHIFT
              *
              *
0B3E- 88            .DA #ROUT      RUBOUT
0B3F- B3            .DA #$B3       3
0B40- 8A            .DA #$8A       LINE FEED
0B41- AD            .DA #$AD       -
0B42- A0            .DA #$A0       SPACE
0B43- A7            .DA #$A7       '
0B44- B8            .DA #$B8       8
0B45- B7            .DA #$B7       7
0B46- 8D            .DA #$8D       CARRIAGE RETURN
0B47- A4            .DA #$A4       $
0B48- B4            .DA #$B4       4
0B49- A7            .DA #$A7       '
0B4A- AC            .DA #$AC       ,
0B4B- A1            .DA #$A1       !
```

Listing 1 continued on page 386

Listing 1 continued:

```
0B4C- BA        6530        .DA #$BA     :
0B4D- A8        6540        .DA #$A8     (,
0B4E- B5        6550        .DA #$B5     5
0B4F- A2        6560        .DA #$A2     "
0B50- A9        6570        .DA #$A9     )
0B51- B2        6580        .DA #$B2     2
0B52- BD        6590        .DA #$BD     =
0B53- B6        6600        .DA #$B6     6
0B54- B0        6610        .DA #$B0     0
0B55- B1        6620        .DA #$B1     1
0B56- B9        6630        .DA #$B9     9
0B57- BF        6640        .DA #$BF     ?
0B58- AB        6650        .DA #$AB     +
0B59- 1B        6660        .DA #$1B     FIGURES
0B5A- AE        6670        .DA #$AE     .
0B5B- AF        6680        .DA #$AF     /
0B5C- BB        6690        .DA #$BB     ;
0B5D- 1F        6700        .DA #$1F     LETTERS
0B5E-           6710 END    .EQ *
                6720        .EN
```

```
SYMBOL TABLE

0B1E- ASCI      097B- NBS
0AE3- BAUD      09E6- NCHN
FBE2- BELL      09B0- NCR
FC10- BS        099D- NLF
0044- BSPC      0966- NOLF
094B- CAP       0040- NOMO
FC9C- CEOL      0AD1- NOT
0A50- CFIG      09BA- NROU
0024- CHAR      0A6E- NRST
0008- CHR       0A59- NSH
0A13- CLOP      09C6- NSND
0003- CNT       0000- NULL
0006- CNUM      09E7- OUT
09CF- CON       0A25- OVER
09C7- COUT      0A82- PRN2
003D- CR        0A80- PRNT
0048- CRC       FFF2- REM
096F- CRN       0800- RING
0A09- CRTS      0088- ROUT
0060- CURS      0007- RSFT
0025- CV        0A78- RUB
FDF0- DISP      0040- RUBO
0001- EMTY      0988- SEND
0B5E- END       0000- SHIFT
0AE2- EXIT      0951- SHOW
0020- FIG       095C- SHW2
001B- FIGS      C058- SPA
0004- FILL      00A0- SPAC
0005- HOLD      0AA3- SPACE
FC58- HOME      0987- SRTS
0080- ILLG      C010- STRB
0A92- ILOP      0A03- TEST
0A3C- INPT      C062- TINP
0A85- IRTS      0AB4- TOP
C000- KEYB      0002- TOUT
0932- KEYS      0A86- TTYI
0950- KRTS      0A0A- TTYO
0000- LET       0009- VALUE
008A- LF        0900- VINT
0042- LINF      0A22- ZERO
091D- LOOP
001F- LSHF
0032- MAXC
09F4- MAXL
C059- MRK
0AB2- MS11
```

Books Received

Computers and the Radio Amateur, Phil Anderson. Englewood Cliffs, NJ: Prentice-Hall, 1982; 23.5 by 17.5 cm, 208 pages, hardcover, ISBN 0-13-166306-2, $18.95.

Computer Performance Evaluation: Tools and Techniques for Effective Analysis, Michael F. Morris and Paul F. Roth. New York: Van Nostrand Reinhold, 1981; 23 by 15.5 cm, 260 pages, hardcover, ISBN 0-442-80325-7, $24.95.

Denotational Semantics: The Scott-Strachey Approach to Programming Language Theory, Joseph E. Stoy. Cambridge, MA: The MIT Press, 1981; 14.5 by 22.5 cm, 414 pages, softcover, ISBN 0-262-69076-4, $12.50.

Developing Structured Systems, A Methodology Using Structured Techniques, Brian Dickinson. New York: Yourdon Press, 1981; 24.5 by 17.5 cm, 344 pages, softcover, ISBN 0-917072-23-5, $40.

International Microcomputer Software Directory, John Graham and Roy Wyand, eds. Los Angeles, CA: Imprint Software, 1981; 27.5 by 21 cm, 400 pages, softcover, ISBN 0-907352-03-0, $29.95.

Laboratory Minicomputing, John R. Bourne. New York: Academic Press, 1981; 15.5 by 23 cm, 297 pages, hardcover, ISBN 0-12-119080-3, $27.

Operational Amplifiers and Linear Integrated Circuits, 2nd edition, Robert F. Coughlin and Frederick F. Driscoll. Englewood Cliffs, NJ: Prentice-Hall, 1982; 15 by 23 cm, 376 pages, hardcover, ISBN 0-13-637785-8, $21.95.

Operating System Elements: A User Perspective, Peter Calingaert, Englewood Cliffs, NJ: Prentice-Hall, 1982; 15 by 23 cm, 240 pages, hardcover, ISBN 0-13-637421-2, $23.95.

Starting FORTH, Leo Brodie. Englewood Cliffs, NJ: Prentice-Hall, 1981; 23 by 16.5 cm, 348 pages, softcover, ISBN 0-13-842922-7, $15.95.

Structured Programming Using PL/C, Joan K. Hughes and Barbara J. La Pearl. New York: John Wiley & Sons, 1981; 27 by 21 cm, 414 pages, softcover, ISBN 0-471-04969-7, $17.95.

Word Processing, 2nd edition, Arnold Rosen and Rosemary Fielden. Englewood Cliffs, NJ: Prentice-Hall, 1981; 23 by 15.5 cm, 430 pages, hardcover, ISBN 0-13-963488-6, $18.95.■

This is a list of books received at BYTE Publications during this past month. Although the list is not meant to be exhaustive, its purpose is to acquaint BYTE readers with recently published titles in computer science and related fields. We regret that we cannot review or comment on all the books we receive; instead, this list is meant to be a monthly acknowledgment of these books and the publishers who sent them.

January 1982

January-February

Intel Microcomputer Workshops, various sites throughout the U.S. Intel's hands-on workshops cover a wide selection of Intel's microcomputer components, boards, software, operating systems, and design tools. The workshops can be held at your company's facility. For information, contact Intel Corp., Customer Training, 27 Industrial Ave., Chelmsford, MA 01824, (617) 256-1374.

January-March

Hands-On Local Network Workshops, various sites throughout the U.S. This series of four-day workshops provides hands-on experience with a local computer network. File, printer, and electronic-mail servers, and various software and hardware components of a local-network computer system will be provided. The local network used as the example will consist of at least a Nestar Cluster One/Model A. Write to Architecture Technology Corp., POB 24344, Minneapolis, MN 55424.

January-April

Computer Network Design and Protocols, various sites throughout the U.S. Participants in this workshop will learn to determine network-system requirements and perform design tradeoffs, implement network-communication and control protocols, use packet- and message-switching techniques, evaluate network hardware and software components, interface local systems to networks, and design and build private networks. The course fee is $845. Contact Ruth Dordick, c/o Integrated Computer Systems, 3304 Pico Blvd., POB 5339, Santa Monica, CA 90405, (800) 421-8166; in California (800) 352-8251.

January-April

Fundamentals of Data Processing for Administrative Assistants and Office Support Staff, various sites throughout the U.S. The American Management Associations (AMA) has designed this three-day course for secretaries, assistants, supervisors, and other personnel desiring to learn the fundamentals of data processing and its use in offices. Computer hardware and software, programming languages, and technology will all be covered. The team fee for AMA members is $470 per individual and $550 for nonmembers. Individual fees are $550 for AMA members and $630 for nonmembers. For a schedule of dates and locations, contact the AMA, 135 West 50th St., New York, NY 10020, (212) 586-8100. To register by phone, call (212) 246-0800.

January-June
Datamation Institute Seminars on Information Management, various sites throughout the U.S. Databases and communications, systems performance, data-processing management, word processing and office automation, computer graphics, and topics of general interest are among the areas to be covered by these two-day seminars. Fees range from $495 to $595. For schedules of times and places, contact Karen Smolens, c/o the Center for Management Research, Datamation Institute Seminar Coordination Office, 850 Boylston St., Chestnut Hill, MA 02167, (617) 738-5020.

January 7-10
The 1982 Winter Consumer Electronics Show (CES), Las Vegas Convention Center, Hilton Hotel, and the Jockey Club, Las Vegas, NV. Conferences, workshops, seminars, sales meetings, press events, and exhibits of audio and video equipment, computers, telephones, and other consumer items highlight this show. For details, contact Consumer Electronics Shows, Suite 1607, Two Illinois Center, 233 North Michigan, Chicago, IL 60601, (312) 861-1040.

January 11-13
Unix and C Conference, San Francisco, CA. This conference is sponsored by Uni-Ops, a Unix users group. Tutorials on the Unix operating system and the C language and sessions for beginners to advanced users will be held. Bulletins of information are available from Uni-Ops, POB 5182, Walnut Creek, CA 94596, (415) 933-8564.

January 11-15
Applied Interactive Computer Graphics, University of Tennessee Space Institute, Tullahoma, TN. Lectures by Sylvan Chasen, Bertrand Herzog, and Carl Machover are the main features of this conference. For technical information, call Dr. F. W. Donaldson (615) 455-0631. For general information, contact Jules Bernard at (615) 455-0631.

January 12-15
Communication Networks Conference and Exposition, Georgia World Congress Center, Atlanta, GA. The Communication Networks Conference is designed to bring users and the telecommunication industry together. The Conference features sessions, panel discussions, and tutorials on voice, data, and electronic-mail communications. For information, contact Communication Networks, 375 Cochituate Rd., POB 880, Framingham, MA 01701, (617) 879-0700.

January 15-16
Microcomputers in Education, Uses for the 80s, Arizona State University, Tempe, AZ. The Tenth Annual Math/Science Conference will emphasize the microcomputer as a medium for instruction, as a tool for research, and as an information manager. Workshops, demonstrations, panel discussions, and problem-solving groups will be offered. Contact Nancy Watson, 203

Payne Hall, Arizona State University, Tempe, AZ 85287. Vendors interested in exhibiting may contact Dr. Gary Bitter, 203 Payne Hall, Arizona State University, Tempe, AZ 85287, (602) 965-3322.

January 19-22
Hands-on Pascal Workshop, Washington, D.C. The Hands-on Pascal Workshop is a four-day course designed by Integrated Computer Systems (ICS). Teams of three will be provided with an Apple Pascal system for use throughout the course. Some of the skills to be taught will be coding in Pascal, using structured programming techniques, and controlling real-time devices. For more details, contact ICS, 3304 Pico Blvd., POB 5339, Santa Monica, CA 90405, (800) 421-8166; in California (800) 352-8251.

January 19-22
Peripheral Array Processors for Signal Processing and Simulation, Sheraton National Hotel, Washington, D.C. The fee for this course is $795. For complete details, contact the Continuing Education Institute, Suite 1030, 10889 Wilshire Blvd., Los Angeles, CA 90024, (213) 824-9545.

In order to gain optimal coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, POB 372, Hancock NH 03449. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

January 19-22
The Which Computer? Show, National Exhibition Centre, Birmingham, England. Information about this show can be obtained from Clapp & Poliak, Inc., 245 Park Ave., New York, NY 10167, (800) 223-1956; in New York (212) 661-8410.

January 20-22
Texas Computer Show, Dallas Convention Center, Dallas, TX. Conferences, panel discussions, and seminars will be featured at this show. The exhibition will include word- and data-processing equipment plus peripherals. Contact the Texas Computer Show, POB 214035, Dallas, TX 75221, (214) 761-9108; in Georgia (404) 452-0114; in Canada (416) 252-7791.

January 21-23
The First Annual Pacific Computer Exposition, San Diego Convention and Performing Arts Center, San Diego, CA. This computer show will feature approximately 200 exhibitions of software and hardware of interest to business, industry, education, and homeowners. Contact Gloria Williams, c/o Williams Professionals, Suite 150, 2333 Camino Del Rio S., San Diego, CA 92108, (714) 296-4025.

January 26-29
Computer Graphics, San Francisco, CA. Computer Graphics is a four-day course designed by Integrated Computer Systems (ICS). The course provides an overview of the state of the art in computer-graphics hardware, software, and applications. Topics include fundamentals,

color techniques, and how to select and implement equipment in graphics applications. Contact ICS, 3304 Pico Blvd., POB 5339, Santa Monica, CA 90405, (800) 421-8166; in California (800) 352-8251.

January 28-30
Conference on Modeling and Simulation on Microcomputers, Bahia Hotel, San Diego, CA. The Society for Computer Simulation (SCS) is presenting this conference, which features papers, panel discussions, and tutorials on discrete and continuous simulation on microcomputers. Contact SCS, POB 2228, La Jolla, CA 92038, (714) 459-3888.

February 1982

February 1-3
The 1982 Instructional Computing Conference, Orlando, FL. The objectives of the conference are to provide insights into the use of computers in education, provide information on hardware and courseware for instructional computing, provide contact with persons now using instructional computing in Florida, and to cover trends in educational technology. Contact J. Warren Binns, State of Florida Dept. of Education, Tallahassee, FL 32301.

February 14-18
The Kuwait Information Management Exhibition: INFO Kuwait, Kuwait International Exhibition Center, Kuwait. Industrial executives from the Middle East are among those expected to attend this conference. Exhibits and speakers will be featured. Contact Clapp & Poliak International, 7315 Wisconsin Ave., Washington, D.C. 20014, (301) 657-3090.

February 18-19
Computer/Micrographics Interface, Stouffer's Greenway Plaza, Houston, TX. The Computer/Micrographics Interface is designed for information managers, systems analysts, micrographics systems analysts, records managers, and others who need information on computer and micrographic technologies. The course is presented by the Battelle Research Institute. Contact Battelle Seminars and Studies Program, 4000 Northeast 41st St., Seattle, WA 98105, (800) 426-6762; in Washington (206) 527-0542.

February 18-19
The Second Annual Talmis Conference and Exhibit, Chicago, IL. The Talmis Conference will focus on educational and reference media for the institutional, training, home-computer, and video markets. Local computer networks in education, the market for electronic educational and reference media in the home, software piracy, and other topics will be discussed. Exhibits of products and services will be featured. The registration fee is $450. For more information, contact Talmis, 115 North Oak Park Ave., Oak Park, IL 60301, (312) 848-4001.

February 22-24
The Eighth Federal DP Expo, Sheraton Washington Hotel, Washington, D.C. More than 150 computer companies will display and demonstrate hardware and software systems and services at the Federal DP Expo. Conferences on data processing and office automation will be held. Approximately 120 computer-industry experts will speak. Contact The Interface Group, 160 Speen St., Framingham, MA 01701, (800) 225-4620; in Massachusetts (617) 879-4502.

February 23-25
Computers and Automated Office Systems Exhibit for Caribbean Markets, Holiday Inn, Paradise Island, Nassau, Bahamas. This show is intended to bring together buyers and distributors with the industry. Exhibits of equipment for businesses in the Caribbean will be featured. For more details, contact Ormand Vee Co., 8852 Leslie Ln., Desplaines, IL 60016, (312) 635-7347.

February 26-28
Computer Expo '82, Tupperware Convention Center, Orlando, FL. Focusing on computers in education, business, industry, professional trades, and the home, the Computer Expo '82 will feature exhibits of computers and peripherals. It is sponsored by Adventure International. General admission is $5. For details, contact Computer Expo '82, 377 East Highway 434, POB 1185, Longwood, FL 32750, (305) 339-1731.

March 1982

March 1-4
Robots VI Conference and Exposition, Cobo Hall, Detroit, MI. An estimated 6000 manufacturing executives and engineers are expected to attend the Robots VI Conference, which features the latest in robotics technology and equipment. Among the topics to be addressed are assembly, foundry operations, aerospace applications, vision and handling, research

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and development, and sessions on human factors associated with robotics. Cincinnati Milacron, Unimation, and Hitachi America are a few of the companies that will be exhibiting at this show. The show is being sponsored by Robotics International of the Society of Manufacturing Engineers (RI/SME). Contact the RI/SME, One SME Dr., POB 930, Dearborn, MI 48128, (313) 271-1500, ext. 416.

March 2-4

The 1982 Vancouver Island Business Show, Empress Hotel, Victoria, British Columbia, Canada. The Vancouver Island Business Show features word-processing, communications, and office systems. The show provides the Vancouver Island business community with the opportunity to meet face-to-face with many Canadian suppliers of computer equipment. For information, contact Southex Exhibitions, 202-2695 Granville St., Vancouver, British Columbia, V6H 3H4, Canada, (604) 736-3331. In eastern Canada, contact Judy Hurd, 1450 Don Mills Rd., Don Mills, Ontario, M3B 2X7, Canada, (416) 445-6641.

March 7-10

The Eleventh Annual TI-MIX Symposium, Las Vegas Hilton, Las Vegas, NV. TI-MIX is an organization for Texas Instruments computer users. Its annual symposium features exhibits, a business meeting, and a new products workshop. Individual presentations, panel discussions, and workshops are planned. Contact TI-MIX, M/S 2200, POB 2909, Austin, TX 78769, (512) 250-7151.

March 9-11

The 1982 International Zurich Seminar on Digital Communications, Zurich, Switzerland. The theme of this seminar is "Man-Machine Interaction." Its aim is to present recent advances in theory and applications of digital-communication systems. Services, facilities, ergonomics, and their impact on peripheral equipment, systems architecture and design, as well as I/O (input/output) concepts and principles, will be covered. For details, contact Secretariat '82 IZS, M. Frey, EAE, Siemens-Albis AG, POB CH-8047, Zurich, Switzerland.

March 10-12

Cincinnati Business Show, Cincinnati Convention Center, Cincinnati, OH. The Cincinnati Business show features the latest in business technology, office systems, and products. Seminars will also be presented. For information, contact Ray G. Nemo, 5679 Creek Rd., Cincinnati, OH 45242, (513) 531-5959.

March 19-21

The Seventh West Coast Computer Faire, Civic Auditorium and Brooks Hall, San Francisco, CA. Attendance this year is expected to reach 35,000. More than 300 exhibitors and a wide assortment of seminars make this one of this largest annual computer shows. For more information, contact The Computer Faire, 333 Swett Rd., Woodside, CA 94062, (415) 851-7075. ■

Clubs and Newsletters

Program Innovators

Program Innovators is a new club for Texas Instruments TI-99/4 programmers and enthusiasts. For information, contact Gene Hitz, 2007 North 71st, Wauwautosa, WI 53213, (414) 453-0499.

Intel Has Solutions

Articles on single-board computers, notes on how to use Intel programmable-memory integrated circuits, new Intel products, new literature, and microcomputer workshops are included in *Solutions*, a bimonthly publication available free from Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051, (408) 987-8080.

Computers In Education

The New Hampshire Association for Computer Education Statewide (NHACES) has evolved to serve in an advisory capacity to public school educators regarding computer education and the use of computers in public schools in New Hampshire. NHACES is working to increase computer literacy and the use of computers in schools, improve the quality of computer education, and coordinate the dissemination of information regarding computer education, hardware, and software. Directories of products and services will be developed, maintained, and distributed to all members of NHACES. For complete details, contact NHACES, c/o Richard F. Antonak, Department of Education, University of New Hampshire, Durham, NH 03824.

VoiceNews Reports on Speech Technology

VoiceNews is a new publication devoted to speech-synthesis and speech-recognition technology. Published ten times a year, *VoiceNews* describes speech products such as integrated circuits, boards, peripherals, and systems. The newsletter also reports on applications for speech I/O (input/output), exhibitions, companies, courses, conferences, and other events in the voice-technology field. Subscriptions to *VoiceNews* are $95 per year. Contact Stoneridge Technical Services, POB 1891, Rockville, MD 20850, (301) 424-0114.

Apples In North Carolina

TAC (Triad Apple Core) is made up of Apple users interested in home and business applications for the Apple. *TAC Notes* is the club's monthly newsletter. For information, contact Mitzi T. Grey, Triad Apple Core, POB 1624, Lexington, NC 27292, (704) 352-7126.

FORTRUG

FORTRUG is interested in popular computers for personal, hobby, and business uses. The club meets monthly on the third Tuesday at 7 p.m. at the Corsair Computer Corporation, 7952 Highway 80, West Fort Worth, TX 76116. Meetings cover applications, programming, problem solving, and idea exchange. A majority of members use TRS-80 computers. No dues or fees are collected. FORTRUG can be contacted at the above address or by calling Linda Gill, (817) 731-8439, or Patrick Coyne, (817) 429-7055.

TRS-80 Color Computer Newsletter

The Rainbow is a monthly newsletter dedicated to Radio Shack's TRS-80 Color Computer. A typical issue contains feature stories, hints and tips on operation, sample programs, and reviews of new products. Annual subscriptions are $12. Contact *Rainbow*, 5803 Timber Ridge Dr., Prospect, KY 40059, (502) 588-6171.

South Florida Computer Group

SFCG (South Florida Computer Group) has user groups for 6800, 8080, Z80, TRS-80, PET, Apple, Digital Group, and other microcomputer systems. The Miami and Fort Lauderdale areas are covered by SFCG's two sections. They publish the *I/O Newsletter*.

The SFCG Fort Lauderdale Section meets on the second Monday of each month at 8 p.m. Membership and newsletter are $8 per year. Contact SFCG, Fort Lauderdale Section, POB 698, Hollywood, FL 33022, (305) 922-0935.

The Miami Section of the SFCG meets on the third Tuesday of each month at 8 p.m. Membership and newsletter are $5 per year. For information, contact SFCG, Miami Section, 240 Northwest 203 Terrace, Miami, FL 33169, (305) 653-0669.

IBM Personal Computer Group

The Philadelphia Area IBM Personal Computer User Group has been formed. Group activities are sponsored, and a monthly newsletter is planned. Members of other IBM Personal Computer groups are invited to submit articles and ideas to the newsletter and the group. For information, contact Craig W. Uthe, 4101 Spruce St., Apt. 311, Philadelphia, PA 19104, (215) 387-8208.

Osborne Software Users

The Osborne Business Software Users Group promotes the use of Osborne/McGraw-Hill software. A newsletter is planned, and assistance to new users on implementation of the software will be provided. Membership fees are $10, which entitles you to a newsletter subscription, bug reports and fixes, and access to compatible business software on 8-inch disks. Contact the Osborne Business Software Users Group, Suite 11, 2256 Main St., Otay, CA 92011, (714) 423-0538.

Computer Telephone Directory

The On-Line Computer Telephone Directory is a quarterly publication that provides information on computer bulletin-board systems and software, terminal equipment and software, and telephone numbers of free-access bulletin-board systems across North America. Contact *The On-Line Computer Telephone Directory*, POB 10005, Kansas City, MO 64111.■

Software Received

Apple

Ampergraph, a graphics utility program for the Apple II. Floppy disk, $25. Midwest Software, POB 9822, Madison, WI 53715.

Cribbage, a board game for the Apple II. Floppy disk, $24.95. On-Line Systems, 36575 Mudge Ranch Rd., Coarsegold, CA 93614.

Discounted Cash Flow/ Manufacturing Costs Estimator, a business package for manufacturing and engineering applications for the Apple II. Floppy disk, $149. Centec, Inc., 11260 Roger Bacon Dr., Reston, VA 22090.

Disk Prep, a disk-testing and formatting program for the Apple II. Floppy disk, $25. Sympathetic Software, 9531 Telhan Dr., Huntington Beach, CA 92646.

Event Cruncher, critical-path-method analysis program for the Apple II. Floppy disk, $85. Notforhire Software, 1671B River Village, Fort Belvoir, VA 22060.

Fender Bender, an arcade game for the Apple II. Floppy disk, $24.95. California Pacific Computer, 1623 Fifth St., Davis, CA 95616.

Genetic Drift, a graphics arcade game for the Apple II. Floppy disk, $29.95. Brøderbund Software, 2 Vista Way, San Rafael, CA 94901.

The Graphics Printing System, screen-graphics printing system for the Apple II. Floppy disk, $109.95. Progressive Software, Suite 323, Blue Bell West, Blue Bell, PA 19422.

Handicapped Typewriter, Version 2, a "non-keyboard typewriter" program for the physically disabled for the Apple II. Floppy disk, $99. Rocky Mountain Software, 214-131 Water St., Vancouver, British Columbia, V6B 4M3, Canada.

Orbitron, an arcade game for the Apple II. Floppy disk, $29.95. Sirius Software, 2011 Arden Way #225A, Sacramento, CA 95825.

Painter Power, a high-resolution-graphics development system for the Apple II. Floppy disk, $39.95. Micro Lab, Inc., 2310 Skokie Valley Rd., Highland Park, IL 60035.

Print II, a print-formatting utility for the Apple II. Floppy disk, $24.95. Computer Systems Design, 2139 Jackson Blvd., Rapid City, SD 57701.

SAT English 1, a tutorial program for the Apple II. Floppy disk, $25. Micro Lab, Inc. (see address above).

Shuffleboard, a graphics arcade game for the Apple II. Floppy disk, $29.95. Innovative Software Design, Inc., POB 1658, Las Cruces, NM 88004.

Space Quarks, a graphics arcade game for the Apple II. Floppy disk, $29.95. Brøderbund Software (see address above).

Star Thief, a graphics arcade game for the Apple II. Floppy disk, $29.95. Cavalier

Computer, POB 2032, Del Mar, CA 92014.

Stock Forecasting System, a program for stock investors for the Apple II. Floppy disk, $175. Urban Aggregates, Inc., 6431 Brass Knob, Columbia, MD 21044.

Universal Graphics, high-resolution graphics development package for the Apple II. Floppy disk, $39.95. Sympathetic Software (see address above).

TRS-80

Asylum, a graphics adventure for the TRS-80 Model I or III. Floppy disk, $19.95. Med Systems Software, POB 2674, Chapel Hill, NC 27514.

Atlantean Odyssey, a graphics adventure for the TRS-80 Model I. Floppy disk, $29.95. Interpro, POB 4211, Manchester, NH 03108.

Blockade, a graphics arcade game for the TRS-80 Color Computer. Cassette, $14.95. Interpro (see address above).

Color Computer Disassembler, a utility program for the TRS-80 Color Computer. Cassette, $19.95. Interpro (see address above).

Domes of Kilgari, an adventure game for the TRS-80 Model I and III. Cassette, $19.95. The Programmer's Guild, POB 66, Peterborough, NH 03458.

Invasion Force, a strategy game for the TRS-80 Model I. Cassette, $14.95. Radio Shack, One 1800 Tandy Center, Fort Worth, TX 76102.

Package #1, five graphics arcade games for the TRS-80 Model I Level II. Cassette, $7. Programmable Software, 508 Margin Rd., Lebanon, PA 17042.

Raaka-Tu, an adventure game for the TRS-80 Level II, Models I and III. Cassette,

Atari

Forest Fire, a fire-fighting simulation for the Atari 800. Floppy disk, $20.95. Dynacomp, Inc., 1427 Monroe Ave., Rochester, NY 14618.

Galactic Chase, a graphics arcade game for the Atari 400/800. Cassette, $24.95; floppy disk, $29.95. Spectrum Computers, 26618 Southfield, Lathrup Village, MI 48076.

Stud Poker, a card-game program for the Atari 800. Floppy disk, $15.95. Dynacomp, Inc. (see address above).

Supergraphics, a three-dimensional graphics and color game development system for the Atari 800. Floppy disk, $39.95. United Software of America, 750 Third Ave., New York, NY 10017.

North Star

Cranston Manor Adventure, an adventure game for the North Star. Floppy disk, $21.95. Dynacomp, Inc., 1427 Monroe Ave., Rochester, NY 14618.

Renumber, a utility program for the North Star. Floppy disk, $39.50. Electronic Technicians Software Services, 1072 Casitas Pass Rd., Carpinteria, CA 93013.

Scan, a utility program for the North Star. Floppy disk, $29.50. Electronic Technicians Software Services (see address above).

$14.95. Radio Shack (see address above).

Space Warp, a strategy game for the TRS-80 Level II, Models I and II. Cassette, $14.95. Radio Shack (see address above).

Ultra-Mon, a utility program for the TRS-80 Model I. Cassette, $24.95. Interpro (see address above).

Wordsmith, a word-processor program for the TRS-80 Model I Level II. Cassette, $14.95. ABS Suppliers, Suite 4A, 3003 Washtenaw, Ann Arbor, MI 48104.

This is a list of software packages that have been received by BYTE Publications during the past month. The list is correct to the best of our knowledge, but it is not meant to be a full description of the product or the forms in which the product is available. In particular, some packages may be sold for several machines or in both cassette and floppy-disk format; the product listed here is the version received by BYTE Publications.

This is an all-inclusive list that makes no comment on the quality or usefulness of the software listed. We regret that we cannot review every software package we receive. Instead, this list is meant to be a monthly acknowledgment of these packages and the companies that sent them. All software received is considered to be on loan to BYTE and is returned to the manufacturer after a set period of time. Companies sending software packages should be sure to include the list price of the packages and (where appropriate) the alternate forms in which they are available.

ZX-80

Super Z, extended BASIC commands for the Sinclair ZX-80. Cassette, $9.95. Lamo-Lem Laboratories, POB 2382, La Jolla, CA 92038.

ZX-80 Home Computer Package, utility and graphics programs for the Sinclair ZX-80. Cassette, $9.95. Lamo-Lem Laboratories (see address above).

Other Computers

IBMPAK, a program to convert Flex files to IBM format for 6809-based Flex systems. Floppy disk, $125. Helix Enterprises, 504 Fort Drum Dr., Austin, TX 78745.

Magic Typewriter Ver 3.0, a word-processing system for CP/M. Floppy disk, $350. California Digital Engineering, POB 526, Hollywood, CA 90028.

Management Simulator, a business simulation for CP/M. 8-inch disk, $26.45. Dynacomp, Inc., 1427 Monroe Ave., Rochester, NY 14618.

Rubik Cube Unscrambler Program. BASIC program listing, $12. Wray, 31 Church Green, Totternhoe, Dunstable, Bedfordshire, LU6 1RF, England.

Unica and XM-80, a Unix-like operating system for CP/M and a macroassembler for the Z80. Floppy disk, $195. Knowlogy, POB 283, Wilsonville, OR 97070.

Valdez, a maritime simulation for CP/M. 8-inch disk, $22.45. Dynacomp, Inc. (see address above)..■

An Effective Text-Compression Algorithm

David Cortesi
2340 Tasso St.
Palo Alto, CA 94301

It is often desirable to be able to *compress* data: to encode it in a shorter form than normal so that it takes up less storage space. In a recent case, I found it essential. I was constructing a word-processing system based on a computer that had only 4096 bytes of memory. Into that tiny space, I had to cram the program as well as words for it to process.

Choice of compression algorithm is dictated by the data characteristics and the amount of space and running time tolerable in the compressing and decompressing routines. In this case, the data was general English text, which is probably the least compressible of any. The compression routines had to be small and simple, but not necessarily fast.

After some figuring, I came up with an algorithm that was fairly simple to implement, quick in execution, and effective. It can usually squeeze text to 75% of its original size. While it may have been written before, the algorithm was new to me. Anyone who needs to compress general text may find it useful, too.

The branch of mathematics called information theory says that data is compressible in so far as it is predictable. That is, the minimum number of bits needed to convey a particular message (using message to mean a piece of information) depends on how many unique messages might be sent. At one limit, if only two messages are sent or stored, then only one bit is needed to encode them. Paul Revere's warning signal in the tower of the Old North Church could have been such a system: "0 = land, 1 = sea." (Historically, the famous signal was, of course, "one if by land, two if by sea.") At the other extreme, if absolutely any message at all might be sent, then an infinite number of bits would be needed to encode any single message uniquely.

Ordinary data falls somewhere between those theoretical limits, usually much closer to the one-bit end than to the other. For any list of practical messages, a theoretical minimum number of bits is needed to represent any one message. Often, the number of bits actually used to store information is larger than the theoretical minimum. The excess bits are *redundant*. The aim of data compression is to remove as much redundancy as possible.

Character data encoded in the ASCII (American Standard Code for Information Interchange) format constitutes a set of 128 possible messages. Any of the 128 pieces of information can be encoded in 7 bits, as a binary number between 0 and 127. Microprocessors designed around an 8-bit word store ASCII characters one per word, for convenience. The inconvenient alternative is to store one and one-seventh characters per word, which would complicate programs considerably. This convenience is bought at a cost of 12% redundancy (1 redundant bit in 8).

Any one collection of data may have even more redundancy. A program in BASIC uses only the uppercase letters, digits, and limited punctuation; fewer than 64 unique characters. The BASIC vocabulary of possible messages could be represented in a code of just 6 bits per character. It's feasible to write a program that would compress a BASIC source file so that every 3-byte group expresses four 6-bit letters. This compression is achieved by predicting and encoding for a smaller vocabulary of messages in the data.

Another type of compression requires knowledge of another kind of predictable characteristic: the statistical distribution of messages in the data. If you could confidently predict that, for example, 50% of all the characters in a file were the letter Z, you could arrange an encoding based on these rules:

- a 1 bit stands for Z
- a 0 bit says "take the next 7 bits as an ASCII character other than Z"

This would produce a nice compression. Fifty percent of the letters in the file (the Zs) would be stored as single bits; the other 50% as groups of 8 bits. The average number of bits used to store a character would be 4.5. This scheme can be generalized by adding more rules, until every *n*th-commonest letter is encoded in exactly by *n* bits (i.e., the most common character is encoded in 1 bit, the second most common is encoded in 2 bits, and so on).

Two things are wrong with this scheme and its generalized variations. It isn't effective unless each character is stored as a variable number of bits,

About the Author
David Cortesi has had extensive experience in the computing world, including work in the fields of machine repair and marketing and as a developer of interactive software. He recently dropped out of the mainframe computer business to write about, and experiment with, personal computers.

Listing 1: *Text-compression algorithms as described in the text, written in a loosely structured pseudocode based on Pascal. The notation @pointer means "the byte addressed by pointer."*

```
procedure COMPRESS( ADIN: points to the input;
                    ADOUT: points to the output)

   local bytes THIS, THAT,
   local numbers FIRST, SECOND.

   REPEAT
      BEGIN
         THIS := @ADIN                    (pick up next character)
         FIRST := MEMBER(THIS,13)
         IF ( FIRST ≠ 13 ) THEN           (THIS is in the long list)
            BEGIN
               THAT := @(ADIN+1)          (check the next byte)
               SECOND := MEMBER(THAT,8)
               IF ( SECOND ≠ 8) THEN      (THAT is in short list)
                  BEGIN                   (build a digraph)
                     THIS := a digraph made from FIRST & SECOND
                     ADIN := ADIN+1
                  END
               ENDIF
            END
         ENDIF
         @ADOUT := THIS                   (store byte or digraph)
         ADOUT := ADOUT+1                 (and bump the pointers)
         ADIN := ADIN+1
      END
   UNTIL ( THIS = string-end-marker byte)
END COMPRESS

function MEMBER( LETTER: a byte; LISTSIZE: a number)
         RETURNS a number

  (this function returns the origin-zero index of LETTER in
   TABLE if it is there, or a failure signal if it is not.
   For clarity the signal is shown as a too-high index, but
   it could be anything, e.g. setting the carry flag.)

   local pointer P, local number T.

   P := address of TABLE (point to " etaoinshrdlu")
   T := LISTSIZE

   REPEAT
      BEGIN
         IF ( LETTER = @P ) THEN GOTO FOUND
         P := P+1
         T := T-1
      END
   UNTIL ( T=0 )
   RETURN LISTSIZE   (indicate failure)

FOUND:  (LETTER is in the first LISTSIZE elements of TABLE;
         at this point T is in the range LISTSIZE..1)
   RETURN LISTSIZE-T  (..origin-zero index)
END MEMBER
```

Listing 1 continued:

```
procedure DECOMPRESS( ADCOMP: points to the compressed input;
                      ADNORM: points to the output)

   local bytes THIS, THAT,
   local number T.

   REPEAT
      BEGIN
         THIS := @ADCOMP
         IF ( Bit 7 of THIS is a 1 ) THEN
            BEGIN
               T := extracted bits "aaaa" of THIS
               @ADNORM := TABLE[T]
               ADNORM := ADNORM+1
               T := extracted bits "bbb" of THIS
               THIS := TABLE[T]
            END
         ENDIF
         @ADNORM := THIS (store 2nd or only character)
         ADNORM := ADNORM+1
         ADCOMP := ADCOMP+1
      END
   UNTIL ( THIS = string-end-marker byte )
END DECOMPRESS
```

without regard to the word size of the processor. This usually makes the compression and decompression processes complex and slow. Second, it won't work at all if the prediction of letter frequencies is wrong. If the two rules above are applied to a file that contains no Zs, then all letters will fall under the second rule and be stored as 8 bits, one more than necessary. In general, if the data is not as predicted, this algorithm will expand it instead of compressing it. The more rules in the algorithm, the more predictions the computer makes about the data, and the greater the error when the predictions are wrong.

Let's try another approach to compression and accept that it's a practical necessity to respect the machine's 8-bit word boundaries. Each word can represent any one of 256 messages. Is there a way to make full use of all 256 messages? If so, we would eliminate at least the basic 12% redundancy. If some of the new messages can be made to stand for groups of the old ones (the ASCII characters) then even more redundancy would be eliminated.

A word of caution. The computer makers already may have made

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assumptions about that "unused" eighth bit in a character byte (the most significant bit, usually designated as bit 7). For example, most firmware monitors assume it is a parity bit and clear it to zero when exchanging a byte with a terminal (thus defeating any value it may have had as a parity check, but never mind). Some video boards use the bit to distinguish the normal character set from a set of 128 graphics symbols. Still, if the compressed data is kept only in storage or in a file and is always decompressed for transmission to a peripheral, it's probably safe to use the eighth bit. That gives us an expanded alphabet of 256 characters to play with, 128 of them new and uncommitted.

One common use of these byte values is the implementation of *run-length encoding*. Each of the 128 new characters is interpreted by these rules:

- set bit 7 to 0, then
- take the resulting integer and replicate the byte that follows it that many times

With this algorithm any string of 3 to 130 identical characters can be expressed in just two bytes. The first byte is one of the new characters; it signals a run of identical characters and tells its length. The second byte indicates the repeated character. When the data predictably contains runs of like characters, then run-length encoding compresses very well. Unfortunately, the general English text with which a word processor must deal contains almost no runs of characters.

I hit upon the idea of using the extra 128 byte values to represent pairs of letters, or *digraphs*. Putting a pair of letters in a single byte will certainly result in compression, but the expanded alphabet will only accommodate 128 unique pairs over and above the standard ASCII characters. To result in compression, the pairs that are encoded must be the pairs that can be predicted to occur the most frequently. Another requirement is that it must be very easy to identify a compressible pair, so that the compression code can be simple. Cryptographers have compiled lists of the frequency of use of digraphs in English. It would be possible to include a table of the 128 most frequent digraphs in the compression routine. But that would require 256 bytes of precious space and entail a lengthy search over the list for every pair of candidate letters.

Cryptographers and printers have long known the sequence "etaoinshrdlu" as the frequency order of the twelve most common letters in English. The same letters are the most common in all the Romance languages, although the order varies. Here is one prediction that can be made with confidence about any sample of text. Inside a computer, the blank space is a letter on par with the others, probably the most frequent one of all, so it should be added to the head of the list.

I reasoned that if these are the most common individual letters, then pairs of letters from that list will be common; not necessarily the most common, but frequent enough to result in compression. That has proved to be the case. The basic notion of the algorithm is to find adjacent pairs of letters in which both letters are on the list of the most frequently occurring letters and make digraph bytes of those pairs.

I chose the following organization for a digraph byte: 1aaaabbb. Bit 7 is set to 1 to signal a digraph. The next four bits, aaaa, represent a binary number in the range 0..12 and stand for the first letter of the pair. The least significant three bits, bbb, are a number in the range 0..7 and stand for the second letter of the pair. This sort of bit manipulation is usually difficult and always obscure in a high-level language. In machine language, it is easy to partition a single byte into two or more groups. Notice that it isn't possible to include two 4-bit numbers plus a flag bit in 1 byte. The digraphs that can be encoded in this way are the 104 pairs whose first character is one of the thirteen letters "(space)etaoinshrdlu" and whose second member is one of the shorter list of eight letters "(space)etaoins." A side benefit of this encoding is that, because the bits marked "aaaa" won't

be used for a number larger than 12, it will never form a byte of the binary form "1111xxxx." The 16 byte values of this form could be used to implement run-length encoding for runs of 3 to 18 characters if that were desired.

I had to implement the algorithm in a tedious manner: by hand-assembling the machine-language instructions and typing them as hexadecimal numbers. This process is likely to produce both typographical and logic errors. To minimize the chance of logic errors, I first wrote the algorithm in a pseudocode, which is a program written in a precise way but not necessarily in any real programming language. Since the pseudocode program will never be read by a machine, one is free to use any kind of notation that will make the meaning clear.

For this project, I carried the pseudocode to a very fine level of detail so that I could translate it directly into machine instructions (see listing 1). Most of its conventions are those of Pascal, loosened and simplified. The notation *@pointer* is a concession to the needs of machine-language programming; it means "the byte addressed by *pointer*."

Procedure COMPRESS is called to compress a single line of characters; the line is terminated by some special character such as a carriage-return. It inspects the line from left to right. If a character is not in the list of thirteen common letters, it is simply copied to the output string; if the copied byte is the end-marker, then the procedure is completed.

When a specific letter is found in the list of thirteen common letters, the next character is tested against the first eight letters of the same list. If it, too, is found, the indices corresponding to the two letters are combined into a single byte and the combined byte is stored.

Function MEMBER tests a character for membership in the list of frequent letters. When it finds the letter in the list, it returns the letter's index in the list, counting from zero. Such origin-zero indices are more convenient to use at the level of machine language. If the character does not

```
Make me a willow cabin at your gate,
And call upon my soul within the house;
Write loyal cantons of contemned love
And sing them loud even in the dead of night;
Halloo your name to the reverberate hills,
And make the babbling gossip of the air
Cry out "Olivia!" O, you should not rest
Between the elements of air and earth,
But you should pity me!

Mak(e )m(e )(a )wil(lo)w cab(in)( a)(t )you(r )g(at)e,
An(d )cal(l )up(on) my( s)ou(l )w(it)(hi)(n )t(he) (ho)(us)e;
W(ri)(te) (lo)ya(l )c(an)(to)(ns)( o)f c(on)(te)m(ne)(d )(lo)ve
An(d )(si)ng( t)(he)m (lo)u(d )ev(en)
                         ( i)(n )t(he) (de)a(d )of( n)ig(ht);
Hal(lo)(o )you(r )(na)m(e )(to)( t)(he)
                         (re)verbe(ra)(te) (hi)l(ls),
An(d )mak(e )t(he) babb(li)ng g(os)(si)p( o)f( t)(he)( a)ir
Cry( o)(ut) "O(li)v(ia)!" O, yo(u )s(ho)ul(d )(no)(t )(re)(st)
B(et)w(ee)(n )t(he)( e)(le)m(en)(ts)( o)f
                          ( a)i(r )(an)(d )(ea)(rt)h,
B(ut) yo(u )s(ho)ul(d )p(it)y me!
```

Figure 1: *Effect of compression on a sample text, from* Twelfth Night. *Each parenthesized pair of characters would be stored as a single byte. There are 339 characters in the sample; 100 pairs are formed for a space saving of 29%.*

appear in the list, MEMBER returns a failure signal.

Procedure DECOMPRESS expands a line that had been processed by COMPRESS. Ordinary characters are just copied to its output. Digraph bytes are split up and the indices they contain are used to find the letters of the pair in the list of common letters.

Figure 1 illustrates the effect of the compression algorithm on a sample of data. The algorithm has proven quite effective. In fact, it is part of the micro word processor used to type this article. Of its 4096 bytes, about 2700 are available for data storage. Compression makes this the equivalent of about 3300 bytes, which is ample room for a typical letter or manuscript page.

The compression code itself occupies fewer than 150 bytes, and the processing overhead it adds is not perceptible in the program's response. I hope the algorithm will work as well in someone else's program as it worked in mine. ■

Ask BYTE

Conducted by Steve Ciarcia

Differing Views on Mail Order

There has been a lot of controversy lately concerning mail-order versus retail purchase of computer hardware. The following letters might help shed some more light on the issues. . . . **Steve**

Dear Steve,

Two recent letters in your column have really upset me. I am a computer-marketing representative for Radio Shack. I would like to address the letters from Jeff Goodling and Dave Storti. (See "Mail-Order Forum" in the October 1981 BYTE, page 316.) Mr. Goodling asks if Radio Shack is dumping defective products through mail order. All mail-order outlets are independent dealers. Some of these outlets openly advertise that they have modified the computer. Why, then, would someone take a chance on getting a modified or damaged piece of equipment when they could test it out locally? A great number of people have already learned that the few dollars saved through mail order isn't such a bargain.

Mr. Storti's case is one most computer representatives see nearly every week: the businessman who wants all that terrific local support and service but doesn't want to pay for it. There is no free lunch, Mr. Storti. That price difference represents the important hand-holding time I'm going to give you. That's something the mail-order folks don't care about. Radio Shack has a leasing plan through A & A Leasing (our own leasing company). I don't know where Mr. Storti came up with his maintenance costs, but it wasn't from a Computer center. Anyone who services an IBM, Wang, or Lanier for $400 to $800 a year less than the cost of service on a Model II is doing it for free, as the service on a Model II is $476 a year. Mr. Storti kept dwelling on a five-year life for his computer system. Four years from now, Mr. Storti will be trying to figure a way out of his lease because the system will be outdated.

Radio Shack is after the business market, and it's getting it. I can't get Model IIs fast enough. I was offered jobs with Apple, Digitial Equipment Corporation, and Data General but chose Radio Shack because I feel it has the best product for the money. Mr. Goodling and Mr. Storti both have the same problem. They expect Radio Shack to be all things to all people and do it for free. The "big guys" don't do it, and I don't think we should either. If either of these gentlemen wants to honestly and intelligently discuss the benefits of a TRS-80 versus any other system, he can call me at (304) 296-5492. Thank you.

Donald C. Kirkendall, Jr.
Morgantown, WV

Dear Steve,

About those mail-order TRS-80s . . .

I was recently involved in the purchase of a TRS-80 Model III through the mail-order firm Marymac Industries, Inc., operating out of the Houston area. We checked out Marymac's offer of local references and found out they included a nationally known, locally based electronics firm that had good things to say about Marymac.

On the strength of that, other references, and telephone conversations with various mail-order firms, we decided to buy from Marymac. It shipped exactly what we ordered on the day we ordered it, and our Model III arrived in six days (two of those were the weekend).

In short, Marymac did what it said it would do. (Incidentally, Marymac picked up the shipping charges.)

But, like many others, our Model III arrived with one of the drives out of commission. However, our encounter with the local Radio Shack Computer Center in Tempe, Arizona, and our request for repair service couldn't have been handled more professionally had we bought directly from the local store.

Store manager David Kelly and salesman Joe Rubey grimaced only slightly when we told them where we bought our "lame" Model III and then took us under their wing. They kept us informed as to how repair work was coming and called when it was ready to be picked up. And, of course, there was no charge.

In short, our mail-order purchase was very satisfactory. Our Model III is now in daily use, and we have been back to the local store for programs and supplies.

My only complaint is that with its Scripsit program up and running the Model III has become too popular in our office, so popular I couldn't get to it to write this letter.

Burton C. Kennedy
Phoenix, AZ 85003

A Loaded Question Answered

I have an answer to Dave Bower's letter, "A Loaded Question." (See the July 1981 "Ask BYTE," page 218.) The solution to the same problem appeared in the July 1978 issue of Radio Shack's *Microcomputer Newsletter*. The article, called "How to Merge Two Programs Using CLOAD Command," suggested this:

1. Make sure that the program to be merged (the one on cassette) has line numbers that are larger than the line numbers of the program located in memory.
2. Look at the contents of locations 16633 and 16634 using PRINT PEEK (16633), PEEK (16634). Write down the numbers.
3. If the contents of 16633 are 2 or greater, execute the following statements:

```
POKE 16548, PEEK (16633)−2:
POKE 16549, PEEK (16634)
```

Then go to step 5.

4. If the contents of 16633 are 0 or 1, execute the following statements:

```
POKE 16548, PEEK (16633)
    +254:
POKE 16549, PEEK (16634)−1
```

5. CLOAD the program from cassette. Then execute the statements:

```
POKE 16548, 233:
POKE 16549, 66
```

6. LIST, RUN, or CSAVE the merged program.

Mr. Bower also asks if there is a system tape to do this. The answer is yes. It is called Remodel & Proload and is manufactured by Racet Computes, Suite M, 1330 North Glassell, Orange, CA 92667, (714) 997-4950. It costs $35, and you must specify whether you have a 16 K-, 32 K-, or 48 K-byte machine. The Remodel & Proload can renumber any

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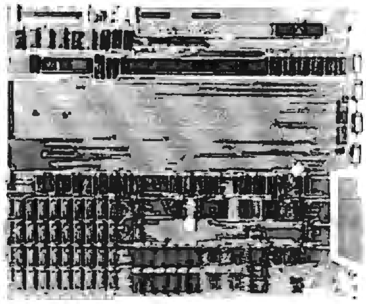

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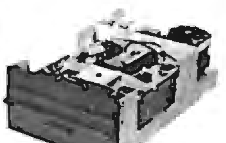

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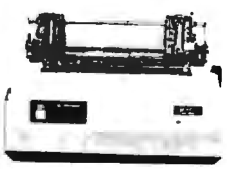

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portion or all of a BASIC program, move any portion of a BASIC program, delete lines or range of lines, merge all or any portion of a BASIC program from tape with renumbering on the way in, save combined and merged program or any portion of a program to tape, and verify the contents of the saved program bit-for-bit. Also, it allows you to selectively save and load a library of data statements, which is a more effective method of retrieving and loading data than using data-tape facilities.

A. C. Posada
Richmond, VA

Just like "Dear Abby," sometimes my readers provide advice that's more up-to-date. A case in point is my answer to Dave Bowers. I've received 20 letters that corrected me on this point. Thank you. . . . **Steve**

Small System Monitor

I have been looking for a Z80 system monitor that can fit into 1 K bytes of space, i.e., a 2708 EPROM (erasable programmable read-only memory). The functions I want are:

- dump memory content to console
- input data to memory through console keyboard
- execute program at user-specified address
- modify and display registers of the Z80 processor
- single-step of absolute program
- breakpoint of user program
- fill memory with user-specified data
- move memory contents from one place to another

Can you provide me with any such program, including source listings? I can do some patching to suit my system.

Albert K. Lee
Scarborough, Ontario, Canada

My latest book, Build Your Own Z80 Computer, *published by BYTE/McGraw-Hill, contains a rather complete 1 K-byte EPROM-resident monitor that does much of what you're looking for. It allows you to display and replace memory, display and replace registers, execute a program in a specified address, and it facilitates serial I/O (input/output). The complete source code is included with the book and can be easily modified to accommodate some of the breakpoint and single-step functions you would like. Contact BYTE Books, 70 Main St., Peterborough, NH 03458, (800) 258-5420; in New Hampshire (603) 924-9281.*

Also, the MicroWorks, POB 44248, Cincinnati, OH 45244, has a small monitor, which I've been using for a number of years, that has all of these features. (I cannot recall whether it's 1 K, it may be more.) MicroWorks' Program Stepper is everything you could want. It was designed to run on a Digital Group Z80 computer, but I'm sure it can be modified for your system. The source code, however, may not be available . . . **Steve**

Color-Monitor Bandwidths

Dear Steve,

What color monitor and what combination monitor/receiver would you recommend for 640 by 200 pixel graphics? What information should I look for when evaluating monitors? My local TV store is of no help at all on these questions. Also, can you recommend a reference to read on this subject?

Ronald I. Frank
Framingham, MA

I can't go into all of the details and theory, but I will try to answer your question. The bandwidth needed is calculated by dividing the active-trace time by the number of horizontal dots. In other words, 48 microseconds divided by 640 dots is 74 nanoseconds per dot, or 13.4 MHz.

These numbers are for a standard monitor. To get the value for the active-trace time for any other monitor, subtract from the reciprocal of the horizontal rate the percentage of time taken by the retrace and blanking intervals.

In modified television sets, the bandwidth is limited to about 8 MHz. For a good, inexpensive black-and-white monitor, the bandwidth usually ranges from 15 to 25 MHz. For color monitors that accept composite video, the bandwidth is about 3.5 MHz for the color information and 6 MHz for the luminance (brightness).

The only color monitors that have more than 3.5 MHz bandwidth are the kind that accept separate inputs for red, green, and blue (commonly called RGB monitors).

By the way, the monitor types I've listed above are also in order of increasing cost.

If you're looking for a good source for monitors, you might check the ads in BYTE. For information on video graphics, BYTE/McGraw-Hill (70 Main St., Peterborough, NH 03458, (800) 258-5420; in New Hampshire (603) 924-9281) has published a number of books on the subject. I would also recommend that you look up the NTSC (National Television Standards Committee) Television Standards Reference *at your library. . . .* **Steve**

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Sweet Talk

Dear Steve,

I read your September 1981 "Circuit Cellar" about the Votrax SC-01 speech synthesizer with great interest. (See "Build an Unlimited-Vocabulary Speech Synthesizer," page 38.) When it came to the parts list for the Sweet Talker, I noticed that the Micromint was offering an Apple II-compatible board as well. Your article said nothing about such a board. Is it different? Would you provide a schematic?

Harvey Kaye
Fort Wayne, IN

The article was written and submitted when I decided to design an Apple II version of the Sweet Talker. Initially I had designed a parallel version as a demonstration board for the SC-01. In the interim, however, I had a chance to review the response to the Digi-Talker-based Micromouth synthesizer presented in the June 1981 BYTE. (See "Build a Low-Cost Speech-Synthesizer Interface," page 46.) It was overwhelmingly Apple II owners!

In an effort not to ignore a substantial portion of the audience, I quickly designed an Apple II Sweet Talker and slipped it into the parts list.

The Apple II Sweet Talker plugs into any Apple II slot and interacts with the computer as a single I/O (input/output) port. Functionally, the operation of the SC-01 is exactly the same as the parallel version. Only the timing is different.

As figure 1 illustrates, the Apple II Sweet Talker contains an 8-bit parallel latch. A POKE to the board address will latch the phoneme data into integrated circuits 2 and 3. To accommodate the required data set-up time of the SC-01, IC6 delays the strobe 10 microseconds. The strobe delay is transparent to the computer and words are spoken simply by POKing the phoneme code to the board. Doing a PEEK at the board address examines the SC-01 busy line.

Finally, unlike the parallel version, the Apple II Sweet Talker is provided with a cassette of demonstration software written in Applesoft BASIC. A disk-based dictionary program is also available.

I apologize for the confusion. Sometimes writing and design leadtimes don't overlap enough. . . . **Steve**

Number	Type	+5 V	GND	+12 V
IC1	SC-01		18	1
IC2	74LS75	5	12	
IC3	74LS75	5	12	
IC4	7416	14	7	
IC5	74LS02	14	7	
IC6	74LS123	16	8	
IC7	74LS367	16	8	
IC8	LM386		4	6

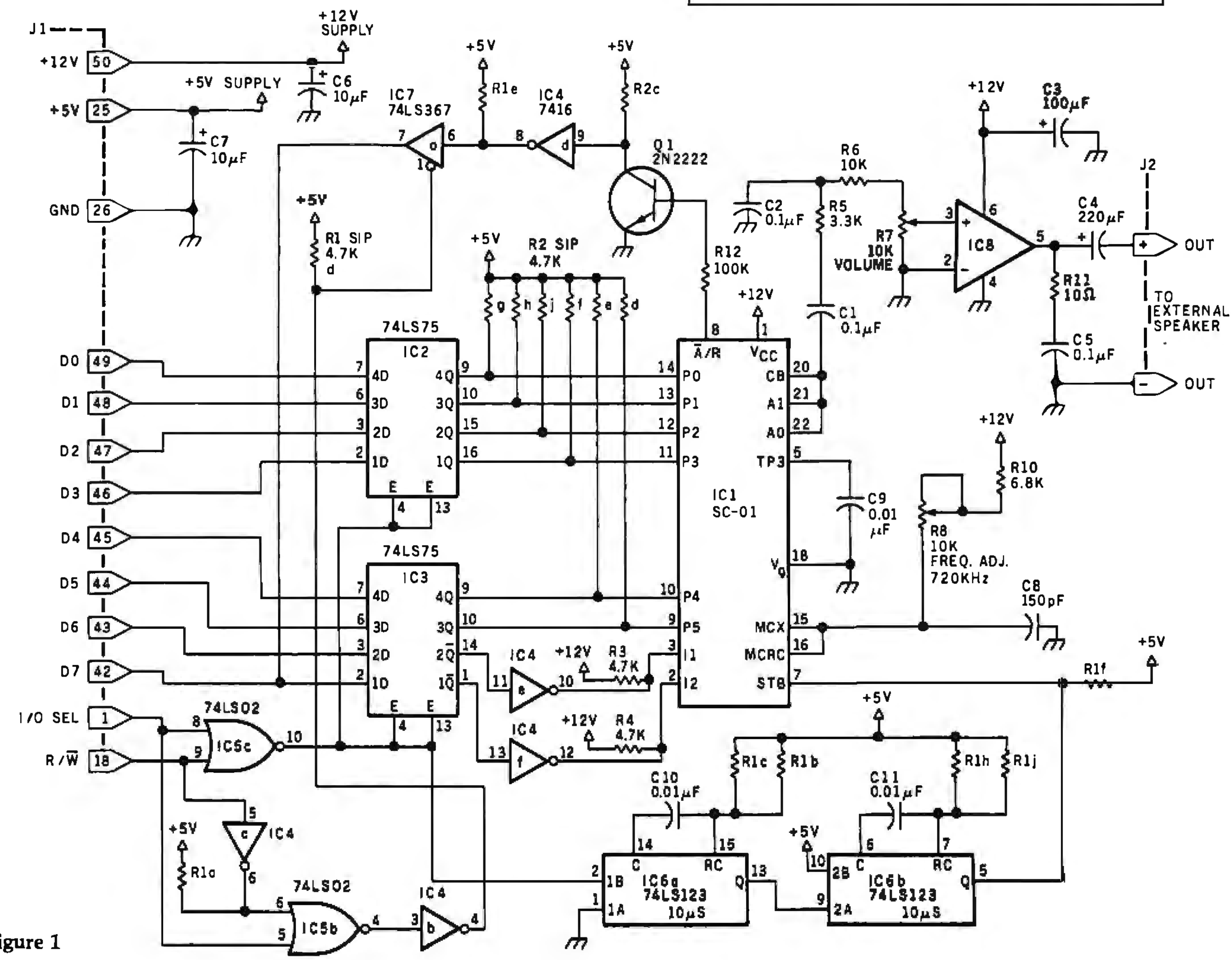

Figure 1

Low-Cost Monitor

Dear Steve,

Do you know where I can get a board that contains a microprocessor, a UART (universal asynchronous receiver/transmitter), and a television interface so that the board could be programmed to let a cheap ($80) television set be used as a data-line monitor (RS-232C asynchronous data)? I would like to be able to display data in both directions at all baud rates, with and without parity, and at different word lengths. I would also like to be able to recognize control codes and display them in some special format.

Single-board computer systems are now available that could be programmed to do this, but I would like to keep the cost below $300.

Edward L. Pavia
Webster, NY

Your best approach would be to use the Z8 BASIC computer-controller board presented in my July and August 1981 "Circuit Cellar" articles (see pages 38 and 50, respectively) and a low-priced terminal such as the ASCII Keyboard/Computer Terminal Kit offered by Netronics Research and Development, Ltd., 333 Litchfield Rd., New Milford, CT 06776, (800) 243-7428; in Connecticut (203) 354-9375. Netronics' 16-line by 64-character terminal ($149.95) plus the Z8 board ($195) is slightly more expensive than you requested, but it appears to me that it will meet your requirements. You would simply program your application in a 2716 EPROM (erasable programmable read-only memory) and set it to run on the BASIC computer-controller board. The only problem that I can see is at extremely high data rates you may be forced to use machine-language coding rather than BASIC.

I hope this helps. . . . **Steve**

More to Draw on

Dear Steve,

I own a Radio Shack TRS-80 Model I and am just beginning to realize its graphics potential.

I am now getting into three-dimensional animated work. Someday I may market a game using the techniques I've learned.

Although the TRS-80 has good graphics potential, I've decided it's not good enough. I don't think any computer currently on the personal-computer market today can satisfy my ever-growing imagination.

I have decided to try to build a vector-graphics display to be TRS-80-controlled and I am looking for information or ideas on low-cost, do-it-yourself systems. Can you help?

Arthur A. Gleckler
Baltimore, MD

It so happens that the first article I ever wrote for BYTE, way back in 1976, was on making a vector-graphics display. The title of the article was "Make Your Next Peripheral a Real Eye-Opener." (See the November 1976 BYTE, page 78. Reprints of BYTE articles are available from University Microfilm, 300 North Zeeb Rd., Ann Arbor, MI 48106.) It was reprinted in the Scelbi-BYTE primer edited by Nat Wadsworth and Carl Helmers (now out of print). The vector-graphics display used two 8-bit D/A (digital-to-analog) converters to create a 256 by 256 resolution display. I used a converted Sanders Associates 720 video terminal that operated on a vector (rather than raster-scan) principle. It was very easy to convert. If you do not have such a display available, a standard 5-inch oscilloscope will also work. The circuit is relatively simple and will probably cost you less than $30 in components.

Over the years, many experimenters have written to me about these articles. At this point, I no longer have any information on the Sanders unit, nor do I even have the prototype that I made. Both have been given away to people who have written to me.

After looking over the article again, the only item that I noticed missing in the reprint was the fact that the power-supply pins for the MC1408L8 D/A converter were not provided. Pin 13 should be connected to +5 V and pin 3 should be connected to −15 V.

Not too many people think about vector-graphics displays anymore because raster scan has become so inexpensive, but I found that I had a lot of fun using it and would still have it if I didn't have so much time tied up making other projects. . . . **Steve■**

In "Ask BYTE," Steve Ciarcia answers questions on any area of microcomputing. The most representative questions received each month will be answered and published. Do you have a nagging problem? Send your inquiry to:
Ask BYTE
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POB 582
Glastonbury CT 06033

If you are a subscriber to The Source, send your questions by electronic mail or chat with Steve (TCE317) directly. Due to the high volume of inquiries, personal replies cannot be given. Be sure to include "Ask BYTE" in the address.

Structured Programming in BASIC

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"Why study structured programming?" Structured programming pays off in increased software reliability, as well as greater ease in debugging and maintenance.

This article will introduce the basic concepts and techniques of structured programming. I'll concentrate on the implementation of modular programs through the use of procedures, as well as discuss control structures and their relationship to program flow. I've also included a Morse-code-generator program so that you can put the elements of this discussion to practical use.

Cromemco 32 K Structured BASIC is the language I have chosen for this discussion. Its interactive nature is well suited to develop structured programming skills. Since BASIC is a "friendly," widely used language, it is possible to concentrate on the details of structured programming rather than the details of the language.

Modules and Procedures

The essence of structured programming is *simplicity*. Since a structured program is broken down into small logical modules, called *procedures*, each of the modules can be independently tested, and the program is easier to debug than the large, tangled mess of a conventional program. When the entire program is finally run, the only untested part is the interaction *between* the modules, and the program is much more likely to execute correctly than an equivalent program that is not built from modules.

Cromemco 32 K Structured BASIC gives you the option of dividing the user memory in the computer into as many as eight partitions. Each partition can contain either a single procedure or a group of related procedures and has its own set of variables, statement labels, and line numbers. When a procedure in a given partition is called from another partition, values and variables may be passed to it as calling parameters and returned as return parameters.

The example in listing 1 is the skeleton of a routine designed to read input from the console terminal. It illustrates the concept of simplifying a program through the use of procedures. In order to further simplify things, I've omitted some important details such as the statements within the procedures, error checking, and parameter passing.

Here we assume that each procedure has access to a common variable (called Buffer$) which acts as a storage buffer for the input string being read. When the topmost procedure (.Read'console'no'blanks'-no'null) is called, a sequence of calls to other procedures is executed, during which the variable Buffer$ is filled with a line of characters from the input terminal. As you can see from the name of this procedure, there will be no leading or trailing blanks placed in Buffer$, and a null string will be suppressed. (If the user types only a carriage return in response to an input prompt on the terminal, the input prompt will be repeated.)

When reducing any task to its smallest logical pieces, you should write the primitive procedures first. (Primitive procedures are those which do not call any other procedures.) These can then be tested and debugged independently of the other primitive procedures. In listing 1, the primitive procedures are:

- .Read'console
- .Strip'leading'blanks
- .Strip'trailing'blanks
- .No'null

After you have broken the task into its most basic pieces and have written primitive procedures to perform each, it's a relatively simple matter to write other, higher layers of procedures (which simply call the primitive procedures).

In the example, the next higher procedure is called .No'blanks, which calls .Strip'leading'blanks and .Strip'trailing'blanks. Higher than .No'blanks is the procedure .Read'console'no'blanks, which calls both .No'blanks and the primitive

Acknowledgments
The author wishes to thank Laura King, Roger Melen, and Roger Sippl for their contributions to this article.

Listing 1: *The skeleton of a structured BASIC routine that reads input from the console terminal. For simplicity, most details have been omitted.*

```
Procedure .Read'console'no'blanks'no'null
     Call .Read'console'no'blanks
     Call .No'null
     Endproc

          Procedure .Read'console'no'blanks
               Call .Read'console
               Call .No'blanks
               Endproc

                    Procedure .No'blanks
                         Call .Strip'leading'blanks
                         Call .Strip'trailing'blanks
                         Endproc

                              Procedure .Read'console
                                   Rem This procedure accepts a
                                   Rem string Buffer$ from the
                                   Rem console.
                                   Endproc

                              Procedure .Strip'leading'blanks
                                   Rem This procedure shifts the
                                   Rem characters in Buffer$ to
                                   Rem the left so that the first
                                   Rem non-blank character is in
                                   Rem the first position of the
                                   Rem string.
                                   Endproc

                              Procedure .Strip'trailing'blanks
                                   Rem This procedure changes
                                   Rem all trailing blanks in
                                   Rem Buffer$ to null characters.
                                   Endproc

                              Procedure .No'null
                                   Rem This procedure will reject
                                   Rem Buffer$ if it contains
                                   Rem nothing but null characters.
                                   Rem Note: the user will have to
                                   Rem be re-prompted.
                                   Endproc
```

procedure .Read'console. The topmost procedure in listing 1 is .Read'console'no'blanks'no'null, which we find appropriately placed at the top of the listing. (Writing the lowest-level procedures first and then proceeding upward is referred to as "bottom-up coding.")

Because this console-reading routine has been written in modular form, it can be entered at several points. For instance, if you want null input accepted from the user and returned in Buffer$, you can call the second procedure (.Read'console'no'blanks). In a similar manner, you can call the primitive procedure .Read'console if the program needs *all* the input from the console terminal.

By combining the four primitive procedures in various ways, you can create a series of more complex and useful routines. The list of primitive procedures can be expanded to include error checking and other operations. When all the necessary primitive procedures are completed, the skeleton routine can be fleshed out into a working program.

Control Structures and Linear Flow

In structured programming, control should flow in a linear or sequential manner. A *control structure* is a means by which the order of execution is changed from the sequential line-number order. In BASIC, the simplest control structure is the GOTO statement. (In nonstructured programming, the flow tends to jump around through the use of multiple GOTO statements.)

Although the GOTO statement is available in Cromemco 32 K Structured BASIC, its use in structured programming is strongly discouraged. Overuse of GOTO statements tends to make programs more difficult to debug and maintain. Structured languages use conditional loops and branches that allow the program to flow in as linear a fashion as possible.

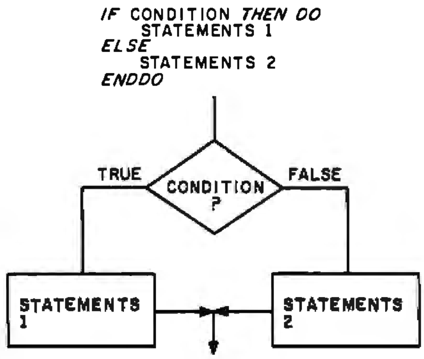

Figure 1: *Flowchart symbols used to represent the IF...THEN...ELSE...ENDDO programming construct that is important to structured programming.*

Cromemco 32 K Structured BASIC provides a number of control structures, including conditional loops and branches, which allow you to write clear, concise, and readable programs that flow in a linear fashion.

The IF...THEN...ELSE...ENDDO structure, shown in flowchart form in figure 1, provides a conditional branch followed by two independent sections of code. Execution of the program can follow either (but not both) of the paths. IF a condition is true (such as a variable having a certain value), THEN certain statements are executed. If the condition is not true, the statements after the ELSE are performed. Each path can contain as many BASIC statements as needed.

The WHILE...ENDWHILE and REPEAT...UNTIL structures (shown in figure 2) are conditional loops. UNTIL or WHILE a condition is true, they cause a set of BASIC instructions to be executed over and over again. But there is one important difference between the two: WHILE tests the condition *before* executing the instructions; REPEAT tests the condition *after* executing the instructions. The REPEAT structure will always execute at least once. The WHILE structure, depending upon the tested condition, may not execute at all.

An Example

The Morse-code generator (shown in listing 2) demonstrates some of the structured-programming concepts I've been discussing. While the program doesn't incorporate some Structured BASIC features, such as the procedure library, memory partitions, common storage area, and parameter passing, it is designed to show a linear and well-documented structured program. (Note that when you call a procedure, use of the keyword CALL is optional. You can call a procedure simply by referencing its name, which always begins with a period in Structured BASIC.)

The procedure that generates the actual Morse-code dits and dahs is called .Tone (see listing 2). To produce audible tones you'll need the Cromemco D+7A I/O (input/output) interface board as well as a pair of Cromemco joystick consoles, which produce the audio output. If you don't have the consoles, the Morse code will be displayed as a

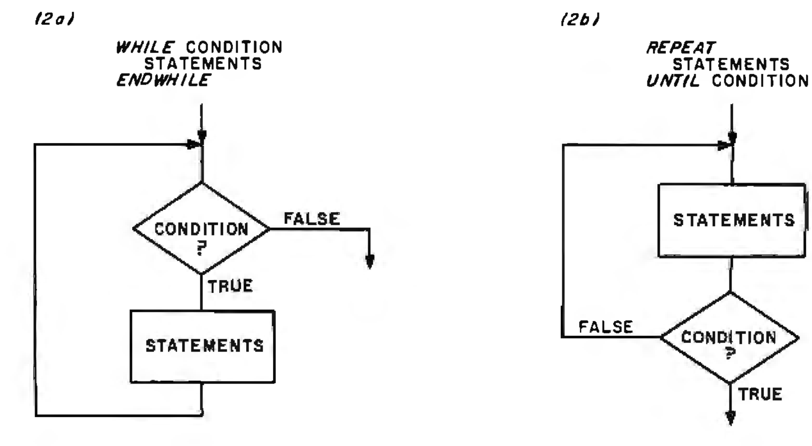

Figure 2: *Flowchart symbols used to represent the WHILE...ENDWHILE (figure 2a) and REPEAT...UNTIL (figure 2b) programming constructs.*

Listing 2: *A Morse-code generator program written in Cromemco 32 K Structured BASIC that illustrates some of the concepts of structured programming. Text for translation to Morse code is read from a disk file. Here the BASIC keywords use only an initial capital letter, instead of the usual all-capital style. Long variable names are used, and names of procedures begin with periods. Arguments enclosed in backslashes refer to disk-file operations.*

```
1000     Rem PROGRAM MORSE
1010     Rem date 9.79
1020     Rem
1030     Rem Program to convert a text file
1040     Rem to its Morse code equivalent.
1050     Rem
1060     Call .Initialize
1070     Call .Set'up
1080     Call .Read'and'process
1090     Call .Finish
1100     Stop
1110     Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1120     Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1130 Procedure .Initialize
1140     Integer Dash'to'dot'ratio,Ies,Ils,Iws,Max'line'length
1150     Rem
1160     Rem The four following parameters control the characteristics
1170     Rem of the code generated and the console display.  They may
1180     Rem be changed by the user.
1190     Rem
1200     Max'line'length=75 :   Rem Maximum line length on console.
1210     Ies=1 :   Rem Inter-element spacing ratio.
1220     Ils=5 :   Rem Inter-letter spacing ratio.
1230     Iws=7 :   Rem Inter-word spacing ratio.
1240     Dash'to'dot'ratio=3 :   Rem This is the standard.
1250     Rem
1260     Rem
1270     Dim Filename$(13),Character$(0),Null$(0)
1280     Dim Valid'characters$(64)
1290     Integer True,False,Error'number,End'of'file'flag
1300     Integer Wpm,Delay,Index,End'of'file'error'number
1310     Integer Num,Low'case,Up'case,P'duration,T'duration
1320     Integer Line'length,Max'line'length
1330     Valid'characters$="aAbBcCdDeEfFgGhHiIjJkKlLmMnNoOpPqQrRsStTuUvV"
1340     Valid'characters$(44)="wWxXyYzZ0123456789 .?"
1350     True=1 : False=0
1360     End'of'file'error'number=138
1370     Null$=""
1380     Line'length=0
1390     Rem Correct inter-word spacing ratio to follow
1400     Rem inter-letter space.
1410     Iws=Iws-Ils
1420     Rem Correct inter-letter spacing ratio to follow
1430     Rem inter-element space.
1440     Ils=Ils-Ies
1450     Rem Correct maximum line length to allow another character
1460     Rem to be displayed.
1470     Max'line'length=Max'line'length-10
1480     Endproc
1490     Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1500     Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1510 Procedure .Set'up
1520     Print : Print
1530     Rem Prompt user for speed and file name.
1540     Input"Morse code speed (WPM)=",Wpm
1550     If Wpm<1 Then 1540
1560     If Wpm>100 Then @"Cannot be greater than 100" ; Goto 1540
1570     Delay=250/Wpm
1580     Input"Filename (XXXXX.XXX)=",Filename$
1590     Open\1\Filename$
1600     Endproc
1610     Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1620     Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1630 Procedure .Read'and'process
1640     On Error Gosub Error'trap
1650     On Esc Gosub Escape
1660     End'of'file'flag=False
1670     Get\1\Character$
1680          While End'of'file'flag=False
1690          .Filter
1700          .Decode'and'output
1720          Get\1\Character$
1730          Endwhile
1740     On Error Stop
1750     Endproc
1760 *Error'trap : Error'number=Sys(3)
1770     End'of'file'flag=True
```

Listing 2 continued on page 414

series of dots and dashes on the video screen.

The program is made up of four major procedures:

- .Initialize
- .Set'up
- .Read'and'process
- .Finish

By simply reading the series of CALL statements at the beginning of the program, you can easily discern the basic flow of control.

The first procedure (.Initialize) initializes the value, type, and dimension of all of the program variables. Note that even though the variable-type-declaration statements are not required, using them results in faster execution and more memory-efficient code.

Four parameters that you can change are identified at the beginning of the initialization procedure. Although the spacing ratios assume that the length of a dot is equal to one unit, the actual dot length generated is dependent on the speed in words per minute that you select when the program is run.

The default values I've selected are a silent pause equal to one dot after each element (dot or dash), a five-dot pause after each complete letter, and a seven-dot pause after each word.

After variable initialization, the procedure .Set'up sets the parameters for program execution by prompting you for the information and then setting up a data file on a peripheral device.

Next, the file must be read and the information processed, by using the procedure .Read'and'process. The first matters of business for .Read'and'process are the setting up of error and escape traps. As program execution comes to an end or is interrupted, the input data file must be closed before control is returned to the user. If it isn't, a file might be left open after an aborted run, resulting in incorrect execution the next time the program is used. The error trap is also used to set the logical value of the end-of-file flag to true when the end of the file is reached.

Listing 2 continued:

```
1780         If Error'number#End'of'file'error'number Then  Do
1790         Rem Print error message, reset error trap,
1800         Rem and abort program execution.
1810         Print
1820         Print"System Error ";Error'number
1830         On Error Stop
1840         .Finish
1850         Stop
1860         Enddo
1870    Return
1880 *Escape
1890    On Error Stop
1900    .Finish
1910    Stop
1920    Return
1930    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1940    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
1950 Procedure .Finish
1960    .Break
1970    Close\1\
1980    Print : Print
1990    Endproc
2000    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2010    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2020 Procedure .Filter
2030    Rem
2040    Rem The following instructions locate the character
2050    Rem in a string of valid characters.  If it is not
2060    Rem found a -1 is returned indicating that it is an
2070    Rem invalid character.  If the character is valid
2080    Rem it is displayed else the character buffer is set
2090    Rem equal to the value of a null character.
2100    Rem
2110         If Pos(Valid'characters$,Character$,0)=-1 Then  Do
2120         Rem If it is a carriage return, display a space.
2130         If Character$=Chr$(13) Then Call .Space
2140         Character$=Null$
2150         Else
2160         Print Character$;
2170         Line'length=Line'length+1
2180         Enddo
2190    Endproc
2200    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2210    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2220 Procedure .Dot
2230    .Tone (1)
2240    Print".";
2250    Line'length=Line'length+1
2260    .Pause (Ies)
2270    Endproc
2280    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2290    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2300 Procedure .Dash
2310    .Tone (Dash'to'dot'ratio)
2320    Print"-";
2330    Line'length=Line'length+1
2340    .Pause (Ies)
2350    Endproc
2360    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2370    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2380 Procedure .Space
2390    Rem Call Pause with inter-word pause value (Iws).
2400    Rem Display a space on the console.
2410    .Pause (Iws)
2420    Print" ";
2430    Line'length=Line'length+1
2440    Endproc
2450    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2460    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2470 Procedure .Pause (P'duration)
2480    Rem Pause for P'duration times dot value.
2490         For Index=1 To Delay*P'duration
2500         Next Index
2510    Endproc
2520    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2530    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2540 Procedure .Tone (T'duration)
2550    Rem Generate tone for T'duration times dot value.
2560    Rem Joystick speakers must be connected to output ports 25 and 27.
2570    Rem Noesc, Esc sequence allows for faster execution so that
2580    Rem a higher frequency tone is generated.
2590    Noesc
2600         For Index=1 To Delay*T'duration
2610         Out 27,0 : Out 27,128
2620         Out 25,0 : Out 25,128
2630         Next Index
2640    Esc
2650    Endproc
2660    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2670    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
```

Listing 2 continued on page 415

The WHILE loop is the heart of the program. It is preceded by a file access to determine whether or not the file is empty. If the file is not empty, the character buffer (Character$) is initialized.

If the end-of-file flag is true, the WHILE loop will not execute and the procedure terminates. If the end-of-file flag is false, the characters continue to be processed. When the end of the file is encountered during a file access, the run-time error is trapped by the ON ERROR instruction and control is transferred to the subroutine at the location denoted by the logical identifier Error'trap.

If the Error'trap subroutine is called and the error number and end-of-file error number are found equal, the end-of-file flag is set to true and the RETURN instruction causes program control to be passed to the instruction following the one that generated the error. In this case, the GET instruction would generate the error, and control would return to the ENDWHILE instruction. ENDWHILE causes control to be returned to the WHILE statement. Because the end-of-file flag has been set to true, the condition for the execution of the WHILE loop is not satisfied and control is passed to the instruction following the ENDWHILE instruction.

If the error number is not equal to the end-of-file error number, execution of the program is aborted. The procedure .Read'and'process calls two other procedures, .Filter and **.Decode'and'output.** Invalid characters are eliminated by .Filter. The string function POS is used to determine whether or not the character in the character buffer, Character$, is valid. This is done by finding the position of the character within the string Valid'characters$, which contains all of the valid characters. If the character cannot be found in the string, the POS function returns a −1. This occurs if Character$ contains an invalid character.

Although the carriage return is an invalid character, it is trapped in this routine and causes a pause to be output. This is done because it is common to terminate words in a file of ASCII (American Standard Code for Information Interchange) characters with a carriage return (new line) and no space.

Valid characters are displayed on the console terminal. If an invalid character is detected in the file, Character$ is assigned a null value. Valid characters are decoded and output by the procedure .Decode'and' output, which contains thirty-eight subroutines, each named for the character it generates. For example, consider the letter "d." Its value is not within the range of the numeric characters. Therefore, no numeric-character subroutine is called. During the check for a lowercase letter, the variable Low'case is assigned a value of 4. The ON...GOSUB instruction transfers control to the fourth subroutine in the list, D.

Subroutine D calls the procedures .Dash, .Dot, .Dot, and .Pause, and then control is returned to the calling routine. Both .Dot and .Dash display characters on the console terminal and call the procedure .Tone to generate the appropriate Morse-code sequence. The duration of the pause generated by .Pause is specified by its argument. In this case, the length of the pause is determined by the value of the variable Ils (inter-letter spacing) multiplied by the length of a dot.

If the displayed output line becomes too long, the .Output-'and'decode procedure generates a new line on the console. If the program reaches a normal or abnormal termination, the statement ON ERROR STOP restores the standard system error-handling routines. Then, the next procedure (.Finish) sends a Morse-code "break" character (S and K sent as one character), which indicates the end of the transmission. At the same time, the input file is closed.

Listing 2 continued:

```
2680 Procedure .Break
2690    Print : Print"Break";
2700    .Pause (Ies+Ils+Iws)
2710    .Dash  : .Dot  : .Dot  : .Dot  : .Dash  : .Dot  : .Dash
2720    Endproc
2730    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2740    Rem- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - *
2750 Procedure .Decode'and'output
2760    Rem
2770    Rem Check for number.
2780    Num=Asc(Character$)-Asc("0")+1
2790    On Num Gosub Zero,One,Two,Three,Four,Five,Six,Seven,Eight,Nine
2800    Rem
2810    Rem Check for lower case letter.
2820    Low'case=Asc(Character$)-Asc("a")+1
2830    On Low'case Gosub A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P,Q,R,S,T,U,V,W,X,Y,Z
2840    Rem
2850    Rem Check for upper case letter.
2860    Up'case=Asc(Character$)-Asc("A")+1
2870    On Up'case  Gosub A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P,Q,R,S,T,U,V,W,X,Y,Z
2880    Rem
2890    Rem Check for punctuation.
2900    If Character$=" " Then .Space
2910    If Character$="?" Then Gosub Questionmark
2920    If Character$="." Then Gosub Period
2930    Rem
2940    Rem Check line length and issue a new line if required.
2950          If Line'length>=Max'line'length Then  Do
2960          Print
2970          Line'length=0
2980          Enddo
2990    Endproc
10000 *Zero  : .Dash : .Dash : .Dash : .Dash : .Dash : .Pause (Ils)  : Return
10001 *One   : .Dot  : .Dash : .Dash : .Dash : .Dash : .Pause (Ils)  : Return
10002 *Two   : .Dot  : .Dot  : .Dash : .Dash : .Dash : .Pause (Ils)  : Return
10003 *Three : .Dot  : .Dot  : .Dot  : .Dash : .Dash : .Pause (Ils)  : Return
10004 *Four  : .Dot  : .Dot  : .Dot  : .Dot  : .Dash : .Pause (Ils)  : Return
10005 *Five  : .Dot  : .Dot  : .Dot  : .Dot  : .Dot  : .Pause (Ils)  : Return
10006 *Six   : .Dash : .Dot  : .Dot  : .Dot  : .Dot  : .Pause (Ils)  : Return
10007 *Seven : .Dash : .Dash : .Dot  : .Dot  : .Dot  : .Pause (Ils)  : Return
10008 *Eight : .Dash : .Dash : .Dash : .Dot  : .Dot  : .Pause (Ils)  : Return
10009 *Nine  : .Dash : .Dash : .Dash : .Dash : .Dot  : .Pause (Ils)  : Return
10010 *A     : .Dot  : .Dash : .Pause (Ils)  : Return
10011 *B     : .Dash : .Dot  : .Dot  : .Dot  : .Pause (Ils)  : Return
10012 *C     : .Dash : .Dot  : .Dash : .Dot  : .Pause (Ils)  : Return
10013 *D     : .Dash : .Dot  : .Dot  : .Pause (Ils)  : Return
10014 *E     : .Dot  : .Pause (Ils)  : Return
10015 *F     : .Dot  : .Dot  : .Dash : .Dot  : .Pause (Ils)  : Return
10016 *G     : .Dash : .Dash : .Dot  : .Pause (Ils)  : Return
10017 *H     : .Dot  : .Dot  : .Dot  : .Dot  : .Pause (Ils)  : Return
10018 *I     : .Dot  : .Dot  : .Pause (Ils)  : Return
10019 *J     : .Dot  : .Dash : .Dash : .Dash : .Pause (Ils)  : Return
10020 *K     : .Dash : .Dot  : .Dash : .Pause (Ils)  : Return
10021 *L     : .Dot  : .Dash : .Dot  : .Dot  : .Pause (Ils)  : Return
10022 *M     : .Dash : .Dash : .Pause (Ils)  : Return
10023 *N     : .Dash : .Dot  : .Pause (Ils)  : Return
10024 *O     : .Dash : .Dash : .Dash : .Pause (Ils)  : Return
10025 *P     : .Dot  : .Dash : .Dash : .Dot  : .Pause (Ils)  : Return
10026 *Q     : .Dash : .Dash : .Dot  : .Dash : .Pause (Ils)  : Return
10027 *R     : .Dot  : .Dash : .Dot  : .Pause (Ils)  : Return
10028 *S     : .Dot  : .Dot  : .Dot  : .Pause (Ils)  : Return
10029 *T     : .Dash : .Pause (Ils)  : Return
10030 *U     : .Dot  : .Dot  : .Dash : .Pause (Ils)  : Return
10031 *V     : .Dot  : .Dot  : .Dot  : .Dash : .Pause (Ils)  : Return
10032 *W     : .Dot  : .Dash : .Dash : .Pause (Ils)  : Return
10033 *X     : .Dash : .Dot  : .Dot  : .Dash : .Pause (Ils)  : Return
10034 *Y     : .Dash : .Dot  : .Dash : .Dash : .Pause (Ils)  : Return
10035 *Z     : .Dash : .Dash : .Dot  : .Dot  : .Pause (Ils)  : Return
10036 *Period: .Dash : .Dot  : .Dot  : .Dot  : .Dash : .Pause (Ils)  : Return
10037 *Questionmark  : .Dot  : .Dot  : .Dash : .Dash : .Dot  : .Dot
10038          .Pause (Ils)  : Return
10039   End
```

A Few Final Thoughts

The following are important points to remember when writing structured programs:

1. Break the program up into logical tasks. Break each task into subtasks. Continue to simplify until each primitive procedure performs a single clear and simple task.
2. Use meaningful names for procedures, variables, and line labels, when possible.
3. Use the preferred control structures, i.e., IF...THEN...ELSE, WHILE...ENDWHILE, and REPEAT ...UNTIL. Avoid using the GOTO instruction.
4. Use remarks in the source code. They will help clarify the purpose of a program section.

Try to keep these suggestions in mind when you design and code programs. They are not hard-and-fast rules, but they will allow you to create programs that are more efficient and easier to maintain.■

CMOS: Memory with a Future

Ideas Behind CompuPro's RAM 17

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The world of personal computers has evolved into two major categories. The all-in-one computer has most of the machine's intelligence residing in one major module produced by a single manufacturer. On the other hand, the bus-oriented computer can accept boards from numerous manufacturers. The major advantage of the bus-oriented computer is flexibility—modules performing distinct functions are available from a variety of vendors operating in a competitive marketplace. Therefore, systems integrators (people who put systems together by selecting boards from a variety of sources) can choose modules best-suited to perform a specific function (i.e., data acquisition, software development, word processing, etc.) from a wide variety of available boards. Furthermore, a bus-oriented computer allows relatively inexpensive upgrading when the requirements of the user either expand or change altogether.

The most popular bus-oriented small computers are based on the S-100 bus, developed by MITS for its Altair computer in the mid-1970s and proposed in 1979 as a standard by the Institute of Electrical and Electronics Engineers (IEEE specification 696). Unfortunately, the publication of specification 696 has not made integrating S-100 systems as simple as one might like. In fact, integrating boards from a variety of manufacturers, while resulting in a more flexible system, can also cause headaches for the integrator—particularly when choosing memory.

First, the strengths and limitations of currently available memory boards must be thoroughly understood in order to predict their effect on system performance. It is by no means certain that a given S-100 memory board—even one designed to meet the IEEE-696 specifications for S-100 bus performance—will function reliably in a given system simply because that system contains only boards that claim to meet these specifications. Claiming to meet specifications is easy; actually meeting those specifications is somewhat more difficult.

Second, since a major attraction of the S-100 bus to the end user is the ease with which these systems can be upgraded, future hardware and software developments must be anticipated so that upgrading the system will be as inexpensive as possible. Unlike an automobile or stereo, an S-100 machine does not have to be replaced in order to make room for next year's higher-performance model; instead, older boards may be replaced and newer boards added in order to achieve the current state of the art.

For example, when a system is upgraded from single-user to multi-user, or is modified for DMA (direct memory access) disk operation, all other aspects of the computer—memory, power supply, motherboard, etc.—may be preserved as is (protecting the initial investment) if the systems integrator had the foresight to choose the modules with future compatibility in mind. Since programmable memory is a high-cost item, it is especially important at the outset to choose a memory board with a future. The advantage of easy upgrading disappears if the system boards lack compatibility or if they are not designed to accommodate future improvements in technology.

Dynamic Versus Static Memory

The controversy over the respective merits of dynamic and static memory in S-100 computers goes back almost as far as the S-100 bus itself, and much ink has been spilled praising one and condemning the other. Many early dynamic-memory boards simply did not work, mostly due to poor design and inadequate (or sometimes nonexistent) quality control. This situation produced an unfair prejudice against the very principle of dynamic memory. Nevertheless, dynamic memory's high density, low power, and low cost, combined with improved design and manufacturing techniques, gradually restored

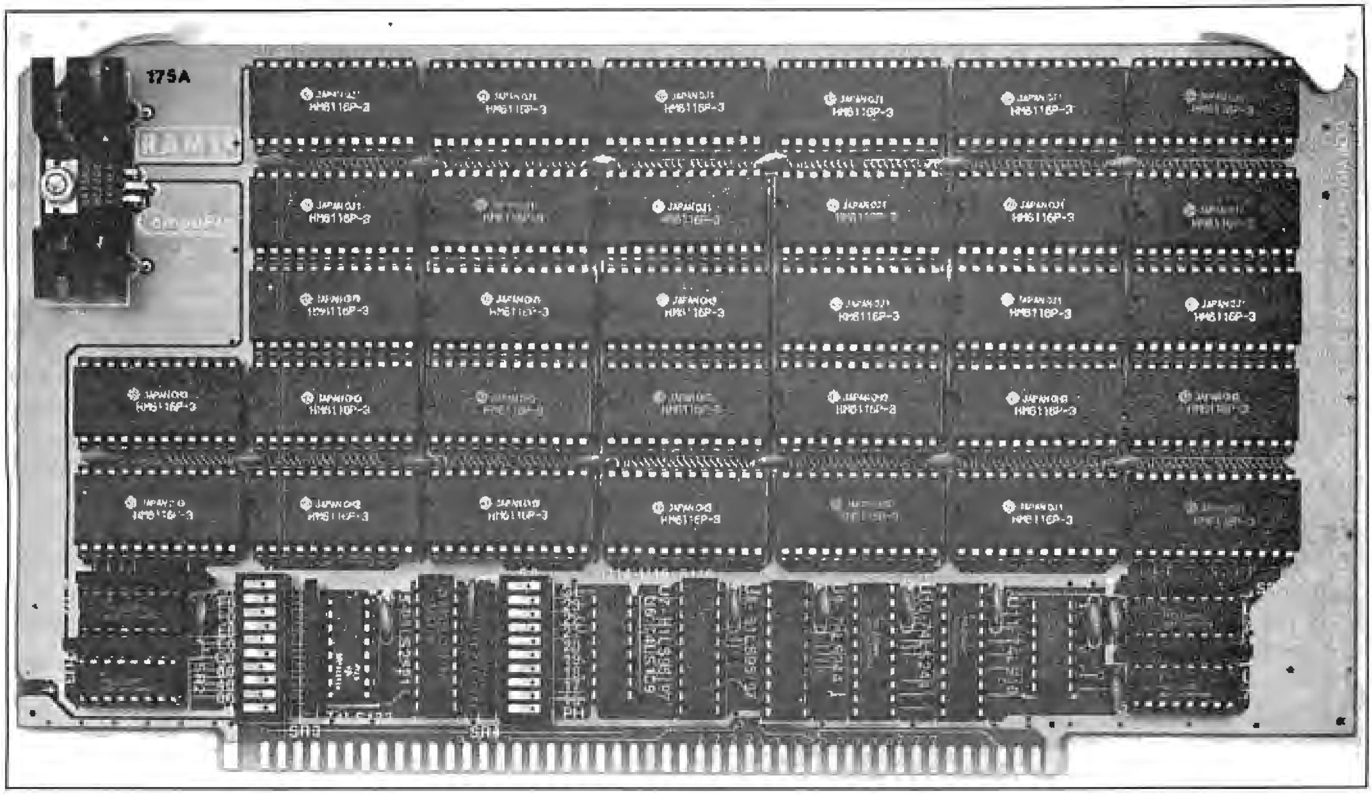

Photo 1: *CompuPro's RAM 17, the first commercially available 64 K-byte static-memory board for the S-100 bus.*

it to respectability and established it as the prime choice in many applications.

Static memory, while consuming more power and costing more than dynamic, offers the advantage of requiring no refresh signals. It is therefore the choice in systems using DMA devices. Until recently, putting a system together involved a necessary compromise; neither form of memory offered the ideal combination of low cost, high density, low power consumption, and the ability to execute DMA flawlessly.

Enter CMOS Memory

CMOS (complementary metal-oxide semiconductor) memory seemed to hold the best hope for being the ideal memory except for one major problem: cost. Until recently, CMOS memory was prohibitively expensive, restricting its use to all but the most expensive computing systems. However, a new generation of CMOS random-access memory has evolved that delivers all the qualities associated with an "ideal" memory at a reasonable price. The first commercially available 64 K-byte static-memory board for the S-100 bus, CompuPro's RAM 17, could not have existed without CMOS memory.

The introduction of low-cost CMOS memory has obsoleted some of the most forceful arguments formerly made in favor of dynamic memory. Five categories of performance have been greatly affected: density, power, speed, compatibility, and reliability/ease of maintenance.

CMOS memory is still more expensive than dynamic memory, although future price decreases are expected to lessen this cost difference. Nonetheless, the true cost of a memory board goes beyond the list price. If a board causes problems due to erratic or unpredictable operation, or needs to be replaced when a system is upgraded, an attractive initial savings may turn into an ugly added expense.

Before comparing the performance of dynamic versus CMOS memory, a brief functional description of CompuPro's RAM 17 is in order. RAM 17 is a 64 K-byte static-memory board using Hitachi's 6116 CMOS "byte-wide" memory integrated circuits (2 K by 8 bits) and is designed to meet all IEEE-696 specifications. The board can be used as *global* or *extended address* memory (global memory decodes only address lines A0-A15 and ignores address lines A16-A23; extended address memory decodes all 24 available address lines). The maximum amount of global memory possible in a system is 64 K bytes; the maximum extended address memory is 16 megabytes.

CompuPro's RAM 17 can be addressed to occupy any 64 K-byte page of memory. Four 16 K-byte "windows" can be switch disabled, and the upper 8 K bytes of the board can be disabled in four individual 2 K-byte increments (this makes room for popular memory-mapped devices such as disk controllers or video interfaces). When used with a CompuPro Memory Manager (available as a separate board or as part of CompuPro's Z80 or

8085/88 processor boards), RAM 17 can be placed in extended address mode and used as a bank-selected board.

Performance Comparison

As mentioned earlier, many of the arguments in favor of dynamic memory are no longer relevant since the development of CMOS memory. The most important differences are summarized below.

Density: Since 32 of Hitachi's 6116 memory devices (64 K bytes) fit on a standard-size S-100 board, it is no longer true that dynamic memory is denser than static memory at the board level. (In fact, CompuPro recently introduced RAM 21, a 128 K-byte static memory that also fits on a standard-size S-100 board, and RAM 16, a 64 K-byte board designed for either 8- or 16-bit systems.) At the systems level, an additional bonus of CMOS operation is the ability of systems with small power supplies to support more static-memory boards than dynamic-memory boards.

Power: CompuPro's RAM 17 typically draws 150 milliamperes (mA) from the +8-volt (V) line, or about 1.2 watts (W). At the sixth West Coast Computer Faire in San Francisco, a 1-megabyte system comprised of RAM 17 boards (16 of them) was run in a standard S-100 enclosure. After 12 hours of work, the system remained cool—the entire megabyte drew only about 3 amperes (A)!

Speed: The Hitachi 6116 has a worst-case access time of 150 nanoseconds (ns), compared with about 250 ns for conventional dynamic-memory devices. This means that a static-memory board can run without wait states with a 6-megahertz (MHz) Z80 microprocessor, while no currently available dynamic-memory board is fast enough to do this. Because there is no need for refresh on a static-memory board, the possibility for real-time applications is limited only by access time.

While dynamic-memory boards may *seem* to have a respectable access time, they cannot be run at their fastest access time because dynamic memory must be refreshed every few milliseconds. This can introduce sporadic delays in system operation in the form of refresh wait states, thereby slowing down the entire system and degrading real-time operation.

Compatibility: Current dynamic-memory-board designs all have serious weaknesses when used in DMA environments, particularly in environments supporting multiple DMA devices. For a fine description of the problems encountered when interfacing dynamic memories with DMA devices, refer to Larry Malakoff's excellent article "Dynamic Memory: Making an Intelligent Decision" (February 1981 BYTE, page 142).

The subject of reliability/ease of maintenance will be covered later in this article.

Static Memory and DMA

Probably the most important aspect of static memory in general, and CMOS memory in particular, is the ability to perform DMA. Therefore, we'll take the time to explain this concept in greater detail.

Direct memory access is a technique whereby a device other than the processor can read into, or write from, the system's memory directly, without the intervention of the processor. One of the most important results of the IEEE's publication of the 696 specifications for the S-100 bus is the definition of a standard protocol for DMA data transfer, including a rigorous arbitration scheme that allows multiple (up to 16) DMA devices to operate in the same system. Prior to the IEEE-696 specifications, DMA on the S-100 bus had a reputation so bad that it made the early reputation of dynamic memory look good. No two implementations of DMA were alike, and, in any event, no implementation seemed to work reliably. This was a terribly serious shortcoming of the S-100 bus that limited its use in truly professional applications.

The biggest advantage of DMA is that it allows extremely fast data transfer, thereby increasing throughput. This is due to the fact that within the S-100 standard the minimum amount of time needed to transfer data from a bus master to a bus slave is three clock cycles. Thus, a system running at 10 MHz, where each clock cycle takes 100 ns, would require a minimum of 300 ns to perform one data transfer. A system using processor-directed transfer would require from 30 to 40 clock cycles (3000 to 4000 ns) to make the same transfer.

A Static CMOS Memory Application

The versatility of the CMOS memory/DMA marriage allows for some novel applications. G & G Engineering markets a system, based on CompuPro hardware, that will run Digital Research's CP/M 2.2 or CP/M-86 on the same system (CompuPro has a dual processor board with an 8085 microprocessor and an 8088 microprocessor that makes this possible). When running CP/M-86, as much as 1 megabyte can be directly addressed by the 8088 (which is simply an 8086 that fetches data one byte at a time). When running CP/M 2.2, the 8085 has control, which means that only 64 K bytes can be directly addressed; but rather than wasting the remaining amount of memory, it is treated as if it were a disk drive. Thus, this vast storage area becomes a pseudo disk drive (which G & G calls Warp Drive), but one that operates at extremely high speed because there are none of the mechanical restraints associated with a traditional disk drive. This configuration allows users to run standard, unmodified CP/M 2.2 programs on the Warp Drive and achieve speed increases of up to 20 times over a standard floppy-disk system. Add to this the advantage of running all CP/M 2.2 programs on a 6-MHz 8085 without wait states, and the increase in performance over conventional 8-bit systems is enormous.

G & G Engineering's technique for implementing its Warp Drive is entirely dependent upon a DMA controller capable of transferring data to *any* location within the entire 16 megabytes of S-100 address space. While this technique could theoretically work with conventional static memory, the excessive power dissipation, power supply requirements, and the shortage of card slots would make the concept of Warp Drive highly impractical. Also, dynamic memory could not handle this type of application at all. As a result, this concept of a "solid-state disk drive" had to wait until the advent of a relatively inexpensive CMOS memory board such as RAM 17.

A future application of high-density, low-power CMOS memory combined with DMA devices involves multi-user systems. Before too long, it will be possible to upgrade single-user systems to powerful 16-bit multi-user systems, such as Digital Research's MP/M-86, Phase One's Oasis 86, and Microsoft's Xenix.

Thanks to the present availability of high-density, low-power CMOS memory, these future upgrades hold the promise of developing super systems without the loss of a single piece of existing computer hardware, except perhaps a processor board. What's more, the new operating systems will be greatly enhanced thanks to the addition of extra DMA devices (e.g., hard-disk controllers, direct I/O channel controllers, etc.). These hardware and software enhancements will produce faster and more efficient systems, making it more and more difficult for dynamic memory to find a niche in tomorrow's high-performance computers.

Reliability and Maintainability

It is important to address the question of reliability when dealing with high-density memories. The all-CMOS memory board has four distinct advantages over dynamic memory:

1. It consumes less power and, therefore, produces less heat and stresses the system power supply less than dynamic memory. (RAM 17 typically draws 150 mA from the +8-V power supply, which is the *only* power source required by this board. This represents a total power dissipation of about 1.2 W per board, compared with about 8 W total power dissipation for the better 64 K-byte dynamic-memory boards.) As Larry Malakoff points out in the article cited earlier, "(a) decrease in power dissipation of more than sixfold can make a big difference in the reliability of the entire system. This is especially true when the system contains more than 64 K bytes of memory, as in a multi-user application. Since the reliability factor for electronic equipment decreases exponentially as the operating temperature increases, the mean time between failures can be drastically improved by using dynamic memories in the larger memory-intensive systems." If, in the last sentence of this excerpt, the word "dynamic" is replaced by "static CMOS," the quotation may be upgraded to remain true in light of today's technology.
2. Static-memory boards have a dramatically lower parts count than equivalent dynamic-memory boards since there is no need for complicated refresh circuitry. Dynamic memories also require about three times more support ICs (about 30 versus 10); the more parts, the more chances for failure.
3. The Hitachi 6116 CMOS memory device used in the RAM 17, in addition to having more power-line noise immunity than a 4116-type dynamic memory, is also less sensitive to so-called soft-errors caused by alpha particle radiation. This means that even without parity checking RAM 17 is still more reliable than a 64 K-byte dynamic-memory board that does include parity checking.
4. The extremely fast, high-current switching occurring in dynamic-memory devices places a stress on these chips that is more severe than any stresses placed on CMOS memories. These stresses can cause dynamic memories to simply "wear out" after long-term operation. Though this wearing-out process may take several years on the average, the more dynamic memory there is in a system, the higher the probability that some devices will fail after only a few months or years.

Serviceability

Basically, any static-memory board is easier to repair than a dynamic-memory board. The near total absence of complex analog circuitry is mostly responsible for this. However, a special feature of CompuPro's RAM 17 makes maintenance even simpler. Though most S-100 memory devices using a bidirectional internal data bus (which includes conventional dynamic-memory boards, as well as RAM 17) may not be read or written from an IMSAI-type (switches and indicators for address and data lines) front panel, a special switch on the RAM 17 board allows these two operations. Therefore, 90 percent of the problems that may develop with the board can be quickly isolated by a technician using only a front panel and a logic probe.

Summing Up

Thanks to their low cost, dynamic memories may still find a home in dedicated, single-board small business/personal computers or even in some S-100 machines whose application is "frozen solid" (i.e., not subject to future upgrades). But the handwriting is on the wall; as CMOS technology becomes more refined and more publicized, the price advantage of dynamic memory will dissipate. In fact, for larger, high-performance systems, any potential economic advantages of dynamic memory are already outweighed by the lower power dissipation, higher speed, and greater reliability of the new generation of CMOS static memories. Of course, incremental improvements in dynamic memory are bound to occur—but it would take quite a breakthrough for dynamic memory to maintain its current share of the S-100 market, especially when you consider the many advantages offered by its CMOS competition. ■

The GEOSAT Program

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Herndon, VA 22071

Scan the night sky on a clear evening and you might see some "stars" ancient astronomers never saw. These new heavenly bodies are communications satellites that relay voice, data, and television signals around the world.

"Parked" at various positions around the equator, these satellites appear to remain stationary above certain points on the earth's surface. Actually, they're orbiting the earth once every 24 hours. Because they maintain their positions relative to a point on earth, they are called *geostationary* or *geosynchronous* satellites.

The idea of geosynchronous communications satellites was first brought to public attention by a young British mathematician in a paper entitled "Extra-Terrestrial Relays." It was initially published in the October 1945 issue of *Wireless World*. In later years, Arthur C. Clarke has speculated on how wealthy he might've become if he'd had the foresight to patent the idea.

Commercial possibilities of these satellites were tapped by Western Union when it launched the first commercial geosynchronous communications satellite in 1974. Since then, nations have joined private corporations in the ever-increasing launching of geosynchronous satellites.

While the legality of transmission reception by nonsubscribing individuals is still being argued, financial and technical problems associated with signal reception are diminishing. If you had a satellite-receiving station (a television-receive-only or TVRO terminal), you could watch news events from around the world, first-run movies, unique sports events, and superstations like Ted Turner's WTBS—all free of charge.

The price for a TVRO terminal can range from $4000 to over $15,000.

Well, *almost* free of charge. The price for a TVRO terminal ranges from $4000 to more than $15,000 (see table 1 for a list of TVRO equipment suppliers).

All you need is a dish antenna, a low-noise amplifier, and a receiver/downconverter to change the satellite signal to a frequency usable by your home television. Before you purchase and install the receiving equipment, it's necessary to know the satellites' locations relative to your site. Frequencies used by the satellites to transmit the television signals (2-4 GHz) require an unobstructed path or *line of sight* (LOS) between the satellite and the receiving antenna. It would be extremely annoying to dish out money for the equipment and whatever zoning permits might be necessary only to learn that the LOS of interest is blocked by a highrise building or lies below the horizon!

The GEOSAT program presented here will calculate the azimuth and elevation angle on which a TVRO antenna must be placed to receive signals from a specified geosynchronous satellite. (Note: while this article discusses TVRO sites in the United States, the program will calculate the antenna look angle for any site in the world.)

For precise designation of any point on or above its surface, the earth is divided into an imaginary grid. Grid lines circling the earth parallel to the equator indicate *latitude*; those extending from pole to pole indicate *longitude* (see figure 1).

Latitude is measured from the equator, which equals 0 degrees latitude. North or south from the

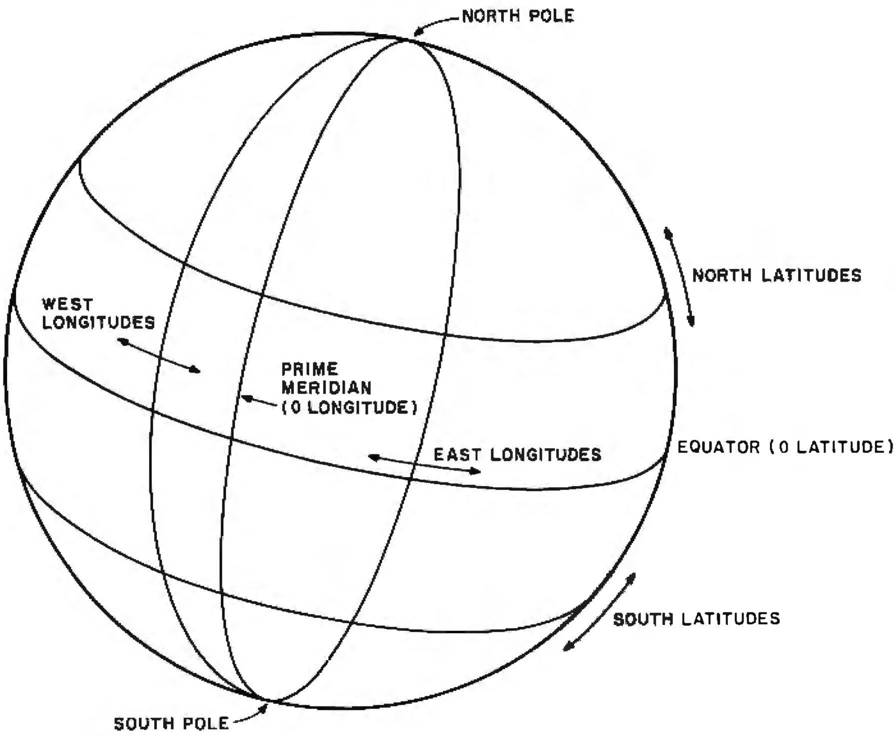

Figure 1: *Longitude is measured from the prime meridian (0 degrees), which passes through Greenwich, England. Latitude is measured from the equator (0 degrees) to the poles.*

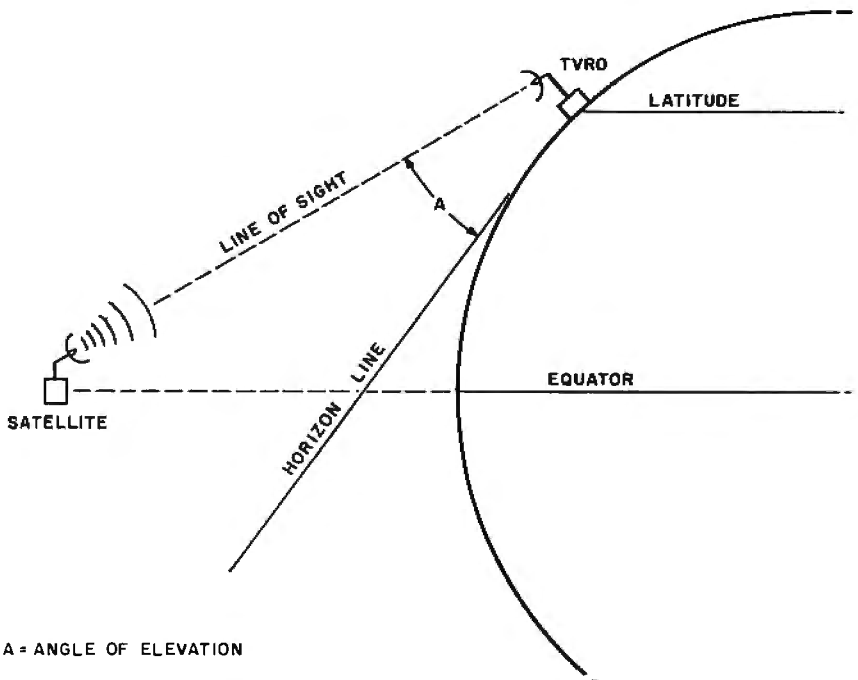

Figure 2: *Elevation angle for the antenna is measured from the horizon (0 degrees) to straight up (90 degrees).*

equator, latitude increases to 90 degrees at the poles. Lines going toward the north pole are called north latitudes; those going toward the south pole are called south latitudes. The United States lies between about 25 and 50 degrees north latitude.

The reference for 0 degrees longitude is a line that extends between the poles and passes through Greenwich, England. Moving away from Greenwich, longitude increases to 180 degrees at the International Date Line (IDL), which is halfway around the world from Greenwich. Imagine yourself standing on the 0-degree longitude line and facing west. Longitudinal lines going west toward the IDL are termed west longitudes, while those going east from 0 degrees are termed east longitudes. The United States lies between about 70 and 125 degrees west longitude.

Since geosynchronous satellites are in orbit around the earth's equator (with an orbital inclination of 0 degrees), the satellites' latitude equals that of the equator: 0 degrees. A satellite's longitude is the point on the equator directly beneath it (the satellite subvehicular or *nadir* point). For communication satellites of interest to continental United States TVRO sites, longitudes range from about 85 to 180 degrees west (see table 3).

The direction in which the TVRO antenna must point for signal reception is given in terms of *azimuth* and *elevation*. To determine the azimuth, draw a circle whose center is the proposed antenna site. Draw a line from the center of the circle toward the north pole; this line has an azimuth of 0 degrees. Now move this line clockwise around the circle. When the line is pointing east, it has an azimuth of 90 degrees. At the half-circle or 180-degree mark, the line is pointing south. Thus, when an azimuth from a TVRO location to a satellite is given as, say, 190 degrees, the antenna is facing a little west of due south.

The *elevation angle* (how high the antenna has to be pointed) is measured with an imaginary line that extends from the TVRO site toward the horizon and ranges from 0 to 90 degrees (see figure 2). An elevation angle of 0 degrees means the antenna is pointing directly at the horizon; at 90 degrees, the antenna is pointing straight up.

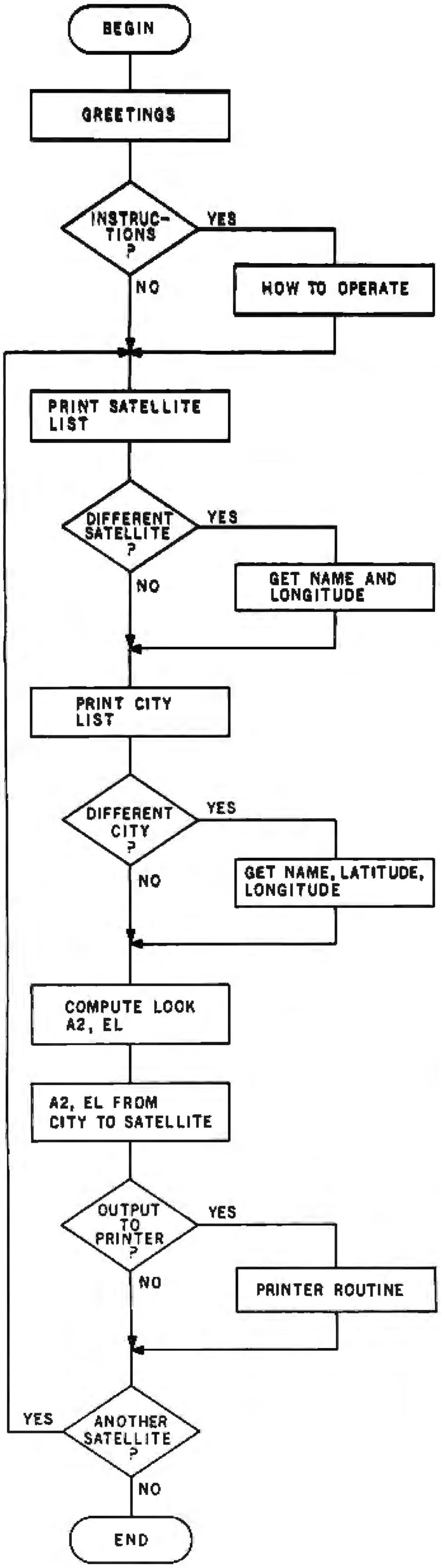

Figure 3: *A flowchart showing organization and operation of the GEOSAT program.*

Thus, given the satellite longitude and the receiving site latitude and longitude, it's possible to determine where the antenna must be pointed to receive signals. Since the satellite is geostationary, the antenna doesn't need to "track" the satellite. Only when reception from another satellite is desired is it necessary to move the antenna. (In the strictest sense, a geostationary satellite *does* move. But movement in latitude and longitude is small compared to the beam width of both the satellite transmitting antenna and the TVRO antenna. Consequently, it can be ignored).

The GEOSAT program (see listing 1, page 424) is written in Applesoft BASIC and composed of nine modules:

INITIAL (6000-6600) sets up data arrays containing satellite and city names and defines several constants.

HEADER (4000-5060) consists of the greeting message and provides operating instructions as needed.

LISTCITY (7000-7460) provides a list of cities whose latitude and longitude data are stored in the program. Option to use one of the cities already stored or to enter a new city is offered (see table 2).

CITYLATLONG (1000-2380) is entered from LISTCITY if a city not in LISTCITY is desired. This module prompts for the city name, latitude, and longitude; it also does some input error checking.

LISTSATELLITE (8000-8460) provides a list of satellites whose longitude data are stored in the program. The option to use one, all, or to enter a new satellite is offered (see table 3).

SATLONG (3000-3700) is entered from LISTSATELLITE if a satellite not in LISTSATELLITE is desired. This module prompts for the satellite name and longitude and does some input error checking.

CALLSETUP (9000-9400) is used to set up some temporary arrays and to initialize some temporary variables prior to performing the actual look-angle calculations.

COMPUTE.LOOK (100-590) performs the look-angle calculation from a given city to the satellite(s) of choice. This module is called once for each satellite of interest.

SCREEN.DISPLAY (10000-10520) displays azimuth and elevation from the chosen city to the satellite(s) of interest and permits printing of results if desired (see table 4).

The overall flow of the program, which is fairly straightforward, is shown in figure 3. Three of the modules, COMPUTE.LOOK, CITYLATLONG, SATLONG, are called as subroutines. Taking advantage of how Applesoft processes a subroutine call, the three subroutines are placed at the beginning of the program. This

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Manufacturing, Inc.
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Poplar Bluff, MO 63901
(314) 785-5988

Antenna Engineering, Inc.
POB 1676
El Cajon, CA 92022
(714) 280-3443

Heath Company
Benton Harbor, MI 49022
(800) 253-0570

Interstar Satellite Systems, Inc.
21708 Marilla St.
Chatsworth, CA 91311
(213) 882-6770

Microwave General
2680 Bayshore Frontage Rd.
Mountain View, CA 94043
(415) 969-3355

Mid-America Video Corporation
POB 511
North Little Rock, AR 72115
(501) 753-3555

NEC
Broadcast Equipment Division
130 Martin Lane
Elk Grove Village, IL 60007
(312) 640-3750

Satellite International
3107 Eagle Rock Rd.
Augusta, GA 30903
(404) 738-5101

Satellite Systems Science
POB 7213
Ocala, FL 32672
(904) 687-4633

Table 1: *Some distributors of TVRO terminal equipment.*

makes for poor program readability but does help increase its responsiveness.

To make the GEOSAT program as generally useful as possible, both satellite and city data are in the program (see tables 2 and 3). If the data do not suit a particular need, the option is given during program operation to enter other data. In addition, it's simple to change the data lists in the program to permanently reflect particular preferences. To accomplish this, just follow these steps:

1. List lines 20030 through 20270.
2. The first DATA statement (20030) contains the number of satellites presently stored in the program (maximum of 30).
3. The following DATA statements (20040-20150) contain the satellite names and their longitudes.
4. To add, delete, or change a satellite entry, simply enter the changes, following the format of the present entries and remembering to use a minus sign for west longitudes.
5. Be certain the number of satellites is correctly reflected in the DATA statement that precedes the list.
6. Immediately following the last satellite name is a DATA statement (20160) that contains the number of cities stored in the program (maximum of 30). Follow steps 4 and 5 to make any changes to the city list. South latitudes must be entered with a minus sign.
7. Save the revised version of the program.

Now whenever the program is run, the new data will be displayed (see table 4). After the azimuth and elevation calculations have been done, go to the potential TVRO site and look in the directions indicated by the program to see if there are any LOS obstructions.

A word of caution: if the elevation angle is low (0-10 degrees) or there's doubt about missing an obstruction, it's worthwhile to conduct a site survey. This survey would include taking into account the beam-width effects of the TVRO antenna and a precise determination of the angular separation of obstructions from the LOS. The larger the TVRO antenna, the narrower its beam width and the less effect obstructions and proximity to the horizon will have on its ability to receive signals from a particular satellite. When in doubt, do the survey. The amount you'll pay to determine whether or not the TVRO site is properly located is minuscule compared to the outlay for a system that can't be used! ■

Name	Latitude (N)	Longitude (W)
Washington, DC	39	77
Los Angeles	34	118
New York	40.5	74
Atlanta	33.5	84.5
Miami	25.75	80.25
Jacksonville	30.5	81.5
Tampa	28	82.75
Anchorage	60.8	147
Nome	65	165
Phoenix	33.5	112
Little Rock	34.75	92.25

Table 2: *Latitude and longitude for these cities have been entered as data statements in the GEOSAT program. Other city locations can be included.*

Name	Longitude (W)
COMSTAR 3	87
WESTAR 3	91
COMSTAR 2	95
WESTAR 1	99
ANIK 1	104
ANIK 2	109
ANIK 3	114
SATCOM 2	119
WESTAR 2	123.5
COMSTAR 1	128
SATCOM 3	132
SATCOM 1	135

Table 3: *These satellites can be "seen" from the United States and are included in the program.*

From: Washington, DC

To	Antenna Azimuth	Antenna Elevation
COMSTAR 3	195	49
WESTAR 3	201	48
COMSTAR 2	207	46
WESTAR 1	212	44
ANIK 1	219	41
ANIK 2	224	38
ANIK 3	230	35
SATCOM 2	235	31
WESTAR 2	239	27
COMSTAR 1	243	23
SATCOM 3	246	20
SATCOM 1	248	17

Table 4: *Sample output of the GEOSAT program for a TVRO terminal located in Washington, D.C. Azimuth and elevation angles for each of the satellites in the program are shown.*

Listing 1: *Using a modular approach, the GEOSAT program has nine major subroutines. DATA statements containing positions for satellites and cities, plus tab positioning and printer routines, are located at the end of the program.*

```
10 FG = 0
20  GOTO 4070
100  REM  ****
110  REM
120  REM   THIS MODULE COMPUTES T
     HE LOOK AZIMUTH AND ELEVATIO
     N FROM A SPECIFIED POSITION
     ON THE EARTH TO A SYNCHRONOU
     S SATELLITE
130  REM
140  REM  ****
150  REM
160  REM  AZIMUTH IS IN Y
170  REM  ELEVATION IS IN EL
180  REM
190  REM  FIRST COMPUTE THE PROPE
     R LONGITUDE DIFFERENCE
200  REM
210 T = M2 - M1
220 TA =  ABS (T)
230  IF TA <  = 180 THEN  GOTO 26
     0
240 TS =  SGN (T)
250 T =  - 1 * ((TS * 360) - T)
260 EP = T
270  REM
280  REM  NOW CONVERT ANGLES INTO
      RADIANS
290  REM
300 T = T / RD:L1 = L1 / RD:EP =
     EP / RD
310  REM
320  REM  NOW COMPUTE "MODIFIED"
     RECEIVER LATITUDE
330 X =  SQR (1 - .5 * ( COS (L1)
      +  COS (EP)))
340 ML = 2 *  FN ARCSYN(X)
350  REM
360  REM  NOW COMPUTE ELEVATION L
     OOK ANGLE
370  REM
380 EL = (PI / 2) - (ML +  ATN (R
      *  SIN (ML) / (R * (1 -  COS
     (ML) * H))))
390  REM
400  REM  NOW COMPUTE LOOK AZIMUT
     H
410  REM
420  IF EP = 0 THEN YA = PI: GOTO
     490
430 ZA = 1 /  TAN (EP / 2)
440 ZB =  TAN (L1 / 2)
450 YA =  ATN (ZA * ZB) +  ATN (Z
     A * (1 / ZB))
```

```
460  REM
470  REM  NOW CONVERT ANGLES BACK
      TO DEGREES
480  REM
490 YA = YA * RD:EL =  INT (EL *
     RD):L1 = L1 * RD
500  REM
510  REM  CORRECT LOOK AZIMUTH FO
     R NORTH/SOUTH HEMISPHERE
520  REM
530 ZF = 360
540  IF L1 < 0 THEN  GOTO 580
550 YA = 360 + YA
560 Y =  FN MOD(YA)
570  RETURN
580 Y =  INT (180 + YA)
590  RETURN
1000  REM  ****
1010  REM
1020  REM  MODULE TO GET CITY NAM
     E,LATITUDE AND LONGITUDE.
1030  REM
1040  REM  ****
1050  HOME
1060  PRINT "WHAT IS THE NAME OF
     THE CITY?  ": INPUT NC$
1070  PRINT : PRINT
1080  PRINT "ENTER THE CITY LATIT
     UDE USING SPACES TO SEPARATE
      DEGREES MINUTES AND N(ORTH)
      OR S(OUTH).  ": INPUT DL$
1090  REM
1100  REM   NOW DECOMPOSE DL$ INT
     O DEGREES,MINUTES AND N OR S

1110  REM  DO DEGREES FIRST
1120  REM
1130 LE =  LEN (DL$)
1140 I = 1
1150  IF  MID$ (DL$,I,1) =  CHR$
     (32) THEN  GOTO 1270
1160  IF (I = LE) THEN  GOTO 1220

1170 I = I + 1: GOTO 1150
1180  REM
1190  REM  DATA IS NOT IN PROPER
     FORMAT
1200  REM  GIVE ERROR MESSAGE AND
      DO AGAIN
1210  REM
1220  VTAB 20: HTAB 1: PRINT "WHE
     N YOU ENTER THE LATITUDE, BE
      SURE TO USE SPACES TO SEPAR
     ATE THE ENTRIES. ": PRINT "A
     NY KEY TO CONTINUE ";: GET K
     $: PRINT K$
1230  VTAB 5: HTAB 1: CALL  - 958
     : GOTO 1080
```

Listing 1 continued:

```
1240  REM
1250  REM  GET DEGREES
1260  REM
1270 J = I - 1
1280 DG =  VAL ( MID$ (DL$,1,J))
1290  REM
1300  REM  NOW LOOK FOR MINUTES
1310  REM
1320 MN = 0:KK = 0
1330 I = I + 1
1340  IF  MID$ (DL$,I,1) =  CHR$
     (32) THEN  GOTO 1400
1350  IF (I = LE) THEN  GOTO 1220

1360 I = I + 1:KK = 1: GOTO 1340
1370  REM
1380  REM  GET MINUTES
1390  REM
1400 JK = I - 1
1410  IF KK <  > 0 THEN MN =  VAL
     ( MID$ (DL$,J + 1,JK))
1420  REM
1430  REM  DEGREES BETWEEN 0-90 A
     ND MINUTES BETWEEN 0-60?
1440  REM
1450  IF  NOT (DG > 90 OR DG < 0 OR
     MN > 60 OR MN < 0) THEN  GOTO
     1540
1460  REM
1470  REM  DEG,MIN BETWEEN CORREC
     T LIMITS
1480  REM
1490  VTAB 20: HTAB 1: PRINT "DEG
     REES ARE BETWEEN 0 AND 90 AN
     D MINUTESARE BETWEEN 0 AND 6
     0.": PRINT "ANY KEY TO CONTI
     NUE ";: GET K$: PRINT K$
1500  VTAB 5: HTAB 1: CALL  - 958
     : GOTO 1080
1510  REM
1520  REM  CONVERT TO DECIMAL
1530  REM
1540 L1 = DG + (MN / 60)
1550  REM
1560  REM  N OR S?
1570  REM
1580 I = I + 1
1590 NS$ =  MID$ (DL$,I,1)
1600  IF NS$ = "N" OR NS$ = "S"
      THEN GOTO 1690
1610  REM
1620  REM  MUST BE NORTH OR SOUTH

1630  REM
1640  VTAB 20: HTAB 1: PRINT "ENT
     ER EITHER N FOR NORTH OR S F
     OR SOUTH.ANY KEY TO CONTINUE
     . ";: GET K$: PRINT K$
1650  VTAB 5: HTAB 1: CALL  - 958
     : GOTO 1080
1660  REM
1670  REM  PUT IN CORRECT SIGN FO
     R LATITUDE
1680  REM
1690  IF NS$ = "S" THEN L1 =  - L
     1
1700  REM
1710  REM
1720  REM  NOW GET CITY LONGITUDE

1730  REM
1740  REM
1750  VTAB 11: HTAB 1
1760  PRINT "ENTER THE CITY LONGI
     TUDE USING SPACES TOSEPARATE
      DEGREES MINUTES AND E(AST)
     OR W(EST).": INPUT DL$
1770  REM
1780  REM    NOW DECOMPOSE DL$ IN
     TO DEGREES,MINUTES AND E OR
     W
1790  REM  DO DEGREES FIRST
1800  REM
1810 LE =  LEN (DL$)
1820 I = 1
1830  IF  MID$ (DL$,I,1) =  CHR$
     (32) THEN  GOTO 1950
1840  IF (I = LE) THEN  GOTO 1900

1850 I = I + 1: GOTO 1830
1860  REM
1870  REM  DATA IS NOT IN PROPER
     FORMAT
1880  REM  GIVE ERROR MESSAGE AND
      DO AGAIN
1890  REM
1900  VTAB 20: HTAB 1: PRINT "WHE
     N YOU ENTER THE LONGITUDE, B
     E SURE TOUSE SPACES TO SEPAR
     ATE THE ENTRIES. ": PRINT "A
     NY KEY TO CONTINUE ";: GET K
     $: PRINT K$
1910  VTAB 11: HTAB 1: CALL  - 95
     8: GOTO 1750
1920  REM
1930  REM  GET DEGREES
1940  REM
1950 J = I - 1
1960 DG =  VAL ( MID$ (DL$,1,J))
1970  REM
1980  REM  NOW LOOK FOR MINUTES
1990  REM
2000 MN = 0:KK = 0
2010 I = I + 1
```

Listing 1 continued on page 426

Listing 1 continued:

```
2020  IF  MID$ (DL$,I,1) =  CHR$
     (32) THEN  GOTO 2080
2030  IF (I = LE) THEN  GOTO 1900

2040 I = I + 1:KK = 1: GOTO 2020
2050  REM
2060  REM  GET MINUTES
2070  REM
2080 JK = I - 1
2090  IF KK <  > 0 THEN MN =  VAL
     ( MID$ (DL$,J + 1,JK))
2100  REM
2110  REM   DEGREES BETWEEN 0-180
      AND MINUTES BETWEEN 0-60?
2120  REM
2130  IF  NOT (DG > 180 OR DG < 0
      OR MN > 60 OR MN < 0) THEN
      GOTO 2220
2140  REM
2150  REM  DEG,MIN BETWEEN CORREC
     T LIMITS
2160  REM
2170  VTAB 20: HTAB 1: PRINT "DEG
     REES ARE BETWEEN 0 AND 180 A
     ND        MINUTES ARE BETWEEN
      0 AND 60.": PRINT "ANY KEY
     TO CONTINUE ";: GET K$: PRINT
      K$
2180  VTAB 11: HTAB 1: CALL  - 95
     8: GOTO 1750
2190  REM
2200  REM  CONVERT TO DECIMAL
2210  REM
2220 M1 = DG + (MN / 60)
2230  REM
2240  REM   E OR W
2250  REM
2260 I = I + 1
2270 EW$ =  MID$ (DL$,I,1)
2280  IF EW$ = "E" OR EW$ = "W"
      THEN GOTO 2370
2290  REM
2300  REM   MUST BE EAST OR WEST
2310  REM
2320  VTAB 20: HTAB 1: PRINT "ENT
     ER EITHER E FOR EAST OR W FO
     R WEST.  ANY KEY TO CONTINUE
     .  ";: GET K$: PRINT K$
2330  VTAB 11: HTAB 1: CALL  - 95
     8: GOTO 1750
2340  REM
2350  REM   PUT IN CORRECT SIGN F
     OR LONGITUDE
2360  REM
2370  IF EW$ = "W" THEN M1 =  - M
     1
2380  RETURN
```

```
3000  REM  ****
3010  REM
3020  REM   MODULE TO GET SATELLI
     TE NAME AND LONGITUDE.
3030  REM
3040  REM  ****
3050  HOME
3060  PRINT "WHAT IS THE NAME OF
     THE SATELLITE?  ": INPUT NS$

3070  PRINT : PRINT
3080  PRINT "ENTER THE SATELLITE
      LONGITUDE USING    SPACES T
     O SEPARATE DEGREES MINUTES A
     ND  E(AST) OR W(EST).": INPUT
      SL$
3090  REM
3100  REM    NOW DECOMPOSE SL$ IN
     TO DEGREES,MINUTES AND E OR
     W
3110  REM  DO DEGREES FIRST
3120  REM
3130 LE =  LEN (SL$)
3140 I = 1
3150  IF  MID$ (SL$,I,1) =  CHR$
     (32) THEN  GOTO 3270
3160  IF (I = LE) THEN  GOTO 3220

3170 I = I + 1: GOTO 3150
3180  REM
3190  REM  DATA IS NOT IN PROPER
     FORMAT
3200  REM  GIVE ERROR MESSAGE AND
      DO AGAIN
3210  REM
3220  VTAB 20: HTAB 1: PRINT "WHE
     N YOU ENTER THE LONGITUDE, B
     E SURE TO USE SPACES TO SEPA
     RATE THE ENTRIES. ": PRINT "
     ANY KEY TO CONTINUE ";: GET
     K$: PRINT K$
3230  VTAB 11: HTAB 1: CALL  - 95
     8: GOTO 1750
3240  REM
3250  REM  GET DEGREES
3260  REM
3270 J = I - 1
3280 DG =  VAL ( MID$ (SL$,1,J))
3290  REM
3300  REM  NOW LOOK FOR MINUTES
3310  REM
3320 MN = 0:KK = 0
3330 I = I + 1
3340  IF  MID$ (SL$,I,1) =  CHR$
     (32) THEN  GOTO 3400
3350  IF (I = LE) THEN  GOTO 3090

3360 I = I + 1:KK = 1: GOTO 3340
```

Listing 1 continued:

```
3370  REM
3380  REM  GET MINUTES
3390  REM
3400 JK = I - 1
3410  IF KK <  > 0 THEN MN =  VAL
     ( MID$ (SL$,J + 1,JK))
3420  REM
3430  REM   DEGREES BETWEEN 0-180
      AND MINUTES BETWEEN 0-60?
3440  REM
3450  IF  NOT (DG > 180 OR DG < 0
      OR MN > 60 OR MN < 0) THEN
      GOTO 3540
3460  REM
3470  REM  DEG,MIN BETWEEN CORREC
     T LIMITS
3480  REM
3490  VTAB 20: HTAB 1: PRINT "DEG
     REES ARE BETWEEN 0 AND 180 A
     ND        MINUTES ARE BETWEEN
      0 AND 60.": PRINT "ANY KEY
     TO CONTINUE ";: GET K$: PRINT
     K$
3500  VTAB 5: HTAB 1: CALL  - 958
     : GOTO 3080
3510  REM
3520  REM  CONVERT TO DECIMAL
3530  REM
3540 M2 = DG + (MN / 60)
3550  REM
3560  REM   E OR W
3570  REM
3580 I = I + 1
3590 EW$ =  MID$ (SL$,I,1)
3600  IF EW$ = "E" OR EW$ = "W"
      THEN GOTO 3690
3610  REM
3620  REM   MUST BE EAST OR WEST
3630  REM
3640  VTAB 20: HTAB 1: PRINT "ENT
     ER EITHER E FOR EAST OR W FO
     R WEST.": PRINT "ANY KEY TO
     CONTINUE.  ";: GET K$: PRINT
     K$
3650  VTAB 11: HTAB 1: CALL  - 95
     8: GOTO 1750
3660  REM
3670  REM   PUT IN CORRECT SIGN F
     OR LONGITUDE
3680  REM
3690  IF EW$ = "W" THEN M2 =  - M
     2
3700  RETURN
4000  REM  ****
4010  REM
4020  REM  HEADER MODULE
4030  REM
4040  REM  ****
4050  REM  THIS MODULE DOES THE H
     EADER AND GIVE INSTRUCTIONS
     AS NEEDED
4060  REM
4070  TEXT : HOME
4080  VTAB 10: HTAB 14: PRINT "G
     E O S A T"
4090  VTAB 13: HTAB 9: PRINT "LOO
     K ANGLE CALCULATOR"
4100  FOR I = 1 TO 2000: NEXT I
4110  HOME
4120  VTAB 4: HTAB 1
4130  PRINT " THIS PROGRAM WILL A
     LLOW YOU TO"
4140  PRINT " DETERMINE WHERE YOU
      HAVE TO POINT"
4150  PRINT " AN ANTENNA TO PERMI
     T RECEPTION OF"
4160  PRINT " SIGNALS TRANSMITTED
      FROM A
4170  PRINT " GEOSYNCHRONOUS SATE
     LLITE."
4180  PRINT : PRINT
4190  PRINT " IF YOU NEED INSTRUC
     TIONS ON THE"
4200  PRINT " OPERATION OF THIS P
     ROGRAM,PRESS"
4210  PRINT " THE <ESC> KEY.  OTH
     ERWISE ANY"
4220  PRINT " OTHER KEY WILL STAR
     T THE PROGRAM."
4230  PRINT
4240  PRINT " THE INSTRUCTIONS AR
     E CONTAINED ON"
4250  PRINT " SEVERAL PAGES.  TO
     SEE THE VARIOUS"
4260  PRINT " PAGES, USE ANY KEY
     TO CHANGE THE"
4270  PRINT " DISPLAY."
4280  VTAB 22: HTAB 2: PRINT "<ES
     C> TO GET INSTRUCTIONS"
4290  PRINT " ANY OTHER KEY TO ST
     ART ";: GET KB$: PRINT KB$
4300  REM
4310  REM  WHAT IS KB$?
4320  REM
4330  IF KB$ <  >  CHR$ (27) THEN
      GOTO 6080
4340  REM
4350  REM  GIVE INSTRUCTIONS
4360  REM
4370  HOME
4380  PRINT : PRINT
4390  PRINT "WHENEVER THERE ARE P
     ARENTHESES AROUND"
4400  PRINT "WORDS OR GROUPS OF L
```

Listing 1 continued on page 428

Listing 1 continued:

```
     ETTERS IN THE"
4410  PRINT "INSTRUCTIONS, THIS M
     EANS THAT THE"
4420  PRINT "THINGS INSIDE THE PA
     RENTHESES ARE"
4430  PRINT "OPTIONAL."
4440  PRINT
4450  PRINT "ITEMS INSIDE THE SYM
     BOLS < > ARE"
4460  PRINT "REQUIRED OPERATIONS
     OR ENTRIES."
4470  PRINT
4480  PRINT " <SP>   IS THE SPACE
      KEY."
4490  PRINT " <RTN>  IS THE RETUR
     N KEY."
4500  PRINT " <ESC>  IS THE ESCAP
     E KEY."
4510  VTAB 24: HTAB 39: GET KB$:
     PRINT KB$
4520  HOME
4530  PRINT
4540  PRINT "AS A PART OF THIS PR
     OGRAM, THERE ARE 2"
4550  PRINT "DATA SETS. ONE CONSI
     STS OF A NUMBER OF"
4560  PRINT "SATELLITES AND THEIR
      LONGITUDES. THE"
4570  PRINT "OTHER IS A NUMBER OF
      CITIES AND THEIR"
4580  PRINT "LATITUDES AND LONGIT
     UDES."
4590  PRINT
4600  PRINT "FOR EACH DATA SET, Y
     OU WILL BE ASKED"
4610  PRINT "WHETHER YOU WISH TO
     USE THE INFORMATION"
4620  PRINT "ALREADY IN THE PROGR
     AM OR WISH TO ENTER"
4630  PRINT "NEW INFORMATION."
4640  PRINT
4650  PRINT "IF YOU CHOOSE TO USE
      THE INFORMATION"
4660  PRINT "ALREADY IN THE PROGR
     AM, SIMPLY ENTER"
4670  PRINT "THE NUMBER THAT CORR
     ESPONDS TO THE CITY"
4680  PRINT "OR SATELLITE YOU DES
     IRE AND PRESS"
4690  PRINT "THE <RTN> KEY."
4700  PRINT
4710  PRINT "IF YOU WISH TO ENTER
      YOUR OWN CITY OR"
4720  PRINT "SATELLITE, PRESS ANY
      KEY THAT DOES NOT"
4730  PRINT "CORRESPOND TO A CITY
      OR SATELLITE AND"
4740  PRINT "PRESS <RTN>."
4750  VTAB 24: HTAB 39: GET KB$:
     PRINT KB$
4760  HOME
4770  PRINT
4780  PRINT "YOU WILL THEN BE ASK
     ED SEVERAL"
4790  PRINT "QUESTIONS."
4800  PRINT
4810  PRINT "FOR NAMES OF CITIES
     OR SATELLITES ENTER"
4820  PRINT "WHATEVER YOU WISH.
     USE SPACES AND NOT"
4830  PRINT "COMMAS AS SEPARATORS
      IF NEEDED."
4840  PRINT
4850  PRINT "WHEN LATITUDE INFORM
     ATION IS REQUESTED,"
4860  PRINT "ENTER THE DATA IN TH
     E FORMAT:"
4870  PRINT
4880  PRINT "DEGREES <SP> MINUTES
      <SP> N OR S <RTN>"
4890  PRINT
4900  PRINT "N(ORTH) OR S(OUTH) M
     UST BE ENTERED, BUT"
4910  PRINT "IF YOU WISH TO SKIP
     THE DEGREE OR"
4920  PRINT "MINUTE ENTRY JUST EN
     TER A SPACE INSTEAD"
4930  PRINT "OF THE NUMBER. COMPL
     ETE THE ENTRY BY"
4940  PRINT "PRESSING THE RETURN
     KEY."
4950  PRINT
4960  PRINT "THE IDENTICAL FORMAT
      IS USED FOR"
4970  PRINT "LONGITUDE DATA. JUST
      REPLACE N OR S BY"
4980  PRINT "E(AST) OR W(EST)."
4990  VTAB 24: HTAB 39: GET KB$:
     PRINT KB$
5000  HOME
5010  PRINT : PRINT : PRINT
5020  PRINT "IF YOU NEED TO SEE T
     HE INSTRUCTIONS"
5030  PRINT "AGAIN, PRESS <ESC>.
      OTHERWISE, USE ANY"
5040  PRINT "OTHER KEY TO START T
     HE PROGRAM."
5050  VTAB 24: HTAB 39: GET KB$:
     PRINT KB$
5060  IF KB$ =  CHR$ (27) THEN
     GOTO 4370
6000  REM  ****
6010  REM
6020  REM   INITIALIZATION MODULE
```


Listing 1 continued:

```
6030  REM
6040  REM  ****
6050  REM
6060  REM  SOME CONSTANTS
6070  REM
6080  HOME :R = 6378:H = 35500:PI
      = 3.14159
6090 RD = 360 / (2 * PI)
6100  REM
6110  REM  ARCSIN DEFINATION
6120  REM
6130  DEF  FN ARCSYN(X) =  ATN (X
      /  SQR ( - X * X + 1))
6140  REM
6150  REM   MODULUS DEFINITION
6160  REM
6170  DEF  FN MOD(Z) =  INT ((Z /
     ZF -  INT (Z / ZF)) * ZF + .
     05) *  SGN (Z / ZF)
6180  REM
6190  REM  READ IN THE SATELLITE
     PARAMETERS
6200  REM
6210  RESTORE
6220  REM
6230  REM  N IS THE NUMBER OR SAT
     ELLITES IN THE LIST
6240  REM
6250  READ N
6260  REM
6270  REM  SN$( IS NAME ARRAY AND
      SN( IS LONGITUDE ARRAY
6280  REM
6290  IF FG = 1 THEN  GOTO 6340
6300  DIM SN$(N),SN(N),DS$(N),DS(
     N),P$(24)
6310  REM
6320  REM  P$( IS PRINTER BUFFER
6330  REM
6340  FOR I = 1 TO N
6350  READ SN$(I)
6360  READ SN(I)
6370  NEXT I
6380 SN(0) = N
6390  REM
6400  REM  A( IS LOOK AZIMUTH ARR
     AY AND E( IS LOOK ELEVATION
     ARRAY
6410  REM
6420  IF FG = 1 THEN  GOTO 6490
6430  DIM A(N),E(N)
6440  REM
6450  REM  READ IN CITY PARAMETER
     S
6460  REM
6470  REM
6480  REM  M IS NUMBER OF CITIES
6490  READ M
6500  REM
6510  REM  CN$( IS CITY NAME ARRA
     Y;CL( IS CITY LATITUDE ARRAY
     ; CM( IS CITY LONGITUDE ARRA
     Y
6520  REM
6530  IF FG = 1 THEN  GOTO 6550
6540  DIM CN$(M),CL(M),CM(M)
6550  FOR I = 1 TO M
6560  READ CN$(I)
6570  READ CL(I)
6580  READ CM(I)
6590  NEXT I
6600 CL(0) = M
7000  REM  ****
7010  REM
7020  REM  THIS MODULE GIVES THE
     CITY LIST ALONG WITH THE OPT
     ION OF CHOOSING ONE OF THE S
     TORED CITIES OR ENTERING A N
     EW ONE
7030  REM
7040  REM  ****
7050  HOME
7060  VTAB 2: HTAB 1: PRINT "THES
     E CITIES ARE AVAILABLE:": VTAB
     5: HTAB 1
7070  REM
7080  REM  GET NUMBER OF CITIES.
     IF >30 THEN TRUNCATE.
7090  REM
7100 M = CL(0)
7110  IF M > 30 THEN M = 30
7120  REM
7130  REM  DETERMINE NUMBER OF RO
     WS OF DUAL COLUMN PRINTING N
     EEDED
7140  REM
7150 M1 = M / 2:M2 =  INT (M1):MP
      = M1 - M2
7160  REM
7170  REM  DEFAULT TAB OFFSET POS
     ITIONS
7180  REM
7190 HL = 3:HR = 23
7200  FOR I = 1 TO M2
7210 J = I + M2
7220  REM
7230  REM  IF MP=0 THERE WILL BE
     2 COLUMNS ON EACH ROW.  OTHE
     RWISE THERE WILL BE AN EXTRA
      ROW.
7240  REM
7250  IF MP <  > 0 THEN J = J + 1

7260  REM
```

Listing 1 continued on page 430

Listing 1 continued:

```
7270  REM  GOSUB  DETERMINES THE
      NUMBER OF DIGITS IN I,J
7280  REM
7290  GOSUB 30000
7300  PRINT  TAB( HL - H1);I; TAB(
      HL + 2);CN$(I); TAB( HR - H2
      );J; TAB( HR + 2);CN$(J)
7310  NEXT I
7320  IF MP <  > 0 THEN  GOSUB 30
      000: PRINT  TAB( HL - H1);I;
       TAB( HL + 2);CN$(I)
7330  REM
7340  REM  GET CHOICE OF CITY.  O
      NLY ONE AT A TIME!!!
7350  REM
7360  VTAB 21: HTAB 1: PRINT "ENT
      ER YOUR CHOICE BY INDICATING
      :"
7370  PRINT  TAB( 2);"A NUMBER BE
      TWEEN 1 AND ";M;" OR USING "

7380  PRINT  TAB( 2);"ANY OTHER K
      EY FOR A NEW CITY  ";: INPUT
      KB$
7390  REM
7400  REM  WHAT IS KB$
7410  REM
7420 CK =  VAL (KB$)
7430  IF CK < 1 OR CK > M THEN
      GOSUB 1050:CK = M + 1
7440  REM
7450  REM  NOW DO SATELLITE
7460  REM
8000  REM  ****
8010  REM
8020  REM   THIS MODULE GIVES THE
       SATELLITE  LIST ALONG WITH
      THE OPTION OF USING ALL THE
      STORED NAMES OR ENTERING A N
      EW ONE
8030  REM
8040  REM  ****
8050  HOME
8060  VTAB 2: HTAB 1: PRINT "THES
      E SATELLITES ARE AVAILABLE:"
      : VTAB 5: HTAB 1
8070  REM
8080  REM  GET NUMBER OF SATELLIT
      ES.  IF >30 TRUNCATE
8090  REM
8100 N = SN(0)
8110  IF N > 30 THEN N = 30
8120  REM
8130  REM  DETERMINE NUMBER OF DU
      AL COLUMN PRINTINGS NEEDED
8140  REM
8150 N1 = N / 2:N2 =  INT (N1):NP
      = N1 - N2
8160  REM
8170  REM  DEFAULT TAB OFFSET POS
      ITIONS
8180  REM
8190 HL = 3:HR = 23
8200  FOR I = 1 TO N2
8210 J = I + N2
8220  REM
8230  REM   IF NP=0 THEN THERE WI
      LL BE 2 COLUMNS FOR EACH ROW
      .  OTHERWISE, AN EXTRA ROW I
      S NEEDED.
8240  REM
8250  IF NP <  > 0 THEN J = J + 1

8260  REM
8270  REM  GOSUB DETERMINES THE N
      UMBER OF DIGITS IN I,J
8280  REM
8290  GOSUB 30000
8300  PRINT  TAB( HL - H1);I; TAB(
      HL + 2);SN$(I); TAB( HR - H2
      );J; TAB( HR + 2);SN$(J)
8310  NEXT I
8320  IF NP <  > 0 THEN  GOSUB 30
      000: PRINT (HL - H1);I; TAB(
      HL + 2);SN$(I)
8330  REM
8340  REM  NOW GET CHOICE OF WHIC
      H SATELLITE(S) TO USE
8350  REM
8360  VTAB 20: HTAB 1: PRINT "ENT
      ER YOUR CHOICE:"
8370  PRINT  TAB( 2);"ZERO(0) TO
      USE ALL OR": PRINT  TAB( 2);
      "ANY NUMBER BETWEEN 1 AND ";
      N;" OR": PRINT  TAB( 2);"ANY
       OTHER KEY FOR A NEW SATELLI
      TE ";: INPUT KB$
8380  REM
8390  REM  WHAT IS KB$
8400  REM
8410 SQ =  ASC (KB$)
8420 SK =  VAL (KB$)
8430  REM
8440  REM  GO GET A NEW SATELLITE
       ?
8450  REM
8460  IF SK = 0 AND (SQ < 48 OR S
      Q > 57) THEN  GOSUB 3050:SK =
      N + 1
9000  REM  ****
9010  REM
9020  REM  SETUP CITY,SATELLITE P
      ARAMETERS PRIOR TO AZ,EL CAL
      CULATION
9030  REM
```

Listing 1 continued:

```
9040  REM  ****
9050  REM
9060  REM  DO CITY FIRST
9070  REM
9080  IF CK > M THEN DC$ = NC$
9090  IF CK < = M THEN DC$ = CN$
     (CK):L1 = CL(CK):M1 = CM(CK)

9100  REM
9110  REM  DO SATELLITE.  FIRST S
     ETUP DEFAULT NAME ARRAY
9120  REM
9130 N = SN(0)
9140  FOR I = 0 TO N
9150 DS$(I) = SN$(I)
9160 DS(I) = SN(I)
9170  NEXT I
9180  REM
9190  REM  IF SK=0 USE ALL
9200  REM
9210  IF SK = 0 THEN  GOTO 9350
9220  REM
9230  REM  DISTINGUISH BETWEEN SK
     =1,N AND SK>N
9240  REM
9250 DS(0) = 1
9260  IF SK > N THEN  GOTO 9300
9270 DS$(1) = DS$(SK)
9280 DS(1) = DS(SK)
9290  GOTO 9350
9300 DS$(1) = NS$
9310 DS(1) = M2
9320  REM
9330  REM  NOW DO AZ,EL CALCULATI
     ON
9340  REM
9350 MX = DS(0)
9360  FOR I = 1 TO MX
9370 M2 = DS(I)
9380  GOSUB 210
9390 A(I) = Y:E(I) = EL
9400  NEXT I
10000  REM  ****
10010  REM
10020  REM   THIS MODULE DOES THE
      SCREEN DISPLAY OF THE CALCU
     LATION RESULTS
10030  REM
10040  REM  ****
10050  HOME
10060  VTAB 2: HTAB 4: PRINT "FRO
     M: ";DC$
10070  VTAB 5: HTAB 29: PRINT "AN
     TENNA"
10080  PRINT  TAB( 4);"TO"; TAB(
     26);"AZIMUTH"; TAB( 35);"ELE
     V."
10090  REM
10100  REM  SETUP TEXT WINDOW TO
     PROTECT LABLES
10110  REM
10120  POKE 34,7
10130  REM
10140  REM  SOME DEFAULTS: LINES/
     PAGE;START LINE;STOP LINE;AZ
     ,EL TABS
10150  REM
10160 LP = 15:ST = 1:SP = LP:HL =
     31:HR = 38
10170  REM
10180  REM  DETERMINE NUMBER OF D
     ISPLAY PAGES
10190  REM
10200 Z1 =  INT (N / 15)
10210 ZP = Z1 + 1
10220  REM
10230  REM  DISPLAY PAGE LOOP
10240  REM
10250  FOR ZQ = 1 TO ZP
10260  VTAB 8
10270  IF DS(0) < SP THEN SP = DS
     (0)
10280  FOR ZR = ST TO SP
10290 I = A(ZR):J = E(ZR)
10300  GOSUB 30000
10310  PRINT  TAB( 2);DS$(ZR); TAB(
     HL - H1);I; TAB( HR - H2);J
10320  NEXT ZR
10330  VTAB 24
10340  PRINT "<ESC> TO PRINT/ANY
     KEY TO CONTINUE ";: GET KB$
10350  REM
10360  REM  IF KB$=CHR$(27) THEN
     GOTO PRINT ROUTINE
10370  REM
10380  IF KB$ =  CHR$ (27) THEN
     GOSUB 50000
10390 ST = SP + 1:SP = SP + LP: HOME

10400  NEXT ZQ
10410  REM
10420  REM  DO ANOTHER SET?
10430  REM
10440  TEXT : HOME
10450  PRINT : PRINT
10460  PRINT "USE <ESC> TO USE TH
     E PROGRAM AGAIN."
10470  PRINT "USE <RTN> TO LEAVE
     THE PROGRAM."
10480  GET KB$: PRINT KB$
10490  IF KB$ =  CHR$ (27) THEN F
     G = 1: GOTO 6080
10500  IF KB$ =  CHR$ (13) THEN
      GOTO 10520
```

Listing 1 continued on page 432

Listing 1 continued:

```
10510  GOTO 10440
10520  TEXT : HOME : END
20000  REM
20010  REM  DATA STATEMENTS
20020  REM
20030  DATA  12
20040  DATA  COMSTAR 3,-87
20050  DATA  WESTAR 3,-91
20060  DATA  COMSTAR 2,-95
20070  DATA  WESTAR 1,-99
20080  DATA   ANIK 1,-104
20090  DATA   ANIK 2,-109
20100  DATA  ANIK 3,-114
20110  DATA  SATCOM 2,-119
20120  DATA  WESTAR 2,-123.5
20130  DATA  COMSTAR 1,-128
20140  DATA  SATCOM 3,-132
20150  DATA  SATCOM 1,-135
20160  DATA  11
20170  DATA  WASHINGTON D.C.,39,-
    77
20180  DATA  LOS ANGELES,34,-118
20190  DATA  NEW YORK,40.5,-74
20200  DATA  ATLANTA,33.5,-84.5
20210  DATA  MIAMI,25.75,-80.25
20220  DATA  JACKSONVILLE,30.5,-8
    1.5
20230  DATA  TAMPA,28,-82.75
20240  DATA  ANCHORAGE,60.8,-147
20250  DATA  NOME,65,-165
20260  DATA  PHOENIX,33.5,-112
20270  DATA  LITTLE ROCK,34.75,-9
    2.25
29970  REM
29980  REM  TAB POSITIONING ROUTI
    NE
29990  REM
30000 H1 = 3:H2 = 3
30010  IF I < 100 THEN H1 = 2
30020  IF I < 10 THEN H1 = 1
30030  IF J < 100 THEN H2 = 2
30040  IF J < 10 THEN H2 = 1
30050  RETURN
49950  REM
49960  REM  PRINTER ROUTINE
49970  REM
49980  REM  FOLLOWS SCREEN FORMAT
     SHOWN ON PAGE 16 OF APPLE R
    EFERENCE MANUAL
49990  REM
50000  FOR I = 1 TO 3
50010 LN = 1024 + (I - 1) * 40
50020  FOR J = 1 TO 8
50030 LM = LN + (J - 1) * 128
50040 A$ = "     "
50050  FOR K = 0 TO 39
50060 A$ = A$ +  CHR$ ( PEEK (LM +
    K))
50070  NEXT K
50080 P$(8 * (I - 1) + J) = A$
50090  NEXT J: NEXT I
50100  PR# 2
50110  FOR J = 1 TO 23
50120  PRINT P$(J): NEXT J
50130  PR# 0
50140  RETURN
```

Z80 Starting Address
One Jump Further

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While designing my homebrew Z80-based computer system, I realized it would be a great advantage to have programmable memory in the first page of memory space. If I could reach that goal, I could make full use of the Z80's restart locations for more flexible programming. But I needed a way to pass control to a memory page other than page 0, where a program in EPROM (erasable programmable read-only memory) would be located. Because experience has taught me to rank flexibility in microprocessor systems as a high priority, I wanted to be able to start at any page.

My approach is similar to the one proposed by Randy Soderstrom in "Forcing the Z80 Starting Address" (February 1981 BYTE, page 288), but mine provides flexibility and the lower device count desirable in a microprocessor system. Program execution can be directed to any of the Z80's 256 memory pages by setting an 8-bit DIP (dual-inline package) switch to the appropriate setting to indicate the desired page, using four integrated circuits.

As shown in figure 1, two SN74LS257 multiplexers drive the switch-settings onto the data bus at the appropriate time. These devices have three-state outputs allowing them to be connected directly to the data bus.

Figure 2 shows the timing sequence associated with the circuit operation. The timing of the forced-jump instruction is controlled by the dual D flip-flop circuit made of IC3. When $\overline{\text{RESET}}$ occurs, these two flip-flops are set, causing the $\overline{\text{JUMP ENABLE}}$ signal to go low. This, in turn, prevents any $\overline{\text{RD}}$ pulses from enabling the bus receivers, and also enables IC1 and IC2 to drive the Z80 data lines.

After a reset, the first address the Z80 places on the address bus is 0000 hexadecimal. The byte it fetches from this address will be interpreted as an operation code, making $\overline{\text{M1}}$ go low and causing IC3 to reset. This action stores the first occurrence of $\overline{\text{M1}}$. With address lines A0 and A1 low, the value placed on the data bus will be C3 hexadecimal—the operation code for a jump instruction. When the address lines go to 0001 hexadecimal to fetch the low byte of the jump address, the multiplexers will place 00 on the data bus. When the address lines go to 0002 to fetch the high byte of the jump address, the value of the 8-bit DIP switch is placed on the data bus. The characteristics of TTL (transistor-transistor logic) mean pullup resistors are not needed on the DIP switch. An open switch will assume a logic 1 state and a closed switch will assume a logic 0 state.

The cursor in figure 2 marks the first $\overline{\text{RD}}$ cycle in the previous sequence. The Z80 will now execute a jump to location *xxxxxxxx*00000000 binary, where *xxxxxxxx* represents the value set by the DIP switch. At this location an operation-code fetch cycle is executed. When $\overline{\text{M1}}$ goes low after this cycle, IC2b is reset, marking the second occurrence of $\overline{\text{M1}}$. The $\overline{\text{JUMP ENABLE}}$ signal is then disabled and the bus-receiver $\overline{\text{RD}}$ signal reenabled. The E marker in figure 2 indicates this point in the timing. The Z80 is now executing program code starting at the page specified by the DIP switch setting.

On my processor card, I connected the data lines of this circuit directly to the Z80 data lines. I connected the $\overline{\text{BUFFER RD}}$ signal to the bus receivers that buffer the backplane to the Z80 data bus. In this way, memory that would normally be read at memory address 0000 would

Number	Type	+5 V	GND
IC1	74LS257	16	. 8
IC2	74LS257	16	8
IC3	74LS74	14	7
IC4	74LS00	14	7

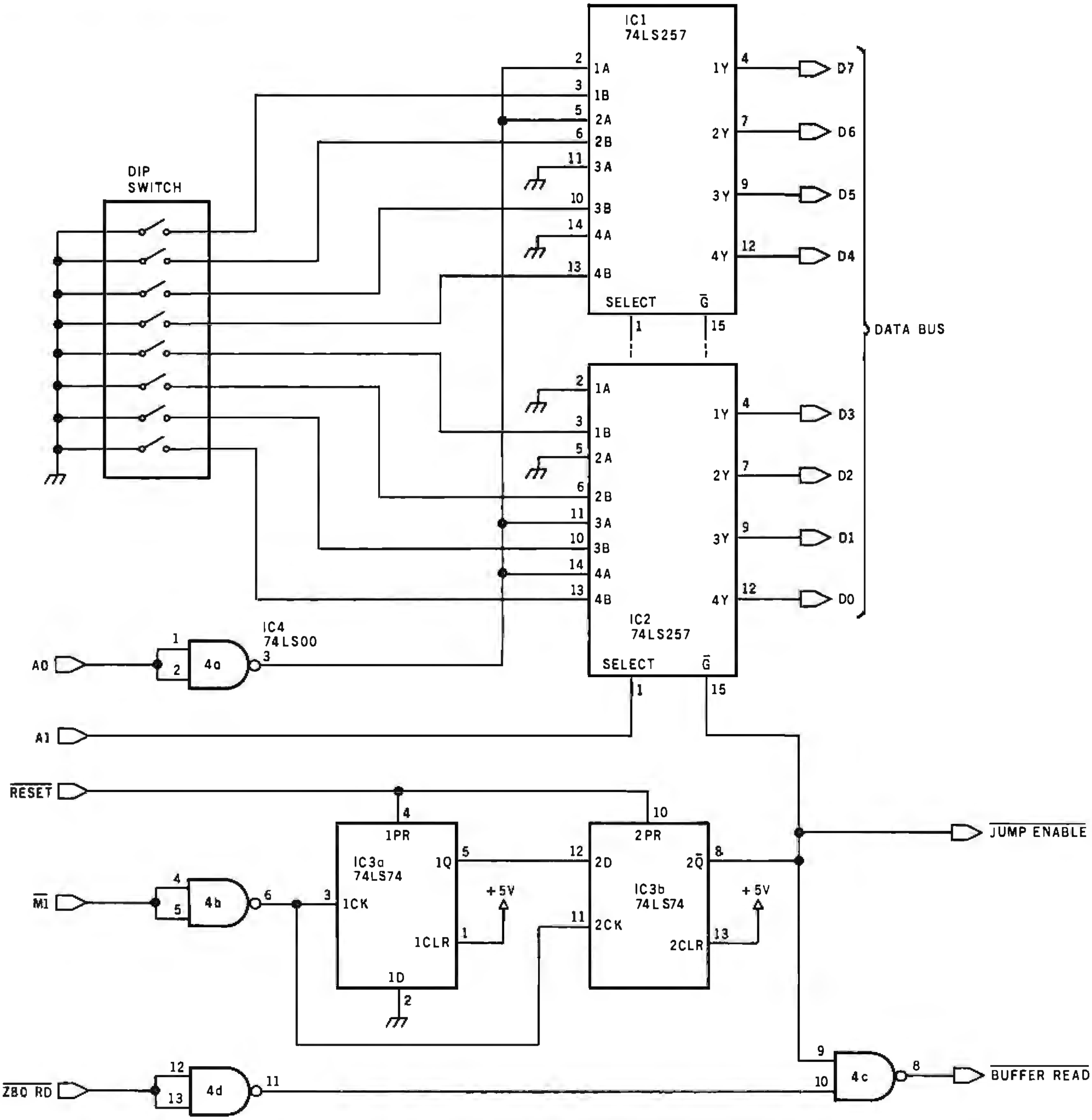

Figure 1: *Schematic diagram of the circuit used to force Z80 starting addresses to any of 256 memory pages. IC1 and IC2 are three-state multiplexers that pass the address set by the switches when the proper combination of reset signals occurs.*

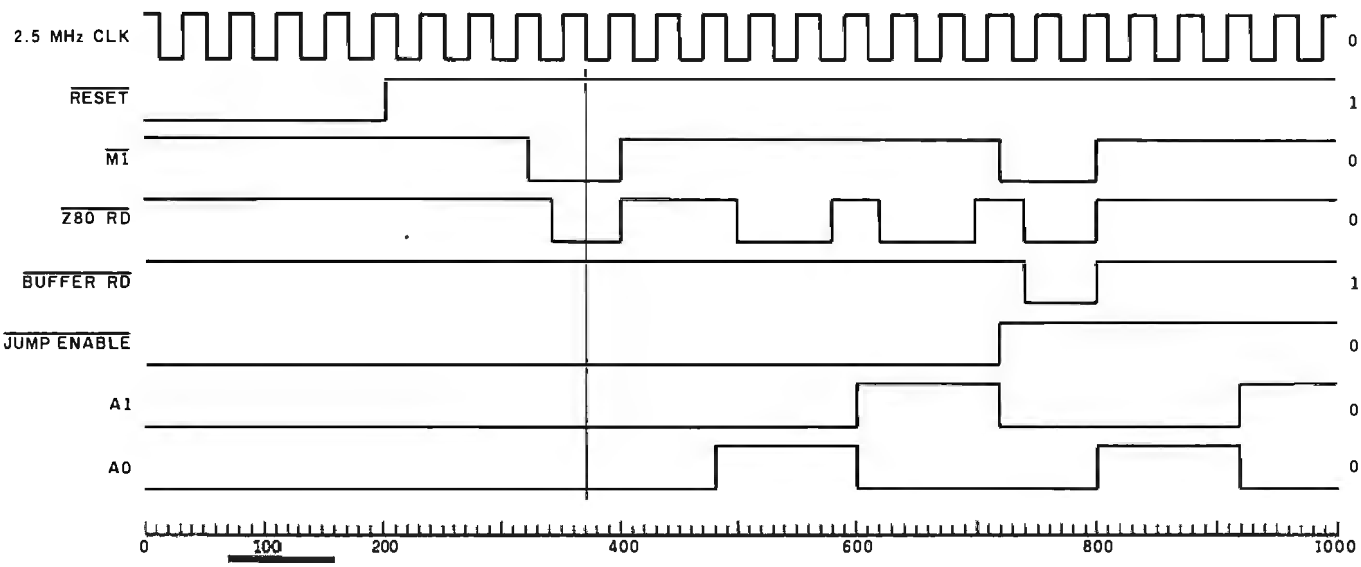

Figure 2: *Timing relationships of the forced jump.*

not affect program flow during the forced-jump sequence. But the circuit could be connected to directly disable memory as suggested by Soderstrom.

If your system has a negative-true bus, you can use an SN74LS258 in place of the SN74LS257. And if you need more current-driving capability, you can use regular TTL in place of the LS TTL in the multiplexer chips.■

SOFTIM
A Software Timer

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I recently found myself in a situation where I had to use a Z80-based microcomputer to collect data as a function of time, then average that data over an extended period of time and subject it to a Fourier transformation to analyze its frequency dependence. This meant that I needed several highly accurate timers that I could set very precisely over a wide range of different time periods.

When precision and accuracy are required (as with computer-synthesized music), a timing job is often assigned to interrupt-driven hardware timer circuits, such as the Zilog CTC (counter/timer circuit) or the Intel 8253 programmable timer. These circuits base their timing intervals on crystal oscillators, and can fulfill a wide range of timing functions if they are available in a system.

If the timing requirements are not very rigid (as with games or video animation), simple software loops are usually adequate. These loops can be "tweaked" empirically to provide the aesthetically appropriate amount of delay.

But what do you do if you need precise, accurate time delays and you don't have the hardware to do it? Could I satisfy all those requirements with software?

I wrote a few simple timer routines, just to identify the problems that I had to solve. (I will classify the routines according to the number of bytes used to count repetitions of a timing loop.) My 1-byte timer was the simplest to code, but it was deficient in both resolution and dynamic range; the 2-byte timer was better in both respects but still not substantial enough for my purposes; the 3-byte timer had an adequate dynamic range, but the internal branching of the routine resulted in timing jitter that depended on the relative number of times each branch was executed. In addition, all of these routines had a finite amount of overhead as they entered and exited the timing loop, which lead to a constant error that was increasingly significant for shorter and shorter time delays.

As a result of these simple routines, I made a list of the characteristics for my ideal software timer:

- at least 3 counter bytes to allow an adequate dynamic range (ratio of longest time to shortest time)
- rapid execution for high resolution (brief timing loop)
- internal branches of identical length to eliminate branching jitter
- subroutine structure to avoid excessive code duplication
- setup and calling sequences within the timing loop to prevent constant timing errors
- capability of generating several different intervals or repeating the same interval in any given program
- time delays that can be defined at run-time from keyboard input or other sources
- if possible, a loop-execution time in even units to eliminate the need for a clumsy conversion routine that shifts from a human time frame to a software time frame

By carefully counting the T-states (external clock cycles) for each instruction (as given in the *Z80-CPU Technical Manual*), and after several false starts, I finally arrived at a deceptively simple program that I call SOFTIM, shown in listing 1. The time-delay count is stored as a 3-byte (24-bit) positive integer that can take on hexadecimal values from 1 to FFFFFF. It is located in memory with the bytes arranged in a low, middle, high format, and it is not modified by the timing loop (which allows the same time delay to be generated repeatedly). The necessary registers are loaded outside the subroutine so that several different time delays can be maintained

Listing 1: *The high-precision timing program, SOFTIM, written for the Zilog Z80 microprocessor. Careful attention to T-states (microprocessor clock cycles) allows high-resolution timing of a broad range of intervals in standard time units.*

```
                ;            **** SOFTIM:  Z80 SOFTWARE TIMER ****
                ;             **** WRITTEN BY:  DAN TERPSTRA ****
                ;              ***** CHEMISTRY  DEPARTMENT *****
                ;               ** FLORIDA STATE  UNIVERISTY **
                ;                ******************************
                ;
                ;     The execution time of this routine is given by:
                ;                         T = (N+2)*40
                ;  where  T is the time in t-states,  and N is the 3  byte
                ;  (positive  integer) delay quantity obtained from memory
                ;  locations  LODELA,  HIDELA.   To calculate the time  in
                ;  seconds, multiply the number of t-states by the time of
                ;  one  clock cycle (e.g.  4 MHz =  250  ns/cycle).   This
                ;  timing  assumes  memory  that  operates  with  no  wait
                ;  states.  The minimum time of execution for a 4 MHz Z80
                ;  is  30  usec  for N = 1  (including the  CALL  and  RET
                ;  sequence),  increasing in steps of 10 usec to a maximum
                ;  of  over  160  sec.   N  = 0  is  undefined,  and  N  =
                ;  FFFFFF(HEX)  is the maximum time period.   There is  NO
                ;  software jitter in this timing loop.
                ;
                ;
                MAIN:              ;CALLING SEQUENCE (INCLUDED IN TIMING)
0100  2A1E01              LD      HL,(LODELA)        ;LOW ORDER COUNT WORD
0103  3A2001              LD      A,(HIDELA)         ;HIGH ORDER COUNT BYTE
0106  CD0A01              CALL    SOFTIM             ;TIME IT
                ;         ...CONTINUE WITH PROGRAM...
0109  C9                  RET
                ;
                ; SOFTIM SUBROUTINE
                ;
                ;  ENTRY CONDITIONS:
                ;         A, HL = 24 BIT POSITIVE COUNT
                ;  EXIT CONDITIONS:
                ;         A = B = HL = 0
                ;  MODIFIES:
                ;         A, B, HL
                ;
010A  3C        SOFTIM:   INC     A                  ;AT LEAST ONE PASS
010B  47                  LD      B,A                ;THROUGH OUTER LOOP
010C  3E00                LD      A,0                ;DUMMY INSTRUCTIONS
010E  C31301              JP      SOFTM2             ;TO KILL TIME
0111  1800      SOFTM1:   JR      SOFTM2             ;DELAY 16 T STATES
0113  00        SOFTM2:   NOP
0114  2B        SOFTM3:   DEC     HL                 ;DECREMENT LOW ORDER
0115  7D                  LD      A,L
0116  B4                  OR      H                  ;HL = 0?
0117  C21101              JP      NZ,SOFTM1          ;NO, LOOK AGAIN
011A  05                  DEC     B                  ;B = ZERO?
011B  20F7                JR      NZ,SOFTM3          ;NO, REPEAT OUTER LOOP
011D  C9                  RET                        ;YES, RETURN
                ;
                ;  STORAGE LOCATION FOR 24-BIT TIME DELAY WORD
011E  (0002)    LODELA:   DS      2                  ;LOW ORDER 16 BITS
0120  (0001)    HIDELA:   DS      1                  ;HIGH ORDER 8 BITS
```

Listing 2: *Version of SOFTIM modified for use with an Intel 8080 processor. This version provides resolution and range similar to the version shown in listing 1, but measurements are not provided in standard units of time.*

```
                ;          *****  SOFTIM: SOFTWARE TIMER *****
                ;           *** MODIFIED FOR 8080 FAMILY ***
                ;            ******************************
                ;
                ;       The execution time of this routine is given by:
                ;                        T = (N+2)*38
                ;  This is 2 t-states shorter than the equivalent Z80
                ;  routine, resulting in a slightly less managable minimum
                ;  time of 28.5 usec and a step size of 9.5 usec, again
                ;  assuming a 4 MHz clock.  All other features of the
                ;  timer remain identical to the Z80 version of this
                ;  program.
                ;
                ;
                MAIN:     ;CALLING SEQUENCE (INCLUDED IN TIMING)
0100 2A2001               LHLD    LODELA  ;LOW ORDER COUNT WORD
0103 3A2201               LDA     HIDELA  ;HIGH ORDER COUNT BYTE
0106 CD0A01               CALL    SOFTIM  ;TIME IT
                ;         ...CONTINUE WITH PROGRAM...
0109 C9                   RET
                ;
                ; SOFTIM SUBROUTINE FOR 8080
                ;
                ;  **********************************
                ;  CODE THAT DIFFERS FROM Z80 VERSION
                ;  IS MARKED OFF BY ASTERISKS
                ;  **********************************
                ;
010A 3C           SOFTIM: INR     A       ;AT LEAST ONE PASS
010B 47                   MOV     B,A     ;THROUGH OUTER LOOP
010C 3E00                 MVI     A,0     ;DUMMY INSTRUCTIONS
                ;*********************************************
010E C31501               JMP     SOFTM3  ;TO KILL TIME
0111 C31401       SOFTM1: JMP     SOFTM2  ;DELAY 14 T STATES
                ;*********************************************
0114 00           SOFTM2: NOP
0115 2B           SOFTM3: DCX     H       ;DECREMENT LOW ORDER
0116 7D                   MOV     A,L
0117 B4                   ORA     H       ;HL = 0?
0118 C21101               JNZ     SOFTM1  ;NO, LOOK AGAIN
011B 05                   DCR     B       ;B = ZERO?
                ;*********************************************
011C C21501               JNZ     SOFTM3  ;NO, REPEAT OUTER LOOP
                ;*********************************************
011F C9                   RET             ;YES, RETURN
                ;
                ;  STORAGE LOCATION FOR 24-BIT TIME DELAY WORD
0120              LODELA: DS      2       ;LOW ORDER 16 BITS
0122              HIDELA: DS      1       ;HIGH ORDER 8 BITS
```

simultaneously in different memory locations.

The calling sequence shown in the three lines following MAIN is part of the timing calculation and should not be modified. The SOFTIM subroutine modifies several registers, as indicated in the listing, so the prior contents of these registers should be saved if they will be needed later. Both branches of the timing loop contain exactly forty T-states, eliminating branch jitter and resulting in an execution time of 10 μs (microseconds) for a 4 MHz Z80. The CALL and RET (return) sequence is eighty T-states, exactly twice as long as the timing loop. This means that all setup error is eliminated by specifying the delay count as 2 less than the number of counts actually required.

SOFTIM can, of course, be modified to run on Intel's 8080 microprocessor, as well as on a Z80 (as shown in listing 2). The only essential changes involve the conversion of two relative jumps to absolute jumps. This has the effect of shortening both branches of the timer loop by two T-states, which requires further modification to the setup portion of the program.

By vectoring the first jump instruction to SOFTM3 rather than SOFTM2, a NOP (no operation) instruction is avoided during setup, and four T-states are eliminated. This restores a 2:1 balance between the setup sequence and the timer loop. (These changes are highlighted with asterisks in listing 2.) Shortening the 8080 version of SOFTIM yields a timing loop of thirty-eight T-states. This results in a somewhat ungainly loop execution time of 9.5 μs at 4 MHz (7.6 μs at 5 MHz), which makes time conversions unavoidably clumsy in this version of SOFTIM.

To the best of my knowledge, SOFTIM overcomes most of the serious drawbacks commonly associated with software-based timing functions. The major remaining disadvantage of this or any other software timer when compared to hardware is that it requires the microprocessor's complete attention while it is timing and prevents the computer from performing any other functions.

A few words of warning are in order at this point: SOFTIM was designed to be run at full speed. If it is burned into EPROM (erasable programmable read-only memory) or used from slow user-programmable memory, wait states can be introduced that affect its timing characteristics. In specific environments, you can probably compensate for this result as long as the wait states are introduced in a consistent manner. Finally, if your computer uses interrupt-driven or DMA (direct memory access) peripherals, be careful not to call SOFTIM while they are active, since timing errors will result if a DMA access or an interrupt service occurs while the timer is busy.

In spite of its shortcomings, SOFTIM provides an accurate and precise alternative to hardware timers—and at a much lower cost. In addition, it gives your microcomputer a chance to have the (software) time of its life. ■

What's New?

PUBLICATIONS

Information-Processing Industry Guide

Data Sources is a 1460-page guide to nearly 7000 software products and more than 6000 systems and peripherals. Product locators and cross-indexes help you find your way to company profiles of 1200 hardware manufacturers, 300 software companies, and 3900 service industries. A single issue of Data Sources costs $20. Charter subscriptions cost $60 per year for four issues. For details, contact Data Sources, 20 Brace Rd., Cherry Hill, NJ 08034, (609) 429-2100.
Circle 550 on inquiry card.

Columbia Products Catalog

Columbia Data Products has a free catalog featuring its data-communication-storage equipment, single- and multiuser distributed-processing systems, and custom-designed microcomputers. Contact Columbia Data Products, 8990 Rte. 108, Columbia, MD 21045, (301) 992-3400.
Circle 551 on inquiry card.

Intronics Catalog

Modules for analog-function computation, power supplies, data-display modules, operational and isolation amplifiers, and nonlinear-function modules are among the products described in a catalog from Intronics, 57 Chapel St., Newton, MA 02158, (617) 964-4000.
Circle 552 on inquiry card.

Computerist's Directory

The Community Computerist's Directory (CCD) is a semiannual national database in telephone-book format for computer users. The "White Pages" contain hundreds of noncommercial listings submitted by individuals and organizations wishing to share interests, information, skills, and resources, including hardware and software. Many list Source and Compuserve numbers.

CCD's "Yellow Pages" also have hundreds of entries, subdivided in 72 categories, including listings and display ads covering hardware, software, databases, consultants, systems houses, publications, and services. A glossary of computer terms, a bulletin board section, and clubs and newsletters listings are also included.

A one-year subscription to the CCD costs $10, which includes a free "White Page" listing, two issues, and quarterly updates. The Community Computerist's Directory is published by Alternet, Inc., POB 405, Forestville, CA 95436, (707) 887-1857.
Circle 553 on inquiry card.

How to Copyright Your Software

Sofprotex has released the report How to Copyright Computer Software. The report costs $20 and is available from Sofprotex, POB 271, Belmont, CA 94002.
Circle 554 on inquiry card.

Microcomputers and Farmers

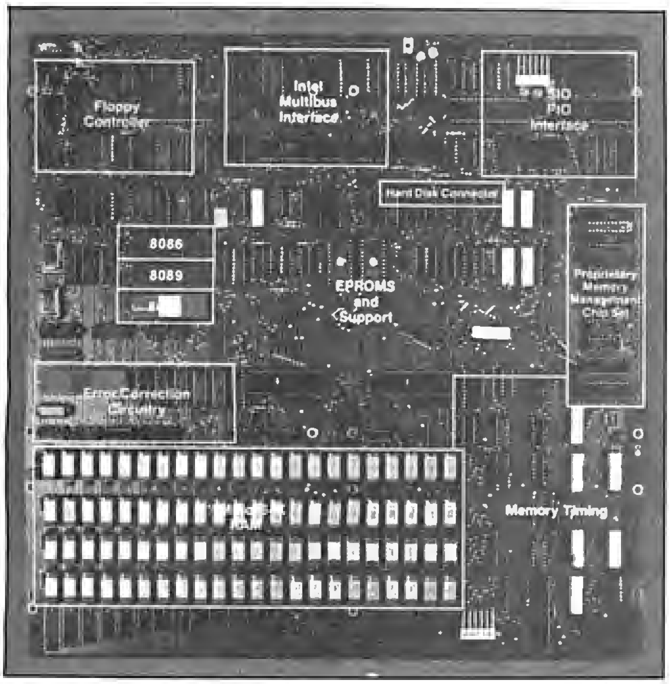
The Farm Computer News is filled with programming help, news of software and hardware, and reviews of computer products concerned with agriculture. The News is published monthly by Successful Farming Magazine, 1716 Locust, Des Moines, IA 50336. Subscriptions are $40 per year.
Circle 555 on inquiry card.

16-Bit Microprocessor Handbook

The 16-Bit Microprocessor Handbook examines the 8086, Z8000 series, 68000, 9900, LSI-11, and 16032 microprocessors. Software benchmarks that can be used for comparisons are provided, and hardware and software support available for the devices is discussed. Registers available, addressing capability, data types processible, clock speed, configurations, and instruction sets are covered. Pinouts, power-supply voltages, and system timing and operation are given. A simple example with I/O (input/output) ports is used to illustrate the interfacing process. Interrupts are covered and complementary circuits and devices are detailed. The 16-Bit Microprocessor Handbook costs $14.95, plus $1 for shipping and handling, and is available from Group Technology, Ltd., POB 87, Check, VA 24072, (703) 651-3153.
Circle 556 on inquiry card.

What's New?

SYSTEMS



16-Bit Microcomputers

The ACS8600 family of 16-bit microcomputers is based on the Intel 8086 microprocessor. The systems provide up to 1 million bytes of main memory, plus online floppy- and Winchester hard-disk storage from 1 to 80 megabytes. Up to 1 megabyte of memory can be addressed directly in blocks of 64 K bytes.

The ACS8600 family is organized around three processors: the 8086 for systems and applications control, the 8089 for DMA (direct-memory access) and I/O (input/output) processing, and the 8087 (optional) for floating-point arithmetic.

Up to eight terminals and peripherals can be supported. Expansion is possible through a Multibus port, and the systems accept both synchronous and asynchronous communications protocols. Data rates of up to 800 kbps (thousand bits per second) can be handled. The floppy-disk system can be upgraded to any of the hard-disk systems, and each hard-disk system can be upgraded to twice its original capacity.

The systems feature error detection and correction and a memory-management system. Each data word is accompanied by 6 bits of error-correction code, which allows the ACS8600 to perform 2-bit error detection and single-bit error detection and correction. Memory management is organized as 256 pages of 4 K bytes and provides both position independence and protection for the memory's contents.

Four operating systems are supported: Xenix, CP/M-86, MP/M-86, and Oasis-16. Languages supporting end-user applications are Microsoft's BASIC, Pascal, COBOL, and FORTRAN, as well as CIS-COBOL, Pascal/M-86, RM-COBOL, and C-BASIC-86.

The basic ACS8600 system has 512 K bytes of programmable memory, a 10-megabyte hard-disk drive and floppy-disk backup, and costs $12,990. Without the Winchester hard-disk backup, the same system, with dual floppy-disk storage of 1 megabyte and 128 K bytes of programmable memory, costs $8990. There are six hard-disk configuations available, and prices range from $12,990 to $18,980, which includes 40 megabytes of memory and magnetic-tape backup. For complete details on the ACS8600 microcomputer family, contact Altos Computer Systems, 2360 Bering Dr., San Jose, CA 95131, (408) 946-6700.

Circle 557 on inquiry card.

Z8000 Processor

Computex Microcomputer Systems' Multibus-compatible processor board features a 16-bit Z8001 microprocessor and sockets for two 2716 EPROMs (erasable programmable read-only memories). The board has eight vectored-interrupt levels plus a nonmaskable-interrupt input, two programmable timers, and a socket for a 9511 arithmetic processor. The board incorporates a memory-management circuit that divides memory into 2 K-byte pages, which are then mapped into addresses by the onboard circuitry. This allows a total system-wide memory of 16 megabytes. The 2 K-byte pages do not have to be contiguous in memory.

The Multibus-compatible board costs $998 and is available from Computex Microcomputer Systems, 5710 Drexel Ave., Chicago, IL 60637, (312) 684-3183.

Circle 558 on inquiry card.

Host of New Telesoft Products

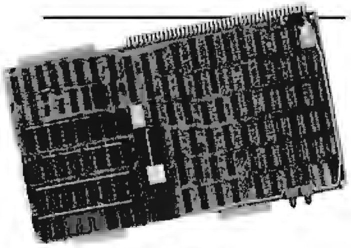
The portable Telesoft-Ada compiler is the key part of the Telesoft-PSE family, which includes a Telesoft-Pascal multitasking compiler, a multitasking operating system, a screen-oriented editor, a 68000 macroassembler, a 68000 native-code translator and object-code linker, and general-purpose utilities. The Ada compiler performs full Ada syntax checking and supports packages, tasks, exceptions, identifier overloading, and separate compilation (with limitations).

Another new Telesoft product is its fully integrated, desktop Workstation computer system. The Workstation features the new Telesoft T68KQ 68000 processor board, which can run on the DEC (Digital Equipment Corporation) Q-bus. The Workstation features an intelligent terminal, floppy-disk or Winchester-disk drives, 256 K bytes of programmable memory, and four serial ports. Telesoft-

PSE for the 68000 is available now and systems are being prepared for the 8086, VAX, and IBM 370 series.

The Telesoft-Ada compiler costs $2400, the screen-oriented editor is $125, the link editor is $275, the 68000 macroassembler and the native-code translator cost $400 each, and the Pascal compiler is available for $425. The T68KQ board is priced at $2995. The Telesoft-Workstation ranges between $10,000 and $20,000, depending on disk configuration. For details, contact Telesoft, 10639 Roselle St., San Diego, CA 92121, (714) 457-2700.

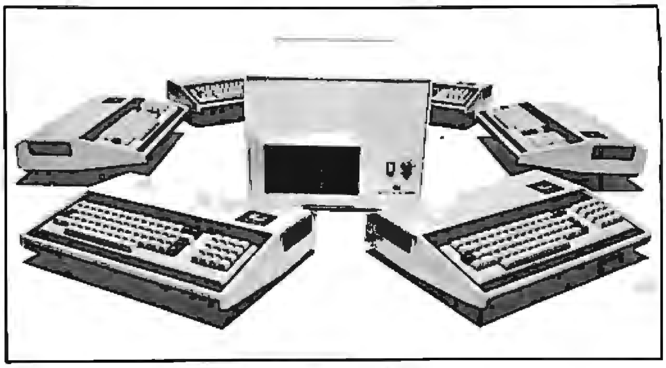
Circle 559 on inquiry card.



68000 Board

TSD Display Products' 68000-based processor board for the Multibus system has 256 K bytes of memory and the ability to work at 8 MHz with no wait states. Edge connectors for a logic analyzer are provided for easy debugging. Bus timeout protection, simple memory protection, and interrupt-type selection are also provided. The TSD Multibus-compatible 68000 board costs $3000 and is available from TSD Display Products, Inc., 35 Orville Dr., Bohemia, NY 11716, (516) 589-6800.

Circle 560 on inquiry card.



Sorcerers Net

The Multi-Net 80 network system consists of an Exidy Sorcerer microcomputer with peripherals that can transfer CP/M files and a timeshared global processor that can handle up to 16 Sorcerers with 64 K bytes of memory in each unit. Each Sorcerer is connected to a serial port on the user module and not through the system bus, which reduces bus contention and operator waiting time. The Multi-Net 80 Global Processor supports 8-inch IBM-compatible Winchester hard-disk drives and 8-inch floppy-disk drives, or cartridge tapes can be configured for backup.

Multi-Net 80 operating-system software consists of CP/NET, CP/NOS, and MP/M, which controls the global processor. The user operating system is CP/NOS, which looks to the user like CP/M 2.2. Network communications between user modules and the global module are under the control of CP/NET.

A single-user Multi-Net 80 system costs approximately $6000 and a 16-user system is about $34,100. Contact Exidy Systems, Inc., 1234 Elko Dr., Sunnyvale, CA 94086, (408) 734-9831.

Circle 561 on inquiry card.

Low-Cost Development Systems

The CDP18S693 1802 microprocessor-development system comes with a floating-point BASIC interpreter and system utility software. It includes a CMOS (complementary metal-oxide semiconductor) single-board computer, memory/cassette-controller board, a cassette-tape drive, a five-card chassis and case, and a 5 V DC power supply. The CDP18S693 costs $499.

The CDP18S694 has all the features of the CDP18S693 plus an 1802 assembler/editor PROM (programmable read-only memory) board and a second cassette drive. Both development systems can be memory expanded up to 64 K bytes and I/O (input/output) capacity can be increased. Further information can be obtained from RCA Solid State Div., POB 3200, Somerville, NJ 08876, (800) 526-3862; in New Jersey (201) 685-6423.

Circle 562 on inquiry card.

SOFTWARE

Supercalc for CP/M

Sorcim Corporation has announced the availability of its Supercalc program for the CP/M operating system. Both 5- and 8-inch drives are supported, including Apple CP/M, Xerox 820, North Star, Superbrain, Micropolis, Zenith, Osborne, and Vector Graphic. Supercalc features automatic formatting of printed reports and the ability to examine all formulas contained in a worksheet on an interactive basis. Other features include the ability to merge several sheets into one and an extensive help command that guides you through all the levels and options in the program.

The Supercalc program costs $295, which includes user guide and tutorial, reference card, and an installation program for use with more than 25 terminals. For details, contact Sorcim Corp., 405 Aldo Ave., Santa Clara, CA 95050, (408) 727-7634.

Circle 563 on inquiry card.

1981 Tax Planning Models

Pansophics 1981 Tax Planning Models incorporate the changes in the federal income tax laws governing the year 1981. The 1981 tax reduction has been incorporated into the tax planning models, along with the combined dividend and interest exclusion, automatic calculation of the 20% capital-gains maximum tax, and the new FICA and self-employment tax rates. Pansophics' tax models can print directly on IRS Form 1040 and your tax is calculated using either the tax tables or the tax-rate schedules automatically, whichever is appropriate.

The 1981 Tax Planning Models are fully supported and will run on 48 K- or 64 K-byte Apple IIs, running either DOS 3.2 or 3.3. There are two versions from which to choose: a personal model for $100 or a professional version for $150, which includes corporate and partnership tax-return models. For details, contact Pansophics, Ltd., Whistlestop Mall, POB 59, Rockport, MA 01966.

Circle 564 on inquiry card.

6800 Pascal Compiler

Technical Systems Consultants has released a 6809 native-code Pascal compiler for operation under 6809 Flex and Uniflex operating systems. The compiler produces 6809 assembly-language source mnemonics that are assembled into object code. The compiler supports integer and floating-point math with up to 16.8 digits of accuracy, scientific functions, variable names unique to 160 characters, sets of up to 128 elements, dynamic-storage allocation and deallocation, parameter passing from the command line to the Pascal program, and the ability to call other Pascal programs. The Uniflex version supports random-access files.

The compiler includes a manual, a copy of the **Pascal User Manual and Report** by Jensen and Wirth, the compiler and run-time object-code programs. The Flex version sells for $200 and a single-processor license for the Uniflex version costs $300. Both versions are provided with one year of maintenance. Contact Technical Systems Consultants, Inc., 1208 Kent Ave., POB 2570, West Lafayette, IN 47906, (317) 463-2502.

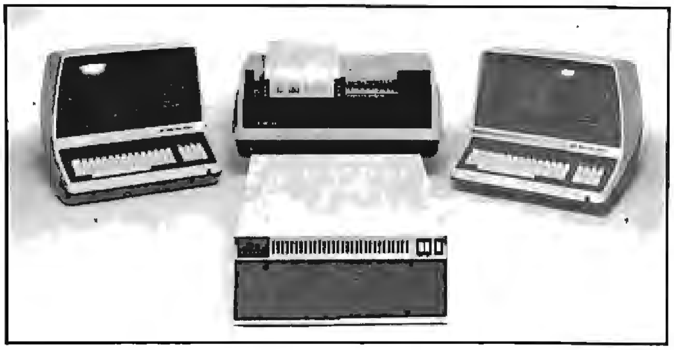
Circle 565 on inquiry card.

High-Quality Apple Graphics

The Graphics Printing System program for the Apple II prints high-resolution images on Diablo-formatted daisy-wheel printers and thimble printers, such as NEC (Nippon Electric Company) 5510s and 5620s, and is stingy with your printer's expensive ribbons. A typical chart or graph takes 3-4 minutes to output to the printer. Images can be selected from any rectangular area of the screen and printed in different sizes and formats.

The Graphics Printing System features an on-screen software device, called the Magicframe, that can output any object down to one pixel in size and surround it with a border. The Graphics Printing System program costs $109.95. Contact Progressive Software, Suite 323, Blue Bell West, Blue Bell, PA 19422, (215) 628-2383.

Circle 566 on inquiry card.



HiNet Networking Software

Digital Mirosystems' HiNet-2 networking software is designed for HiNet local computer networks. HiNet's 500-k-bits-per-second data cable can address up to 255 users. HiNet-2 allows the use of CP/M 2.2 software on the network. Another feature converts CP/M software for multi-user networking. SDLC (synchronous data-link control) protocols are standard with automatic error detection, correction, and resend. The networking software also features a print-spooling utility and a utility that provides single-sector tracks on floppy disk to back up hard disks. The transfer rate to the drives is 14 K bytes per second. For details on the HiNet-2 software, contact Digital Microsystems, 1840 Embarcadero, Oakland, CA 94606, (415) 532-3686.

Circle 567 on inquiry card.

Tax Help for TRS-80 Users

The Tax/Forecaster and Tax/Saver programs are designed to help TRS-80 users do their tax work. Tax/Saver features special screen formatting for data input, displaying to a video screen, two types of printout, and disk storage of data files. Tax/Saver compares all possible filing statuses, compares itemized deductions to national averages, computes certain limitations, checks for excess FICA, and helps determine dependents. The Tax/Forecaster turns the Tax/Saver into a tax forecaster. Both programs are tax deductible and run on TRS-80 Models I and III with 32 K bytes of memory and two disk drives. Including a user manual, Tax/Saver I costs $79.95, Tax/Saver II (an enhanced version) is $119.95, and Tax/Forecaster is $29.95. The manual is available separately for $19.95. For details, contact Micromatic Programming Co., POB 158, Georgetown, CT 06829, (203) 544-8777.

Circle 568 on inquiry card.

BASEX Compiler for the Heath H-8

The BASEX language combines the features of BASIC with executable machine-language code. BASEX programs typically run up to 10 times faster than similar BASIC programs. BASEX compiler and loader programs on cassette for Heath H-8 microcomputers are now available from Interactive Microware. This enhanced revision of BASEX includes a console driver, commands to save and load programs on tape, and a manual, which has listings of the compiler and execution routines. The manual, a Heath H-8 addendum, and cassette are offered for $33. The BASEX manual can be purchased separately for $8 from BYTE Books, 70 Main St., Peterborough, NH 03458, (800) 258-5420; in New Hampshire (603) 924-9281.

BASEX cassettes are also offered for TRS-80 Level II, Sorcerer, Sol, and Poly-88 systems, and disk versions are available for 5-inch North Star and 8-inch single-density CP/M systems. For additional information, contact Interactive Microware Inc., POB 771, State College, PA 16801, (814) 238-8294.
Circle 569 on inquiry card.

Convert Apple to Apple

The Super Apple Textwriter allows you to convert a file generated by Applewriter, Supertext, and Superscribe word processors into a file accessible by the other two. It can convert standard text files into files accessible by either Supertext or Applewriter and it converts Applewriter or Supertext files into standard text files. It lets you edit information obtained from a communications network as well as transmit files through a modem. It is possible to develop and edit a BASIC program using a word processor and then use Super Apple Textwriter to convert the file into a text file that can be executed into memory. Super Apple Textwriter retails for $49.95 and is available from Mint Software, 6422 Peggy St., Baton Rouge, LA 70808, (504) 766-2318.
Circle 570 on inquiry card.

Overlay Linker

The Overlay Linker can link files produced by Cromemco's Macro Assembler and by the FORTRAN, C, and COBOL compilers to produce executable object files. The Linker permits the construction and execution of programs that are too large to fit into available memory. Any standard Cromemco relocatable file that does not include absolute loading can be loaded by the Linker. It can also manage an arbitrary number of common blocks and create an arbitrary number of overlays, each in a separate file on disk. Commands can be given to the Linker as a part of the command line. A relocatable library-file manager is also included.

The Overlay Linker operates under CDOS or Cromix operating systems. It's available on 5- or 8-inch disks for $395. For additional information, contact Cromemco, Inc., 280 Bernardo Ave., Mountain View, CA 94043, (415) 964-7400.
Circle 571 on inquiry card.

TRS-80 BASIC Compiler

RSBASIC is a business-oriented BASIC compiler for the TRS-80 Models I and III that compiles programs and allows interactive debugging in a run mode prior to compilation. Among its features are sequential, random, and single-key ISAM (indexed sequential-access method) file access; direct calls to machine-language programs; program-chaining capabilities with common variable storage; numeric accuracy to 14 digits; step and trace debugging; printer and disk utilities; strings, arithmetic, trigonometric, and bit operations; and conversions between data types.

RSBASIC is equipped with BEDIT, an editor for source programs, and RUNBASIC, which executes compiled programs. RSBASIC will not convert programs written for BASIC interpreters. RSBASIC requires a TRS-80 Model I or III, 48 K bytes of memory, and two floppy-disk drives. It is available for $149 from Radio Shack, 1800 One Tandy Center, Fort Worth, TX 76102, (817) 390-3272.
Circle 572 on inquiry card.

Supervyz Your CP/M

Supervyz allows nontechnical users an easier way of dealing with CP/M. Communication with CP/M for many users has been abbreviated, impolite, and not helpful when a mistake is made. The symbols can be cryptic and frustrating for many users. Aided by error mesages and computer-assisted tutoring, Supervyz helps the operator avoid mistakes and advises the next step in a polite manner. It serves as a mediator between the user and CP/M, requesting information in plain English and translating the response into a form CP/M understands.

Supervyz is an enhanced CP/M with a number of new intrinsic (built-in) commands, such as GET, which loads a program, GO, which executes the loaded program, and WAIT, which requests keyboard input before proceeding with the program. Supervyz costs $95 and is manufactured by Epic Computer Corp., 9181 Chesapeake Dr., San Diego, CA 92123, (714) 569-0440.
Circle 573 on inquiry card.

Spellguard 2.0

Spellguard 2.0 proofreads text 1.5 times faster than its predecessor, Spellguard 1.0, and occupies ⅓ less space (54 K bytes). It can proofread up to 60 double-spaced pages (15,000 words) per minute, using double-density 8-inch disk drives. Deletions from and additions to the Spellguard's 20,000-word dictionary present no problem.

Spellguard 2.0 is available on 5- or 8-inch disks for the Apple and other microcomputers with 32 K bytes of memory, one disk drive, and the CP/M operating system. It costs $295. For $35, owners of Spellguard 1.0 can upgrade to version 2.0 by returning

their disk to the company. Contact Innovative Software Applications, Suite 300, 260 Sheridan Ave., Palo Alto, CA 94306, (415) 326-0805.
Circle 574 on inquiry card.

Crank Up UCSD Pascal

Using Professional Business Software's Crank utility, you can convert CP/M BIOS to UCSD Pascal BIOS, which will allow UCSD Pascal to run on any 48 K-byte computer that runs CP/M. The Crank works with floppy- and hard-disk drive systems. A UCSD p-system for CP/M-based machines is available for $450. Run-time-only systems are available for $150 from Professional Business Software, 119 Fremont St., San Francisco, CA 94105, (415) 546-1596.
Circle 575 on inquiry card.

MISCELLANEOUS

RS-232C Cable Designer

The RS-232C DB25 Pin Reconfiguration Adapter (PRA) lets you mate almost any serial I/O (input/output) device to any computer by rerouting RS-232C signals. The PRA eliminates the task of making special cables or resoldering existing cable wiring to achieve proper interfaces. A flat cable with DB25 connectors and the PRA adapter will tie proper signal lines together. All you do is position the slide switches for proper signal routing through the adapter.

The PRA package is made up of a printed-circuit card with one male and one female DB25 connector mounted on it and a matrix switch. It has a suggested retail price of $59.95 and is available from Mountain Computer, Inc., 300 El Pueblo Rd., Scotts Valley, CA 95066, (408) 436-6650.
Circle 576 on inquiry card.

68000 Memory-Management Unit

The MC68451 memory-management unit provides address translation and protection of the 16-megabyte addressing space of the 16-bit 68000 processor. It also provides address-space separation of system user resources and write-protection. The MC68451 costs $215 and is available from Motorola, Inc., MOS Integrated Circuits Div., 3501 Ed Bluestein Blvd., Austin, TX 78721, (512) 928-6369.
Circle 579 on inquiry card.

Lowercase for the Apple II

The McLaren LCG (lowercase generator) for the Apple II generates the full 96-character ASCII (American Standard Code for Information Interchange) set with true descenders. Installation is simple and requires no soldering. The McLaren LCG costs $49.95 and is distributed by Great Lakes Digital Resources, POB 32133, Detroit, MI 48232, (313) 538-7963.
Circle 580 on inquiry card.

Tiny Core Memory

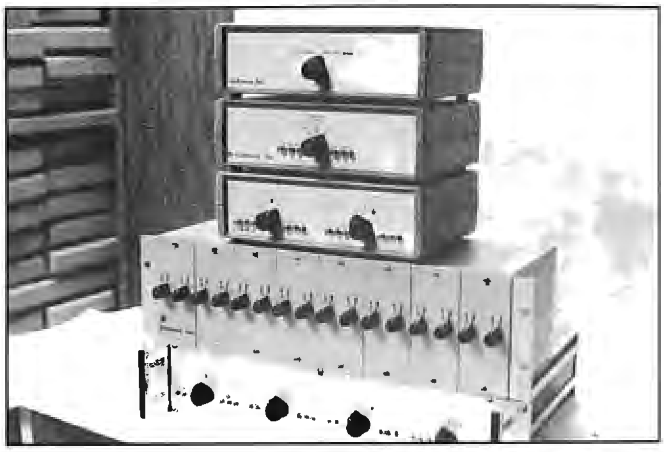
The Controlex Model 120 is a tiny core-memory module for use as a nonvolatile store of microprocessor data. Its 4-bit array can store a status word upon power shutdown or loss and retain it indefinitely. In a typical application, the 120 would be accessed by a microprocessor I/O (input/output) port in response to power shutdown. Data are squentially loaded in four cycles and retained. When power is returned, the data are sequentially loaded back to return to the status word.

The Model 120 comes in a 14-pin DIP (dual inline package). Variations, including longer word lengths (i.e., 8 bits), parallel access, and custom-support circuitry are available. The Model 120 operates on +5 V and uses low-cost, common TTL (transistor-transistor logic) devices as support circuits. It costs $6.90 in OEM (original equipment manufacturer) quantities. Contact Controlex Corp., 16005 Sherman Way, Van Nuys, CA 91406, (213) 780-8877.
Circle 581 on inquiry card.

Convert Signals

The Mint-01 interface board converts TTL (transistor-transistor logic) levels to RS-232C or 20 mA current-loop signals in a 5 V DC environment. The board will convert TTL voltages to a single 20 mA current-loop input and output, or to RS-232C inputs and four RS-232C outputs, selectable with on-board jumpers. A DC-to-DC converter provides ±12 V DC for the conversion circuitry, while requiring a +5 V DC input at 400 mA. The Mint-01 can be attached to any TTL-level logic through a 14-pin cable connector. The price is $105 from Miller Technology, 647 North Santa Cruz Ave., Los Gatos, CA 95030, (408) 395-2032.
Circle 582 on inquiry card.

What's New?

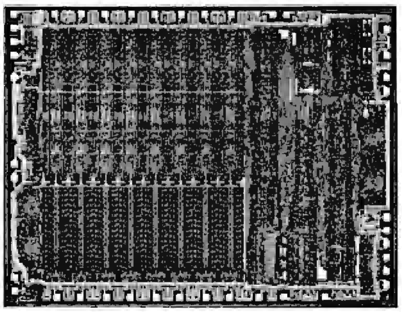


Share Up to Six Peripherals

Giltronix Inc.'s position-switching and port-sharing units allow several computers to share a common device, such as a printer or terminal, or allow a single computer to use several devices from one microprocessor port. The Models GRS 232-S8AD, -S8AE, and -S8AF switching units have four, five, and six positions and can connect up to six devices to a common I/O (input/output) device. All units can switch eight lines of an RS-232C interface.

Options for the series include monitoring capabilities and a rack-mountable enclosure. Prices are $249, $299, and $339, respectively. For more information, contact Giltronix, Inc., 450 San Antonio Ave., Palo Alto, CA 94306, (415) 493-1300.

Circle 583 on inquiry card.



Fast CMOS Microprocessor

The CDP1802A CMOS (complementary metal-oxide semiconductor) microprocessor offers a clock frequency of 3.2 MHz at 5 V DC and 6.4 MHz at 10 V DC, guaranteed over a range of -40°C to +85°C. It also features an internal Schmitt-trigger buffer on the $\overline{\text{CLEAR}}$ input, which eliminates the need for external logic devices for power-on reset.

The CDP1802A is pin-for-pin compatible with the CDP1802 and is priced at $3.98 in OEM (original equipment manufacturer) quantities. Contact RCA Solid State Div., Rte. 202, Box 3200, Somerville, NJ 08876.

Circle 584 on inquiry card.

The Speaker's Voice

The Speaker is a voice synthesizer for SS-50, SS-50C, and TRS-80 Color Computers. Typically, 1 or 2 bytes are required to represent the phonetic-speech codes. The board can be used from any BASIC by using PEEK and POKE commands. Data statements are used for speech storage. The Speaker for the SS-50/50C costs $189.95. It's available with demonstration software for Technical Systems Consultants and Smoke Signal Broadcasting disk operating systems. The TRS-80 Color Computer version comes with demonstration and utility programs operating in machine language and Color BASIC. It costs $179.95. For more information, contact Alford & Associates, POB 6745, Richmond, VA 25250, (804) 320-6722.

Circle 585 on inquiry card.

Digital Timer Circuit

Slow operate and release, intervals, and flashings from 6 microseconds to infinity can be programmed with the LS7210 digital-timer circuit. The device can be driven by an on-circuit oscillator set by an external remote-control network, or by an external clock. Delays of 36 days are obtainable. Circuits can be cascaded for sequential events. The LS7210 can be operated in four modes: delayed operate, delayed release, dual delay, and one-shot modes. All inputs on the device are CMOS- (complementary metal-oxide semiconductor), PMOS- (p-type MOS), and TTL- (transistor-transistor logic) compatible. The cost is $3.70 in 1- to 24-unit quantities. Contact LSI Computer Systems, Inc., 1235 Walt Whitman Rd., Melville, NY 11747, (516) 271-0400.

Circle 586 on inquiry card.

Boost the Atari 800's Memory

The RAMdisk is a 128 K-byte programmable memory system for the Atari 800. RAMdisk has software that makes the system appear to the computer to be a disk drive. RAMdisk is compatible with existing software written for the Atari 800 and is up to 20 times faster than the Atari 810. RAMdisk can also be programmed as bank-selectable memory in eight 16 K-byte pages. No modifications to the 800 are required.

The complete RAMdisk memory system includes the 128 K module, operating manual, DOS (disk operating system) memory-management software, and utility software. The suggested retail price is $699 from Axlon, Inc., 170 North Wolfe Rd., Sunnyvale, CA 94086, (408) 730-0216.

Circle 587 on inquiry card.

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Odyssey	$29.95 now	$25.39
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MISCELLANEOUS

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Space Quark	$29.95 now	$25.39
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U.S. Constitution	$29.95 now	$25.39
Merger	$49.95 now	$42.49
Super Stellar Trek	$39.95 now	$33.89
LISA	$79.95 now	$67.89
V-Plot (Yuccipa)	$29.95 now	$25.39
V-Stat	$29.95 now	$25.39
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Info Master	$150.00 now	$127.49
Waterloo II	$49.95 now	$42.39
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Softlights

By Fred Huntington

More and more fantastic things are becoming available for the Apple®. We just received one of my favorites – the **Passport Designs SOUNDCHASER Computer Music System.** It's easy to set up and an absolute blast to play with.

Price is $650 for the keyboard and $350 for each synthesizer board.

We recommend two boards. When you buy the complete system, we will give you $100 worth of free software (your choice from our current catalog).

Having worked my way through college playing in a small band, I keep thinking how great my group would have sounded if we had had the Passport Designs setup.

You can actually record a song and then play it back and even play along with it – no tapes or accessing the disk. You have to see it (and hear it) to believe it. Five stars!

HARD DISK

We're now official dealers for Nestar. We think the Nestar system is so great, we've adopted it for in-house use. We have four Apples hooked up to a 16 Megabyte disk. This allows us to have several people processing orders at the same time, all working off the same inventory disk.

Our system has the capability of expanding to 64 Apples hooked up together.

And, by the time you read this, CP/M® (a registered trade mark of Digital Research) should be available for the system.

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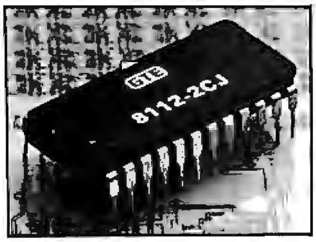


New Circuits from GTE

The 8112 static programmable-memory integrated circuit is pin-for-pin-compatible with the 2716 EPROM (erasable programmable read-only memory). A delatched write function allows data to be controlled by the write-enable function, making a delayed write possible. The 8112 operates in the enabled and the disabled modes. In the enabled mode, the device typically uses 135 mW of power and in the disabled mode it uses 30 mW. Organized as a 1 K by 8-bit circuit, the 8112 is available in 200, 300, and 400 ns versions. It requires a single +5 V DC power supply. Depending on speed, the 8112's price ranges from $10.10 to $13.05. Contact GTE Microcircuits, 2000 West 14th St., Tempe, AZ 85281, (602) 968-4431.

Circle 588 on inquiry card.

5 V DC, 10 A Switching Power Supply

Suitable for 90 V to 135 V AC or 180 V to 270 V AC, the Model USB 5-10, a 5 V DC 10 A open-frame switching power supply, can handle a line frequency of between 47 and 440 Hz. Efficiency is more than 72% at full load, 115 or 230 V AC and 25°C. The supply can compensate for up to 0.5 V line drop and has crowbar overvoltage protection. The price for the USB 5-10 switching supply is $99. Contact Adtech Power, Inc., 1621 South Sinclair, Anaheim, CA 92806, (714) 634-9211.

Circle 589 on inquiry card.

BitSwitch

BitSwitch is a manually activated device that allows one of two RS-232C interfaces to be switched to a common port. With BitSwitch, printers, modems, and terminals can be shared. The Model 117 BitSwitch can be placed under modems or telephones and is priced at $124 from Development Associates, 1520 South Lyon St., Santa Ana, CA 92705, (714) 835-9512.

Circle 590 on inquiry card.

TRS-80 Control Keys

Clockwork Software's Control Key system is a hardware and software combination that lets you control your TRS-80 Model I's 32 K- or 48 K-byte floppy-disk system with single keystrokes. The hardware converts the TRS-80's numeric keypad into a set of 12 programmable-function keys accessible by BASIC or machine-language commands.

Four Control Key programs are available: Doskey, Baskey Scripkey, and Numkey. Doskey allows execution of the most frequently used DOS (disk operating system) functions with a single key. Baskey aids the entering and debugging of BASIC programs by configuring the keypad to accommodate BASIC commands. Scripkey works in conjunction with the Scripsit word-processing program and allows 24 Scripsit commands to be entered with single keystrokes. Numkey converts the Control Key hardware back into a numeric pad for data entry. A total of 24 functions/commands are available from the Control Key keyboard during the execution of each Control Key program.

The Control Key hardware costs $150 assembled, $70 partially assembled, or $20 for the bare board, including documentation. Doskey and Numkey come with the assembled and partially assembled versions. Baskey and Scripkey cost $20 each. For details, contact Clockwork Software, POB 704, Colorado Springs, CO 80901.

Circle 591 on inquiry card.

RS-232C Cable Assemblies

Belden Corp.'s shielded interface-cable assemblies comply with the EIA's (Electronics Industries Association's) RS-232C standards. Belden's molded cable assemblies feature a 25-conductor shielded cable with subminiature male or female D connectors. This design protects signals from external interference. Connector pins and sockets feature gold over copper-flashed beryllium copper. Prices range from $21.06 for a 5-foot length to $56.82 for a 70-foot piece. Contact Joe Prechodnik, Belden Corp., Interconnect Systems Operation, 105 Wolfpack Rd., Gastonia, NC 28052, (704) 865-4513.

Circle 592 on inquiry card.

Voltage Suppressor

The Voltage Surge and Transient Suppressor electronically removes or reduces sudden voltage changes that can affect electronic equipment. The Suppressor is plugged into an AC-line power receptacle on the same 15 A breaker circuit as the electronic equipment being protected. Overvoltage surges beyond 132 V AC are clipped and high-frequency transients are cut off. A 2 A internal fuse provides overload protection. A power indicator lets you know whether your AC-input voltages are normal or poor. For information on the suppressor, contact Cuesta Systems, Inc., 3440 Roberto Court, San Luis Obispo, CA 93401, (805) 541-4160.
Circle 593 on inquiry card.

North Star-Compatible Disk Controller

The Phase Lock II North Star-compatible disk controller can handle double- and quad-density floppy-disk drives. The Phase Lock II runs programs made for the North Star controller and supports four extra disk drives. The controller is capable of supporting a mixed configuration of 48- and 96-track-per-inch drives.

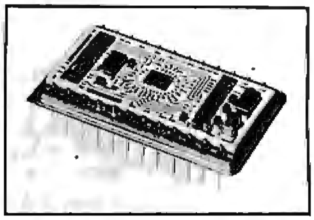
Optionally, the Phase Lock II can allow boot-up at a user-selectable address. Available with the selectable-address option is Super DOS-96 & Boot PROM (programmable read-only memory), which automatically tracks the controller-board address and continues to function at different addresses. The Super DOS-96 & Boot PROM permits users to boot up on a drive other than number 1. Additionally, Super DOS-96 does not require a GO command: the user merely types in the file name followed by a RETURN and Super DOS-96 will automatically load and execute a file. A file program provided on a disk lets users merge files from a single- or double-density disk to another single- or double-density disk.

The Phase Lock II costs $450 or $500 with the multi-address option. Contact HSC Computer Services, Ltd., POB 43, Brooklyn, NY 11236, (212) 780-0022.
Circle 594 on inquiry card.

Controller for 5-Inch Seagate Drives

Xebec Corporation's S1410 controller is designed specifically for Seagate 5-inch-compatible drives. The S1410 is compatible with DTC (Data Technolgy Corp.) 510 and SA1400 interfaces, which allows the controller to operate with host adapters supplied by DTC and Shugart, such as those for the Apple, Q-Bus, Multibus, and S-100 computers. The microprocessor-controlled S1410 combines an onboard data separator with a Shugart Associates SA1400 series host interface. It can handle two drives simultaneously and it features a control that can configure the size of the drive through software commands. The S1410's power requirements are +5 V at 2.5 A and +12 V at 50 mA.

Other features include automatic seek and verify, automatic head and cylinder switching, a full-sector buffer, variable-sector size, automatic retries, and user-programmable drive characteristics. The host system initializes the drive size by sending the controller the maximum number of cylinders and heads. The S1410 controller costs $295. Contact Xebec Corp., 432 Lakeside Dr., Sunnyvale, CA 94086, (408) 733-1340.
Circle 595 on inquiry card.



12-Bit 35 ns D/A Converter

Designed as a pin-for-pin replacement for the earlier ADH-030, the ADH-030 II D/A (digital-to-analog) converter provides 12-bit linearity, settling in 35 ns to within 0.01%. The device is useful for applications in video displays, including television and radar video reconstruction, x-y deflection positioning, and digitally controlled frequency agile oscillators. The ADH-030 II comes in two temperature grades: 0° to 70°C and -55° to +105°C. Prices begin at $139, for single pieces. For more information, contact ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716, (516) 567-5600.
Circle 596 on inquiry card.

Dot-Matrix Printers

Printek's Models 910 and 920 dot-matrix printers share many features: a 9 by 9 format, graphics density of 144 by 144 dots per inch, and a 96-character ASCII (American Standard Code for Information Interchange) set with optional

fonts, underlining, super- and subscript, lowercase descenders, double-width characters, and downloadable character set. Both printers have a 1.8 K-byte character buffer. The Models 910 and 920 differ only in their bidirectional print speed and throughput. The 910 can print up to 170 cps (characters per second); the 920 up to 340 cps. The Model 910 has a maximum throughput of 140 lpm (lines per minute); the 920 can do 270 lpm. In graphics, the 910 prints 2000 dots per second, while the 920 prints 4000 dots per second.

The Model 910 has a suggested list price of approximately $1695; the Model 920 is $2345. Complete details are available from Printek, Inc., 1517 Townline Rd., Benton Harbor, MI 49022, (616) 925-3200.

Circle 597 on inquiry card.

Alps Printers

Using a special ballpoint pen, the Alps Electric Model 1200 color printer prints four-color graphic symbols, letters, numbers, Chinese ideograms, and drawings and graphs. During color printing, the printer selects the appropriate pen through software routines. Another printer, the Model 1100, uses a single pen and can write 12 cps (characters per second) in its smallest column size.

Alps printers are available as stand-alone units or as the printing mechanism alone. The price for the one-color printer is $325, the mechanism alone is $140. The four-color Model 1200 is $450; the mechanism alone is $180. For details, contact Alps Electric, Inc., 100 North Centre Ave., Rockville Centre, NY 11570, (516) 766-3636.

Circle 598 on inquiry card.

Desktop Digitizer

Summagraphics Corporation has introduced a new version of its Bit Pad digitizer: the Bit Pad 10. The device is useful for cursor control, business-data entry, and graphics-information entry. RS-232C, IEEE (Institute of Electrical and Electronics Engineers), and 8-bit parallel interfaces are available for the 11-inch square digitizer

The Bit Pad 10 costs between $895 and $990, depending upon accessories. For complete details, contact Summagraphics Corp., 35 Brentwood Ave., Fairfield, CT 06430, (203) 384-1344.

Circle 599 on inquiry card.

Tabletop Drum Plotter

Houston Instrument's CPS-16, a four-pen, tabletop drum plotter, is microprocessor-based. The CPS-16 can produce four-color drawings on paper, mylar, or vellum. It accepts data from RS-232C or 20 mA current-loop sources and can operate in an on-line or remote time-share environment. It features up to 172 characters containing upper- and lowercase letters, positive paper feed, buffer memory, and protocol for detection and correction of data-transmission errors. Writing speeds of 10 or 15 inches per second with a 0.05 mm (0.002 inches) resolution are touch-selectable. For additional information, contact Houston Instrument, One Houston Sq., Austin, TX 78753, (512) 837-2820.

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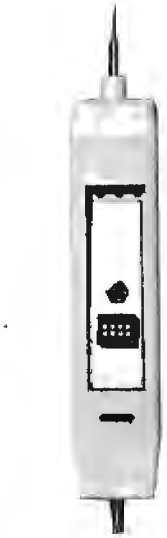

Smart Logic Probe

The SP-1 Smart Probe is a logic probe with four address lines that can connect to TTL- (transistor-transistor logic) level circuitry. When the logic levels of the address lines match the parameters that the user has set into the switches, the TTL-logic level present at the probe tip is latched and displayed on an LED (light-emitting diode). This gives the user the ability to latch and display the logic level of a circuit at any specific instant. The SP-1 costs $55 and is available from New Technologies Co., POB 32, Streamwood, IL 60103, (312) 289-4410.

Circle 601 on inquiry card.

Auto-Cat

The Auto-Cat is an auto answer, FCC- (Federal Communications Commission) approved, direct-connect 300-bit-per-second modem that can automatically answer calls at any time. Auto-Cat has three data modes: automatic answer, manual answer, and manual originate. It can operate in full- or half-duplex and features local and remote loopback test functions. The interface is RS-232C.

The Auto-Cat costs $249. For complete details, contact Novation, Inc., 18664 Oxnard St., Tarzana, CA 91356, (213) 996-5060.

Circle 602 on inquiry card.

Where Do New Products Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. The information is printed more or less as a first-in first-out queue, subject to occasional priority modifications. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

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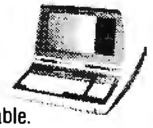

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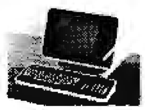

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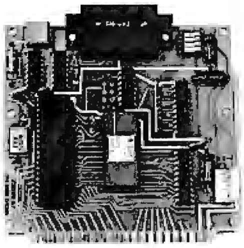

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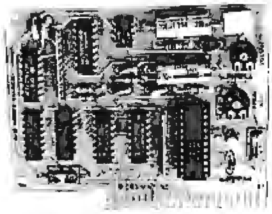

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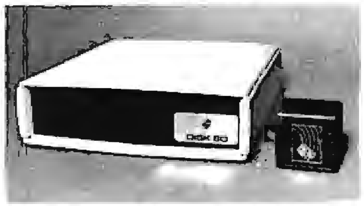

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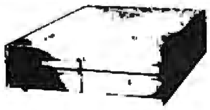

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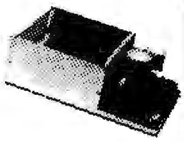

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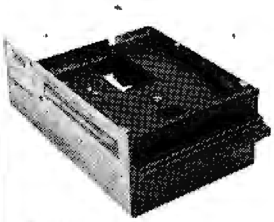

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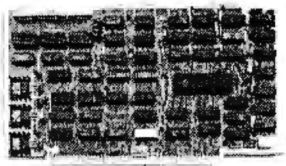

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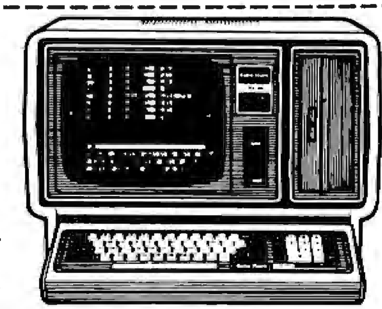

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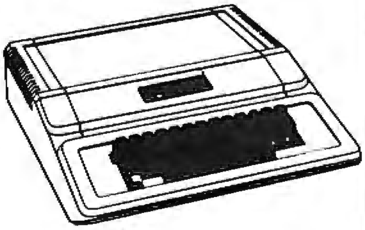

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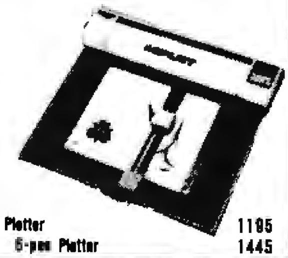

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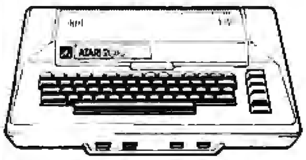

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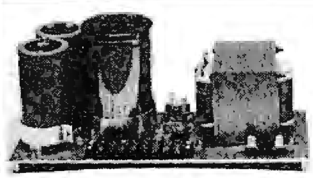

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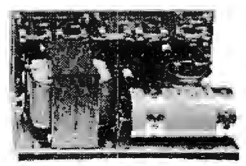

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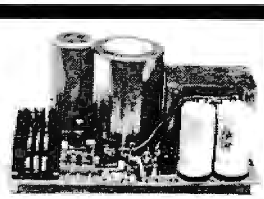

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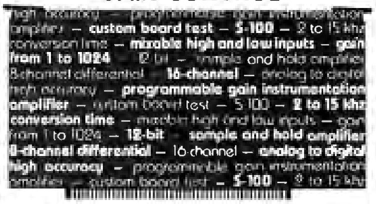

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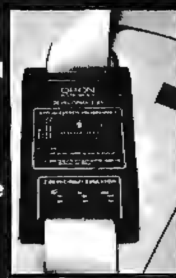

Only $329 including personality module for 2716, 2516, 2758, 2508, 2532, 2816, 2808, 48016.

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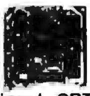
CRT CONTROLLER



This intelligent CRT Controller uses an 8085A CPU & an 8275 Integrated CRT Controller. It features:

- 25 lines (80 char./line)
- 5x7 dot matrix
- Upper & lowercase
- Two 2716's (controller & char. generator)
- Serial interface RS232 & TTL
- Baud rates of 110, 150, 300, 600, 1200, 2400, 4800 and 9600
- Keyboard scanning system
- Unencoded keyboard required
- Uses +5V & ± 12V Power Supplies
- Does not have graphic capabilities.

Documentation includes program listing and composite video circuit.

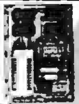
Bare Board only (with doc)	$39.95
2716 Char. Gen. A7	$19.95
2716 Program A 12	$19.95

A-D CONVERTER

JBEs 16 channel A-D Converter plugs into your Apple II computer. It uses an ADC0817 which incorporates a 16 channel multiplexer and an 8 bit A-D Converter. The 16 inputs are high impedance and the voltage range is 0 to 5.12 volts. Conversion time is <100 μsec. The resolution is 8 bits or 256 steps, linearity is ± 1/2 step. Two 16 pin DIP sockets are used for input, GND & reference voltage connections. There are 3 single bit TTL inputs. Doc. includes sample program.

81-132A Assm.	$89.95
81-132K Kit	$69.95
81-132B Bare Board	$29.95

EPROM PROGRAMMER



JBE's EPROM Programmer is designed to program 5V 2516's, 2532's & 2716's. It interfaces to the JBE Parallel I/O card using four ribbon cables. An LED indicates when the EPROM is being programmed. A textool zero insertion force socket is used for the EPROM. Comes with complete documentation for writing and reading EPROM's in the Apple II or Apple II Plus. Cables available separately.

80-244A Assm.	$49.95
80-244K Kit	$39.95
80-244B Bare Board	$24.95

PARTS

6502 MPU	$9.95
6522 VIA	$9.95
Z-80 MPU	$9.95
Z-80 PIO	$9.95
TWO 2114 RAM	$9.95
2716	$14.95
50 pin conn.	$5.95
Dip Jumper 2 ft.	$4.95

6522 APPLE II INTERFACE

The JBE 6522 Parallel Interface for the Apple II Computer, plugs directly into any slot 1 through 7 in the Apple. This card has 2 6522 VIA's that provide:

- Four 8 bit bi-directional I/O ports
- Four 16 bit programmable timer/counters
- Serial shift registers
- Handshaking

A 74LS05 is for timing. Four 16 pin sockets provide easy connections to other peripheral devices. (Dip jumpers with ribbon cable are also available from JBE) The 6522 Parallel I/O card interfaces to the JBE EPROM programmer. Understanding of machine language required to use this board. Inputs and outputs are TTL compatible.

79-295A	$69.95 Assembled
79-295K	$59.95 Kit
79-295B	$19.95 Bareboard

SPEECH SYNTHESIZERS

JBEs Speech Synthesizers use the Votrax SC-01 Phoneme Synthesizer chip. The SC-01 phonetically synthesizes continuous speech of unlimited vocabulary. The SC-01 contains 64 different phonemes and 4 levels of inflection accessed by an 8 bit code. It requires 10 Bytes per second for continuous speech. Both boards have an audio amp for direct connection to an 8 ohm speaker.

Documentation includes basic user programs, a phoneme chart and listing of coded words to help you get started. Documentation for the Apple II® Speech Synthesizer includes a disk with many user programs.

81-088 Apple II Speech Synthesizer	$139.95
81-120 Parallel input Speech Synthesizer	$149.95

Prices include the SC-01 Chip
SC-01 sold separately for $ 75.95

EPROM EXPANSION CARD

JBE EPROM Expander for the Apple II holds six 5V 2716s for a total of 12K bytes of EPROM. This board takes the place of the on board ROM in the Apple. It is software switchable by the same technique used by the Apple II firmware card. Solder jumpers are for reset to the Apple ROM or EPROM Expansion Card. Use JBE EPROM Programmer and Parallel I/O to program your EPROMs. EPROMs sold separately.

81-085A Assm.	$59.95
81-085K Kit	$49.95
81-085B Bare Board	$39.95

81-260 "SLIM"

Single board large scale Integration Microcomputer. This 4.5 x 6.5 board uses the 6502 Microprocessor, two 6522 VIA's, four 2114 RAM's, 2516, 2716 or 2532 EPROM. The fully buffered 22/44 pin bus is similar to the KIM®, SYM®, and AIM® expansion connector. The four 8 bit I/O ports connect through 16 pin dip sockets. This board was designed for control and is ideal for Personal and OEM use.

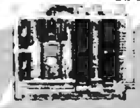
- 6502 MPU
- Two 6522 VIA's
- Four 2114 RAM's (2K bytes)
- One EPROM 2516 or 2532
- Crystal clock 1 Mhz
- Requires 5V 1AMP Power
- 4.5 x 6.5 card
- Power on reset
- Fully buffered-expandable
- Solder mask-both sides

Use your Apple II Computer, JBE 6522 Parallel Interface card and EPROM Programmer as a development system for SLIM.

Prices:

81-260A	$199.95 Assembled
81-260K	$149.95 Kit
81-260B	$ 39.95 Bare Board

6502 MICROCOMPUTER



6502 MPU, 6522 VIA, 2716 EPROM, 2114 RAM single board computer. Single 5 volt power supply at 400 Ma. Two independent 8 bit I/O ports with handshake lines. RC controlled 1 Mhz clock.

Complete documentation. I/O lines use 50 pin edge connector. Data and address lines are not accessible. Mod. for 2532 is included. EPROM is not included. 1K RAM, 2K EPROM, 2 I/O ports.

80-153 Assm.	$110.95
80-153 Kit	$ 89.95
80-153 Bare Board	$ 19.95

Z-80 MICROCOMUTER

Z-80 MPU, Z-80 PIO, 2716 EPROM, 2114 RAM single board computer. Single 5 volt power supply at 300 Ma. Two independent 8 bit I/O ports with handshake lines. RC controlled 2Mhz clock.

Complete documentation. I/O lines use 50 pin edge connector. Data and address lines are not accessible. Mod. for 2532 is included. EPROM is not included. 1K RAM, 2K EPROM, 2 I/O ports.

80-280 Assm.	$129.95
80-280 Kit	$119.95
80-280 Bare Board	$ 19.95

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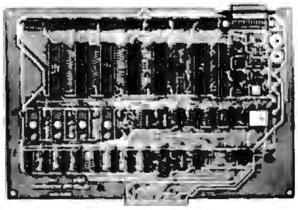

JBE's 7.75 x 11.75 6502 base Microcomputer has the capacity for 16K of EPROM, 4K of RAM, 8 Parallel Ports and 1 Serial Port. Monitor and Tiny Basic are also available. The fully populated version includes:

- 1 6502 CPU
- 4 6522 VIA (8 Parallel I/O Ports)
- 1 AY5-1013 (Serial I/O Ports)
- 8 2114 RAM (4K)
- 2 2716 EPROM (Monitor & Tiny Basic)

The partially populated version includes:

- 1 6502 CPU
- 1 6522 VIA (2 Parallel I/O Ports)
- 1 AY5-1013 (Serial I/O Port)
- 2 2114 RAM (1K)
- 1 2716 EPROM (with Monitor)

Both versions include sockets for 2716s or 2532s, 8 16 pin sockets for I/O interfacing and a DB25 connector for RS232.

All address and data lines are brought off the board to the 50 pin edge connector. (similar to the Apple II bus)

This board also features power on reset and cassette interface.

81-030 C Fully Populated	$349.95
81-030M Partially Populated	$249.95
81-030B Bare Board	$ 89.95
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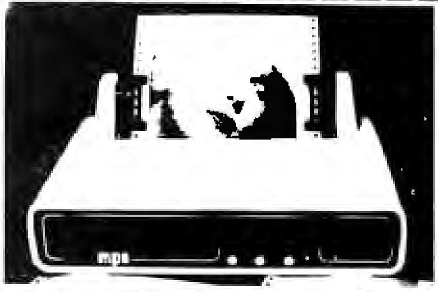

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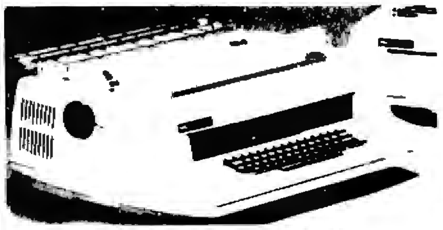

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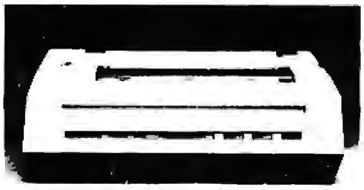

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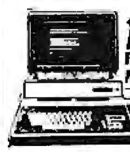

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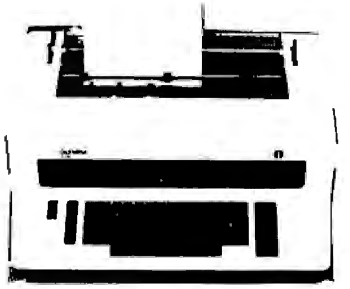

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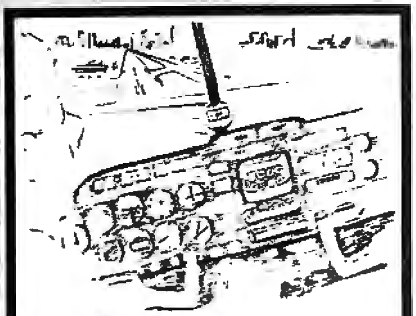

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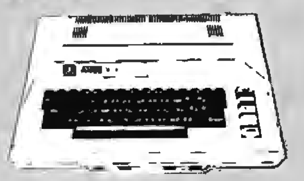

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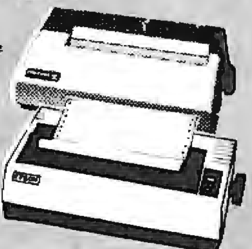

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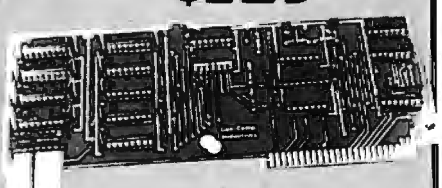

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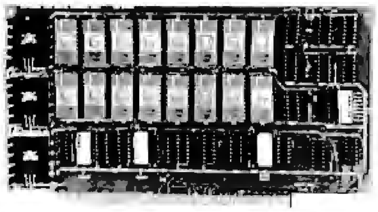

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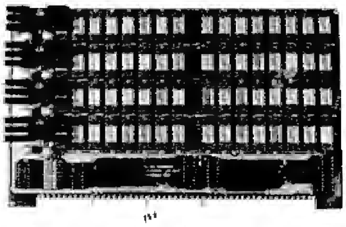

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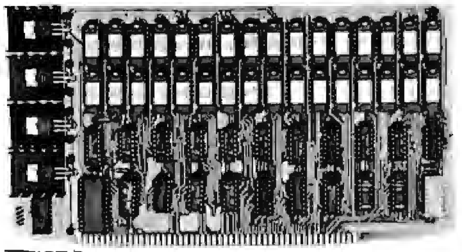

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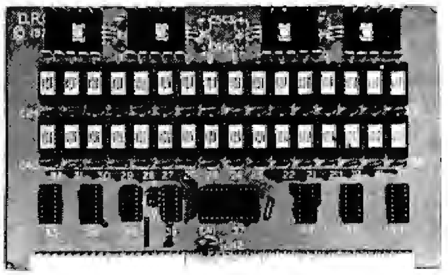

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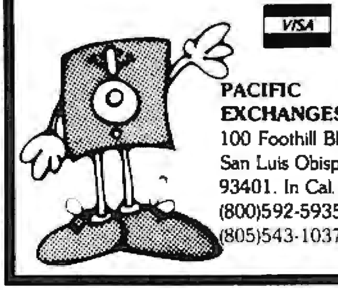

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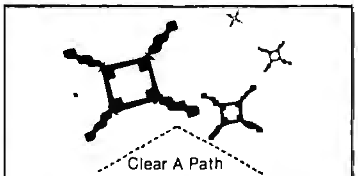

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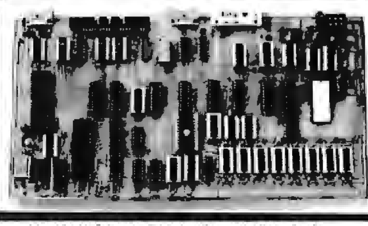

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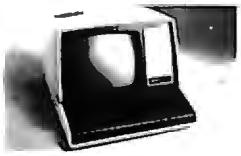

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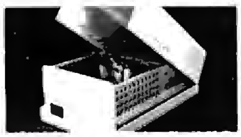

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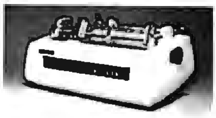

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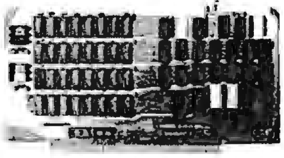

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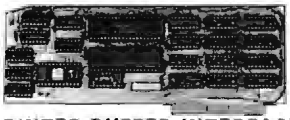

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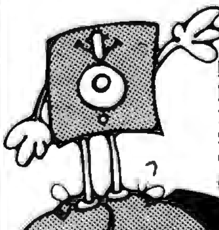

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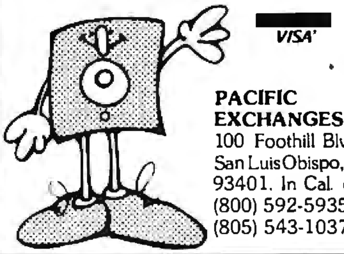

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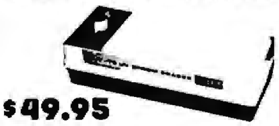

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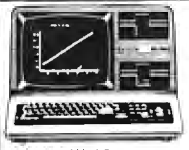

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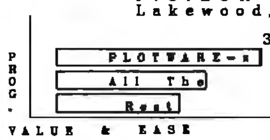

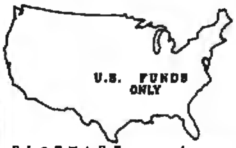

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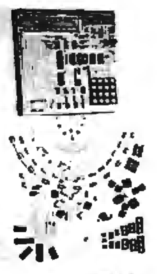

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C-60	13.50	57.00
C-90	17.50	77.50

5-screw shell, boxes, labels, product warranty, UPS shipping included. Please no P.O. box. CA Customers add taxes.

MICROSETTE CO.
475 Ellis St., Mt. View,
CA 94043 (415) 968-1604

Circle 247 on inquiry card.

Circle 194 on inquiry card. →

The Best Boards
SD Prices Slashed !!!

Single User System

SBC-200, 64K ExpandoRAM II, Versafloppy II, CP/M 2.2

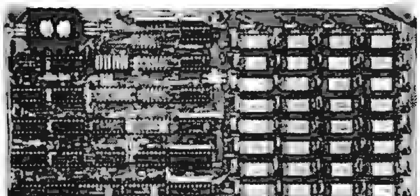
$995.00

4 MHz Z-80A CPU, 64K RAM, serial I/O port, parallel I/O port, double-density disk controller, CP/M 2.2 disk and manuals, system monitor, control and diagnostic software.

-All boards are assembled and tested-

ExpandoRAM III

64K to 256K expandable RAM board



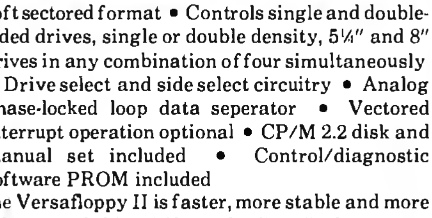
SD Systems has **duplicated** the famous reliability of their ExpandoRAM I and II boards in the new ExpandoRAM III, a board capable of containing 256K of high speed RAM. Utilizing the new 64K x 1 dymanic RAM chips, you can configure a memory of 64K, 128K, 192K, or 256K, all on one S-100 board. Memory address decoding is done by a programmed bipolar ROM so that the memory map may be dip-switch configured to work with either COSMOS/MPM-type systems or with OASIS-type systems.

Extensive application notes concerning how to operate the ExpandoRAM III with Cromemco, Intersystems, and other popular 4 MHz Z-80 systems are contained in the manual.

MEM-65064A	*64K A & T*	**$495.00**
MEM-65128A	*128K A & T*	**$639.95**
MEM-65192A	*192K A & T*	**$769.95**
MEM-65256A	*256K A & T*	**$879.95**

Versafloppy II

Double density controller with CP/M 2.2



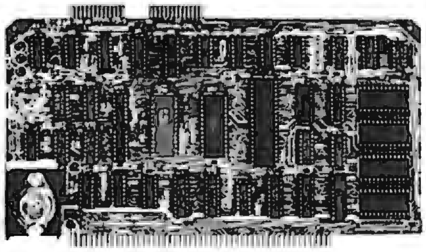
• S-100 bus compatible • IBM 3740 compatible soft sectored format • Controls single and double-sided drives, single or double density, 5¼" and 8" drives in any combination of four simultaneously • Drive select and side select circuitry • Analog phase-locked loop data seperator • Vectored interrupt operation optional • CP/M 2.2 disk and manual set included • Control/diagnostic software PROM included

The Versafloppy II is faster, more stable and more tolerant of bit shift and "jitter" than most controllers. CP/M 2.2 and all necessary control and diagnostic software are included.

IOD-1160A *A & T with CP/M 2.2* .. **$370.00**

SBC-200

2 or 4 MHz single board computer



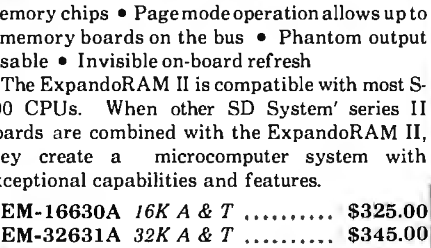
• S-100 bus compatible • Powerful 4MHz Z-80A CPU • Synchronous/asynchronous serial I/O port with RS-232 interface and software programmable baud rates up to 9600 baud • Parallel input and parallel output port • Four channel counter/timer • Four maskable, vectored interrupt inputs and a non-maskable interrupt • 1K of on-board RAM • Up to 32K of on-board ROM • System monitor PROM included

The SBC-200 is an excellent CPU board to base a microcomputer system around. With on-board RAM, ROM, and I/O, the SBC-200 allows you to build a powerful three-board system that has the same features found in most five-board microcomputers. The SBC-200 is compatible with both single-user and multi-user systems.

CPU-30200A *A & T with monitor* . **$299.95**

ExpandoRAM II

16K to 64K expandable RAM board



• S-100 bus compatible • Up to 4MHz operation • Expandable from 16K to 64K • Uses 16 x 1 4116 memory chips • Page mode operation allows up to 8 memory boards on the bus • Phantom output disable • Invisible on-board refresh

The ExpandoRAM II is compatible with most S-100 CPUs. When other SD System' series II boards are combined with the ExpandoRAM II, they create a microcomputer system with exceptional capabilities and features.

MEM-16630A	*16K A & T*	**$325.00**
MEM-32631A	*32K A & T*	**$345.00**
MEM-48632A	*48K A & T*	**$365.00**
MEM-64633A	*64K A & T*	**$385.00**

COSMOS

Multi-user operating system

• Multi-user disk operating system • Allows up to 8 users to run independent jobs concurrently • Each user has a seperate file directory

COMOS supports all the file structures of CP/M 2.2, and is compatible at the applications program level with CP/M 2.2, so that most programs written to run under CP/M 2.2 or SDOS will also run under COSMOS.

SFC-55009039F *COSMOS on 8" disk* **$395.00**

Multi-User System

SBC-200, 256K ExpandoRAM III, Versafloppy II, MPC-4 COSMOS Multi-User Operating System, C BASIC II

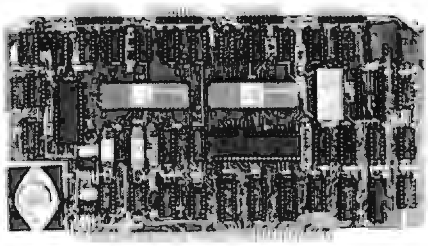
$1995.00

Two Z-80A CPUs (4 MHz), 256K RAM, 5 serial I/O ports with independently programmable baud rates and vectored interrupts, parallel input port, parallel output port, 8 counter/timer channels, real time clock, single and double sided/single or double density disk controller for 5¼" and 8" drives, up to 36K of on-board ROM, CP/M 2.2 compatible COSMOS interrupt driven multi-user disk operating system, allows up to 8 users to run independent jobs concurrently, C BASIC II, control and diagnostic software in PROM included.

-All boards are assembled and tested-

MPC-4

Intelligent communications interface



• Four buffered serial I/O ports • On-board Z-80A processor • Four CTC channels • Independently programmable baud rates • Vectored interrupt capability • Up to 4K of on-board PROM • Up to 2K of on-board RAM • On-board firmware

This is not just another four-port serial I/O board! The on-board processor and firmware provide sufficient intelligence to allow the MPC-4 to handle time consuming I/O tasks, rather than loading down your CPU. To increase overall efficiency, each serial channel has an 80 character input buffer and a 128 character output buffer. The on-board firmware can be modified to make the board SDLC or BISYNC compatible. In combination with SD's COSMOS operating system (which is included with the MPC-4), this board makes a perfect building block for a multi-user system.

IOI-1504A *A & T with COSMOS* .. **$495.00**

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Continental U.S.	*Inside California*
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For Technical Inquires or Customer Service call:

213-973-7707

JADE

Computer Products

4901 W. Rosecrans, Hawthorne, Ca 90250

TERMS of SALE: Cash, checks, credit cards, or Purchase Orders from qualified firms and institutions. **Minimum Order $15.00.** California residents add 6% tax. Minimum shipping & handling charge $3.00. Pricing & availibility subject to change

JADE

Computer Products

S-100 CPU Boards

THE BIG Z* - Jade

2 or 4 MHz switchable Z-80 CPU with serial I/O, accomodates 2708, 2716, or 2732 EPROM, baud rates from 75 to 9600*

CPU-30201K	*Kit*	$139.95
CPU-30201A	*A & T*	$189.95
CPU-30200B	*Bare board*	$35.00

2810 Z-80* CPU - Cal Comp Sys

2/4 MHz Z-80A CPU with RS-232C serial I/O port and on-board MOSS 2.2 monitor PROM, front panel compatible.*

CPU-30400A	*A & T*	$269.95

CB-2 Z-80 CPU - S.S.M.

2 or 4 MHz Z-80 CPU board with provision for up to 8K of ROM or 4K of RAM on board, extended addressing, IEEE S-100, front panel compatible.

CPU-30300K	*Kit*	$239.95
CPU-30300A	*A & T*	$299.95

S-100 PROM Boards

PROM-100 - SD Systems

2708, 2716, 2732 EPROM programmer w/software

MEM-99520K	*Kit*	$189.95
MEM-99520A	*A & T*	$249.95

PB-1 - S.S.M.

2708, 2716 EPROM board with built-in programmer

MEM-99510K	*Kit*	$154.95
MEM-99510A	*A & T*	$219.95

EPROM BOARD - Jade

16K or 32K uses 2708's or 2716's, 1K boundary

MEM-16230K	*Kit*	$79.95
MEM-16230A	*A & T*	$119.95

S-100 Video Boards

VB-3 - S.S.M.

80 characters x 24 lines expandable to 80 x 48 for a full page of text, upper & lower case, 256 user defined symbols, 160 x 192 graphics matrix, memory mapped, has key board input.

IOV-1095K	*4 MHz kit*	$349.95
IOV-1095A	*4 MHz A & T*	$439.95
IOV-1096K	*80 x 48 upgrade*	$39.95

VDB-8024 - SD Systems

80 x 24 I/O mapped video board with keyboard I/O, and on-board Z-80A.*

IOV-1020A	*A & T*	$459.95

VIDEO BOARD - S.S.M.

64 characters x 16 lines, 128 x 48 matrix for graphics, full upper/lower case ASCII character set, numbers, symbols, and greek letters, normal/reverse/blinking video, S-100.

IOV-1051K	*Kit*	$149.95
IOV-1051A	*A & T*	$219.95
IOV-1051B	*Bare board*	$34.95

S-100 Motherboards

ISO-BUS - Jade

Silent, simple, and on sale - a better motherboard

6 Slot (5¼" x 8⅝")		
MBS-061B	*Bare board*	$19.95
MBS-061K	*Kit*	$39.95
MBS-061A	*A & T*	$49.95
12 Slot (9¾" x 8⅝")		
MBS-121B	*Bare board*	$29.95
MBS-121K	*Kit*	$69.95
MBS-121A	*A & T*	$89.95
18 Slot (14½" x 8⅝")		
MBS-181B	*Bare board*	$49.95
MBS-181K	*Kit*	$99.95
MBS-181A	*A & T*	$139.95

S-100 RAM Boards

MEMORY BANK - Jade

4 MHz, S-100, bank selectable, expandable from 16K to 64K

MEM-99730B	*Bare Board*	$49.95
MEM-99730K	*Kit no RAM*	$199.95
MEM-32731K	*32K Kit*	$239.95
MEM-64733K	*64K Kit*	$279.95
Assembled & Tested		add $50.00

64K RAM - Calif Computer Sys

4 MHz bank port / bank byte selectable, extended addressing, 16K bank selectable, PHANTOM line allows memory overlay, 8080 / Z-80 / front panel compatible.

MEM-64565A	*A & T*	$575.00

64K STATIC RAM - Mem Merchant

64K static S-100 RAM card, 4-16K banks, up to 8MHz

MEM-64400A	*A & T*	$789.95

32K STATIC RAM - Jade

2 or 4 MHz expandable static RAM board uses 2114L's

MEM-16151K	*16K 4 MHz kit*	$169.95
MEM-32151K	*32K 4 MHz kit*	$299.95
Assembled & tested		add $50.00

16K STATIC RAM - Mem Merchant

4 MHz 16K static RAM board, IEEE S-100, bank selectable, Phantom capability, addressable in 4K blocks, "disable-able" in 1K segments, extended addressing, low power

MEM-16171A	*A & T*	$164.95

S-100 Disk Controllers

DOUBLE-D - Jade

Double density controller with the inside track, on-board Z-80A, printer port, IEEE S-100, can function on an interrupt driven buss*

IOD-1200K	*Kit*	$299.95
IOD-1200A	*A & T*	$375.00
IOD-1200B	*Bare board*	$59.95

DOUBLE DENSITY - Cal Comp Sys

5¼" and 8" disk controller, single or double density, with on-board boot loader ROM, and free CP/M 2.2 and manual set.*

IOD-1300A	*A & T*	$374.95

S-100 I/O Boards

S.P.I.C. - Jade

Our new I/O card with 2 SIO's, 4 CTC's, and 1 PIO

IOI-1045K	*2 CTC's, 1 SIO, 1 PIO*	$179.95
IOI-1045A	*A & T*	$239.95
IOI-1046K	*4 CTC's, 2 SIO's, 1 PIO*	$219.95
IOI-1046A	*A & T*	$299.95
IOI-1045B	*Bare board w/ manual*	$49.95

I/O-4 - S.S.M.

2 serial I/O ports plus 2 parallel I/O ports

IOI-1010K	*Kit*	$179.95
IOI-1010A	*A & T*	$249.95
IOI-1010B	*Bare board*	$35.00

S-100 Mainframes

MAINFRAME - Cal Comp Sys

12 slot S-100 mainframe with 20 amp power supply

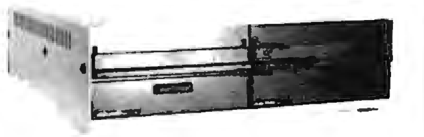
ENC-112105	*Kit*	$329.95
ENC-112106	*A & T*	$399.95

DISK MAINFRAME - N.N.C.

Holds 2 8" drives and a 12 slot S-100 system. Attractive metal cabinet with 12 slot motherboard & card cage, power supply, dual fans, lighted switch, and other professional features

ENS-112325	*with 25 amp p.s.*	$799.95

Disk Drives



Handsome metal cabinet with proportionally balanced air flow system • Rugged dual drive power supply • Power cable kit • Power switch, line cord, fuse holder, cooling fan • Never-Mar rubber feet • All necessary hardware to mount 2-8" disk drives, power supply, and fan • Does not include signal cable

Dual 8" Subassembly Cabinet

END-000420	*Bare cabinet*	$59.95
END-000421	*Cabinet kit*	$225.00
END-000431	*A & T*	$359.95

8" Disk Drive Subsystems Single Sided, Double Density

END-000423	*Kit w/2 FD100-8Ds*	$924.95
END-000424	*A & T w/2 FD100-8Ds*	$1124.95
END-000433	*Kit w/2 SA-801Rs*	$999.95
END-000434	*A & T w/2 SA-801Rs*	$1195.00

8" Disk Drive Subsystems Double Sided, Double Density

END-000426	*Kit w/2 DT-8s*	$1224.95
END-000427	*A & T w/2 DT-8s*	$1424.95
END-000436	*Kit w/2 SA-851Rs*	$1495.00
END-000437	*A & T w/2 SA-851Rs*	$1695.00

QUME DT-8

8" Double-Sided, Double-Density Disk Drive

1 Drive	$524.95 each
2 Drives	$499.95 each
10 Drives	$479.95 each

Jade Part Number MSF-750080

Shugart 801R

8" Single-Sided, Double-Density Disk Drive

1 Drive	$394.95 each
2 Drives	$389.95 each

Jade Part Number MSF-10801R

SIEMENS 8"

8" Single-Sided, Double-Density Disk Drive

1 Drive	$384.95 each
2 Drives	$349.95 each
10 Drives	$324.95 each

Jade Part Number MSF-201120

Shugart 400

5¼" Single-Sided, Double-Density Disk Drive

1 Drive	$234.95 each
2 Drives	$224.95 each
10 Drives	$219.95 each

Jade Part Number MSM-104000

END-000213	*Case & power supply*	$74.95

Circle 195 on inquiry card.

7400

SN7400N	.20	SN7472N	.29	SN74156N	.79
SN7401N	.20	SN7473N	.35	SN74157N	.69
SN7402N	.25	SN7474N	.35	SN74160N	.89
SN7403N	.25	SN7475N	.49	SN74161N	.89
SN7404N	.25	SN7476N	.35	SN74162N	.89
SN7405N	.29	SN7479N	5.00	SN74163N	.89
SN7406N	.35	SN7480N	.50	SN74164N	.89
SN7407N	.35	SN7482N	.99	SN74165N	.89
SN7408N	.29	SN7483N	.69	SN74166N	1.25
SN7409N	.29	SN7485N	.89	SN74167N	2.79
SN7410N	.25	SN7486N	.35	SN74170N	1.95
SN7411N	.29	SN7489N	1.75	SN74172N	4.95
SN7412N	.35	SN7490N	.49	SN74173N	1.39
SN7413N	.40	SN7491N	.59	SN74174N	.99
SN7414N	.69	SN7492N	.45	SN74175N	.89
SN7416N	.29	SN7493N	.45	SN74176N	.79
SN7417N	.29	SN7494N	.69	SN74177N	.79
SN7420N	.25	SN7495N	.69	SN74179N	1.49
SN7421N	.29	SN7496N	.69	SN74180N	.79
SN7422N	.45	SN7497N	3.00	SN74181N	2.25
SN7423N	.29	SN74100N	1.49	SN74182N	.79
SN7425N	.29	SN74104N	.89	SN74184N	2.49
SN7426N	.29	SN74105N	.89	SN74185N	2.49
SN7427N	.25	SN74107N	.35	SN74190N	1.25
SN7428N	.49	SN74109N	.39	SN74191N	1.25
SN7430N	.25	SN74116N	1.95	SN74192N	.89
SN7432N	.29	SN74121N	.39	SN74193N	.89
SN7437N	.25	SN74122N	.55	SN74194N	.89
SN7438N	.40	SN74123N	.59	SN74195N	.89
SN7439N	.25	SN74125N	.49	SN74196N	.89
SN7440N	.20	SN74126N	.49	SN74197N	.89
SN7441N	.89	SN74132N	.75	SN74198N	1.49
SN7442N	.59	SN74136N	.75	SN74199N	1.49
SN7443N	1.10	SN74141N	.99	SN74221N	1.25
SN7444N	1.10	SN74142N	3.25	SN74251N	.99
SN7445N	.89	SN74143N	3.49	SN74276N	1.95
SN7446N	.79	SN74144N	3.49	SN74279N	.79
SN7447N	.69	SN74145N	.79	SN74283N	1.49
SN7448N	.79	SN74147N	1.95	SN74284N	3.95
SN7450N	.20	SN74148N	1.29	SN74285N	3.95
SN7451N	.20	SN74150N	1.25	SN74365N	.69
SN7453N	.20	SN74151N	.69	SN74366N	.69
SN7454N	.20	SN74152N	.69	SN74367N	.69
SN7459A	.25	SN74153N	.79	SN74368N	.69
SN7460N	.20	SN74154N	1.25	SN74390N	1.49
SN7470N	.29	SN74155N	.79	SN74393N	1.49

74LS

74LS00	.29	74LS92	.75	74LS192	1.15
74LS01	.29	74LS93	.75	74LS193	1.15
74LS02	.29	74LS95	.99	74LS194	1.15
74LS03	.29	74LS96	1.15	74LS195	1.15
74LS04	.35	74LS107	.45	74LS197	1.19
74LS05	.35	74LS109	.45	74LS221	1.19
74LS08	.35	74LS112	.45	74LS240	1.49
74LS09	.35	74LS113	.49	74LS241	1.49
74LS10	.35	74LS114	.49	74LS242	1.49
74LS11	.39	74LS122	.89	74LS243	1.49
74LS12	.35	74LS123	1.15	74LS244	1.49
74LS13	.59	74LS125	.59	74LS245	2.95
74LS14	.99	74LS126	.59	74LS247	1.19
74LS15	.35	74LS132	.99	74LS248	1.19
74LS20	.35	74LS133	.89	74LS249	1.19
74LS21	.35	74LS136	.49	74LS251	.99
74LS22	.35	74LS138	.89	74LS253	.99
74LS26	.35	74LS139	.89	74LS257	.89
74LS27	.35	74LS151	.89	74LS258	.89
74LS28	.35	74LS153	.89	74LS260	.69
74LS30	.35	74LS154	1.75	74LS266	.69
74LS32	.35	74LS155	.89	74LS273	1.95
74LS33	.59	74LS156	.89	74LS279	.89
74LS37	.45	74LS157	.89	74LS283	.89
74LS38	.39	74LS158	.89	74LS290	.99
74LS40	.35	74LS160	1.15	74LS293	.99
74LS42	.89	74LS161	1.15	74LS298	1.25
74LS47	.89	74LS162	1.15	74LS352	1.29
74LS48	1.15	74LS163	1.15	74LS353	1.29
74LS49	1.15	74LS164	1.15	74LS365	.69
74LS51	.35	74LS165	1.15	74LS366	.69
74LS54	.35	74LS168	1.19	74LS367	.69
74LS55	.35	74LS169	1.19	74LS368	.69
74LS73	.45	74LS170	1.95	74LS373	1.95
74LS74	.45	74LS173	.99	74LS374	1.95
74LS75	.59	74LS174	.99	74LS375	.89
74LS76	.45	74LS175	.99	74LS386	.69
74LS78	.49	74LS181	2.95	74LS393	2.49
74LS83	.89	74LS190	1.25	74LS399	2.49
74LS85	1.25	74LS191	1.25	74LS670	2.49
74LS86	.49			81LS95	1.95
74LS90	.69			81LS97	1.95

74S

74S00	.45	74S124	3.95	74S243	3.25
74S02	.45	74S133	.55	74S244	3.25
74S03	.45	74S134	.69	74S251	1.45
74S04	.55	74S135	1.19	74S253	1.45
74S05	.55	74S136	1.75	74S257	1.35
74S08	.50	74S138	1.35	74S258	1.35
74S09	.50	74S139	1.35	74S260	.79
74S10	.45	74S140	.79	74S280	2.95
74S11	.45	74S151	1.35	74S287	3.25
74S15	.45	74S153	1.35	74S288	2.75
74S20	.45	74S157	1.35	74S373	3.49
74S22	.45	74S158	1.35	74S374	3.49
74S30	.45	74S160	2.95	74S387	2.95
74S32	.55	74S174	1.59	74S471	10.95
74S38	1.25	74S175	1.59	74S472	10.95
74S40	.50	74S188	2.95	74S473	10.95
74S51	.45	74S194	1.95	74S474	12.95
74S64	.50	74S195	1.95	74S475	12.95
74S65	.50	74S196	1.95	74S570	5.95
74S74	.75	74S240	2.95	74S571	5.95
74S86	.79	74S241	2.95	74S572	9.95
74S112	.79	74S242	3.25	74S573	9.95
74S113	.79			74S940	3.15
74S114	.79			74S941	3.15

CA—LINEAR

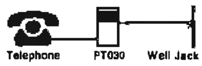
CA3010H	.99	CA3060N	3.25	CA3089N	3.75
CA3013H	2.15	CA3080H	1.25	CA3096N	3.95
CA3023H	3.25	CA3081N	2.00	CA3130H	1.39
CA3035H	2.49	CA3082N	2.00	CA3140H	1.25
CA3039H	1.35	CA3083N	1.60	CA3160H	1.25
CA3046N	1.30	CA3086N	.85	CA3401N	.69
CA3059N	3.25			CA3600N	3.50

CD—CMOS

CD4000	.39	CD4041	1.49	CD4098	2.49
CD4001	.39	CD4042	.99	CD4506	.75
CD4002	.39	CD4043	.89	CD4507	.99
CD4006	1.19	CD4044	.89	CD4508	3.95
CD4007	.25	CD4046	1.79	CD4510	1.39
CD4009	.49	CD4047	2.50	CD4511	1.29
CD4010	.49	CD4048	1.35	CD4512	1.49
CD4011	.39	CD4049	.49	CD4514	3.95
CD4012	.25	CD4050	.69	CD4515	2.95
CD4013	.49	CD4051	1.19	CD4516	1.49
CD4014	1.39	CD4052	1.19	CD4518	1.79
CD4015	1.19	CD4053	1.19	CD4519	.89
CD4016	.59	CD4056	2.95	CD4520	1.29
CD4017	1.19	CD4059	9.95	CD4526	1.79
CD4018	.99	CD4060	1.49	CD4528	1.19
CD4019	.49	CD4066	.79	CD4529	1.95
CD4020	1.19	CD4068	.39	CD4543	2.79
CD4021	1.39	CD4069	.45	CD4562	11.95
CD4022	1.19	CD4070	.55	CD4566	2.79
CD4023	.29	CD4071	.49	CD4583	2.49
CD4024	.79	CD4072	.49	CD4584	.75
CD4025	.23	CD4073	.39	CD4723	1.95
CD4026	2.95	CD4075	.39	CD4724	1.95
CD4027	.69	CD4076	1.39	MC14409	17.95
CD4028	.89	CD4078	.55	MC14410	18.95
CD4029	1.49	CD4081	.39	MC14411	15.95
CD4030	.49	CD4082	.39	MC14412	15.95
CD4034	3.49	CD4093	.99	MC14419	7.95
CD4035	.99			MC14433	15.95
CD4040	1.49			MC14538	2.49
				MC14541	1.95

Phone Tunes

As Seen on "Good Morning America"
Replaces the Telephone Ringer Bell with a Selection of 30 Familiar Tunes



Each Unit will play any of the following tunes:

- Rule Brittania
- O Canada
- Colonel Bogey
- Westminister Chimes
- Mexican Hat Dance
- Twinkle, Twinkle Little Star
- Deutschlandlied
- God Save the Queen
- Close Encounters
- Happy Birthday
- Wedding March
- Jingle Bells
- Auld Lang Syne
- Soldiers Chorus
- Sailor's Hornpipe
- Chargel
- Greensleeves
- Lorelei
- Eyes of Texas
- Star Spangled Banner
- Oranges and Lemons
- Wilhelmus
- Mozart Sonata
- Pomp & Circumstance
- William Tell Overture
- Bach Toccata in D Minor
- Shave and a Haircut
- Blue Danube Waltz
- Beethoven's 5th
- La Marseillaise

FEATURES

Replaces monotonous telephone ringer bell. Easily connects to any standard telephone. Can be used alongside regular phone or replace a remote ringer elsewhere in building or outside. FCC approved. Can be used on any telephone system — worldwide. Use a different tune to identify extension phones. Microprocessor controlled. Adjustable volume control and variable tune speed control. Operates on two 9-volt batteries or AC Adapter (not included).

PT030 Phone Tunes $49.95
AD30 AC Adapter $8.95

DISCRETE LEDS

XC556R	.200"	red	5/$1	MV50	.085"	red	6/$1
XC556G	.200"	green	4/$1	XC209R	.125"	red	5/$1
XC556Y	.200"	yellow	4/$1	XC209G	.125"	green	4/$1
XC556C	.200"	clear	4/$1	XC209Y	.125"	yellow	4/$1
XC22R	.200"	red	5/$1	XC526R	.185"	red	5/$1
XC22G	.200"	green	4/$1	XC526G	.185"	green	4/$1
XC22Y	.200"	yellow	4/$1	XC526Y	.185"	yellow	4/$1
MV10B	.170"	red	4/$1	XC526C	.185"	clear	4/$1

.200(T1¾) Red/Green

Diffused Bi-Color LED

Part No.	1-99	100+
XC5491	.79	.69

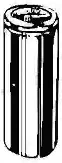
XC111 RED LED, METAL MTG. HDW, 1/4" LEADS.
RL-2 . . $.39 ea. or 3/$1.00

DISPLAY LEDS

C.A. — Common Anode
D.D. — Double Digit
C.C. — Common Cathode
RHD — Right Hand Decimal

Type	Polarity	Ht	Price	Type	Polarity	Ht	Price
MAN 1	C.A.—red	.270	2.95	DLG507	C.A.—green	.500	1.25
MAN 2	5x7 D.M.—red	.300	4.95	DL704	C.C.—red	.300	1.25
MAN 3	C.C.—red	.125	.25	DL707	C.A.—red	.300	1.25
MAN 52	C.A.—green	.300	.99	DL728	C.C.—red	.500	1.49
MAN 54	C.C.—green	.300	.99	DL741	C.A.—red	.600	1.25
MAN 71	C.A.—red	.300	.75	DL747	C.A.—red	.600	1.49
MAN 72	C.A.—red	.300	.75	DL750	C.C.—red	.600	1.49
MAN 74	C.C.—red	.300	1.25	DLO847	C.A.—orange	.800	1.49
MAN 82	C.A.—yellow	.300	.49	DLO850	C.C.—orange	.800	1.49
MAN 84	C.C.—yellow	.300	.99	DL338	C.C.—red	.110	.35
MAN 3620	C.A.—orange	.300	.49	FND358	C.C. ± 1	.357	.99
MAN 3630	C.A.—orange ± 1	.300	.99	FND357	C.C.	.357	.75
MAN 3640	C.C.—orange	.300	.99	FND500	C.C. (FND503)	.500	.99
MAN 4610	C.A.—orange	.400	.99	FND507	C.A. (FND510)	.500	.99
MAN 6610	C.A.—orange—DD	.560	.99	HDSP-3401	C.A.—red	.800	1.50
MAN 6630	C.A.—orange ± 1	.560	.99	HDSP-3403	C.C.—red	.800	1.50
MAN 6640	C.C.—orange—DD	.560	.99	HDSP-3406	C.C. red ± 1	.800	1.50
MAN 6650	C.C.—orange ± 1	.560	.99	5082-7751	C.A., R.H.D.—red	.430	1.25
MAN 6660	C.A.—orange	.560	.99	5082-7760	C.C., R.H.D.—red	.430	1.25
MAN 6710	C.A.—red—DD	.560	.99	5082-7300	4x7Numeric (RHD)	.600	22.00
MAN 6740	C.C.—red—DD	.560	.99	5082-7302	4x7Numeric (LHD)	.600	22.00
MAN 6750	C.C.—red ± 1	.560	.99	5082-7340	4x7 Hxdcl. (0-9/A-F)	.600	22.50
DLO304	C.C.—orange	.300	1.25	4N28	Photo Xsistor Opto-Isol.		.69
DLO307	C.A.—orange	.300	1.25	LIT-1	Photo Xsistor Opto-Isol.		.69
DLG500	C.C.—green	.500	1.25	MOC3010	Optically Isol. Triac Driver		1.25

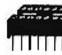
COMPUTER GRADE CAPACITORS



MFD	WVDC	PRICE	MFD	WVDC	PRICE	MFD	WVDC	PRICE
[illegible]	[illegible]	[illegible]	10,000	15	2.95	24,000	20	7.95
500	200	2.49	10,000	16	3.95	27,000	10	2.95
1,250	[illegible]	.99	11,000	19	4.95	32,500	25	4.95
1,500	25	1.95	11,000	55	[illegible]	40,000	25	5.95
1,500	50	2.95	11,000	60	[illegible]	43,000	10	5.95
2,000	10	2.95	13,000	16	[illegible]	50,000	20	7.95
2,250	100	3.95	14,000	13	[illegible]	52,000	20	[illegible]
2,300	33	[illegible]	14,000	35	[illegible]	55,000	15	5.95
2,500	15	2.95	18,000	10	3.95	58,000	[illegible]	5.95
3,000	25	1.95	20,000	20	2.95	65,000	10	7.95
3,600	40	[illegible]	20,000	55	3.95	73,600	5	7.95
4,500	50	3.95	21,000	15	3.95	80,000	15	[illegible]
5,500	25	4.49	23,000	7	1.95	90,000	10	[illegible]
6,100	40	2.49	23,000	10	2.95	160,000	10	[illegible]
[illegible]	50	4.95	23,000	20	3.95	200,000	3	12.95

OVER 200 OTHER VALUES AVAILABLE — CALL OR WRITE FOR YOUR REQUIREMENT

LOW PROFILE (TIN) SOCKETS

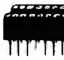


	1-24	25-49	50-100
8 pin LP	.17	.16	.15
14 pin LP	.20	.19	.18
16 pin LP	.22	.21	.20
18 pin LP	.29	.28	.27
20 pin LP	.34	.32	.30
22 pin LP	.37	.36	.35
24 pin LP	.38	.37	.36
28 pin LP	.45	.44	.43
36 pin LP	.60	.59	.58
40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100
14 pin ST	.27	.25	.24
16 pin ST	.30	.27	.25
18 pin ST	.35	.32	.30
24 pin ST	.49	.45	.42
28 pin ST	.99	.90	.81
36 pin ST	1.39	1.26	1.15
40 pin ST	1.59	1.45	1.30

SOLDERTAIL (GOLD) STANDARD



	1-24	25-49	50-100
8 pin SG	.39	.35	.31
14 pin SG	.49	.45	.41
16 pin SG	.54	.49	.44
18 pin SG	.59	.53	.48
24 pin SG	.79	.75	.69
28 pin SG	1.10	1.00	.90
36 pin SG	1.65	1.40	1.26
40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100
8 pin WW	.59	.54	.49
10 pin WW	.69	.63	.58
14 pin WW	.79	.73	.67
16 pin WW	.85	.77	.70
18 pin WW	.99	.90	.81
20pin WW	1.19	1.08	.99
22 pin WW	1.49	1.35	1.23
24 pin WW	1.39	1.26	1.14
28pin WW	1.69	1.53	1.38
36 pin WW	2.19	1.99	1.79
40pin WW	2.29	2.09	1.89

1/4 WATT RESISTOR ASSORTMENTS – 5%

		Values						
ASST. 1	5ea.	10 Ohm 12 Ohm 15 Ohm 18 Ohm 22 Ohm / 27 Ohm 33 Ohm 39 Ohm 47 Ohm 56 Ohm					50pcs.	$1.95
ASST. 2	5ea.	68 Ohm 82 Ohm 100 Ohm 120 Ohm 150 Ohm / 180 Ohm 220 Ohm 270 Ohm 330 Ohm 390 Ohm					50pcs.	$1.95
ASST. 3	5ea.	470 Ohm 560 Ohm 680 Ohm 820 Ohm 1K / 1.2K 1.5K 1.8K 2.2K 2.7K					50pcs.	$1.95
ASST. 4	5ea.	3.3K 3.9K 4.7K 5.6K 6.8K / 8.2K 10K 12K 15K 18K					50pcs.	$1.95
ASST. 5	5ea.	22K 27K 33K 39K 47K / 56K 68K 82K 100K 120K					50pcs.	$1.95
ASST. 6	5ea.	150K 180K 220K 270K 330K / 390K 470K 560K 680K 820K					50pcs.	$1.95
ASST. 7	5ea.	1M 1.2M 1.5M 1.8M 2.2M / 2.7M 3.3M 3.9M 4.7M 5.6M					50pcs.	$1.95
ASST. 8R		Includes Resistor Assts. 1-7 (350 pcs.)						$10.95 ea.

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1/82

INTERSIL

Part No.	Function	Price
7045IPI	CMOS Precision Timer	14.95
7045EV/Kit*	Stopwatch Chip, XTL	24.95
7106CPL	3½ Digit A/D (LCD Drive)	16.95
7106EV/Kit*	IC, Circuit Board, Display	34.95
7107CPL	3½ Digit A/D (LED Drive)	15.95
7107EV/Kit*	IC, Circuit Board, Display	29.95
7116CPL	3½ Digit A/D LCD Dis. HLO.	18.95
7117CPL	3½ Digit A/D LED Dis. HLO.	17.95
7201IDR	Low Battery Volt Indicator	2.25
7205IPG	CMOS LED Stopwatch/Timer	12.95
7205EV/Kit*	Stopwatch Chip, XTL	19.95
7206CJPE	Tone Generator	5.15
7206CEV/Kit*	Tone Generator Chip, XTL	12.95
7207AIPD	Oscillator Controller	6.50
7207AEV/Kit*	Freq. Counter Chip, XTL	13.95
7208IPI	Seven Decade Counter	17.95
7209IPA	Clock Generator	3.95
7215IPG	4 Func. CMOS Stopwatch CKT	13.95
7215EV/Kit*	4 Func. Stopwatch Chip, XTL	19.95
7216AIJI	8-Digit Univ. Counter C.A.	32.00
7216CIJI	8-Digit Freq. Counter C.A.	26.95
7216DIPI	8-Digit Freq. Counter C.C.	21.95
7217IJI	4-Digit LED Up/Down Counter	12.95
7218CIJI	8-Digit Univ. LED Drive	10.95
7224IPL	LCD 4½ Digit Up Counter DRI	11.25
7226AIJL	8-Digit Univ. Counter	31.95
7226AEV/Kit*	5 Function Counter Chip, XTL	74.95
7240IJE	CMOS Bin Prog. Timer/Counter	4.95
7242IJA	CMOS Divide-by-256 RC Timer	2.05
7250IJE	CMOS BCD Prog. Timer/Counter	6.00
7260IJE	CMOS BCD Prog. Timer/Counter	5.25
7555IPA	CMOS 555 Timer (8 pin)	1.45
7556IPD	CMOS 556 Timer (14 pin)	2.20
7611BCPA	CMOS Op Amp Comparator 5MV	2.25
7612BCPA	CMOS Op Amp Ext. Cmvr. 5MV	2.95
7621BCPA	CMOS Dual Op Amp Comp. 5MV	3.95
7631CCPE	CMOS Tri Op Amp Comp. 10MV	5.35
7641CCPD	CMOS Quad Op Amp Comp. 10MV	7.50
7642CCPD	CMOS Quad Op Amp Comp. 10MV	7.50
7660CPA	Voltage Converter	2.95
8038CCPD	Waveform Generator	4.95
8048CCPE	Monolithic Logarithmic Amp	21.60
8069CCQ	50ppm Band—GAP Volt Ref. Diode	2.50
8211CPA	Volt Ref/Indicator	2.95
8212CPA	Volt Ref/Indicator	2.95

74C

74C00	.39	74C95	1.59	74C221	1.95
74C02	.39	74C107	1.89	74C240	2.25
74C04	.39	74C151	2.95	74C244	2.25
74C08	.39	74C154	3.95	74C373	2.49
74C10	.39	74C157	2.25	74C374	2.75
74C14	.75	74C160	1.69	74C901	.69
74C20	.39	74C161	1.60	74C903	.69
74C30	.39	74C162	1.49	74C911	10.95
74C42	1.39	74C163	1.69	74C912	10.95
74C48	1.95	74C164	1.59	74C915	1.69
74C73	.79	74C173	1.39	74C917	10.95
74C74	.79	74C174	1.39	74C922	5.49
74C85	1.95	74C175	1.19	74C923	5.75
74C86	.99	74C192	1.69	74C925	7.50
74C89	6.95	74C193	1.69	74C926	7.50
74C90	1.29	74C195	1.59	80C95	.79
74C93	1.29			80C97	.79

LINEAR

LH0002CN	6.85	LM340T-5	1.25	LM702H	.79
LM10CLH	4.50	LM340T-12	1.25	LM703CN	.89
LM11CLH	4.75	LM340T-15	1.25	LM709N	.29
LH0070-0H	4.95	LM341P-5	.75	LM710N	.79
TL071CP	.79	LM341P-12	.75	LM711N	.79
TL072CP	1.39	LM341P-15	.75	LM723N	.69
TL074CN	2.49	LM342P-5	.69	LM733N	1.00
LH0082CD	35.80	LM342P-12	.69	LM739N	1.19
TL082CP	1.19	LM342P-15	.69	LM741CN	.35
TL084CN	2.19	LM348N	1.25	MC1741SCG	3.00
LH0094CD	36.80	LM350K	5.75	LM747N	.79
LM300H	.99	LF351N	.60	LM748N	.59
LM301CN	.35	LF353N	1.00	LM1014N	2.75
LM302H	1.95	LF355N	1.10	LM1310N	1.95
LM304H	1.95	LF356N	1.10	LM1458CN	.59
LM305H	.99	LM358N	1.00	LM1488N	1.25
LM307CN	.45	LM359N	1.79	LM1489N	1.25
LM308CN	1.00	LM370N	4.49	LM1496N	1.95
LM309H	1.95	LM373N	3.25	LM1556V	1.75
LM309K	1.25	LM377N	2.95	LM1800N	2.95
LM310CN	1.75	LM380N	1.25	LM1871N	5.49
LM311/CN	.90	LM381N	1.95	LM1872N	5.49
LM312H	2.49	LM382N	1.79	LM1877N-9	3.25
LM317MP	1.15	LM384N	1.95	LM1889N	3.20
LM317T	1.75	LM386N-3	1.29	LM1896N	1.75
LM317K	3.95	LM387N	1.45	LM2002T	1.49
LM318CN	1.95	LM389N	1.35	LM2877P	2.05
LM319N	1.95	LM392N	.69	LM2878P	2.25
LM320K-5	1.35	LF398N	4.00	LM2896P-1	2.25
LM320K-12	1.35	LM399H	5.00	LM3189N	2.95
LM320K-15	1.35	TL494CN	4.49	LM3900N	.69
LM320T-5	1.25	TL496CP	1.75	LM3905CN	1.25
LM320T-12	1.25	NE510A	6.00	LM3909N	1.15
LM320T-15	1.25	NE529A	4.95	LM3914N	3.95
LM323K	5.95	NE531H	3.95	LM3915N	3.95
LM324N	.99	NE536H	6.00	LM3916N	3.95
LM329DZ	.65	NE540H	6.00	RC4136N	1.25
LM331N	3.95	NE544N	4.95	RC4151NB	3.95
LM334Z	1.30	NE550A	1.30	RC4194TK	6.95
LM335Z	1.40	NE555V	.39	RC4195TK	5.49
LM336Z	1.75	LM556N	.99	LM4500A	3.25
LM337T	1.95	NE564N	3.95	ICL8038B	4.95
LM337MP	1.15	LM565N	1.25	LM13080N	1.29
LM338K	6.95	LM566CN	1.95	LM13600N	1.49
LM339N	.99	LM567V	1.25	75138N	1.95
LM340K-5	1.35	NE570N	4.95	75450N	.89
LM340K-12	1.35			75451CN	.39
LM340K-15	1.35			75492	.89

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

Value	1-9	10-99	100+	Value	1-9	10-99	100+
10 pf	.08	.06	.05	.001µF	.08	.06	.05
22 pf	.08	.06	.05	.0047µF	.08	.06	.05
47 pf	.08	.06	.05	.01µF	.08	.06	.05
100 pf	.08	.06	.05	.022µF	.09	.07	.06
220 pf	.08	.06	.05	.047µF	.09	.07	.06
470 pf	.08	.06	.05	.1µF	.15	.12	.10

100 VOLT MYLAR FILM CAPACITORS

.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022mf	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+20% DIPPED TANTALUMS (Solid) CAPACITORS

.1/35V	.39	.34	.29	1.5/35V	.41	.37	.29
.15/35V	.39	.34	.29	2.2/35V	.51	.45	.34
.22/35V	.39	.34	.29	3.3/25V	.53	.47	.37
.33/35V	.39	.34	.29	4.7/25V	.63	.56	.45
.47/35V	.39	.34	.29	6.8/25V	.79	.69	.55
.68/35V	.39	.34	.29	15/25V	1.39	1.25	.95
1.0/35V	.39	.34	.29	22/6V	.79	.69	.55

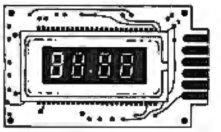
MINI. ALUMINUM ELECTROLYTIC CAPACITORS

Axial	1-99	100-499	500+	Radial	1-99	100-499	500+
.47/50V	.16	.14	.10	.47/25V	.15	.13	.12
1.0/50V	.19	.16	.12	.47/50V	.16	.14	.13
3.3/50V	.17	.15	.11	1.0/16V	.15	.13	.12
4.7/25V	.18	.15	.11	1.0/25V	.16	.14	.13
10/25V	.18	.15	.11	1.0/50V	.17	.15	.14
10/50V	.19	.16	.12	4.7/16V	.15	.13	.12
22/25V	.19	.16	.12	4.7/25V	.16	.14	.13
22/50V	.24	.20	.18	4.7/50V	.17	.15	.14
47/25V	.25	.21	.19	10/16V	.15	.13	.12
47/50V	.29	.25	.23	10/25V	.16	.14	.13
100/25V	.28	.24	.22	10/50V	.17	.15	.14
100/50V	.41	.37	.34	47/50V	.25	.21	.19
220/25V	.39	.34	.33	100/16V	.21	.17	.14
220/50V	.49	.45	.41	100/25V	.28	.23	.21
470/25V	.54	.49	.45	100/50V	.37	.34	.31
1000/16V	.79	.69	.61	220/16V	.25	.21	.19
2200/16V	.89	.79	.69	470/25V	.35	.31	.27

Circle 196 on inquiry card.

National Semiconductor

Clock Modules



12VDC AUTOMOTIVE/ INSTRUMENT CLOCK

APPLICATIONS:
- In-dash autoclocks
- After-market auto/ RV clocks
- Aircraft-marine clks.
- 12VDC oper. Instru.
- Portable/battery powered instrumnts.

Features: Bright 0.3" green display. Internal crystal timebase. ± 0.5 sec./day accur. Auto.display brightness control logic. Display color filterable to blue, blue-green, green & yellow. Complete—just add switches and lens.

MA1003 Module (3.05"Lx1.75"Hx.58"D) . **$16.95**

CLOCK MODULES

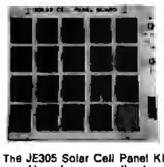
MA1023	.7" Red Digital LED Clock Module	8.95
MA1026	.7" Dig. LED Alarm Clock/Thermometer	18.95
MA5036	.3" Red Digital LED Clock/Timer	6.95
MA1002	.5" Red Digital LED Clock & Xformer	9.95
MA1010	.8" Red Digital LED Clock	7.95
MA1032	CBA .5" Digital LCD Clock	17.95
MA1043	.7" Green Digital LED Clock	8.95

TRANSFORMERS

102-P20	Xformer for MA1023,1043 & 5036 Mods.	3.49
102-P22	Xformer for MA1026 Clock Modules	3.49
102-P24	Xformer for MA1010 Clock Modules	3.49

NEW!

Sun Power Your Electronics! SOLAR CELL PANEL KIT



Features:
- Output: 10VDC, to 100mA in Series 5VDC, to 200mA in Parallel
- Panel may be easily connected for Series or Parallel out
- Over 11 square inches of active cell surface
- Voltage line tap @ 0.5V increments
- Provision for charging batteries
- Overall panel size: 4¼"L x 4½"H x ½"D

The JE305 Solar Cell Panel Kit contains 20 each solar cells. On the panel board are power line taps which allow the user to select voltages (one voltage at a time) from 0.5VDC to 10VDC. The applications of each panel can be further expanded by coupling additional panels in series for more voltage or in parallel for more current. The premium grade solar cells provide the current necessary for the operation of most portable transistor radios, small battery powered cassette tape players and unlimited experimental solar projects.

JE305 . . . . $39.95

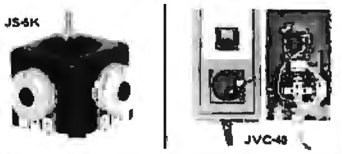
EPROM Erasing Lamp

- Erases 2708, 2716, 1702A, 5203Q, 5204Q, etc.
- Erases up to 4 chips within 20 minutes.
- Maintains constant exposure distance of one inch.
- Special conductive foam liner eliminates static build-up.
- Built-in safety lock to prevent UV exposure.
- Compact — only 7-5/8" x 2-7/8" x 2"
- Complete with holding tray for 4 chips.

UVS-11EL Replacement Bulb $16.95

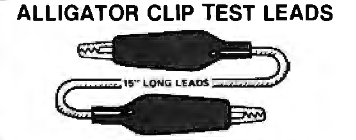
UVS-11E $79.95

JOYSTICKS



JS-5K	5K Linear Taper Pots	$5.25
JS-100K	100K Linear Taper Pots	$4.95
JVC-40	40K (2) Video Controller in case . . .	$4.95

ALLIGATOR CLIP TEST LEADS



Heavy-duty leads, color coded, insulated alligator clip on each end. 15" long. Two each black, red, blue, white and yellow.

#ALCP (10 per pack) . . . . $2.95/pkg.

NEW!

JE215 Adjustable Dual Power Supply

General Description: The JE215 is a Dual Power Supply with independent adjustable positive and negative output voltages. A separate adjustment for each of the supplies provides the user unlimited applications for IC current voltage requirements. The supply can also be used as a general all-purpose variable power supply.

FEATURES:
- Adjustable regulated power supplies, pos. and neg. 1.2VDC to 15VDC.
- Power Output (each supply): 5VDC @ 500mA, 10VDC @ 750mA, 12VDC @ 500mA, and 15VDC @ 175mA.
- Two, 3-terminal adj. IC regulators with thermal overload protection.
- Heat sink regulator cooling
- LED "on" indicator
- Printed Board Construction
- 120VAC Input
- Size: 3-1/2"w x 5-1/16"L x 2"H

JE215 Adj. Dual Power Supply Kit (as shown) . . $24.95

(Picture not shown but similar in construction to above)

JE200 Reg. Power Supply Kit (5VDC, 1 amp) . .	$14.95
JE205 Adapter Brd. (to JE200) ±5,±9 & ±12V.	$12.95
JE210 Var. Pwr. Sply. Kit, 5-15VDC, to 1.5amp.	$19.95

MICROPROCESSOR COMPONENTS

8080A/8080A SUPPORT DEVICES

INS8080A	CPU	4.95
DP8212	8-Bit Input/Output	3.25
DP8214	Priority Interrupt Control	5.95
DP8216	Bi-Directional Bus Driver	3.49
DP8224	Clock Generator/Driver	3.95
DP8226	Bus Driver	3.49
DP8228	System Controller/Bus Driver	4.95
DP8238	System Controller	5.95
INS8243	I/O Expander for 48 Series	9.95
INS8250	Asynchronous Comm. Element	16.95
DP8251	Prog. Comm. I/O (USART)	6.95
DP8253	Prog. Interval Timer	9.95
DP8255	Prog. Peripheral I/O (PPI)	5.95
DP8257	Prog. DMA Control	9.95
DP8259	Prog. Interrupt Control	9.95
DP8275	Prog. CRT Controller	39.95
DP8279	Prog. Keyboard/Display Interface	9.95
DP8303	System Timing Element	6.95
DP8304	8-Bit Bi-Directional Receiver	3.95
DP8307	8-Bit Bi-Directional Receiver	3.95
DP8308	8-Bit Bi-Directional Receiver	3.95
DP8310	Octal Latched Peripheral Driver	5.25
DP8311	Octal Latched Peripheral Driver	5.25

6800/6800 SUPPORT DEVICES

MC6800	MPU	7.95
MC6802CP	MPU with Clock and RAM	14.95
MC6810API	128x8 Static RAM	4.95
MC6821	Peripheral Inter. Adapt (MC6820)	7.49
MC6828	Priority Interrupt Controller	17.95
MC6830L8	1024x8-Bit ROM (MC68A30-8)	14.95
MC6850	Asynchronous Comm. Adapter	6.95
MC6852	Synchronous Serial Data Adapter	6.95
MC6860	0-600bps Digital MODEM	10.95
MC6862	2400bps Modulator	12.95
MC6880A	Quad 3-State Bus. Trsvr. (MC8T26)	2.29

MICROPROCESSOR CHIPS

Z80 (780C)	CPU (MK3880N) (2MHz)	11.95
Z80A (780-1)	CPU (MK3880N-4) (4MHz)	13.95
CDP1802	CPU	19.95
2650	MPU	16.95
1OM2901AOC	CPU—4-Bit Slice (Com. Temp. Grade)	19.95
MCS6502	MPU w/Clock (65K Bytes Memory)	11.95
INS8035N-6	MPU—8-Bit (6MHz)	7.95
INS8039N-6	CPU—Sgl. Chip 8-Bit (128bytes RAM)	9.95
INS8040N-6	CPU (256 Bytes RAM)	24.95
INS8070N	CPU—64 Bytes RAM	24.95
INS8073N	CPU w/Basic Micro Interpreter	29.95
P8085	CPU	9.95
TMS9900JL	MPU—16-Bit	39.95

SHIFT REGISTERS

MM500H	Dual 25-Bit Dynamic	.50
MM503H	Dual 50-Bit Dynamic	.50
MM506H	Dual 100-Bit Static	.50
MM510H	Dual 64-Bit Accumulator	.50
MM1402N	256-Bit Dynamic	2.95
MM5013N	1024-Bit Dynamic/Accumulator	1.95
MM5016H	500/512-Bit Dynamic	1.95
MM5034N	Octal 80-Bit	9.95
MM5035N	Octal 80-Bit	9.95
2504V (1404A)	1024-Bit Dynamic	1.95
2518N	Hex 32-Bit Static	3.95
2522V	Dual 132-Bit Static	2.95
2524V	512-Bit Dynamic	.99
2525V	1024-Bit Dynamic	2.95
2527V	Dual 256-Bit Static	2.95
2528V	Dual 250-Bit Static	4.00
2529V	Dual 240-Bit Static	4.00
2532N	Quad 80-Bit Static	2.95
3341PC	Fifo (Dual 80)	6.95

DATA ACQUISITION

AF100-1CN	Universal Active Filter 2.5%	5.95
AF121-1CJ	Touch Tone Low Band Filter	19.95
AF122-1CJ	Touch Tone High Band Filter	19.95
LM308CH	Super GainOp Amp	1.15
LM334Z	Constant Current Source	1.30
LM335Z	Temperature Transducer	1.40
LF356N	JFET Input Op Amp	1.10
LF398N	Sample & Hold Amplifiers	3.95
LM399H	Temp.Comp. Prec. Ref. (.5ppm/C°)	5.00
ADC0804LCN	8-Bit A/D Converter (1 LSB)	4.95
DAC0806LCN	8-Bit D/A Converter (0.78% Lin.)	2.25

DATA ACQUISITION (CONTINUED)

ADC0809CCN	8-Bit A/D Converter (8-Ch. Multi.)	5.25
ADC0817CCN	8-Bit A/D Converter (16-Ch. Multi.)	10.95
DAC1000LCN	10-Bit D/A Conv. Micro. Comp. (0.05%)	13.95
DAC1008LCN	10-Bit D/A Conv. Micro. Comp. (0.20%)	8.95
DAC1020LCN	10-Bit D/A Converter (0.05% Lin.)	8.49
DAC1022LCN	10-Bit D/A Converter (0.20% Lin.)	5.95
DAC1222LCN	12-Bit D/A Converter (0.20% Lin.)	9.95
CD4051N	8-Channel Multiplexer	1.19
AY-5-1013	30K BAUD UART	6.95

RAM'S

1101	256x1 Static	1.49
1103	1024x1 Dynamic	.99
2101 (8101)	256x4 Static	3.95
2102	1024x1 Static	1.75
21L02	1024x1 Static	1.95
2111 (8111)	256x4 Static	3.95
2112	256x4 Static MOS	4.95
2114	1024x4 Static 450ns	3.25
2114L	1024x4 Static 450ns Low Power	3.49
2114-2	1024x4 Static 200ns	3.95
2114L-2	1024x4 Static 200ns Low Power	4.95
74S200	256x1 Static	6.95
4116N-4 (UPD416)	16K Dynamic 250ns (MM5290N-4)	2.95
4164N-3	64K Dynamic 200ns	19.95
MM2147J	4096x1 Fast 70ns	7.95
5101	256x4 Static	7.95
MM5261	1024x1 Dynamic Fully Decoded	.99
MM5262	2Kx1 Dynamic	.49
MM5280/2107	4096x1 Dynamic	4.95
MM5290N-2 (4116)	16K Dynamic 150ns (UPD416C-3)	3.95
MM5298J-3A	8K Dyn. 200ns (lower½ of MM5790J)	1.95
HM6116-4	16K (2Kx8) Static 200ns	14.95
82S25	64 Bit RAM (16x4OC)	3.49
UPD414/MK4027	4K Dynamic 16-pin	4.95
TMS4044-45NL	4K Static	9.95
TMS4045	1024x4 Static	9.95

PROMS/EPROMS

1702A	2K UV Erasable PROM	6.95
2708	8K EPROM	4.95
TMS2716	16K EPROM (-5V, +5V, +12V)	9.95
2716Intel(2516)TI	16K EPROM (Single +5V)	8.95
2732Intel TI	32K EPROM	17.95
2758	8K EPROM (450ns) (Single +5V)	7.49
2764Q	64K EPROM (Hitachi HN462764)	49.95
5203	2048 PROM	14.95
82S23(74S188)	32x8 PROM (Open Collector)	3.95
82S115	4096 Bipolar PROM	14.95
82S123(74S288)	32x8 Tri-State Bipolar PROM	3.95
82S185	8K PROM	16.95

— Over 30 More PROMS Listed in Our Catalog —

ROM'S

2513(2140)	Character Generator (Upper Case)	9.95
2513(3021)	Character Generator (Lower Case)	9.95

NMOS READONLY MEMORIES

MCM66710P	128x9x7 ASCII Shifted w/Greek	13.50
MCM66740P	128x9x7 Math Symbol & Pictures	13.50
MCM66750P	128x9x7 Alpha. Control Char. Gen.	13.50

MICROPROCESSOR MANUALS

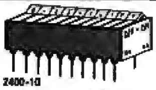
M-Z80	User Manual	7.50
M-CDP1802	User Manual	7.50
M-2650	User Manual	5.00

SPECIAL FUNCTION

DS0025CN	Dual MOS Clock Driver (5MZ)	3.50
DS0026CN	Dual MOS Clock Driver (5MZ)	1.95
INS1771N-1	Floppy Disc Controller	24.95
INS2651N	Communication Chip	19.95
MM58167N	Microprocessor Real Time Clock	8.95
MM58174N	Microprocessor Compatible Clock	11.95
COP402N	Microcontroller with 64-Digit RAM and Direct LED Drive	6.95
COP402MN	Microcontroller with 64-Digit RAM & Direct LED Drive w/N Buss Int.	7.49
COP470N	32-Seg. VAC Fluor. Driver (20-pin pkg.)	3.25

TELEPHONE/KEYBOARD CHIPS

AY-5-9100	Push Button Telephone Dialer	14.95
AY-5-9200	Repertory Dialer	14.95
AY-5-9500	CMOS Clock Generator	4.95
AY-5-2376	Keyboard Encoder (88 keys)	11.95
HD0165-5	Keyboard Encoder (16 keys)	7.95
74C922	Keyboard Encoder (16 keys)	5.49
74C923	Keyboard Encoder (20 keys)	5.75
MM53190N	Push Button Pulse Dialer	7.95
MM57499N	96/144-Key Serial Keyboard Encoder	8.95



2400-10

EECO Rocker DIP Switch — "Mini-Dip™" 2400 Series

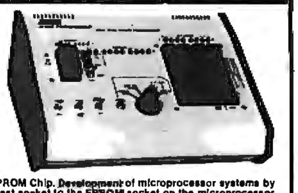
THE MOST UNIQUE DIP SWITCH AVAILABLE!

MINI-DIP is designed to retrofit all major brands of Dip switches. Unique features include locking rod design to prevent accidental actuation and gold self-wiping contact. One-piece housing and press-fit terminals prevent contamination. 2-10 station Form "A" and 1-5 station Form "C." • Terminals on .100 x .300 (2.54 x 7.62) centers • PCB or dip socket mountable • Positive cleaning/wiping action with gold contact • Total seal and bottom seal

Part No.	Pos.	Configuration	Socket	Price	Part No.	Pos.	Configuration	Socket	Price
2400-2	2	12	8 pin	.79 - 10/ 6.95	2400-6	6	123456	14 pin	1.09 - 10/ 9.95
2400-3	3	123	8 pin	.89 - 10/ 7.95	2400-7	7	1234567	14 pin	1.19 - 10/10.95
2400-4	4	1234	8 pin	.99 - 10/ 8.95	2400-8	8	12345678	16 pin	1.29 - 10/11.95
2400-ABCD	4	ABCD	8 pin	.99 - 10/ 8.95	2400-9	9	123456789	18 pin	1.39 - 10/12.95
2400-5C	6	C54321	14 pin	1.09 - 10/ 9.95	2400-10	10	0123456789	20 pin	1.49 - 10/13.95

JE608 PROGRAMMER

2704/2708 EPROM PROGRAMMER



GENERAL APPLICATIONS:
- To program EPROMS 2704 and 2708.
- Developmental system for microcomputer circuits
- To read the contents of a pre-programmed EPROM
- To compare EPROM(s) for content differences
- To emulate a programmed EPROM
- To store program in RAMS for alterations
- Three separate Display Registers: 8 LED's for Hex Key entries, 10 LED's (2⁸·2⁹) for Address Register and 8 LED's for Data Memory Register. The Data Memory Register displays the content of the RAMs from the EPROM Chip. Development of microprocessor systems by means of a ribbon cable from the programmer panel test socket to the EPROM socket on the microprocessor board. Rapid checking verification of programmed data changes. User may move data from a master to RAM's or write into RAM's with keyboard entries. Allows manual stepping manipulation (up and down) at any address location. Stand-alone EPROM Programmer consisting of: A 19-key Hexadecimal Keyboard assembly, Programmer Board assembly with 4 power supplies and a LED/Test Socket Panel Board assembly. The Test Socket is zero force insertion type. Power requirements: 115VAC, 60 Hz, 6W. Compact desk-top enclosure: Color-coordinated designer's case with light tan panels and molded end pieces in mocha brown. Size: 3¼"H x 11"W x 8¾"D. Weight: 5 lbs.

The JE608 EPROM Programmer is a completely self-contained unit which is independent of computer control and requires no additional systems for its operations. The EPROM can be programmed from the Hexadecimal Keyboard or from a pre-programmed EPROM. The JE608 Programmer can emulate a programmed EPROM by the use of its internal RAM circuits. This will allow the user to test or pretest a program for a system, prior to programming a chip. Any changes in the program can be entered directly into the memory circuits with the Hexadecimal Keyboard so that rewriting the entire program will not be necessary. The JE608 Programmer contains a Programmer/Board w/25 IC's & includes power supplies of: -5V, +5V, +12V and +26V. The Hexadecimal Keyboard and LED/Test Socket Panel board are separate assemblies within the system.

JE608K Kit $399.95

JE608A Assembled and Tested $499.95

JE608-16K ADAPTER BOARD FOR 2716/2758 EPROMS

GENERAL DESCRIPTION:
The JE608-16K Adapter Board allows the JE608 Programmer to be modified for the additional programming of the 2716 and 2758 EPROMS. The adapter provides for adding an address switch for the 2¹¹ bit and also for selecting the proper power and timing pulses to be applied to the EPROM. Programming and emulating the 2716 (16K) EPROM is done separately to each half (1024x8) of the EPROM because of the existing 8K RAM capacity in the JE608 Programmer.

JE608-16K	Adapter Board Kit	$29.95
JE608-Upgrade	(Send assembled JE608 to factory for adapter installation . . . . . . of the JE608-16K Adapter Board Kit)	$99.95
JE609A-16K Mod.	Assembled JE608 w/Adapter (JE608-16K) Installed	$599.95

$10.00 Min. Order — U.S. Funds Only
Calif. Residents Add 6% Sales Tax
Postage—Add 5% plus $1.50 Insurance

Spec Sheets — 25¢
Send 86¢ Postage for your
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BOOKS

National Semiconductor — Interall — Intel

30001	National CMOS Data Book . . . . (640 pages) 74C, CD4000, and A/D Converters	$6.95
30002	National Interface Data Book . . . . (704 pages) OP, DS8000, DS3600, DS75000, etc.	$6.95
30003	National Linear Data Book . . . . (1376 pages) LM, LF, ADC, DAC, LH Series	$8.95
30004	National Series 80 — Board Level Computer (224 pages) . .	$4.95
30005	National TTL Logic Data Book . . . . (624 pages) 7400, LS, L, H, S, and DM8000 Series	$8.95
30006	Buy above (3) 30001,3,5 as a set	$19.95/lot
30009	Interall Data Book (1074 pages)	$6.95
010400	Intel Component Data Catalog . . . . Full data sheets for Intel's products incl. memory devices, microproc., peripherals & indust./mil. products (1328 pages)	$10.00
206810	Intel Peripheral Design Handbook . . . . Full data sheets, appl. notes for Intel peripheral device components (644 pages)	$7.50

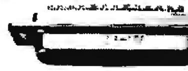
AC and DC Wall Transformers

With Universal Plug and 9V Battery Snap

Selective voltages: 6,9,12VDC. Polarity selection (+/-). six-foot line from adapter to plugs — six-inch line from adapter to battery snap. 120V/60Hz. 300mA.

Part No.	Input	Output	Price
AC 250	117V/60Hz	12VAC 250mA	$3.95
AC 500	117V/60Hz	12VAC 500mA	$4.95
AC1000	117V/60Hz	12VAC 1 amp	$5.95
AC1700	117V/60Hz	9VAC 1.7 amp	$3.95
DC6912	120V/60Hz	6,9,12VDC 300mA	$9.95
DV9200	117V/60Hz	9VDC 200mA	$3.25
DC900	120V/60Hz	9VDC 500mA	$3.95

CONNECTORS



DB25P	D-Subminiature Plug	$2.95
DB25S	D-Subminiature Socket	$3.50
D20418-2	Screw Lock Hdwr. (2) DB25S/P	2/$.99
DB51226	Cover for DB25P/S	$1.75
22/44SE	P.C. Edge (22/44 Pin)	$2.95
UG88/U	BNC Plug	$1.79
UG89/U	BNC Jack	$3.79
UG175/U	UHF Adapter	$ .49
SO239	UHF Panel Recp.	$1.29
PL258	UHF Adapter	$1.60
PL259	UHF Plug	$1.60
UG260/U	BNC Plug	$1.79
UG1094/U	BNC Bulkhead Recp.	$1.29

TRS-80 16K Conversion Kit

Expand your 4K TRS-80 System to 16K.
Kit comes complete with:
★ 8 ea. MM5290 (UPD416/4116) 16K Dyn. Rams (*NS)
★ Documentation for Conversion

TRS-16K2 *150NS	$29.95
TRS-16K3 *200NS	$24.95
TRS-16K4 *250NS	$19.95

JE610 ASCII Encoded Keyboard Kit

The JE610 ASCII Keyboard Kit can be interfaced into most any computer system. The kit comes complete with an industrial grade keyboard switch assembly (62-keys), IC's, sockets, connector, electronic components and a double-sided printed wiring board. The keyboard assembly requires +5V @ 150mA and −12V @ 10 mA for operation. Features: 60 keys generate the 126 characters, upper and lower case ASCII set. Fully buffered. Two user-define keys provided for custom applications. Caps lock for upper-case-only alpha characters. Utilizes a 2376 (40-pin) encoder read-only memory chip. Outputs directly compatible with TTL/DTL or MOS logic arrays. Easy interfacing with a 16-pin dip or 18-pin edge connector. Size: 3½"H x 14½"W x 8¾"D

JE610/DTE-AK (After assembled as pictured above) . . . **$124.95**

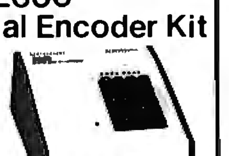
JE610 Kit 62-Key Keyboard, PC Board, & Components (no case) . . . . . **$ 79.95**

K62 62-Key Keyboard (Keyboard only) . . . **$ 34.95**

DTE-AK (case only — 3¼"Hx11"Wx8¾"D) **$ 49.95**

NEW! JE212 — Negative 12VDC Adapter Board Kit for JE610 ASCII KEYBOARD KIT
Provides -12VDC from incoming 5VDC . . $9.95

JE600 Hexadecimal Encoder Kit



FULL 8-BIT LATCHED OUTPUT 19-KEY KEYBOARD

The JE600 Encoder Keyboard Kit provides two separate hexadecimal digits produced from sequential key entries to allow direct programming for 8-bit microprocessor or 8-bit memory circuits. Three additional keys are provided for user operations with one having a bistable output available. The outputs are latched and monitored with 9 LED readouts. Also included is a key entry strobe. Features: Full 8-bit latched output for microprocessor use. Three user-define keys with one being bistable operation. Debounce circuit provided for all 19 keys. 9 LED readouts to verify entries. Easy interfacing with standard 16-pin IC connector. Only +5VDC required for operation. Size: 3½"H x 8¾"W x 8¾"D

JE600/DTE-HK (After assembled as pictured above) **$99.95**

JE600 Kit 19-Key Hexadec. Keyboard, PC Board & Cmpnts. (no case) . . **$59.95**

K19 19-Key Keyboard (Keyboard only) **$14.95**

DTE-HK (case only —3½"Hx8¾"Wx8¾"D) **$44.95**

ADVANCED COMPUTER PRODUCTS

16K UPGRADE ONLY $24.95 SPECIFY COMPUTER

7400

SN7400N	.19	SN74123N	.59
SN7401N	.22	SN74125N	.39
SN7402N	.22	SN74126N	.44
SN7403N	.22	SN74128N	.59
SN7404N	.22	SN74132N	.69
SN7405N	.23	SN74136N	.75
SN7406N	.23	SN74139N	.95
SN7407N	.23	SN74141N	.79
SN7408N	.26	SN74142N	2.95
SN7409N	.23	SN74143N	2.95
SN7410N	.22	SN74144N	2.95
SN7411N	.29	SN74145N	.62
SN7412N	.29	SN74147N	1.95
SN7413N	.39	SN74148N	1.20
SN7414N	.59	SN74150N	1.09
SN7416N	.29	SN74151N	.67
SN7417N	.29	SN74152N	.67
SN7420N	.22	SN74153N	.67
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SN7483N	.55	SN74198N	1.39
SN7485N	.65	SN74199N	1.39
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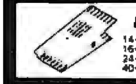

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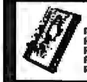

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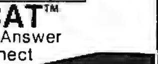

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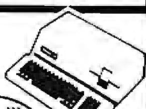

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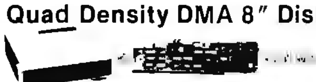

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V-1000 Vista "V-DRIVE"

Qume. DATATRAK 8

THE LAST WORD IN 8" FLOPPY-DISK ENCLOSURES

The VISTA V-1000 FLOPPY DISK DRIVE SUBSYSTEM • Deluxe chassis with internal slide easy access for drive positioning and mounting • Built to mechanically and electrically accommodate single sided drives—including the most popular 8-inch Winchester and Shugart floppy disk drives, and 8-inch streaming tape units • Storage capacity from 0.5 to 40 megabytes • Industrial quality cabinet with die cast front bezel • Meets all UL and OSHA standards • Additional Savings! Front and rear frame rail mounts provided at no extra charge (no extrusion slides) • Desk or rack mountable • Features modular construction with removeable sub-assembly that allows easy cabinet positioning and mounting • Drives pull out for easy service and maintenance

DISCOUNT PRICES

CABINET	$ 395
CABINET with (2) single sided drives (including power supply & cable)	$1495
CABINET with (2) double sided drives (including power supply & cable)	$1995

Vista V-80 5¼" DISK

FOR TRS 80® MODEL I, PMC 80, ZENITH H89, S-100, etc.

ONLY 310⁰⁰ ea.

MODEL V-801, 80 TRACKS, SS

ONLY 425⁰⁰ ea.

2 DRIVE CABLE 29.95 4 DRIVE CABLE 39.95

MOSTEK MK4015 4K Dynamic RAM

Refresh while supply lasts only .49¢

Pin equivalent to MK4027 except has 1 ms.

S-100 WW

$2.99 each

FIRST QUALITY AT SURPLUS PRICE

2708 EPROMS

PRIME-450 Ns.

8 for $29.95

4K STATIC RAM SELL-OFF

Zilog 6104-4

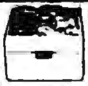
Same as TMS 4044 but designed specifically for Z-80 based systems. This is full-spec 4K × 1 RAM, 450 Ns.

While supply lasts $1.49 each.

SPECIAL PURCHASE

$59.95 Limited Supply $59.95

16K Altair RAM Boards Fully Populated as is.



FLOPPY DISK DRIVES

OUME® Datatrack 8
• Double Sided
• Double Density

ACP LOW PRICE $569.95

Tandom TM100-1 5¼" Disk Drive	249.95
MPI B51-5¼", 40 tracks	239.95
Shugart SA400-5¼" 35 tracks	295.00
Shugart 800/801R 8"	449.00
Siemens Shugart Compatible Model FDD-120-8D	429.00
PERSCI Model 277 Dual	1195.00
MPI 852 5¼" Dual	348.00
WANGO/SIEMENS 82	290.00
MPI 91 Double Track Density Single Side, 80 Tracks	375.00
MPI 92 Double Track Density Double Side, 160 Track	475.00

6800 MICROMODULE™ PRICE LIST

MODELNO	DESCRIPTION	PRICE
9600A	Single Board Microcomputer	$495.00
9609	Advanced Single Bd. Comp (6809)	595.00
9601	16 Slot Mother Board	175.00
9602	Card Cage	75.00
9603	8 Slot Mother Board	100.00
9604	Power Supply	275.00
9605	DC Input Power Supply	325.00
9610	Utility Proto Board	39.00
9611	Arith. Proc/Memory Module	495.00
9612	Buffered Utility Proto Board	49.00
9616	32K EPROM/RAM Module	250.00
9617	EPROM Programming Head	250.00
9620	16 Channel Parallel I/O Module	295.00
9622	Serial-Parallel I/O Module	325.00
9627	16K Static RAM Module 470ns	395.00
9629	32K Static RAM 450ns	695.00
9629A	32K Static RAM 200ns	895.00
9630	Card Extender	68.00
9640	Multiple Programmable Timer	395.00
9650	8 Channel Duplex Serial I/O Mod.	395.00
9655	Intelligent Tape Controller	550.00
96103	32/32 I/O Module	275.00
96702	Contact Closure Module	350.00

UNPOPULATED BOARDS (Also Available)

$24.95 TRS-80/APPLE $24.95

MEMORY EXPANSION KITS.
4116's, 16K (200/250 ns.)

16K — 8 pcs for $24.95 — Specify Computer — RAM

Call For Volume Pricing

CENTRONICS PRINTER

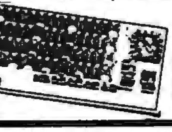
Model 737

• Centronics complete printer
• The 737 has everything Check and compare the features
• New low price **$835.00**

32K STATIC RAM BOARD

2 or 4 MHz Expandable uses 2114L's

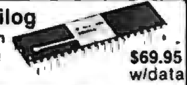
S-100



16K 4 MHz Kit	159.95
16K 4 MHz A&T	217.95
32K MHz Kit	289.95
32K 4 MHz A&T	339.00
Bare Board	39.95
Bare Bd. w/all parts less mem	99.95

NEW! from Zilog

Z-8 CPU comes with Tiny Basic & debug program on the I.C.



$69.95 w/data

BIPOLAR CPU SALE

Signetics 8 × 300 8 bit CPU

While stock lasts 14.95 ea.

UV "Eprom" Eraser

Model UVs-11E $69.95

Model S-52T... $325.00

NON-LINEAR SYSTEMS, INC. NLS

TOUCH-TEST 20

DIGITAL MULTIMETER $319⁹⁵

BECKMAN DIGITAL MULTIMETERS

AS LOW AS 100⁰⁰

TECH 300 Digital Multimeter	$110
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DC-202 Deluxe Carrying Case	$24
HV-211 High Voltage Probe	$35
RP-221 RP Probe	$35
CT-231 AC Current Clamp	$42
DL-241 Deluxe Test Lead Kit	$10
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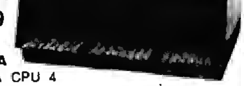
The Preferred S-100 Box

The new Series II CPU Board features a 4 MHz Z-80A CPU and full-feature front panel. 20-slot actively terminated mother-board, with 25 amp power supply (50/60 Hz operation, incl. 68 cfm fan).

DPS-1, List **$1795**

ACP Price **$1499**



SYSTEM 2A with Z-80A CPU 4 MHz, 64K RAM, I/O Board, 20 slots, front panel, double density disk controller board. Full 1-year warranty.

List **$3795** ACP Price **$2995**

NEC PC-8000 Series Microcomputer System.

NEW INTRO PRICING $1099.00

• Z-80A CPU 4 MHz
• 5 user programmable function keys
• 82 Keys with numeric keypad
• 160x100 resolution
• 80 character screen

PC-8001A Microcomputer w/32KRAM	$1295.00	1099.00
PC-8012A I/O Unit w/32K RAM, Expansion slots	795.00	699.00
PC-8031A Dual Mini Disk Drive Unit	1295.00	1099.00
PC-8032A Add-On Dual Mini-Disk Drive Unit	1095.00	949.00
PC-8023A Impact Matrix Printer, Tractor/Friction Feed	860.00	769.00
PC-8094A Cable for PC-8023A Printer	49.95	44.95
JB-1201M(A) High Resolution Green Monitor	265.00	239.00
JC-1202DH(A) High Resolution Color Monitor w/RGB Input	1195.00	1049.00
PC-8091A RGB Cable for JC-1202DH(A) Color Monitor	19.95	17.95
Basic Language Learning Guide		19.95
PC-8001A Microcomputer Reference Manual		19.95
PC-8012A I/O Unit User's Manual		14.95
PC-8031A Dual Disk User's Manual		14.95

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Z8001 16 bit to 8Mb	$189.00
Z8002 16 bit to 64K	149.00
Z80	9.95
Z80A	13.95
F-8 (3850)	16.95
2650	16.95
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8080A	4.75
8080A-4MHz	19.95
SALE 8085	14.95
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2903 4-bit Superslice	29.95
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6502	9.95
6502A	16.95
IM6100	29.95
6800	11.75
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6802P	17.95
8035	14.95
8039	19.95
INS 8073N	24.95
8755	49.95
8748	69.95
6809	37.95
8088	69.95

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AM9511 Arith. Processor	175.00
9512 Arith Processor	175.00
9513 Univ Timing	79.95
AM9517DMA Controller	18.95
AM9519Universal Interrupt	18.95

Z-80 SUPPORT CHIPS

Z80-PIO	2.5 MHz	8.75
Z80A-PIO	4.0 MHz	12.95
Z80-CTC	2.5 MHz	8.75
Z80A-CTC	4.0 MHz	12.95
Z80-DMA	2.5 MHz	29.95
Z80A-DMA	4.0 MHz	36.95
Z80-SIO/0	2.5 MHz	35.95
Z80A-SIO/0	4.0 MHz	39.40
Z80-SIO/1	2.5 MHz	35.95
Z80A-SIO/1	4.0 MHz	39.40
Z80-SIO/2	2.5 MHz	35.95
Z80-SIO/2	4.0 MHz	39.40

8080/8085 SUPPORT

8155/8156 I/O	24.95
8755 I/O with Eprom	84.95
8202 Dyn Ram Cont.	34.95
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8224 ClockGen	2.95
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8228 Sys. Control	4.50
8238 Sys.Cont	5.50
8243 I/OExp.	9.50
8250 Asyn Comm	15.95
8251 Prog I/O	6.95
8253 Int Timer	12.95
8255 Prog I/O	6.50
8257 Prog DMA	16.95
8259 Prog. Int.	15.95
8275 CRT Controller	45.95
8279 Prog Keyboard	15.95

6800 SUPPORT CHIPS

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6821	6.50
6828 Priority Int.	10.75
6834-1 512 x 8 Eprom	16.95
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6847Color CRT	29.95
6850ACIA	5.95
6852 Serial Adapter	5.95
6860 Modem	10.95
6862 Modulator	11.95
6871A 1.0MHz OSC	25.95
8875	6.95
6880 Bus Driver	2.19
MC68488	19.95
68047	24.95

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6522 Mult.	11.95
6530-002.003.004.005	21.95
6532	19.95
6551	19.95

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We do Custom Programming

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82S123/5610/74S288(32x8)TS	4.25
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82S129/5623/74S287 (256x4)TS	4.25
82S130/5604/74S570(512x4)OC	6.50
82S131/74S571 (512x4)TS	8.95
82S137/74S573(1024x4)TS	12.95
82S141/3624/74S474 (512x8)TS	12.95
82S147/74S472 (512x8)TS	12.95
74S471/6309 (256x8)TS	7.95

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2764(8Kx8)TS	89.95
2732 (4Kx8)TS	18.95
2716/2516 5V (2Kx8)TS	8.95
TMS2716, ±5V.12V	17.95
2758.5V, (450NS)	7.50
2708 (450NS)	5.75
2708 (650NS)	5.25
1702A	5.75
MM5203AO	14.50
MM5204O	9.95

CHARACTER GEN.

2513-001 (5V) Upper	9.50
2513-005 (5V) Lower	10.95
2513-AOM3 (5V) Lower	14.95
MCM66710 Ascii Shifted	12.95
MCM66740 Math Symbol	13.45
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TR1602B (5V 12V)	3.95
AY51013 (5V 12V)	4.95
AY51014A 1612 (5-14V)	6.95
AY51015A-1863 (5V)	6.95
IM6402	7.95
IM6403	8.95
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1671B Astros	24.95
SALE TR1472B	8.95
MC14411	11.95
4702	14.95
WD1941	9.95
COM 5016	16.95
INS 8250	15.95

KEYBOARD ENCODERS

AY5-2376	13.75
AY5-3600	13.75

STATIC RAMS

SALE 2102 .89

	1-24	25-99	100
21L02 450ns	1.30	1.25	.99
21L02 250ns	1.59	1.55	1.15
2111	3.75	3.65	3.55
2112-1	2.95	2.65	2.65
2101-1	2.80	2.70	2.55
2114N (450NS.)	3.75	3.50	3.25
2114L-250ns (4045)	6.50	5.95	5.50
2114L-450ns. (4045)	4.75	4.25	3.95
4044 250ns	8.95	7.50	6.90
4044 450ns	5.95	5.35	4.75
EMM4200A	9.75	8.75	7.95
EMM4402	7.95	7.25	6.25
AMD9140/41	10.95	10.25	9.25
AMD9130/31	12.95	11.95	10.25
1101	1.95	1.75	1.25
P2125/93425 (45ns)	9.95	8.35	8.25
6518 1K x 1 CMOS	7.95	7.95	7.25
2147 Low Power 4K Static	9.95	8.95	6.95
93415	9.95	8.95	8.50

DYNAMIC RAMS

416/4116 16K (16 Pin)	2.49
Set of 8 416's 200 Ns	24.95
4115 8K (16 Pin)	2.49
4050 4K x 1 (18 Pin)	4.95
4060 4K x 1 (22 Pin)	4.95
4096 4K x 1 (16 Pin)	3.95
2104 4K x 1 (16 Pin)	4.75
40274K x 1 (16 Pin)/UPD414	4.95

5261	1.95	64K RAMS $19.95	4103	.95
5262	1.95		4008L	4.95
5270	4.95		6605	7.95
5280	4.95		6604	4.95
			6002	1.50

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# Pins	Lo Pro Solder Tail	Wire Wrap 3 Level Tin	Wire Wrap 3 Level Gold
8	12	32	45
14	19	36	59
16	20	36	62
18	24	59	84
20	29	69	99
22	24	79	1.10
24	38	85	1.20
28	43	1.10	1.49
36	58	1.25	1.69
40	60	1.40	1.89

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24 Pin $5.50 28 Pin $7.50 40 Pin $11.25

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Part no.	Size	Color	Description	Price
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DL707	300	Red	Comm Anode	99
FND357	357	Red	Comm Cathode	99
FND501	500	Red	Comm Cathode (+1)	99
FND503(500)	500	Red	Comm Cathode	99
FND507(510)	500	Red	Comm Anode	99
FND508	500	Red	Comm Anode (+1)	99
FND530	500	Green	Comm Cathode	1.49
FND550	500	Orange	Comm Cathode	1.49
FND803(800)	800	Red	Comm Cathode	1.75
FND810(810)	800	Red	Comm Anode	1.75
HP5082-7340	600	Red	4 x 7 Hexidecimal	25.95
HP5082-7300	600	Red	4 x 7 Sgl Digit RHD	18.95
HP5082-7731	300	Red	Comm Anode	75
TIL305	—	Red	Array 5 x 7	7.95
TIL308	270	Red	Numerical Display	10.95
TIL309	270	Red	Numerical Display	9.95
TIL311	270	Red	4 x 7 Hexidecimal	10.95
MAN2A	320	Red	Array	5.95
MAN6A	270	Red	Alpha Numeric	8.95
XAN3061	300	Red	Comm Anode Rght DP	1.25
XAN3062	300	Red	Comm Anode Left DP	1.25
XAN3063	300	Red	Overflow CA Left DP	1.25
XAN3064	300	Red	Comm Cathode Rght DP	1.25
XAN3051	300	Green	Comm Anode Rght DP	1.99
XAN3052	300	Green	Comm Cathode Left DP	1.99
XAN3053	300	Green	Overflow CA Left DP	1.99
XAN3054	300	Green	Comm Cathode Rght DP	1.99
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XAN3082	300	Yellow	Comm Anode Left DP	2.10
XAN3083	300	Yellow	Overflow CA Left DP	2.10
XAN3084	300	Yellow	Comm Cathode Rght DP	2.10

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82S0964x9 Ram	8.95
DP8304 Octal Driver	2.95
DAC86EX D/A Conv.	6.95
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MC6852 SSDA	3.49
MC10145 16x4 ECL Ram	4.50
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MK3853 Static Mem I/O	4.95
SN75136 .46 78M06	.49
MC10210 .89 79M06	.49
LM339 .79 74157	.49
LM710CN .29 74161	.49
LM711 CN .29 74C74	.39
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ICM 7207 Oscillator Controller	7.50
Seven Decade Counter 7208	18.95
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ICL 8211 Voltage Reference	1.95
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8700CJ 8 Bit A/D	9.95
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6604/VPD 414/4027/2660/MK 4096/4Kx1 Dynamic 16 Pin	1.95

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MC1372	8.95	RC 4131	2/1.00
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LM 377	1.25	COM 5037	49.95
LM380	1.25		

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100% CERTIFIED ERROR-FREE!

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525-10	10 Hole Hard NS Apple etc.	$29.95
525-16	16 Hole Hard Micropolis	$29.95

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577-01	Soft Sectored TRS 80 etc.	$32.25
577-10	10 Hole Hard NS Apple etc.	32.25
577-16	16 Hole Hard Micropolis	32.25

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FD850-01	Soft Double Sided Double Density 3740	49.00

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2143 ClockGen.	18.95

FLOPPY CHIP SET

Double Density
Double Sided Includes: 1797 1691 2143

$79.95/set

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8703 8 bit TS	13.50
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1408L8 8 bit	5.95
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DAC08	9.95
DAC 100	9.95

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AY38515 Color Converter	2.95
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AY38607-1 Shooting Gallery.	8.95
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SN76477 TISound Generator	3.95
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MM57100 NSC Color TV	6.95
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2517V	1.49	MM5060N	2.95
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2525	1.49	2847	4.95
2527	1.49	3341	4.95
2528	1.49	3351	17.95
2529	1.49	3357	6.95
2533	1.49	9403	24.95
3347	5.95	9408	9.95

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CTS206-5	1.75	CTS206-9	1.95
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S-100 Sound Board	$34.95
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Vector 8800 Proto	22.20
Vector 8803 11 slot MB	29.95
ACP Extender w/Conn	18.95
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S100(AY5-8910)Sound Bd.	34.95
Apple Sound Bd.	24.95

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MX-80 FT	595.00
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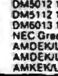
MX-70	425.00
Centronics 739	799.00
Vista V-300/25 cps	1495.00
V-300/45 cps	1795.00
Malibu 165	1995.00
Anadex 9500/9501	1450.00
Base II 800 MST	549.00

TERMINALS

TELEVIDEO

912C	[illegible]
920C	[illegible]
950C	[illegible]
AddS Viewpoint	$599
Ampex Dialog 80	$1025
Soroc IQ120	$609
IQ135	$899
IQ140	1149.00

SANYO MONITORS



VM4509 9" BW Sale Price	159.95
DM5012 12" B/W	239.00
DM5112 12" Green	249.00
DM6013 13" Color	415.00
NEC Green	259.00
AMDEK/LEEDEX Video 100	149.00
AMDEK/LEEDEX 13" Color	399.00
AMKEK/LEEDEX 12" Green	179.00

TERMS: Use check, M/C VISA AMEX CB or COD COD requires 25% deposit Charge Orders please include expiration date Foreign pay U.S. Funds. Order by phone, mail or TWX MINIMUM $10.00 Please include magazine issue and phone no. SHIPPING U.S.A. add $2.00 for first 2 lbs. For surface add 30¢ for additional lbs. For air add 70¢ for additional lbs. FOREIGN Add 10% shipping and handling COD's $1.85 extra. Not responsible for typos. Some items subject to prior sale. We reserve right to limit quantities, some items subject to precious metal adder. Retail pricing may vary from Mail Order. We reserve the right to substitute manufacturer.

RETAIL STORES OPEN MON-SAT

STORE #1: 1310 "B" E. Edinger, Santa Ana, CA 92705 Showrooms, Retail, Warehouse
STORE #2: 542 W. Trimble Road, San Jose, CA 95131 • (408) 946-7010

**Retail prices may vary.

P.O. Box 17329 Irvine, Calif. 92713

Direct Order Lines: (714) 558-8813

(800) 854-8230 or (800) 854-8241

FOR INTERNATIONAL ORDERS:
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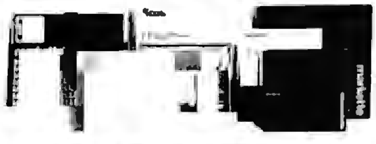
Santa Ana, CA 92705 TWX: 910-595-1565

Circle 10 on inquiry card.

California Digital

Post Office Box 3097 B • Torrance, California 90503



DISKETTES

FREE PLASTIC LIBRARY CASE INCLUDED WITH THE PURCHASE OF EVERY BOX OF DISKETTES

[illegible] And of course, [illegible] library case is included with every box [illegible]. MAD-CDM01(10) Please specify computer or required sectors.

$24.95 BOX

Ten boxes $22.75 One hundred boxes $21.50

MINIDISKETTES	Box	10 boxes		Box	10 boxes
[illegible] 3(0)	$27.00	$25.00	Scotch 744(0)(10)(16)	$31.00	$29.00
[illegible] 525(01)(10)	28.00	27.00	Dysan	45.00	43.00

[illegible]	Scotch	box	10 bx.	Dysan	box	10 bx.	MRX	box	10 bx.
[illegible] den.	740-0	$35.	$33.	3740/1	$48.	$47.	3060	$ 5.	$.3.
[illegible] den.	741-0	45.	43.	3740/1d	75.	73.	3090	37.	35.
[illegible]	740-33	35.	33.	na.			na.		
[illegible]	743-0	65.	59.	na.			3115	49.	

[illegible] brand head cleaning kit. $24.95 MMA-CK(5)(8) please specify 5 1/4 8"
[illegible] available on request for: tape, cartridges, diskpacks, volumn diskettes.

26 Megabyte Hard Disk Drive from GEORGE MORROW'S Thinker Toys

$3495

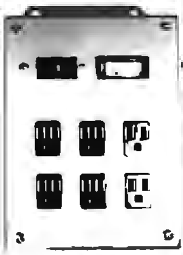
Other Morrow Products	
Addition al hard disk	[illegible]
Discus 2D 1 drive	[illegible]
Discus 2D 2 drives	1027
Discus 2+2 1 drive	[illegible]
Discus 2+2 2 drives	2247
Disk Jockey 2D controller	
Disk Jockey 1 Controller	
M26 hard disk Controller	
Switchboard Interface	
New [illegible]	
M-10 [illegible]	

NEW ZENITH GREEN PHOSPHOR MONITOR

The new Zenith ZVM-121 features a P31 green phosphor tube along with 15 MHz bandwidth. Switch selectable for 40/80 character screen. Fully compatable with 80 column Apple cards. VDM-Z121 30 lbs.

$119

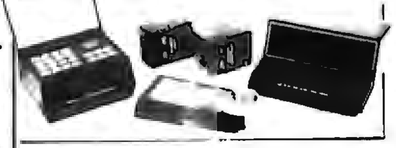
10+ $109 100+ $99



POWER STATION $99

Two Stage Noise Filter
Surge Suppressor
Line VoltageMeter

The Power House eliminates interference caused by noise generating motors and office machines. This product is a must for anyone who has experienced a power fault while operating a computer. Double filtering circuitry eliminates both high and low frequency line noise. Suppression de[illegible] clip voltage spikes above 130 VAC. Volt meter monitors RMS line voltage. Six power [illegible]cle three filtered. Constructed in water [illegible] industrial enclosure. [illegible] 12 lbs.



BSR SYSTEM X-10

The new BSR timer runs your home just like clockwork. Turns on lamps and appliances while your away from home. Completely compatible with your existing System X-10 devices.

BSR Timer eight channel	$65.00
Master control console	34.95
Ultrasonic Controller	19.95
Appliance Module 500 W.	$13.95
Lamp Module 300 Watts	13.95
NEW full control wall switch	14.50

MEMORY

64K DYNAMIC	16K STATIC
$11.95	$13.95
4164 100-$9.75	2167 200ns.
16K DYNAMIC	**2716 EPROM**
$2.10	$4.95
4116 100-$1.85	100-$4.50 1K-$4.00

2732 EPROM SALE $8.95

STATIC

	ea.	32+	100+	1K+
21L02 450ns.	1.19	1.05	.99	
21L02 250ns	1.49	1.45	1.39	
2114L4 450ns	3.95	2.95	2.75	2.50
2114L3 300ns	4.25	3.75	3.00	2.75
4044-4 450ns	4.95	4.50	4.25	4.00
4044-2 250ns	5.50	4.95	4.50	4.35
5257-3 300ns	4.47	4.25	4.05	3.75

EPROM

	ea.	32+	100+	1K+
2708 450ns	4.95	4.50	3.75	3.25
2716 5V.	4.95	4.50	4.00	
2716 tri-volt	9.95	9.00	8.25	7.50
2732 Intel	9.00	9.50	8.00	
2532 TI	21.50	19.00		
2764	*			

Shugart Associates

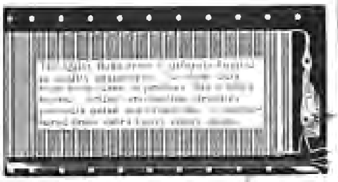
$395

801/ R Disk Drive 15 lbs.

Shugart 801/R with CP 206 power supply, muffin exhaust fan, complete in dual enclosure with all the necessary harnessing cables. Documentation included. 36 pounds. MSD-1801 **$795**

Same as above but with two Shugart 801R disk drives. 39 pounds. MSD-2801 **$1195**

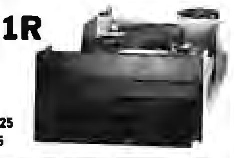
Disk drive cable. 6 foot 50 conductor with edge card connector at both ends. WCA-830S $25.00
Export Disk drives. 220V. 50MHz add $50.00 per disk drive.



S-100 Mother Board $35

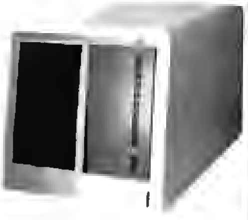
Quiet Buss

IMSAI 18 Slot CAL-M18



SHUGART 801R $395

Shugart 851R Double Sided ... $525
QumeDT8 Double Sided ... $495



NEW from Shugart Technology 5 Megabyte Hard Disk Drive

Packaged in the same physical size as the industry standard 5 1/4" minifloppy disk drive. The micro-Winchester stores thirty times as much data (6.38 megabytes unformatted), accesses data twice as fast (170 milliseconds) and transfers data twenty times faster (5.0 megabits per second.)

The ST506 is factory sealed to protect the media from environmental contaminates. Requires only DC voltage.

Dual California Digital 5 1/4" enclosure. ST506 drive and power supply. **$1500**

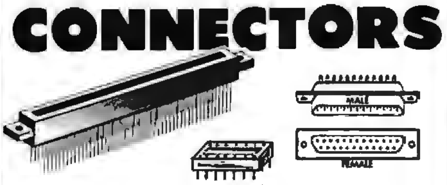
Shugart Associates SA100 removable media disk drive for above package. add: **$300**

SWITCHES

DIP SWITCHES pos.	ea.	100+	1K+
4	.88	.75	.69
7	.90	.83	.79
8	1.05	.91	.87
12	1.10	.99	.91

TOGGLE		ea.	100+
7101	on/on	1.39	.98
7103	on/off/on	1.39	1.19
7107	[illegible]	1.39	1.19
7108	[illegible]	1.39	1.19
7205	dpdt [illegible]	1.85	1.85

CONNECTORS



GOLD EDGE CONNECTORS	each	10+
S-100 .125 [illegible]		
Imsai solder .250" [illegible]	$2.95	$2.50
Imsai wire wrap (TI)	3.95	3.50
Sullins Hi-Rel. .250'	4.60	4.00
Sullins Hi-Rel. W/W	5.35	4.90
Sullins / Altair .140'	4.95	4.50
.156' Centers [illegible]		
22/44 Kim Eyelet	2.40	2.15
36/72 Digital Group S/T	5.95	5.30
36/72 Digital Group W/W	6.60	6.15
43/86 Motorola 6800S/T	6.60	6.15
43/86 Moto. 6800 W/W	7.00	6.85

INTEGRATED CIRCUIT SOCKETS	Low Profile each	100+	Wire Wrap each	100+
8 pin	$.10	$.09	$.18	$.11
14 pin	.10	.09	.17	.41
16 pin	.12	.11	.50	.41
18 pin	.15	.14	.60	.61
24 pin		.24	.84	.87
40 pin	.42	.40	1.60	1.47

D Type	each	10-24	25+
DB25P male	$1.60	$1.40	$1.30
DB25S female	2.35	2.00	1.90
DE hood	1.50	1.35	1.20
DA15P male	2.45	2.15	2.00
DA15S female	4.25	3.10	4.90
DA hood 2/P	1.60	1.35	1.30
DB25P male	2.50	2.45	2.25
DB25S female	3.35	3.15	3.05
DB hood 2/P	1.45	1.15	1.05
DC37P male	4.20	4.00	3.70
DC37S female	6.00	5.75	5.50
DC hood 2/P	2.25	2.00	1.75
DD50P male	5.50	5.10	4.75
DD50S female	9.40	8.60	8.00
DD50 hood 2/P	2.60	2.10	2.10
CENTRONIX			
[illegible]	7.95	6.75	5.7
RIBBON CABLE CONNECTORS			
17/14 5" disk	[illegible]	[illegible]	[illegible]
20 40 [illegible]	[illegible]	[illegible]	4.70
40	[illegible]	[illegible]	5.00

direct connect MODEM

Your Choice $169

Direct connect [illegible] Choose either of these two [illegible]

The Universal Data Systems 103LP is switch selectable between answer and originate modes. Fully Bell 103 compatible. Directly connects to the new modular telephone jack. 100% powered from the telephone line. No need to locate modem in proximity to A.C. power receptacle. MOD-103LP 3 pounds.

Novation [illegible] connects to most of the new "Bell" modular handsets. Ideal for [illegible] telephones. Requires external A.C. power. MOD-[illegible]

Universal Data Auto Answer 103LPJ $219
Novation Auto Cat RS232 $239

Regulated Power Supply 5 VOLT 5 AMP $11.95

[illegible]

VISA

master charge

All merchandise sold by California Digital is premium grade.
Shipping: First five pounds $2.00; each additional add $.40
Foreign orders 10% shipping. Excess will be refunded.
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Warehouse: 15608 Inglewood Blvd. Visitors by appointment.

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TWX 910 325-6212

16K Memory

4116-200ns **8/15.95**

ALL MERCHANDISE 100% GUARANTEED!

CALL US FOR VOLUME QUOTES

EPROMS

			Each	8 pcs
1702	256 x 8	(1 ns)	4.95	4.50
2708	1024 x 8	(450ns)	2.99	2.75
2758	1024 x 8	(5V) (450ns)	9.95	8.95
TMS2516	2048 x 8	(5V) (450ns)	6.95	5.95
2716	2048 x 8	(5V) (450ns)	5.50	4.95
2716-1	2048 x 8	(5V) (350ns)	9.00	8.50
TMS2716	2048 x 8	(450ns)	9.95	8.95
TMS2532	4096 x 8	(5V) (450ns)	12.95	11.95
2732	4096 x 8	(5V) (450ns) (200ns)		CALL
2764	8192 x 8	(5V) (450ns)		CALL

DYNAMIC RAMS

				100 pcs
4027	4096 x 1	(250ns)	2.50	2.00
4116-120	16,384 x 1	(120ns)	8/29.95	CALL
4116-150	16,384 x 1	(150ns)	8/18.95	1.95
4116-200	16,384 x 1	(200ns)	8/15.95	1.80
4116-300	16,384 x 1	(300ns)	8/14.95	1.75
4164	64,536 x 1	(200ns)		CALL

STATIC RAMS

				100 pcs
2101	256 x 4	(450ns)	1.95	1.85
2102-1	1024 x 1	(450ns)	.89	.85
21L02-4	1024 x 1	(LP) (450ns)	1.29	1.15
21L02-2	1024 x 1	(LP) (250ns)	1.69	1.55
2111	256 x 4	(450ns)	2.99	2.49
2112	256 x 4	(450ns)	2.99	2.79
2114	1024 x 4	(450ns)	8/16.95	1.95
2114L-2	1024 x 4	(LP) (200ns)	8/19.95	2.35
2114L-3	1024 x 4	(LP) (300ns)	8/18.95	2.25
2114L-4	1024 x 4	(LP) (450ns)	8/17.95	2.10
2147	4096 x 1	(55ns)	9.95	CALL
TMS4044-4	4096 x 1	(450ns)	3.49	3.25
TMS4044-3	4096 x 1	(300ns)	3.99	3.75
TMS40L44-2	4096 x 1	(LP) (200ns)	4.49	4.25
TMM2016	2048 x 8	(200ns) (150ns)		CALL
HM6116	2048 x 8	(200ns) (150ns) (120ns)		CALL

LP = LOW POWER

CRYSTALS

32.768 KHZ	3.95
1.0 MHZ	4.95
1.8432	4.95
2.0	3.95
2.097152	3.95
2.4576	3.95
3.2768	3.95
3.579545	3.95
4.0	3.95
5.0	3.95
5.0688	3.95
5.185	3.95
5.7143	3.95
6.5536	3.95
8.0	3.95
10.0	3.95
14.31818	3.95
18.0	3.95
18.432	3.95
20.0	3.95
22.1184	3.95
32.0	3.95

MISC.

AY5-2376	12.50
11C90	13.95
XR2206	4.95
3242	7.95
3480	9.00
MC4024	3.95
MC4044	4.50
7103	9.50
7106	9.95
7107	12.95
76477	3.95
8038	3.95
95H90	7.99
9602	1.50

DISC CONTROLLERS

1771	24.95
1791	36.95
1793	44.95
1797	54.95

UARTS

AY3-1014	6.95
AY5-1013	3.95
TR1602	4.95
IM6402	7.95

INTERFACE

8T26	1.69
8T28	2.49
8T95	.99
8T96	.99
8T97	.99
8T98	.99
DM8131	2.95
DS8836	1.29

CLOCK CIRCUITS

MM5369	3.95
MM5375	3.95
MSM5832	7.45
7207	7.50
7208	15.95

CONVERTERS

MC1408 L8	4.95
DAC-0800	4.95
ADC-0804	4.95

January Specials

Z-80A-CPU	6.00
Z-80A-PIO	6.00
8214	2.95
8216	1.50
6800	4.95
6810	3.95

TMS 40L44-20
4096 x 1 low power 200ns RAMS

By Texas Instruments - not equivalent part number made by another manufacturer as sold by others:

4.49 each 125.00/32 pcs.

Specials end January 31, 1982

Please state "January Specials" when ordering

6502

6502	6.95
6502-A	12.95
6504	6.95
6505	8.95
6507	9.95
6520	4.35
6522	9.95
6532	14.95
6551	11.85

Z80

Z80-CPU	8.95
Z80A-CPU	6.00
Z80-P10	6.50
Z80A-P10	6.00
Z80-CTC	5.95
Z80A-CTC	8.65
Z80-DART	15.25
Z80A-DART	18.75
Z80-DMA	17.50
Z80A-DMA	27.50
Z80-S10/0	23.95
Z80A-S10/0	28.95
Z80-S10/1	23.95
Z80A-S10/1	28.95
Z80-S10/2	23.95
Z80A-S10/2	28.95
Z80-S10/09	17.95
Z80A-S10/9	22.95
Z80B-CPU	18.95
Z80B-CTC	17.95
Z80B-P10	17.95
Z8671	39.95
Z6132	34.95

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				74LS166	2.40	74LS293	1.85
74LS00	.25	74LS85	1.15	74LS168	1.75	74LS295	1.05
74LS01	.25	74LS86	.40	74LS169	1.75	74LS298	1.20
74LS02	.25	74LS90	.65	74LS170	1.75	74LS324	1.75
74LS03	.25	74LS91	.89	74LS173	.80	74LS352	1.55
74LS04	.25	74LS92	.70	74LS174	.95	74LS353	1.55
74LS05	.25	74LS93	.65	74LS175	.95	74LS363	1.35
74LS08	.35	74LS95	.85	74LS181	2.15	74LS364	1.95
74LS10	.25	74LS96	.95	74LS189	9.95	74LS365	.95
74LS11	.35	74LS107	.40	74LS190	1.00	74LS366	.95
74LS12	.35	74LS109	.40	74LS191	1.00	74LS367	.70
74LS13	.45	74LS112	.45	74LS192	.85	74LS368	.70
74LS14	1.00	74LS113	.45	74LS193	.95	74LS373	.99
74LS15	.35	74LS114	.50	74LS194	1.00	74LS374	1.75
74LS20	.25	74LS122	.45	74LS195	.95	74LS377	1.45
74LS21	.35	74LS123	.95	74LS196	.85	74LS378	1.18
74LS22	.25	74LS124	2.99	74LS197	.85	74LS379	1.35
74LS26	.35	74LS125	.95	74LS221	1.20	74LS385	1.90
74LS27	.35	74LS126	.85	74LS240	.99	74LS386	.65
74LS28	.35	74LS132	.75	74LS241	.99	74LS390	1.90
74LS30	.25	74LS136	.55	74LS242	1.85	74LS393	1.90
74LS32	.35	74LS137	.99	74LS243	1.85	74LS395	1.65
74LS33	.55	74LS138	.75	74LS244	.99	74LS399	1.70
74LS37	.55	74LS139	.75	74LS245	1.90	74LS424	2.95
74LS38	.35	74LS145	1.20	74LS247	.76	74LS447	.37
74LS40	.35	74LS147	2.49	74LS248	1.25	74LS490	1.95
74LS42	.55	74LS148	1.35	74LS249	.99	74LS668	1.69
74LS47	.75	74LS151	.75	74LS251	1.30	74LS669	1.89
74LS48	.75	74LS153	.75	74LS253	.85	74LS670	2.20
74LS49	.75	74LS154	2.35	74LS257	.85	74LS674	9.65
74LS51	.25	74LS155	1.15	74LS258	.85	74LS682	3.20
74LS54	.35	74LS156	.95	74LS259	2.85	74LS683	2.30
74LS55	.35	74LS157	.75	74LS260	.65	74LS684	2.40
74LS63	1.25	74LS158	.75	74LS266	.55	74LS685	2.40
74LS73	.40	74LS160	.90	74LS273	1.65	74LS688	2.40
74LS74	.45	74LS161	.95	74LS275	3.35	74LS689	2.40
74LS75	.50	74LS162	.95	74LS279	.55	81LS95	1.69
74LS76	.40	74LS163	.95	74LS280	1.98	81LS96	1.69
74LS78	.50	74LS164	.95	74LS283	1.00	81LS97	1.69
74LS83	.75	74LS165	.95	74LS290	1.25	81LS98	1.69

CMOS

74C00	.35	74C374	2.75	4019	.45	4098	2.49
74C02	.35	74C901	.80	4020	.95	4099	1.95
74C04	.35	74C902	.85	4021	.95	14409	12.95
74C08	.35	74C903	.85	4022	1.15	14410	12.95
74C10	.35	74C905	10.95	4023	.35	14411	11.95
74C14	1.50	74C906	.95	4024	.75	14412	12.95
74C20	.35	74C907	1.00	4025	.35	14419	4.95
74C30	.35	74C908	2.00	4026	1.65	4502	.95
74C32	.50	74C909	2.75	4027	.65	4503	.65
74C42	1.75	74C910	9.95	4028	.80	4508	1.95
74C48	2.10	74C911	10.00	4029	.95	4510	.95
74C73	.65	74C912	10.00	4030	.45	4511	.95
74C74	.85	74C914	1.95	4034	2.95	4512	.95
74C76	.80	74C915	2.00	4035	.85	4514	1.25
74C83	1.95	74C918	2.75	4040	.95	4515	2.25
74C85	1.95	74C920	17.95	4041	1.25	4516	1.55
74C86	.95	74C921	15.95	4042	.75	4518	1.25
74C89	4.50	74C922	5.95	4043	.85	4519	1.25
74C90	1.75	74C923	5.95	4044	.85	4520	1.25
74C93	1.75	74C925	6.75	4046	.95	4522	1.25
74C95	1.75	74C926	7.95	4047	.95	4526	1.25
74C107	1.00	74C927	7.95	4049	.55	4527	1.95
74C150	5.75	74C928	7.95	4050	.55	4528	1.25
74C151	2.25	74C929	19.95	4051	.95	4531	.95
74C154	3.25	74C930	19.95	4053	.95	4532	1.95
74C157	1.75	4000	.35	4060	1.45	4538	1.95
74C160	2.00	4001	.35	4066	.75	4539	1.95
74C161	2.00	4002	.25	4068	.40	4543	2.70
74C162	2.00	4006	.95	4069	.35	4555	.95
76C163	2.00	4007	.29	4070	.35	4556	.95
74C164	2.00	4008	.95	4071	.30	4581	1.95
74C165	2.00	4009	.45	4072	.30	4582	1.95
74C173	2.00	4010	.45	4073	.30	4584	.95
74C174	2.25	4011	.35	4075	.30	4585	.95
74C175	2.25	4012	.25	4076	.95	4702	12.95
74C192	2.25	4013	.45	4078	.30	4724	1.50
74C193	2.25	4014	.95	4081	.30	80C07	.95
74C195	2.25	4015	.95	4082	.30	80C95	.85
74C200	5.75	4016	.45	4085	.95	80C96	.95
74C221	2.25	4017	1.15	4086	.95	80C97	.95
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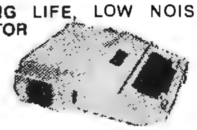

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EPROM ERASERS

PE-14	78.50
PE-14T (with timer)	108.50
PE-24T (with timer)	154.50

ALL ARE HIGH QUALITY UNITS ENCLOSED IN A BLACK ANODIZED ALUMINUM ENCLOSURE.

OUR AD MAY BE IMITATED BUT OUR SERVICE CAN NEVER BE DUPLICATED.

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22 pin ST	.30	.27
24 pin ST	.30	.27
28 pin ST	.40	.32
40 pin ST	.49	.39

ST = SOLDERTAIL

8 pin WW	.59	.49
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16 pin WW	.69	.58
18 pin WW	.99	.90
20 pin WW	1.09	.98
22 pin WW	1.39	1.28
24 pin WW	1.49	1.35
28 pin WW	1.69	1.49
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WW = WIREWRAP

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RS232 MALE	3.25
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RS232 HOOD	1.25
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S-100 WW	4.95

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2N3055	.79	10/ 6.99
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2N3906	10/1.00	100/ 8.99
1N4148 (1N914)		10/ 1.00
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7812T	.79	7915T	1.19
7815T	.99	7924T	1.19
7824T	.99		
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7812K	1.39	7912K	1.49
7815K	1.39	79LO5	.79
78LO5	.69	79L12	.79
78L12	.69	79L15	.79
78L15	.69		
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LM555V	.39
LM556	.69
LM565	.99
LM566V	1.49
LM567V	1.29
LM723	.49
LM733	.98
LM741V	.29
LM747	.79
LM748V	.59
LM1310	2.90
MC1330V	1.89
MC1350V	1.29
MC1358	1.79
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LM1489	.99
LM1800	2.99
LM1889	2.49
LM3900	.59
LM3909V	.98
LM3914	3.95
LM3915	3.95
LM3916	3.95
75451V	.39
75452V	.39
75453V	.39

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5082-7760 .43"CC	.79
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74S02	.48	74S85	2.39	74S168	4.65	74S258	1.49
74S03	.48	74S86	1.44	74S169	5.44	74S260	1.83
74S04	.79	74S112	1.59	74S174	1.09	74S274	19.95
74S05	.79	74S113	1.98	74S175	1.09	74S275	19.95
74S08	.48	74S114	1.50	74S181	4.47	74S280	2.90
74S09	.98	74S124	2.77	74S182	2.95	74S287	4.75
74S10	.69	74S132	1.24	74S188	3.95	74S288	4.45
74S11	.88	74S133	.98	74S189	14.95	74S289	6.98
74S15	.70	74S134	.69	74S194	2.95	74S301	6.95
74S20	.68	74S135	1.48	74S195	1.89	74S373	3.45
74S22	.98	74S138	1.08	74S196	4.90	74S374	3.45
74S30	.48	74S139	1.25	74S197	4.25	74S381	7.95
74S32	.98	74S140	1.45	74S201	14.95	74S387	5.75
74S37	1.87	74S151	1.19	74S225	8.95	74S412	2.98
74S38	1.68	74S153	1.19	74S240	3.98	74S471	9.95
74S40	.44	74S157	1.19	74S241	3.75	74S472	16.85
74S51	.78	74S158	1.45	74S244	3.98	74S474	17.85
74S64	.79	74S161	2.85	74S251	1.90	74S482	15.60
74S65	1.25	74S162	3.70	74S253	7.45	74S570	7.80
						74S571	7.80

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7401	.19	7453	.23	74141	.65	74190	1.15
7402	.19	7454	.23	74142	2.95	74191	1.15
7403	.19	7460	.23	74143	2.95	74192	.79
7404	.19	7470	.35	74144	2.95	74193	.79
7405	.22	7472	.29	74145	.60	74194	.85
7406	.22	7473	.34	74147	1.75	74195	.85
7407	.22	7474	.35	74148	1.20	74196	.79
7408	.24	7475	.49	74150	1.35	74197	.75
7409	.19	7476	.35	74151	.65	74198	1.35
7410	.19	7480	.59	74152	.65	74199	1.35
7411	.25	7481	1.10	74153	.55	74221	1.35
7412	.30	7482	.95	74154	1.40	74246	1.35
7413	.35	7483	.50	74155	.75	74247	1.25
7414	.55	7485	.65	74156	.65	74248	1.85
7416	.25	7486	.35	74157	.55	74249	1.95
7417	.25	7489	4.95	74159	1.65	74251	.75
7420	.19	7490	.35	74160	.85	74259	2.25
7421	.35	7491	.40	74161	.70	74265	1.35
7422	.29	7492	.50	74162	.85	74273	1.95
7423	.29	7493	.49	74163	.85	74276	1.25
7425	.29	7494	.65	74164	.85	74279	.75
7426	.29	7495	.55	74165	.85	74283	2.00
7427	.29	7496	.70	74166	1.00	74284	3.75
7428	.45	7497	2.75	74167	2.95	74285	3.75
7430	.19	74100	1.00	74170	1.65	74290	.95
7432	.29	74107	.30	74172	5.95	74293	.75
7433	.45	74109	.45	74173	.75	74298	.85
7437	.29	74110	.45	74174	.89	74351	2.25
7438	.29	74111	.55	74175	.89	74365	.65
7440	.19	74116	1.55	74176	.89	74366	.65
7442	.49	74120	1.20	74177	.75	74367	.65
7443	.65	74121	.29	74178	1.15	74368	.65
7444	.69	74122	.45	74179	1.75	74376	2.20
7445	.69	74123	.55	74180	.75	74390	1.75
7446	.59	74125	.45	74181	2.25	74393	1.35
7447	.69	74126	.45	74182	.75	74425	3.15
7448	.69	74128	.55	74184	2.00	74426	.85
7450	.19	74132	.45	74185	2.00	74490	2.55

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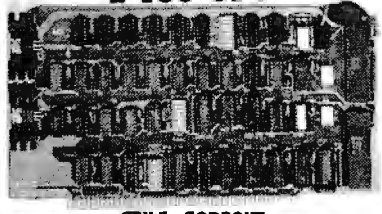
PRIORITY ONE ELECTRONICS

S-100 CPU



CPU-Z - GODBOUT
2/4 MHZ Z80 CPU 24 Bit Addressing

GBT 160A	A&T	$199.00
GBT 160C	CSC 3-6 MHZ	$375.00

DUAL PROCESSOR 8085-8088 - GODBOUT
6 or 8 MHz Provides true 16 Bit Power with a standard 8 bit S-100 bus.

GBT 1612A	A&T...6 MHZ	$399.00
GBT 1612C	CSC...8 MHZ	$498.00

SOLID STATE DISK DRIVE, 3500% FASTER!
Not Really, But the Next Best Thing For Godbout 8085/88 Users. Call For Details on M-Drive. See Page 340 of November BYTE

GBT MD 128K	$1550.00
GBT MD 256K	$3,000.00

2810 Z80 CPU-CA. COMP. SYST.
2/4 MHz Z80A CPU with RS232C Serial I/O Port complete with Monitor PROM for 2422 Disk Controller

CCS 2810A	A&T	$280.00

CB2 Z80 CPU - S.S.M.
2/4 MHZ will accept 2716, or 2732, or RAM RUN/STOP and single step switches

SSMCB2K	Kit	$260.00
SSMCB2A	A&T	$310.00
SSMZ80M	SSMZ80 Monitor	$89.00

CBIA 8080 CPU - S.S.M.
8080 CPU, 1K RAM, Holds 1 2708, 1 8 Bit parallel input port.

SSMCB1K	Kit	$183.00
SSMCB1A	A&T	$225.00
SSM8080M	SM 8080 Monitor	$59.00

S-100 I/O BOARDS

SYSTEM SUPPORT 1 - GODBOUT
Serial port (software prog baud), 4K EPROM OR RAM provision, 15 levels of interrupt, real time clock, optional math processor

PART NO.	DESCRIPTION	LIST PRICE	OUR PRICE
GBT162A	Assembled & Tested	$39.00	$360.00
GBT162C	CSC	$495.00	$460.00
GBTB231	Math Chip		$195.00
GBT8232	Math Chip		$195.00
GBT162AM1	A&T with 8231 Math Chip		$555.00
GBT162CM1	CSC with 8231 Math Chip		$655.00
GBT162AM2	A&T with 8232 Math Chip		$555.00
GBT162CM2	CSC with 8232 Math Chip		$655.00

MPX CHANNEL BOARD - GODBOUT
I/O Multiplexer, using 8085a-2 cpu on board

GBT186A	Assembled & Tested	$495.00	$450.00
GBT166C	CSC	$595.00	$550.00

INTERFACER I - GODBOUT
Two Serial I/O

GBT133A	A&T	$249.00	$219.00
GBT133C	CSC	$324.00	$298.00

INTERFACER II - GODBOUT
Three parallel, one serial I/O board

GBT150A	A&T	$249.00	$219.00
GBT150C	CSC	$324.00	$289.00

INTERFACER III - GODBOUT
Eight channel multi-use serial I/O board

GBT1748A	Assembled & Tested	$699.00	$629.00
GBT1748C	CSC 200 hr. Burn In Test	$849.00	$629.00

INTERFACER 3 WITH 5 SERIAL PORTS

GBT1745A	Assembled & Tested	$599.00	$5_3.00
GBT1745C	CSC 200 hr. Burn In Test	$699.00	$629.00

MULTI I/O - MORROW DESIGNS
Three Serial, Two parallel

MOSMB3200	A&T	$329.00	$309.00

SWITCHBOARD-MORROW DESIGNS
Two serial I/O, four parallel I/O, one status port, one strobe port

MOSSB2411	$259.00	$239.00

I/O4 - SSM
Two serial I/O, two parallel I/O

SSMI04K	Kit		$210.00
SSMI04A	A&T	$290.00	$260.00

2710 4 PORT SERIAL - CCS
4 Full handshaking RS232 ports and optional 2K ROM

CCS271001	A & T	$340.00	$310.00

2718 2 SERIAL & 2 PARALLEL - CCS
2 RS232 C ports, 2 8 bit parallel ports, & optional 2K ROM

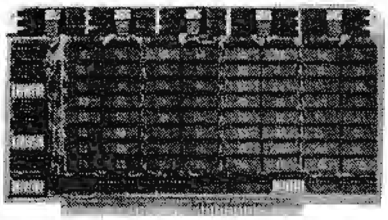
CCS271801	A & T	$360.00	$325.00

2720 4 PORT PARALLEL - CCS
4 8 bit parallel ports and optional 2K ROM

CCS272001	A & T	$250.00	$225.00

S-100 10 MHZ STATIC RAM

NEW LOW PRICES!



32K STATIC RAM - GODBOUT
RAM 20 10 MHZ, 4Kbyte block disable, bank or 24 bit addressings available 8, 16, 24 or 32K

PART NO.	DESCRIPTION	LIST PRICE	OUR PRICE
GBT164AA8	8K A&T	$210.00	$190.00
GBT164AC8	8K CSC	$280.00	$260.00
GBT164AA16	16K A&T	$285.00	$260.00
GBT164AC16	16K CSC	$355.00	$325.00
GBT164AA24	24K A&T	$355.00	$325.00
GBT164AC24	24K CSC	$425.00	$385.00
GBT164AA32	32K A&T	$425.00	$385.00
GBT164AC32	32K CSC	$495.00	$450.00

64K STATIC RAM - GODBOUT
RAM 17, 10 MHZ, 2 Watt, DMA Compatable 24 Bit Addressing

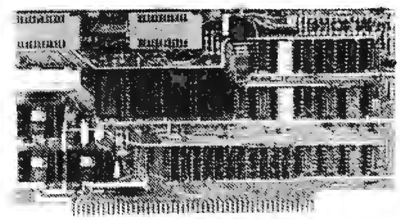
GBT175A48	48K A&T	$650.00	$619.00
GBT175C48	48K CSC 200hr.	$750.00	$710.00
GBT175A64	64K A&T	$795.00	$755.00
GBT175C64	64K CSC 200hr.	$895.00	$850.00

NEW! 32K x 16 BIT STATIC RAM - GODBOUT
RAM 16 10 MHZ, 32K x 16 or 64K x 8 IEEE/696 16 BIT 2 Watt, 24 Bit Addressing

GBT180A	64K A&T	$895.00	$850.00
GBT180C	64K CSC	$995.00	$945.00

NEW! 128K STATIC RAM - GODBOUT
RAM 21 10MHZ 128K x 8 or 64K x 16
IEEE/696 8 or 16 Bit 1.2 Amps 24 Bit Addressing

GBT167A	128K A&T	$1695.00	$1610.00
GBT167C	128K CSC	$1895.00	$1795.00



S-100 ROM

PBI PROM PROGRAMMER - SSM
Programs 2708 or 2716's, operates as a 4K/8K EPROM BOARD AS WELL.

SSMPB1K	Kit		$179.00
SSMPB1A	Assembled & Tested	$265.00	$220.00

ECONOROM 2708 - GODBOUT
16K x 8eprom Board using 2708, Power on jump to any 256 byte

GBT125A	Assembled & Tested	$135.00	$120.00
GBT125C	CSC	$195.00	$175.00

S-100 VIDEO BOARDS

SPECTRUM - GODBOUT
Color Graphics board with Parallel I/O

GBT144A	Assembled & Tested	$399.00	$349.00
GBT144C	CSC	$449.00	$399.00
GBT20	Sublogic Universal Graphics Interpreter Software		$35.00

VB - 3 S.S.M.
80 x 25 or 50 character video display Memory Mapped, Parallel Keyboard port

SSMVB3K24	80x24 Kit		$425.00
SSMVB3A24	80x24 A&T	$499.00	$440.00
SSMVB3UP	80x50 Line Upgrade		$ 39.00

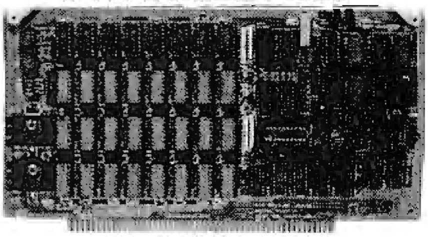
VB2-S.S.M.
I/O Mapped Video Board, with Parallel Keyboard port 64 x 16

SSMVB2K	Kit		$199.00
SSMVB2A	Assembled & Tested	$269.00	$229.00

VBIC - S.S.M.
Memory Mapped Video Board 64x16 character display or 64x16 graphics display

SSMVB1K	Kit		$179.00
SSMVB1A	Assembled & Tested	$242.00	$220.00

S-100 DYNAMIC RAM

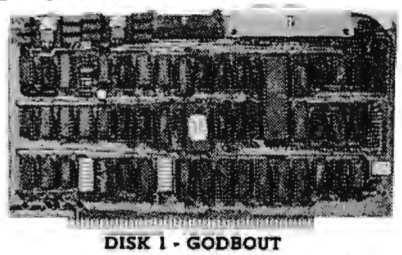


THE EXPANDABLE 1
PRIORITY 1 ELECTRONICS

THE EXPANDABLE 1" 64 K Dynamic Ram board provides your S-100 system with 64K of reliable, high-speed dynamic RAM. Compatable with most of the major S-100 systems on the market, including those with front panels, it supports DMA operations and requires no Wait states with current microprocessors.
• User expandale from 16 to 64K • Supports DMA • Designed to IEEE proposed S-100 bus standards • 2 or 4 MHz operation • Operates with either an 8080 or Z-80 based S-100 system, providing processor-transparent refreshes with both • Supports IMSAI-type front panels • Jumper-selectable Phantom input • Uses Popular 4116 RAMS • All ICs in sockets • Any 16K block can be made bank-independent • Fully buffered address and data lines • Fail-safe refresh circuitry for extended Wait states • Board configuration with reliable, easy-to-configure Berg jumpers

PRIEXP116	16K Assembled & Tested	$299.00
PRIEXP132	32K Assembled & Tested	$339.00
PRIEXP148	48K Assembled & Tested	$379.00
PRIEXP164	64K Assembled & Tested	$409.00

S-100 DISK CONTROLLERS



DISK 1 - GODBOUT
FAST DMA. Soft Sector. Controls 8" or 5¼", single or double density OUR BEST!

		LIST PRICE	OUR PRICE
GBT171A	Assembled & Tested	$495.00	$450.00
GBT171C	CSC	$595.00	$555.00
GBTCPM80*	CP/M 2.2 for Z80/8085 with manuals & BIOS 8" S/D disk		$175.00
GBTOAS8S	Oasis 8 bit single user 8" S/D disk		$500.00
GBTOAS8M	Oasis 8 bit multi-user, 8" S/D disk		$850.00

2422A - CA. COMP. SYST.
I/O Mapped, controls 8" or 5¼" single or double density A&T with CPM 2.2 8" S.D.

CCS2422A	$475.00	$375.00

DISK JOCKEY 2D - MORROW
I/O Mapped, controls 8", single or double density, serial I/O

MOSDJ2208	A&T with CP/M 22	$399.00	$375.00

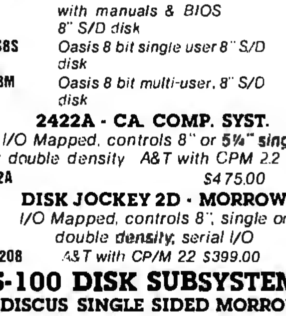
S-100 DISK SUBSYSTEMS

DISCUS SINGLE SIDED MORROW
8" DBL Density drives with cabinet, power supply controller, with CP/M 2.2 and Microsoft Basic

MOSF1218	Single Drive System	1095.00	$950.00
MOSF1228	Dual Drive System	$1875.00	$1598.00

DISCUS DOUBLE SIDED - MORROW
8" DBL Density/sided drives with cabinet Power supply controller, with CP/M 2.2 and Microsoft Basic

MOSF2218	Single Drive System	1395.00	$1250.00
MOSF2228	Dual Drive System	$2495.00	$2050.00



S-100 HARD DISK - MORROW

8" 10 & 20MB .14" - 26MB formatted hard disk complete with cainet. P.S., Controller. CPM 2.2 and Microsoft Basic

		LIST PRICE	SALE PRICE
MOSM10S	10 MB	$3695.00	$2950.00
MOSM20S	20 MB	$4795.00	$3825.00
MOSM26S	26 MB	$4495.00	$3495.00

PRIORITY ONE ELECTRONICS

S-100 SYSTEMS

"LITTLE 8" Z80 SYSTEM STARTER SET GODBOUT

CPU Z: A 4MHz Z80 A-based 8-bit workhorse CPU board that includes all the standard features plus many of the convenience options. Meets all IEEE 696/S-100 specifications, including timing.
DISK 1 DMA High Performance Disk Controller: disk controllers don't have to be your system's bottleneck! The DISK 1 is lightning fast thanks to properly implemented DMA (with arbitration) and transfer that is independent of CPU speed.
RAM 20 32K High Speed Static RAM. This board has it all Operates at speeds up to 10MHz, ultra-low power consumption, IEEE 696/S-100 extended addressing protocol, bank select and flawless DMA.
CP/M 2.2: The de facto standard of 8-bit operating systems ready to load and go!

ANOTHER PRIORITY 1 EXCLUSIVE!
We went to GODBOUT and made a special buy on the nucleous of the best S-100 Z80A systems ever.

LOOK AT WHAT YOU GET:

1 GBT180A 2/4 MHz Z80 CPU	$295.00
1 GBT164A32 32K 10MHz Static Ram	$425.00
1 GBT171A DMA Disk Controllers	$495.00
1 GBTCPM80 CP/M 2.2	$175.00
IT ALL ADDS UP TO...	$1039.00

TOTAL PACKAGE PRICE ONLY $1095.00
ORDER NO. PDBGBTSG

SUPERSIXTEEN — GODBOUT

LOOK WHAT $3495.00 WILL BUY!
WHY WAIT ANY LONGER?
HERE IS WHAT EACH PACKAGE INCLUDES:

GBT1612A 6 MHz 8085/8088 Dual Processor Board
GBT171A High Speed DMA Disk Controller
GBT162A System Support 1 Multi Function Board
GBT133A Interfacer 1 Dual Serial I/O
128K 10MHz Low Power Static Ram
CP/M 86 16 Bit Operating System Ready to Load & Go
Cables and Documentation Three interfacer cables one disk I/O cable, complete documentator for all hardware, and manuals for both CP/M operating systems.
Compu Pro's famous **1 Year** limited warranty.

Now to the best part of all. If purchased separately, these quality components would list for $4,344.00. **BUT SuperSixteen's low package price is an amazing $3,495.00. Yo save $849.00!** (For boards qualified under the Certified System Component high-reliability program - with extended 2 year warranty, 200 hour burn-in and 8MHz processors - add $600 to the package price.
Sh. Wt. 15 lbs.

POBGBTSJ	SuperSixteen A&T	$3495.00
POBGBTSK	SuperSixteen CSC	$4095.00

S-100 SOFTWARE

PRIORITY 1 is pleased to offer the finest in industry standard software. All software is supplied on 8" Single Density IBM 3740 CP/M compatible disketts. All software is sold "AS IS" and is non-returnable. If you have questions about the software for your application, order the manual first.

CCS803 CP/M Version 2.2 Microcompouter Control Program	$150.00
CCS2301 MAC-CP/M Macro Assembler	$90.00
CCS2401 SID-CP/M Symbolic Instruction Debugger	$75.00
CCS2501 TEX-CP/M Text Formatter	$75.00
CCS2601 DESPOOL-CP/M Background Print Utility	$50.00

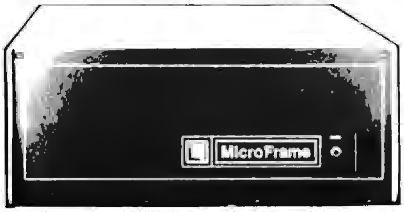
CP/M, MAC, SID, TEX, and DESPOOL are registered trademarks of Digital Research

PART NO.	DESCRIPTION	LIST PRICE	OUR PRICE
CCS401	C-BASIC-2 Interp	$150.00	$139.00
CCS401M	Manual		$ 32.00
CCS1101	FMS-80 by Systems Plus	$995.00	$895.00
CCS1101M	Manual		$ 70.00

GRAHAM-DORIAN ACCOUNTING

CCS1301	General Ledger	$820.00	$750.00
SCCS1301M	Manual		$ 50.00
CCS1501	Accounts Receivable	$820.00	$750.00
CCS151M	Manual		$50.00
CCS1401	Accounts Payable	$820.00	$750.00
CCS1401M	Manual		$ 50.00
CCS1701	Inventory II	$820.00	$750.00
CCS1701M	Manual		$ 50.00
CCS1801	Payroll II	$555.00	$495.00
CCS1801M	Manual		$ 50.00
CCS20001	Job Costing	$820.00	$750.00
CCS2001M	Manual		$ 50.00
CCS2701	Order Entry/Invoice	$820.00	$750.00
CCS2701M	Manual		$ 50.00
MEDICAL PRACTIC PATIENT BILLING			
CCS1801	15 Programs	$820.00	$780.00
CCS1801M	Manual		$ 50.00
DENTAL PRACTICE PATIENT BILLING			
CCS1901	14 Programs	$820.00	$750.00
CCS1901M	Manual		$ 50.00

S-100 MAINFRAMES



S-100 MICROFRAME - TEI

110V 60HZ CVT Mainframes, the best money can buy!
12 Slot ±8V 17A ±16V @ 2A
22 Slot ±8v @ 30A ±16V @ 4A

TEI has announced a 5 - 8% Price Increase Feb 1 - Hurry!

		LIST PRICE	OUR PRICE 1-9	10-24
TEIMCS 112	12 Slot Desk	$685.00	$615.00	$570.00
TEIMCS 122	22 Slot Desk	$825.00	$760.00	$705.00
TEIRM 12	12Slot Rackmnt	$725.00	$720.00	$819.00
TEIRM 22	22 Slot Rackmnt	$875.00	$850.00	$750.00

Shipping Weight: On 12 Slot Mainframes 45 lbs.
On 22 Slot Mainframes 55 lbs.

S-100 FRAMES 2 - 5" DISK CUTOUTS - TEI

±8V @ 17±16V @ 2A +12V @ 1.2A. Internal Cables

			1-9	10-24
TEITF12	12 Slot desk	$675.00	$625.00	$580.00
TEIRO12	12 Slct Rackmnt	$795.00	$715.00	$665.00

Shipping Weight: On 12 SlotDesk 40 lbs.
On 12 Slot Rackmount 45 lbs.

DUAL 8" DISK DRIVE CHASSIS - TEI

For Shugart 800/801R or 850/851R withinternal power cables provided
+24V @ 1.5A +5V @ 1.0A - 5V @ .25A

			1-9	10-24
TEIOFOO	Desk Top	$535	$485	$455
TEIRFOO	Rack Mount	$720	$870	$630
POBOFOOS1	DFDO with 1 Shugart 801R			$970.00
POBOFOOS2	DFDO with 2 Shugart 801Rs			$1375.00
POBRFOOS1	RFDO with 1 Shugart 801R			$1095.00
POBRFOOS2	RFDO with 2 Shugart 801Rs			$1495.00
PRI50PGCE2	Internal Data Cable.50 pin plug connector to 2 Card Edge.			$34.95

Due to UPS shipping regulations, disk drives will be shipped separately from the cabinet. Don't forget to include shipping for each drive. (Shipping Wt. 16 lbs., each)

CALL FOR NEW TEI PRICES FEBRUARY 1st.

S-100 MAINFRAME - GODBOUT

110V 60HZ CVT Mainframe uses famous 20 slot GODBOUT Motherboard. 55 lbs.

GBTENC2CRM	20 Slot Rack Mount	$895.00	$825.00
GBTENC20DK	20 Slot Desk Top	$825.00	$760.00

GODBOUT Mainframe, Less Motherboard & Power Supply - Kit. 23 lbs

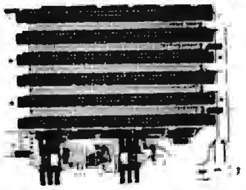
GBTBOX DESK	Desk Top Main Frame	$289.00
GBTBOX RACK	Rack Mount Main Frame	$329.00

S-100 MAINFRAME - CCS

12-slot motherboard with removable termination card.

CCS2200-01	Office Cream	35 lbs	$575.00	$535.00
CCS2200-02	Blue	35 lbs	$575.00	$535.00

S-100 MOTHERBOARDS



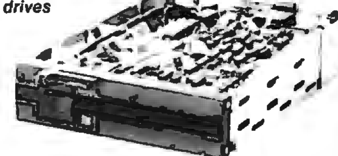
MOTHERBOARD - GODBOUT

Active termination, 6-12-20 slot

GBT153A	A&T 6 slot, 2 lbs	$140.00	$128.00
GBT153C	CSC 6 slot, 2 lbs.	$190.00	$175.00
GBT154A	A&T 12 slot, 2 lbs.	$175.00	$155.00
GBT154C	CSC 12 slot, 2 lbs.	$240.00	$220.00
GBT155A	A&T 20 slot, 4 lbs.	$265.00	$235.00
GBT155C	CSC 20 slot, 4 lbs.	$340.00	$310.00

FLOPPY DISC DRIVES

Tandon TM-800 Thinline is exactly half the size of conventional 8" floppy disk drives



Exactly one-half the height of any other model.
Propietary, high-resolution, read-write heads patented by Tandon
D.C. only operation - no A.C. required
Industry standard interface.
Three millisecond track-to-track access time 9 lbs.

TNDTM8481 ... Single Sided $495.00 2 or more ...	$470.00
TNDTM8482. Double Sided $625.00 2 or more...	$600.00
TNDTM8M.... Manual not included with drive....	$10.00

801R - SHUGART

Single sided doubledensity most popular 8" drive

SHU801R.... $425.00 ea. or 2 or more (16 lbs.)...	$395.00
SHUSA801RM....... Manual for 801R drives	$10.00

DT-8 - QUME

Data track 8 double sided, double density 8"

QMEDT8.....$575.00 ea or 2 or more (16 lbs.).....	$540.00
QMEDT8M............. Manual for DT-8	$10.00

5¼" DRIVES - TANDON

TNDTM1001...... Single Sided, 250KB (5 lbs)......	$310.00
TNDTM1002... ..... Double Sided, 500KB.........	$370.00
TNDTM1003.......... Single Sided, 500KB..........	$375.00
TNDTM1004. .... Double Sided, 1000KB.........	$495.00
TNDTM5M ..... Manual, not included with drive	$10.00

DISK CABINETS

V-100 - VISTA

• Desk or rack mountable • Internal power and data cables
• Drives pull out for easy service and maintenance

VISV100 Disk Drive Cabinet (35 lbs)	$495.00	$449.00

SINGLE 8" - Q.T.

Single 8" cabinet with power supply

QTCDDC8.. (2 lbs)	$195.00

DUAL 8" - Q.T.

Dual 8" cabinet with power supply

QTCDDC88.. (25 lbs)	$349.00

5" CABINETS - VISTA

VIS-9801............ Single 5" with P.S.	$75.00
VIS-9802.. .... Dual 5" with P.S.	$95.00

5¼" MINIFLOPPY - VISTA

Totally compatible with several microcomputers including TRS-80Northstar, Exidy, Texas Instruments, Heath/Zenith and others.

PART NO.	CAPACITY	NO. DRIV	TRAC	SIDE	LIST PRICE	OUR PRICE
VISV80	10SK	1	40	1	395.00	380.00
VISV800	204K	1	40	2	595.00	540.00
VISV801	204K	1	80	1	595.00	540.00
VISV8000	408K	1	80	2	775.00	695.00
VISV802	204K/408K	2	40	1	775.00	695.00
VISV8002	408K/816K	2	40	2	1095.00	995.00
VISV8012	408K/816K	2	80	1	1095.00	995.00
VISV8002	816K/16M	2	80	2	1495.00	1350.00

S-100 MOTHERBOARDS - QT

QTCMB6BB	6 Slot Bare Board	$ 25.00
QTCMB6K	6 Slot Kit	$ 40.00
QTCMB6A	6 Slot A&T	$ 50.00
QTCMB8BB	8 Slot Bare Board	$ 27.00
QTCMB8K	8 Slot Kit	$ 55.00
QTCMB8A	8 Slot A&T	$ 70.00
QTCMB12BB	12 Slot Bare Board	$ 30.00
QTCMB12K	12 SlotKit	$ 70.00
QTCMB12A	12 Slot A&T	$ 90.00
QTCMB18BB	18 Slot Bare Board	$ 50.00
QTCMB18K	18 Slot Kit	$100.00
QTCMB18A	18 Slot A&T	$140.00

VISA master charge **PRIORITY ONE ELECTRONICS** MEMBER MITA

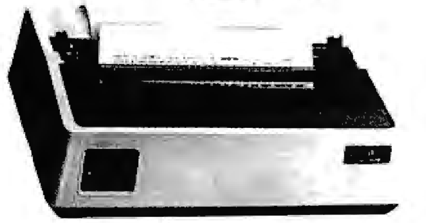
9161-B DEERING AVE ● CHATSWORTH, CA 91311
ORDER TOLL FREE (800) 423-5922 CA, AK, HI CALL (213) 709-5464

Terms U.S. VISA, MC, BAC, Check Money Order, U.S. Funds Only. CA residents add 6% Sales Tax. MINIMUM PREPAID ORDER $15.00. Include MINIMUM SHIPPING & HANDLING of $2.50 for the first 3 lbs. plus 25¢ for each additional pound. Orders over 50 lbs. sent freight collect. Just in case, please include your phone no. Prices subject to change without notice. We will do our best to maintain prices through January, 1982. Credit Card orders will be charged appropriate freight. See November BYTE for 60 page Catalog or send $1.00 for your copy today. Sale prices are for prepaid orders only.

NEDA

Circle 306 on inquiry card.

OKIDATA MICROLINE PRINTERS

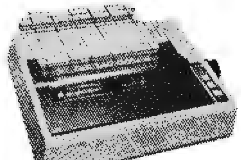


WITH FRICTION AND TRACTOR FEED

- BI-DIRECTIONAL - 120 CPS
- 9x9 Matrix (Alphanumeric)
- 6x9 or 12 Matrix for Graphics
- 5, 8.3, 10, 16 Characters Per Inch
- 6 or 8 Lines Per Inch
- 80 CPL @ 10 CPI for 82A
- 132 CPL @ 10 CPI for 83A
- Parallel and Serial I/O
- 110 Through 1200 Baud
- Self Test
- Out of Paper Switch
- Friction or Tractor Feed
- 3" to 14" Top of Form (Switch Selectable)
- 10 Different Character Sets

Part No.	Description	List Price	Sale Price
OKIDAT82AT	80CPL@10CPI	$ 799.00	$539.00
OKIDAT83AT	132CPL@10CPI	$1195.00	$750.00

EPSON MX-80



The **EPSON MX-80** Dot Matrix Printer is a highly versatile, general-purpose and computer-grade printer featuring 80 CPS bi-directional printing with logical seeking capability and 9x9 dot-matrix character formation. The MX-80 accepts the ASCII 96 codes and codes for special characters/symbols. It also accepts codes for 64 graphic patterns. Characters can be printed in any desired size — enlarged, condensed, emphasized, normal etc. The one-chip microprocessor is engaged in performing all functions of the Printer and the two built-in stepper motors of the MX-80 control the carriage and paper feeding functions respectively. Therefore, versatile software controls, such as horizontal and vertical tabs, and form feed are at your disposal.
In addition, various interface options are available to permit handshaking with most personal computers. Centronics type 8 bit parallel interface standard.

EPN MX80 Tractor Feed . . . List $645.00 **Sale $450.00**

PRINTER INTERFACES

RS232 Serial Interface Conversion for **EPSON MX-80**

MBSSEII Assembled & Tested $55.00

Apple 8 bit Centronics Parallel Interface for OKIDATA, EPSON, and CENTRONICS printers

MBSAEII Assembled & Tested $55.00

MBSAECI Cable for above $14.95

THE STAR MODEM from PRENTICE

FEATURE
FITS GTE HANDSETS!
1 YEAR WARRANTY

EXCLUSIVE ACOUSTIC CHAMBERS:
The exclusive triple seal of Prentice's new flat mounted cups locks the handset into the acoustic chamber yielding superior acoustic isolation and mechanical cushioning. Designed to adapt to most common handsets used throughout the world.

SELF TEST:
The self test feature on the STAR allows the user to verify total operation of the acoustic modem by using the terminal in the full duplex mode. No need for remote assistance in diagnosing terminal or modem problems.

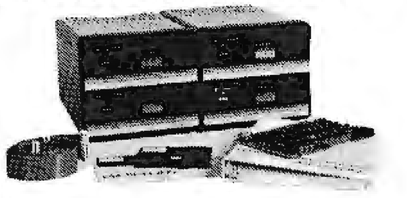
SPECIFICATIONS:
- **Data Rate:** 0 to 300 baud
- **Compatability:** Bell 103 and 1'3: CCITT
- **Frequency Stability:** ±0.3 percent Crystal controlled
- **Receiver Sensitivity:** -50 dBm ON, -53 dBm OFF
- **Modulation:** Frequency shift keyed (FSK)
- **Carrier Detect Delay:** 1.2 seconds ON; 120 sec OFF
- **EIA Terminal Interface:** Compatable with RS232 specs
- **Teletype Interface:** 20 milliampere current loop
- **International (CCITT) frequencies available.**
- **Switches:** Originate/Off/Answer: Full duplex/Test/-Half Duplex
- **Indicators:** Transmit Data, Receive Data, Carrier Ready, Test

PART NO.	DESCRIPTION	LIST PRICE	OUR PRICE
PRNSTAR	RS232, TTL 200 Ma Current Loop	$199.00	$129.00
PRNSTAR-V21	CCITT European Standard	$229.00	$209.00

CABLES

PART NO.	DESCRIPTION	PRICE
CNDRS2328F	RS232 8 Cond 8 Ft.	$19.95
IDCCABLE12	RS232 25 Cond 3 Ft.	$14.95

MICROPOLIS™



- Dual 5¼" S-100 Floppy Disk Subsystem
- 315K Per Drive, 630K Total — Single Sided
- 630K Per Drive, 1.2 MB Total — Double Sided
- S-100 Controller (8080, 8085, Z80 Compatable)
- Handles Up to 4 Heads
- Comes Complete With MDOS, Basic and Text Editor
- Built-in LED Indicates Drive Select, Drive Address and File Protect.

		OUR PRICE
MCP1053M2	Single Sided, 630K LIST PRICE $1534.00	**$995.00**
MCP1053M4	Double Sided 1.2MB LIST PRICE $1888.00	**$1395.00**

See page 10 of our ENGINEERING SELECTION GUIDE in the November, 1981 **BYTE** for more details

ANCHOR AUTOMATION MODEM PRICE BREAKTHROUGH!!

$129.00

THE SIGNALMAN MK 1

Meet the direct-connect SIGNALMAN MK1 .. the smallest, lightest, most compact modem available today. Its long life 9 volt self-contained battery and exclusive audible Carrier Detect Signal allows you to install the SIGNALMAN anywhere .. out of he way, and out of sight. Now, there is no need for messy cables, and no need to look at an LED to verify carrier.

Anchor's SIGNALMAN has been designed for transmitting both voice and data signals over all common telephone lines. And when you're in the data position, your SIGNALMAN automatically changes from ORIGINATE to ANSWER and back again as the need arises — ending all that confusion.

Your SIGNALMAN is tuly compatible with all BELL 103 modems — putting your computer in instant communications with thousands of other computers.

Anchor Automation has taken the FUSS out of communications. For business or fun, SIGNALMAN is the ideal modem.

PRODUCT FEATURES
- Direct Connect Modem
- Built-in RS232C Cable and Connector
- Self-contained 9V Battery— Wall plug transformer available.
- Audible carrier detect signal.
- Automatic mode selection.
- Talk/Data switch.
- CONNECTS IN SERIES WITH MODULAR *HANDSET* JACK ON TELEPHONE
- Complete with RS232C and Modular Handset Cables, eliminates need to buy cables — save $20.00 -$30.00, assures correct fit.
- Uses low cost 9V battery. Eliminates unsightly cords and need for "another"
- AC outlet. Optional plug-in transformer available.
- Audio Transducer eliminates need to view LED to confirm connection — can be placed anywhere (velcro tape provided).
- Advanced IC Circuitry eliminates confusion of who is originator — ends need to manually switch from Originate to Answer and Vice/Versa.
- Permits you to listen/talk on phone or switch to data communications mode.
- Permits you to communicate with most other computer networks.
- Small size, light weight permits you to install the SIGNALMAN anywhere.
- Lowest priced modem available.

RS232C SPECIFICATIONS

Data Format: Serial, binary, asynchronous. **Operate Mode:** Manual dial, Automatic ANSW/ORIG selection **Data Rate:** 0 to 300 bps, full duplex. **Modulation:** Frequency shift keyed (FSK). **Line Interface:** Direct Conect. **Data Interface:** RS232C, Cable to Computer Built-In.

Transmit Frequency:		ORIG	ANSW
	MARK	1270 Hz	2225 Hz
	SPACE	1070 Hz	2025 Hz

Transmit Frequency Accuracy: 0.1%. **Transmit Level:** -12dbm.

Receive Frequency		ORIG	ANSW
	MARK	2225 Hz	1270 Hz
	SPACE	2025 Hz	1070 Hz

Carrier Detect Threshold: -44 dbm, plus or minus 2 dbm (ORIG). / -46 dbm, plus or minus 2 dbm (ANSW). **Carrier Detect Indicator:** Audible Tone. **Power Requirement:** Self-Contained — 9V Transistor Battery* / 110VAC Through Adapter*. **Mechanical:** 8" x 4" x 1" *Not Included

ANCMK1 **$129.00**

GSC LOGIC PROBES

LP-1 LOGIC PROBE - Hand-held logic probe provides instant reading of logic levels for TTL, DTL, HTL or CMOS. **INPUT IMPEDANCE:** 100,000 Ohms. **Min. Detectable Pulse:** 50 ns. **Max Input Signal (Frequency):** 10 MHz. **Pulse Detector (LED):** *High* speed train or single event. **Pulse Memory:** Pulse or level transition detected and stores.

GSCLP1 . . . . . . List $50.00 **Our Price $45.00**

LP-2 LOGIC PROBE - Economy version of Model LP-1 Saterthan a voltmeter, ore accurate than a scope. **Input Impedance:** 300,000 Ohms. **Min Detectable Pulse:** 300 ns **Max. Input Signal (Frequency):** 1.5 MHz. **Pulse Detector(LED):** High speed train or single event. **Pulse Memory:** none.

GSCLP2 . . . . . . List $32.00 **Our rice $30.00**

LP-3 LOGIC PROBE - High speed logic probe. Captures pulses as short as 10 ns. **Input Impedance:** 500,000 Ohms. **Minimum Detectable Pulse:** 6 ns. **Max Input Signal (Frequency):** 60 MHz. **Pulse Detector (LED):** High speed train or single event. **Pulse Memory:** Pulse or level transition detected and stored.

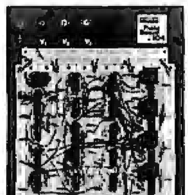
GSCLP3 . . . . . . List $77.00 **Our Price $69.00**

DIGITAL PULSER

GSCDP1 . . . . . . List $83.00 **$76.00**

GSCLTC-1 Logical Analysis Kit - Complete with LP-1 logic Probe, DP-1 Logic Pulser, LM-1 Logic Monitor wiring accessories, manuals and molded case. . . . . . . **Our Price $220.00**

GSCLTC-2 Logical Analysis Kit - For high-speed and memory analysis. Same as Model LTC-1, except substitutes LP-3 High-Speed Logic Probe . . . . . . **Our Price $245.00**

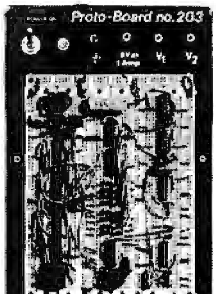


GSC PROTO-BOARD UNITS

All the speed and convenience of QT sockets and Bus Strips plus backplanes and binding posts in both kits and pre-assembled units. Assemble, test and modify circuits as fast as you can think.

Part No.		Dip Capacity	Board Size Inches	Price
GSCPB6	Kit	10(14's)	6 x 4 x ¼	$19.95
GSCPB100	Kit	10(14's)	4½ x 6 x ¼	$21.95
GSCPB101	ASM	10(14's)	6 x 4½ x ¼	$28.95
GSCPB102	ASM	12(14's)	7¼ x 4½ x ¼	$34.95
GSCPB103	ASM	24(14's)	9 x 6 x ¼	$59.95
GSCPB104	ASM	32(14's)	9⅛ x 8 x ¼	$77.00

PROTO-BOARD PB-203 - HOLDS 24 14-PIN IC's



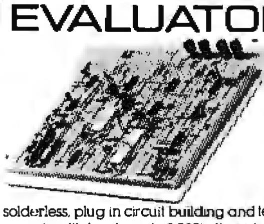
Fully assembled breadboard contains built-in, short-proof, fused, 5VDC at 1 amp, regulated power supply, in addition to three QT-59S sockets, four QT-59B bus strips, one QT-47B bus strip and four binding posts. Capacity for most digital and many analog projects. **SIZE:** 9.75" Lg, 6.6" w, 3.25" h **WEIGHT:** 5 lbs.

GSCPB203 . . . . . . List Price $133.00
OUR PRICE $125.00

GSCPB203A . . All features plus ±15VDC @ 500mA . . $174.00
Our Price $160.00

GSCPB203AK . . . . . Kit version of the 203A $149.95
Our Price $138.00

AP ALL-CIRCUIT EVALUATORS



Ace for fast, solderless, plug in circuit building and testing. Plug in any components with leads up to 0.032" diameter. Interconnect with solid wire up to 20 gauge. Gold-anodized aluminum base/ground. Non corrosive nickel silver terminals. 4 rubber feet.

PART NO.	ACE MODEL NO.	DIP CAPACITY	TIE POINTS	NO. BUSES	NO. POSTS	PRICE EACH
923333	200-K (kit)	8	728	2	2	$22.75
923332	208 (assem)	8	872	8	2	$30.70
923334	201-K (kit)	12	1032	2	2	$29.95
923331	212 (assem)	12	1224	8	2	$37.05
923326	218 (assem)	18	1760	10	2	$49.80
923325	227 (assem)	27	2712	28	4	$63.55
923324	236 (assem)	36	3648	36	4	$84.75

PRIORITY ONE ELECTRONICS

BUY WITH CONFIDENCE
From the Nation's Largest

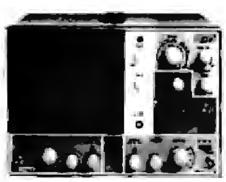
HITACHI Hitachi Denshi, Ltd. **Distributor**

Single and dual trace, 15 thru 100 MHz. All high sensitivity Hitachi oscilloscopes are built to demanding Hitachi quality standards and are backed by a 2-year warranty. They're able to measure signals as low as 1mV/division (with X5 vertical magnifier). It's a specification you won't find on any other 15 or 30 MHz scopes. Plus Z-axis modulation, trace rotation, front panel X-Y operation for all scopemodels, and X10 sweep magnification. And, 30 thru 100 MHz oscilloscopes offer internal signal delay lines. For ease of operation, functionally related controls are grouped into three blocks on the color coded front panel. Now here's the clincher: For what you'd expect to pay more, you actually pay less. Check our scopes before you decide. All scopes complete with probes.

HITV302B List $995.00

30 MHz DUAL TRACE OSCILLOSCOPE

Our Price: $859.00

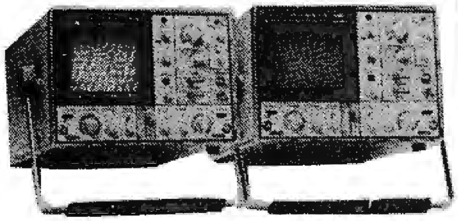


- TV sync-separator circuit
- High-sensitivity 1mV/div (5MHz)
- Sweep-time magnifier (10 times)
- Z-axis input (intensity modulation)
- Signal delay line
- Complete with 2 probes
- CH1, CH2, DUAL, ADD DIFF, Vertical Deflection Modes
- X-Y operation
- Trace Rotation

Hitachi . . . The measure of quality.

HITV152B DUAL TRACE 15MHZ (no delay)

LIST $735.00 **OUR PRICE $650.00**



HIT-V352
35MHz DUAL TRACE WITH DELAY
LIST PRICE $1150.00
OUR PRICE: $998.00

- Economically priced dual trace oscilloscope
- Square CRT with internal graticule (illuminated scale)
- High-accuracy voltage axis & time axis set at ±3% (certified at 10° to 35° C)
- **High-sensitivity 1mV/div.**
- **Low drift**
- **2 Year Warranty**

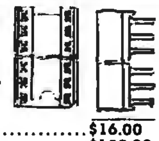
HIT-V202
20MHz DUAL TRACE
LIST PRICE: $850
OUR PRICE: $765

- Dynamic range 8 div.
- TV sync separator circuit
- Built-in signal delay line (V-352)
- X-Y operation
- Sweep-time magnifier (10 times)
- Trace rotation system
- Fine adjusting, click-positioning function

50 MHz & 100 MHz DUAL TRACE WITH CALIBRATED TIME DELAY

HIT V550B	HIT V1050
50MHz with 3rd TRACE TRIGGER VIEW	100MHz with 3rd & 4th TRACE TRIGGER VIEW
LIST $1745.00	LIST $2390.00
SALE $1495.00	SALE $1995.00

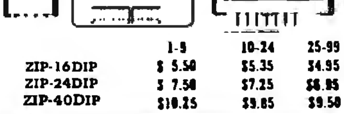
SPECIAL PURCHASE GOLD 16 PIN LOW PROFILE IC. C95 SOCKETS



TIG-16LP pkg of 100	$16.00
TIG-16LP pkg. of 1000	$120.00

OEMS Stock up at this LOW PRICE

ZERO INSERTION FORCE TEST SOCKETS



	1-9	10-24	25-99
ZIP-16DIP	$ 5.50	$5.35	$4.95
ZIP-24DIP	$ 7.50	$7.25	$6.85
ZIP-40DIP	$10.25	$9.85	$9.50

MICROCOMPUTER PRODUCTS

MEMORY

PART NO.	PRICE
4116AC20	8/$20.00
2016P3	8/$100.00
2114N3L	8/$28.00
5257N3L	8/$50.00
2732	8/$120.00
2716	8/$50.00
2708	8/$20.00

Z80 SERIES

Z80A	$14.95
Z80AP10	$14.95
Z80ACTC	$13.95
Z80ADMA	$45.00
Z80AS100	$59.95
Z80AS101	$59.95
Z80AS102	$59.95

UARTS

AY51013A	$5.95
TR1602B	$5.95
TR1863	$6.95
IM6402	$7.95

8080 SERIES

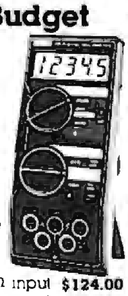
PART NO.	PRICE
INS 8080A	$5.50
INS 8085A	$19.95
DP8212N	$2.95
DP8214N	$5.25
DP8216N	$2.95
DP8224N	$3.25
DP8224-4N	$9.95
DP8226N	$3.50
DP8228N	$5.55
DP8238N	$5.55
INS8250N	$15.00
INS8251N	$7.50
INS8253N	$17.95
INS8255N	$6.80
INS8257N	$16.45
INS8259N	$18.00
INS8275N	$59.95
INS8279N	$49.95

FLOPPY DISC CONTROLLER

FD1771B-01	$24.95
FD1791B-01	$44.95

KEITHLEY

Handheld DMMs For Every Application and Budget



- Easy to-use Rotary Switches
- Large 0.6" LCD displays
- dc Voltage
- ac Voltage
- dc Current
- ac Current
- Resistance
- Diode Test
- 3½ or 4½ Digit Accuracy
- Overload Protection
- Externally Accessible Battery & Fuse
- Rugged 0.1" ABS Plastic Case
- Shock-Mounted PC Board

KTH130	± 0.5% DCV accuracy, 10M Ω input impedence auto polarity and current measurement through 10A	$124.00
KTH131	Same as KTH130 except 0.25% accuracy and enhanced bandwith on top ACV ranges	$139.00
KTH128	See/hear display includes both over/under threshold indicator arrows, audible tone that operates on all ranges & functions, and adjustable threshhold	$139.00
KTH135	4½ digit, 0.05% accuracy	$235.00
KTH870	Thermocouple (TC) based themometer	$199.00
KTH1304	Soft Carrying Case & Stand (handhelds)	$ 10.00
KTH1306	Deluxe Carrying Case (handhelds)	$ 25.00

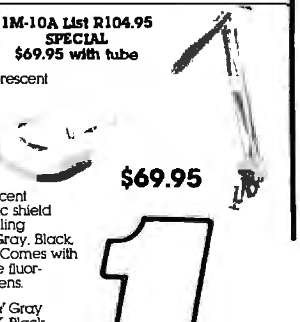
LCD & LED Bench DMMs

KTH169	3½ Digit, LCD Display	$189.00
KTH176	4½ Digit, LCD Display	$269.00
KTH179-20A	4½ Digit, LED Display, TRMS	$439.00
KTH1793	IEEE-488 Interface (Model 179-20A)	$325.00

See pp. 42-43 of our Engineering Selection Guide in the November BYTE for a complete list of specifications and accessories

LEDU

IM-10A List R104.95 SPECIAL $69.95 with tube



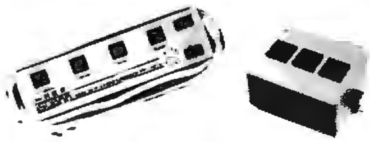
Perfectly balanced fluorescent lighting with precision magnifier lens. Tough thermoplastic shade. Easy lens removal. New wire clip design permits easy installation and removal of fluorescent tube. Comes with plastic shield to protect tube from soiling and damage. Colors: Gray, Black, and Chocolate Brown. Comes with one 22 watt T-9 Circline fluorescent tube, 3 diopter lens. 10 lbs.

$69.95

LDUIM10GY Gray
LDUIM10BK Black
LDUIM10CB Brown

GSC ISOBAR 1

With Built-In Noise Filters and Surge Suppressors



ISOLATES SENSITIVE AND VALUABLE EQUIPMENT FROM: Equipment interaction - Damaging High Voltage Spikes - AC line noise and hash.
PROTECTS AGAINST: Voltage transients caused by lightning, contact switching, turn-off of inductive components, noise due to electromagnetic coupling.
USE THE GSC ISOBAR TO ISOLATE: Microprocessor from peripherals - Lab instruments from noisy equipment - Sensitive pre-amp or tape deck from power amplifier.
THE GSC ISOBAR ELIMINATES: Equipment interaction - Equipment damage from power line spikes and surges - Errors - False printouts - Disk Skips - Audio or video hash.
FEATURES: Inuctive isolated ground - Sockets individually filter isolated - Circuit breaker protected at 15A
VOLTAGE TRANSIENT SPIKE PROTECTION: 2000 A peak for up to 6 Sec duration spikes. 1000A, 8/20 Sec protection from repeated spikes.
LOAD HANDLING: 1875 W max. total load; 15A per socket.
INPUT: 125 VAC, 15 amps; standard 3-prong plug.

Three common outlets built-in circuit breaker, pilot light, hang-up bracket and a 6 foot cord.

		LIST PRICE	OUR PRICE
GOFIBAR3	SH. WT. 3 lbs.	$59.95	$39.95

IBAR 46 - Four independently isolated outlets. Built-in 15A circuit breaker, pilot light, switch, and 6 foot cord

GOFIBAR46	SH. WT. 4 lbs.	$79.95	$49.95

IBAR 86 - 8 outlets, grouped to form 4 independently isolated sets of two. Built in 15A circuit breaker, on/off switch, pilot light.

GOFIBAR86	SH. WT. 5 lbs.	$84.95	$54.95

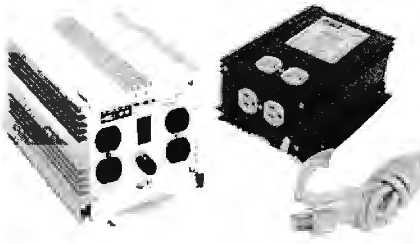
IBAR 9RM - Eight rear-mounted outlets grouped to form four independently isolated sets of two, plus one non-isolated convenience outlet on front face. 19" rack mount cabinet. Built in 15A circuit breaker, pilot light, on/off switch, and 6 foot cord

GOFIBAR9RM	SH. WT. 6 lbs.	$99.95	$74.95

GSC POWERMATE

LINE STABILIZERS

FULLY AUTOMATIC LINE REGULATION OVER AN 85V AC TO 125V AC INPUT RANGE, 15 AMP LOAD CAPACITY



TRA SERIES SPECIFICATIONS

- Constant 115V AC output.
- 4% output regulation for all combined effects of line and load
- 4 or 6 ground 3 prong outlets
- 6 ft. 14 gauge - 3 conductor power cord.
- Fully protected against overload.
- Rugged anodized aluminum case.
- Designed for direct wall or floor mounting, or bench top use.

		LIST PRICE	OUR PRICE
TRA650 500 WATTS, 4 RECEPTICLES			
GOFTRA650	SH. WT. 10 lbs.	$79.95	$69.95
TRA1150 1000 WATTS 4 RECEPTICLES			
GOFTRA1150	SH. WT. 20 lbs.	$159.95	$139.95
TRA1650 1500 WATTS, 6 RECEPTICLES			
GOFTRA1650	SH. WT. 20 lbs.	$239.95	$210.00

VISA MEMBER MITA master charge NEDA

PRIORITY ONE ELECTRONICS
9161-B DEERING AVE ● CHATSWORTH, CA 91311
ORDER TOLL FREE (800) 423-5922 CA, AK, HI CALL (213) 709-5464

Terms U.S. VISA, MC, BAC, Check Money Order, U.S. Funds Only. CA residents add 6% Sales Tax. MINIMUM PREPAID ORDER $15.00. Include MINIMUM SHIPPING & HANDLING of $2.50 for the first 3 lbs. plus 25¢ for each additional pound. Orders over 50 lbs. sent freight collect. Just in case, please include your phone no. Prices subject to change without notice. We wil do our best to maintain prices through January, 1982. Credit Card orders will be charged appropriate freight. See November BYTE for 60 page Catalog or send $1.00 for your copy today. Sale prices are for prepaid orders only.

WIRE WRAPPING TOOLS AND WIRE

"HOBBY" WIRE WRAPPING TOOL BATERY POWERED

For .025" (0.63mm) sq post "MODIFIED" wrap, positive indexing anti-overwrapping device.

OKMBW2630	Tool	$21.95
OKMBC1	Batteries and Charger	$14.95
OKMBT30	Bit for AWG 30	$ 4.19
OKMBT2628	Bit for AWG 26-28	$ 6.49

Use "C" size NICAD Batteries, not included

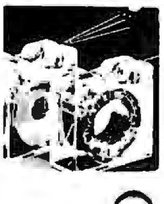
OKMWSU30M	Modified Wrap	$8.49

BW928 INDUSTRIAL WRAPPING TOOL GREAT FOR PRODUCTION!

- Accepts Industrial Bits & Sleeves (Gardner Denver or equivalent)
- Auto-Indexing
- Modified Wrap
- Back-Force available (Recommended for #30)

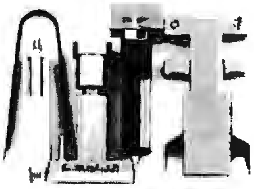
PART NO.	DESCRIPTION	PRICE:
OKMBW928	Tool	$64.95
OKMBW928BF	Tool (with Backforce)	$69.95
OKMBT301	#30 Bit and Sleeve	$34.95
OKMBCI	Batteries & Charger	$14.95

TRI-COLOR DISPENSER



- 3 Rolls of Wire in one dispenser
- 3 Colors Blue, White, Red 50 ft. of each color
- AWG 30 (0.25mm) KYNAR Insulated Wire
- Built-in Plunger cuts wire to desired length
- Built-in Stripper strips 1" of insulation
- Refillable (for refills, see below)

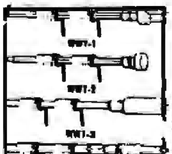
OKMWO30TRI	Tri-Color Dispenser	$6.49
OKMR30TRI	Replacement Rolls	$6.49



WK-7 IC INSERTION

OKMWK 7	Complete IC Inserter/Extractor Kit	$34.95
	INDIVIDUAL COMPONENTS	
OKMMOS1416	14-16 Pin MOS CMOS Safe Inserter	$ 6.95
OKMMOS2428	24-28 Pin MOS CMOS Safe Inserter	$ 6.95
OKMMOS40	36-40 Pin MOS CMOS Safe Inserter	$ 9.95
OKMEX1	14-16 Pin Extractor Tool	$ 1.95
OKMEX2	24-40 Pin CMOS SAfe Extractor Tool	$ 9.95
OKMINS1416	14-16 Pin Dip/IC Inserter	$ 3.95

TERMINALS

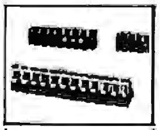


- .025" (0.63mm) Square Post
- 3 Level Wire-Wrapping
- GoldPlated — 25 per Pkge.

OKMWWT1	Slotted Terminal	$6.29
OKMWWT2	Single Sided Termi al	$3.79
OKMWWT3	IC Socket Terminal	$6.29
OKMWWT4	DBL Sided Terminal	$2.19

TERMINAL INSERTING TOOL FOR ABOVE: OKMINS1 $2.98

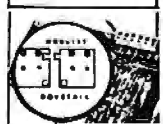
P.C.B. TERMINAL STRIPS



The TS strips provide positive screw activated clamping acdtion, accomodate wire sizes 14-30 AWG (1.6-0.24mm) Pins are solder plated copper. .042 inch (1mm) diameter on 200 inch (5mm) centers.

OKMTS4	4-Pole	$1.96
OKMTS8	8-Pole	$2.96
OKMTS12	12-Pole	$3.96

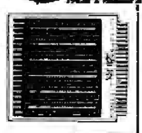
MODULAR TERMINAL STRIPS



The space-saving terminals take conductors from 26 through 16 AWG conforming to 20 inch (5.08mm) hole spacing on board up to .126 inch (3.20mm) thick.

OKMTS6MD	2-Pole	$2.19

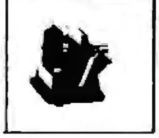
PC BOARD



The 4 x 4.5 x 1/16 inch board is made of glass coated EPOXY Laminated and features solder coated 1 oz copper pads. The board has provision for a 22/44 two sided edge connector with contacts on standard 156 spacing.

OKMHPCB1	Hobby Board	$5.49

VACUUM VISE



Unique vacuum based light duty vise for precision handling of small components and assemblies. Rugged ABS construction 1½" (38mm) width jaws, 1¼ (32mm) travel for maximum versatility. Also features crew lugs for permanent installation (mounting screws included)

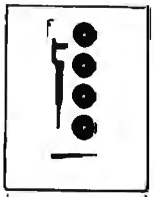
OKMVV1	Vacuum Vise	$3.79

WHY CUT? WHY STRIP? WHY SLIT? WHY NOT . . JUST WRAP

- AWG 30 Wire
- .025" Square Posts
- Daisy Chain or Point to Point
- No Stripping or Slitting Required . JUST WRAP
- Built in Cut Off
- Easy Loading of Wire
- Available Wire Colors Blue, White, Red & Yellow

Just Wrap Tool With One 50 Ft Roll of Wire

COLOR	PART NO.	LIST
Blue	OKMJWB	$15.95
White	OKMJWW	$15.95
Yellow	OKMJWY	$15.95
Red	OKMJWR	$15.95

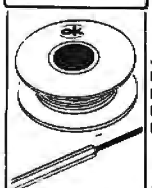


JUST WRAP KIT

CONTAINS

- JUST WRAP Tool
- Roll of Blue Wire, 50 ft
- Roll of White Wire, 50 ft
- Roll of Yellow Wire, 50 ft.
- Roll of Red Wire, 50 ft
- Unwrapping Tool

OKMJWK6	JUST WRAP Kit	$26.95



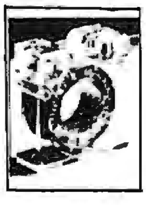
JUST WRAP REPLACEMENT ROLLS

OKMRJWB	Blue Wire	50 ft. roll	3.49
OKMRJWW	White Wire	50 ft. roll	3.49
OKMRJWY	Yellow Wire	50 ft. roll	3.49
OKMRJWR	Red Wire	50 ft. roll	3.49

UNWRAP TOOL FOR JUST WRAP

OKMJUW1	Unwrapping Tool	3.79

WIRE DISPENSER



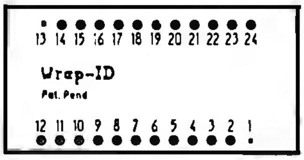
- With 50 ft. Roll of AWG 30 KYNAR wire-wrapping wire
- Built-in Plunger cuts wire to desired length
- Built-in Stripper strips 1" of insulation
- Refillable (For refills, see below)

OKMWO30B	Blue Wire	$5.49
OKMWO30Y	Yellow Wire	5.49
OKMWO30W	White Wire	5.49
OKMWO30R	Red Wire	5.49

DISPENSER REPLACEMENT ROLLS

Wire for wire-wrapping AWG-30 (0.25mm) KYNAR wire 50 ft. roll, silver plated solid conductor, easy stripping.

PGS050U	30-AWG Blue 50 ft. roll	$3.49
PGS050Y	30-AWG Yellow 50 ft. roll	3.49
PGS050W	30-AWG White 50 ft. roll	3.49
PGS050R	30-AWG Red 50 ft. roll	3.49



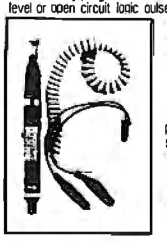
SOCKET WRAP — ID

Slipped onto socket before wrapping to identify pins

PART NO.	PKG. QTY.	PRICE	PART NO.	PKG. QTY.	PRICE
OKM1410	10	$1.69	OKM1410100	100	$8.95
OKM1610	10	1.69	OKM1610100	100	8.95
OKM1810	10	1.69	OKM181050	50	8.95
OKM2010	5	1.69	OKM201050	50	8.95
OKM2410	5	1.69	OKM241050	50	9.95
OKM2810	5	1.69	OKM2850	50	9.95
OKM4010	5	1.69	OKM4025	25	8.95

PRB-1 DIGITAL LOGIC PROBE

Compatible with all logic families using a 4 to 15V power supply. Threshholds automatically programmed. Visual indication of logic levels to show high, low, bad level or open circuit logic pulses.



- 10 nsec. pulse responses
- 120K input impedance
- Automatic resetting memory.
- Includes tip with protective cap & coiled cord

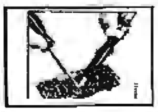
PSL-1 LOGIC PULSAR

Superimposes a pulse train (20pps) or a single pulse onto the circuit node under test without unsoldering IC's

- Automatic polarity sensing
- 2 us pulse width
- Finger tip push button actuated
- Includes tip with protective cap & coiled cord

OKMPRB1	Digital Logic Probe	$39.95
OKMPLS1	Logic Pulser	$54.95

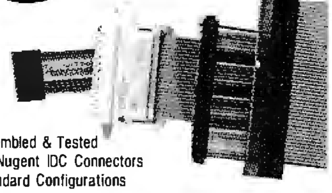
PI DESOLDERING PUMP



Easy one hand operation. Rugged all metal construction. Replaceable TEFLON Tip. Self Cleaning on each stroke. Suction precisely regulated for reliable desoldering without damage to delicate circuitry.

PART NO.	DESCRIPTION	PRICE
OKMPI	Desoldering Pump	$11.95

page ASSEMBLED AND TESTED CABLES



- Fully Assembled & Tested
- Robinson-Nugent IDC Connectors
- Many Standard Configurations
- Custom lengths and combinations available

DIP JUMPERS

Available with 14, 16, 24 and 40 contacts. Mates with standard IC socket.

PGC 14P36	14 PIN DIP JUMPER 36"SGL	$ 4.00
PGC 14P06P	14 PIN DIP JUMPER 06"DBL	$ 4.60
PGC 14P12P	14 PIN DIP JUMPER 12"DBL	$ 4.75
PGC 14P18P	14 PIN DIP JUMPER 18"DBL	$ 4.95
PGC 14P24P	14 PIN DIP JUMPER 24"DBL	$ 5.10
PGC 14P36P	14 PIN DIP JUMPER 36"DBL	$ 5.50
PGC 16P36	16 PIN DIP JUMPER 36"SGL	$ 4.50
PGC 16P06P	16 PIN DIP JUMPER 06"DBL	$ 4.90
PGC 16P12P	16PIN DIP JUMPER 12"DBL	$ 5.20
PGC 16P18P	16 PIN DIP JUMPER 18"DBL	$ 5.40
PGC 16P24P	16 PIN DIP JUMPER 24"DBL	$ 5.65
PGC 16P36P	16 PIN DIP JUMPER 36"DBL	$ 6.05
PGC 24P36	24 PIN DIP JUMPER 36"SGL	$ 6.50
PGC 24P06P	24 PIN DIP JUMPER 06"DBL	$ 7.50
PGC 24P12P	24 PIN DIP JUMPER 12"DBL	$ 7.75
PGC 24P18P	24 PIN DIP JUMPER 18"DBL.	$ 8.05
PGC 24P24P	24 PIN DIP JUMPER 24"DBL	$ 8.35
PGC 24P36P	24 PIN DIP JUMPER 36"DBL	$ 8.95
PGC 40P36	40 PIN DIP JUMPER 36"SGL.	$10.50
PGC 40P06P	40 PIN DIP JUMPER 06"DBL.	$11.35
PGC 40P12P	40 PIN DIP JUMPER 12"DBL	$11.65
PGC 40P18P	40 PIN DIP JUMPER 18"DBL	$12.35
PGC 40P24P	40 PIN DIP JUMPER 24"DBL	$12.80
PGC 40P36P	40 PIN DIP JUMPER 36"DBL	$13.75

CARD EDGE JUMPERS

Mate with standard 0.62" PC boards

PGC 20E36	20 PIN CARD EDGE 36"SGL	$ 7.25
PGC 20E36E	20 PIN CARD EDGE 36"DBL.	$10.95
PGC 26E36	26 PIN CARD EDGE 36"SGL.	$ 8.50
PGC 26E36E	26 PIN CARD EDGE 36"DBL	$12.40
PGC 34E36	34 PIN CARD EDGE 36"SGL.	$10.50
PGC 34E36E	34 PIN CARD EDGE 36"DBL	$15.15
PGC 40E36	40 PIN CARD EDGE 36'SGL.	$12.25
PGC 40E36E	40 PIN CARD EDGE 36"DBL	$17.50
PGC 50E36	50 PIN CARD EDGE 36"SGL.	$15.00
PGC 50E36E	50 PIN CARD EDGE 36"DBL.	$21.65

SOCKET JUMPERS

Mates with two rows of posts on .100" centers

PGC 20S36	20 PIN SOCKET 36"SGL.	$ 5.50
PGC 20S36S	20 PIN SOCKET 36"DBL	$ 7.50
PGC 26S36	26 PIN SOCKET 36"SGL	$ 6.95
PGC 26S36S	26 PIN SOCKET 36"DBL	$ 9.40
PGC 34S36	34 PIN SOCKET 36"SGL.	$ 8.65
PGC 34S36S	34 PIN SOCKET 36"DBL.	$11.90
PGC 40S36	40 PIN SOCKET 36"SGL.	$10.35
PGC 40S36S	40 PIN SOCKET 36"DBL	$13.40
PGC 50S36	50 PIN SOCKET 36"SGL.	$12.75
PGC 50S36S	50 PIN SOCKET 36"DBL	$17.05

"D" CONNECTORS

Mates with any standard female DB25 "D" Subminiature Connector

PGC 25DP36	25 PIN IDB25P 36"SGL.	$12.00
PGC 25DP06DP	25 PIN IDB25P 06"DBL	$17.95
PGC 25DP12DP	25 PIN IDB25P 12"DBL	$18.25
PGC 25DP18DP	25 PIN IDB25P 18"DBL	$18.55
PGC 25DP24DP	25 PIN IDB25P 24"DBL	$18.65
PGC 25DP36DP	25 PIN IDB25P 36"DBL	$19.45
PGC 25DP60DP	25 PIN IDB25P 60"DBL	$20.65

SPECIAL COMBINATIONS

Designed to meet the needs of computer I/O and Floppy Disk interfacing.

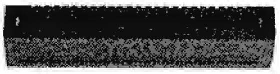
PGC 26S06DS	26 PIN SOCKET/25 PIN IDB25S 06"	$13.70
PGC 26S12DS	26 PIN SOCKET/25 PIN IDB25S 12"	$14.05
PGC 26S18DS	26 PIN SOCKET/25 PIN IDB25S 18"	$14.35
PGC 26S24DS	26 PIN SOCKET/25 PIN IDB25S 24"	$14.65
PGC 26S36DS	26 PIN SOCKET/25 PIN IDB25S 36"	$15.30
PGC 25S60DS	26 PIN SOCKET/25 PIN IDB25S 60"	$16.55
PGC 25DP06DS	25 PIN IDB25P/IDB25S 06"	$18.80
PGC 25DP12DS	25 PIN IDB25P/IDB25S 12"	$19.10
PGC 25DP18DS	25 PIN IDB25P/IDB25S 18"	$19.40
PGC 25DP24DS	25 PIN IDB25P/IDB25S 24"	$19.75
PGC 25DP36DS	25 PIN IDB25P/IDB25S 36"	$20.35
PGC 25DP60DS	25 PIN IDB25P/IDB25S 60"	$21.60
PGC 50E06S	50 PIN CARD EDGE/SOCKET 06"	$16.35
PGC 50E12S	50 PIN CARD EDGE/SOCKET 12"	$16.95
PGC 50E18S	50 PIN CARD EDGE/SOCKET 18"	$17.55
PGC 50E24S	50 PIN CARD EDGE/SOCKET 24"	$18.15
PGC 50E36S	50 PIN CARD EDGE/SOCKET 36"	$19.35
PGC 50E60S	50 PIN CARD EDGE/SOCKET 60"	$21.75
PGC 34S48E30E	34 PIN SOCKET/CARD EDGE 48"/30"	$22.95
PGC 34S60E30E	34 PIN SOCKET/CARD EDGE 60"/30"	$23.95
PGC 50S48E30E	50 PIN SOCKET/CARD EDGE 48"/30"	$31.95
PGC 50S60E30E	50 PIN SOCKET/CARD EDGE 60"/30"	$32.95
PGC 34S48EX4	34 PIN SOCKET/EDGE CARD X 4	$34.95
PGC 34S60EX4	34 PIN SOCKET/EDGE CARD X 4	$35.95
PGC 50S48EX4	50 PIN SOCKET/EDGE CARD X 4	$51.95
PGC 50S60EX4	50 PIN SOCKET/EDGE CARD X 4	$52.95

PRIORITY ONE ELECTRONICS

Connectors, Plugs, and Sockets

RN ROBINSON NUGENT, INC.

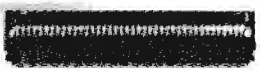
EDGECARD CONNECTOR



.1" Spacing. Crimps onto cable with ordinary vise & mates with standard .062" Card Edge.

PART NO.	NO. OF PINS	1-9	10-24	25-99	100-249
RNIDE20	10/20	4.35	4.00	3.30	3.00
RNIDE26	13/26	5.00	4.50	5.75	3.25
RNIDE34	17/34	6.00	5.40	4.50	4.00
RNIDE40	20/40	6.90	6.20	5.30	4.80
RNIDE50	25/50	7.25	6.80	5.90	5.30

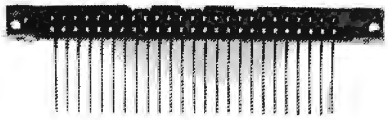
SOCKET CONNECTOR



.1" Spacing. Crimps onto cable with ordinary vise & mounts to header sold

PART NO.	NO. OF PINS	1-9	10-24	25-99	100-249
RNIDS20	10/20	2.75	2.50	1.65	1.70
RNIDS26	13/26	3.50	3.20	2.40	2.20
RNIDS34	17/34	4.50	4.20	3.10	2.90
RNIDS40	20/40	5.40	5.00	3.65	3.30
RNIDS50	25/50	6.50	6.00	4.60	4.20

HEADER CONNECTOR



.1" Spacing. Mounts on PC Board & Mates with IDS Socket above.

RIGHT ANGLE SOLDERTAIL GOLD HEADER

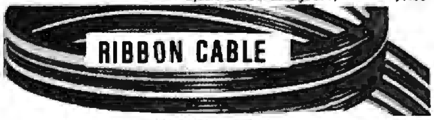
PART NO.	1-9	10-24	25-99	100-249
RNSIDH20SR	1.90	1.60	1.20	1.00
RNSIDH26SR	2.25	2.00	1.55	1.30
RNSIDH34SR	2.95	2.60	2.05	1.70
RNSIDH40SR	3.60	3.00	2.40	2.10
RNSIDH50SR	4.30	3.60	3.00	2.55

RIGHT ANGLE WIRE WRAP GOLD HEADER

PART NO.	1-9	10-24	25-99	100-249
RNIDH20WR	4.15	3.60	2.75	2.40
RNIDH26WR	5.30	4.30	3.60	3.10
RNIDH34WR	5.95	5.00	4.15	3.70
RNIDH40WR	7.00	6.00	4.90	4.30
RNIDH50WR	7.95	6.80	6.15	5.20

Straight headers are also available at the above prices.
Drop the R from the end of the part number to specify Straight.
RNIEJ24 Header Ejector Bars (Package of 4) $1.00

RIBBON CABLE



COLOR CODED LAMINATED CABLE FOR INSULATION DISPLACEMENT 28 GUAGE, 7 STRAND

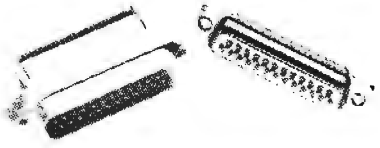
PART NO.	NO. OF CONDUCTORS	PRICE PER SPOOL /C 10 Ft.	100 Ft.
IDC09CC*	9	3.80	30.00
IDC14CC*	14	4.75	40.00
IDC16CC*	16	5.50	45.00
IDC20CC*	20	7.00	60.00
IDC25CC*	25	8.50	72.00
IDC26CC*	26	8.50	72.00
IDC34CC*	34	11.00	100.00
IDC40CC*	40	13.00	115.00
IDC50CC*	50	16.00	145.00

GRAY LAMINATED CABLE FOR INSULATION DISPLACEMENT 28 Gauge 7 Strand

PART NO.	NO. OF CONDUCTORS	PRICE PER SPOOL /C 10 Ft.	100 Ft.
IDC09GY*	9	2.50	18.05
IDC14GY*	14	3.50	26.00
IDC16GY*	16	4.00	32.00
IDC20GY*	20	4.80	40.00
IDC25GY*	25	6.00	50.00
IDC26GY*	26	6.00	50.00
IDC34GY*	34	8.30	66.00
IDC40GY*	40	10.00	77.00
IDC50GY*	50	12.00	95.00

*Add "/C" to Part No. for 100 Ft. Spool

D-SUBMINIATURE CONNECTORS



Solder Style solders onto cale, IDC. Style crimps onto cable with vise.

INSULATION DISPLACEMENT TYPE

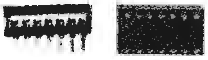
P = Plug, Male Type - S = Socket, Female Type - C = Cover Hood

PART NO.	NO. OF PINS	1-9	10-24	25-99	100-249
IDCDE9P	9	4.20	4.00	3.60	3.20
IDCDE9S	9	4.50	4.20	3.80	3.40
IDCDE9C	9	1.25	1.10	1.00	.95
IDCDA15P	15	4.35	4.20	3.75	3.40
IDCDA15S	15	5.00	4.85	4.35	3.90
IDCDA15C	15	1.40	1.25	1.10	.95
IDCDB 25P	25	6.25	6.00	5.20	4.70
IDCDB 25S	25	6.60	6.35	5.60	5.00
IDCDB 25C	25	1.60	1.50	1.35	1.20
IDCDC37P	37	8.80	8.00	7.20	6.40
IDCDC37S	37	11.00	10.25	9.20	8.20
IDCDC37C	37	2.25	2.20	1.80	1.60

SOLDER TYPE

PART NO.	DESCRIPTION	1-9	10-24	25-99
CNDDE9P	9 Pin Male	$2.10	$1.90	$1.70
CNDDE9S	9 Pin Female	$2.70	$2.40	$2.10
CNDDE9C	9 Pin Cover	$1.50	$1.25	$1.10
CNDDA15P	15 Pin Male	$2.75	$2.45	$2.15
CNDDA15S	15 Pin Female	$3.95	$3.60	$3.20
CNDDA15C	15 Pin Cover	$1.50	$1.30	$1.10
CNDDB25P	25 Pin Male	$3.00	$2.75	$2.25
★ CNDDB25P 100 pcs at $1.95 ea. ★				
CNDDB25S	25 Pin Female	$4.00	$3.75	$3.00
★ CNDDB25S 100 pcs at $2.95 ea. ★				
CNDDB51226	2 Pc. Black Hood	$1.90	$1.65	$1.45
★ CNDDB51226 100 pcs at $1.00 ea ★				
CNDDB51212	1 Pc. Grey Hood	$1.60	$1.45	$1.30
CNDP25H	2 Pc. Grey Hood	$1.50	$1.25	$1.10
CNDDC37P	37 Pin Male	$5.60	$5.10	$4.45
CNDDC37S	37 Pin Female	$8.70	$7.70	$6.70
CNDDC37C	37 Pin Cover	$1.80	$1.55	$1.30
CNDDD50P	50 Pin Male	$8.75	$7.75	$6.70
CNDDD50S	50 Pin Female	$11.65	$10.25	$8.90
CNDDD50S	50 Pin Cover	$2.00	$1.80	$1.60
CND0020418	Hardware Set 2 Pr.	$1.00	$ .80	$ .70
	RS232, DB25P, EIA			
CNDRS2328F	Class 1 Cable 8 Con. 8 Ft	$19.95	$17.95	$15.95
CN05730360	Cent. 700 Series/Epson Printer Conn.	$9.00	$7.50	$6.00
IDC5730360	IDC Version of Above	$9.95	$9.00	$8.00

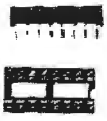
DIP PLUGS



.1" Spacing. Crimps onto cable with ordinary vise & plugs into standard I C Socket.

PART NO.	NO. OF PINS	1-9	10-24	25-99	100-249
RNIDP14	14	1.50	1.40	1.25	1.10
RNIDP16	16	1.70	1.60	1.45	1.30
RNIDP24	24	2.50	2.20	2.00	1.80
RNIDP40	40	4.15	3.65	3.30	3.00

RN ICU Series Solder Tail Sockets



End side stackable. Low profile Closed Entry. Lead Entry has RN "EZ" Entry feature to guide IC leads into socket. Standoff to facilitate board cleaning. Self lock leads hold socket firmly in place while soldering. Contact's long movement arm provides low insertion force. Normal force of contact combined with uncoiling force provide high retention (making socket vibration resistant). Gas tight. Tin Plated.

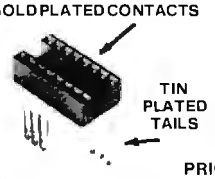
PART NO.	PINS	1-9	10-49	50-99	100-499	500-999	1,000+
RNS08LP	08	N/A	.15	.10	.08	.07	.06
RNS14LP	14	N/A	.18	.15	.14	.12	.11
RNS16LP	16	N/A	.20	.18	.16	.13	.12
RNS18LP	18	.30	.25	.22	.18	.15	.13
RNS20LP	20	.30	.25	.23	.20	.17	.145
RNS22LP	22	.35	.30	.25	.22	.19	.17
RNS24LP	24	.40	.35	.30	.24	.20	.18
RNS28LP	28	.45	.40	.35	.28	.24	.21
RNS40LP	40	.50	.45	.42	.40	.35	.31

*MINIMUM ORDER $1.00 Per Line Item
Call for RN High Reliability Solder Sockets

ICN SERIES GOLD 3 LEVEL WIRE WRAP SOCKETS

- 10 μ in GOLD Plated Pins
- Deep Chamfered Closed Entry Contacts
- RN Side Wipe Contact Design
- Phosphor Bronze Contact Material
- Terminal Barbs Allow Self-lock into PC Board
- Rugged Socket Body Design
- Deep Chamfered Closed Entry Contacts

PART NO.	PINS	1-9	10-24	25-99	100-249	250-999
RNS08WWG	8	.60	.55	.49	.45	.41
RNS14WWG	14	.75	.70	.65	.55	.48
RNS16WWG	16	.85	.75	.70	.60	.52
RNS18WWG	18	1.00	.90	.80	.75	.71
RNS20WWG	20	1.20	1.05	.96	.91	.87
RNS22WWG	22	1.35	1.25	1.15	1.05	.99
RNS24WWG	24	1.35	1.25	1.15	1.05	.99
RNS28WWG	28	1.70	1.55	1.40	1.34	1.25
RNS40WWG	40	2.20	2.05	1.85	1.60	1.50



NEW! SELECTIVE PLATED PINS THAT WILL SAVE YOU MONEY BY HAVING GOLD ONLY WHERE IT COUNTS! Same as above except pins are selectively plated.

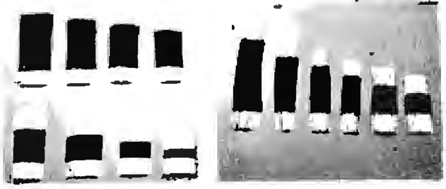
PART NO.	PINS	1-9	10-24	25-99	100-24	250-99
RNS08TWW	8	.55	.50	.45	.41	.37
RNS14TWW	14	.65	.55	.50	.47	.44
RNS16TWW	16	.75	.65	.52	.51	.46
RNS18TWW	18	.90	.79	.75	.70	.65
RNS20TWW	20	1.10	.95	.91	.87	.82
RNS22TWW	22	1.25	1.15	1.05	.94	.89
RNS24TWW	24	1.25	1.15	1.05	.96	.89
RNS28TWW	28	1.50	1.45	1.35	1.25	1.15
RNS40TWW	40	2.00	1.80	1.60	1.40	1.30

Call for RN High Reliability Wire Wrap Sockets

page

PRECUT WIRE WRAP WIRE

Precut Wire Save Time and Costs Less Than Wire on Spools



Kynar precut wire. All lengths are overall including 1" strip on each end. Colors and lengths cannot be mixed for quantity pricing. Choose from colors Red (R), Blue (U), Black (B) and Yellow (Y).

PART NO.	LENGTH	/C 100/Tube	/D 500/Tube	/M 1000/Tube
PGP025†*	2.5"	$1.38	$3.94	$6.19
PGP030†*	3.0"	1.43	4.25	6.78
PGP035†*	3.5"	1.51	4.57	7.37
PGP040†*	4.0"	1.56	4.88	7.94
PGP045†*	4.5"	1.63	5.21	8.54
PGP050†*	5.0"	1.69	5.54	9.13
PGP055†*	5.5"	1.74	5.92	9.72
PGP060†*	6.0"	1.82	6.23	10.31
PGP070†*	7.0"	2.19	7.44	12.44
PGP080†*	8.0"	2.35	8.12	13.79
PGP090†*	9.0"	2.46	8.92	15.01
PGP100†*	10.0"	2.63	9.58	16.28

† Specify package size when ordering: 100 (C), 500 (D), 1000 (M).
* Specify color when ordering. RED (R), BLUE (U), BLACK (B), & YELLOW (Y). Example: If you wish to order (2) pkg 1000 4". Red

2	PGP040MR	$7.94	$15.88

BUY PRECUT WIRE IN KITS AND SAVE

PGPWK1* $9.95 — CONTAINS

200	3"	100	4½"
200	3½"	100	5"
100	4"	100	6"

PGPWK2* $24.95 — CONTAINS

250	2½"	250	5"
500	3"	100	5½"
500	3½"	100	6"
500	4"	100	6½"
250	4½"	100	7"

PGPWK3* $34.95 — CONTAINS

250	2½"	500	4½"
500	3	500	5"
500	3½"	500	5½"
500	4"	500	6"

PGPWK4* $59.95 — CONTAINS

500	2½"	1000	4½"
1000	3"	1000	5"
1000	3½"	1000	5"
1000	4"	1000	6"

*Wire kit assortments are available in the 4 colors mentioned above along with a rainbow assortment. Use color code (A) for the rainbow assortment. Example: If you wish to order (2) wire kit 3 in blue

2	PGPWK3U	$34.95	$69.90

master charge VISA

PRIORITY ONE ELECTRONICS

9161-B DEERING AVE. • CHATSWORTH, CA 91311

MEMBER MTA NEDA

ORDER TOLL FREE (800) 423-5922 CA, AK, HI CALL (213) 709-5464

Terms: U.S. VISA, MC, BAC, Check, Money Order, U.S. Funds Only. CA residents add 6% Sales Tax. MINIMUM PREPAID ORDER $15.00. Include MINIMUM SHIPPING & HANDLING of $2.50 for the first 3 lbs. plus 25¢ for each additional pound. Orders over 50 lbs sent freight collect. Just in case, please include your phone no. Prices subject to change without notice. We will do our best to maintain prices through January, 1982. SOCKET and CONNECTOR prices based on GOLD, not exceeding $700.00 per oz. Credit Card orders will be charged appropriate freight.

Unclassified Ads

FOR SALE: AIM-65 with 4 K, assembler, BASIC, and new enclosure. In excellent working condition; $450. Assembled and working Video-I with 4 K, D/A, and A/D (A/D module needs work); $300. Both for $700. Also, video terminal; negotiable. Dave Troutt, 3261 Michigan Ave., Costa Mesa, CA 92626, (714) 546-7481.

FOR SALE: Amateur radio transceiver; 580-Delta, 9-band, TENTEC, solid state; $690. Power supply; $90. Will consider trade for computer equipment. H.D. Chapin, POB 1918, Fort Collins, CO 80522, (303) 484-4121

FOR SALE OR SWAP: H-P microprocessor training course. Complete in brand-new condition. Contains 5036A lab, 5004A signature analyzer, and 5024A logic probe kit. $2270 or swap for Tektronix 5658 oscilloscope. Walter Lindell, 757 Columbus Ave., San Francisco, CA 94133.

FOR SALE: OSI Challenger 1P, Series I (metal case), upgraded to 8 K, switch-selectable 1 or 2 MHz clock, tape read/write, print at 300, 600 and 1200 bps, and CEGMON PROM expanded monitor; $350. Variety of tape software, including OSI assembler/editor and extended monitor; $50. Mike Pichtelman, 72-61 113 St., Forest Hills, NY 11375, (212) 263-1221 evenings.

WANTED: TRS-80 Level II programs to swap: games, home, and business programs. Send tape, disk, or listing with your name and address. George Vandervort, POB 199, San Marcos, TX 78666.

FOR SALE: IBM Selectric I/O printer, correspondence code. With parallel interface (8 bits out, 1 bit in) and driver software for a 6502. Also, manuals and spare parts. $450 plus shipping. Al Thomason, 2544 Union #27, Klamath Falls, OR 97601, (503) 883-3278.

FOR SALE: Sinclair ZX80 personal computer in perfect condition. 16 K programmable memory, 8 K floating-point BASIC, and Z80A processor. Manual included, plus subscription to Sync, and all back issues. Clock speed is 3.25 MHz. $240 or best offer. Cost $350 new. Brad Konia, Spring Hill Farm, Easton, PA 18042, (215) 252-7134.

FOR SALE: C1P in good condition. With 8 K, case, power supply, manuals, BASIC instruction book, R/F modulator, cables, and demonstration tapes. Best offer takes all. Mike Kirk, 1205 Washington, Friona, TX 79035, (806) 247-3767 weekends.

FOR SALE: ADDS Regent 100 video terminal, like new; $600. US Robotics auto-answer/originate modem Model USR 320; $100. InterTec InterTube 3 video terminal, one-month old; $600. Jack Hardman, 600 Cortlandt St., Belleville, NJ 07109, (201) 751-3005.

WANTED: Nonprofit microcomputer club in France requests contacts with similar organizations in the United States and Great Britain, with special regard to software. We also seek reprint rights of magazines and benchmarks, and software for our organization's two radio stations. AMIF, 6 rue des Ormes, 94120 Fontenay-Sous-Bois, France.

FOR SALE: LSI-11/2 complete system. WH-11A with 64 K, three WH-11-5 serial cards, WH-27 dual 8-inch floppies, WH-14 printer, Hazeltine 1510 terminal, and AJ acoustic coupler. Runs UCSD Pascal or DEC PDP-11/03 software. Best offer. F. Monaco, 570 C. Connor Rd., West Point, NY 10996, (914) 446-4217.

WANTED: Hewlett-Packard HP-19 calculator in good condition. John Dilday, 621 Vickers Ave., Durham, NC 27701, (919) 682-1121

FOR SALE: Commodore PET computer, 8 K upgraded to 32 K, with tape drive, keyboard, and screen; $950. DeLinn Shields, 903 Enterprise Dr., Suite 1, Sacramento, CA 95825, (916) 929-7670

FOR SALE: H-8 64 K Trionyx board, H-8-5 interface, H-17 disk controller only, and H-P terminal (unmodified); $1200. Joe Cross, 8010 East Zimmerly, Wichita, KS 67207, (316) 685-8673.

FOR SALE: Heath H-8 computer, 8 K programmable memory, I/O interface board, H-9 video terminal, BASIC, Extended BASIC, editor, games, and documentation. $500. Al Meyer, 28 Skipper Dr., West Islip, NY 11795, (516) 422-0891.

FOR SALE: HP-2621A video-display terminal in original box with all manuals. This is a professional unit with two pages of memory, scroll up/down, previous/next page, addressing, editing, N-key rollover, auto repeat any key, and detached keyboard. It is capable of displaying control characters as a selectable mode. In mint condition. I pay shipping. $1095 takes it. Three Heath 8 K programmable-memory boards with DIP switches for address and one Heath WH-8-16 16 K programmable-memory board. All manuals, etc., included. Seven TMS 4044-4 4 K programmable-memory chips. I pay shipping. $419 takes it all. Brian Branson, 2255 Cahuilla Rd. #108, Colton, CA 92324, (714) 824-0144.

FOR SALE: Commodore PET Model 2001 with 8 K programmable memory, a self-contained cassette recorder, original documentation, Hayden's Basic BASIC book, and a cassette with many programs. $450, you pay shipping. Expand this PET with BETSI PET to S-100 interface with an Expando-Ram with 24 K of additional programmable memory. Also contains four 2 K PROM sockets. Includes power supply and documentation. An additional $300. John Lemkelde, 5980 Bull Rd., Dover, PA 17315, (717) 292-4933.

FOR SALE: ADDS Regent 200 editing terminal with protected fields, half-intensity, blinking, and reverse video. Like new; $750. North Star single-density disk controller and SA-400 minifloppy drive; $350. IMSAI PIC-8 priority interrupt controller and programmable clock. New; $75. IMSAI MPU-A 2.0 MHz processor card; $50. D. Sellar, 616 North Delaware Ave., Lindenhurst, NY 11757.

WANTED: Nonfunctional Hazeltine 1500 CRT, with or without tube, to be used as spare parts for my own flaky Hazeltine 1500. James Vliet, 32 Wesley St., Monmouth Beach, NJ 07750, (201) 222-4313 evenings.

FOR SALE: Compucolor Model 4, 16 K microcomputer with 101-key keyboard, eight-color display, Disk BASIC language, software, and manuals. Hardly used; $1000/offer. Kathy Silva, 2954 Kilkare Rd., Sunol, CA 94586, (415) 862-2146, 792-9800.

FOR SALE: Lear-Siegler ADM3A terminal with uppercase/lowercase read-only memories, 80 columns, 24 rows, absolute and indirect cursor addressing. Includes operator's manual. Excellent condition; $650. Shugart SA-801 8-inch floppy-disk drive with power supply and cabinet with fan. Includes manuals. Good condition; $550. Dave Gewirtz, (201) 796-3140.

FOR SALE: Drum memory, military airborne type. Over 100 R/W heads (no drive electronics), includes 110 VAC drive motor; $100 plus shipping. Also, Processor Technology programs on cassette (CUTS format), never used: Trek-80 (Startrek with sound), Software #1 (8080 assembler), and FOCAL language; $10 each. George Bonicatto, 5 Southview Dr., Apt. #D, Hibbing, MN 55746, (218) 263-5306 after 4 p.m.

FOR SALE: Digital Group Z80 computer (26 K) with dual Phi-Decks (extra controller board), printer B, full-function ASCII keyboard, video modulator, 32 K static (TMS-4044, etc.) bare board, and lots of software (including Sargon, Business BASIC, MaxiBASIC, Mini and Tiny BASIC, and games). Complete with full documentation, but no covers. Includes the Audio ROM and Phi ROM. $1500. D.M. Lazok, 1161 North Cherrywood Dr., East Layton, UT 84041, (801) 766-0885.

WANTED: S-100 adapter board, any type. Also, schematic and parts list for Processor Technology CUTS. I have some PT boards and want to interface with a single-board computer. Larry Bates, 39 Hanover St., Asheville, NC 28806.

FOR SALE: Complete S-100 video subsystem. Includes Polymorphic video terminal interface card, Sanyo 9-inch video monitor, Microage keyboard with 10-key pad, all cables and connectors, and complete documentation. Upgraded my system to VDT after 18 months of no-problem use. $350 takes it all. Joe Rothstein, 3529 Kaau St., Honolulu, HI 96816.

FOR SALE: TRS-80 Model I with expansion interface, 48 K, RS-232C, LNW double density, 80-Graphix, and Archbold speedup. Running over 6 months. Includes DOS plus 3.3D operating system. $1500 or best offer. Ithaca Intersystems S-100 2708/2716 EPROM board. Factory sealed with 16 K of 2708 EPROMs. Must sell. $150 or best offer. Mike Okrent, 11 Prince Dr., Bethany, CT 06525, (203) 393-2662.

FOR SALE: PET and Apple software by Soft Sector. Includes: 1. electrical engineering—ladder network analysis, active filter design (lowpass, highpass, bandpass, allpass), attenuator design, and Butterworth and Chebychev filter design; 2. audio engineering—passive crossover and inductor design, acoustic speaker design, and exponential horn design. For PET and Apple on disk and tape. Must sell. Send for complete program descriptions and sample printouts. R. Majef, 534 Apollo, Richardson, TX 75081

FOR SALE: Back issues of BYTE from September 1975 through June 1980. Highest reasonable bid. Gary Dawkins, 3523 Bunyan, San Antonio, TX 78247, (512) 494-5995.

FOR SALE: First 60 issues of BYTE (issue #1 through vol. 5, no. 8) in excellent condition. $120 plus shipping. Shipped only to areas served by UPS (shipping charges COD). Send name, address (no POB numbers), certified check or postal money order, and SASE for return of check. Sorry, will not sell partial set or return checks without SASE. David B. Lamkins, 56 Lakeshore Dr., Marlboro, MA 01752, (617) 481-6192 6 to 9 p.m. ET.

FOR SALE: H-17 floppy bare board (Heathkit) with all components, including read-only memory, hardware, and instruction manuals. No cable, disks, or cabinet. $95. Anthony J. Gasbarre, (603) 847-9797.

FOR SALE: H-11 32 K-byte memory board; $320. Two DLVII serial interface; $85 each. H-11 complete with 40 K-byte memory, DLVII, boot and memory test board, and LTC option; $1450. Mike Kennedy, 3630 South Kenwood Lane, Phoenix, AZ 85282, (602) 978-0748.

FOR SALE: Computer ideal for personal finances, beginners, and bright youngsters. Complete with video monitor, keyboard, multipurpose cassette recorder, blank cassettes, prerecorded game cassettes, comprehensive how-to manuals, creative graphics book, eight-lesson cassette instruction course, and all necessary connection cables. Assembles in 15 minutes. Lots of software available. Complete package for $400 or best offer. Mike Sutherland, 419 East Pershing St., Appleton, WI 54911

FOR SALE: Scantron optical mark reader Model 5098-2. Good for reading test answer sheets, other data records, etc. Three years old; factory reconditioned. Excellent operating condition. $1200 or best offer. Municipal Personnel Service, 1675 Green Rd., Ann Arbor, MI 48105, (313) 662-3246.

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Readers Vote IBM Number One

It looks like our article on the IBM Personal Computer really hit the spot. Philip Lemmons' report, "The IBM Personal Computer: First Impressions," was voted number one by our readers. Phil will receive the $100 kitty. Steve Ciarcia placed second with his article, "Build an Intelligent EPROM Programmer." He'll receive $50. As Steve put it, it's not so bad taking second place to IBM. A close third place goes to Ken Clements and Dave Daugherty for "Ultra-Low-Cost Network for Personal Computers." Evidently our readers found the authors' low-cost approach to networking intriguing in its simplicity.

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Excellent	801	805	809	813	817	821	825	829	833	837	841	845	849	853	857	861	865	869	873	877	881	885	889	893	897
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Fair	803	807	811	815	819	823	827	831	835	839	843	847	851	855	859	863	867	871	875	879	883	887	891	895	899
Poor	804	808	812	816	820	824	828	832	836	840	844	848	852	856	860	864	868	872	876	880	884	888	892	896	900

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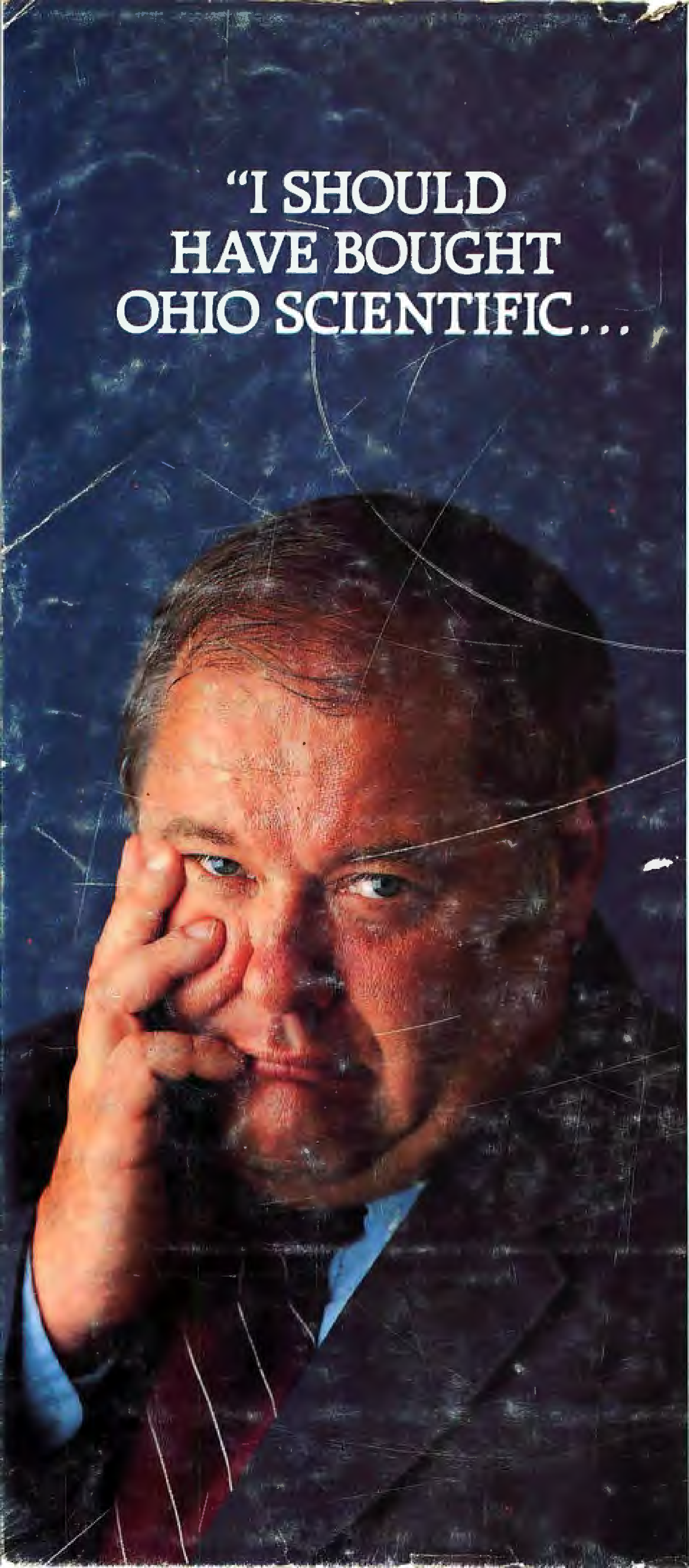

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